







CSD25480F3 SLPS578B - APRIL 2016 - REVISED FEBRUARY 2022

# CSD25480F3 -20-V P-Channel FemtoFET

#### 1 Features

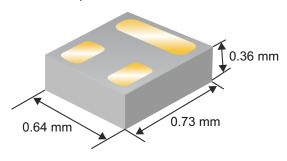
- Low on-resistance
- Ultra-low  $Q_g$  and  $Q_{gd}$
- Ultra-small footprint
  - 0.73 mm × 0.64 mm
- Low profile
  - 0.36-mm max height
- Integrated ESD protection diode
- Lead and halogen free
- RoHS compliant

# 2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

# 3 Description

This -20-V, 110-m $\Omega$ , P-Channel MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.



**Typical Part Dimensions** 

# **Product Summary**

T <sub>A</sub> = 25°	С	TYPICAL VA	UNIT		
V <sub>DS</sub>	Drain-to-Source Voltage	-20	-20		
Qg	Gate Charge Total (-4.5 V)	0.7	nC		
Q <sub>gd</sub>	Gate Charge Gate-to-Drain	0.10		nC	
		V <sub>GS</sub> = -1.8 V	420		
В	Drain-to-Source	V <sub>GS</sub> = -2.5 V	203	mΩ	
R <sub>DS(on)</sub>	On-Resistance	V <sub>GS</sub> = -4.5 V	132	11122	
		V <sub>GS</sub> = -8.0 V	110		
V <sub>GS(th)</sub>	Threshold Voltage	-0.95		V	

# **Device Information**(1)

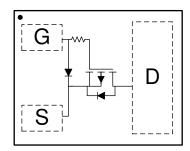
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD25480F3	3000		Femto	Tape
CSD25480F3T	250	7-Inch Reel	0.73-mm × 0.64-mm Land Grid Array (LGA)	and Reel

For all available packages, see the orderable addendum at the end of the data sheet.

#### **Absolute Maximum Ratings**

T <sub>A</sub> = 25	°C (unless otherwise stated)	VALUE	UNIT
V <sub>DS</sub>	Drain-to-Source Voltage	-20	V
V <sub>GS</sub>	Gate-to-Source Voltage	-12	V
I <sub>D</sub>	Continuous Drain Current <sup>(1)</sup>	-1.7	Α
I <sub>DM</sub>	Pulsed Drain Current <sup>(1)</sup> (2)	-10.6	Α
P <sub>D</sub>	Power Dissipation <sup>(1)</sup>	500	mW
	Human-Body Model (HBM)	4000	V
V <sub>(ESD)</sub>	Charged-Device Model (CDM)	2000	V
T <sub>J</sub> , T <sub>stg</sub>	Operating Junction, Storage Temperature	-55 to 150	°C

- Typical  $R_{\theta JA}$  = 255°C/W mounted on FR4 material with minimum Cu mounting area.
- Pulse duration ≤100 µs, duty cycle ≤1%.



**Top View** 



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Changes from Revision A (August 2017) to Revision B (February 2022)	Page
Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height	
Updated ultra-low profile image height from 0.35 mm to 0.36 mm	
Changed ultra-low profile image height from 0.35 mm to 0.36 mm	
Added FemtoFET Surface Mount Guide note	
Changes from Revision * (April 2016) to Revision A (August 2017)	Page
Added the Section 6.1 section in Section 6	<u> </u>
Added Recommended Minimum PCB Layout	
Updated the Section 7.3	

# **5 Specifications**

# **5.1 Electrical Characteristics**

T<sub>A</sub> = 25°C (unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC	CHARACTERISTICS					
BV <sub>DSS</sub>	Drain-to-source voltage	$V_{GS} = 0 \text{ V}, I_{DS} = -250 \mu\text{A}$	-20			V
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -16 V			-50	nA
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -12 V			-25	nA
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = -250 \mu A$	-0.70	-0.95	-1.20	V
		$V_{GS} = -1.8 \text{ V}, I_{DS} = -0.1 \text{ A}$		420	840	
l D	Dunin to account on marietanes	$V_{GS} = -2.5 \text{ V}, I_{DS} = -0.4 \text{ A}$		203	260	0
R <sub>DS(on)</sub>	Drain-to-source on-resistance	$V_{GS} = -4.5 \text{ V}, I_{DS} = -0.4 \text{ A}$		132	159	mΩ
		$V_{GS} = -8 \text{ V}, I_{DS} = -0.4 \text{ A}$		110	132	
9 <sub>fs</sub>	Transconductance	$V_{DS} = -10 \text{ V}, I_{DS} = -0.4 \text{ A}$		8.0		S
DYNAMI	C CHARACTERISTICS		,			
C <sub>iss</sub>	Input capacitance			119	155	pF
C <sub>oss</sub>	Output capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = -10 \text{ V},$ f = 1  MHz		48	62	pF
C <sub>rss</sub>	Reverse transfer capacitance	J - 1 WH 12		3.6	4.7	pF
$R_G$	Series gate resistance			16		Ω
Qg	Gate charge total (–4.5 V)		,	0.70	0.91	nC
Q <sub>gd</sub>	Gate charge gate-to-drain	V - 40 V I - 0 4 A		0.10		nC
Q <sub>gs</sub>	Gate charge gate-to-source	$V_{DS} = -10 \text{ V}, I_{DS} = -0.4 \text{ A}$		0.26		nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>			0.15		nC
Q <sub>oss</sub>	Output charge	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V		1.3		nC
t <sub>d(on)</sub>	Turnon delay time		,	9		ns
t <sub>r</sub>	Rise time	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V,		5		ns
t <sub>d(off)</sub>	Turnoff delay time	$I_{DS} = -0.4 \text{ A}, R_G = 10 \Omega$		13		ns
t <sub>f</sub>	Fall time			7		ns
DIODE C	CHARACTERISTICS				1	
V <sub>SD</sub>	Diode forward voltage	$I_{SD} = -0.4 \text{ A}, V_{GS} = 0 \text{ V}$		-0.78	-1.0	V
Q <sub>rr</sub>	Reverse recovery charge	V 40.V/1 0.4.0 1/1/4 100.1/		1.2		nC
t <sub>rr</sub>	Reverse recovery time	$V_{DS}$ = -10 V, I <sub>F</sub> = -0.4 A, di/dt = 100 A/ $\mu$ s		6.4		ns

## **5.2 Thermal Information**

 $T_A = 25$ °C (unless otherwise stated)

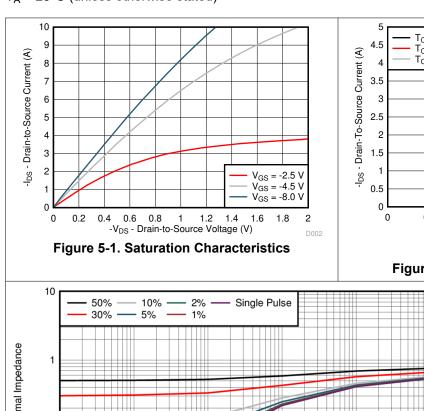
	THERMAL METRIC	TYPICAL VALUES	UNIT
D	Junction-to-ambient thermal resistance <sup>(1)</sup>	90	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	255	C/VV

 <sup>(1)</sup> Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz. (0.071-mm) thick Cu.
 (2) Device mounted on FR4 material with minimum Cu mounting area.



# **5.3 Typical MOSFET Characteristics**

T<sub>A</sub> = 25°C (unless otherwise stated)



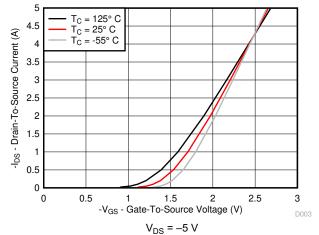


Figure 5-2. Transfer Characteristics

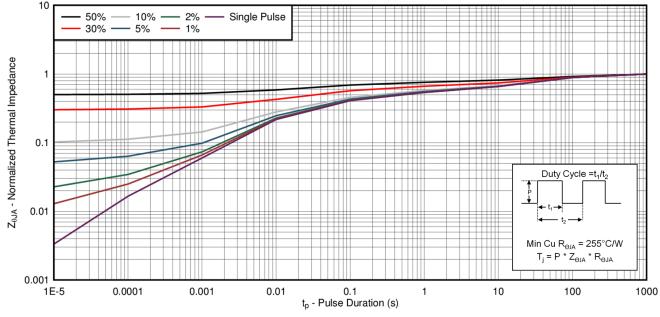
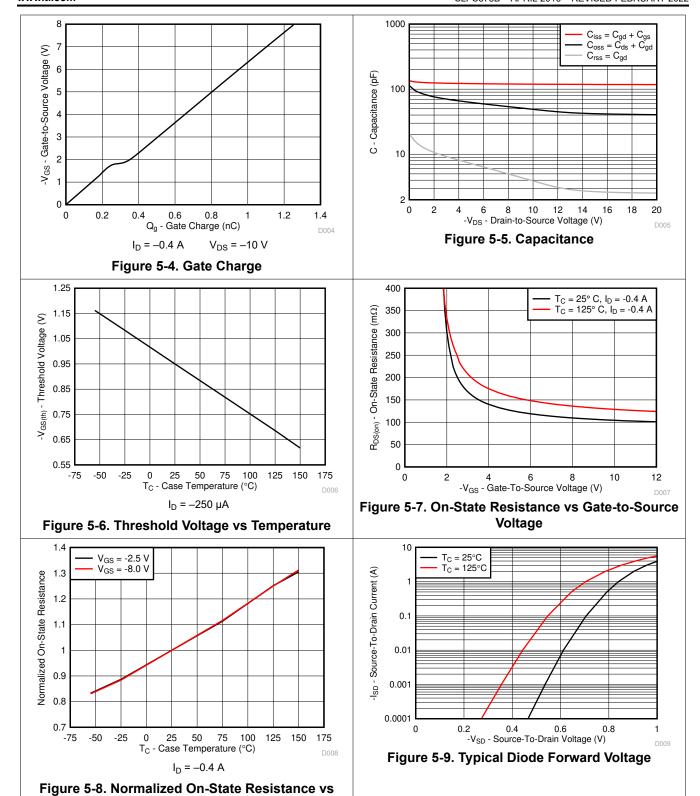


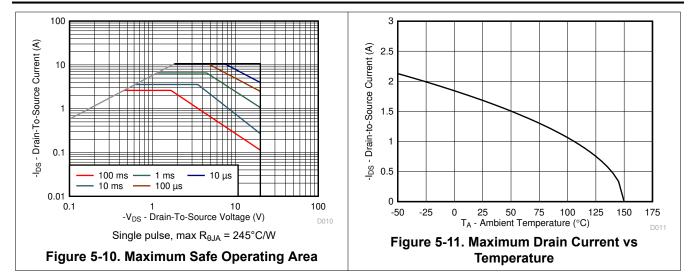
Figure 5-3. Transient Thermal Impedance

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**Temperature** 





# **6 Device and Documentation Support**

# 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

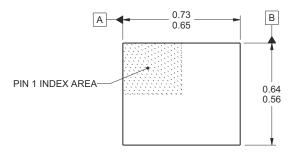
## **6.2 Trademarks**

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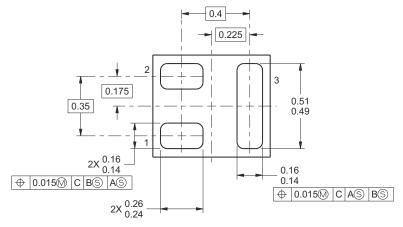
# 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

#### 7.1 Mechanical Dimensions







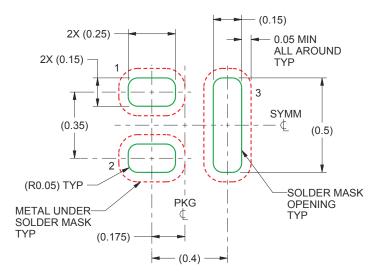
- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a lead-free solder land design.

Table 7-1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

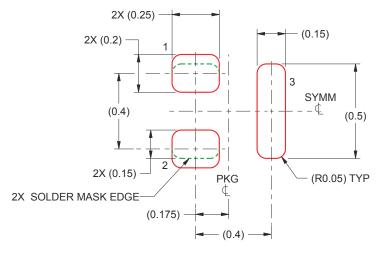
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# 7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see FemtoFET Surface Mount Guide (SLRA003D).

#### 7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
CSD25480F3	Active	Production	PICOSTAR (YJM)   3	3000   LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	4
CSD25480F3.B	Active	Production	PICOSTAR (YJM)   3	3000   LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	4
CSD25480F3T	Active	Production	PICOSTAR (YJM)   3	250   SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	4
CSD25480F3T.B	Active	Production	PICOSTAR (YJM)   3	250   SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	4

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	CSD25480F3	PICOSTAF	YJM	3	3000	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
L	CSD25480F3T	PICOSTAF	YJM	3	250	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2

**PACKAGE MATERIALS INFORMATION** 

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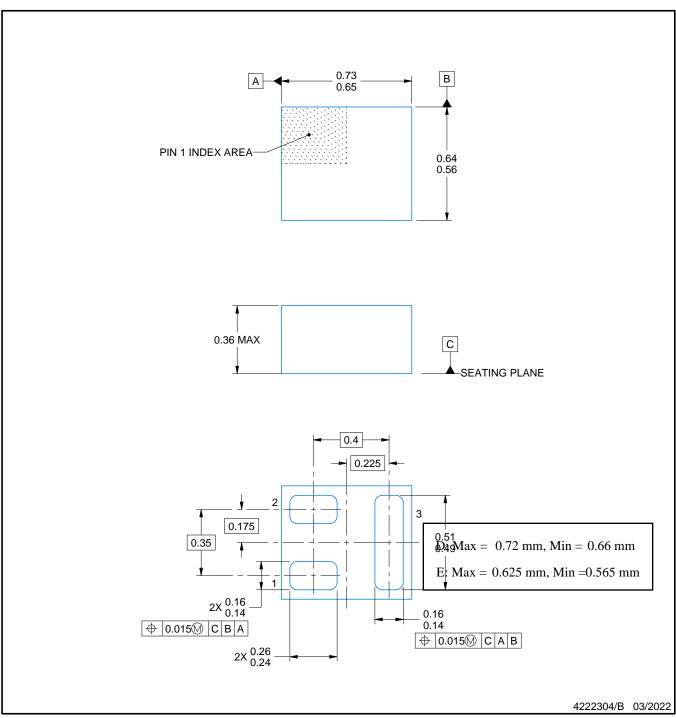


#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25480F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD25480F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0



PicoStar™



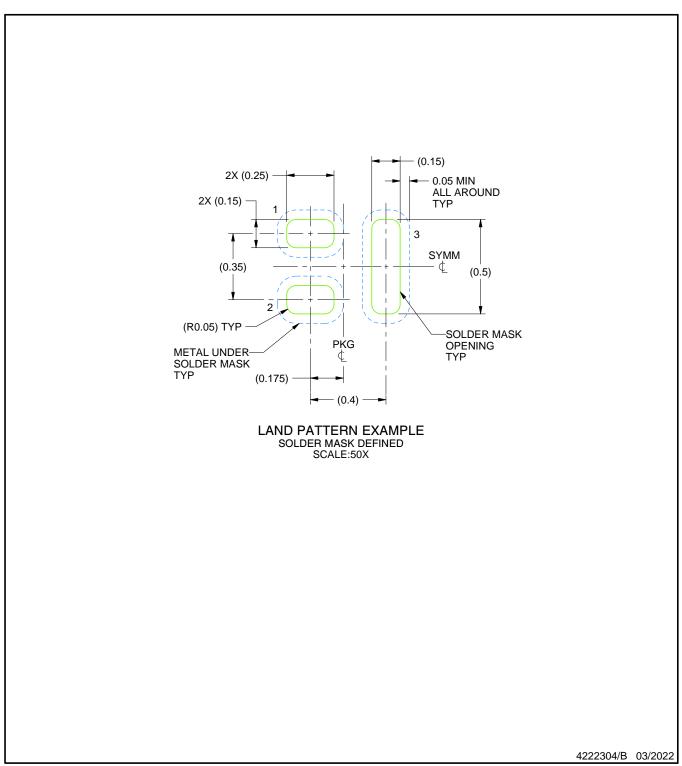
#### NOTES:

PicoStar is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
  2. This drawing is subject to change without notice.
- This drawing is subject to charge without notice.
   This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.



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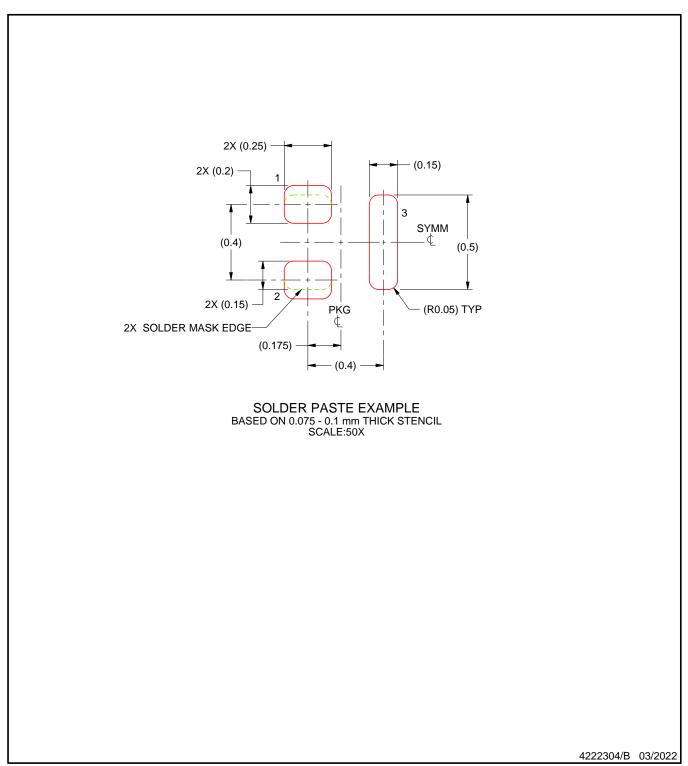


NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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