

P-Channel NexFET™ Power MOSFET

Check for Samples: [CSD25213W10](#)

FEATURES

- Ultra Low Qg and Qgd
- Small Footprint 1mm x 1mm
- Low Profile 0.62mm Height
- Pb Free
- Gate-Source Voltage Clamp
- Gate ESD Protection
- RoHS Compliant
- Halogen Free

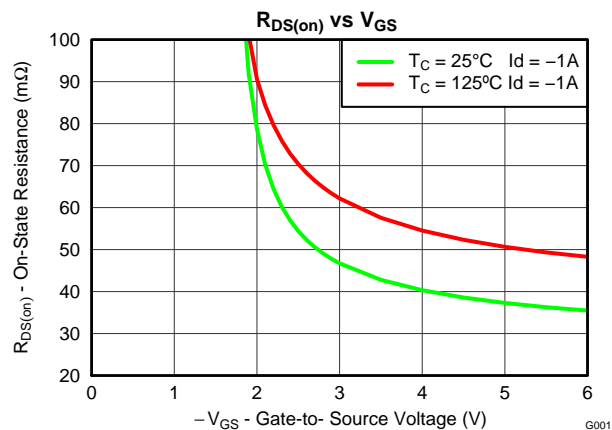
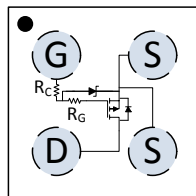
APPLICATIONS

- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

Top View



PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	-20	V
Q _g	Gate Charge Total (4.5V)	2.2	nC
Q _{gd}	Gate Charge Gate to Drain	0.14	nC
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = -2.5V	54 mΩ
		V _{GS} = -4.5V	39 mΩ
V _{GS(th)}	Threshold Voltage	-0.85	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD25213W10	1 x 1 Wafer Level Package	7-inch reel	3000	Tape and Reel

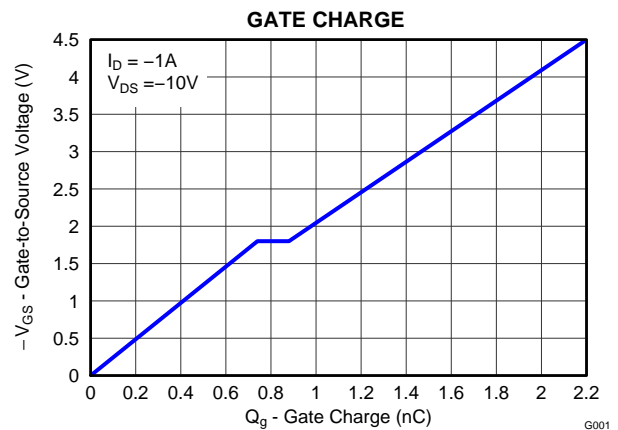
ABSOLUTE MAXIMUM RATINGS

T _A = 25°C unless otherwise stated		VALUE	UNIT
V _{DS}	Drain to Source Voltage	-20	V
V _{GS}	Gate to Source Voltage	-6.0	V
I _D	Continuous Drain Current, T _A = 25°C ⁽¹⁾	-1.6	A
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	-16	A
I _G	Continuous Gate Clamp Current ⁽³⁾	-5	mA
P _D	Power Dissipation ⁽¹⁾	1	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

(1) R_{θJA} = 75°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300μs, duty cycle ≤2%

(3) Limited by gate resistance.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2013, Texas Instruments Incorporated



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = −250μA	−20			V
BV _{GSS}	Gate to Source Voltage;	V _{DS} = 0V, I _G = −250μA	−6.0			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = −10V	−1			μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = −6V	−100			nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = −250μA	−0.60	−0.85	−1.10	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = −2.5V, I _D = −1A		54	67	mΩ
		V _{GS} = −4.5V, I _D = −1A		39	47	mΩ
g _{fs}	Transconductance	V _{DS} = −10V, I _D = −1A		6.2		S
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = −10V, f = 10kHz		368	478	pF
C _{OSS}	Output Capacitance			148	192	pF
C _{RSS}	Reverse Transfer Capacitance			7.8	10.1	pF
R _G	Series Gate Resistance			20		Ω
R _C	Series Clamp Resistance			5000		Ω
Q _g	Gate Charge Total (−4.5V)	V _{DS} = −10V, I _D = −1A		2.2	2.9	nC
Q _{gd}	Gate Charge Gate to Drain			0.14		nC
Q _{gs}	Gate Charge Gate to Source			0.74		nC
Q _{g(th)}	Gate Charge at V _{th}			0.43		nC
Q _{OSS}	Output Charge		V _{DS} = −10V, V _{GS} = 0V		2.5	
t _{d(on)}	Turn On Delay Time	V _{DS} = −10V, V _{GS} = −2.5V, I _D = −1A R _G = 10Ω		510		ns
t _r	Rise Time			520		ns
t _{d(off)}	Turn Off Delay Time			1000		ns
t _f	Fall Time			970		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _S = −1A, V _{GS} = 0V		−0.77	−1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = −10V, I _F = −1A, di/dt = 200A/μs		4.0		nC
t _{rr}	Reverse Recovery Time	V _{DS} = −10V, I _F = −1A, di/dt = 200A/μs		11		ns

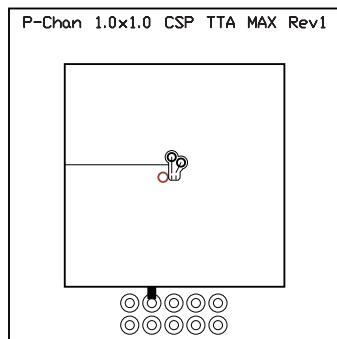
THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

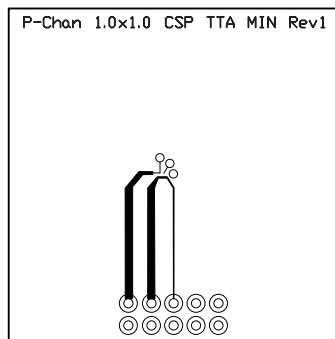
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to Ambient Thermal Resistance ⁽¹⁾		75		$^\circ\text{C}/\text{W}$
	Junction to Ambient Thermal Resistance ⁽²⁾		265		$^\circ\text{C}/\text{W}$

(1) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.



Max $R_{\theta JA} = 90^{\circ}\text{C/W}$
when mounted on
1inch² of 2 oz. Cu.



Max $R_{\theta JA} = 333^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

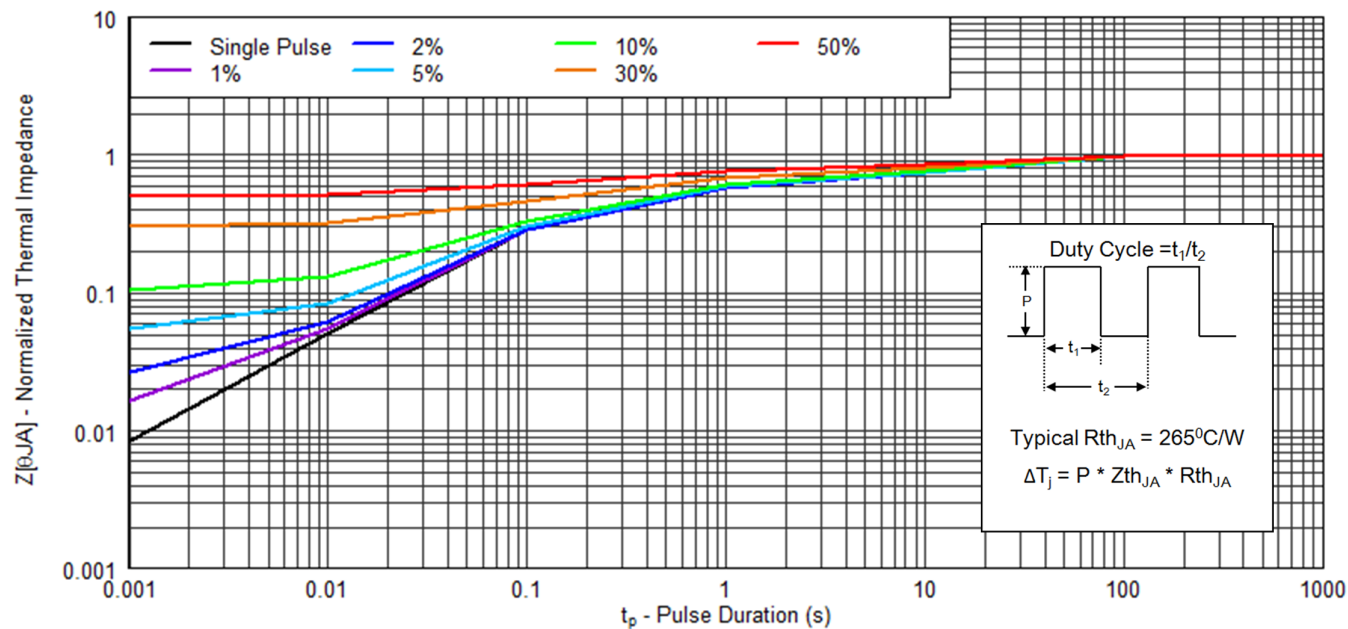


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

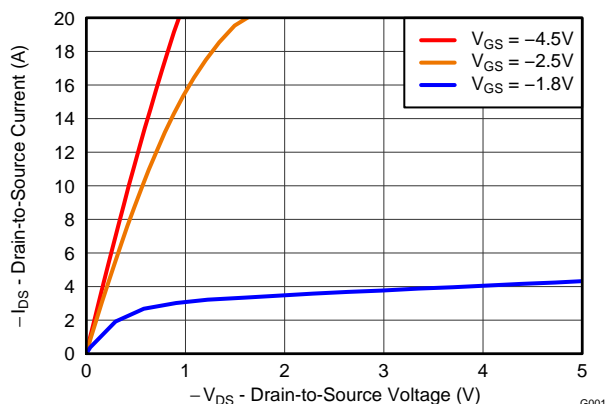


Figure 2. Saturation Characteristics

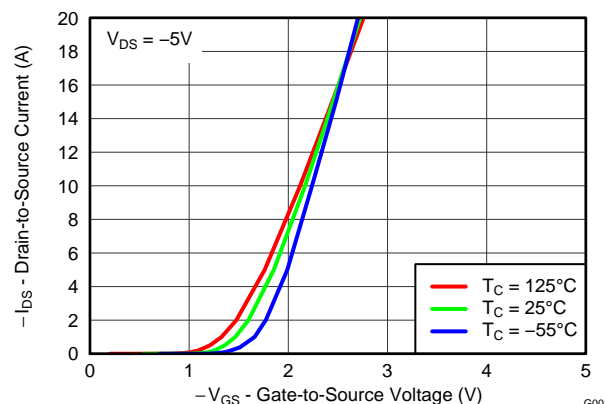


Figure 3. Transfer Characteristics

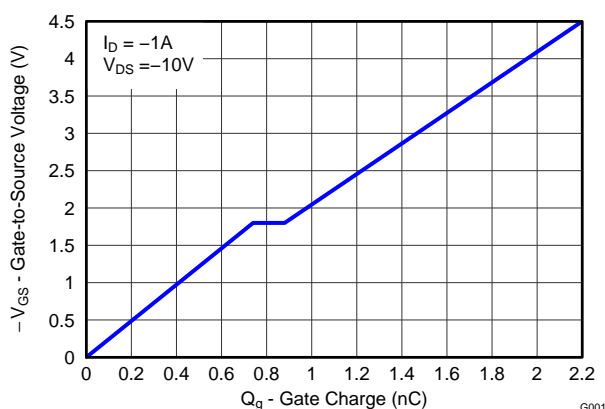


Figure 4. Gate Charge

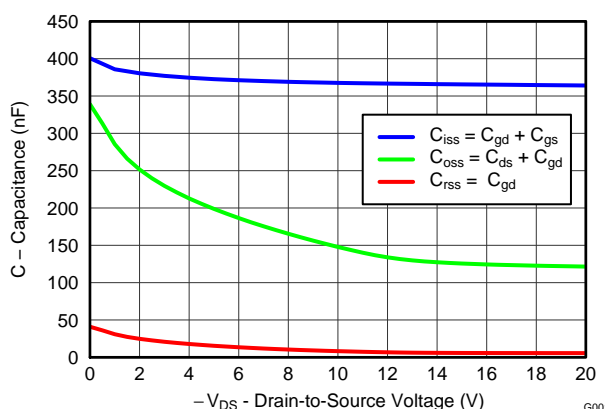


Figure 5. Capacitance

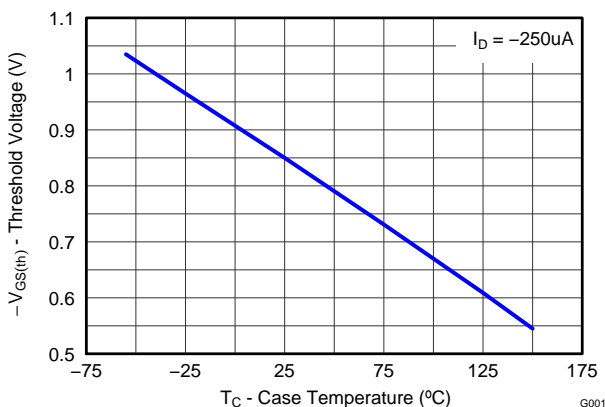


Figure 6. Threshold Voltage vs. Temperature

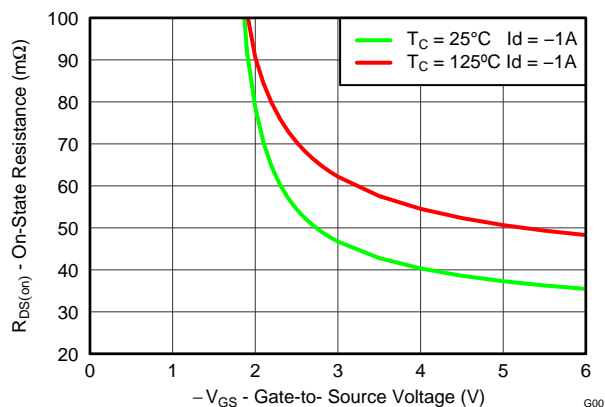


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

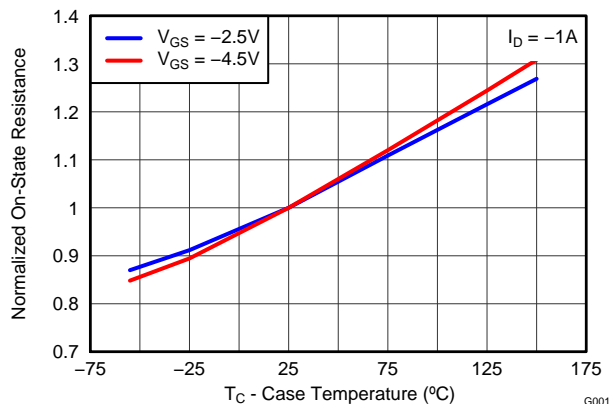


Figure 8. Normalized On-State Resistance vs. Temperature

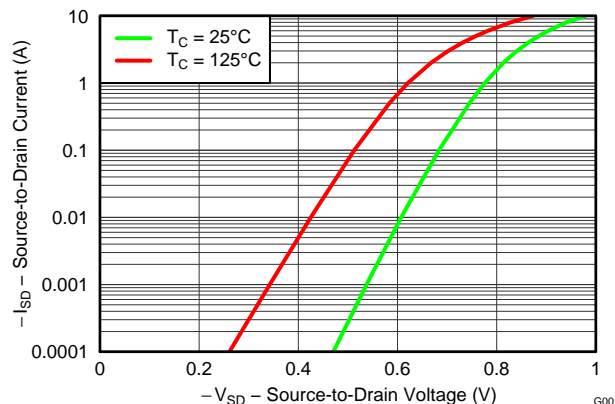


Figure 9. Typical Diode Forward Voltage

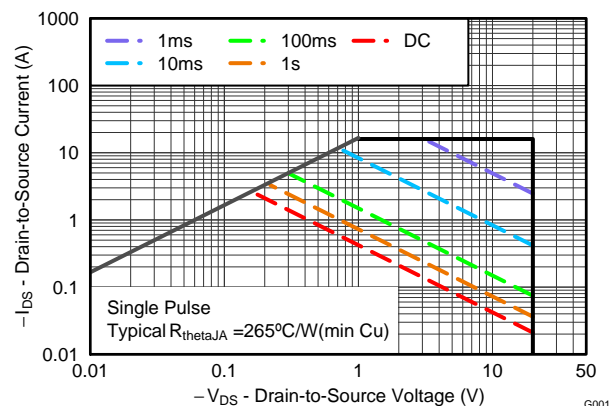


Figure 10. Maximum Safe Operating Area

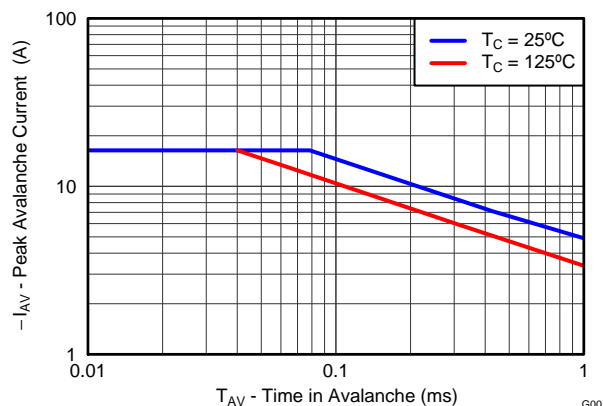


Figure 11. Single Pulse Unclamped Inductive Switching

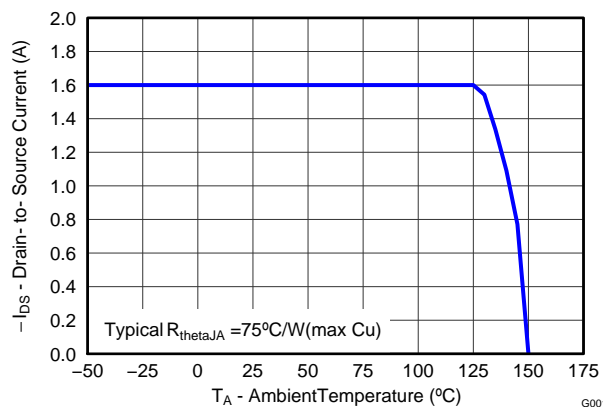
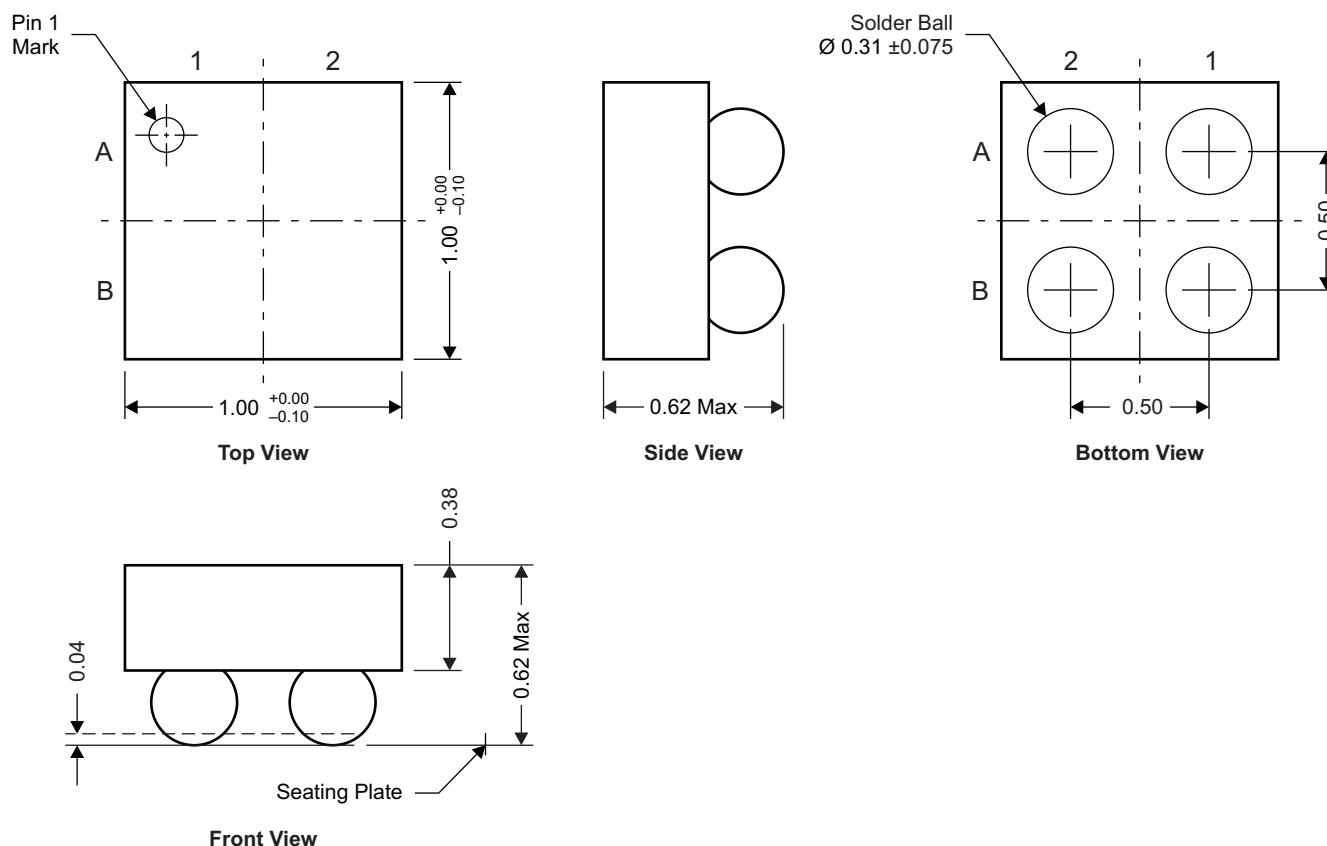


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD25213W10 Package Dimensions



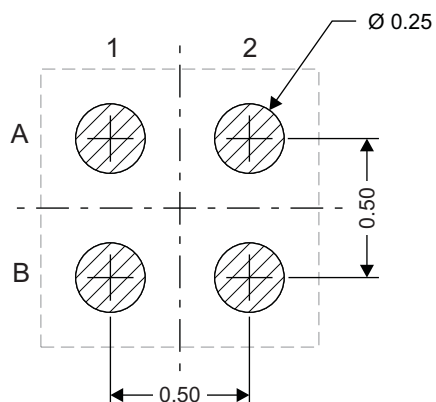
NOTE: All dimensions are in mm (unless otherwise specified)

M0151-01

Pin Configuration Table

POSITION	DESIGNATION
A1	Gate
B1	Drain
A2, B2	Source

Land Pattern Recommendation



M0152-01

NOTE: All dimensions are in mm (unless otherwise specified)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD25213W10	Active	Production	DSBGA (YZB) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	213
CSD25213W10.B	Active	Production	DSBGA (YZB) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	213

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

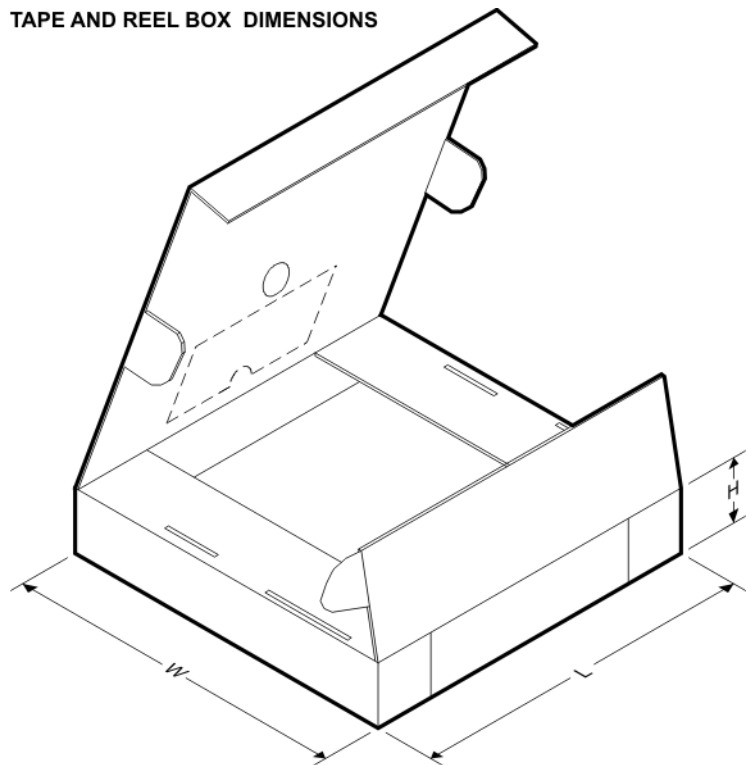
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25213W10	DSBGA	YZB	4	3000	180.0	8.4	1.06	1.06	0.69	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25213W10	DSBGA	YZB	4	3000	182.0	182.0	20.0

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated