



# CSD23203W –8-V P-Channel NexFET™ Power MOSFET

## 1 Features

- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low  $R_{DS(on)}$
- Small Footprint
- Low Profile 0.62-mm Height
- Lead Free
- RoHS Compliant
- Halogen Free
- CSP 1-mm × 1.5-mm Wafer Level Package

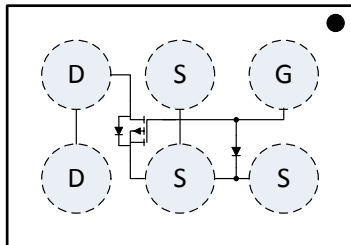
## 2 Applications

- Battery Management
- Load Switch
- Battery Protection

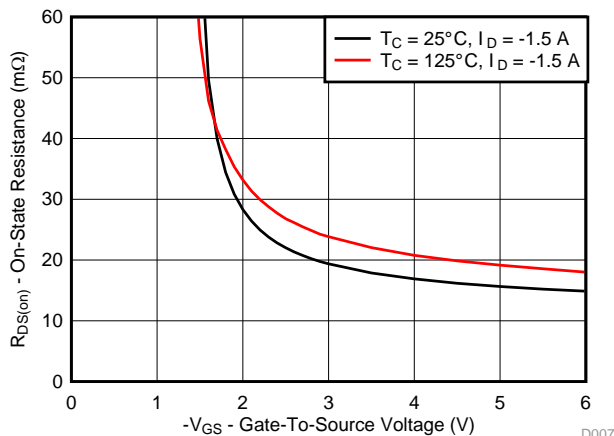
## 3 Description

This 16.2-m $\Omega$ , –8-V, P-Channel device is designed to deliver the lowest on-resistance and gate charge in a small 1 × 1.5 mm outline with excellent thermal characteristics in an ultra-low profile.

Top View

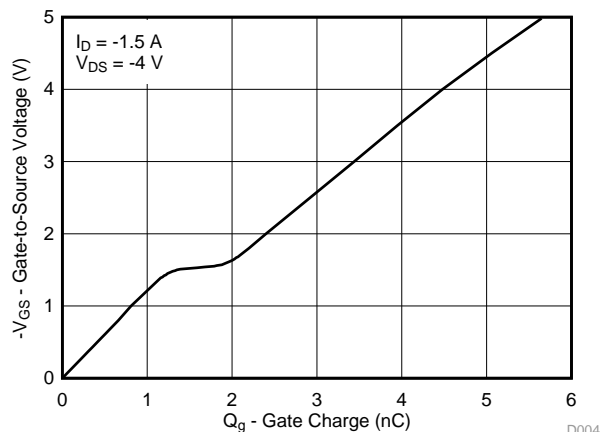


$R_{DS(on)}$  vs  $V_{GS}$



D007

Gate Charge



D004

### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	–8		V
$Q_g$	Gate Charge Total (–4.5 V)	4.9		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	0.6		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = -1.8\text{ V}$	35	m $\Omega$
		$V_{GS} = -2.5\text{ V}$	22	m $\Omega$
		$V_{GS} = -4.5\text{ V}$	16.2	m $\Omega$
$V_{GS(th)}$	Voltage Threshold	–0.8		V

### Device Information<sup>(1)</sup>

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD23203W	3000	7-Inch Reel	1.00-mm × 1.50-mm Wafer Level Package	Tape and Reel
CSD23203WT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	–8	V
$V_{GS}$	Gate-to-Source Voltage	–6	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	–3	A
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	–54	A
$P_D$	Power Dissipation	0.75	W
$T_J, T_{stg}$	Operating Junction, Storage Temperature	–55 to 150	$^\circ\text{C}$

(1) Device operating at a temperature of 105 $^\circ\text{C}$ .

(2) Typ  $R_{\theta JA} = 170^\circ\text{C/W}$ , pulse width  $\leq 100\text{ }\mu\text{s}$ , duty cycle  $\leq 1\%$ .



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Original (December 2014) to Revision A</b>	<b>Page</b>
• Corrected MOSFET body tie in <i>Top View</i> image. ....	<b>1</b>
• Added <i>Receiving Notification of Documentation Updates</i> and <i>Community Resources</i> sections .....	<b>7</b>

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-to-source voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = −250 μA	−8			V
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = −6.4 V			−1	μA
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = −6 V			−100	nA
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = −250 μA	−0.6	−0.8	−1.1	V
R <sub>DS(on)</sub>	Drain-to-source on-resistance	V <sub>GS</sub> = −1.8 V, I <sub>D</sub> = −1.5 A	35		53	mΩ
		V <sub>GS</sub> = −2.5 V, I <sub>D</sub> = −1.5 A	22		26.5	mΩ
		V <sub>GS</sub> = −4.5 V, I <sub>D</sub> = −1.5 A	16.2		19.4	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = −0.8 V, I <sub>D</sub> = −1.5 A	14			S
DYNAMIC CHARACTERISTICS						
C <sub>ISS</sub>	Input capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = −4 V, f = 1 MHz	703		914	pF
C <sub>OSS</sub>	Output capacitance		391		508	pF
C <sub>RSS</sub>	Reverse transfer capacitance		133		172	pF
Q <sub>g</sub>	Gate charge total (−4.5 V)	V <sub>DS</sub> = −4 V, I <sub>D</sub> = −1.5 A	4.9		6.3	nC
Q <sub>gd</sub>	Gate charge gate-to-drain		0.6			nC
Q <sub>gs</sub>	Gate charge gate-to-source		1.3			nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>		0.6			nC
Q <sub>OSS</sub>	Output charge	V <sub>DS</sub> = −4 V, V <sub>GS</sub> = 0 V	1.9			nC
t <sub>d(on)</sub>	Turnon delay time	V <sub>DS</sub> = −4 V, V <sub>GS</sub> = −4.5 V, I <sub>D</sub> = −1.5 A R <sub>G</sub> = 10 Ω	14			ns
t <sub>r</sub>	Rise time		12			ns
t <sub>d(off)</sub>	Turnoff delay time		58			ns
t <sub>f</sub>	Fall time		27			ns
DIODE CHARACTERISTICS						
V <sub>SD</sub>	Diode forward voltage	I <sub>S</sub> = −1.5 A, V <sub>GS</sub> = 0 V	−0.75		−1	V
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DS</sub> = −4.7 V, I <sub>F</sub> = −1.5 A	6.1			nC
t <sub>rr</sub>	Reverse recovery time	di/dt = 100 A/μs	21			ns

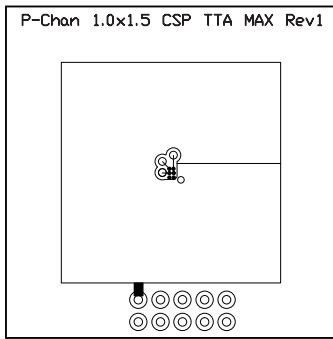
### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>		170		$^\circ\text{C}/\text{W}$
	Junction-to-ambient thermal resistance <sup>(2)</sup>		55		

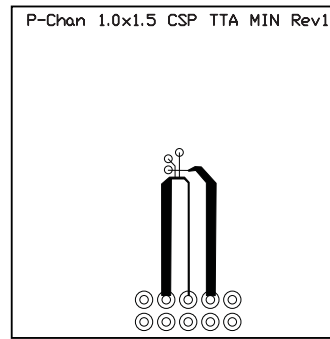
(1) Device mounted on FR4 material with minimum Cu mounting area.

(2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.



M0155-01

Typ  $R_{\theta JA} = 55^{\circ}\text{C/W}$   
when mounted on  
1 in<sup>2</sup> of 2-oz Cu.



M0156-01

Typ  $R_{\theta JA} = 170^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of  
2-oz Cu.

### 5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$  (unless otherwise stated)

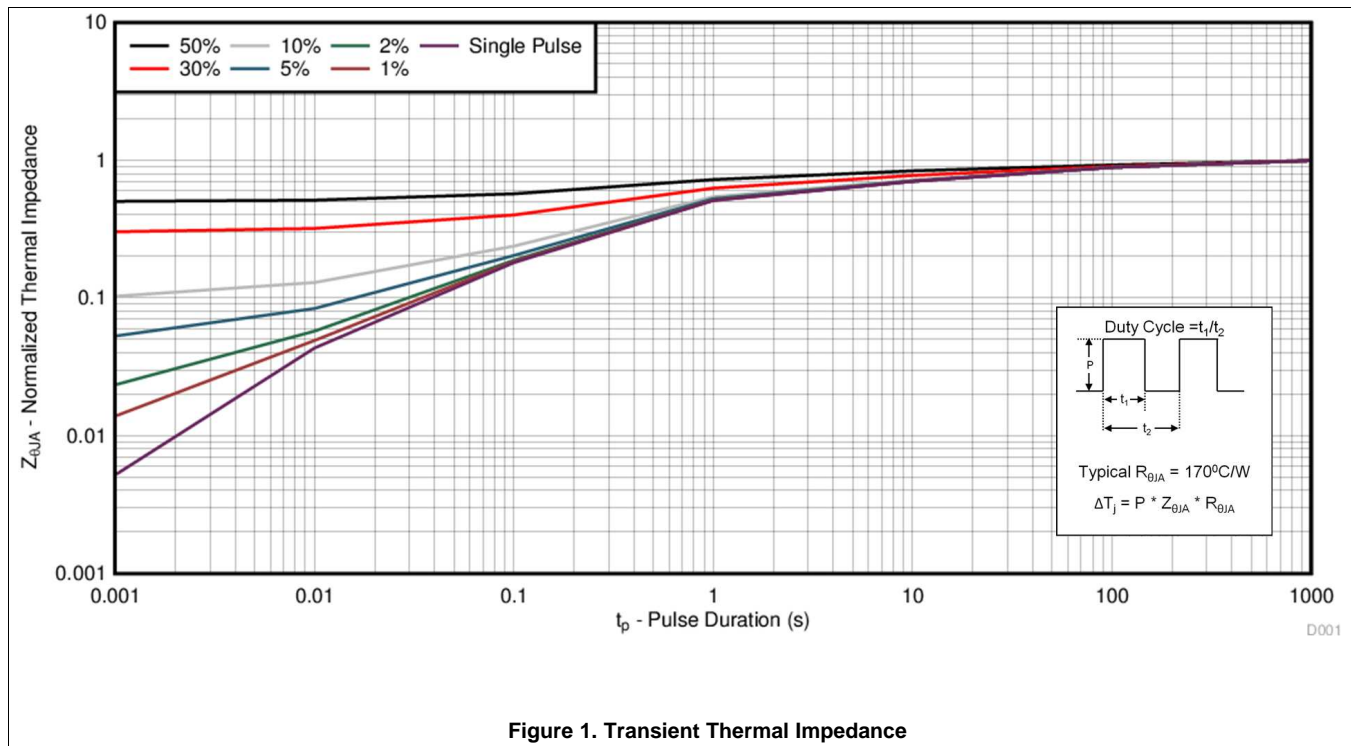


Figure 1. Transient Thermal Impedance

## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

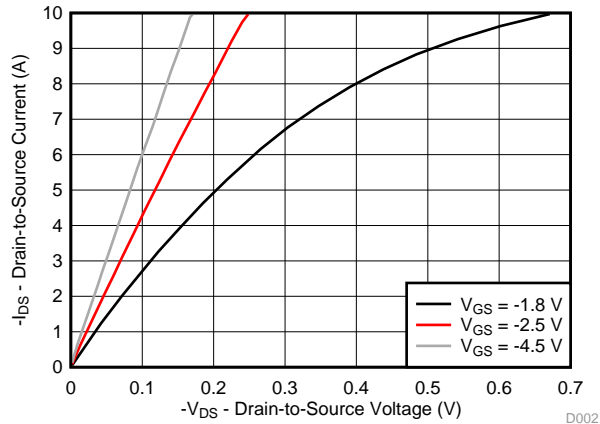


Figure 2. Saturation Characteristics

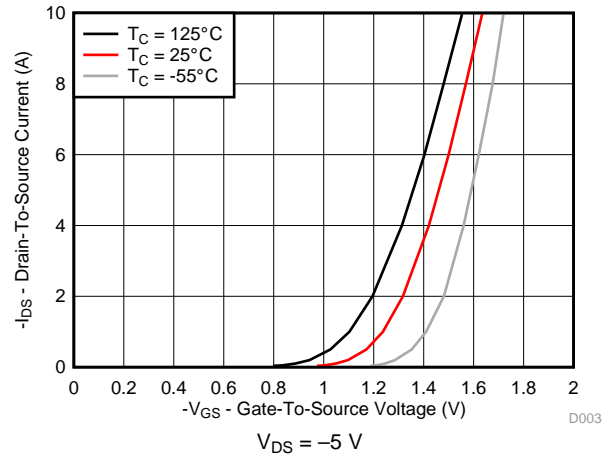


Figure 3. Transfer Characteristics

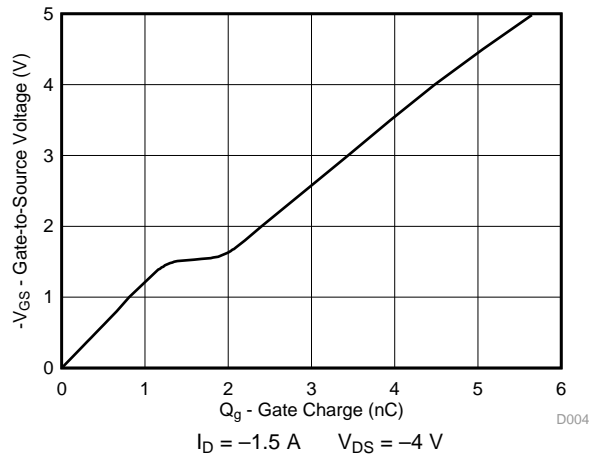


Figure 4. Gate Charge

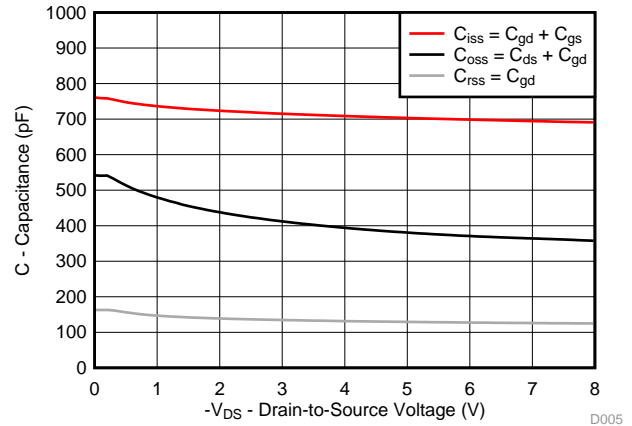


Figure 5. Capacitance

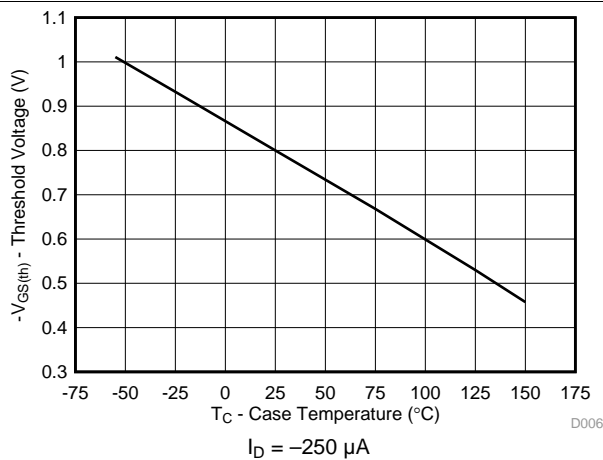


Figure 6. Threshold Voltage vs Temperature

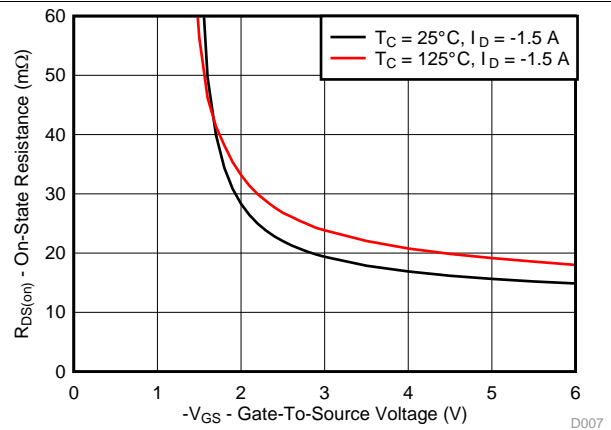


Figure 7. On-State Resistance vs Gate-to-Source Voltage

## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

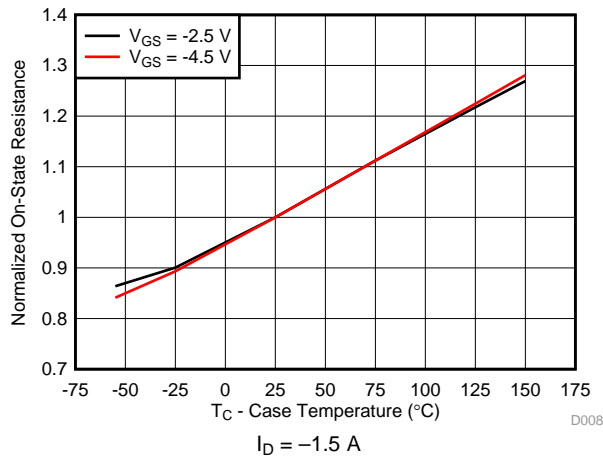


Figure 8. Normalized On-State Resistance vs Temperature

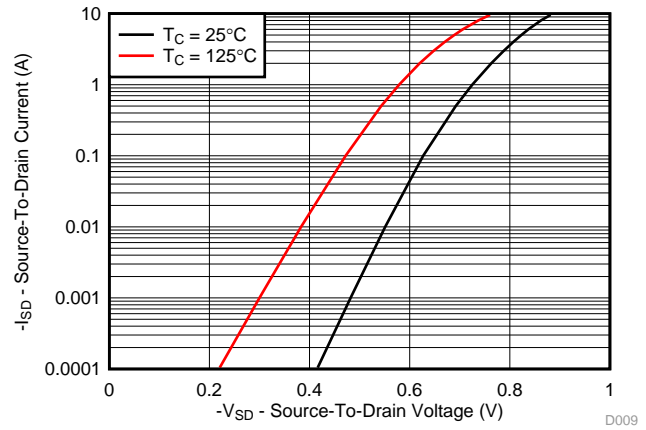


Figure 9. Typical Diode Forward Voltage

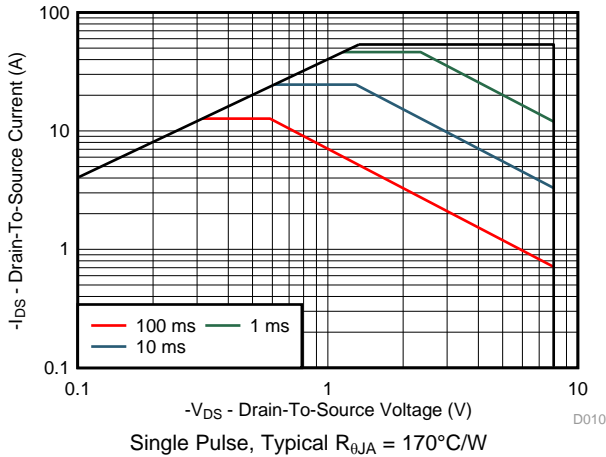


Figure 10. Maximum Safe Operating Area

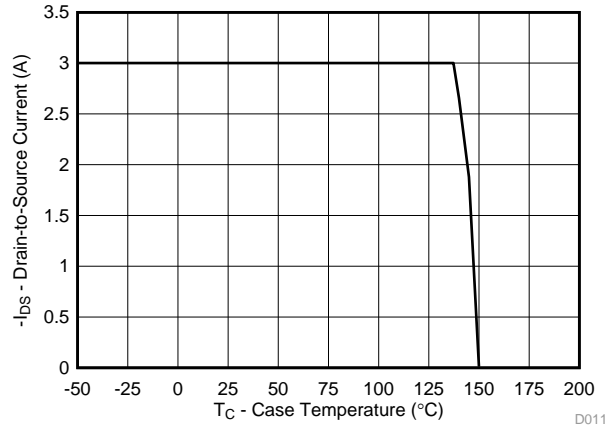


Figure 11. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

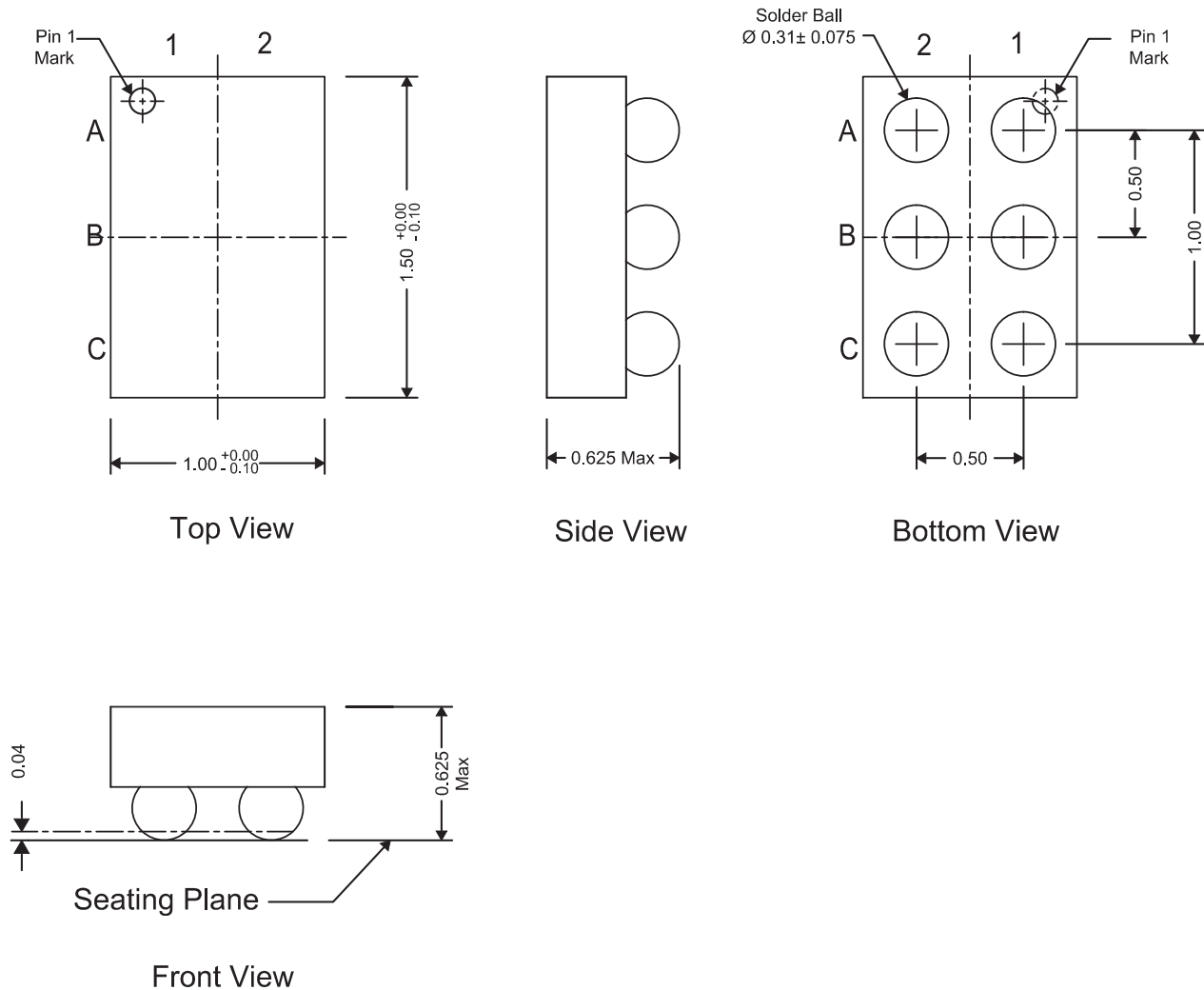
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 CSD23203W Package Dimensions



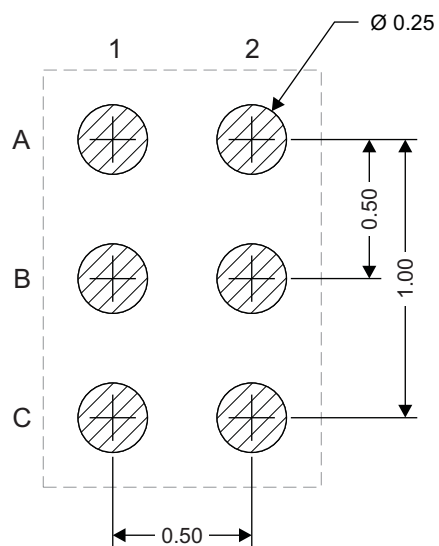
NOTE: All dimensions are in mm (unless otherwise specified).

**Table 1. Pinout**

POSITION	DESIGNATION
C1, C2	Drain
A1	Gate
A2, B1, B2	Source



## 7.2 Land Pattern Recommendation



M0158-01

NOTE: All dimensions are in mm (unless otherwise specified).

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23203W	ACTIVE	DSBGA	YZC	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		23203	<a href="#">Samples</a>
CSD23203WT	ACTIVE	DSBGA	YZC	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	23203	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD23203W</a>	Active	Production	DSBGA (YZC)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	23203
CSD23203W.B	Active	Production	DSBGA (YZC)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	23203
<a href="#">CSD23203WT</a>	Active	Production	DSBGA (YZC)   6	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	23203
CSD23203WT.B	Active	Production	DSBGA (YZC)   6	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	23203

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD23203W	DSBGA	YZC	6	3000	180.0	8.4	1.18	1.68	0.83	4.0	8.0	Q1
CSD23203WT	DSBGA	YZC	6	250	180.0	8.4	1.18	1.68	0.83	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD23203W	DSBGA	YZC	6	3000	182.0	182.0	20.0
CSD23203WT	DSBGA	YZC	6	250	182.0	182.0	20.0

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