











CSD22206W

SLPS689 - MAY 2017

## CSD22206W -8-V P-Channel NexFET™ Power MOSFET

#### **Features**

- Ultra-Low Resistance
- Small Footprint 1.5 mm x 1.5 mm
- Lead Free
- Gate ESD Protection
- **RoHS Compliant**
- Halogen Free
- Gate-Source Voltage Clamp

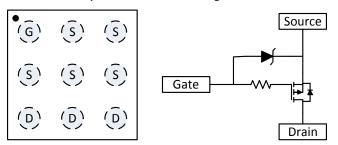
## Applications

- Load Switch Applications
- **Battery Management**
- **Battery Protection**

#### Description 3

This -8-V, 4.7-m $\Omega$ , 1.5-mm × 1.5-mm device is designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Low on resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

#### **Top View and Circuit Configuration**



### **Product Summary**

$T_A = 25^{\circ}C$		TYPICAL VA	UNIT	
$V_{DS}$	Drain-to-Source Voltage	-8		V
$Q_g$	Gate Charge Total (-4.5 V)	11.2		nC
$Q_{gd}$	Gate Charge Gate-to-Drain		nC	
D	Drain-to-Source On Resistance	$V_{GS} = -2.5 \text{ V}$	6.8	mΩ
R <sub>DS(on)</sub>	Drain-to-Source On Resistance	$V_{GS} = -4.5 \text{ V}$	4.7	11177
V <sub>GS(th)</sub>	Threshold Voltage	-0.7	V	

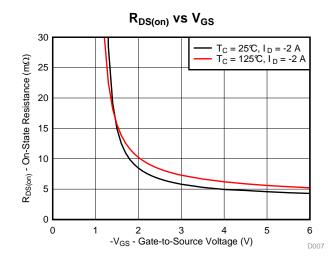
#### **Device Information**

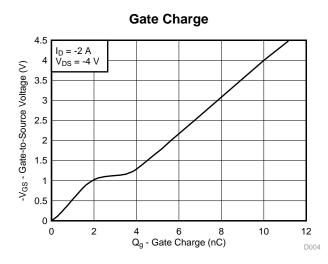
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD22206W	3000		1.50-mm × 1.50-mm	Tape
CSD22206WT	250	7-Inch Reel	Wafer BGA Package	and Reel

#### **Absolute Maximum Ratings**

T <sub>A</sub> = 2	5°C	VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	-8	V
$V_{\text{GS}}$	Gate-to-Source Voltage	-6	V
	Continuous Drain Current <sup>(1)</sup>	<b>-</b> 5	Α
I <sub>D</sub>	Pulsed Drain Current <sup>(2)</sup>	-108	Α
P <sub>D</sub>	Power Dissipation	1.7	W
T <sub>J</sub> , T <sub>stg</sub>	Operating Junction, Storage Temperature	-55 to 150	°C

- (1) Device operating at a temperature of 105°C.
- (2) Typ  $R_{\theta,IA} = 75^{\circ}C/W$ , mounted on FR4 material with maximum Cu mounting area, pulse width ≤ 100 μs, duty cycle ≤ 1%.









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## 4 Revision History

DATE	REVISION	NOTES
May 2017	*	Initial release.

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# 5 Specifications

#### 5.1 Electrical Characteristics

 $T_A = 25^{\circ}C$  (unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC	CHARACTERISTICS					
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0 \text{ V}, I_{DS} = -250 \mu\text{A}$	-8			V
$BV_GSS$	Gate-to-source voltage	$V_{DS} = 0 \ V, \ I_G = -250 \ \mu A$	-6			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0 \text{ V}, V_{DS} = -6.4 \text{ V}$			-1	μΑ
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0 V$ , $V_{GS} = -6 V$			-100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = -250 \mu A$	-0.4	-0.7	-1.05	V
D	Drain to course on registence	$V_{GS} = -2.5 \text{ V}, I_{DS} = -2 \text{ A}$		6.8	9.1	mΩ
R <sub>DS(on)</sub>	Drain-to-source on resistance	$V_{GS} = -4.5 \text{ V}, I_{DS} = -2 \text{ A}$		4.7	5.7	11122
g <sub>fs</sub>	Transconductance	$V_{DS} = -0.8 \text{ V}, I_{DS} = -2 \text{ A}$		20		S
DYNAMI	C CHARACTERISTICS					
C <sub>ISS</sub>	Input capacitance			1750	2275	pF
Coss	Output capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = -4 \text{ V},$ f = 1  MHz		960	1250	pF
C <sub>RSS</sub>	Reverse transfer capacitance	J = 1 1VII 12		340	440	pF
$R_{G}$	Series gate resistance			30		Ω
Qg	Gate charge total (-4.5 V)			11.2	14.6	nC
$Q_{gd}$	Gate charge gate-to-drain	$V_{DS} = -4 V$ ,		1.8		nC
Q <sub>gs</sub>	Gate charge gate-to-source	$I_D = -2 A$		2.1		nC
Q <sub>g(th)</sub>	Gate charge at Vth			1.3		nC
Q <sub>OSS</sub>	Output charge	$V_{DS} = -4 \text{ V}, V_{GS} = 0 \text{ V}$		7.2		nC
t <sub>d(on)</sub>	Turnon delay time			37		ns
t <sub>r</sub>	Rise time	$V_{DS} = -4 \text{ V}, V_{GS} = -4.5 \text{ V},$		17		ns
t <sub>d(off)</sub>	Turnoff delay time	$I_{DS} = -2 \text{ A}, R_G = 0 \Omega$		118		ns
t <sub>f</sub>	Fall time			45		ns
DIODE C	CHARACTERISTICS				<del></del>	
V <sub>SD</sub>	Diode forward voltage	$I_{DS} = -2 \text{ A}, V_{GS} = 0 \text{ V}$	-	-0.69	-1.0	
Q <sub>rr</sub>	Reverse recovery charge	$V_{DS} = -4 \text{ V}, I_F = -1 \text{ A},$		24		nC
t <sub>rr</sub>	Reverse recovery time	di/dt = 200 A/μs		59		ns

#### 5.2 Thermal Information

 $T_A = 25^{\circ}C$  (unless otherwise stated)

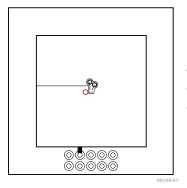
,,	THERMAL METRIC	TYPICAL VALUES	UNIT
D	Junction-to-ambient thermal resistance <sup>(1)</sup>	75	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	230	- C/VV

(1) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

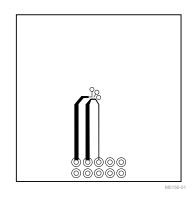
(2) Device mounted on FR4 material with minimum Cu mounting area.

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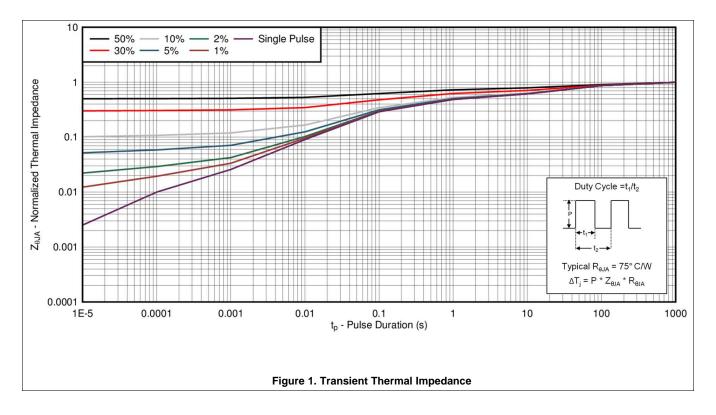
Typ  $R_{\theta JA} = 75^{\circ}C/W$ when mounted on 1 in<sup>2</sup> of 2-oz Cu.



Typ  $R_{\theta JA} = 230^{\circ}\text{C/W}$  when mounted on minimum pad area of 2-oz Cu.

## 5.3 Typical MOSFET Characteristics

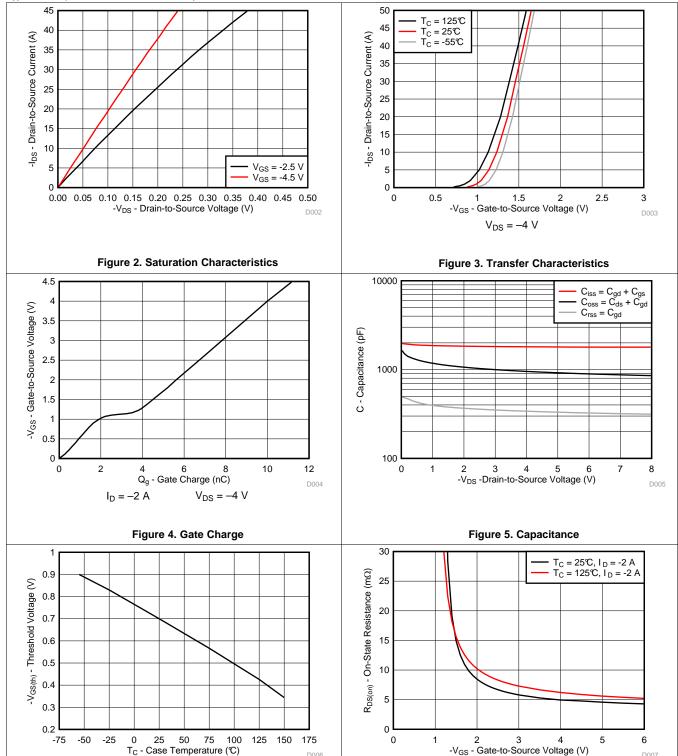
 $T_A = 25$ °C (unless otherwise stated)





#### **Typical MOSFET Characteristics (continued)**

 $T_A = 25$ °C (unless otherwise stated)



 $I_D = -250 \mu A$ 

Figure 6. Threshold Voltage vs Temperature

Figure 7. On-State Resistance vs Gate-to-Source Voltage

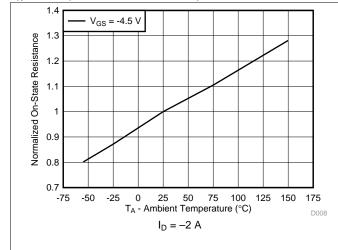
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## **Typical MOSFET Characteristics (continued)**

 $T_A = 25$ °C (unless otherwise stated)



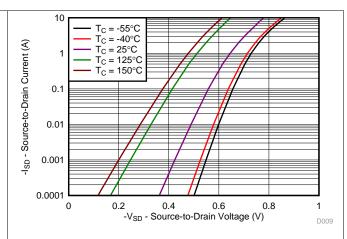


Figure 8. Normalized On-State Resistance vs Temperature

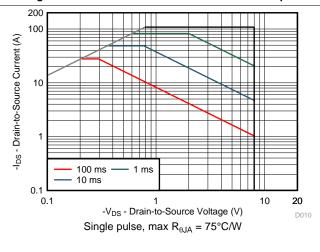


Figure 10. Maximum Safe Operating Area

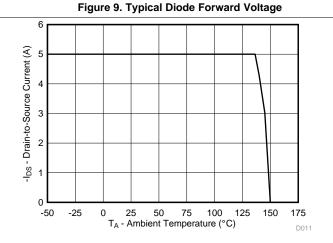


Figure 11. Maximum Drain Current vs Temperature



#### 6 Device and Documentation Support

#### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 6.3 Trademarks

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#### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 6.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

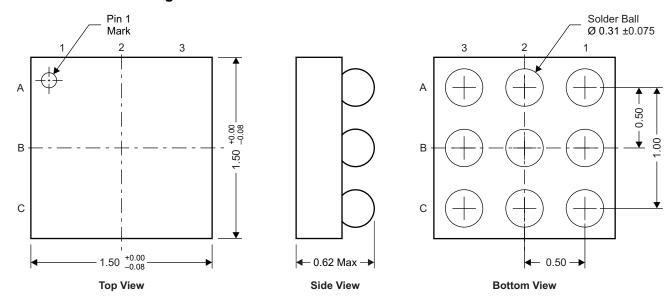
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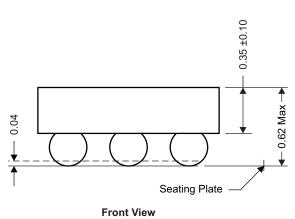
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# 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 7.1 CSD22206W Package Dimensions





M0171-01

NOTE: All dimensions are in mm (unless otherwise specified).

Table 1. Pinout

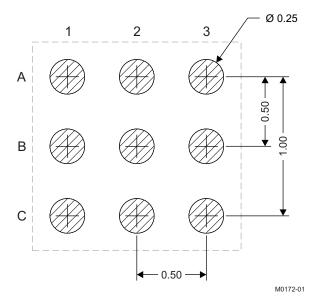
POSITION	DESIGNATION
A1	Gate
A2, A3, B1, B2, B3	Source
C1, C2, C3	Drain

Product Folder Links: CSD22206W

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## 7.2 Recommended Land Pattern



NOTE: All dimensions are in mm (unless otherwise specified).

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
CSD22206W	Active	Production	DSBGA (YZF)   9	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	22206
CSD22206W.B	Active	Production	DSBGA (YZF)   9	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	22206
CSD22206WT	Active	Production	DSBGA (YZF)   9	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	22206
CSD22206WT.B	Active	Production	DSBGA (YZF)   9	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	22206

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## **PACKAGE MATERIALS INFORMATION**

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#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD22206W	DSBGA	YZF	9	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
CSD22206WT	DSBGA	YZF	9	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1



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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD22206W	DSBGA	YZF	9	3000	182.0	182.0	20.0
CSD22206WT	DSBGA	YZF	9	250	182.0	182.0	20.0

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