

# CSD19505KTT 80 V N-Channel NexFET™ Power MOSFET

## 1 Features

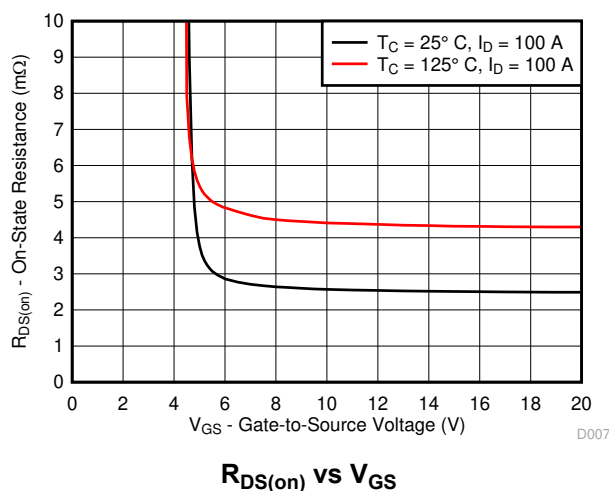
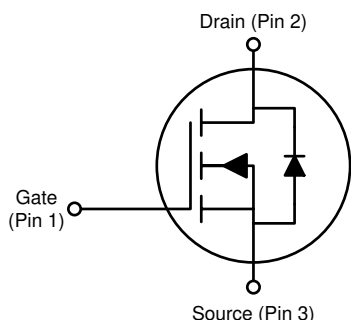
- Ultra-low  $Q_g$  and  $Q_{gd}$
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free
- D<sup>2</sup>PAK plastic package

## 2 Applications

- Secondary side synchronous rectifier
- Motor control

## 3 Description

This 80V, 2.6mΩ, D<sup>2</sup>PAK (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	80		V
$Q_g$	Gate Charge Total (10V)	76		nC
$Q_{gd}$	Gate Charge Gate to Drain	11		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{V}$	2.9	mΩ
		$V_{GS} = 10\text{V}$	2.6	mΩ
$V_{GS(th)}$	Threshold Voltage	2.6		V

## Device Information (1)

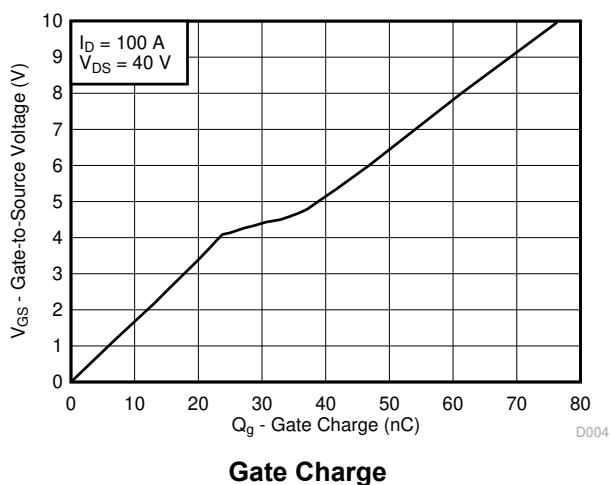
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD19505KTT	500	13-Inch Reel	D <sup>2</sup> PAK Plastic Package	Tape & Reel
CSD19505KTTT	50			

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	80	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D$	Continuous Drain Current (Package Limited)	200	A
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	212	A
	Continuous Drain Current (Silicon Limited), $T_C = 100^\circ\text{C}$	150	A
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	400	A
$P_D$	Power Dissipation	300	W
$T_J$ , $T_{stg}$	Operating Junction, Storage Temperature	–55 to 175	°C
$E_{AS}$	Avalanche Energy, Single Pulse $I_D = 101\text{A}$ , $L = 0.1\text{mH}$ , $R_G = 25\Omega$	510	mJ

- (1) Max  $R_{\theta JC} = 0.5^\circ\text{C/W}$ , pulse duration  $\leq 100\mu\text{s}$ , duty cycle  $\leq 1\%$ .



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## 4 Specifications

### 4.1 Electrical Characteristics

(T<sub>A</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
STATIC CHARACTERISTICS							
BV <sub>DSS</sub>	Drain-to-source voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	80			V	
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 64V	1			μA	
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 20V	100			nA	
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.2	2.6	3.2	V	
R <sub>DS(on)</sub>	Drain-to-source on-resistance	V <sub>GS</sub> = 6V, I <sub>D</sub> = 100A	2.9			3.8	mΩ
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 100A	2.6			3.1	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 8V, I <sub>D</sub> = 100A	262			S	
DYNAMIC CHARACTERISTICS							
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 40V, f = 1MHz	6090			7920	pF
C <sub>oss</sub>	Output capacitance		1600			2080	pF
C <sub>rss</sub>	Reverse transfer capacitance		26			34	pF
R <sub>G</sub>	Series gate resistance		1.4			2.8	Ω
Q <sub>g</sub>	Gate charge total (10V)	V <sub>DS</sub> = 40V, I <sub>D</sub> = 100A	76				nC
Q <sub>gd</sub>	Gate charge gate-to-drain		11				nC
Q <sub>gs</sub>	Gate charge gate-to-source		25				nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>		15				nC
Q <sub>oss</sub>	Output charge	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V	214				nC
t <sub>d(on)</sub>	Turn on delay time	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 10V, I <sub>DS</sub> = 100A, R <sub>G</sub> = 0Ω	11				ns
t <sub>r</sub>	Rise time		5				ns
t <sub>d(off)</sub>	Turn off delay time		22				ns
t <sub>f</sub>	Fall time		3				ns
DIODE CHARACTERISTICS							
V <sub>SD</sub>	Diode forward voltage	I <sub>SD</sub> = 100A, V <sub>GS</sub> = 0V	0.9			1.1	V
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DS</sub> = 40V, I <sub>F</sub> = 100A,	400				nC
t <sub>rr</sub>	Reverse recovery time	di/dt = 300A/μs	88				ns

### 4.2 Thermal Information

(T<sub>A</sub> = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction-to-case thermal resistance			0.5	°C/W
R <sub>θJA</sub>	Junction-to-ambient thermal resistance			62	°C/W

### 4.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

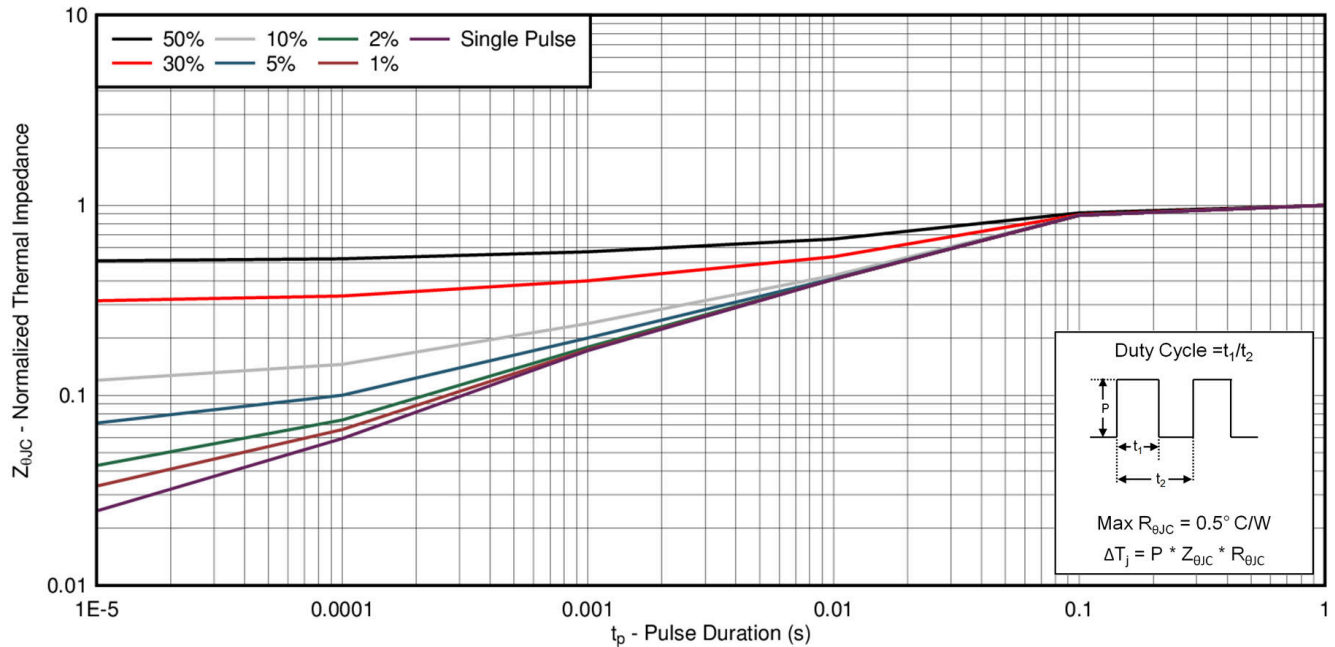


Figure 4-1. Transient Thermal Impedance

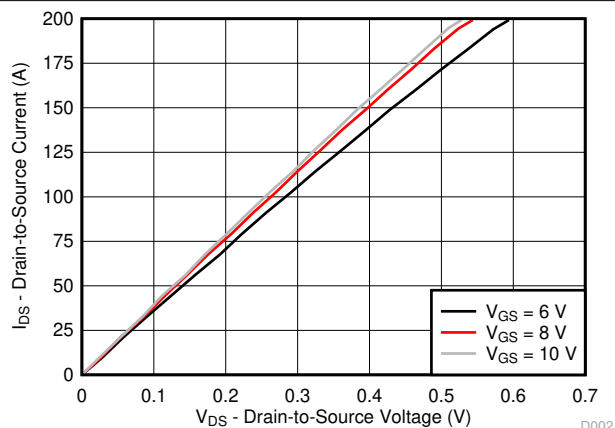


Figure 4-2. Saturation Characteristics

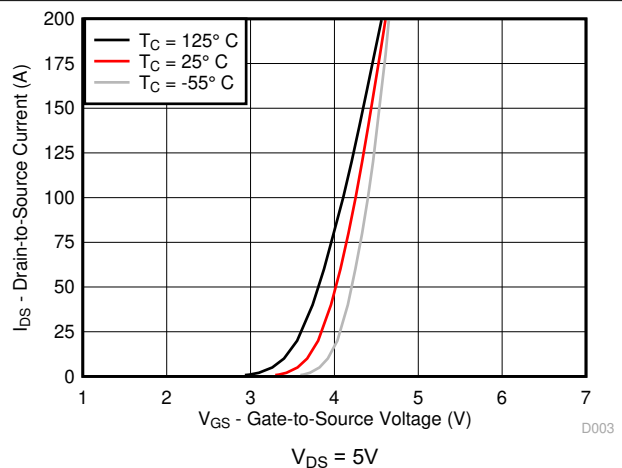
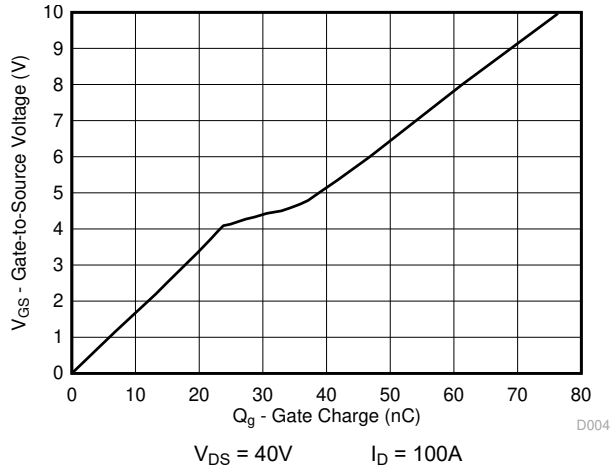
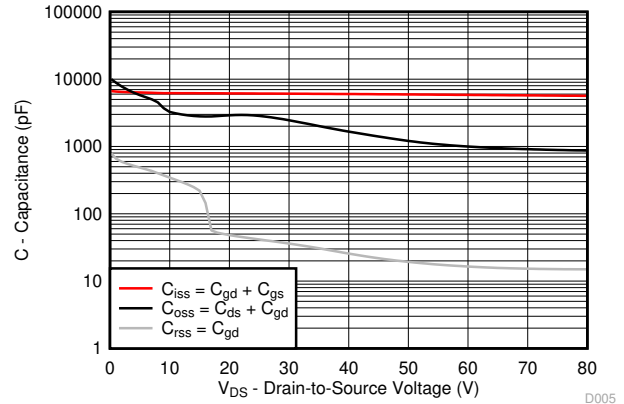


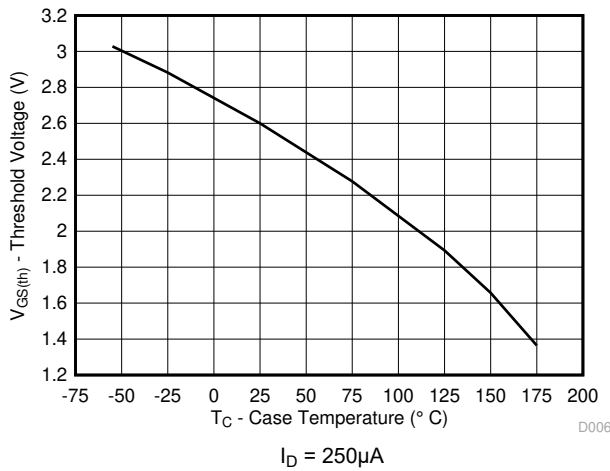
Figure 4-3. Transfer Characteristics



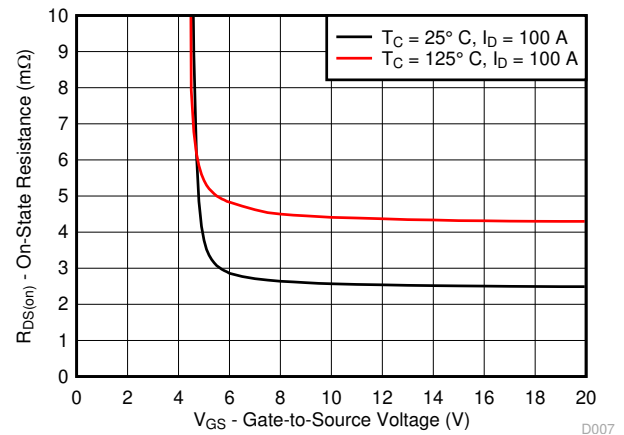
**Figure 4-4. Gate Charge**



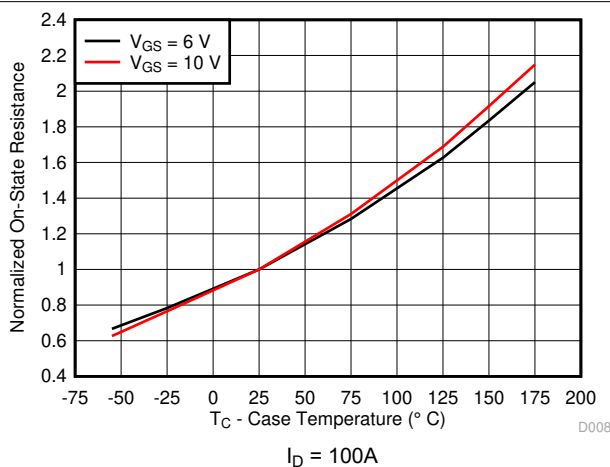
**Figure 4-5. Capacitance**



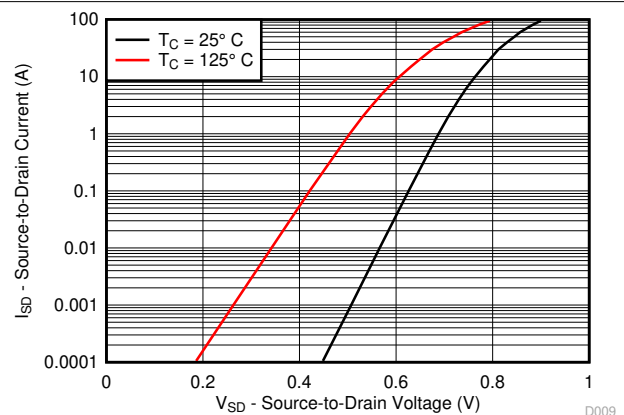
**Figure 4-6. Threshold Voltage vs Temperature**



**Figure 4-7. On-State Resistance vs Gate-to-Source Voltage**



**Figure 4-8. Normalized On-State Resistance vs Temperature**



**Figure 4-9. Typical Diode Forward Voltage**

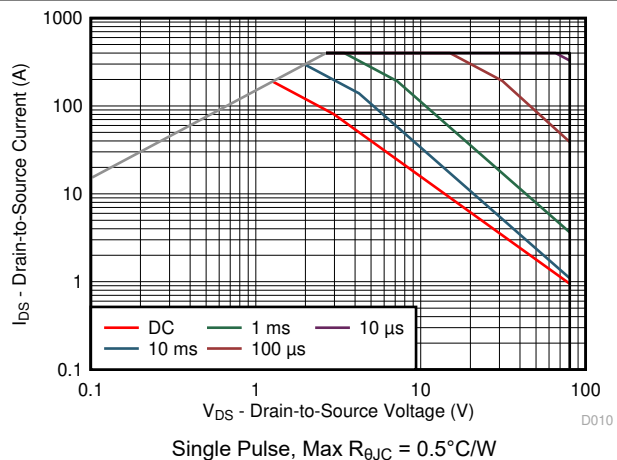


Figure 4-10. Maximum Safe Operating Area

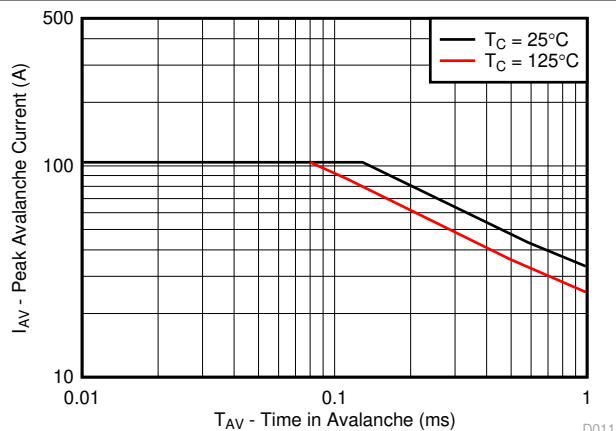


Figure 4-11. Single Pulse Unclamped Inductive Switching

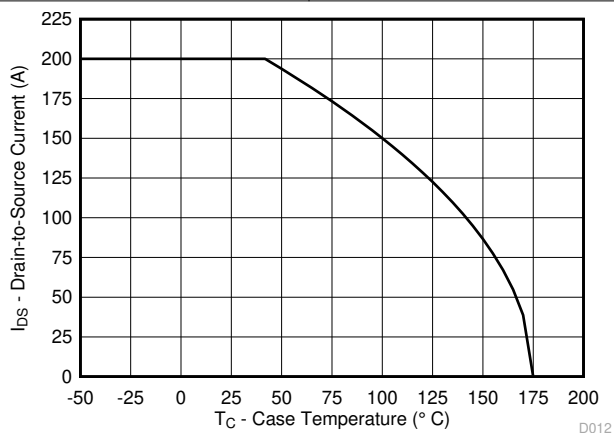


Figure 4-12. Maximum Drain Current vs Temperature

## 5 Device and Documentation Support

### 5.1 Third-Party Products Disclaimer

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### 5.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 5.4 Trademarks

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### 5.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 5.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 6 Revision History

Changes from Revision * (March 2016) to Revision A (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD19505KTT</a>	Active	Production	DDPAK/ TO-263 (KTT)   2	500   LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19505KTT
CSD19505KTT.B	Active	Production	DDPAK/ TO-263 (KTT)   2	500   LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19505KTT
<a href="#">CSD19505KTTT</a>	Active	Production	DDPAK/ TO-263 (KTT)   2	50   SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19505KTT
CSD19505KTTT.B	Active	Production	DDPAK/ TO-263 (KTT)   2	50   SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19505KTT

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

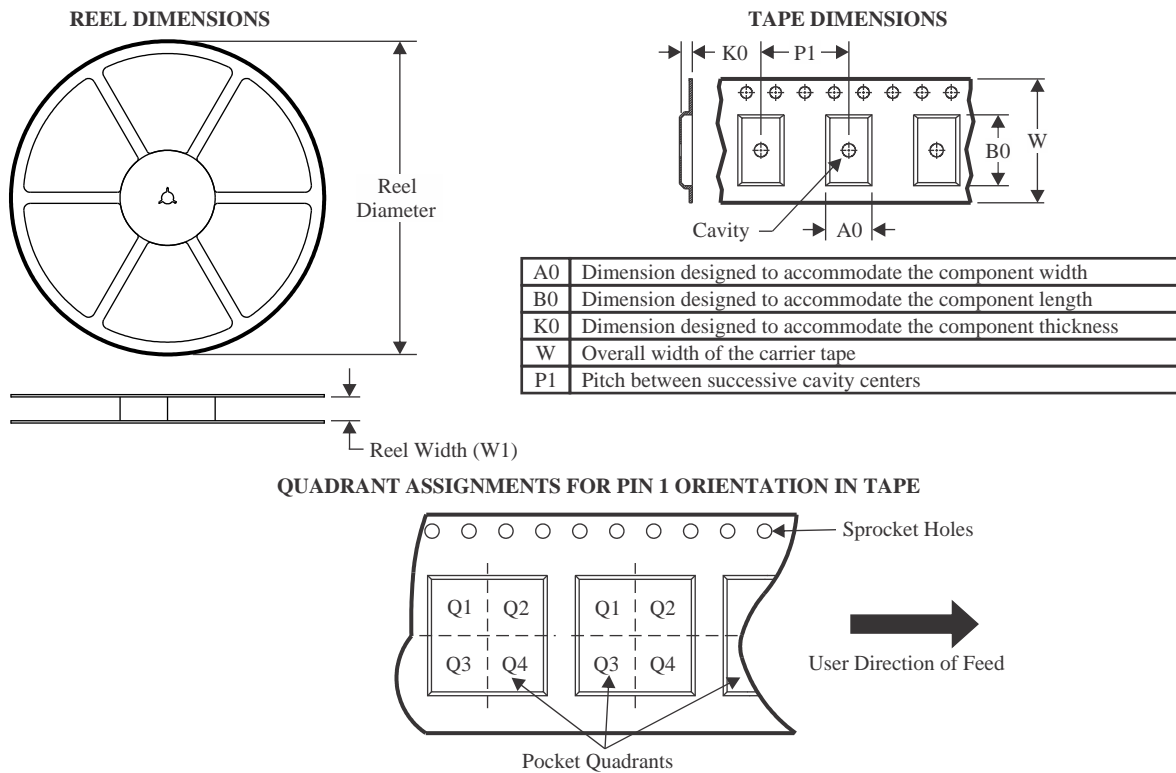
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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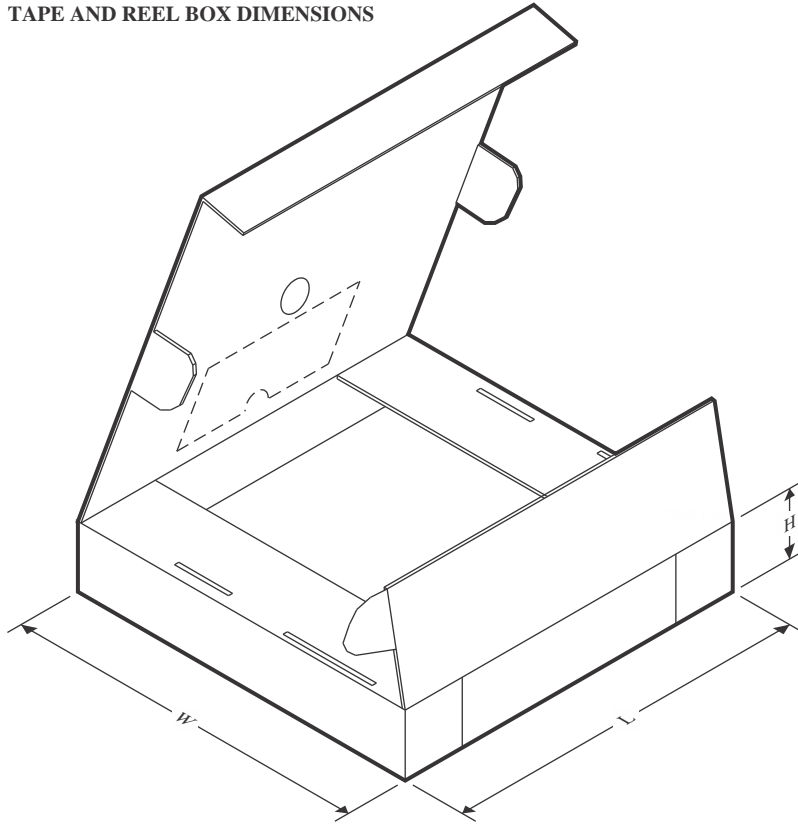
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

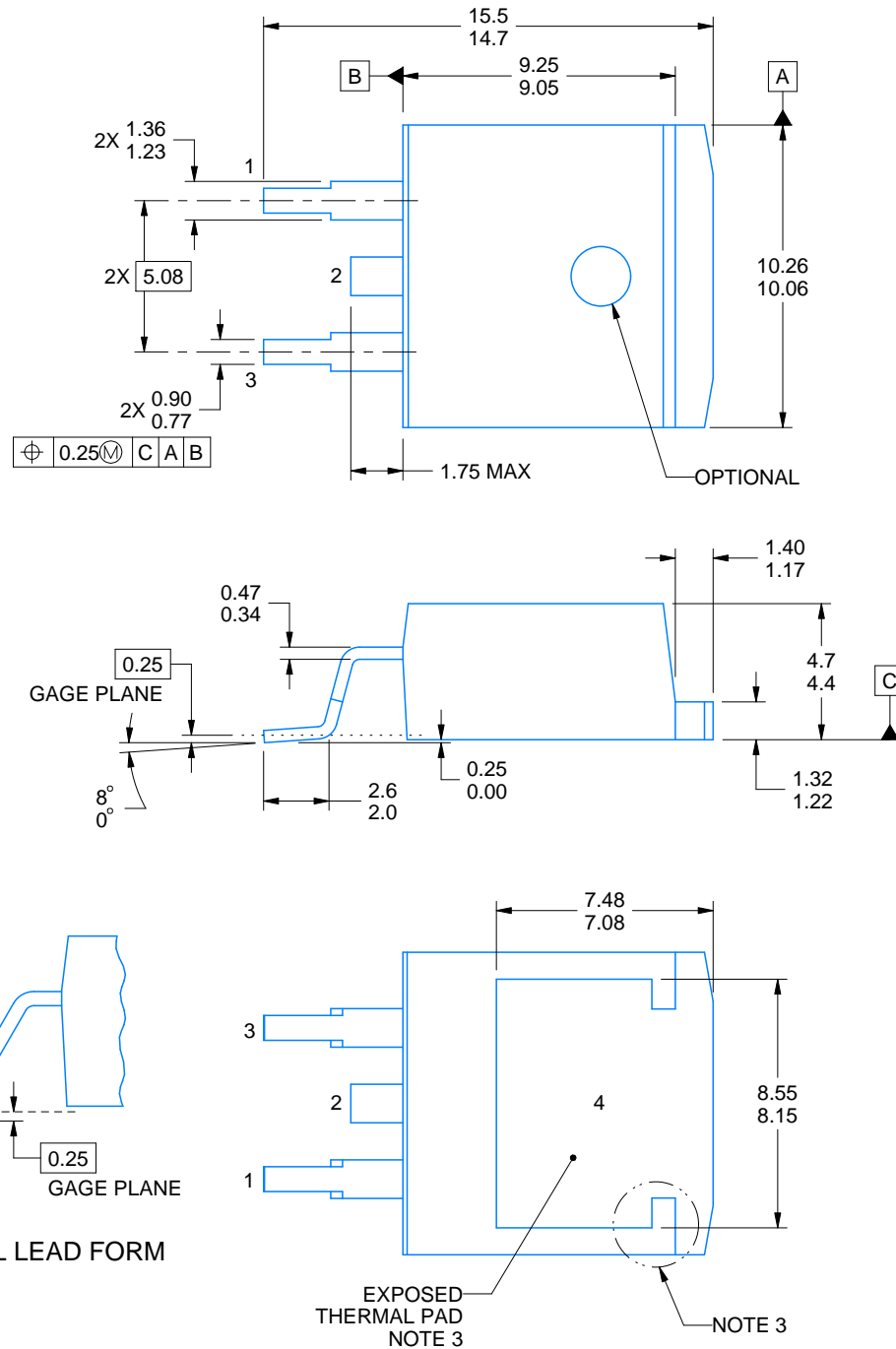
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD19505KTT	DDPAK/TO-263	KTT	2	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
CSD19505KTTT	DDPAK/TO-263	KTT	2	50	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD19505KTT	DDPAK/TO-263	KTT	2	500	340.0	340.0	38.0
CSD19505KTTT	DDPAK/TO-263	KTT	2	50	340.0	340.0	38.0



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## NOTES:

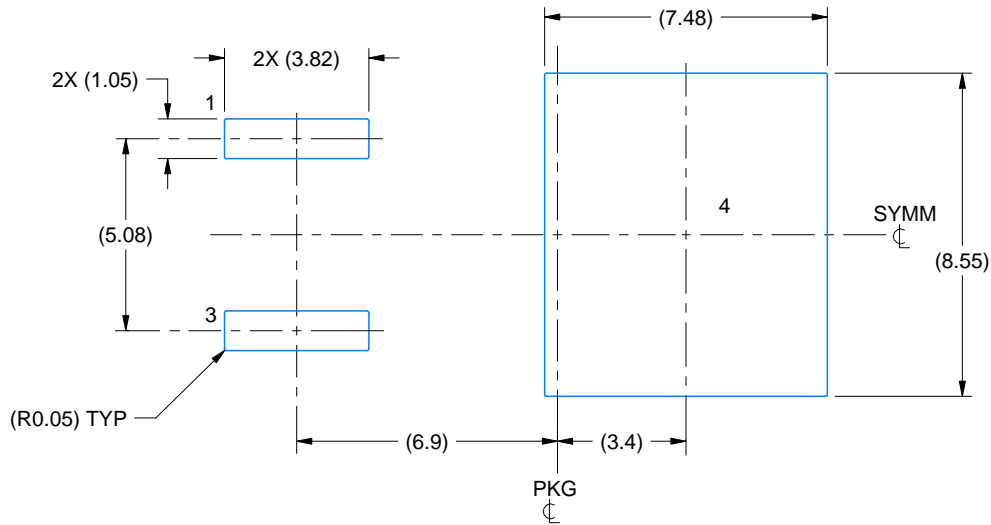
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-263.

# EXAMPLE BOARD LAYOUT

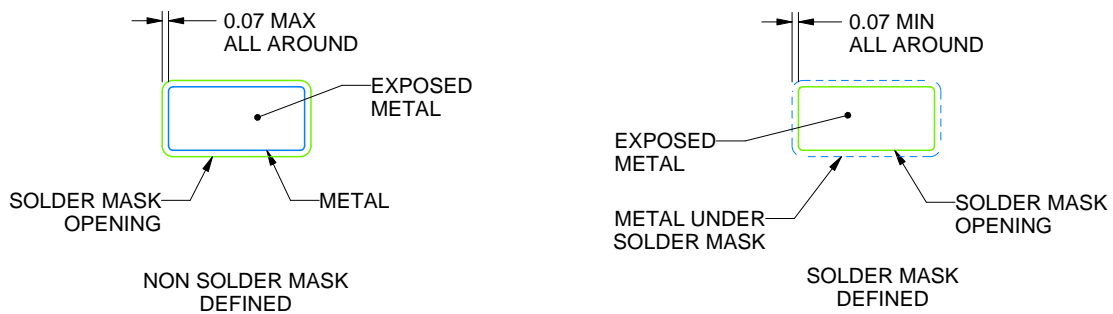
KTT0002A

TO-263 - 4.7 mm max height

TO-263



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:5X



SOLDER MASK DETAILS

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NOTES: (continued)

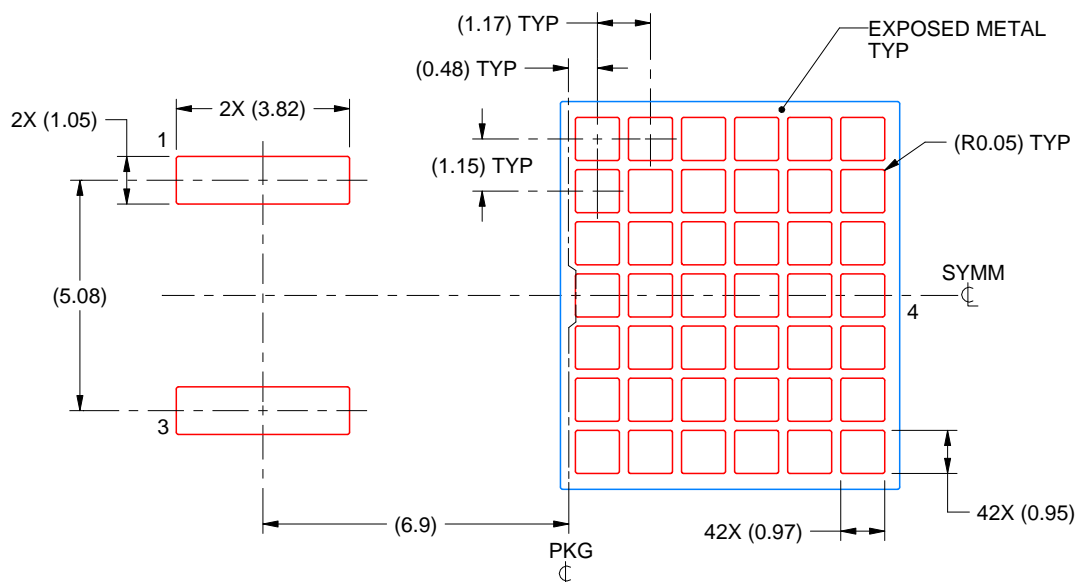
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slm002](http://www.ti.com/lit/slm002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

KTT0002A

TO-263 - 4.7 mm max height

TO-263



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
60.5% PRINTED SOLDER COVERAGE BY AREA  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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