

## CSD18532Q5B 60-V N-Channel NexFET™ Power MOSFETs

### 1 Features

- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low-Thermal Resistance
- Avalanche Rated
- Logic Level
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

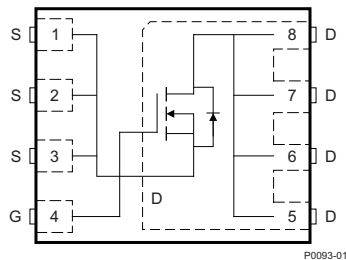
### 2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Isolated Converter Primary Side Switch
- Motor Control

### 3 Description

This 2.5-m $\Omega$ , 60-V SON 5-mm × 6-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



P0093-01

#### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	60	V
$Q_g$	Gate Charge Total (10 V)	44	nC
$Q_{gd}$	Gate Charge Gate-to-Drain	6.9	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	3.3
		$V_{GS} = 10\text{ V}$	2.5
$V_{GS(th)}$	Threshold Voltage	1.8	V

#### Device Information<sup>(1)</sup>

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18532Q5B	2500	13-Inch Reel	SON 5.00-mm × 6.00-mm Plastic Package	Tape and Reel
CSD18532Q5BT	250	13-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

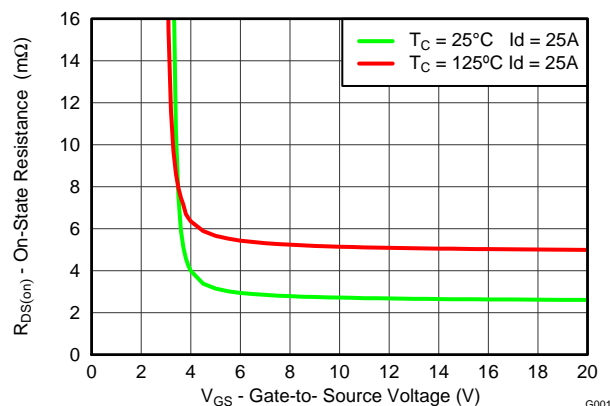
#### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	60	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	172	
	Continuous Drain Current <sup>(1)</sup>	23	
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	400	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.2	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	156	
$T_J$ , $T_{stg}$	Operating Junction Temperature, Storage Temperature	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, Single Pulse $I_D = 80\text{ A}$ , $L = 0.1\text{ mH}$ , $R_G = 25\ \Omega$	320	mJ

(1) Typical  $R_{\theta JA} = 40^\circ\text{C/W}$  on a 1-in<sup>2</sup>, 2-oz Cu pad on a 0.06-in thick FR4 PCB.

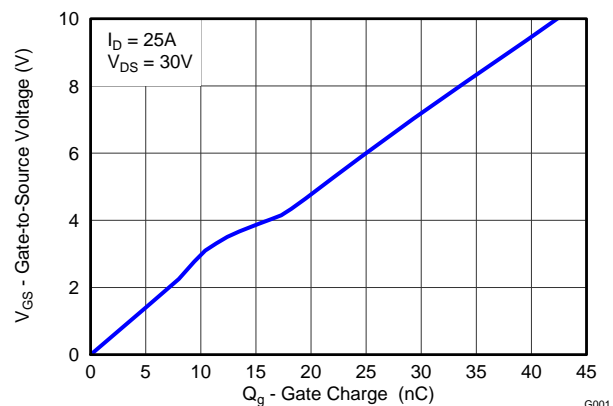
(2) Max  $R_{\theta JC} = 0.8^\circ\text{C/W}$ , pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .

$R_{DS(on)}$  vs  $V_{GS}$



G001

Gate Charge



G001



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## 4 Revision History

### Changes from Revision C (May 2017) to Revision D Page

• Extended the $V_{DS}$ on <a href="#">Figure 5</a> to 60 V.....	<b>4</b>
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### Changes from Revision B (July 2014) to Revision C Page

• Added the <i>Receiving Notification of Documentation Updates</i> and <i>Community Resources</i> sections to <i>Device and Documentation Support</i> . ....	<b>7</b>
• Changed the dimension between pads 3 and 4 from 0.028 inches: to 0.050 inches in the <i>Recommended PCB Pattern</i> section diagram .....	<b>9</b>

### Changes from Revision A (May 2014) to Revision B Page

• Changed "7-Inch Reel" to state "13-Inch Reel". ....	<b>1</b>
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### Changes from Original (Nov 2012) to Revision A Page

• Updated the device description. ....	<b>1</b>
• Specified $Q_g$ at 10 V. ....	<b>1</b>
• Added small reel option. ....	<b>1</b>
• Increased pulsed drain current to 400 A. ....	<b>1</b>
• Added line for max power dissipation with case temperature held to 25°C. ....	<b>1</b>
• Updated the pulsed drain current conditions. ....	<b>1</b>
• Eliminated $Q_g$ at 4.5 V. ....	<b>3</b>
• Changed <a href="#">Figure 1</a> from a normalized $R_{\theta JA}$ curve to a $R_{\theta JC}$ curve.....	<b>4</b>
• Updated the safe operating area in <a href="#">Figure 10</a> . ....	<b>6</b>
• Updated the mechanical drawing. ....	<b>8</b>

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  unless otherwise stated

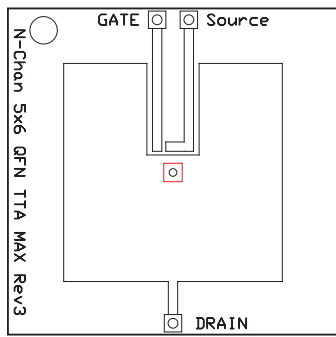
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
STATIC CHARACTERISTICS							
BV <sub>DSS</sub>	Drain-to-source voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V	
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 48 V	1			μA	
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V	100			nA	
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	1.8	2.2	V	
R <sub>DS(on)</sub>	Drain-to-source on-resistance	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 25 A	3.3			mΩ	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A	2.5				
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 25 A	143			S	
DYNAMIC CHARACTERISTICS							
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V, f = 1 MHz	3900			5070	pF
C <sub>oss</sub>	Output capacitance		470			611	pF
C <sub>rss</sub>	Reverse transfer capacitance		13			17	pF
R <sub>G</sub>	Series gate resistance		1.2			2.4	Ω
Q <sub>g</sub>	Gate charge total (10 V)	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 25 A	44			58	nC
Q <sub>gd</sub>	Gate charge gate-to-drain		6.9				nC
Q <sub>gs</sub>	Gate charge gate-to-source		10				nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>		6.3				nC
Q <sub>oss</sub>	Output charge	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	52				nC
t <sub>d(on)</sub>	Turnon delay time	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>DS</sub> = 25 A, R <sub>G</sub> = 0 Ω	5.8				ns
t <sub>r</sub>	Rise time		7.2				ns
t <sub>d(off)</sub>	Turnoff delay time		22				ns
t <sub>f</sub>	Fall time		3.1				ns
DIODE CHARACTERISTICS							
V <sub>SD</sub>	Diode forward voltage	I <sub>SD</sub> = 25 A, V <sub>GS</sub> = 0 V	0.8			1	V
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DS</sub> = 30 V, I <sub>F</sub> = 25 A, di/dt = 300 A/μs	111				nC
t <sub>rr</sub>	Reverse recovery time		49				ns

### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  unless otherwise stated

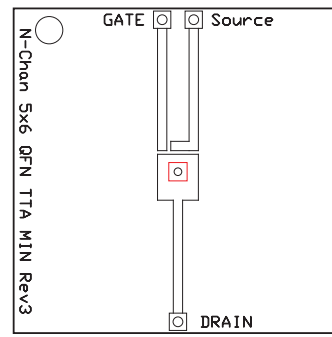
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance <sup>(1)</sup>			0.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>			50	$^\circ\text{C}/\text{W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.



M0137-01

Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$   
when mounted on 1 in<sup>2</sup>  
(6.45 cm<sup>2</sup>) of  
2-oz (0.071-mm) thick  
Cu.

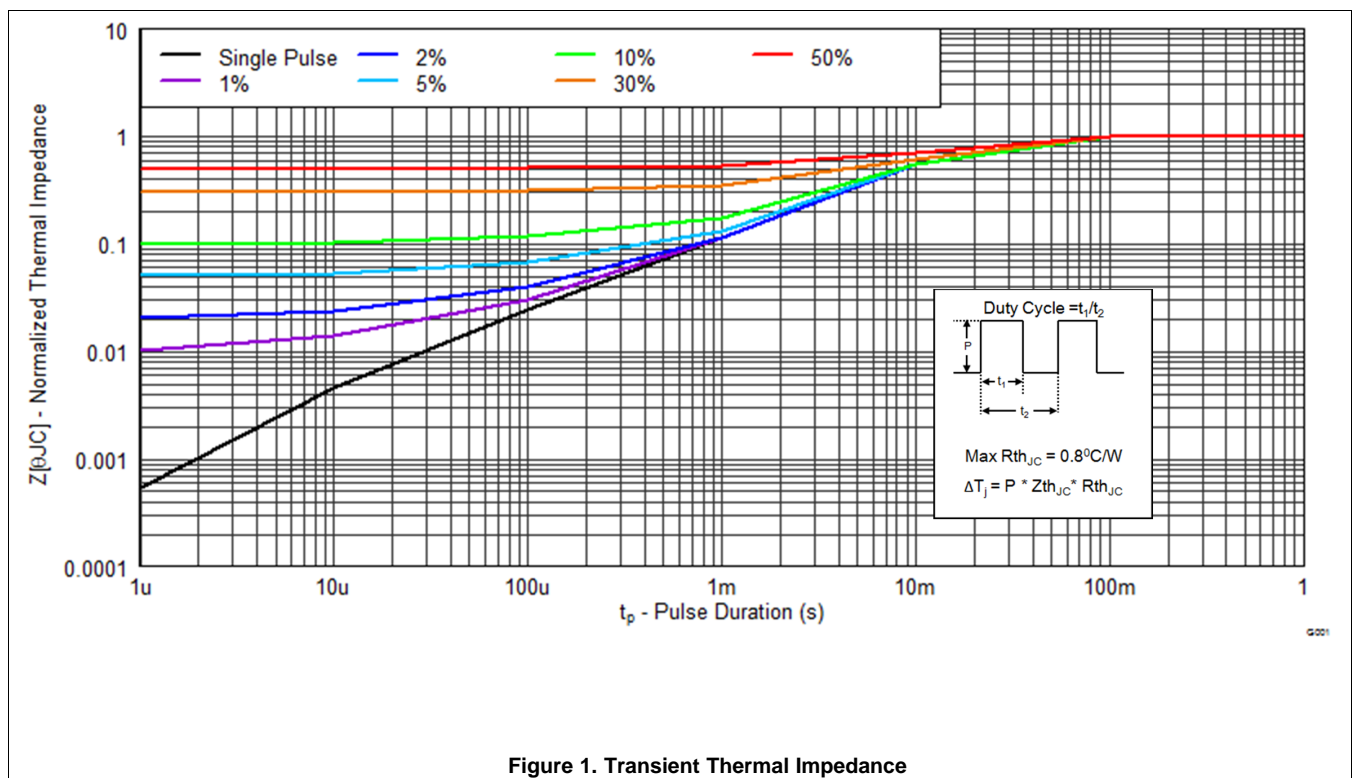


M0137-02

Max  $R_{\theta JA} = 125^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz (0.071-mm) thick  
Cu.

### 5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$  unless otherwise stated



## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  unless otherwise stated

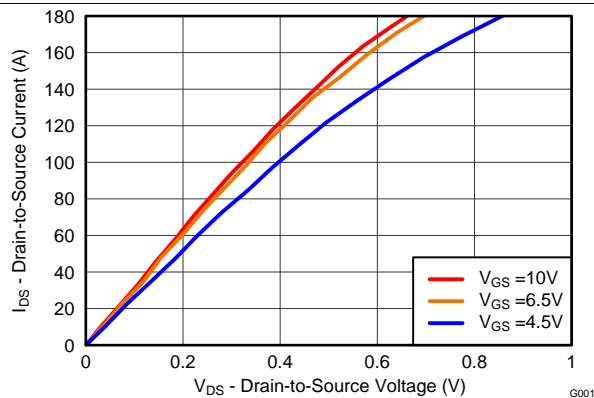


Figure 2. Saturation Characteristics

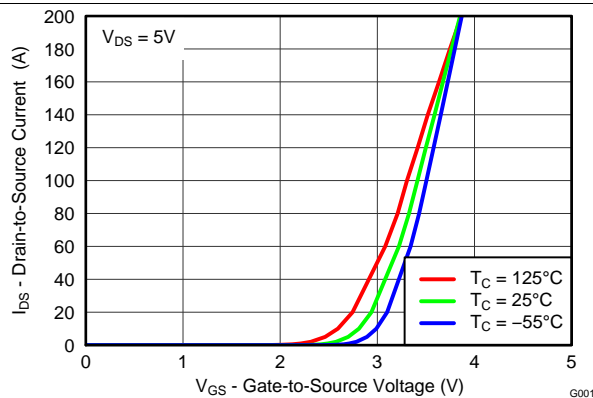


Figure 3. Transfer Characteristics

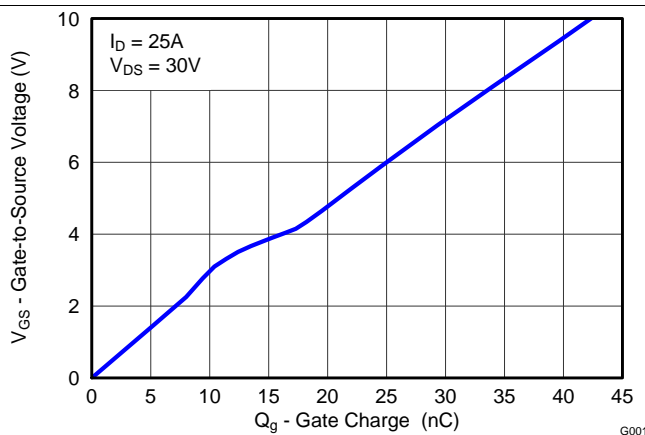


Figure 4. Gate Charge

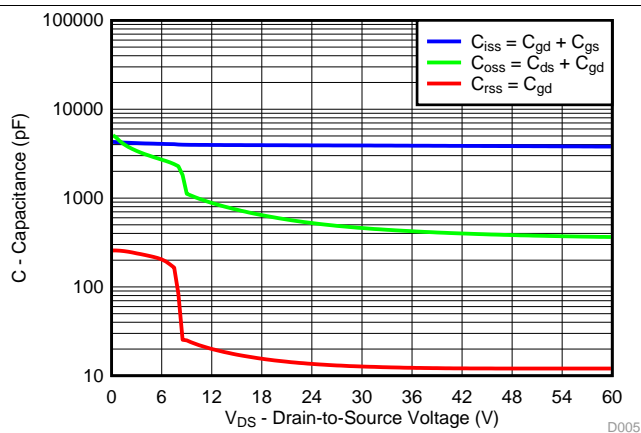


Figure 5. Capacitance

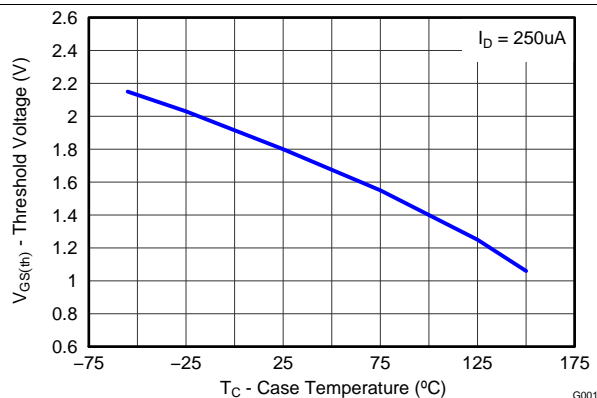


Figure 6. Threshold Voltage vs Temperature

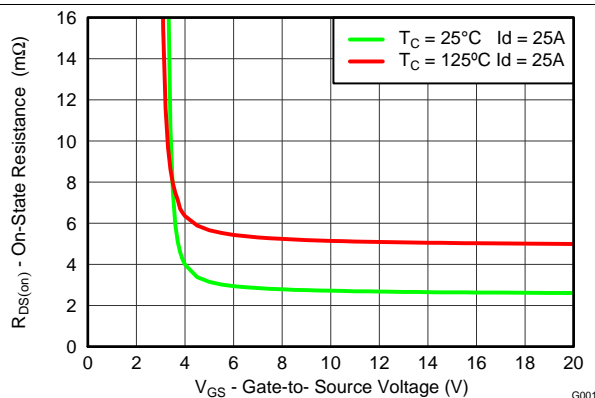


Figure 7. On-State Resistance vs Gate-to-Source Voltage

## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  unless otherwise stated

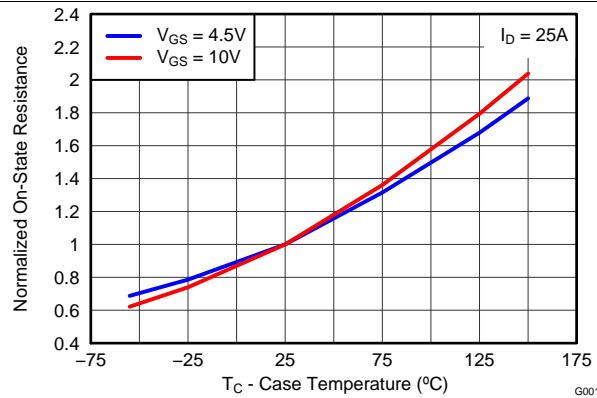


Figure 8. Normalized On-State Resistance vs Temperature

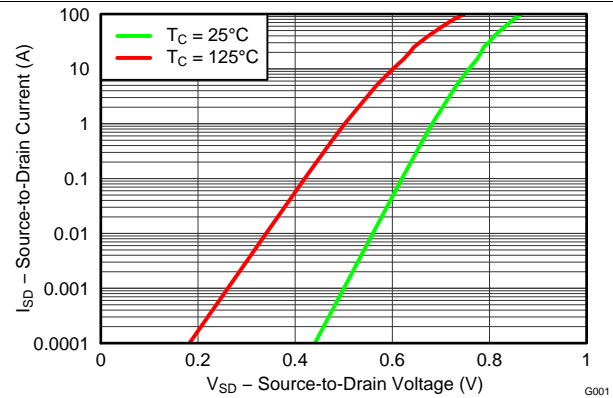


Figure 9. Typical Diode Forward Voltage

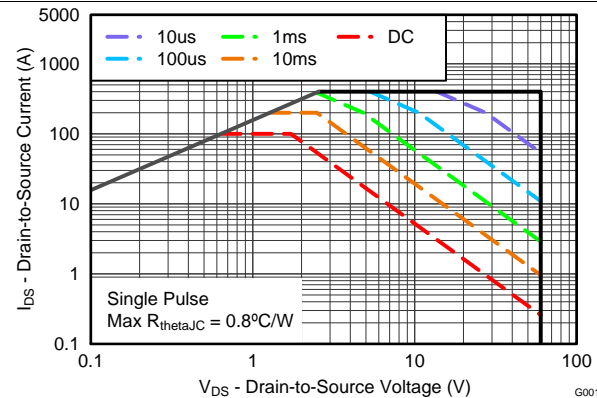


Figure 10. Maximum Safe Operating Area

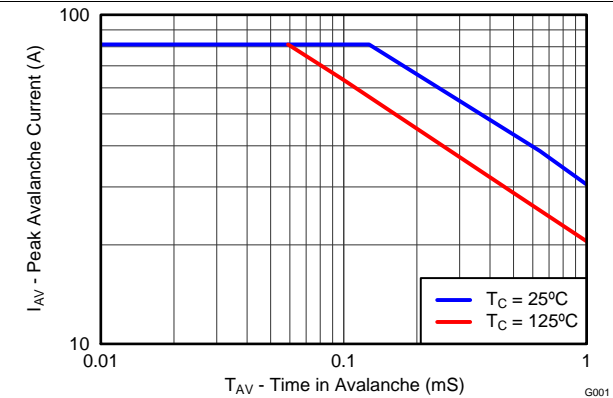


Figure 11. Single Pulse Unclamped Inductive Switching

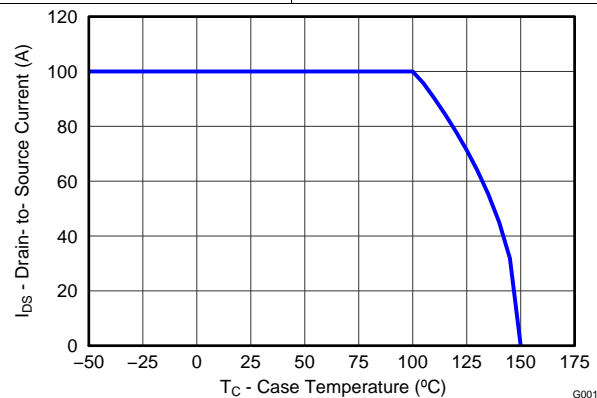


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

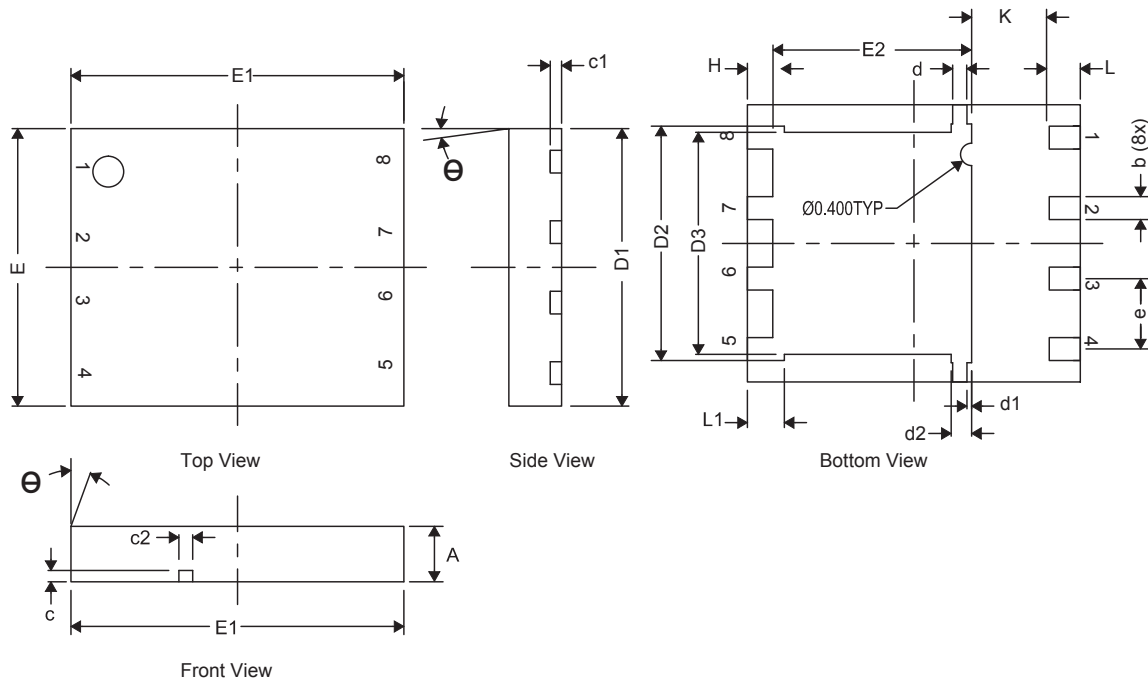
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Q5B Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 TYP		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 TYP		



Technical drawing of a mechanical part, likely a bracket or flange, showing dimensions in inches (in parentheses) and millimeters (in brackets). The drawing includes a central vertical axis labeled 'C' and a horizontal axis labeled 'SYM'.

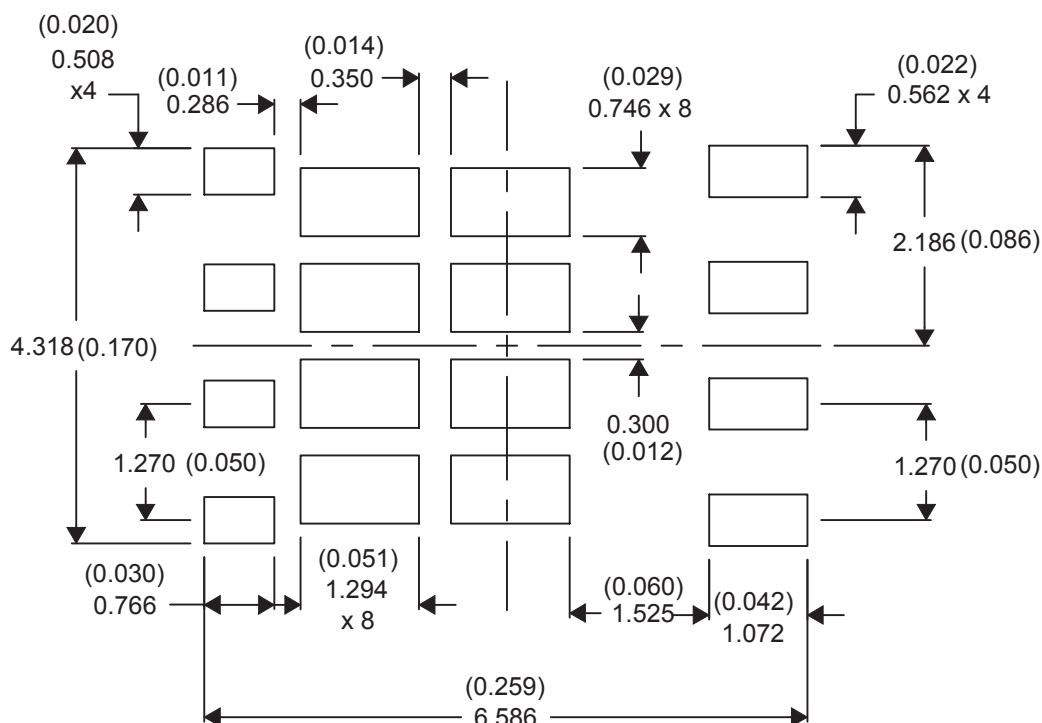
**Dimensions:**

- Overall Width:** 4.440 (0.175)
- Overall Height:** 4.520 (0.178)
- Top Flange Width:** 1.100 (0.043)
- Top Flange Height:** 1.270 (0.050)
- Bottom Flange Width:** 1.372 (0.054)
- Bottom Flange Height:** 0.710 (0.028)
- Central Section Width:** 3.456 (0.136)
- Central Section Height:** 0.590 (0.023)
- Central Section Thickness:** 0.984 (0.039)
- Top Flange Thickness:** 0.710 (0.028)
- Bottom Flange Thickness:** 0.560 (0.022)

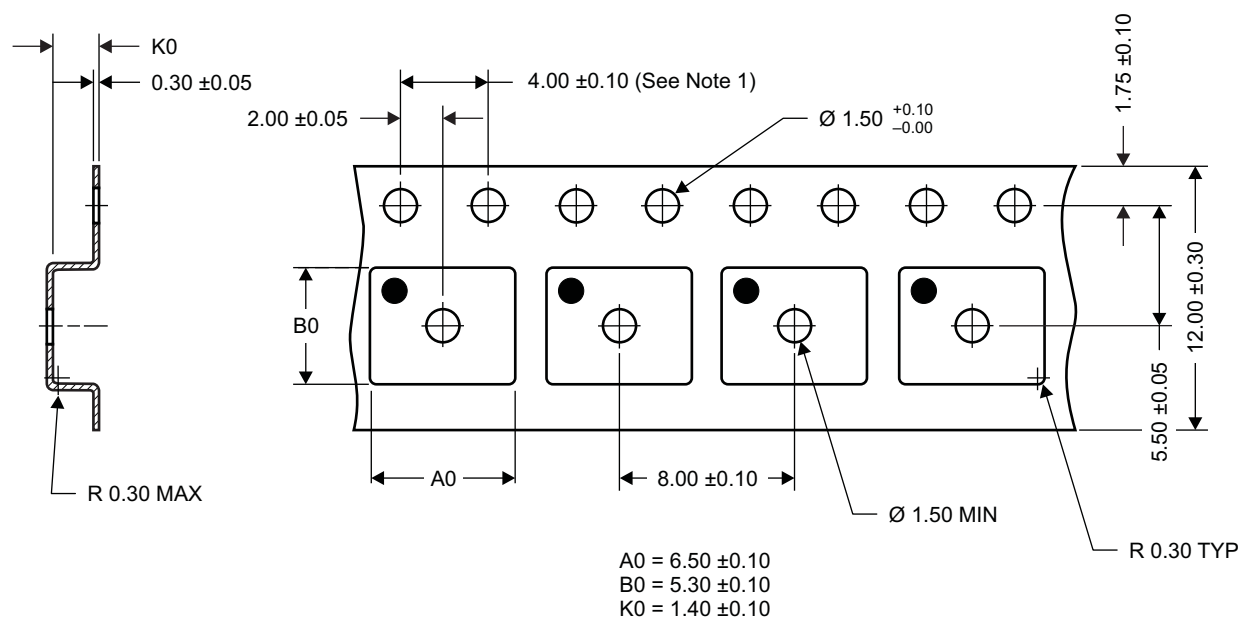
**Labels:**

- C:** Central vertical axis.
- SYM:** Symmetry line.
- 4:** Feature identifier for the top flange.
- 8:** Feature identifier for the bottom flange.

### 7.3 Recommended Stencil Pattern



## 7.4 Q5B Tape and Reel Information



M0138-01

### Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD18532Q5B</a>	Active	Production	VSON-CLIP (DNK)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 150	CSD18532
CSD18532Q5B.B	Active	Production	VSON-CLIP (DNK)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18532
CSD18532Q5BG4	Active	Production	VSON-CLIP (DNK)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18532
CSD18532Q5BG4.B	Active	Production	VSON-CLIP (DNK)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18532
<a href="#">CSD18532Q5BT</a>	Active	Production	VSON-CLIP (DNK)   8	250   SMALL T&R	ROHS Exempt	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 150	CSD18532
CSD18532Q5BT.B	Active	Production	VSON-CLIP (DNK)   8	250   SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18532

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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