CSD17575Q3 30-V N-Channel NexFET™ Power MOSFET

1 Features

- Low Q_g and Q_{gd}
- Low $R_{DS(on)}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

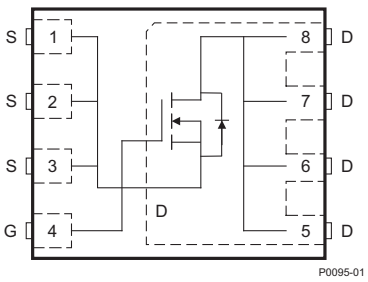
2 Applications

- Point of Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Synchronous FET Applications

3 Description

This 1.9 mΩ, 30 V, SON 3×3 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5V)	23		nC
Q_{gd}	Gate Charge Gate-to-Drain	5.4		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	2.6	mΩ
		V_{GS} = 10 V	1.9	
V_{th}	Threshold Voltage	1.4		V

Ordering Information[1]

Device	Media	Qty	Package	Ship
CSD17575Q3	13-Inch Reel	2500	SON 3.3 × 3.3 mm Plastic Package	Tape and Reel
CSD17575Q3T	13-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

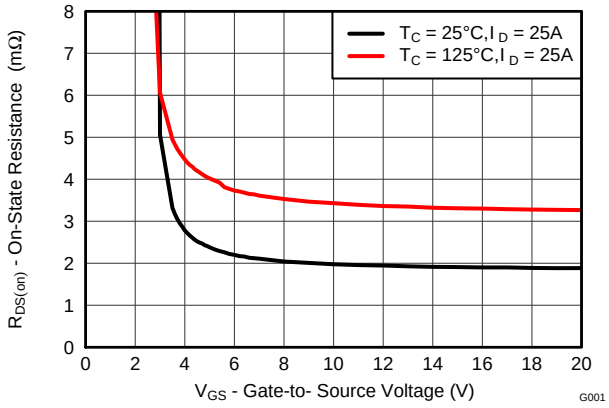
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limit)	60	A
	Continuous Drain Current (Silicon Limit), T_C = 25°C	182	
	Continuous Drain Current[1]	27	
I_{DM}	Pulsed Drain Current[2]	240	A
P_D	Power Dissipation[1]	2.8	W
	Power Dissipation, T_C = 25°C	108	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 48, L = 0.1 mH, R_G = 25 Ω	115	mJ

(1) Typical $R_{\theta JA}$ = 45°C/W on 1-inch^2 Cu (2 oz.) on 0.060-inch thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.5°C/W, pulse duration ≤100 µs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge

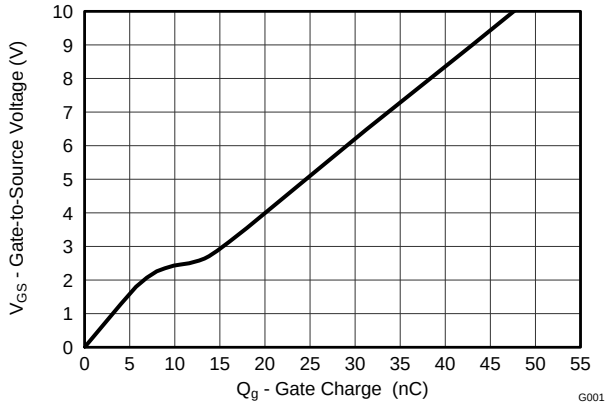


Table of Contents

4 Revision History

Changes from Original (June 2014) to Revision A **Page**

- Added b1, d, d1, and K dimensions to the mechanical information table ... 8

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

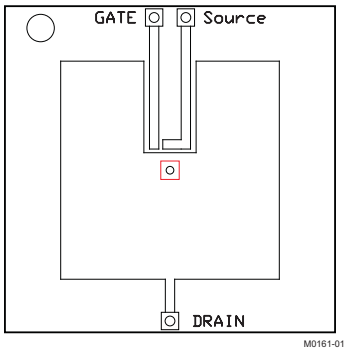
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.1	1.4	1.8	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_D = 25 A		2.6	3.2	mΩ
		V_{GS} = 10 V, I_D = 25 A		1.9	2.3	
g_{fs}	Transconductance	V_{DS} = 3 V, I_D = 25 A		118		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		3400	4420	pF
C_{OSS}	Output Capacitance			393	511	pF
C_{RSS}	Reverse Transfer Capacitance			157	204	pF
R_g	Series Gate Resistance			0.9	1.8	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 15 V, I_D = 25 A		23	30	nC
Q_{gd}	Gate Charge Gate-to-Drain			5.4		nC
Q_{gs}	Gate Charge Gate-to-Source			8.5		nC
$Q_{g(th)}$	Gate Charge at V_{th}			4.6		nC
Q_{OSS}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		11.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 4.5 V I_D = 25 A R_G = 2 Ω		4		ns
t_r	Rise Time			10		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 15 V, I_F = 25 A, di/dt = 300 A/µs		15		nC
t_{rr}	Reverse Recovery Time			13		ns

5.2 Thermal Information

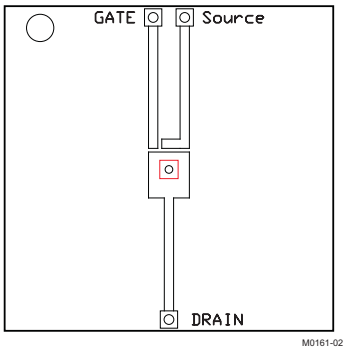
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			1.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			55	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), Cu pad on a 1.5-inches × 1.5-inches thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas RθJA is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 2-oz.Cu.



Max $R_{\theta JA}$ = 55°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 160°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

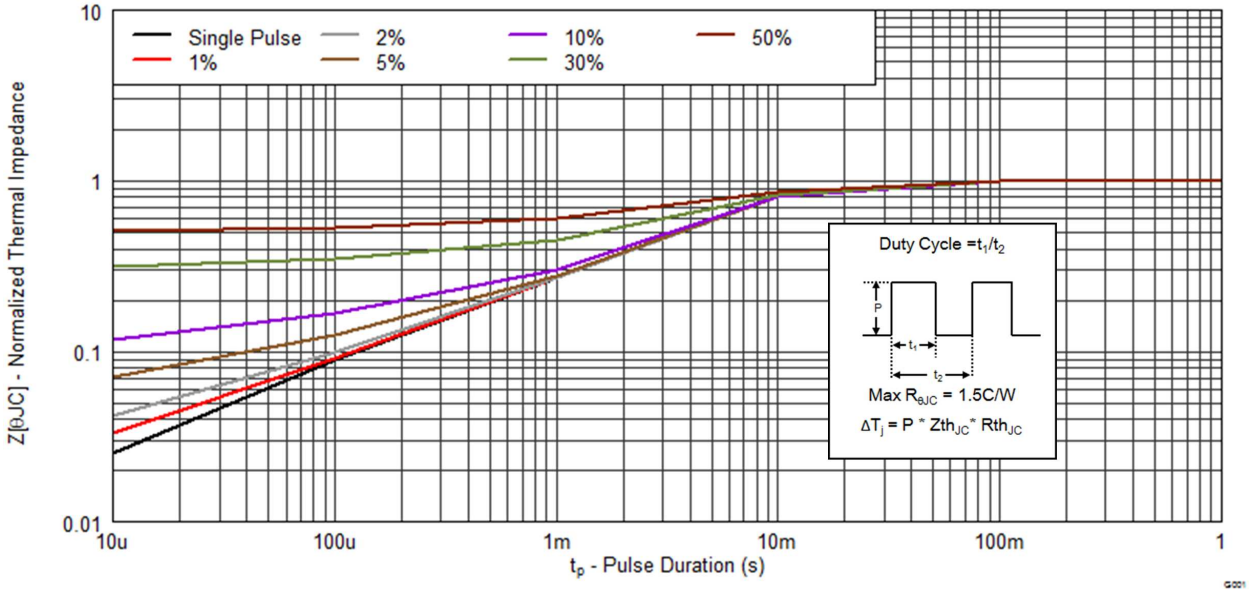


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

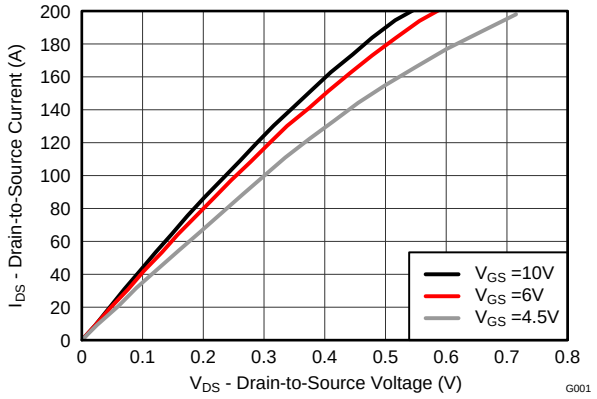


Figure 2. Saturation Characteristics

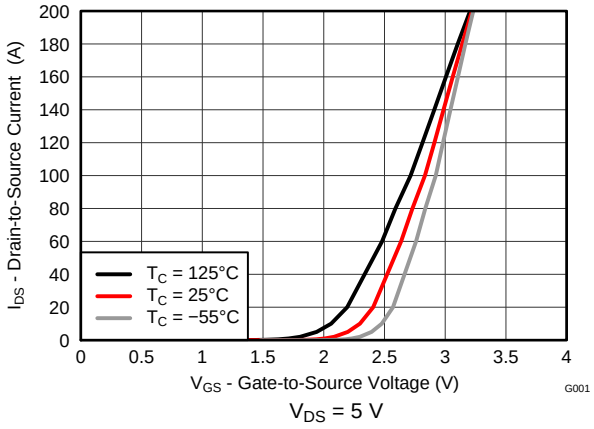


Figure 3. Transfer Characteristics

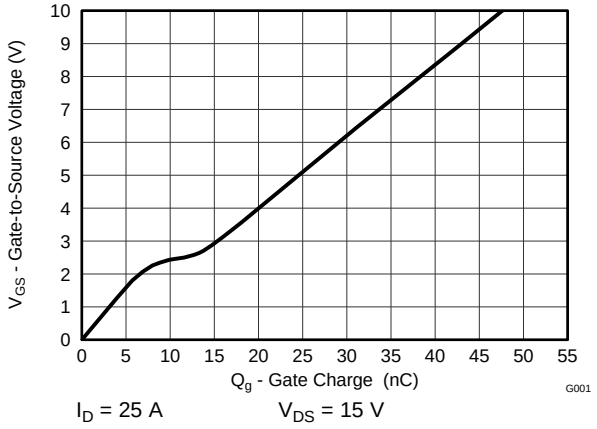


Figure 4. Gate Charge

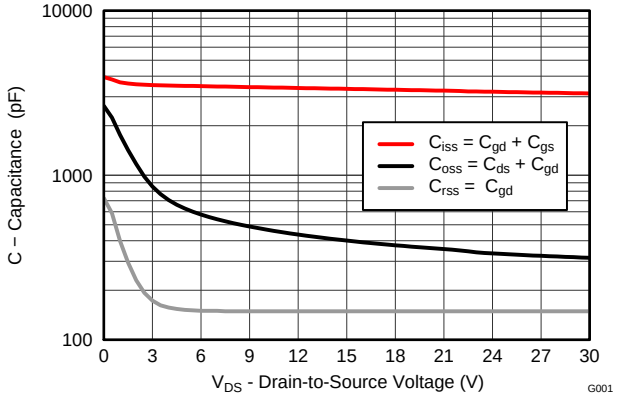


Figure 5. Capacitance

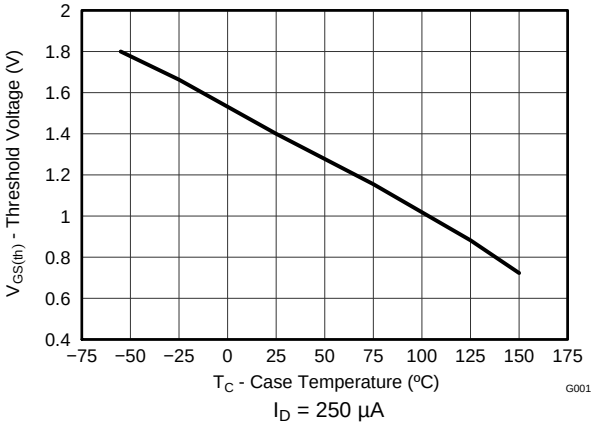


Figure 6. Threshold Voltage vs Temperature

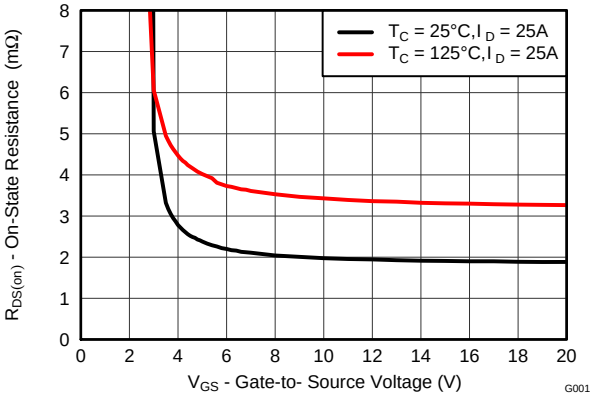


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

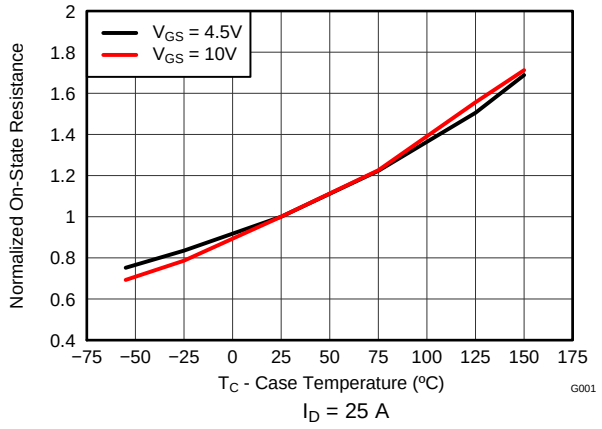


Figure 8. Normalized On-State Resistance vs Temperature

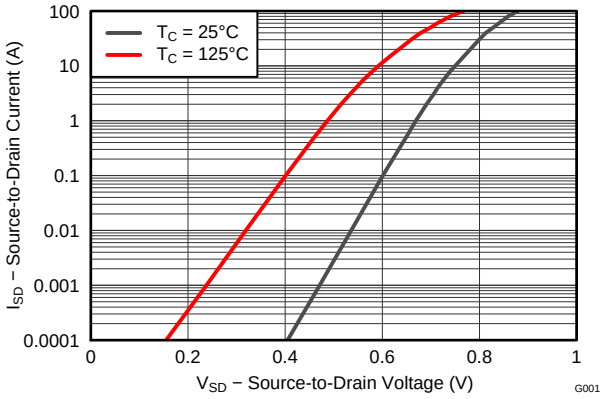


Figure 9. Typical Diode Forward Voltage

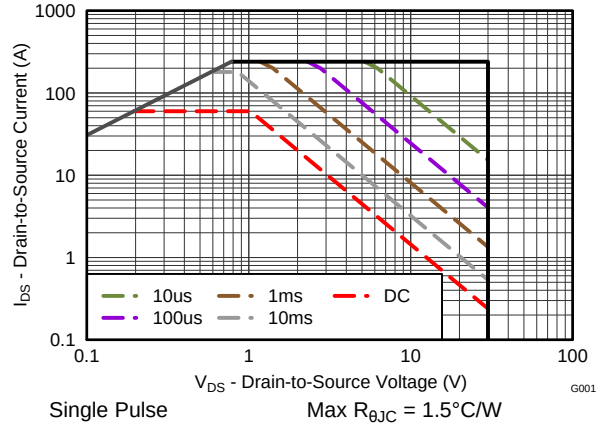


Figure 10. Maximum Safe Operating Area

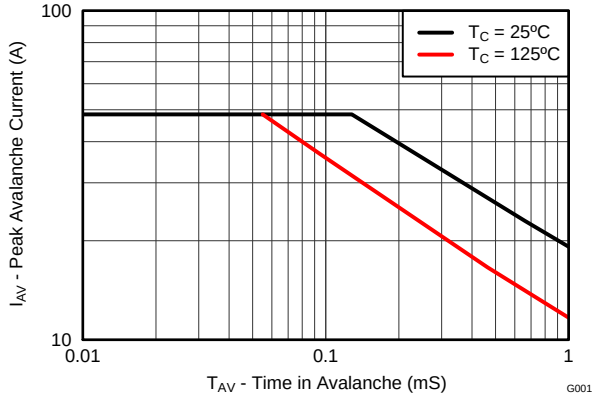


Figure 11. Single Pulse Unclamped Inductive Switching

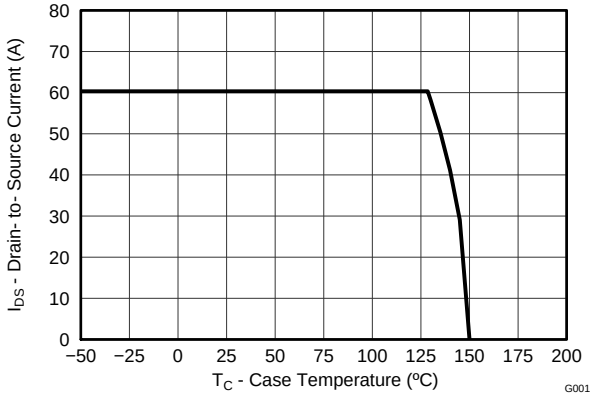


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

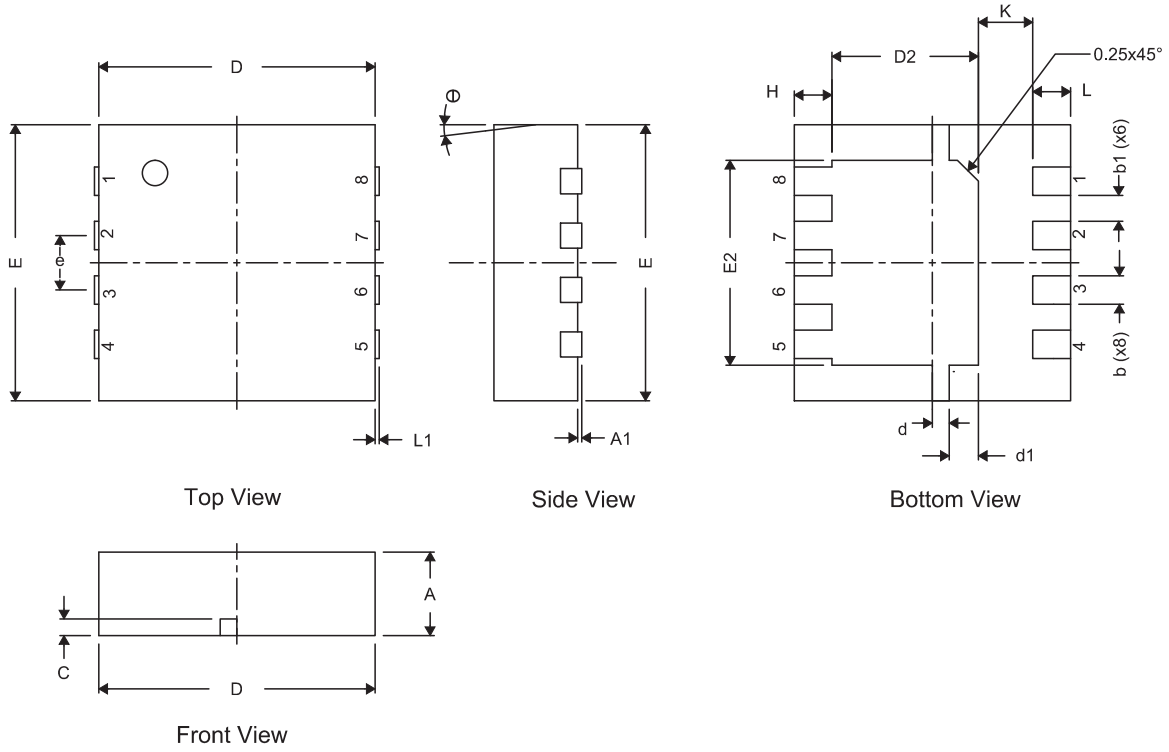
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

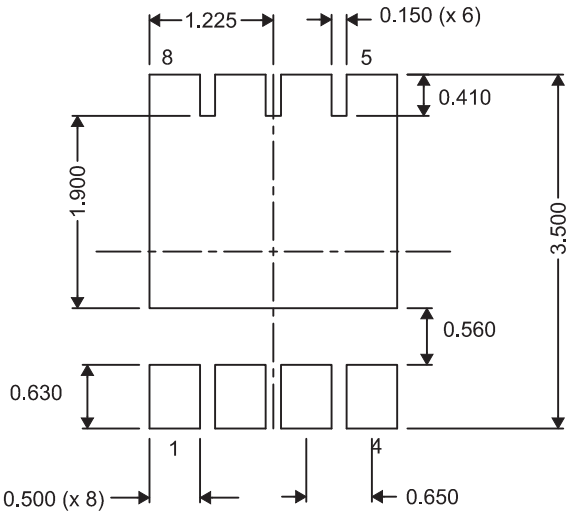
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



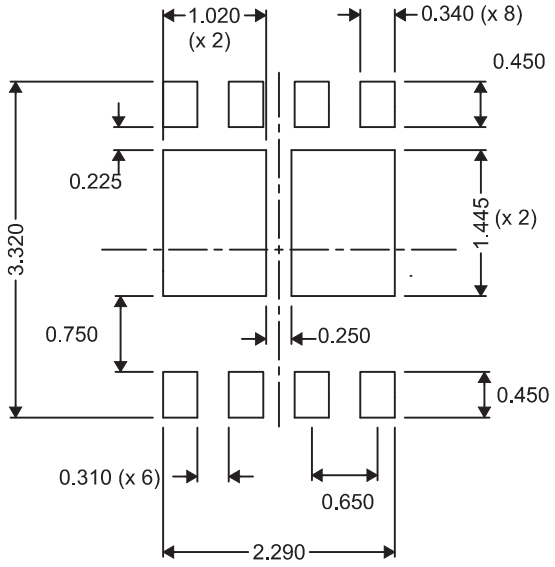
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1		0.310 NOM			0.012 NOM	
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e		0.650 TYP			0.026	
H	0.35	0.450	0.550	0.014	0.018	0.022
K		0.650 TYP			0.026 TYP	
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



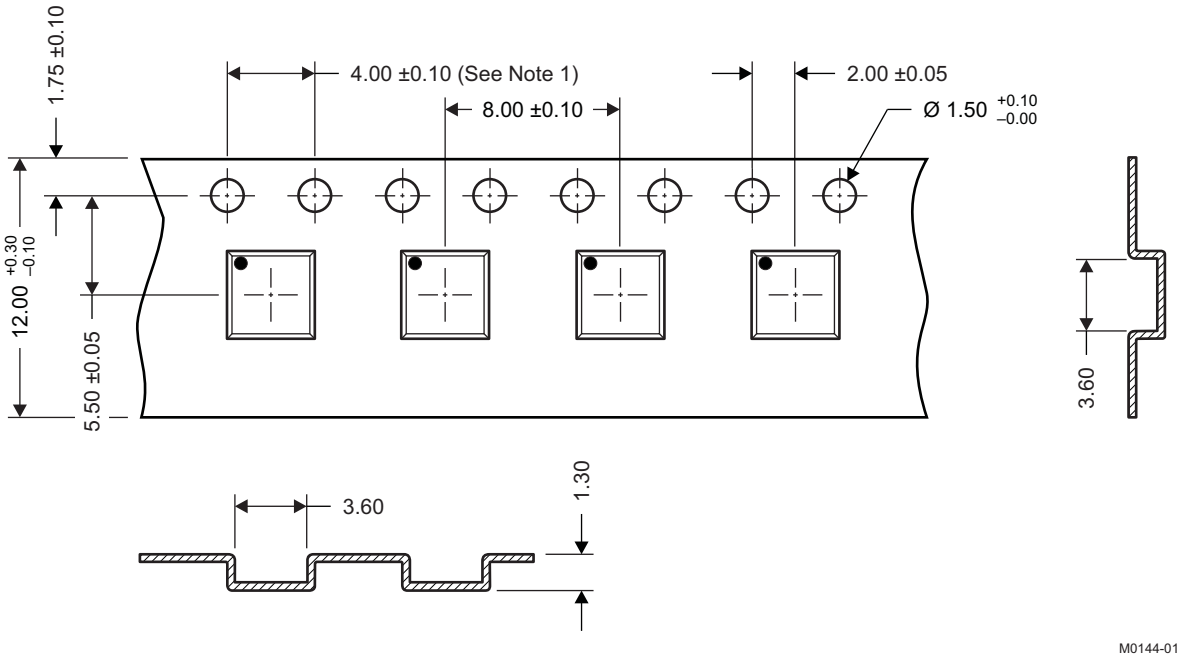
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ±0.05 mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17575Q3	Active	Production	VSON-CLIP (DQG) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-	CSD17575
CSD17575Q3.B	Active	Production	VSON-CLIP (DQG) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17575
CSD17575Q3T	Active	Production	VSON-CLIP (DQG) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17575
CSD17575Q3T.B	Active	Production	VSON-CLIP (DQG) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17575

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265