CSD17571Q2 30V N-Channel NexFET™ Power MOSFETs

1 Features

- Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 2 mm × 2 mm Plastic Package

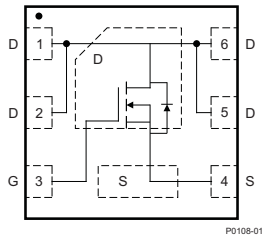
2 Applications

- Optimized for Load Switch Applications
- Storage, Tablets, and Handheld Devices
- Optimized for Control FET Applications

3 Description

This 30 V, 20 mΩ, SON 2×2 NexFET™ power MOSFET is designed to minimize losses in power conversion and load management applications, while offering excellent thermal performance for the size of the package.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	2.4		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.6		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	24	mΩ
		V_{GS} = 10 V	20	mΩ
$V_{GS(th)}$	Threshold Voltage	1.6		V

Ordering Information(1)

Device	Media	Qty	Package	Ship
CSD17571Q2	7-Inch Reel	3000	SON 2 x 2 mm Plastic Package	Tape and Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

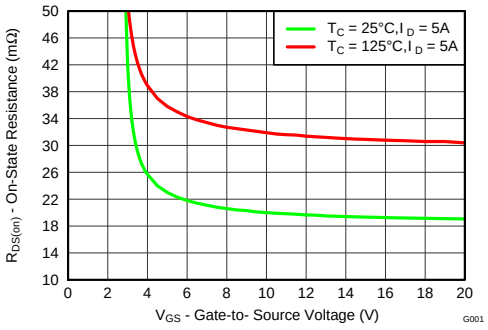
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limit)	22	A
	Continuous Drain Current(1)	7.6	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	39	A
P_D	Power Dissipation(1)	2.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 12 A, L = 0.1 mH, R_G = 25 Ω	7.2	mJ

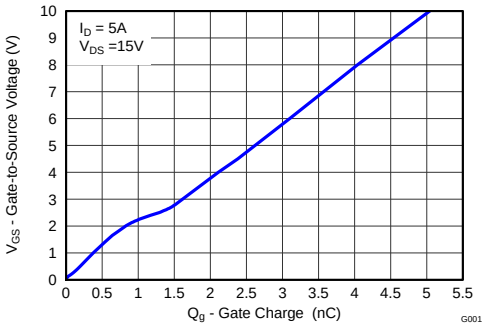
(1) $R_{\theta JA}$ = 50 on 1 in² Cu (2 oz.) on 0.060" thick FR4 PCB

(2) Pulse duration 10 µs, duty cycle ≤2%

$R_{DS(on)}$ vs V_{GS}



Gate Charge



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4 Revision History

Changes from Original (October 2013) to Revision A **Page**

- Updated Figure #8 6

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C

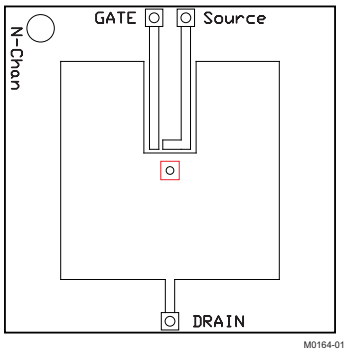
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.3	1.6	2	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_{DS} = 5 A		24	29	mΩ
		V_{GS} = 10 V, I_{DS} = 5 A		20	24	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 5 A		43		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		360	468	pF
C_{OSS}	Output Capacitance			101	131	pF
C_{RSS}	Reverse Transfer Capacitance			9	12	pF
R_g	Series Gate Resistance			3.8	7.6	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 15 V, I_{DS} = 5 A		2.4	3.1	nC
Q_{gd}	Gate Charge – Gate-to-Drain			0.6		nC
Q_{gs}	Gate Charge Gate-to-Source			0.9		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{OSS}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		3.4		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 5 A, R_G = 2 Ω		5.3		ns
t_r	Rise Time			19		ns
$t_{d(off)}$	Turn Off Delay Time			8		ns
t_f	Fall Time			2.6		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{DS} = 5 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 15 V, I_F = 5 A, di/dt = 300 A/µs		2.3		nC
t_{rr}	Reverse Recovery Time			11		ns

5.2 Thermal Information

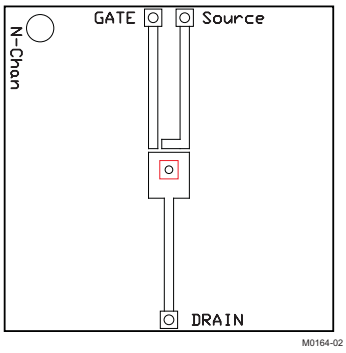
T_A = 25°C unless otherwise specified

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			6.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			65	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 65 when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 235 when mounted on minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C unless otherwise specified

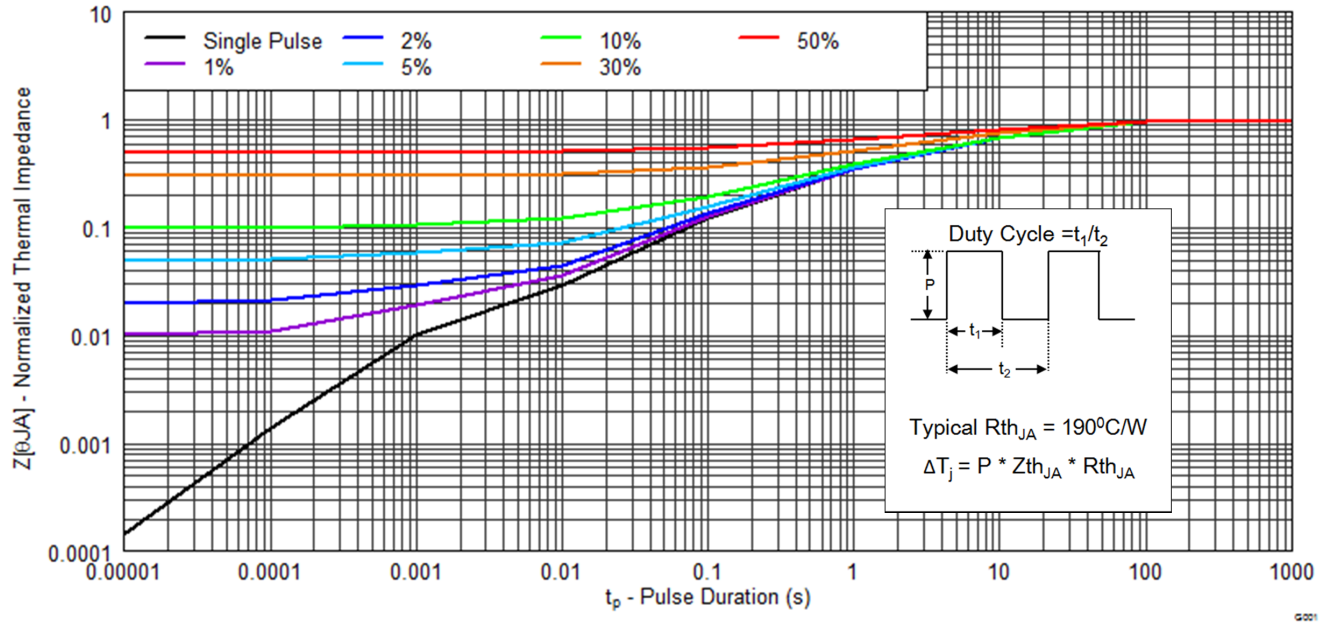


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise specified

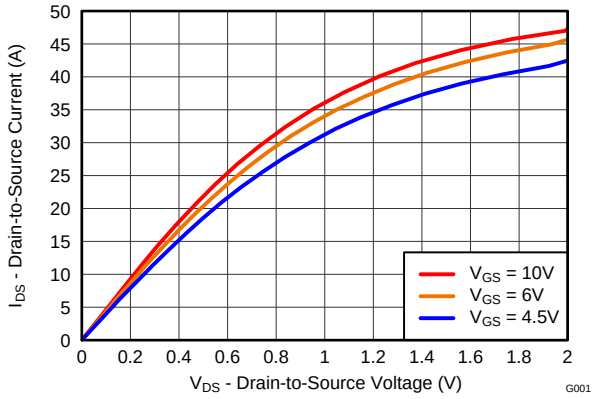


Figure 2. Saturation Characteristics

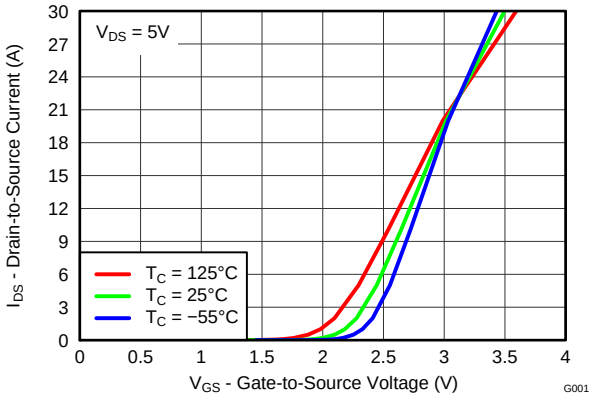


Figure 3. Transfer Characteristics

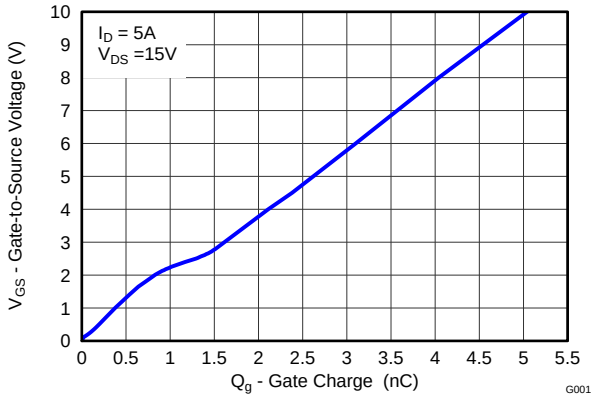


Figure 4. Gate Charge

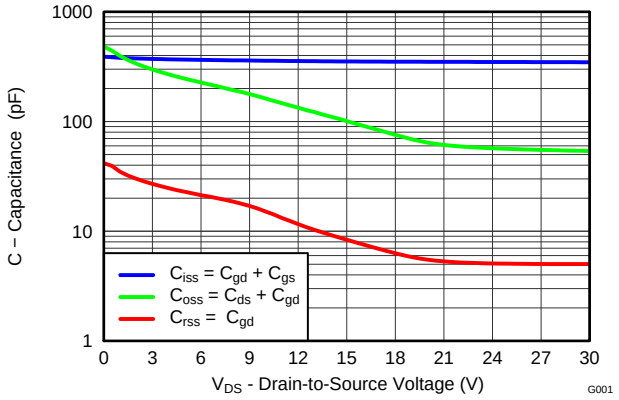


Figure 5. Capacitance

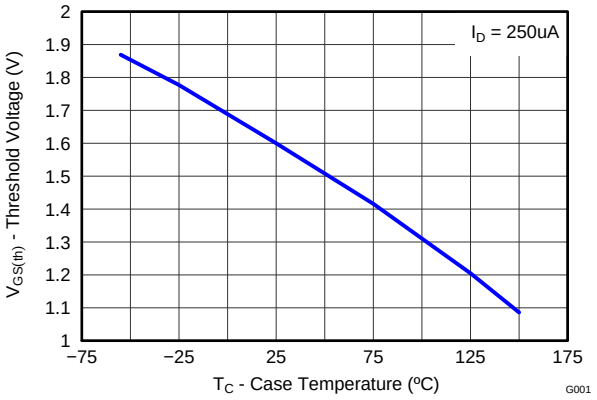


Figure 6. Threshold Voltage vs Temperature

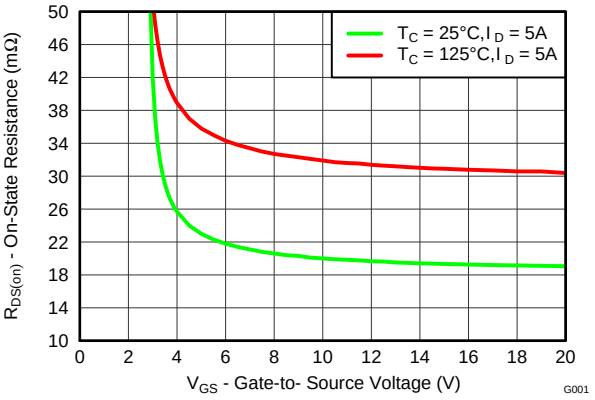


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise specified

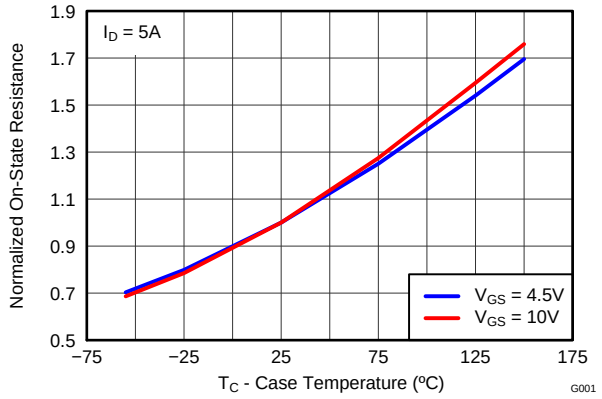


Figure 8. Normalized On-State Resistance vs Temperature

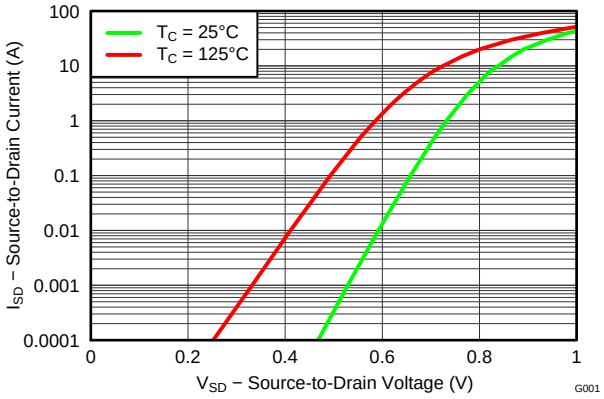


Figure 9. Typical Diode Forward Voltage

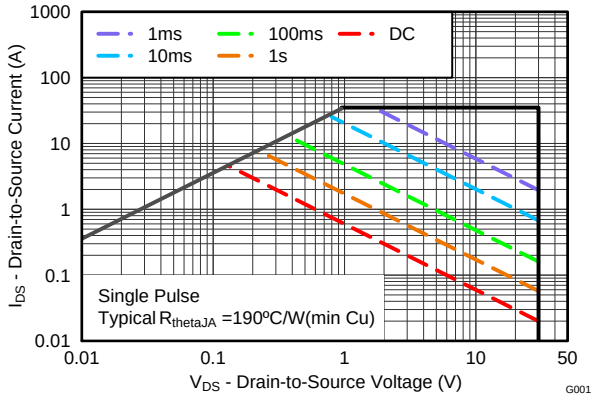


Figure 10. Maximum Safe Operating Area

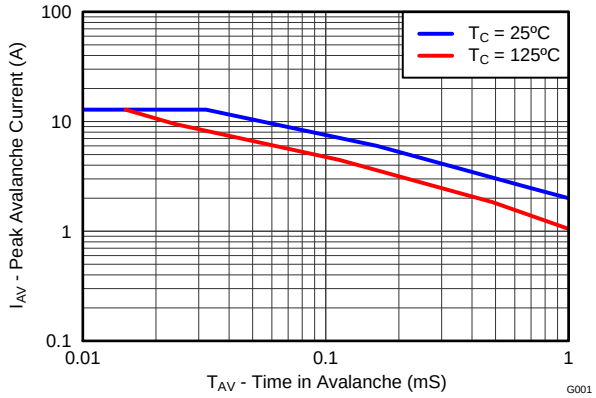


Figure 11. Single Pulse Unclamped Inductive Switching

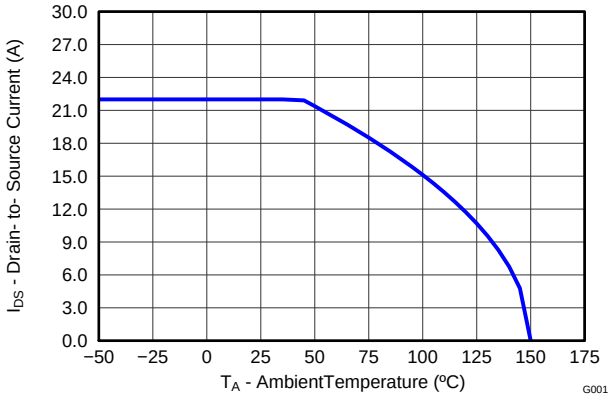


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

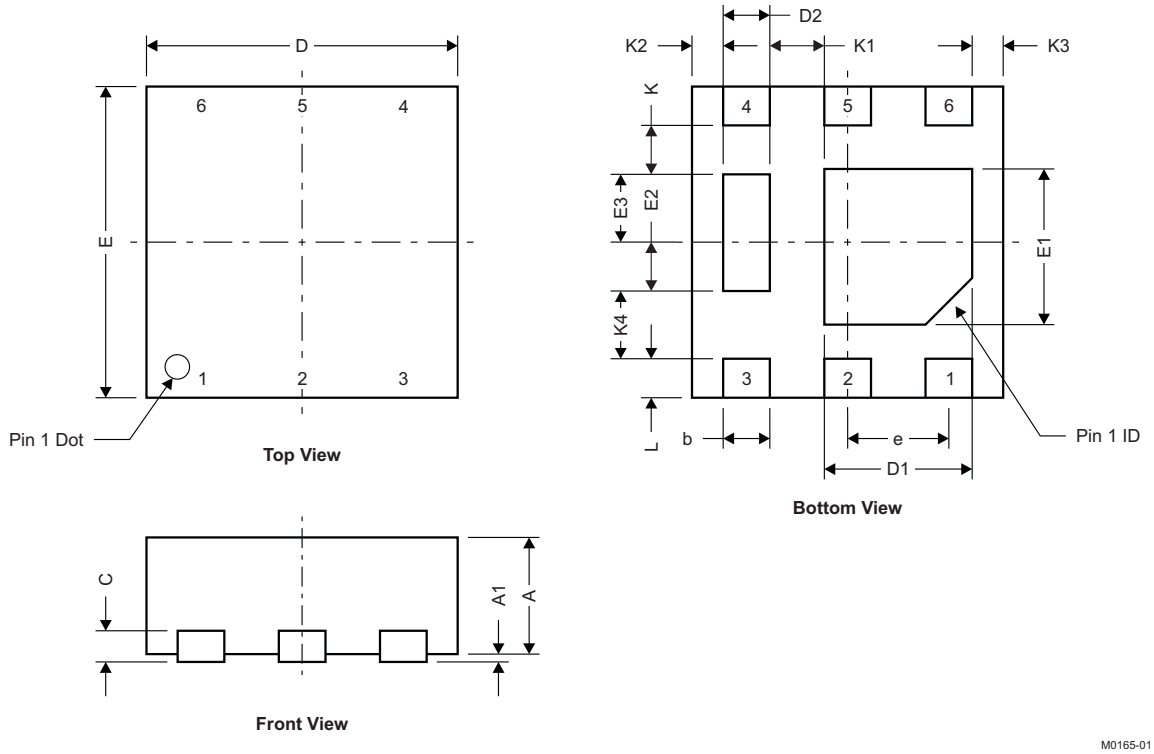
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

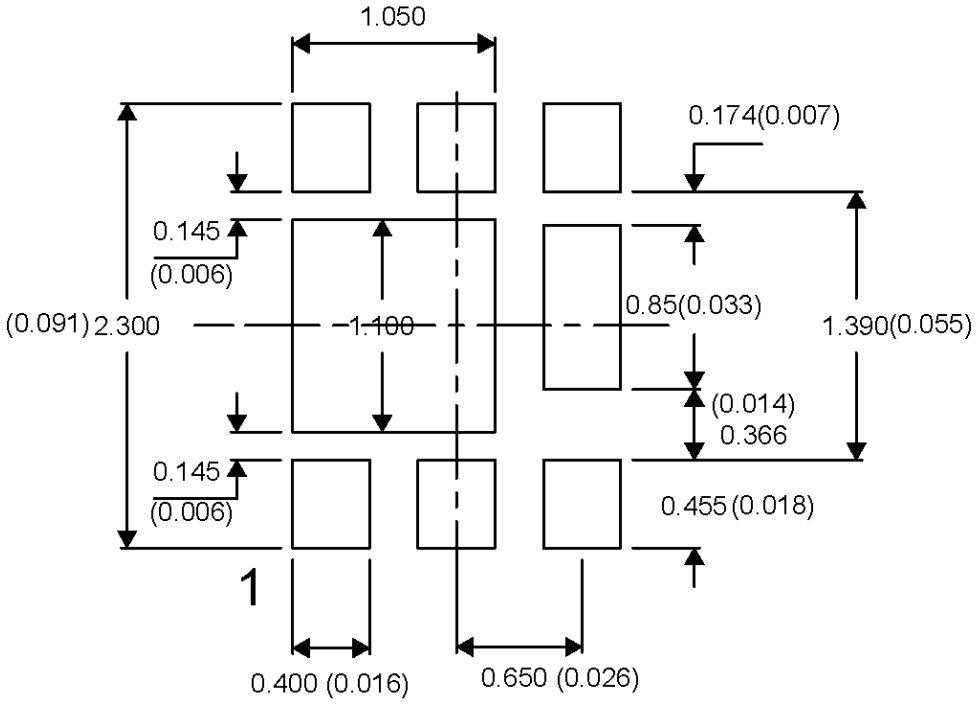
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q2 Package Dimensions



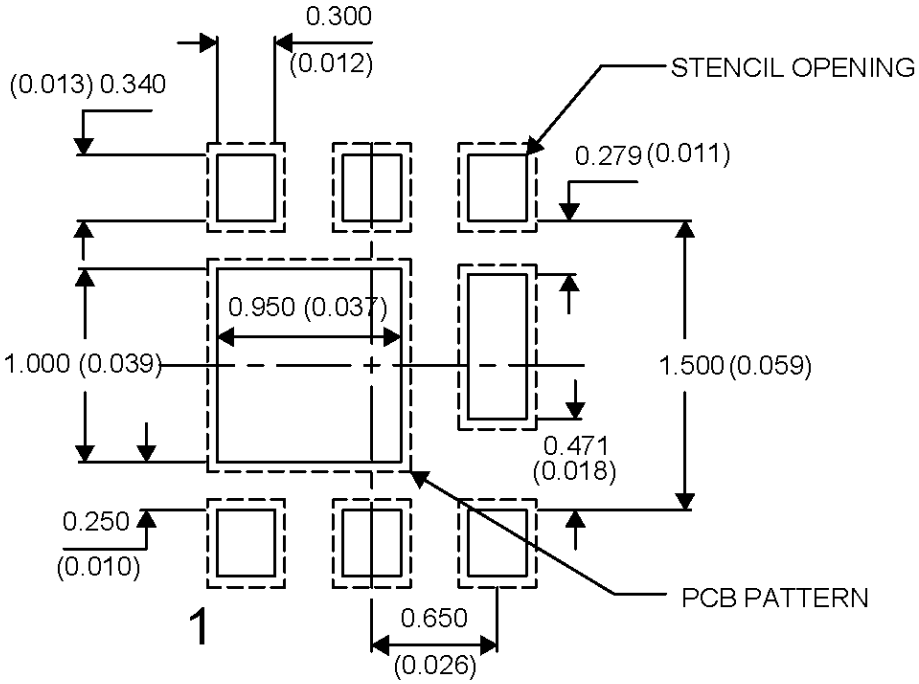
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C		0.203 TYP			0.008 TYP	
D		2.000 TYP			0.080 TYP	
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2		0.300 TYP			0.012 TYP	
E		2.000 TYP			0.080 TYP	
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2		0.280 TYP			0.0112 TYP	
E3		0.470 TYP			0.0188 TYP	
e		0.650 BSC			0.026 TYP	
K		0.280 TYP			0.0112 TYP	
K1		0.350 TYP			0.014 TYP	
K2		0.200 TYP			0.008 TYP	
K3		0.200 TYP			0.008 TYP	
K4		0.470 TYP			0.0188 TYP	
L	0.200	0.25	0.300	0.008	0.010	0.012

7.1.1 Recommended PCB Pattern



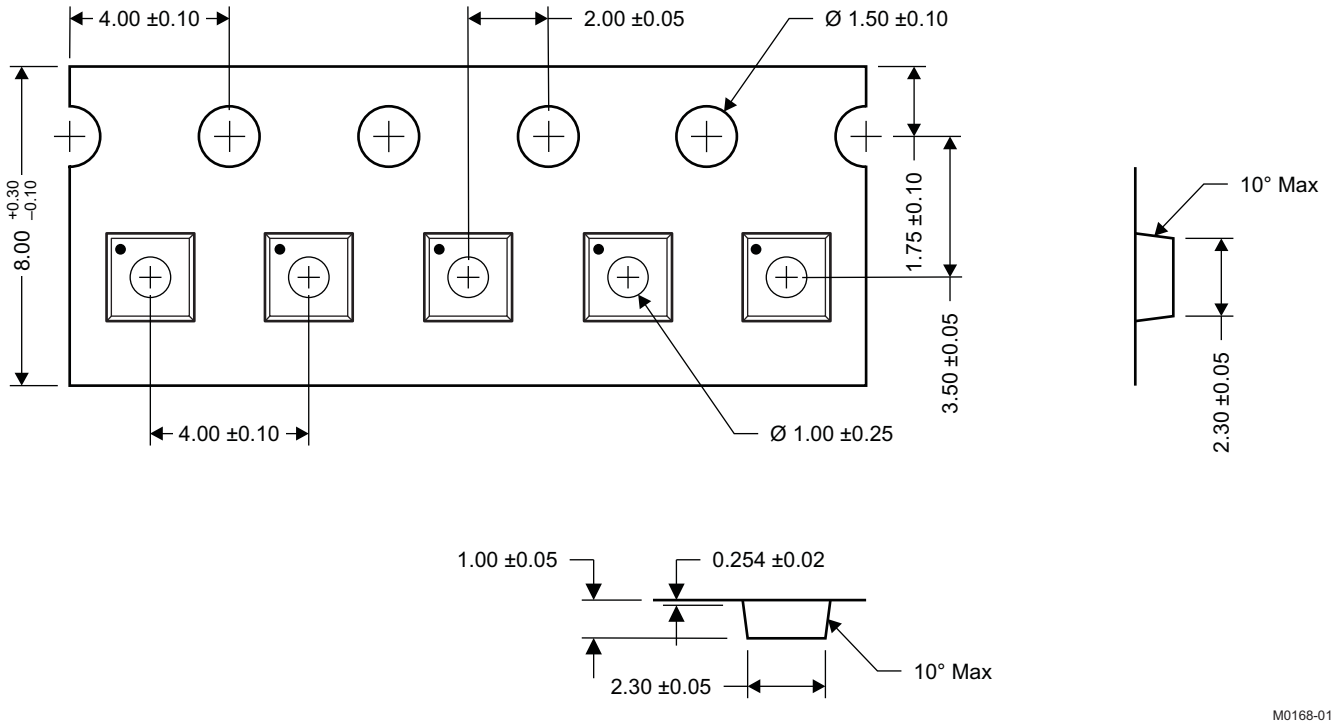
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.1.2 Recommended Stencil Pattern



Note: All dimensions are in mm, unless otherwise specified.

7.2 Q2 Tape and Reel Information



Notes: 1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ±0.20
3. Other material available
4. Typical SR of form tape Max 10^9 OHM/SQ
5. All dimensions are in mm, unless otherwise specified.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17571Q2	Active	Production	WSON (DQK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1751
CSD17571Q2.B	Active	Production	WSON (DQK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1751
CSD17571Q2G4.B	Active	Production	WSON (DQK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1751

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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