N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD16407Q5

FEATURES

- **Ultralow Qg and Qgd**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **SON 5-mm × 6-mm Plastic Package**

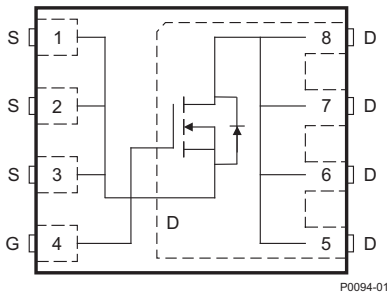
APPLICATIONS

- **Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems**
- **Optimized for Synchronous FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



PRODUCT SUMMARY

V_{DS}	Drain-to0source voltage	25		V
Q_g	Gate charge, total (4.5 V)	13.3		nC
Q_{gd}	Gate charge, gate-to-drain	3.5		nC
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V	2.5	mΩ
		V_{GS} = 10 V	1.8	mΩ
$V_{GS(th)}$	Threshold voltage	1.6		V

ORDERING INFORMATION

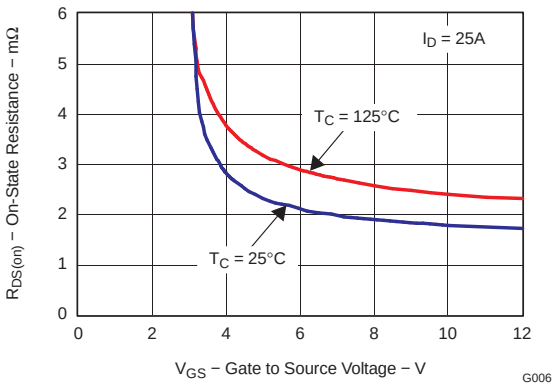
Device	Package	Media	Qty	Ship
CSD16407Q5	SON 5 × 6 plastic package	13-inch reel	2500	Tape and reel

ABSOLUTE MAXIMUM RATINGS

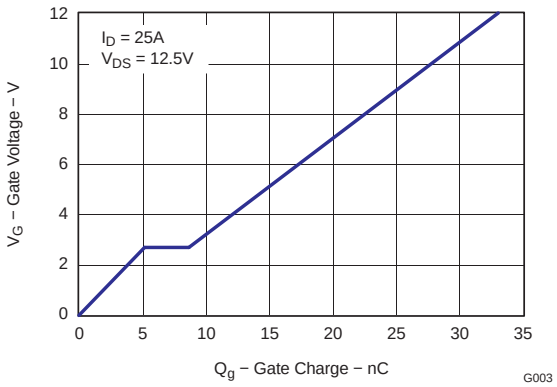
T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-source voltage	25	V
V_{GS}	Gate-to-source voltage	+16 / –12	V
I_D	Continuous drain current, T_C = 25°C	100	A
	Continuous drain current(1)	31	A
I_{DM}	Pulsed drain current, T_A = 25°C(2)	200	A
P_D	Power dissipation(1)	3.1	W
T_J, T_{STG}	Operating junction and storage temperature range	–55 to 150	°C
E_{AS}	Avalanche energy, single pulse I_D = 66A, L = 0.1 mH, R_G = 25 Ω	218	mJ

(1) $R_{\theta JA}$ = 40°C/W on 1 in^2 (6.45 cm^2) Cu [2 oz. (0.071 mm thick)] on 0.060-inch (1.52-mm) thick FR4 PCB.
(2) Pulse duration ≤300 μs, duty cycle ≤2%

$r_{DS(ON)}$ vs V_{GS}



Gate Charge



ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 16 V to –12 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.3	1.6	1.9	V
$r_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_D = 25 A		2.5	3.3	mΩ
		V_{GS} = 10 V, I_D = 25 A		1.8	2.4	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 25 A		111		S
Dynamic Characteristics						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		2040	2660	pF
C_{OSS}	Output capacitance			1600	2080	pF
C_{RSS}	Reverse transfer capacitance			115	160	pF
R_g	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5 V, I_D = 25 A		13.3	18	nC
Q_{gd}	Gate charge, gate-to-drain			3.5		nC
Q_{gs}	Gate charge, gate-to-source			5.3		nC
Qg(th)	Gate charge at Vth			3.1		nC
Q_{OSS}	Output charge	V_{DS} = 13.5 V, V_{GS} = 0 V		33		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 25 A R_G = 2 Ω		11.9		ns
t_r	Rise time			18.4		ns
$t_{d(off)}$	Turnoff delay time			16		ns
t_f	Fall time			9		ns
Diode Characteristics						
V_{SD}	Diode forward voltage	I_S = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 13.5 V, I_F = 25 A, di/dt = 300 A/μs		41		nC
t_{rr}	Reverse recovery time	V_{DD} = 13.5 V, I_F = 25 A, di/dt = 300 A/μs		34		ns

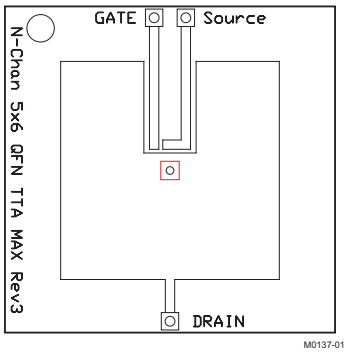
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

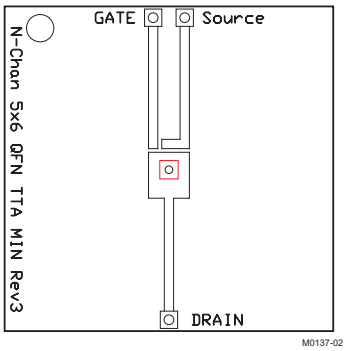
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case(1)			1.1	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient(1) (2)			51	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch (2.54-cm) square 2-oz (0.071-mm thick). Cu pad on a 1.5-inch (3.81-cn) × 1.5-inch (3.81-cm) × 0.060-inch (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1 $inch^2$ (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 121°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

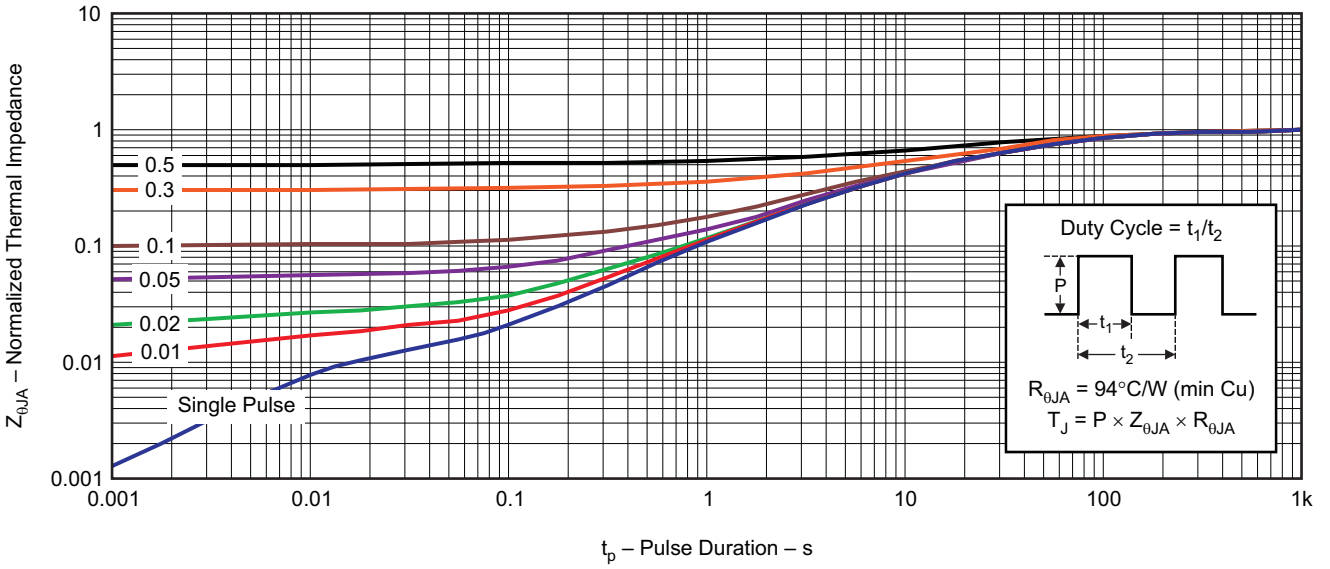


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

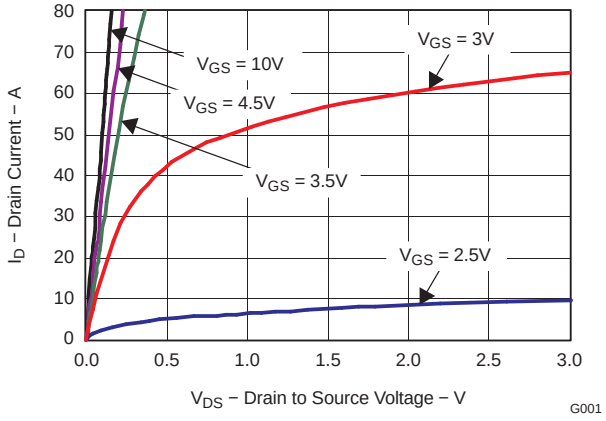


Figure 2. Saturation Characteristics

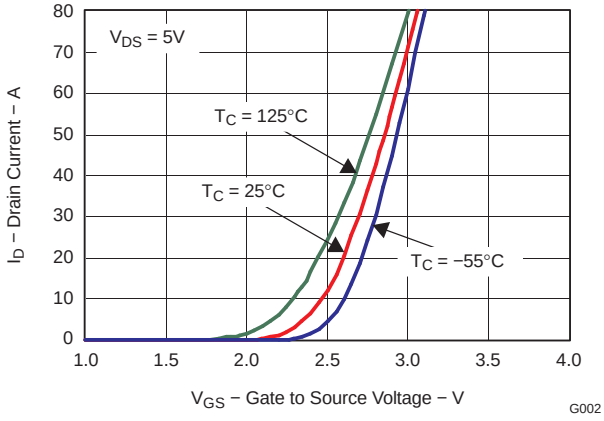


Figure 3. Transfer Characteristics

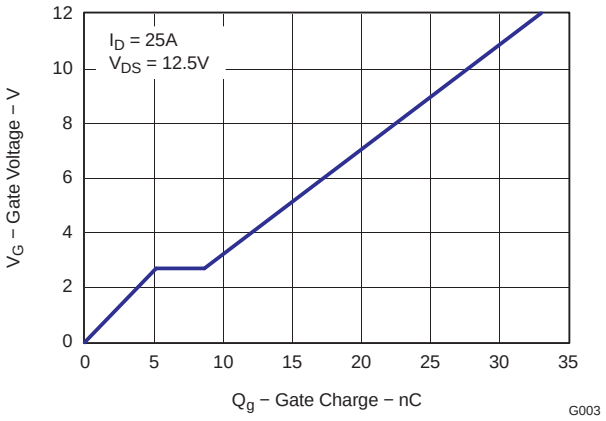


Figure 4. Gate Charge

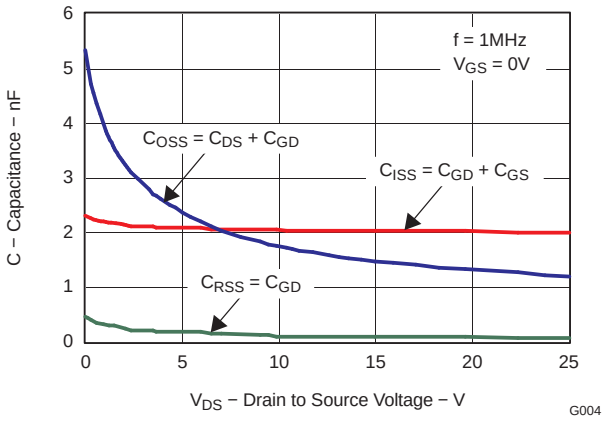


Figure 5. Capacitance

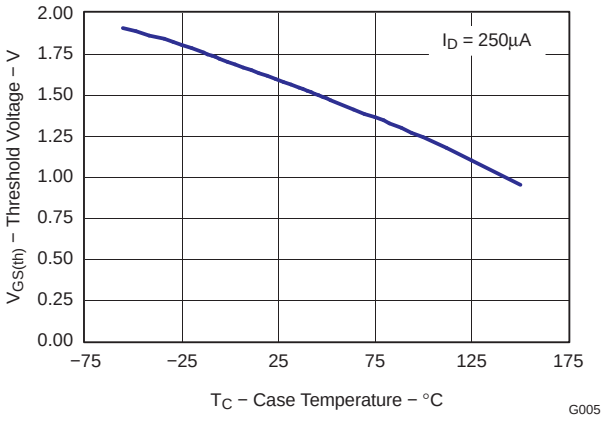


Figure 6. Threshold Voltage vs. Temperature

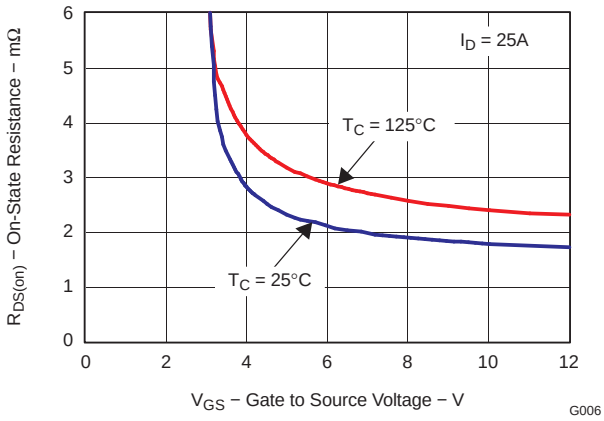


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

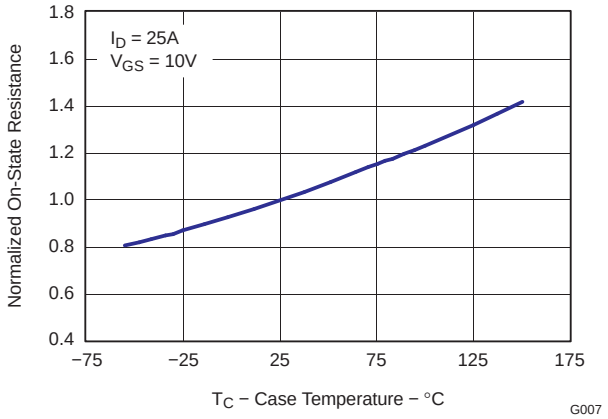


Figure 8. On Resistance vs. Temperature

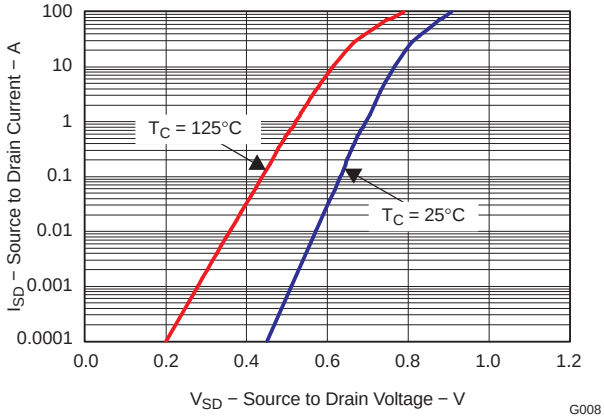


Figure 9. Typical Diode Forward Voltage

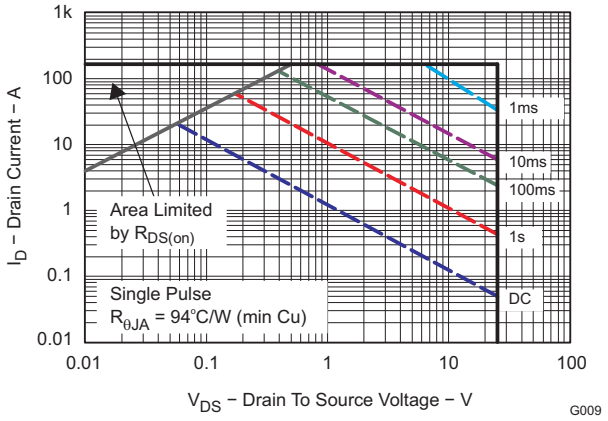


Figure 10. Maximum Safe Operating Area

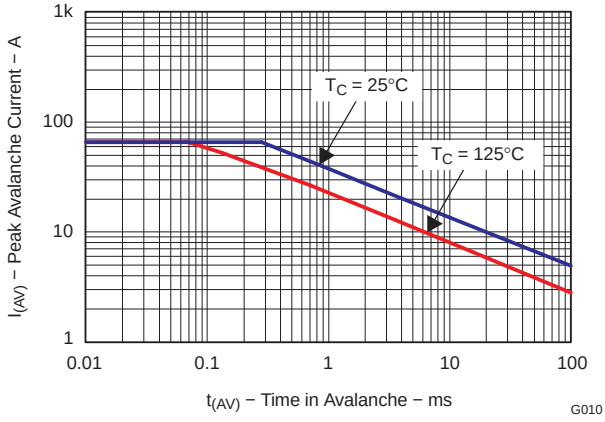


Figure 11. Single Pulse Unclamped Inductive Switching

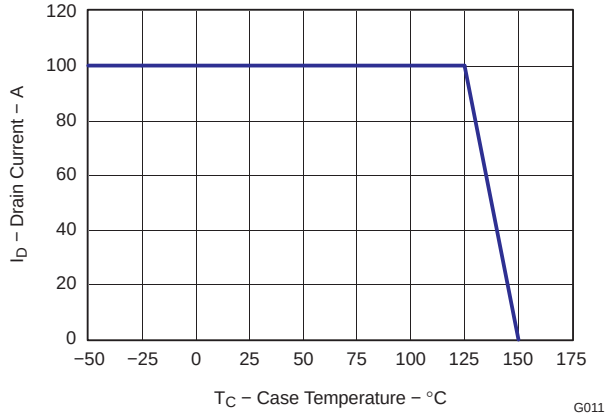
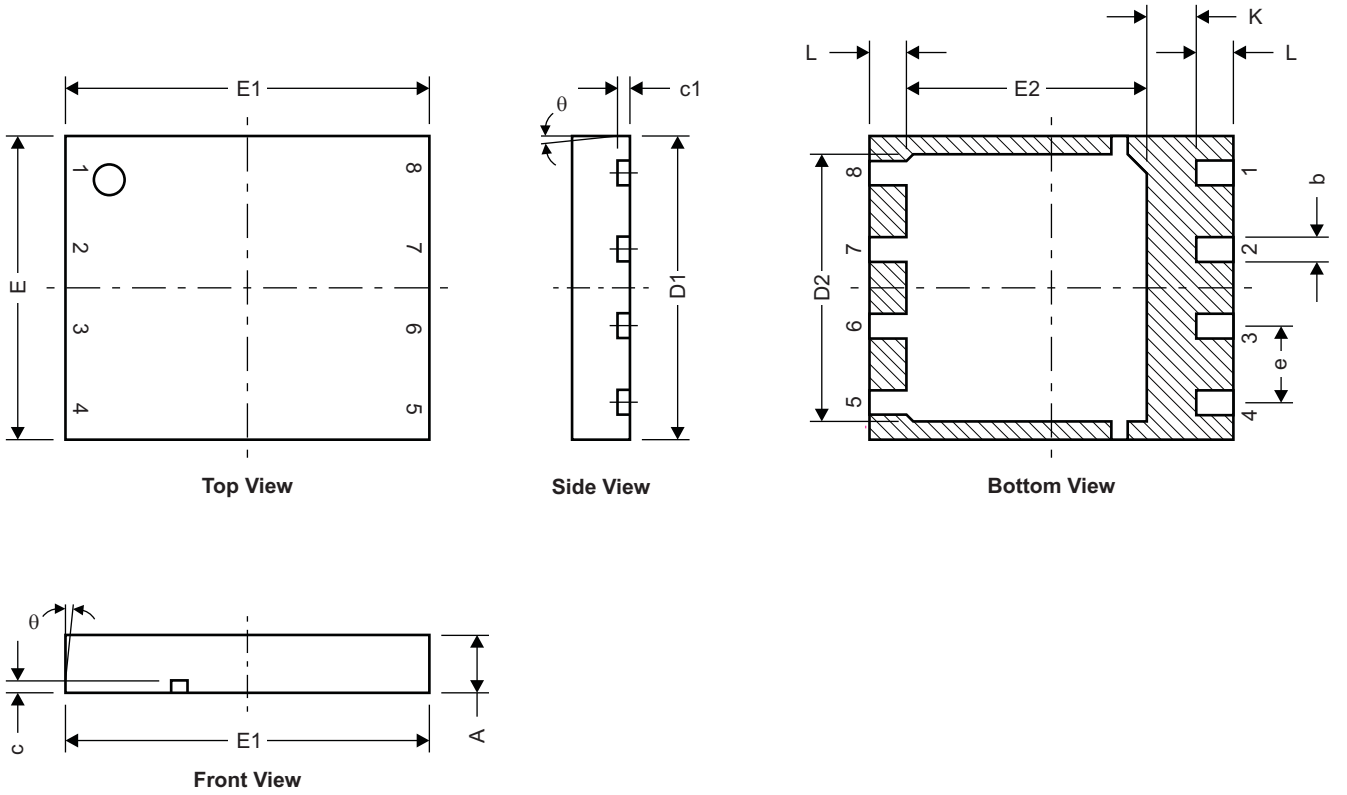


Figure 12. Maximum Drain Current vs. Temperature

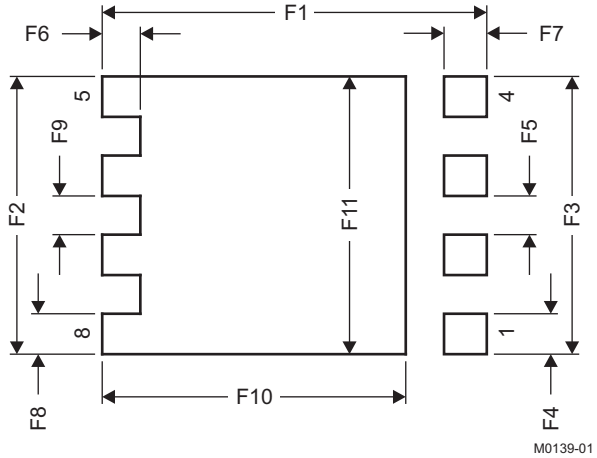
MECHANICAL DATA

Q5 Package Dimensions



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
L	0.510	0.710	0.020	0.028
θ	0.00	–	–	–
K	0.760	–	0.030	–

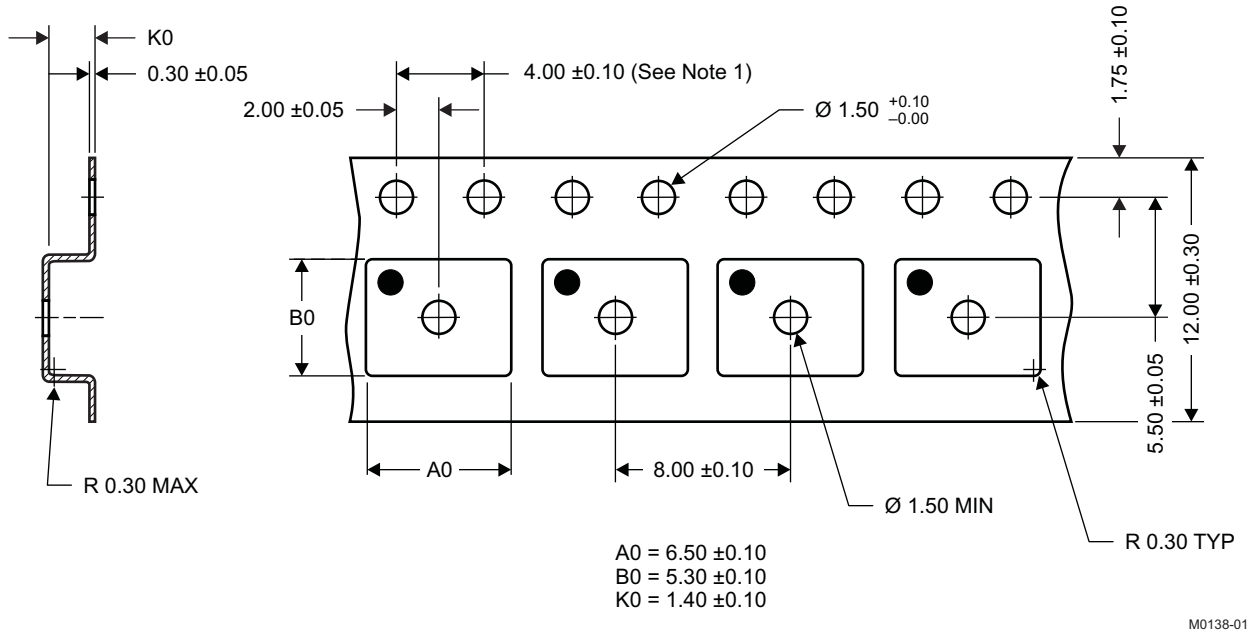
Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.2440	0.248
F2	4.460	4.560	0.1760	0.180
F3	4.460	4.560	0.1760	0.180
F4	0.650	0.700	0.0260	0.028
F5	0.620	0.670	0.0240	0.026
F6	0.630	0.680	0.0250	0.027
F7	0.70	0.800	0.0380	0.031
F8	0.650	0.700	0.0260	0.028
F9	0.620	0.670	0.0240	0.026
F10	4.900	5.000	0.1930	0.197
F11	4.460	4.560	0.1760	0.180

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q5 Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm IN 100 mm, noncumulative over 250 mm
3. Material:black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: 0.30 ±0.05 mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

REVISION HISTORY

Changes from Revision Original (August 2009) to Revision A	Page
• Deleted environmental bullets from features list	1
• Deleted package marking at end of data sheet	7

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16407Q5	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16407
CSD16407Q5.B	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16407

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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