CSD16321Q5 25V N-Channel NexFET™ Power MOSFET

1 Features

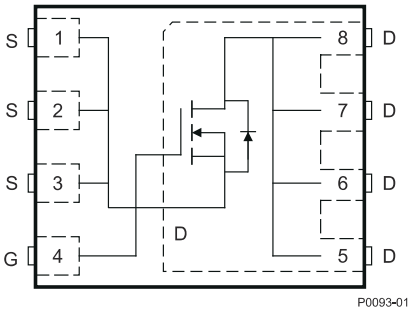
- Optimized for 5V gate drive
- Ultra-low Q_g and Q_{gd}
- Low-thermal resistance
- Avalanche rated
- Lead-free terminal plating
- RoHS compliant
- SON 5mm × 6mm plastic package

2 Applications

- Point-of-load synchronous buck converter for applications in networking, telecom, and computing systems
- Optimized for synchronous FET applications

3 Description

This 25V, 1.9mΩ, 5mm × 6mm SON NexFET™ power MOSFET has been designed to minimize losses in power conversion and optimized for 5V gate drive applications.



Top View

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	14		nC
Q_{gd}	Gate Charge Gate-to-Drain	2.5		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 3V	2.8	mΩ
		V_{GS} = 4.5V	2.1	
		V_{GS} = 8V	1.9	
$V_{GS(th)}$	Threshold Voltage	1.1		V

Device Information(1)

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD16321Q5	13-Inch Reel	2500	SON 5.00mm × 6.00mm Plastic Package	Tape and Reel
CSD16321Q5T	7-Inch Reel	250		

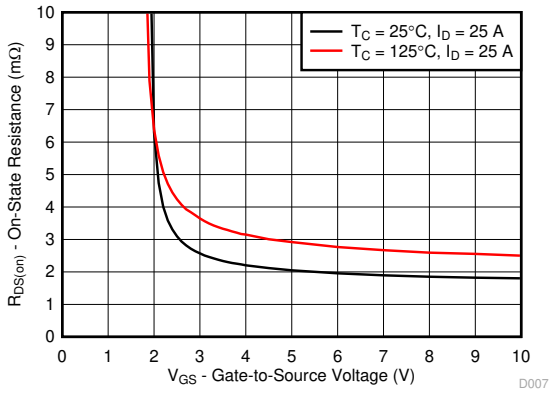
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

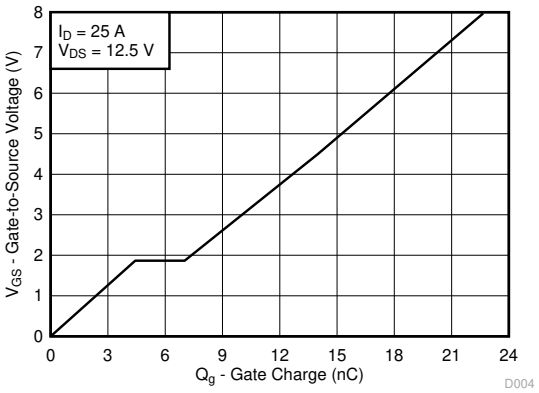
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	+10 / –8	V
I_D	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	177	
	Continuous Drain Current(1)	29	
I_{DM}	Pulsed Drain Current(2)	400	A
P_D	Power Dissipation(1)	3.1	W
	Power Dissipation, T_C = 25°C	113	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 66A, L = 0.1mH, R_G = 25Ω	218	mJ

(1) Typical $R_{\theta JA}$ = 40°C/W on 1in², 2oz Cu pad on 0.06in thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.1°C/W, pulse duration ≤ 100µs, duty cycle ≤ 1%.



$R_{DS(ON)}$ vs V_{GS}



Gate Charge

Table of Contents

4 Specifications

4.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

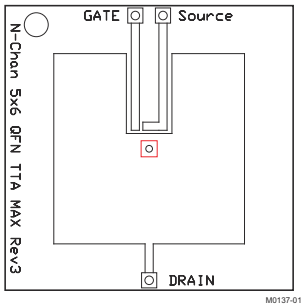
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 250µA	25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 20V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = +10 / –8V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 3V, I_D = 25A		2.8	3.8	mΩ
		V_{GS} = 4.5V, I_D = 25A		2.1	2.6	
		V_{GS} = 8V, I_D = 25A		1.9	2.4	
g_{fs}	Transconductance	V_{DS} = 12.5V, I_D = 25A		150		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz		2360	3100	pF
C_{oss}	Output capacitance			1700	2200	pF
C_{rss}	Reverse transfer capacitance			115	150	pF
R_G	Series gate resistance			1.5	3	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5V, I_D = 25A		14	19	nC
Q_{gd}	Gate charge gate-to-drain			2.5		nC
Q_{gs}	Gate charge gate-to-source			4		nC
$Q_{g(th)}$	Gate charge at V_{th}			2.1		nC
Q_{oss}	Output charge	V_{DS} = 15V, V_{GS} = 0V		36		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 25A, R_G = 2Ω		9		ns
t_r	Rise time			15		ns
$t_{d(off)}$	Turnoff delay time			27		ns
t_f	Fall time			17		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 25A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 13V, I_F = 25A, di/dt = 300A/µs		33		nC
t_{rr}	Reverse recovery time	V_{DD} = 13V, I_F = 25A, di/dt = 300A/µs		32		ns

4.2 Thermal Information

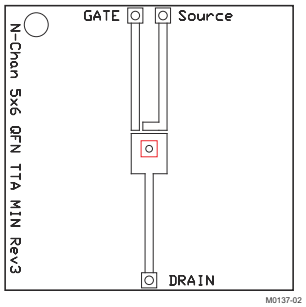
T_A = 25°C (unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			1.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1in^2, 2oz Cu pad on a 1.5in × 1.5in, 0.06in thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 Material with 1 in^2 of 2oz Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1in^2 of 2oz Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2oz Cu.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

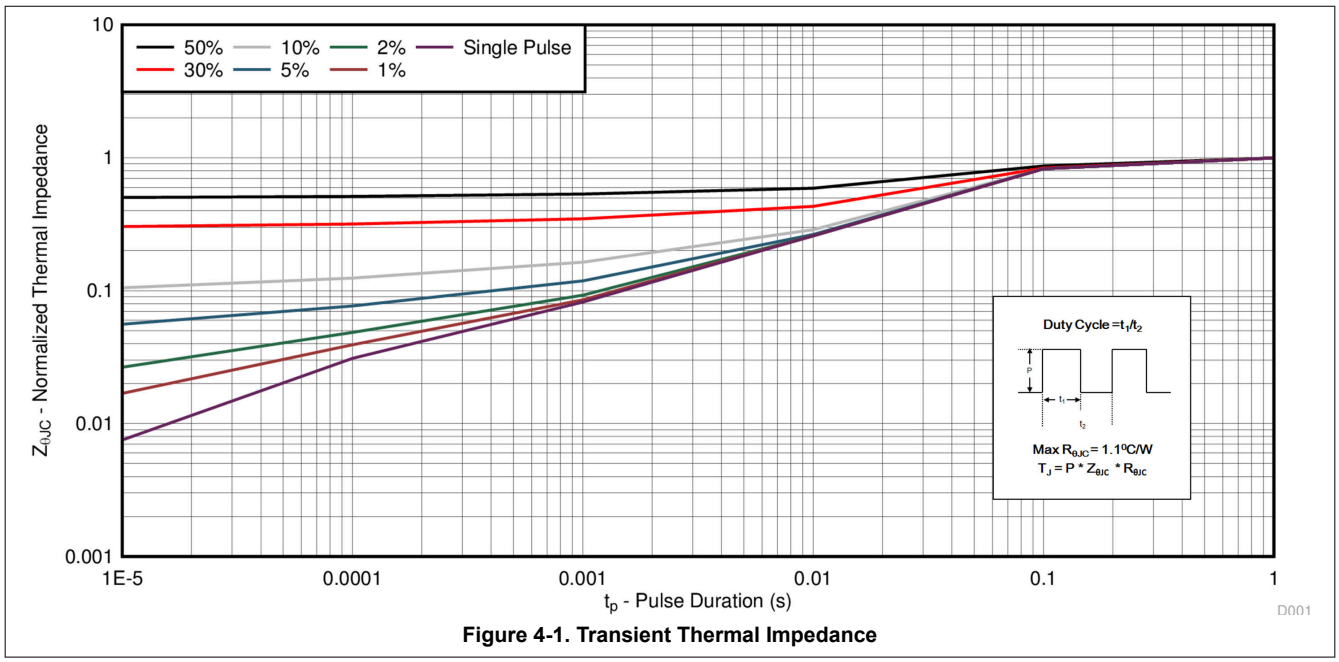


Figure 4-1. Transient Thermal Impedance

4.3 Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

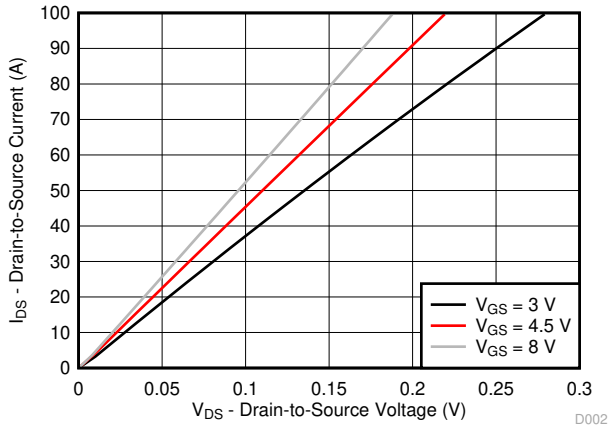
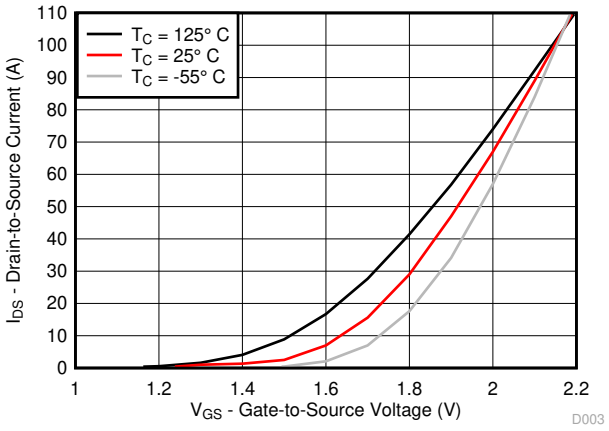
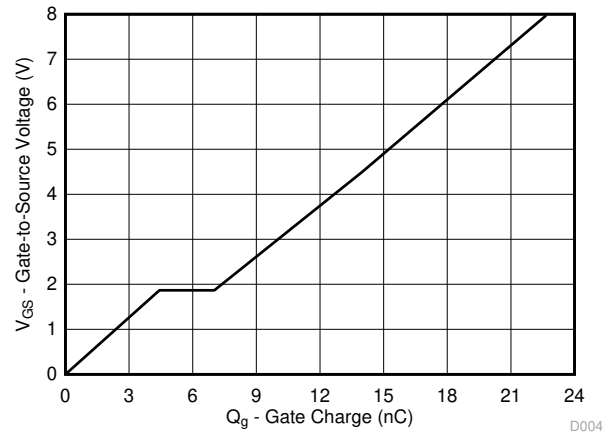


Figure 4-2. Saturation Characteristics



V_{DS} = 5V

Figure 4-3. Transfer Characteristics



V_{DS} = 12.5V I_D = 25A

Figure 4-4. Gate Charge

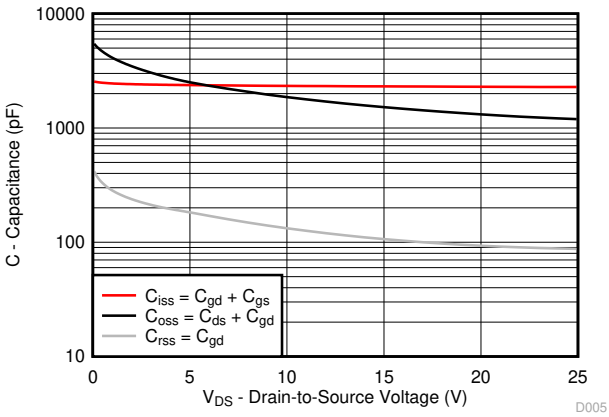
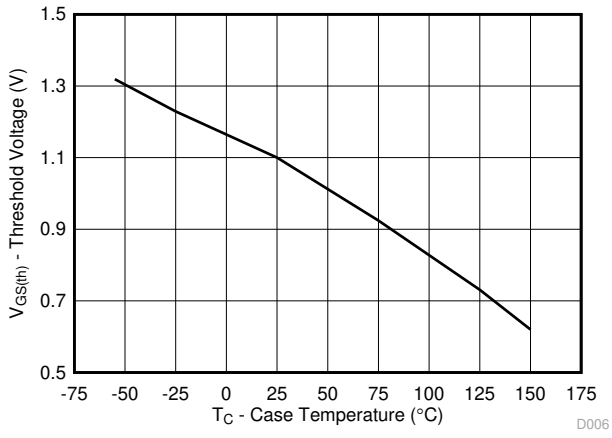


Figure 4-5. Capacitance



I_D = 250µA

Figure 4-6. Threshold Voltage vs Temperature

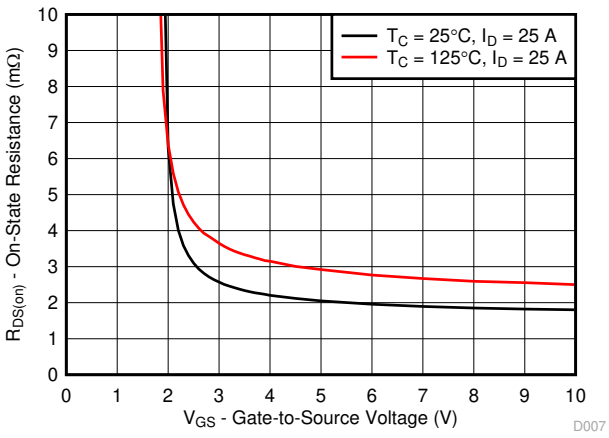
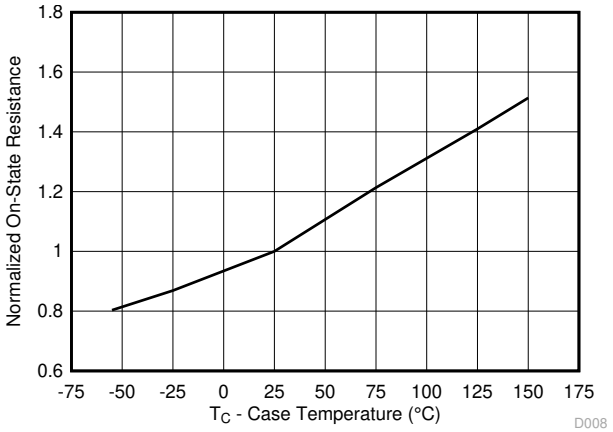


Figure 4-7. On Resistance vs Gate Voltage

4.3 Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



I_D = 25A V_{GS} = 8V

Figure 4-8. On Resistance vs Temperature

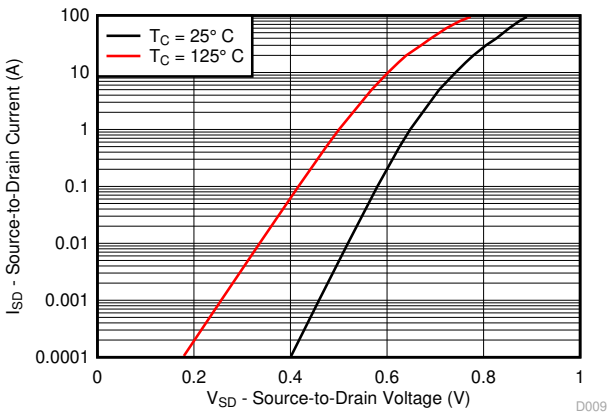
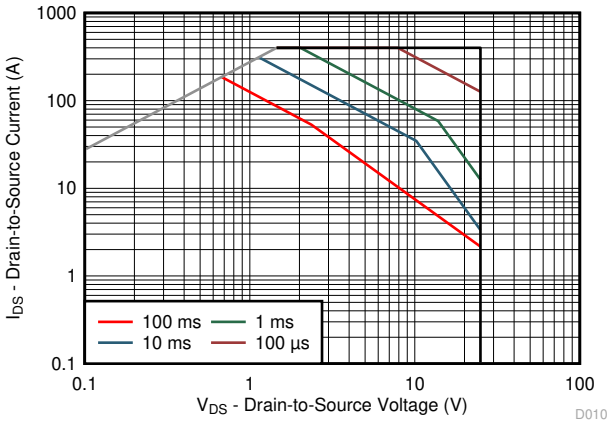


Figure 4-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 1.1°C/W

Figure 4-10. Maximum Safe Operating Area

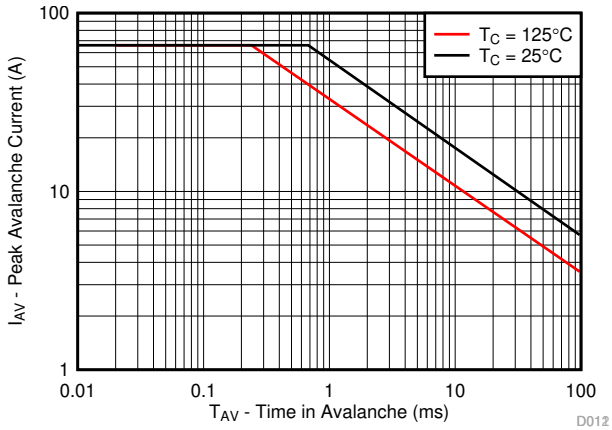


Figure 4-11. Single Pulse Unclamped Inductive Switching

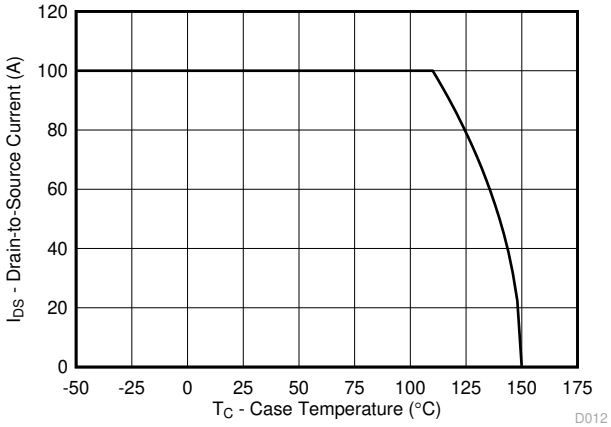


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.3 Trademarks

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5.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2017) to Revision E (December 2023) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision C (December 2016) to Revision D (May 2017) **Page**

- Changed the $R_{DS(ON)}$ values at 3 V, 4.5 V, 8 V & the *Description* to match the values on the *Electrical Characteristics* table. 1

Changes from Revision B (May 2010) to Revision C (December 2016) **Page**

- Changed *Description* text..... 1
- Added silicon limited continuous drain current to *Absolute Maximum Ratings* table..... 1
- Added max power dissipation at T_C = 25°C to *Absolute Maximum Ratings* table..... 1
- Changed Note 2 in *Absolute Maximum Ratings* table..... 1
- Changed $R_{\theta JA}$ max from 48°C/W : to 50°C/W..... 3
- Changed the SOA in Figure 4-10 to reflect measured data..... 4
- Changed *MECHANICAL DATA* section to *Mechanical, Packaging, and Orderable Information* section..... 9

Changes from Revision A (January 2010) to Revision B (May 2010) **Page**

- Changed $R_{DS(on)}$ - V_{GS} = 3V, I_D = 25A MAX value From: 3.5 To: 3.8..... 3

Changes from Revision * (August 2009) to Revision A (January 2010) **Page**

- Changed the labels on the Top View pinout image..... 1
- Changed Note 1 of the *Absolute Maximum Ratings* From: $R_{\theta JA}$ = 39°C/W To: Typical $R_{\theta JA}$ = 39°C/W..... 1
- Changed Figure 4-1 text From: $R_{\theta JA}$ = 92°C/W To: Typical $R_{\theta JA}$ = 93°C/W..... 4
- Changed Figure 4-10 text From: $R_{\theta JA}$ = 92°C/W To: Typical $R_{\theta JA}$ = 93°C/W..... 4
- Changed Figure 4-11 X-axis values..... 4

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16321Q5	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321
CSD16321Q5.B	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321
CSD16321Q5T	Active	Production	VSON-CLIP (DQH) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321
CSD16321Q5T.B	Active	Production	VSON-CLIP (DQH) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

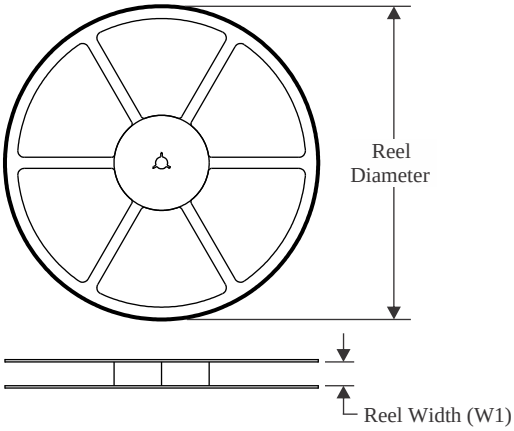
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

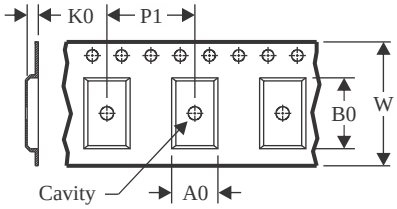
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

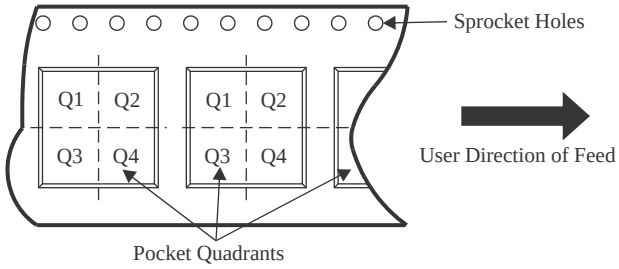


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

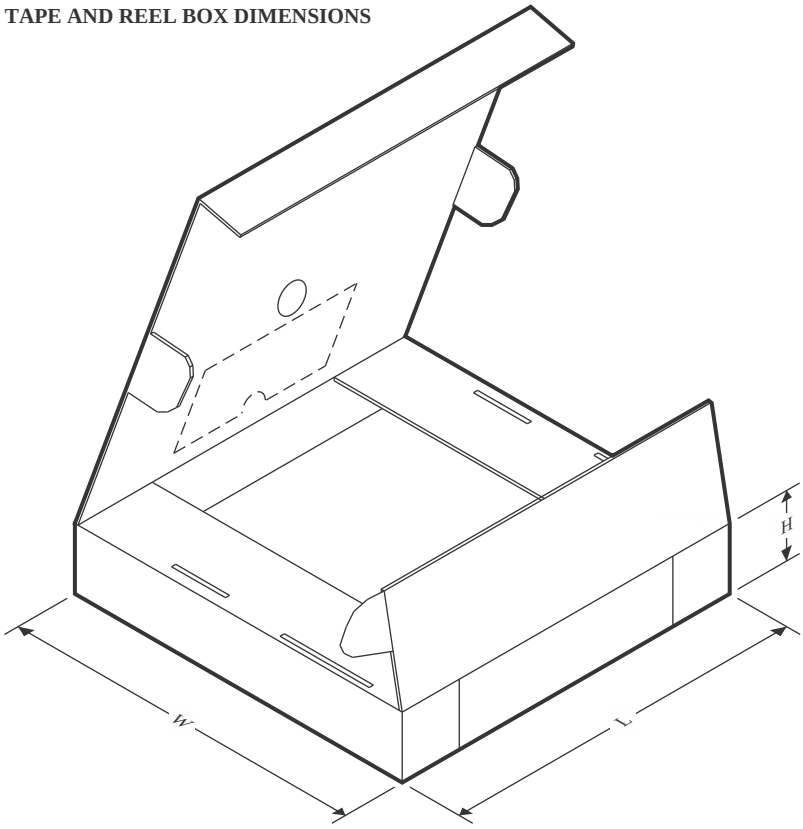
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16321Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

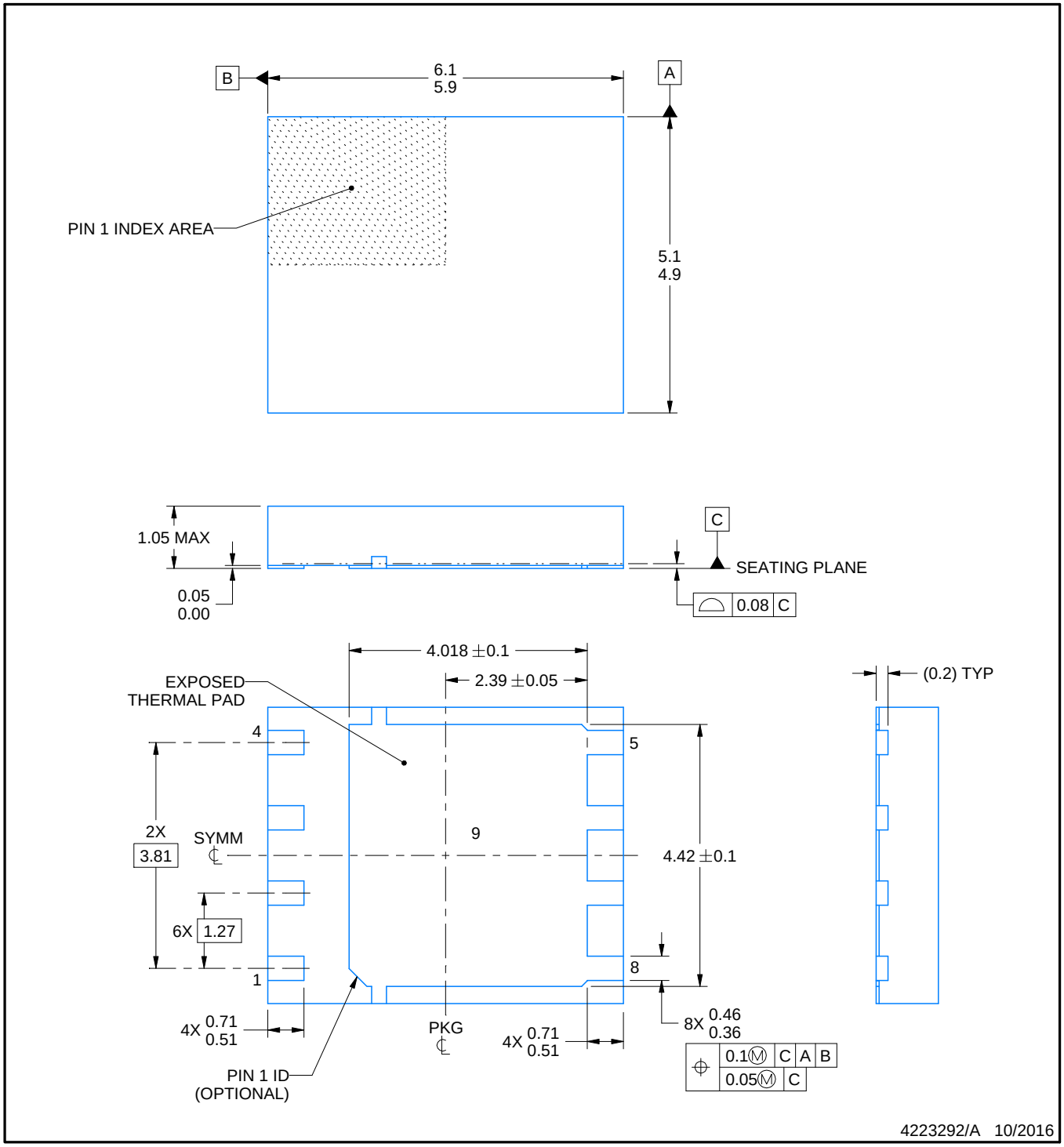
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16321Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0

PACKAGE OUTLINE

DQH0008A

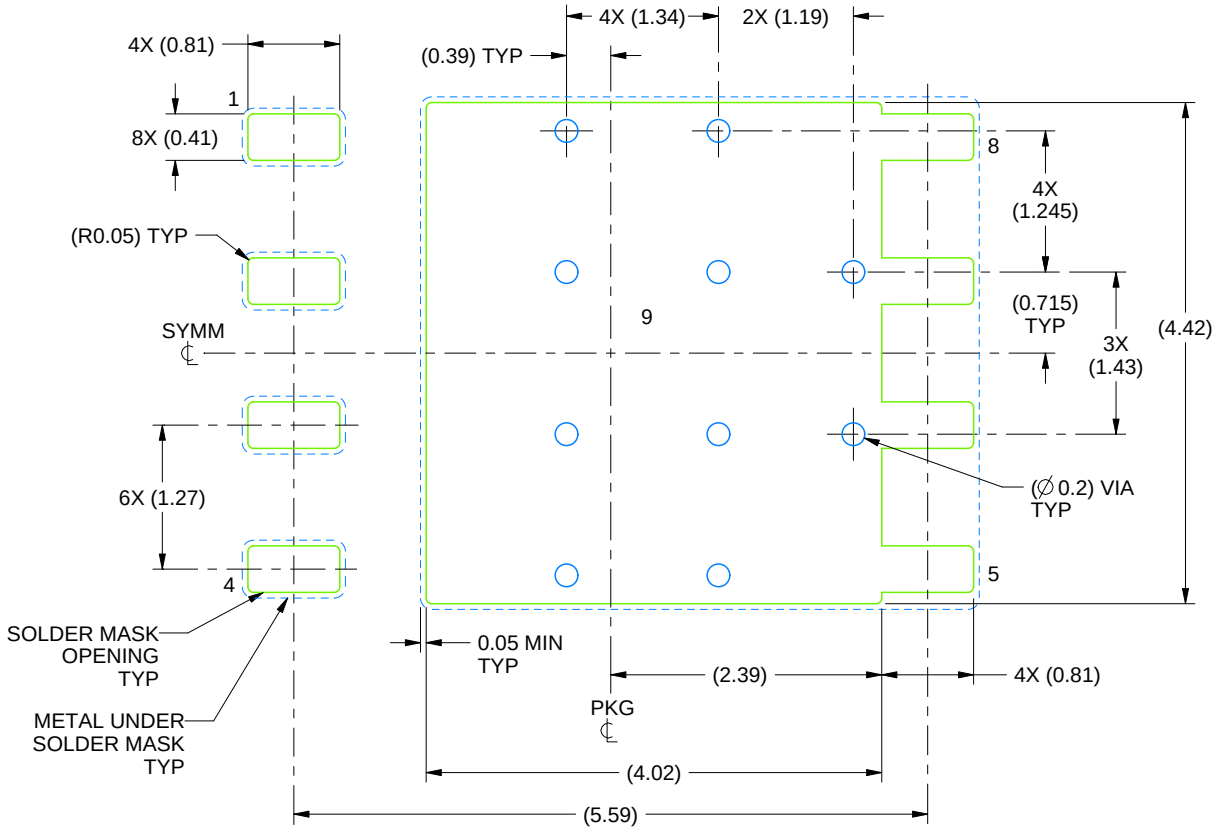
VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

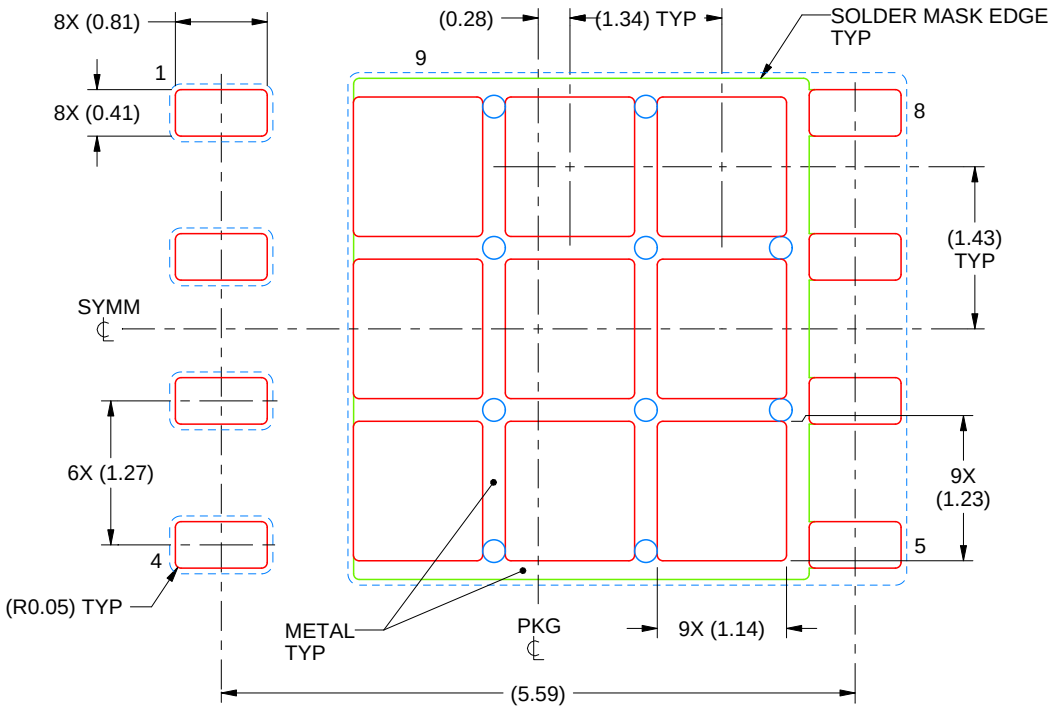


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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