CSD13381F4 12-V N-Channel FemtoFET™ MOSFET

1 Features

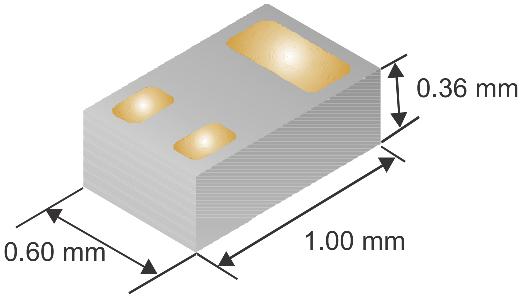
- Low on-resistance
- Low Q_g and Q_{gd}
- Low threshold voltage
- Ultra-small footprint (0402 case size)
  - 1.0 mm × 0.6 mm
- Ultra-low profile
  - Maximum height: 0.36-mm
- Integrated ESD protection diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Single-cell battery applications
- Handheld and mobile applications

3 Description

This 140-mΩ, 12-V N-channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.



Typical Device Dimensions

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-source voltage	12		V
Q_g	Gate charge total (4.5 V)	1060		pC
Q_{gd}	Gate charge gate-to-drain	140		pC
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 1.8 V	310	mΩ
		V_{GS} = 2.5 V	170	mΩ
		V_{GS} = 4.5 V	140	mΩ
$V_{GS(th)}$	Threshold voltage	0.85		V

Ordering Information

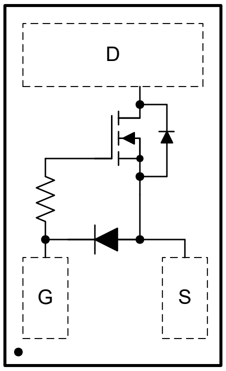
DEVICE(1)	QTY	MEDIA	PACKGE	SHIP
CSD13381F4	3000	7-inch reel	Femto (0402) 1.0-mm × 0.6-mm SMD lead less	Tape and reel
CSD13381F4T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-source voltage	12	V
V_{GS}	Gate-to-source voltage	8	V
I_D	Continuous drain current, T_A = 25°C(1)	2.1	A
I_{DM}	Pulsed drain current, T_A = 25°C(2)	7	A
I_G	Continuous gate clamp current	35	mA
	Pulsed gate clamp current(2)	350	
P_D	Power dissipation(1)	500	mW
ESD Rating	Human body model (HBM)	4	kV
	Charged device model (CDM)	2	kV
T_J, T_{stg}	Operating junction and storage temperature range	–55 to 150	°C
E_{AS}	Avalanche energy, single pulse I_D = 7.4 A, L = 0.1 mH, R_G = 25 Ω	2.7	mJ

(1) Typical $R_{\theta JA}$ = 90°C/W on 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.
(2) Pulse duration ≤ 300 µs, duty cycle ≤ 2%



Top View

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2021) to Revision F (January 2022)	Page
• Changed Maximum height from "0.35 mm" to "0.36 mm" in *Features*	1
• Changed package height from "0.35 mm" to "0.36 mm" in *Typical Device Dimensions*	1
• Changed package height from "0.35 mm" to "0.36 mm" in *Mechanical Dimensions*	8

Changes from Revision D (May 2015) to Revision E (October 2021)	Page
• Added footnote with link to support document	9

Changes from Revision C (September 2014) to Revision D (May 2015)	Page
• Corrected typo for I_{GSS} Test Condition	3

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	12			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 9.6 V			100	nA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 8 V			50	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	0.65	0.85	1.10	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 1.8 V, I_{DS} = 0.5 A		310	400	mΩ
		V_{GS} = 2.5 V, I_{DS} = 0.5 A		170	225	mΩ
		V_{GS} = 4.5 V, I_{DS} = 0.5 A		140	180	mΩ
$g_{ƒs}$	Transconductance	V_{DS} = 6 V, I_{DS} = 0.5 A		3.2		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 6 V, ƒ = 1 MHz		155	200	pF
C_{oss}	Output Capacitance			47	62	pF
C_{rss}	Reverse Transfer Capacitance			2.5	3.3	pF
R_G	Series Gate Resistance			23		Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 6 V, I_{DS} = 0.5 A		1060	1400	pC
Q_{gd}	Gate Charge Gate-to-Drain			140		pC
Q_{gs}	Gate Charge Gate-to-Source			230		pC
$Q_{g(th)}$	Gate Charge at V_{th}			155		pC
Q_{oss}	Output Charge	V_{DS} = 6 V, V_{GS} = 0 V		1120		pC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_{DS} = 0.5 A, R_G = 2 Ω		3.7		ns
t_r	Rise Time			1.5		ns
$t_{d(off)}$	Turn Off Delay Time			11.0		ns
$t_ƒ$	Fall Time			3.8		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 0.5 A, V_{GS} = 0 V		0.73	0.9	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 6 V, I_F = 0.5 A, di/dt = 300 A/μs		1550		pC
t_{rr}	Reverse Recovery Time			6		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{θJA}$	Junction-to-Ambient Thermal Resistance(1)	90	°C/W
	Junction-to-Ambient Thermal Resistance(2)	250	

(1) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

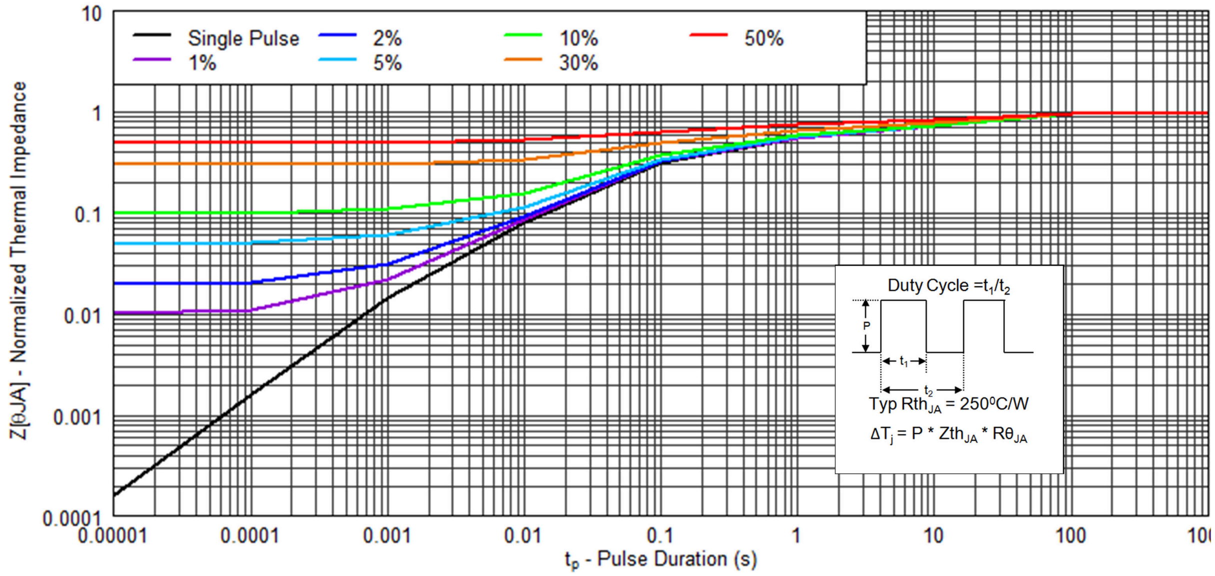

Figure 5-1. Transient Thermal Impedance

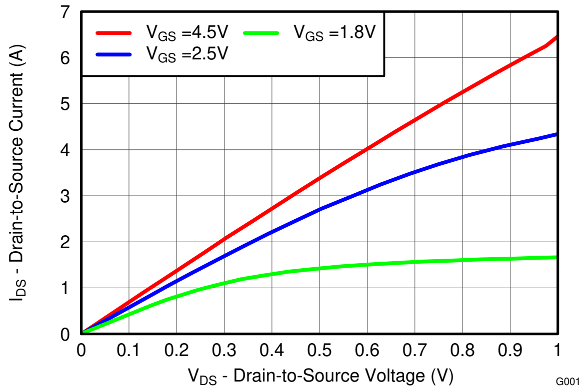

Figure 5-2. Saturation Characteristics

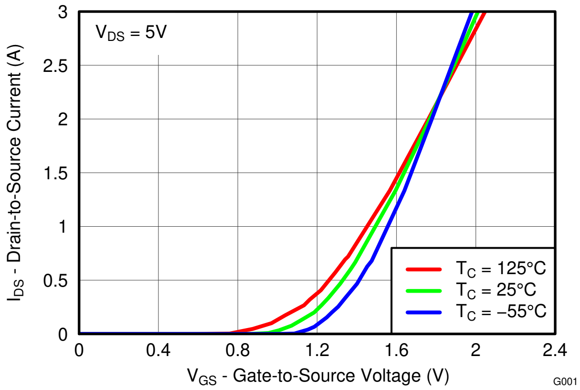

Figure 5-3. Transfer Characteristics

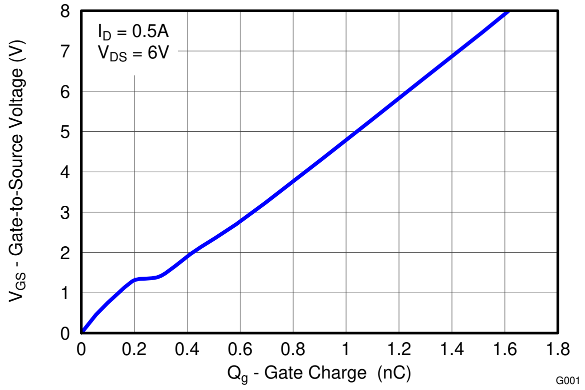

Figure 5-4. Gate Charge

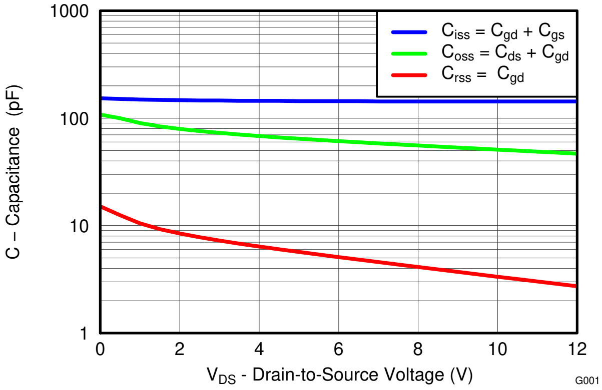

Figure 5-5. Capacitance

5.3 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

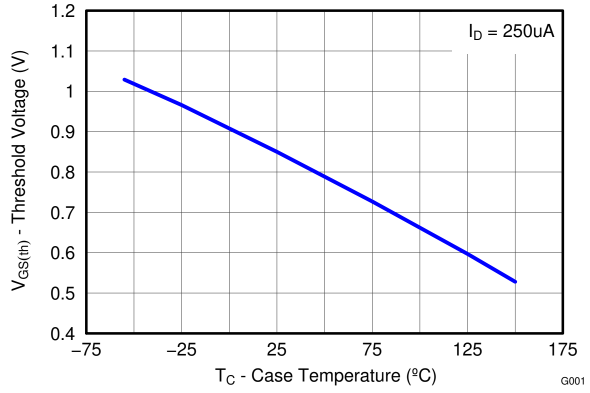

Figure 5-6. Threshold Voltage vs Temperature

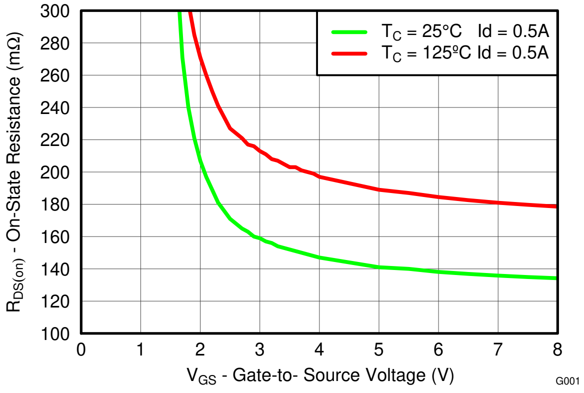

Figure 5-7. On-State Resistance vs Gate-to-Source Voltage

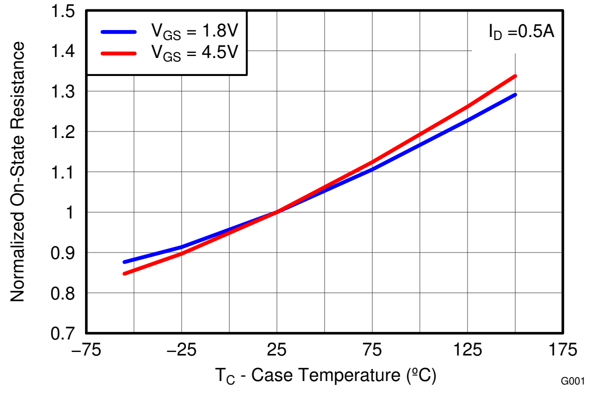

Figure 5-8. Normalized On-State Resistance vs Temperature

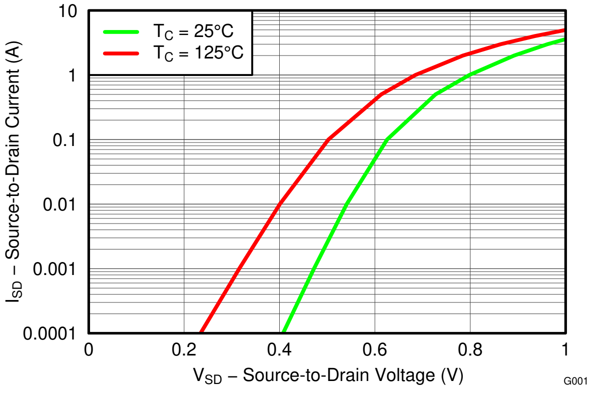

Figure 5-9. Typical Diode Forward Voltage

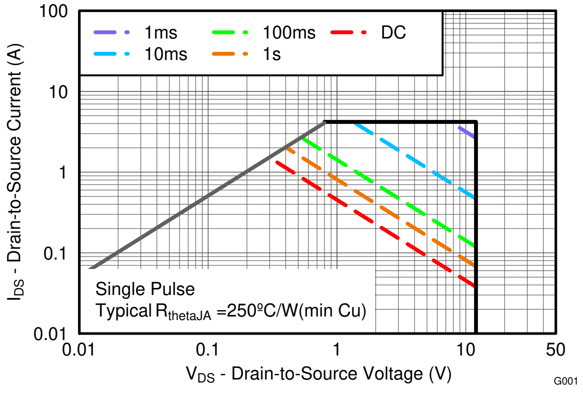

Figure 5-10. Maximum Safe Operating Area (SOA)

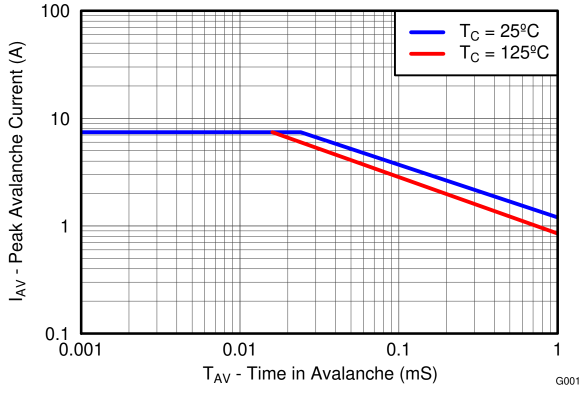

Figure 5-11. Single Pulse Unclamped Inductive Switching

5.3 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

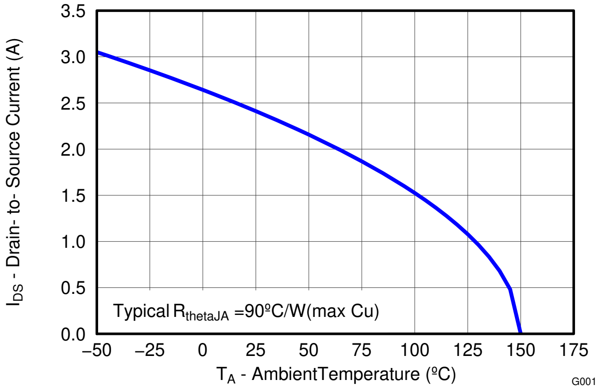

Figure 5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

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is a trademark of Texas Instruments.
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6.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

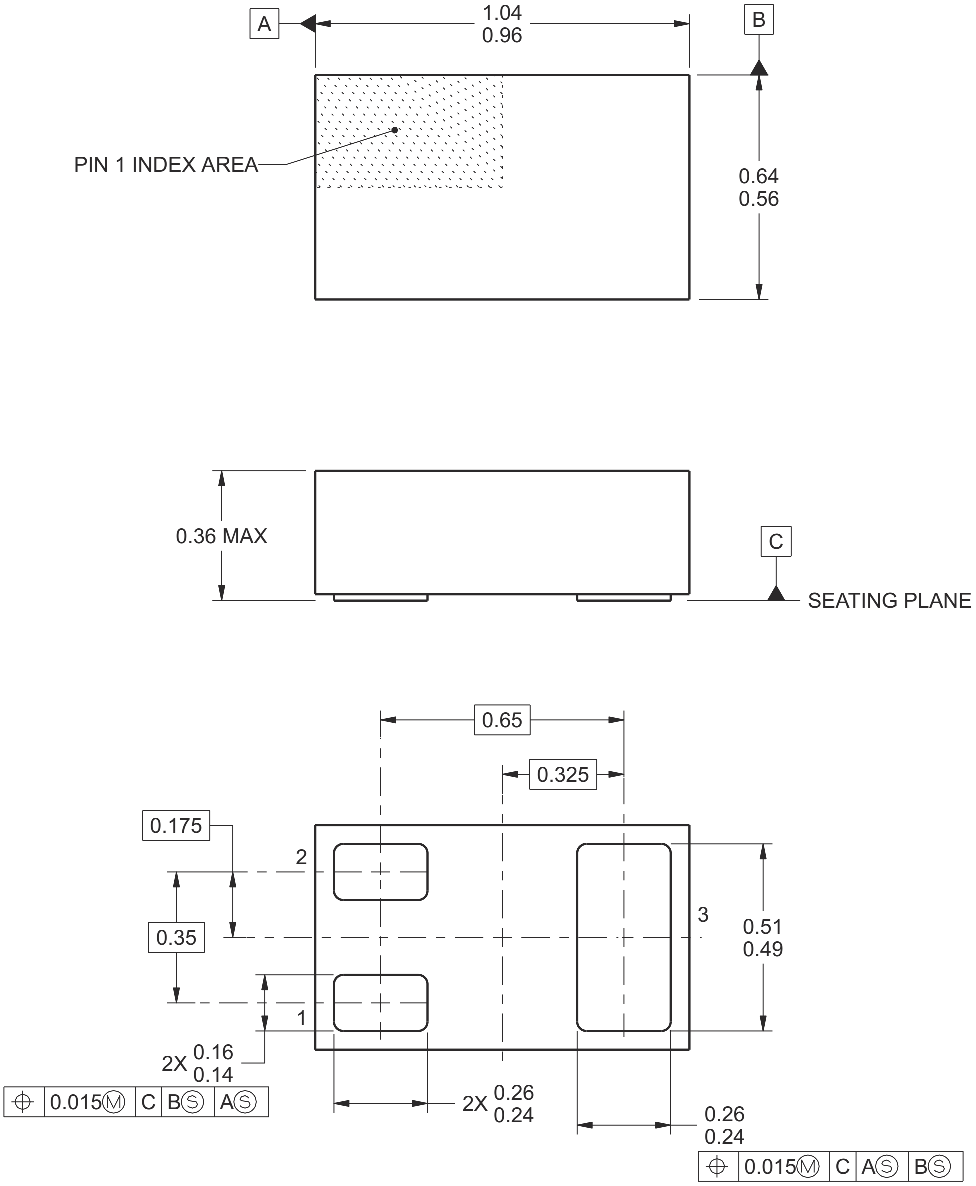
6.3 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

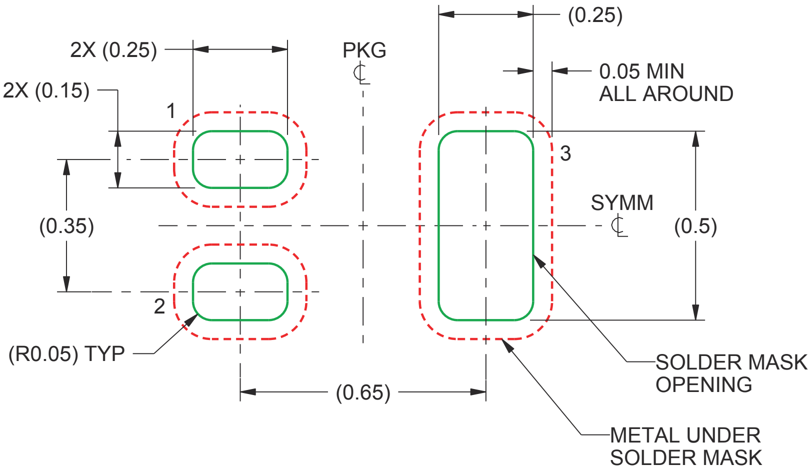


A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).

B. This drawing is subject to change without notice.

C. This package is a PB-free solder land design.

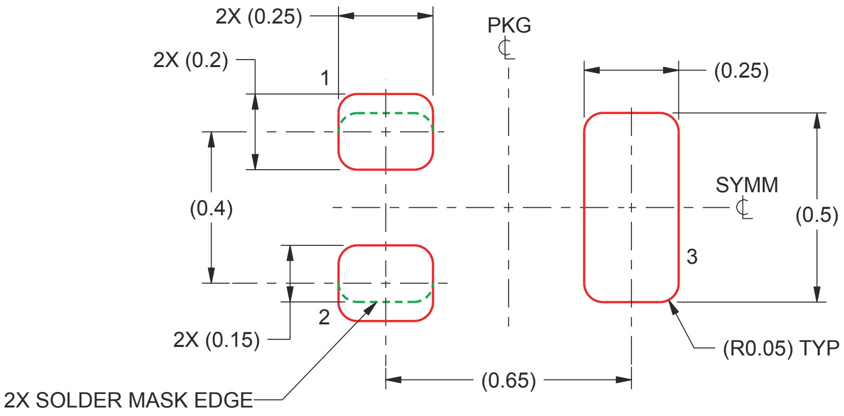
7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.

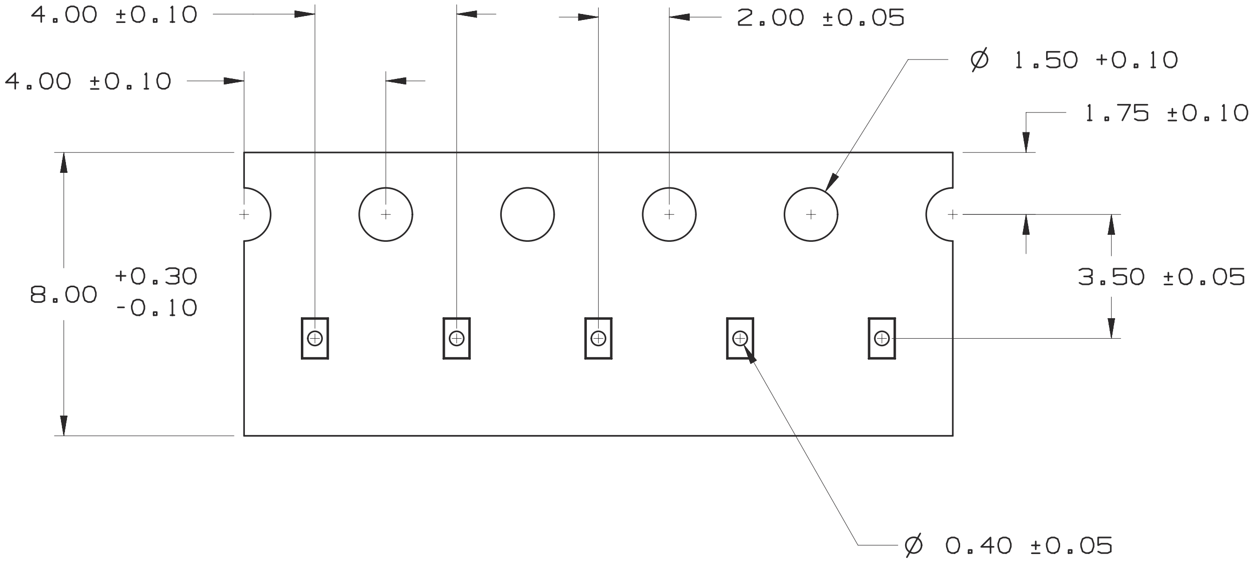
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

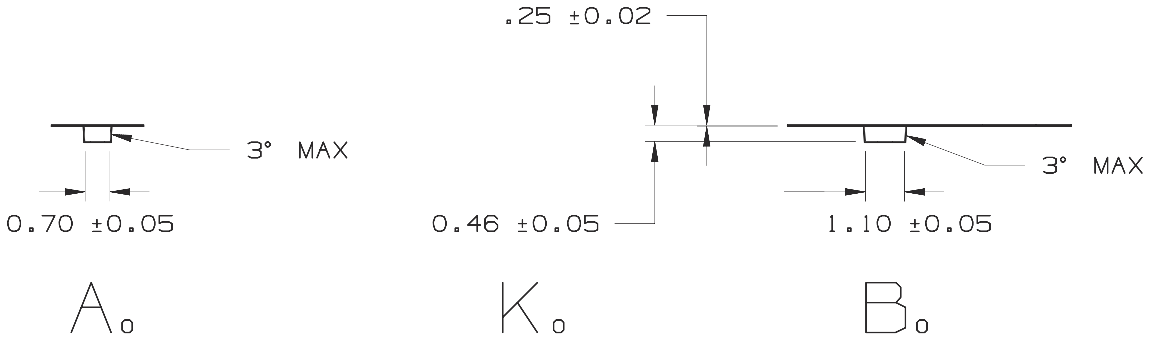
7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

7.4 CSD13381F4 Embossed Carrier Tape Dimensions





A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD13381F4	Active	Production	PICOSTAR (YJC) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DQ
CSD13381F4.B	Active	Production	PICOSTAR (YJC) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DQ
CSD13381F4T	Active	Production	PICOSTAR (YJC) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DQ
CSD13381F4T.B	Active	Production	PICOSTAR (YJC) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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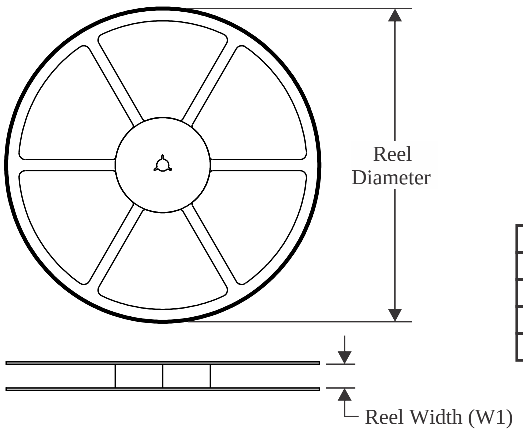
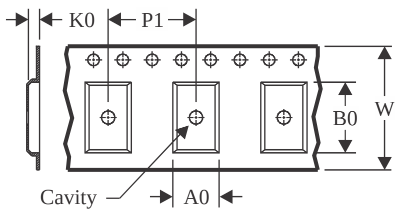
TAPE AND REEL INFORMATION

REEL DIMENSIONS

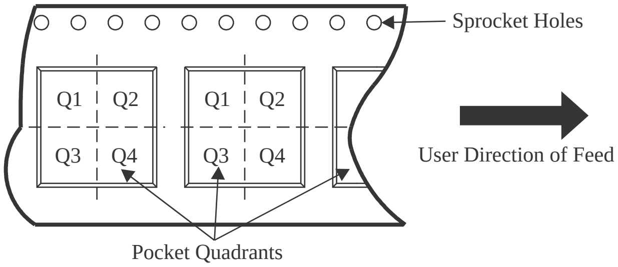


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

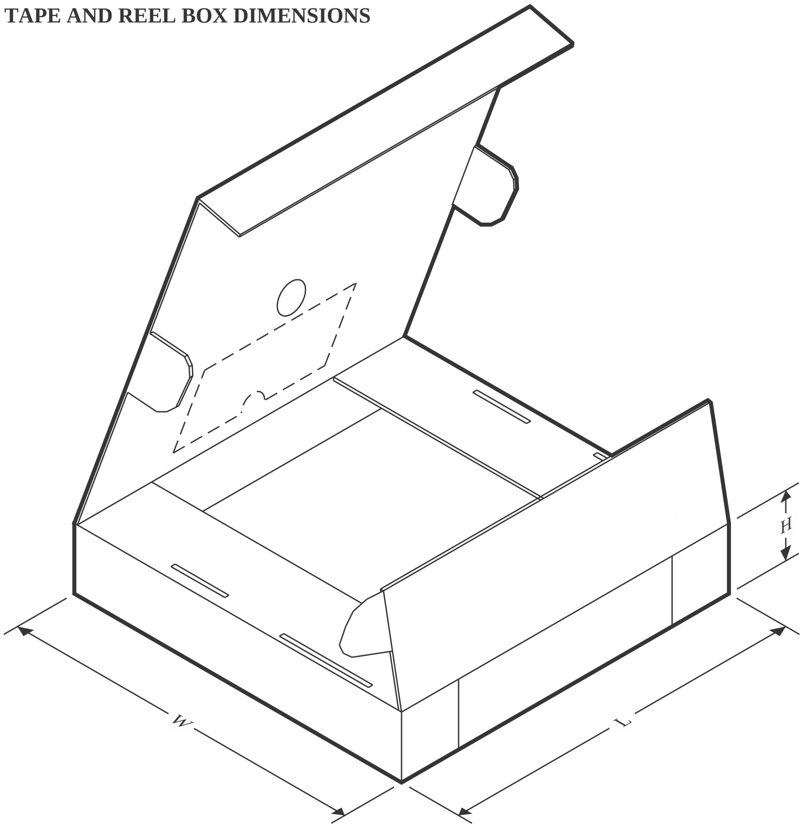
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13381F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD13381F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13381F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD13381F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

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