CDx4HC243, CDx4HCT243 High-Speed CMOS Logic Quad-Bus Transceiver with Three-State Outputs

1 Features

- Typical propagation delay (A to B, B to A) of 7ns at V_{CC} = 5 V, C_L = 15pF, T_A = 25ºC
- Three-state outputs
- Buffered inputs
- Fanout (over temperature range)
  - Standard outputs : 10 LSTTL loads
  - Bus driver outputs : 15 LSTTL loads
- Wide operating temperature range : -55ºC to 125ºC
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- HC types
  - 2 V to 6 V Operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL}= 0.8 V (Max), V_{IH} = 2 V (Min)
  - CMOS input compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

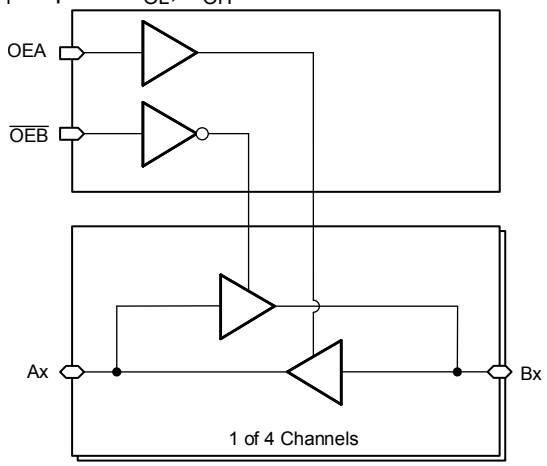
2 Description

The CDx4HC243 and CDx4HCT243 are quad bus transceivers with 3-state outputs. The OEA and $\overline{OEB}$ inputs control both the high-impedance state as well as the direction of communication through the device.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD54HC243F	CDIP (14)	19.55 mm × 6.71 mm
CD74HC243E	PDIP (14)	19.31 mm × 6.35 mm
CD74HC243M	SOIC (14)	8.65 mm × 3.90 mm
CD74HCT243E	PDIP (14)	19.31 mm × 6.35 mm
CD74HCT243M	SOIC (14)	8.65 mm × 3.90 mm

(1) For all packages see the orderable addendum at the end of the datasheet.



Functional Block Diagram

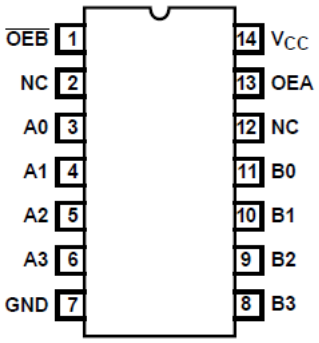
Table of Contents

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2003) to Revision E (March 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards	1

4 Pin Configuration and Functions



J, N, or D Package
14-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
I_{IK}	Input diode current	For V_I < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_{OK}	Output diode current	For V_C < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Drian Current, per output	For -0.5V < V_O < V_{CC} + 0.5V		±35	mA
I_O	Output source or sink current per output pin	For V_O > -0.5V or V_O < V_{CC} + 0.5V		±25	mA
	Continuous current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature range		-65	150	°C
T_J	Junction temperature			150	°C
	Lead temperature (Soldering 10s)(SOIC - Lead Tips Only)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input rise and fall time	V_{CC} = 2V		1000	ns
		V_{CC} = 4.5V		500	
		V_{CC} = 6V		400	
T_A	Temperature Range		-55	125	°C

5.3 Thermal Information

THERMAL METRIC		N (PDIP) 14 PINS	D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	80	86	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[1]	V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High-level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low-level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High-level output voltage CMOS loads	I_{OH} = – 20µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20µA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20µA	6	5.9			5.9		5.9		
	High-level output voltage TTL loads	I_{OH} = – 6mA	4.5	3.98			3.84		3.7		
		I_{OH} = – 7.8mA	6	5.48			5.34		5.2		
V_{OL}	Low-level output voltage CMOS loads	I_{OL} = 20µA	2			0.1		0.1		0.1	V
		I_{OL} = 20µA	4.5			0.1		0.1		0.1	
		I_{OL} = 20µA	6			0.1		0.1		0.1	
	Low-level output voltage TTL	I_{OL} = 6mA	4.5			0.26		0.33		0.4	
		I_{OL} = 7.8mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_{CC} or GND	6			±0.1		±1		±1	µA
I_{CC}	Supply Current	V_{CC} or GND	6			8		80		160	µA
I_{OZ}	Three-state leakage current	V_{IL} or V_{IH}	6			±0.5		±0.5		±10	µA
HCT TYPES											
V_{IH}	High-level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low-level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High-level output voltage CMOS loads	I_{OH} = – 20µA	4.5	4.4			4.4		4.4		V
	High-level output voltage TTL loads	I_{OH} = – 6mA	4.5	3.98			3.84		3.7		
V_{OL}	Low-level output voltage CMOS loads	I_{OL} = 20µA	4.5			0.1		0.1		0.1	V
	Low-level output voltage TTL loads	I_{OL} = 6mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_{CC} to GND	5.5			±0.1		±1		±1	µA
I_{CC}	Supply current	V_{CC} or GND	5.5			8		80		160	µA
ΔI_{CC} [2] [3]	Additional supply current per input pin	One of An or Bn	4.5 to 5.5		100	396		495		539	µA
		One of OEA or $\overline{OEB}$	4.5 to 5.5		100	216		270		294	
I_{OZ}	Three-state leakage current	V_{IL} or V_{IH}	5.5			±0.5		±5		±10	µA

(1) $V_I = V_{IH}$ or V_{IL}, unless otherwise noted.
(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(3) Inputs held at V_{CC} – 2.1.

5.5 Switching Characteristics

Input t_t = 6ns. Unless otherwise specified, C_L = 50pF

PARAMETER		V_{CC} (V)	25°C		-40°C to 85°C	-55°C to 125°C	UNIT
			TYP	MAX	MAX	MAX	
HC TYPES							
t_{pd}	Propagation delay data to outputs	2		90	115	135	ns
		4.5	7[1]	18	23	27	
		6		15	20	23	
t_{PZL}, t_{PZH}	Output high-Z, to high level to low level	2		150	190	225	ns
		4.5	12[1]	30	38	45	
		6		26	33	38	
t_{PHZ}, t_{PLZ}	Output high level, output low level to high-Z	2		150	190	225	ns
		4.5	12[1]	30	38	45	
		6		26	33	38	
t_t	Output transition times	2		60	75	90	ns
		4.5		12	15	18	
		6		10	13	15	
C_i	Input capacitance			10	10	10	pF
C_O	Three-state output capacitance			20	20	20	pF
C_{pd} [2] [3]	Power dissipation capacitance	5	80				pF
HCT TYPES							
t_{pd}	Propagation delay data to outputs	4.5	9[1]	22	28	33	ns
t_{PZH}, t_{PLZ}	Output high-Z to high level to low level	4.5	14[1]	34	43	51	ns
t_{PHZ}, t_{PLZ}	Output high level, output low level to high-Z	4.5	14[1]	35	44	53	ns
t_t	Output transition times	4.5		12	15	18	ns
C_i	Input capacitance			10	10	10	pF
C_O	Three-state output capacitance			20	20	20	pF
C_{pd} [2] [3]	Power dissipation capacitance	5	91				pF

(1) Typical value tested at 5V, C_L = 15pF.
(2) C_{PD} is used to determine the dynamic power consumption, per channel.
(3) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

6 Parameter Measurement Information

t_{PD} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

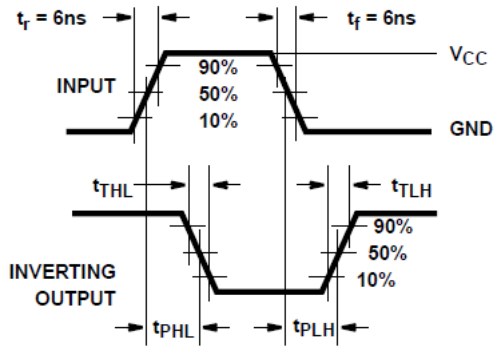


Figure 6-1. HC and HCT transition times and propagation delay times, combination logic

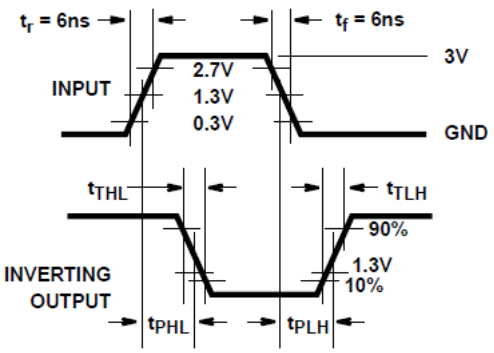


Figure 6-2. HCT transition times and tpopationg delay times, combination logic

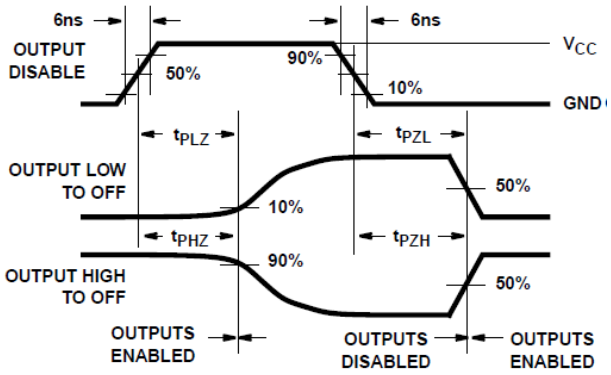


Figure 6-3. HC three-state propagation delay waveform

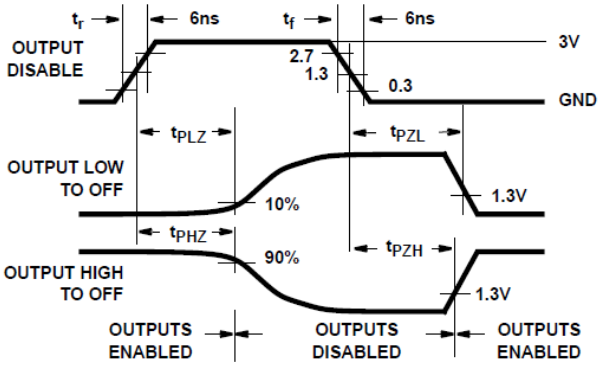
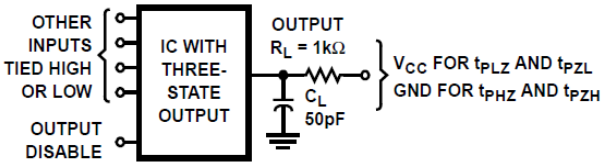


Figure 6-4. HCT three-state propagation delay waveform



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

Figure 6-5. HC and HCT three-state propagation delay test circuit

7 Detailed Description

7.1 Overview

The CDx4HC243 and CDx4HCT243 silicon-gate CMOS three-state bidirectional noninverting buffers are intended for two-way asynchronous communication between data buses. They have high-drive-current outputs that enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits and have speeds comparable to low-power Schottky TTL circuits. They can drive 15 LSTTL loads.

The states of the output-enable ($\overline{OEB}$, OEA) inputs determine both the direction of flow (A to B, B to A), and the three-state mode.

7.2 Functional Block Diagram

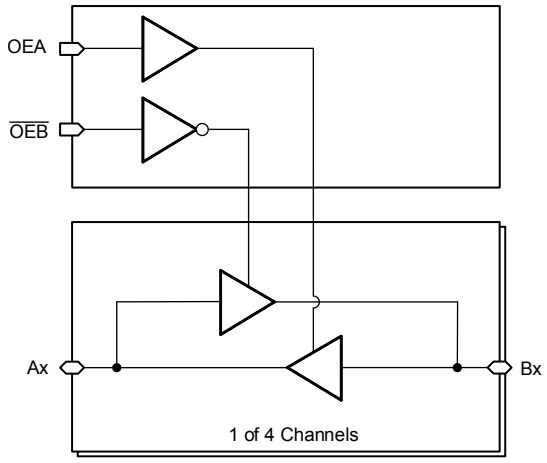


Figure 7-1. Functional Diagram

7.3 Device Functional Modes

Table 7-1. Truth Table[1][2]

Control Inputs		HC, HCT243 Series	
		Data port status	
$\overline{OEB}$	OEA	An	Bn
H	H	O	I
L	H	Z	Z
H	L	Z	Z
L	L	I	O

(1) H = High voltage level. L = Low voltage level. I = Input. O = Output (Same level as input). Z = High Impedance

(2) To prevent excess currents in the High Z modes all I/O terminals hsould be terminated with 10kΩ to 1MΩ resistors.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
8409001CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A
CD54HC243F	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC243F
CD54HC243F.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC243F
CD54HC243F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A
CD54HC243F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A
CD74HC243E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC243E
CD74HC243E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC243E
CD74HC243EE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC243E
CD74HC243M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC243M
CD74HC243M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HC243M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HC243M96.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HC243M96G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HC243M96G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HCT243E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT243E
CD74HCT243E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT243E
CD74HCT243M	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT243M
CD74HCT243M.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT243M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54HC243, CD74HC243 :

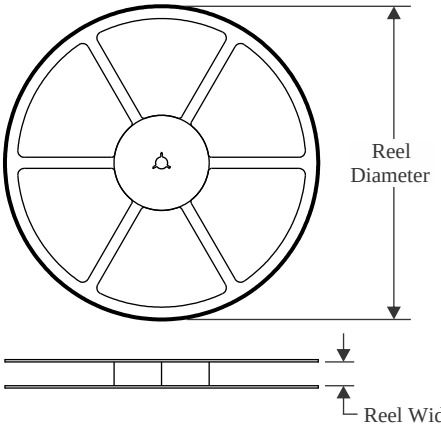
- Catalog : CD74HC243
- Military : CD54HC243

NOTE: Qualified Version Definitions:

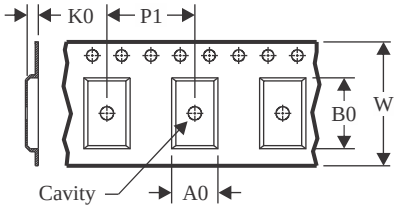
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

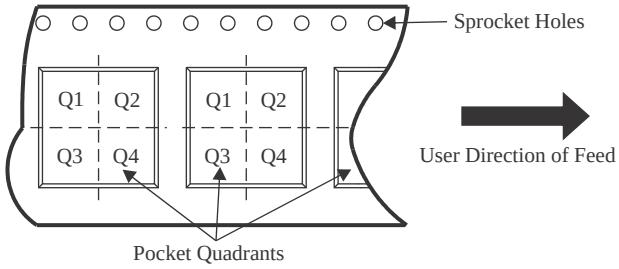


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

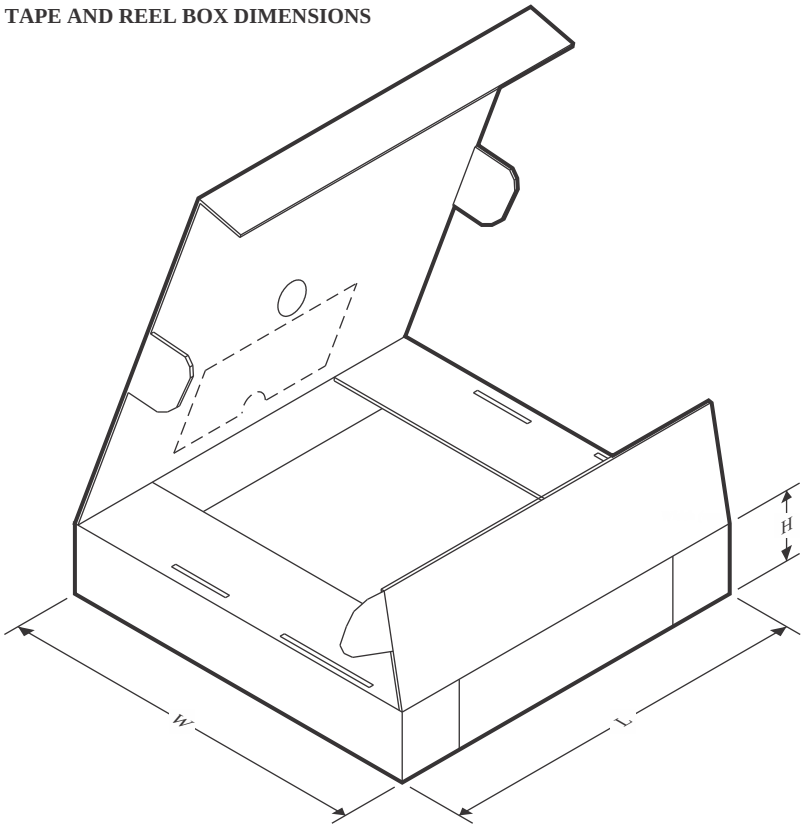
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC243M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC243M96	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HC243M96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

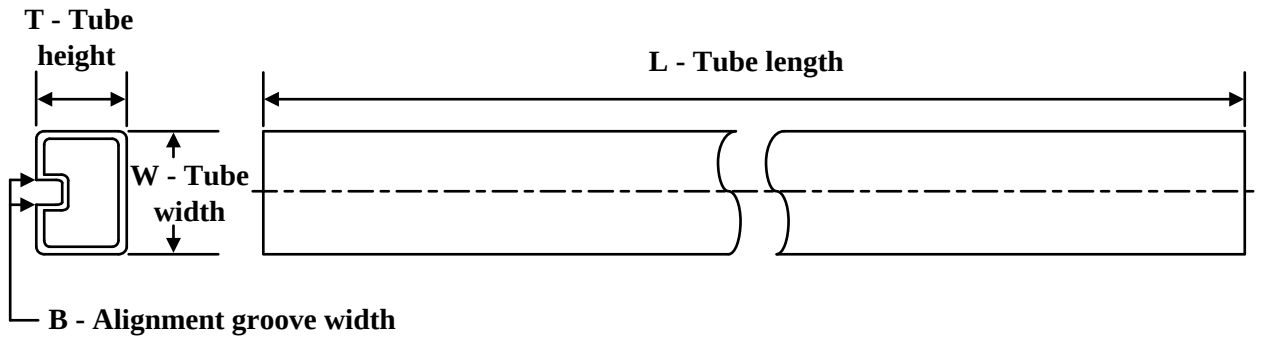
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

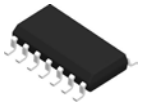
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC243M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74HC243M96	SOIC	D	14	2500	366.0	364.0	50.0
CD74HC243M96G4	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243M	D	SOIC	14	50	506.6	8	3940	4.32
CD74HCT243M.A	D	SOIC	14	50	506.6	8	3940	4.32

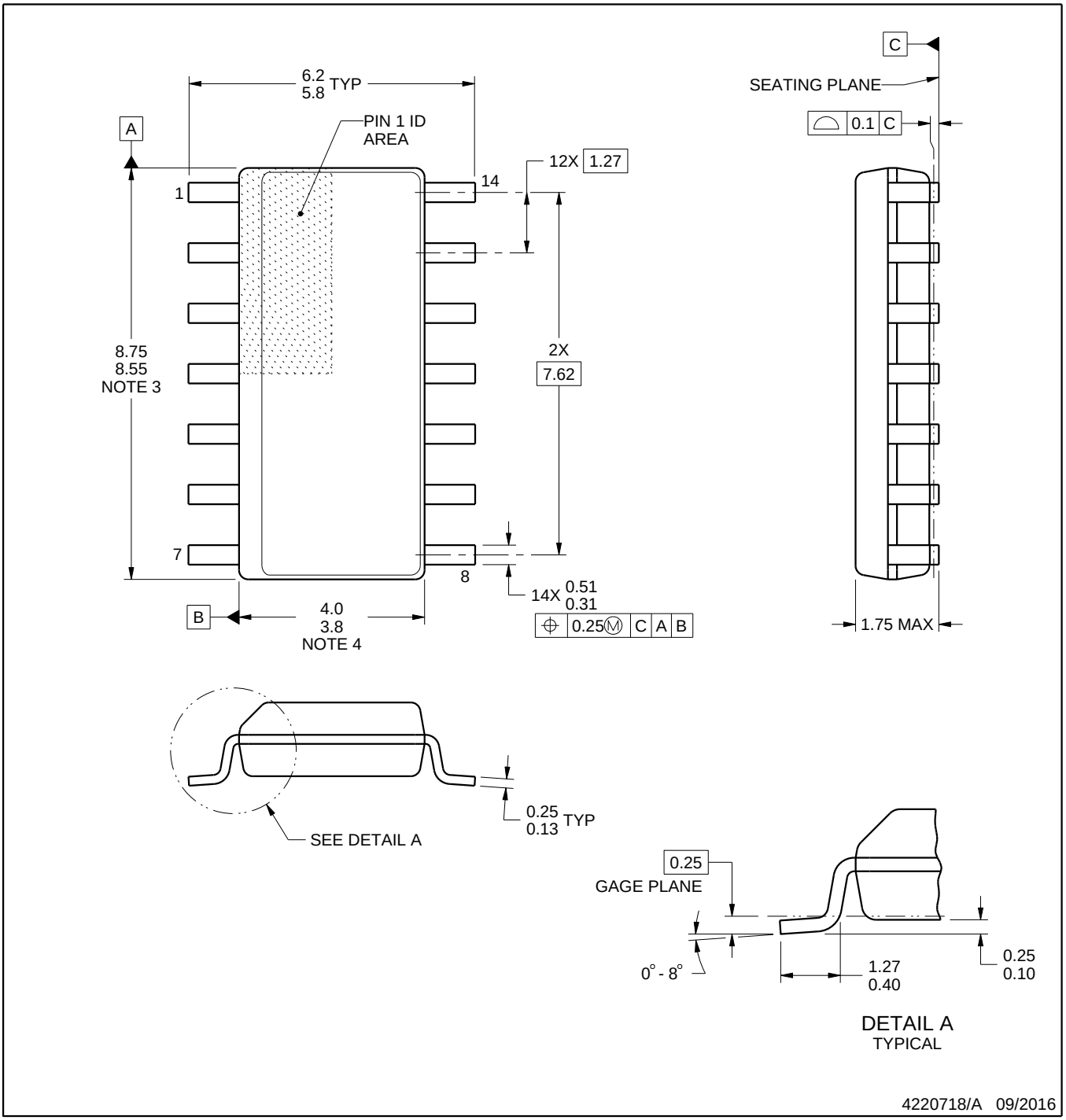


PACKAGE OUTLINE

D0014A

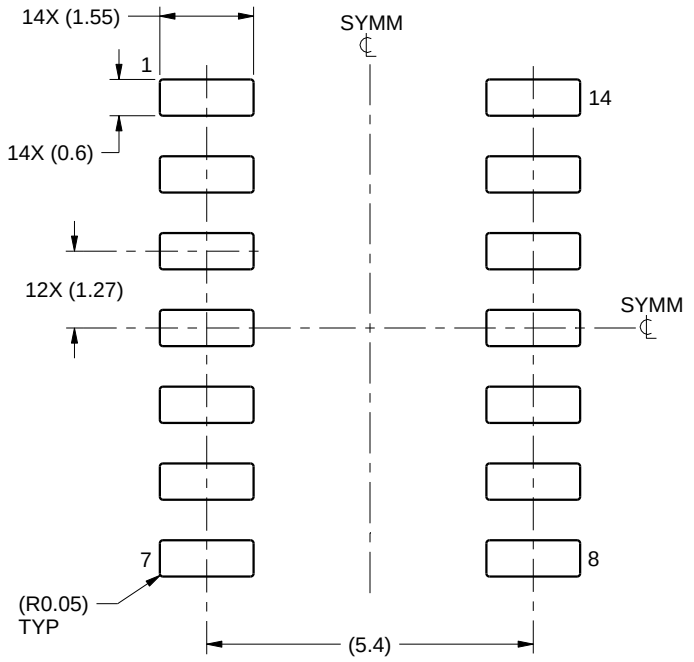
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

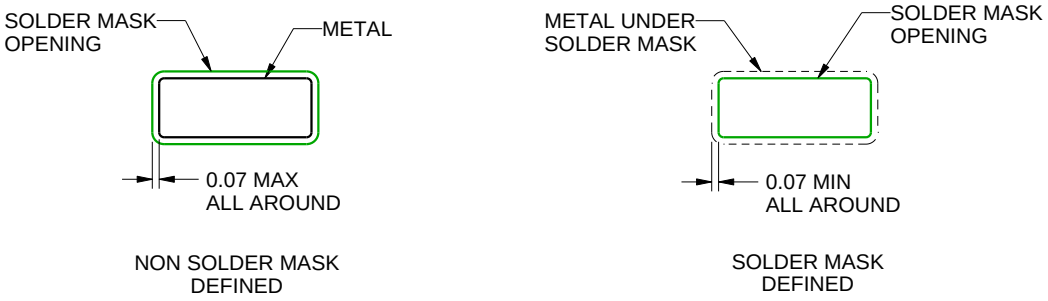


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

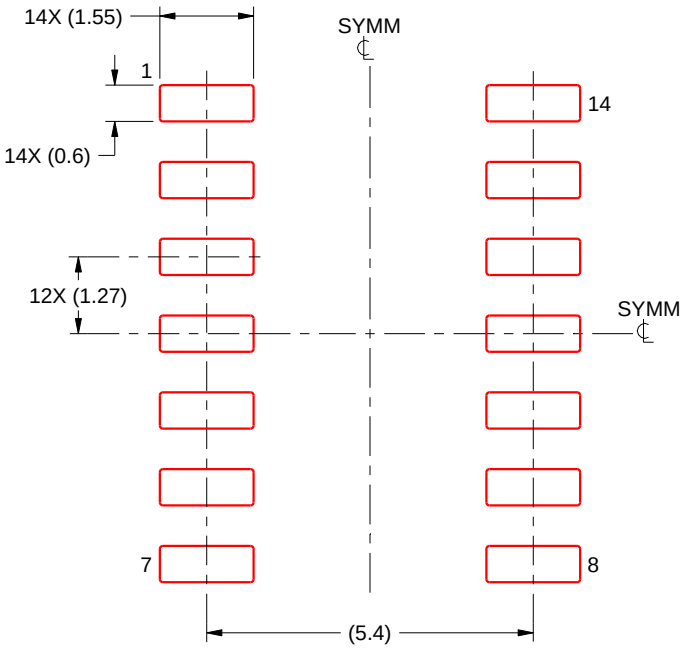
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

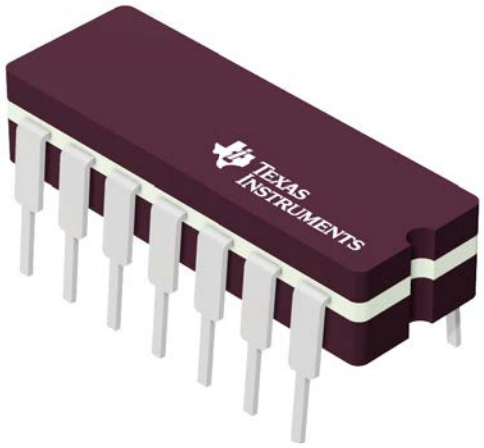
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

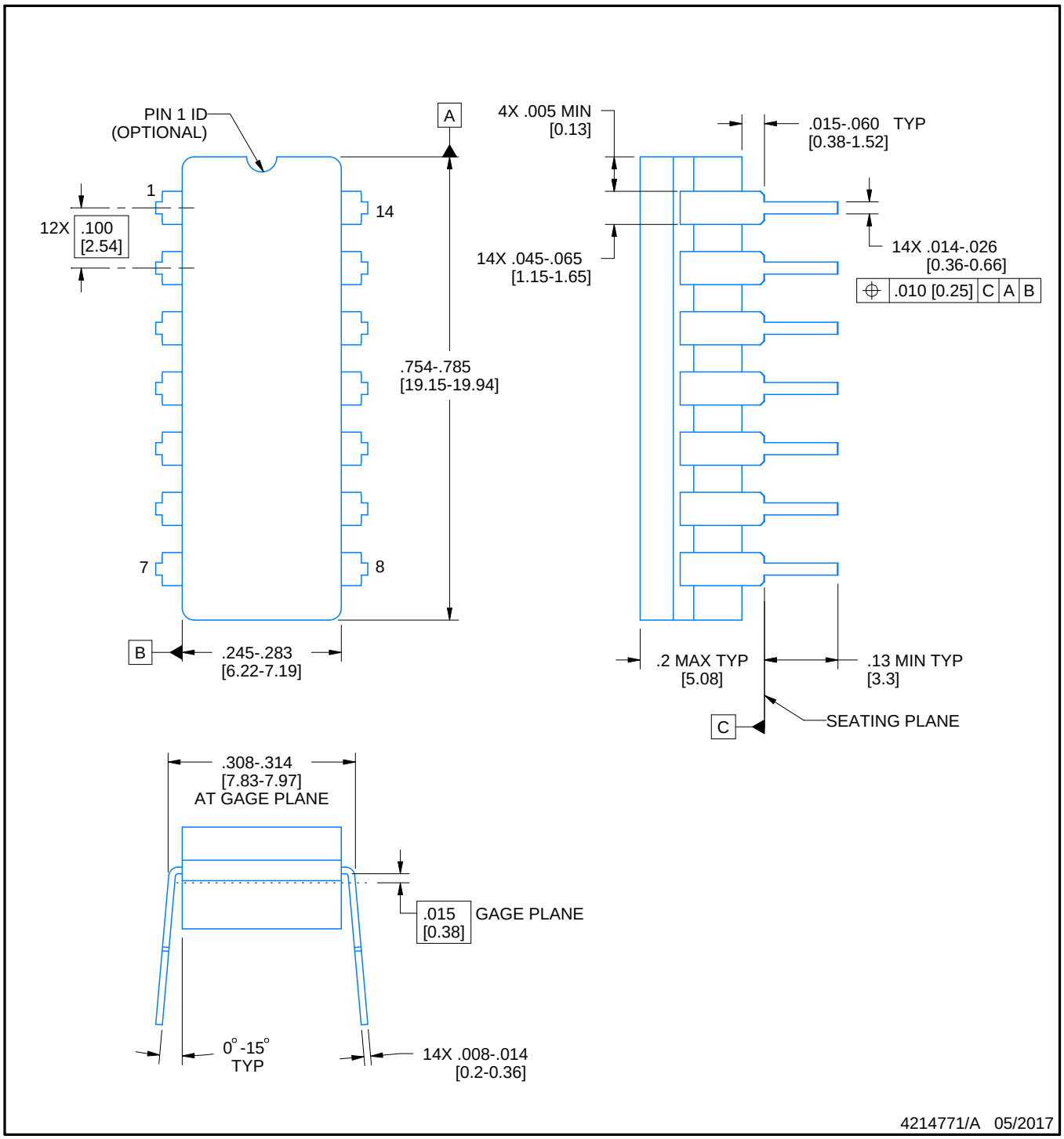
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

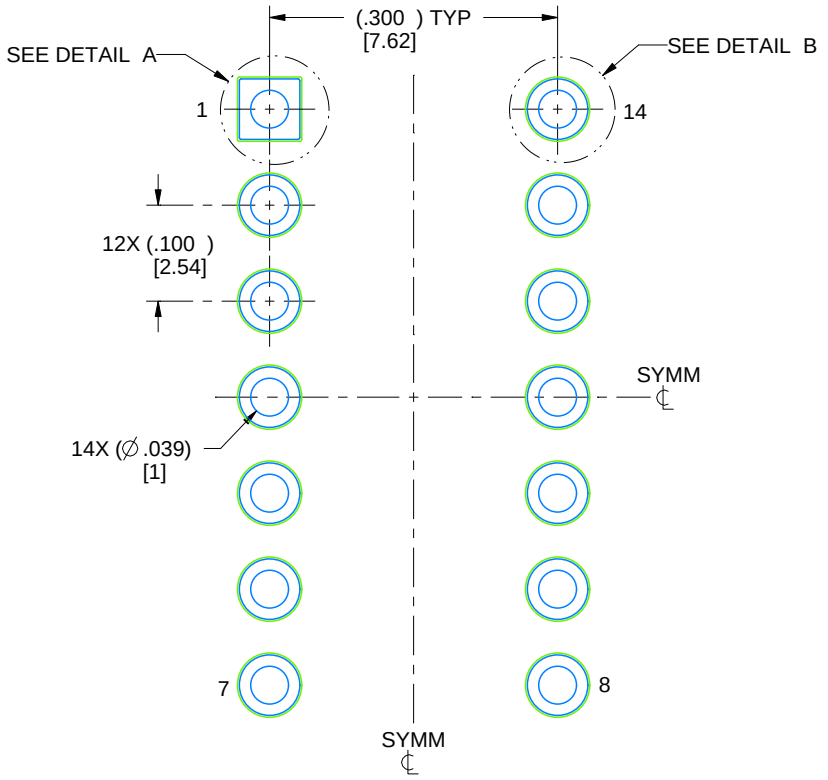
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

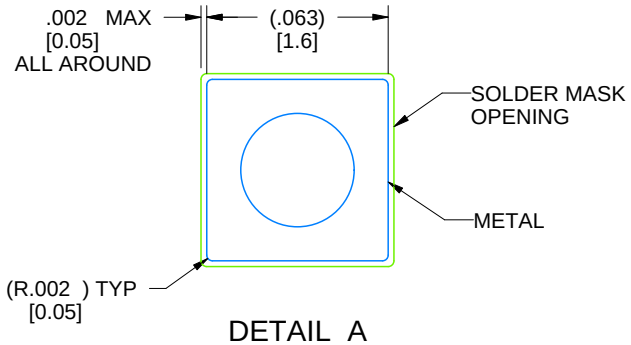
J0014A

CDIP - 5.08 mm max height

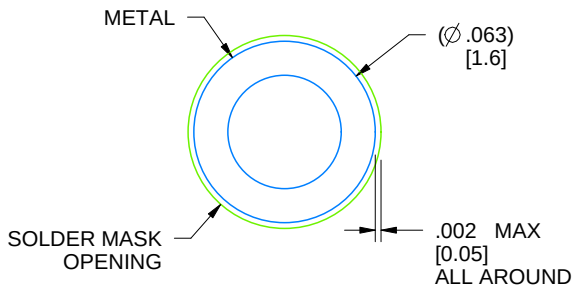
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



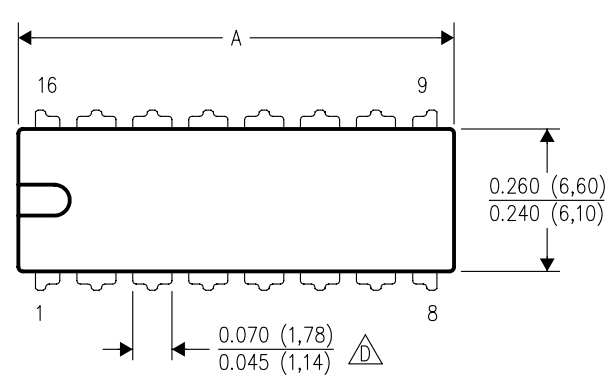
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

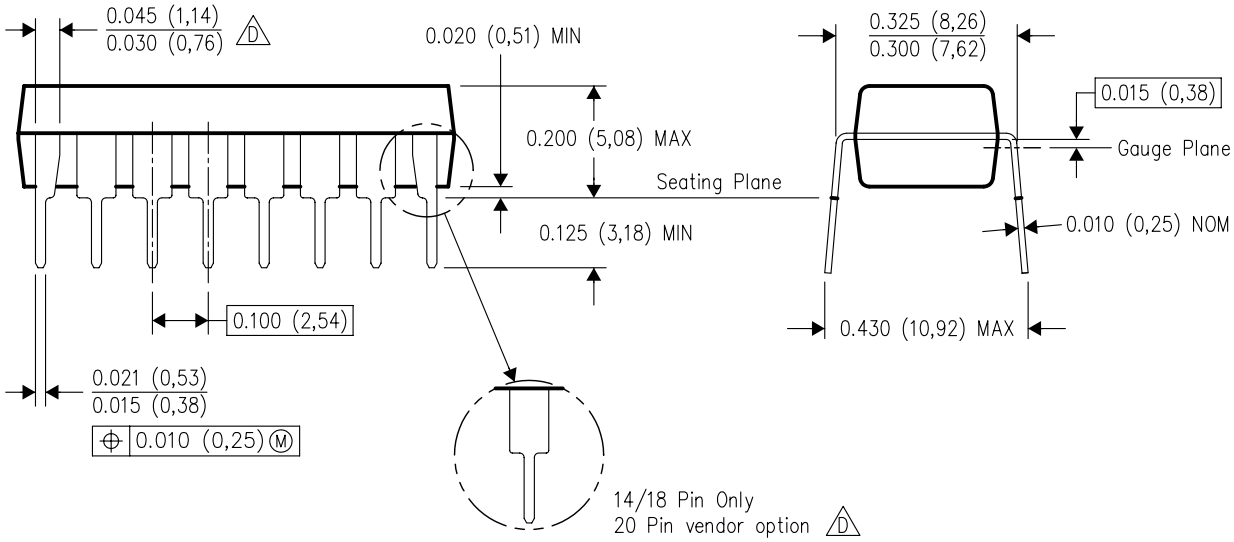
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265