

## CDx4HCT10 Triple 3-Input NAND Gates

### 1 Features

- LSTTL input logic compatible
  - $V_{IL(max)} = 0.8\text{ V}$ ,  $V_{IH(min)} = 2\text{ V}$
- CMOS input logic compatible
  - $I_I \leq 1\text{ }\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$
- Buffered inputs
- 4.5 V to 5.5 V operation
- Wide operating temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Supports fanout up to 10 LSTTL loads
- Significant power reduction compared to LSTTL logic ICs

### 2 Applications

- [Alarm / tamper detect circuit](#)
- S-R latch

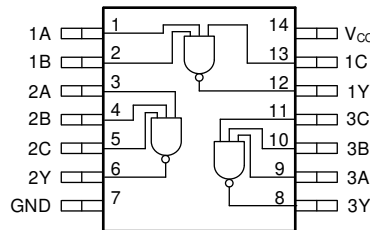
### 3 Description

This device contains three independent 3-input NAND gates. Each gate performs the Boolean function  $Y = \overline{A \bullet B \bullet C}$  in positive logic.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD74HCT10M	SOIC (14)	8.70 mm × 3.90 mm
CD74HCT10E	PDIP (14)	19.30 mm × 6.40 mm
CD54HCT10F	CDIP (14)	21.30 mm × 7.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional pinout



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## 4 Revision History

DATE	REVISION	NOTES
June 2020	*	Initial release. Moved the HCT devices from the SCHS128 to a standalone data sheet.

## 5 Pin Configuration and Functions

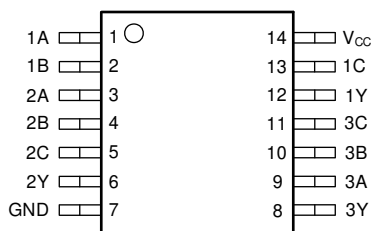


Figure 5-1. D, N, or J Package 14-Pin SOIC, PDIP, or CDIP Top View

## Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
2A	3	Input	Channel 2, Input A
2B	4	Input	Channel 2, Input B
2C	5	Input	Channel 2, Input C
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
3C	11	Input	Channel 3, Input C
1Y	12	Output	Channel 1, Output Y
1C	13	Input	Channel 1, Input C
V <sub>CC</sub>	14	—	Positive Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		–0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < –0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < –0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> > –0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±25	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>J</sub>	Junction temperature <sup>(3)</sup>			150	°C
	Maximum Lead Temperature (Soldering 10s)	SOIC - Lead Tips Only		300	°C
T <sub>stg</sub>	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

### 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5		5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2			V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V			0.8	V
V <sub>I</sub>	Input voltage		0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0		V <sub>CC</sub>	V
t <sub>t</sub>	Input transition time	V <sub>CC</sub> = 4.5 V			500	ns
		V <sub>CC</sub> = 5.5 V			400	
T <sub>A</sub>	Operating free-air temperature		–55		125	°C

### 6.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CD74HCT10		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	61.9	94.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	49.7	48.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	41.7	50.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	29.3	11.9	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	41.4	50.2	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.4 Electrical Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT
					25°C			–40°C to 85°C			–55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = –20 μA	4.5 V	4.4			4.4			4.4		V	
			I <sub>OH</sub> = –4 mA	4.5 V	3.98			3.84			3.7			
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	4.5 V				0.1			0.1		V	
			I <sub>OL</sub> = 4 mA	4.5 V				0.26			0.33			0.4
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> and GND	I <sub>O</sub> = 0	5.5 V				±0.1			±1		μA	
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	5.5 V				2			20		40 μA	
ΔI <sub>CC</sub> (1)	Additional Quiescent Device Current Per Input Pin	V <sub>I</sub> = V <sub>CC</sub> – 2.1		4.5 V to 5.5 V			100		360		450		490 μA	
C <sub>i</sub>	Input capacitance						10					10	pF	

(1) For dual-supply systems theoretical worst case ( $V_I = 2.4\ \text{V}$ ,  $V_{CC} = 5.5\ \text{V}$ ) specification is 1.8 mA.

## 6.5 Switching Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		FROM	TO	TEST CONDITIO NS	V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT
						25°C			−40°C to 85°C			−55°C to 125°C			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>pd</sub>	Propagation delay	A, B or C	Y	C <sub>L</sub> = 50 pF	4.5 V	24			30			36			ns
		A, B or C	Y	C <sub>L</sub> = 15 pF	5 V	9									
t <sub>t</sub>	Transition-time		Y	C <sub>L</sub> = 50 pF	4.5 V	15			19			22			ns

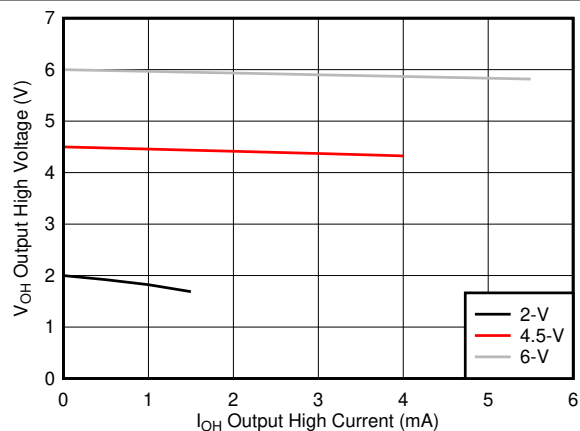
## 6.6 Operating Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

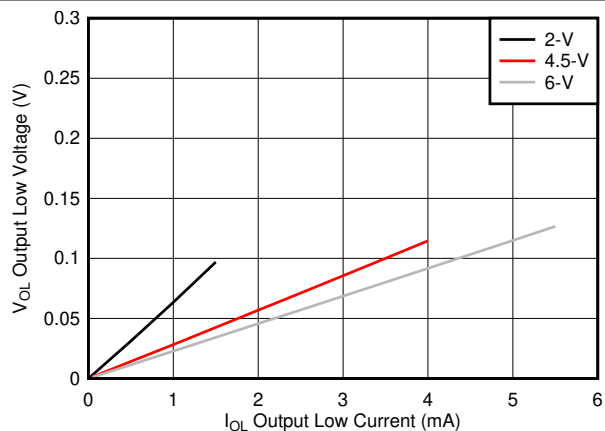
PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$C_{pd}$	Power dissipation capacitance per gate	No load	4.5 V to 5.5 V		28		pF

## 6.7 Typical Characteristics

$T_A = 25^\circ\text{C}$



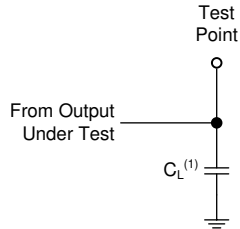
**Figure 6-1. Typical output voltage in the high state ( $V_{OH}$ )**



**Figure 6-2. Typical output voltage in the low state ( $V_{OL}$ )**

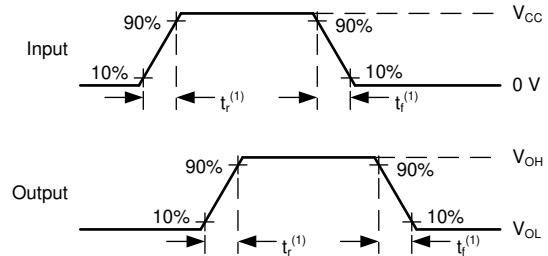
## 7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .
- The outputs are measured one at a time, with one input transition per measurement.



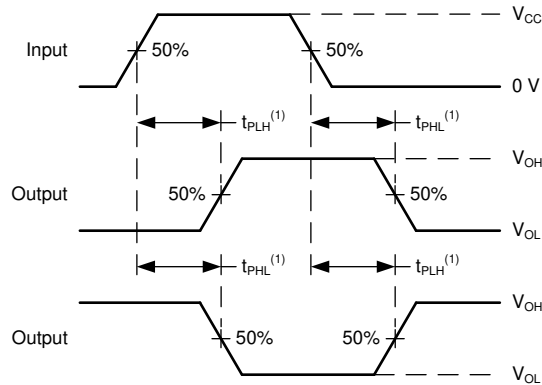
A.  $C_L = 50 \text{ pF}$  and includes probe and jig capacitance.

**Figure 7-1. Load Circuit**



A.  $t_t$  is the greater of  $t_r$  and  $t_f$ .

**Figure 7-2. Voltage Waveforms Transition Times**



A. The maximum between  $t_{PLH}$  and  $t_{PHL}$  is used for  $t_{pd}$ .

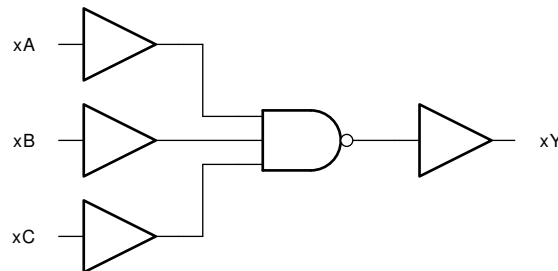
**Figure 7-3. Voltage Waveforms Propagation Delays**

## 8 Detailed Description

### 8.1 Overview

This device contains three independent 3-input NAND gates. Each gate performs the Boolean function  $Y = A \bullet B \bullet C$  in positive logic.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [Section 6.1](#) must be followed at all times.

The CD74HCT10 can drive a load with a total capacitance less than or equal to the maximum load listed in the [Section 6.5](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [Section 6.1](#).

#### 8.3.2 TTL-Compatible CMOS Inputs

TTL-Compatible CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [Section 6.4](#). The worst case resistance is calculated with the maximum input voltage, given in the [Section 6.1](#), and the maximum input leakage current, given in the [Section 6.4](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t/\Delta v$  in the [Section 6.2](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the TTL-compatible CMOS input.

TTL-Compatible CMOS inputs have a lower threshold voltage than standard CMOS inputs to allow for compatibility with older bipolar logic devices. See the [Section 6.2](#) for the valid input voltages for the CD74HCT10.

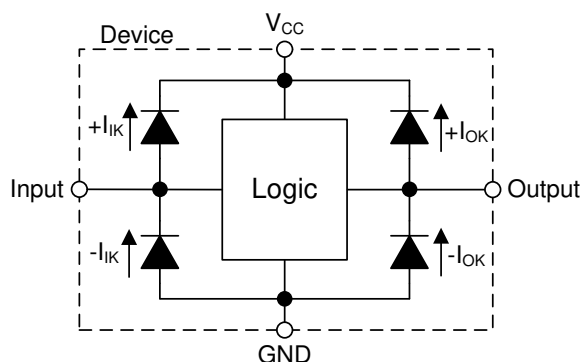


### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Figure 8-1](#).

#### CAUTION

Voltages beyond the values specified in the [Section 6.1](#) table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

**Table 8-1. Function Table**

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

In this application, two 3-input NAND gates are used to create an active-low SR latch as shown in [Figure 9-1](#). The additional gate can be used for another application, or the inputs can be grounded and the channel left unused.

This device is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the R input which returns the Q output back to LOW.

### 9.2 Typical Application

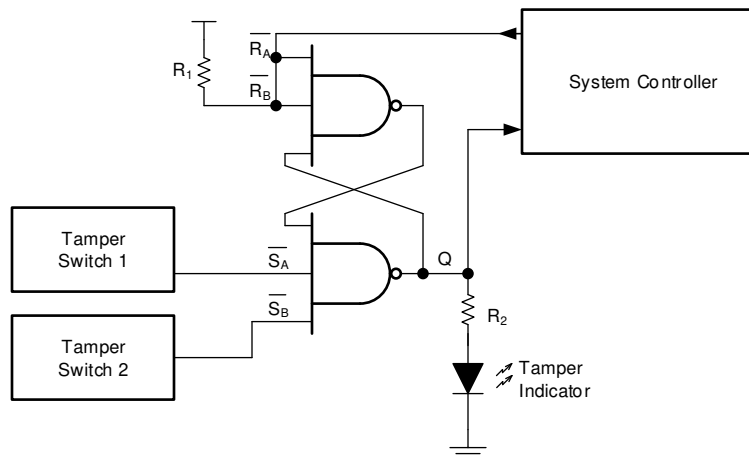


Figure 9-1. Typical application schematic

#### 9.2.1 Design Requirements

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Section 6.2](#). The supply voltage sets the device's electrical characteristics as described in the [Section 6.4](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HCT10 plus the maximum supply current,  $I_{CC}$ , listed in the [Section 6.4](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or  $V_{CC}$  listed in the [Section 6.1](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and  \$C\_{pd}\$  Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

### CAUTION

The maximum junction temperature,  $T_J(\text{max})$  listed in the [Section 6.1](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Section 6.1](#). These limits are provided to prevent damage to the device.

#### 9.2.1.2 Input Considerations

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HCT10, as specified in the [Section 6.4](#), and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

Refer to the [Section 8.3](#) for additional information regarding the inputs for this device.

#### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the [Section 6.4](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the [Section 6.4](#).

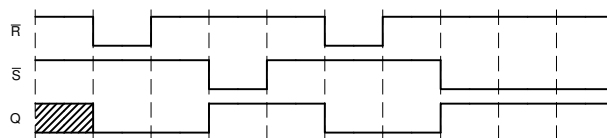
Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to [Section 8.3](#) for additional information regarding the outputs for this device.

#### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the [Section 11](#).
2. Ensure the capacitive load at the output is  $\leq 70$  pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HCT10 to the receiving device.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(\text{max})}) \Omega$ . This will ensure that the maximum output current from the [Section 6.1](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

#### 9.2.3 Application Curves



**Figure 9-2. Typical application timing diagram**

## 10 Power Supply Recommendations

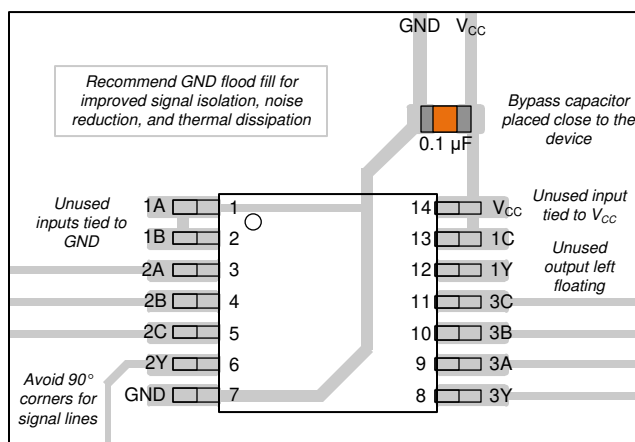
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 6.2](#). Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [Figure 11-1](#).

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example



**Figure 11-1. Example layout for the CD74HCT10**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

### 12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-8984301CA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8984301CA CD54HCT10F3A
<a href="#">CD54HCT10F3A</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8984301CA CD54HCT10F3A
CD54HCT10F3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8984301CA CD54HCT10F3A
<a href="#">CD74HCT10E</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT10E
CD74HCT10E.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT10E
<a href="#">CD74HCT10M</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	HCT10M
<a href="#">CD74HCT10M96</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT10M
CD74HCT10M96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT10M
CD74HCT10M96G4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT10M
<a href="#">CD74HCT10MT</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	HCT10M

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CD54HCT10, CD74HCT10 :**

- Catalog : [CD74HCT10](#)
- Military : [CD54HCT10](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT10M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT10M96	SOIC	D	14	2500	356.0	356.0	35.0

## TUBE

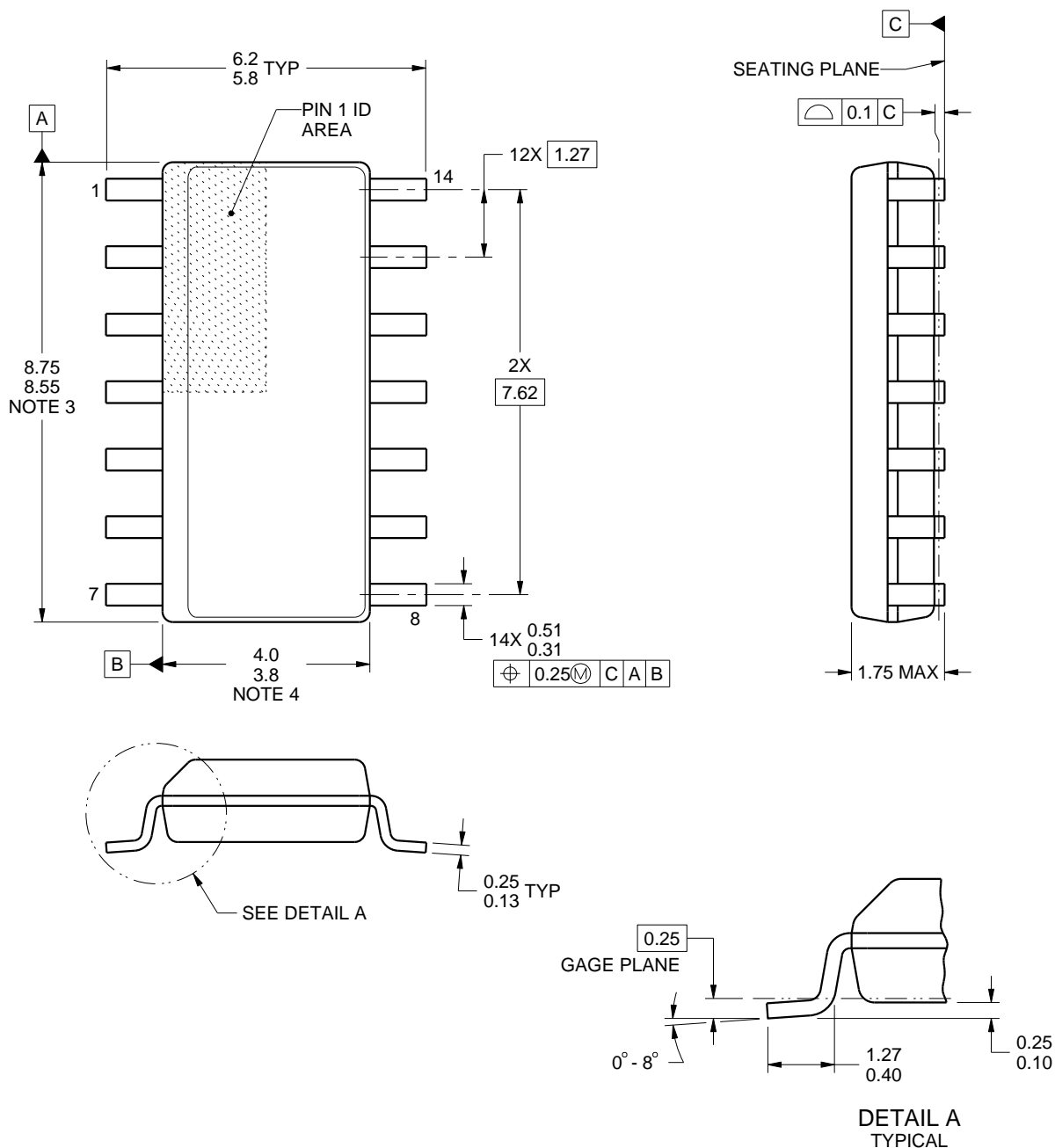


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HCT10E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT10E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT10E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT10E.A	N	PDIP	14	25	506	13.97	11230	4.32

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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