CD74HC4016

Data sheet acquired from Harris Semiconductor
SCHS199C

February 1998 - Revised August 2004

High-Speed CMOS Logic Quad Bilateral Switch

Features

- **Wide Analog-Input-Voltage Range . . . . . 0V to 10V**
- **Low "ON" Resistance**
  - **45Ω (Typ) . . . . . V_{CC} = 4.5V**
  - **35Ω (Typ) . . . . . V_{CC} = 6V**
  - **30Ω (Typ) . . . . . 1fcV_{CC} = 9V**
- **Fast Switching and Propagation Delay Times**
- **Low "OFF" Leakage Current**
- **Built-In "Break-Before-Make" Switching**
- **Suitable for Sample and Hold Applications**
- **Wide Operating Temperature Range . . . -55^{O}C to 125^{O}C**
- **HC Types**
  - **2V to 10V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

Description

The CD74HC4016 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

Each switch has two input/output terminals (nY, nZ) and an active high enable input (nE). Current through the switch will not cause additional V_{CC} current provided the analog voltage is maintained between V_{CC} and GND.

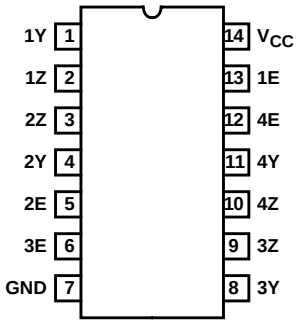
Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE
CD74HC4016E	-55 to 125	14 Ld PDIP
CD74HC4016M	-55 to 125	14 Ld SOIC
CD74HC4016MT	-55 to 125	14 Ld SOIC
CD74HC4016M96	-55 to 125	14 Ld SOIC
CD74HC4016PW	-55 to 125	14 Ld TSSOP
CD74HC4016PWR	-55 to 125	14 Ld TSSOP

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

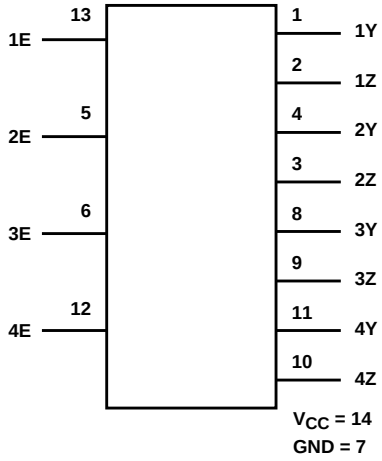
Pinout

CD74HC4016
(PDIP, SOIC, TSSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram

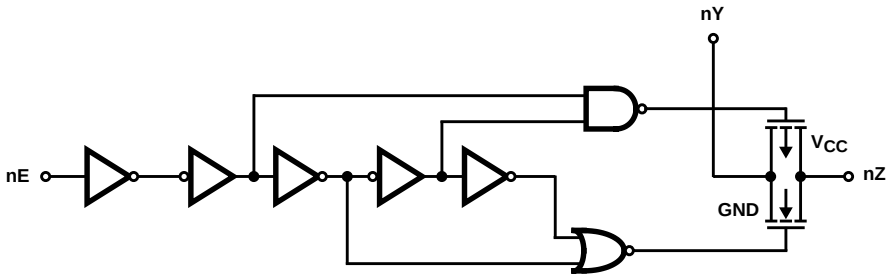


TRUTH TABLE

INPUT nE	SWITCH
L	OFF
H	ON

H = High Level Voltage
L = Low Level Voltage

Logic Diagram



Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, per Output, I_O
For -0.5V < V_O < V_{CC} + 0.5V . . . . . ±25mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 10V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V . . . . . 500ns (Max)
6V . . . . . 400ns (Max)
9V . . . . . 250ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
E (PDIP) Package	80
M (SOIC) Package	86
PW (TSSOP) Package	96

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implie

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
"ON" Resistance I_O = 1mA	R_{ON}	V_{IH} or V_{IL}	V_{CC} or GND	4.5	-	45	180	-	225	-	270	Ω
				6	-	35	160	-	200	-	240	Ω
				9	-	30	135	-	170	-	205	Ω
				4.5	-	85	320	-	400	-	480	Ω
				6	-	55	240	-	300	-	360	Ω
				9	-	35	170	-	215	-	255	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR_{ON}	V_{IL} or V_{IH}	V_{CC} or GND	4.5	-	10	-	-	-	-	-	Ω
				6	-	8.5	-	-	-	-	-	Ω
Switch Off Leakage Current	I_{IZ}	En = GND	V_{CC} or GND	6	-	-	±0.1	-	±1	-	±1	µA
				10	-	-	±0.1	-	±1	-	±1	µA
Logic Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current I_O = 0mA	I_{CC}	V_{CC} or GND	V_{CC} or GND	6	-	-	2	-	20	-	40	µA
				10	-	-	16	-	160	-	320	µA

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, Switch In to Switch Out	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
		C_L = 15pF	5	-	4	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	10	-	13	-	15	ns
			9	-	-	8	-	10	-	12	ns
Propagation Delay, Switch Turn-On En to Out	t_{PZH}, t_{PZL}	C_L = 50pF	2	-	-	190	-	240	-	285	ns
			4.5	-	-	38	-	48	-	57	ns
		C_L = 15pF	5	-	16	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	32	-	41	-	48	ns
			9	-	-	28	-	35	-	42	ns
Propagation Delay, Switch Turn-Off En to Out	t_{PHZ}, t_{PLZ}	C_L = 50pF	2	-	-	145	-	180	-	220	ns
			4.5	-	-	29	-	36	-	44	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	25	-	31	-	38	ns
			9	-	-	22	-	28	-	33	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 2, 3)	C_{PD}	-	5	-	12	-	-	-	-	-	pF

NOTES:

2. C_{PD} is used to determine the dynamic power consumption, per package.
3. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications T_A = 25°C

PARAMETER	TEST CONDITIONS	V_{CC} (V)	CD74HC4016	UNITS
Switch Frequency Response Bandwidth at -3dB Figure 3	Figure 6, Notes 4, 5	4.5	>200	MHz
Crosstalk Between Any Two Switches, Figure 4	Figure 5, Notes 5, 6	4.5	TBE	dB
Total Harmonic Distortion	1kHz, V_{IS} = 4V_{P-P} Figure 7	4, 5	0.078	%
	1kHz, V_{IS} = 8V_{P-P} Figure 7	9	0.018	%

Analog Channel Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	TEST CONDITIONS	V_{CC} (V)	CD74HC4016	UNITS
Control to Switch Feedthrough Noise	Figure 8	4.5	TBE	mV
		9	TBE	mV
Switch "OFF" Signal Feedthrough, Figure 4	Figure 9, Notes 5, 6	4.5	-62	dB
Switch Input Capacitance, C_S		-	5	pF

NOTES:

4. Adjust input level for 0dBm at output, f = 1MHz.
5. V_{IS} is centered at $V_{CC}/2$.
6. Adjust input for 0dBm at V_{IS}.

Typical Performance Curves

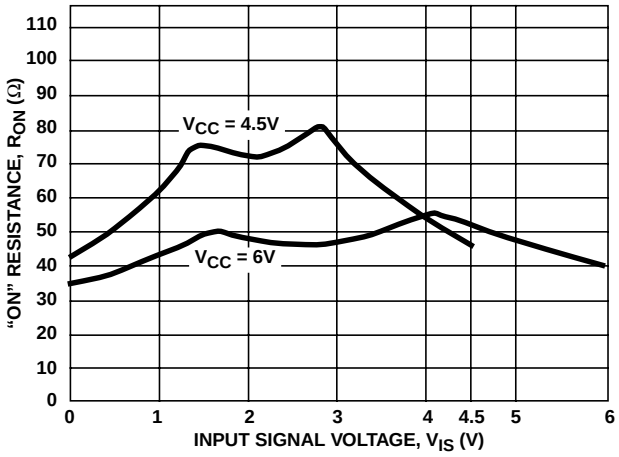


FIGURE 1. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

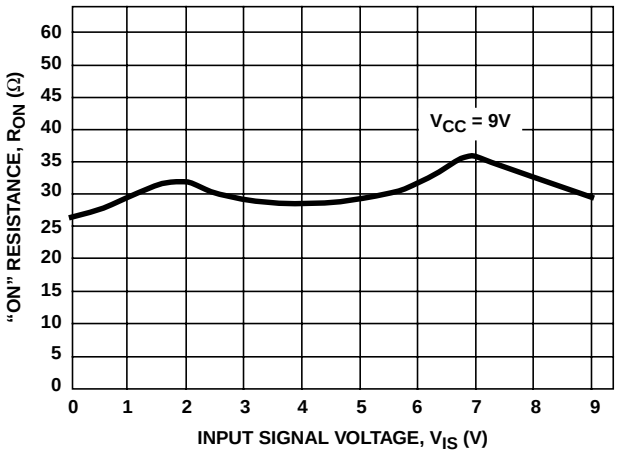


FIGURE 2. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

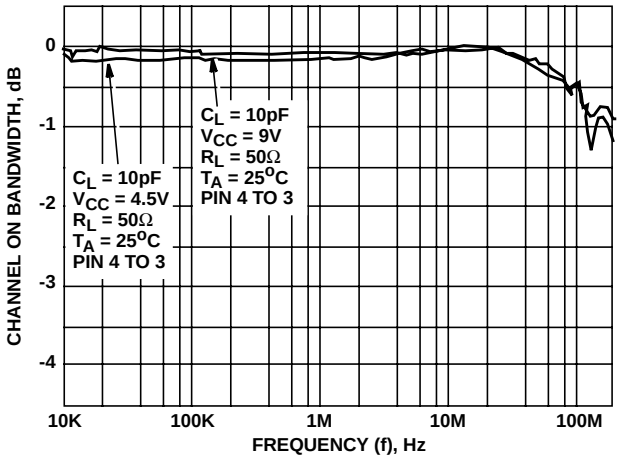


FIGURE 3. SWITCH FREQUENCY RESPONSE

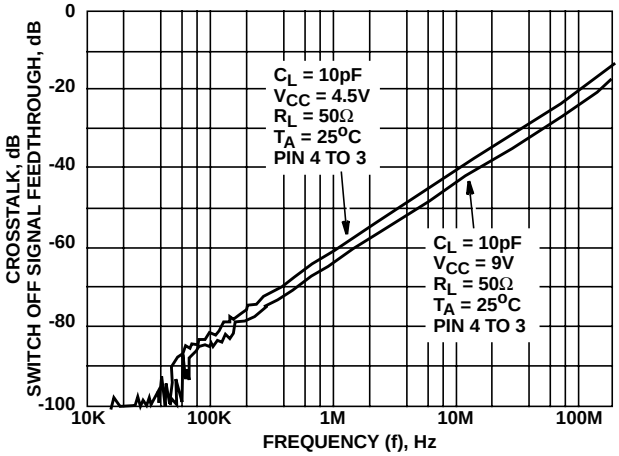


FIGURE 4. SWITCH-OFF SIGNAL FEEDTHROUGH AND CROSSTALK vs FREQUENCY

Analog Test Circuits

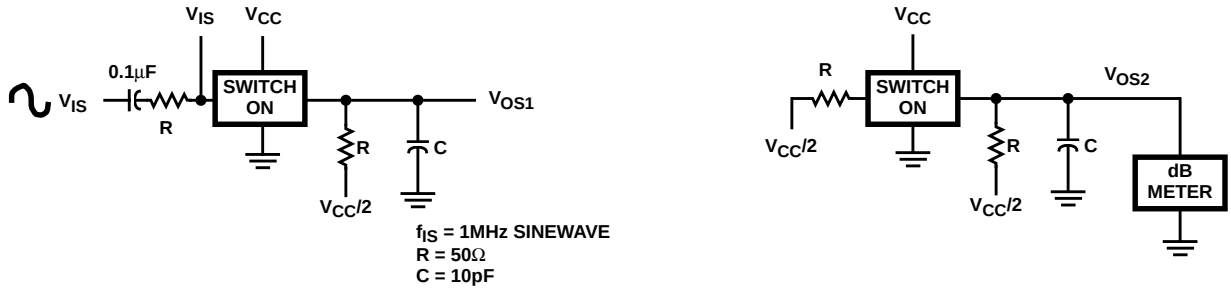


FIGURE 5. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

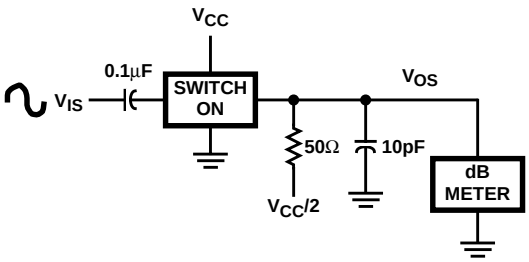


FIGURE 6. FREQUENCY RESPONSE TEST CIRCUIT

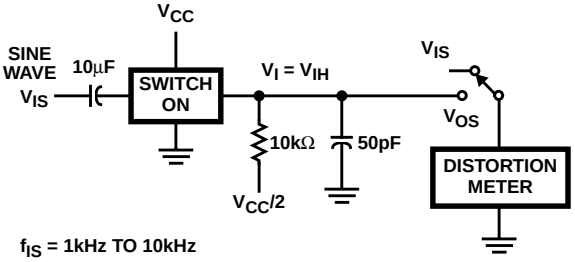


FIGURE 7. TOTAL HARMONIC DISTORTION TEST CIRCUIT

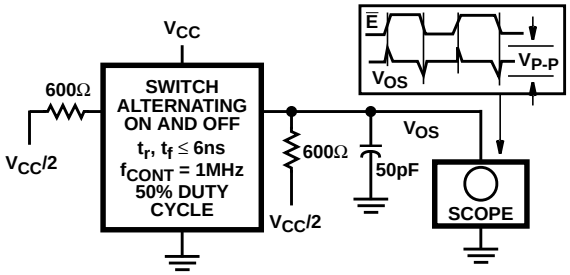


FIGURE 8. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

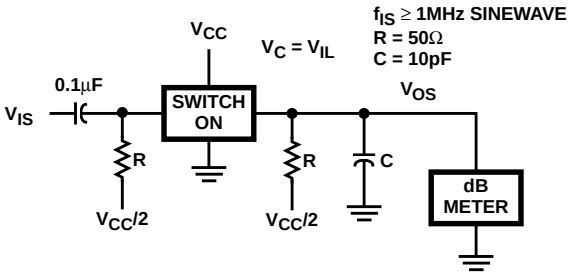


FIGURE 9. SWITCH OFF SIGNAL FEEDTHROUGH

Test Circuits and Waveforms

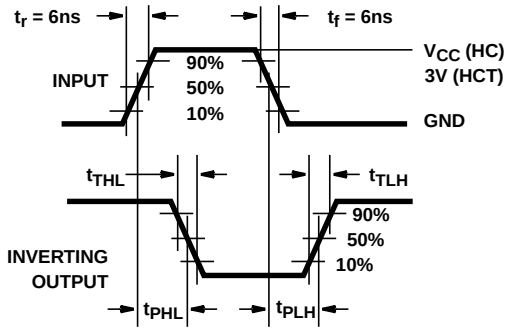


FIGURE 10. HC/HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

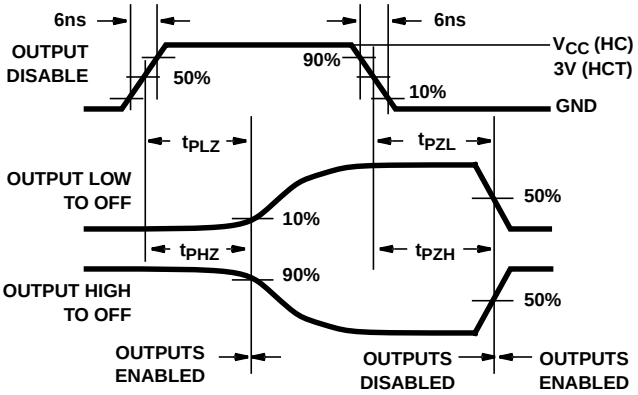


FIGURE 11. SWITCH TURN-ON AND TURN-OFF PROPAGATION DELAY TIMES

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC4016E	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4016E
CD74HC4016E.A	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4016E
CD74HC4016M96	NRND	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4016M
CD74HC4016M96.A	NRND	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4016M
CD74HC4016MT	NRND	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4016M
CD74HC4016MT.A	NRND	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4016M
CD74HC4016PW	NRND	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP14
CD74HC4016PW.A	NRND	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP14

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

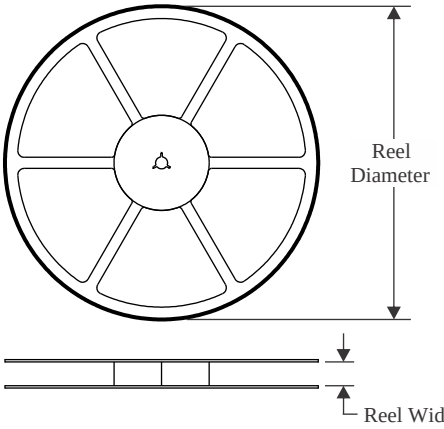
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

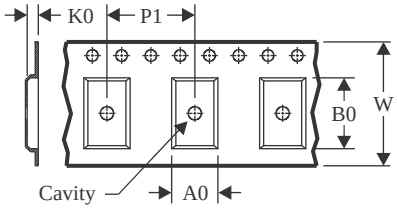
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

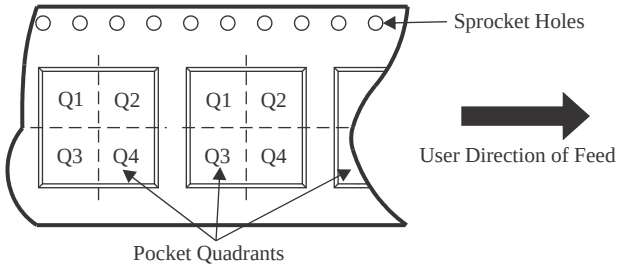


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

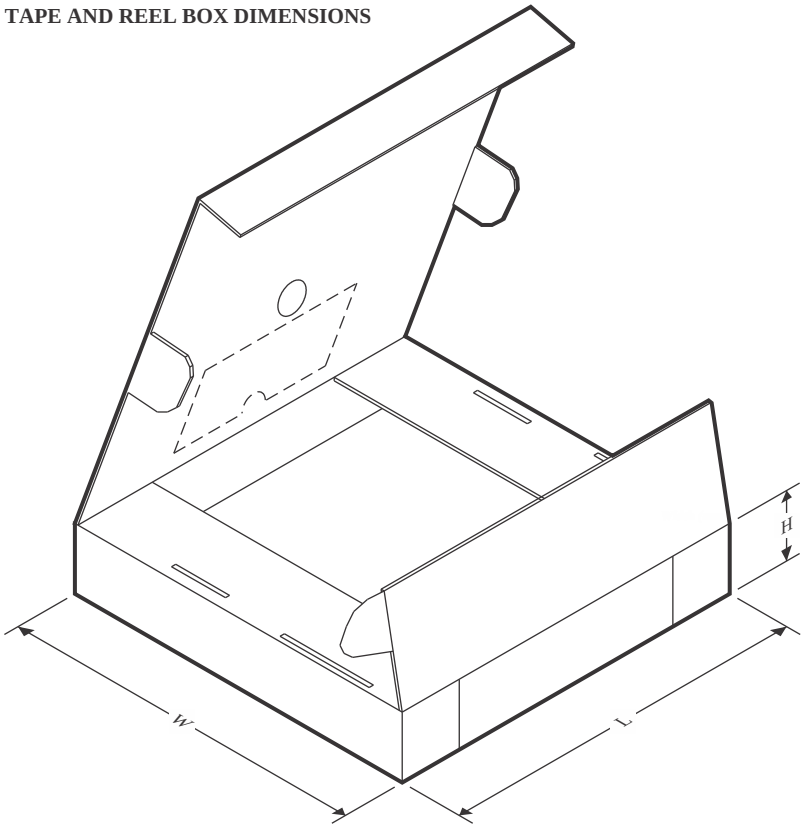
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4016M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC4016MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

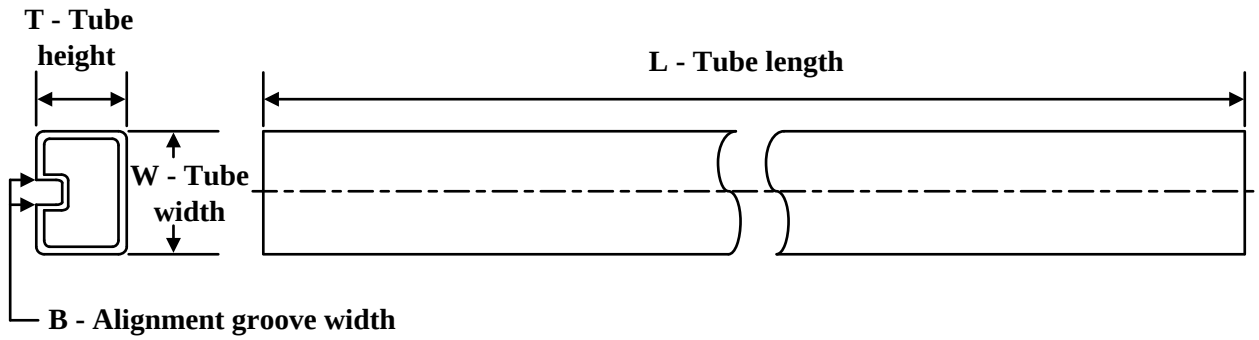
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

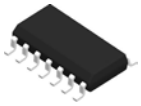
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4016M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74HC4016MT	SOIC	D	14	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC4016E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4016E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4016E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4016E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4016PW	PW	TSSOP	14	90	530	10.2	3600	3.5
CD74HC4016PW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

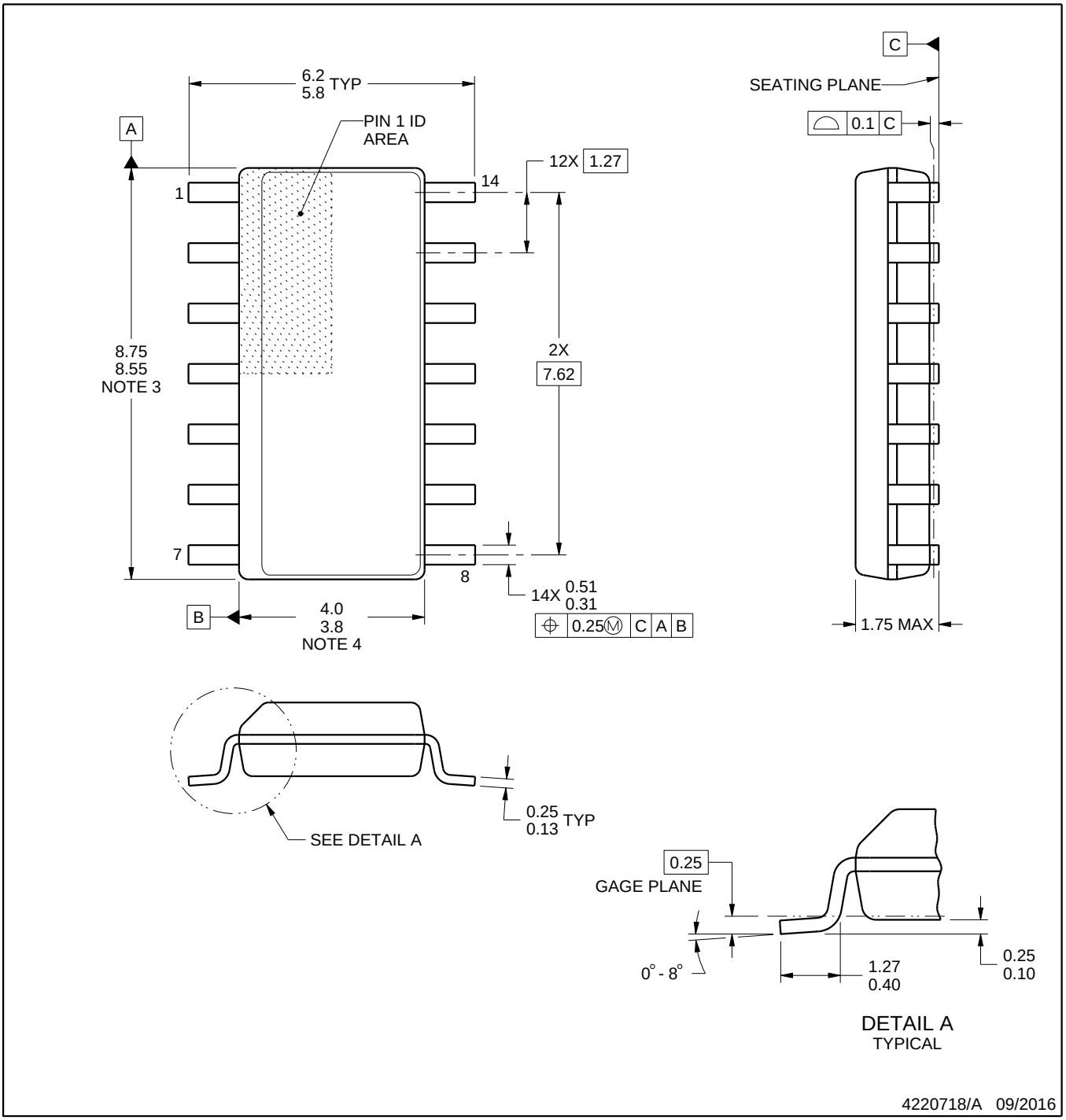


PACKAGE OUTLINE

D0014A

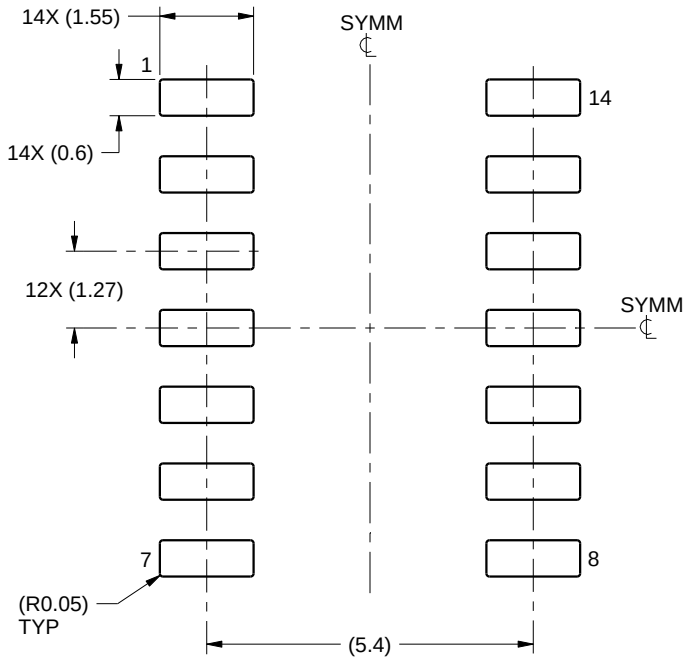
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

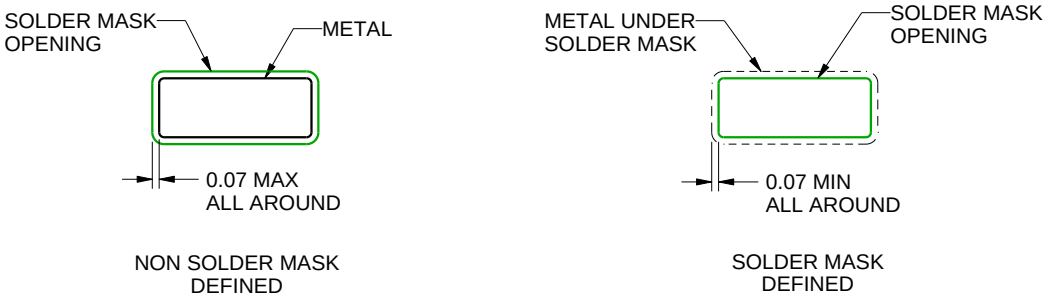


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

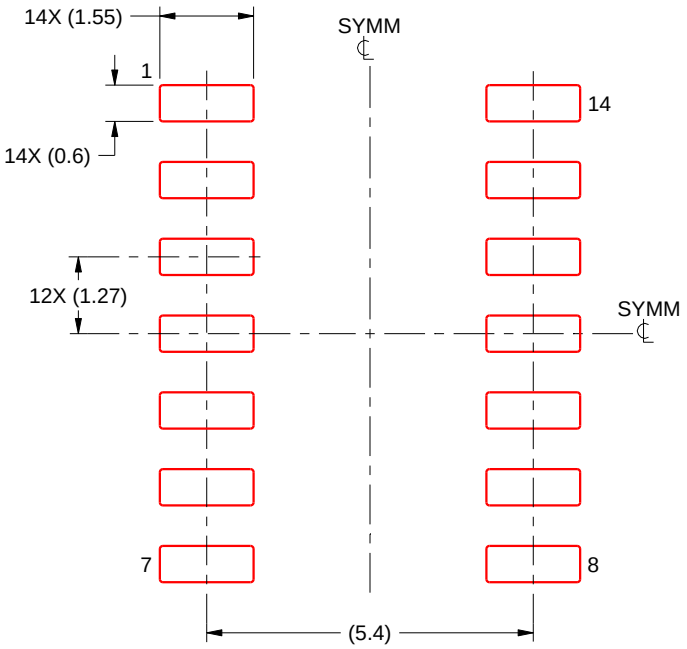
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

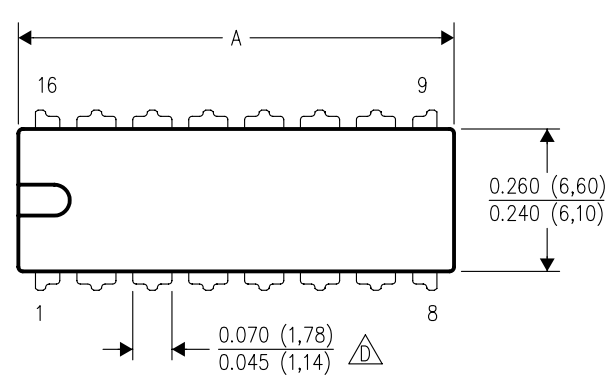
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

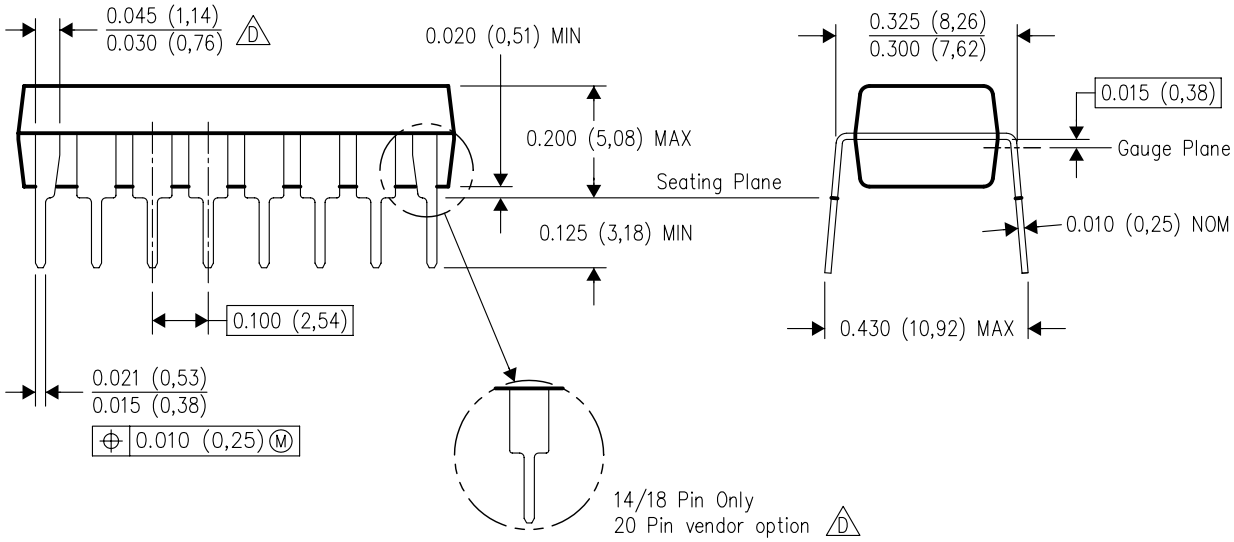
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

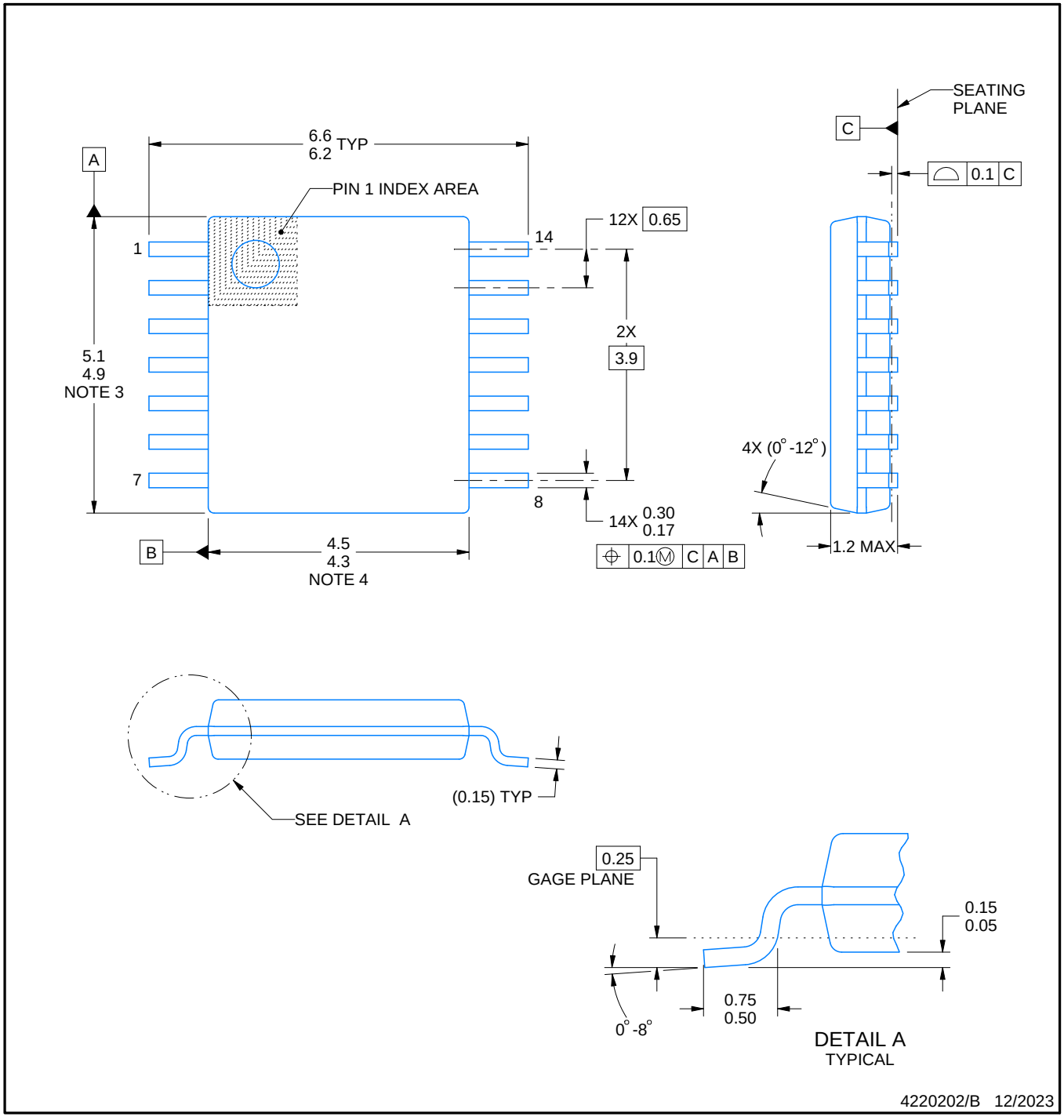
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

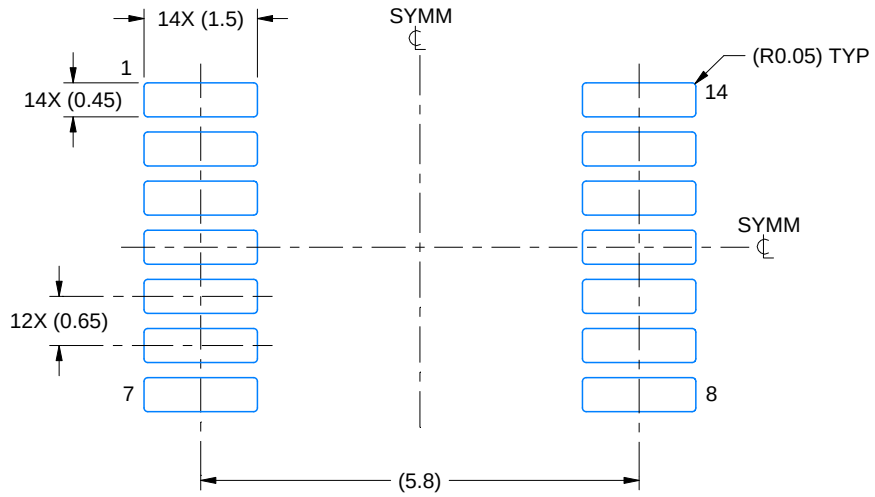
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

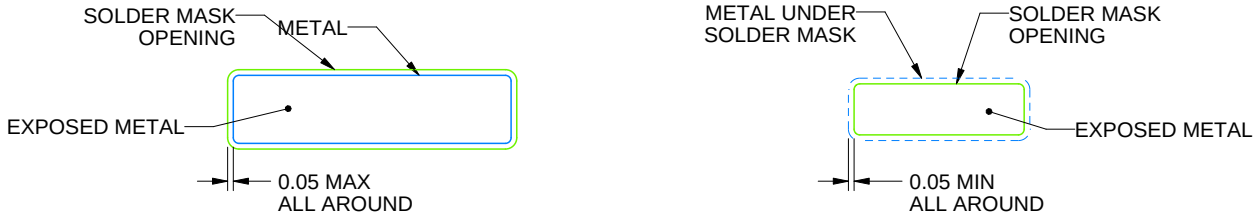


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

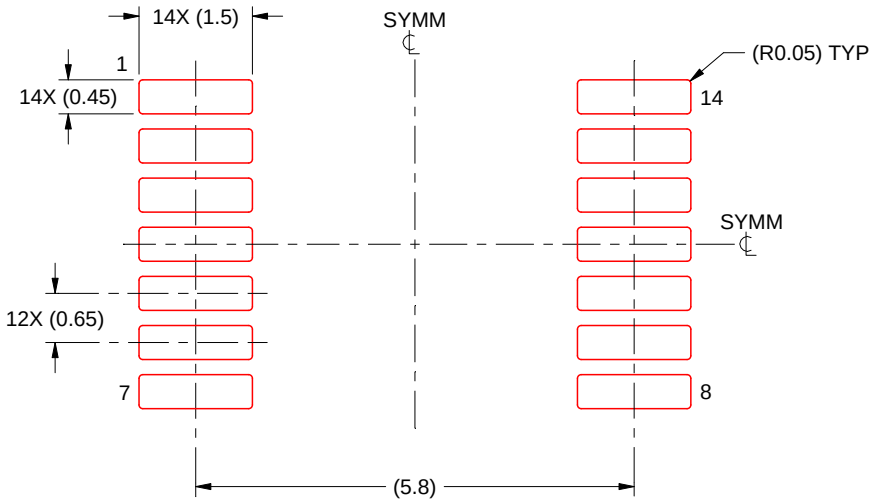


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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