CD74HC390, CDx4HCT390 High-Speed CMOS Logic Dual Decade Ripple Counter

1 Features

- Two BCD decade or bi-quinary counters
- One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50, 100
- Two controller reset inputs to clear each decade counter individually
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range: -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- HC types
  - 2V to 6V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V (max), V_{IH} = 2 V (min)
  - CMOS input compatibility, $I_I \leq 1\ \mu A$ at V_{OL}, V_{OH}

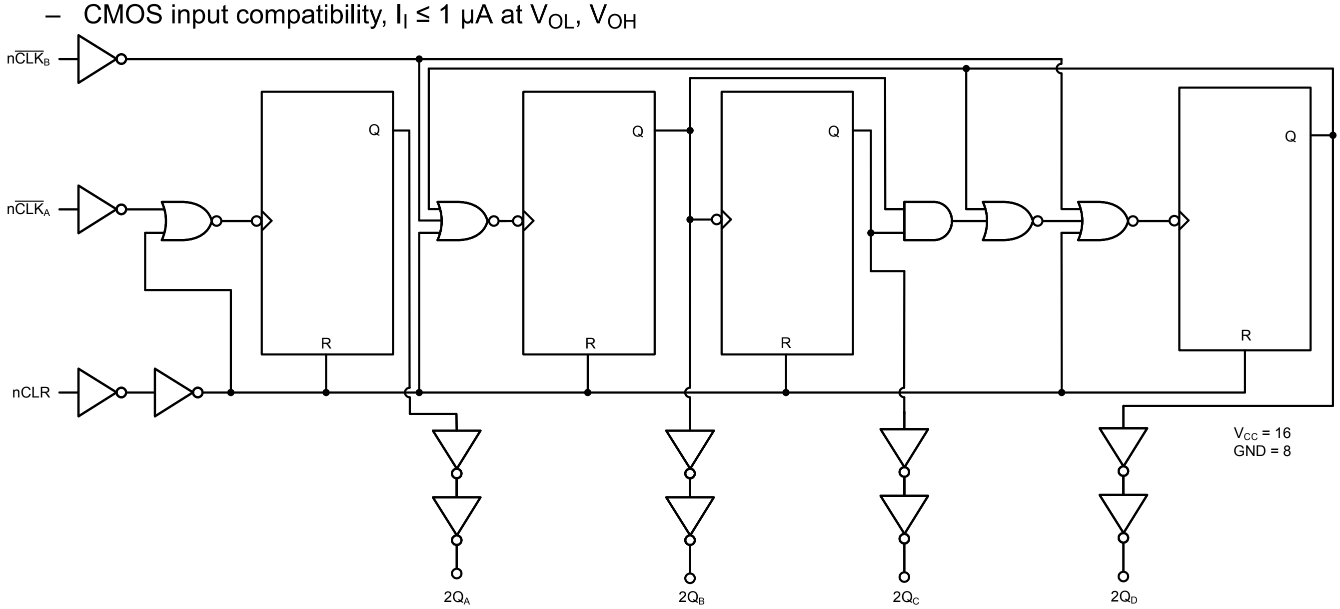
2 Description

The SN74HC390 and ‘HCT390 devices include two independent 4-bit decade ripple counters, falling-edge clocked with asynchronous clear. Each counter is divided into two sections, a divide-by-2 and divide-by-5 counter, each of which has an independent clock input. This allows for very flexible configuration of the device.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD54HCT390F3A	CDIP (16)	24.38 mm × 6.92 mm
CD74HC390M	SOIC (16)	9.90 mm × 3.90 mm
CD74HCT390M	SOIC (16)	9.90 mm × 3.90 mm
CD74HC390E	PDIP (16)	19.31 mm × 6.35 mm
CD74HCT390E	PDIP (16)	19.31 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

Table of Contents

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

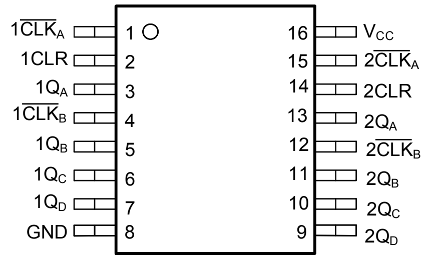
Changes from Revision D (November 2021) to Revision E (April 2022) — **Page**

- Corrected table 7-3, Q_C value 6 from H to L.......10

Changes from Revision C (September 1997) to Revision D (November 2021) — **Page**

- Updated the numbering, formatting, tables, figures, and cross-references throughout the doucment to reflect modern data sheet standards.......1
- Updated pin names to match current TI naming conventions. $1\overline{CP0}$ is now $1\overline{CLK}_A$; 1MR is now 1CLR; $1Q_0$ is now $1Q_A$; $1\overline{CP1}$ is now $1\overline{CLK}_B$; $1Q_1$ is now $1Q_B$; $1Q_2$ is now $1Q_C$; $1Q_3$ is now $1Q_D$; $2Q_3$ is now $2Q_D$; $2Q_2$ is now $2Q_C$; $2Q_1$ is now $2Q_B$; $2\overline{CP1}$ is now $2\overline{CLK}_B$; $2Q_0$ is now $2Q_A$; 2MR is now 2CLR; $2\overline{CP0}$ is now $2\overline{CLK}_A$. 1

4 Pin Configuration and Functions



J, N or D Package
16-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input diode current[2]	($V_I < 0$ or $V_I > V_{CC}$)		±20	mA
I_{OK}	Output diode current[2]	($V_O < 0$ or $V_O > V_{CC}$)		±20	mA
I_O	Output source or sink current per output pin	($V_O = 0$ to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C
	Lead temperature (Soldering 10s) (SOIC - Lead tips only)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V_I, V_O	Input or output voltage		0	V_{CC}	V
t_t	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		–55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC		CD74HC390, CD74HCT390 D (SOIC) 16 PINS	CD74HC390, CD74HCT390 N (PDIP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	73	67	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[1]	V_{CC} (V)	25℃ MIN	25℃ TYP	25℃ MAX	-40℃ to 85℃ MIN	-40℃ to 85℃ MAX	-55℃ to 125℃ MIN	-55℃ to 125℃ MAX	UNIT
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	V
			6			1.8		1.8		1.8	V
V_{OH}	High level output voltage	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
		I_{OH} = – 20 µA	6	5.9			5.9		5.9		V
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
		I_{OH} = – 5.2 mA	6	5.48			5.34		5.2		V
V_{OL}	Low level output voltage	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
		I_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
		I_{OL} = 20 µA	6			0.1		0.1		0.1	V
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	6			±0.1		±1		±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	6			8		80		160	µA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
V_{OL}	Low level output voltage	I_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	5.5			±0.1		±1		±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	5.5			8		80		160	µA
ΔI_{CC} [2]	Additional supply current per input pin	$n\overline{CLK}_A$ inputs held at V_{CC} – 2.1	4.5 to 5.5		100	162		202.5		220.5	µA
		$n\overline{CLK}_B$, CLR inputs held at V_{CC} – 2.1	4.5 to 5.5		100	216		270		294	

(1) $V_I = V_{IH}$ or V_{IL}, unless otherwise noted.
(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8mA.

TEXAS INSTRUMENTS
www.ti.com

5.5 Prerequisite for Switching Characteristics

PARAMETER		V_{CC} (V)	25℃	-40℃ to 85℃		-55℃ to 125℃		UNIT
			MIN	MIN	MAX	MIN	MAX	
HC TYPES								
f_{MAX}	Maximum Clock Frequency	2	6	5		4		MHz
		4.5	30	24		20		
		6	35	28		24		
t_W	Clock Pulse Width, $n\overline{CLK}_A$, $n\overline{CLK}_B$	2	80	100		120		ns
		4.5	16	20		24		
		6	14	17		20		
t_{REM}	Reset Removal Time	2	70	90		105		ns
		4.5	14	18		21		
		6	12	15		18		
t_W	Reset Pulse Width	2	50	65		75		ns
		4.5	10	13		15		
		6	9	11		13		
HCT TYPES								
f_{MAX}	Maximum Clock Frequency	4.5	27	22		18		MHz
t_W	Clock Pulse Width, $n\overline{CLK}_A$, $n\overline{CLK}_B$	4.5	19	24		29		ns
t_{REM}	Reset Removal Time	4.5	15	19		22		ns
t_W	Reset Pulse Width	4.5	13	16		20		ns

5.6 Switching Characteristics

Input t_r, t_f = 6 ns. Unless otherwise specified, C_L = 50pF. (see Parameter Measurement Information)

PARAMETER		V_{CC}(V)	25℃		-40℃ to 85℃	-55℃ to 125℃	UNIT
			TYP	MAX	MAX	MAX	
HC TYPES							
t_{pd}	$n\overline{CLK}_A$ to nQ_A	2		175	220	265	ns
		4.5	14[3]	35	44	53	ns
		6		30	37	45	ns
	$n\overline{CLK}_B$ to nQ_B	2		185	230	280	ns
		4.5		37	46	56	ns
		6		31	39	48	ns
	$n\overline{CLK}_B$ to nQ_C	2		245	305	370	ns
		4.5		49	61	74	ns
		6		42	52	63	ns
	$n\overline{CLK}_B$ to nQ_D	2		180	225	270	ns
		4.5	15[3]	36	45	54	ns
		6		31	38	46	ns
	$n\overline{CLK}_A$ to nQ_D	2		365	455	550	ns
		4.5		73	91	110	ns
		6		62	77	94	ns
	CLR to Q_n	2		190	240	285	ns
		4.5	16[3]	38	48	57	ns
		6		32	41	48	ns

5.6 Switching Characteristics (continued)

Input t_r, t_f = 6 ns. Unless otherwise specified, C_L = 50pF. (see Parameter Measurement Information)

PARAMETER		V_{CC}(V)	25℃		-40℃ to 85℃	-55℃ to 125℃	UNIT
			TYP	MAX	MAX	MAX	
t_t	Output Transition Times	2		75	95	110	ns
		4.5		15	19	22	ns
		6		13	16	19	ns
C_{IN}	Input Capacitance			10	10	10	pF
C_{PD}	Power Dissipation Capacitance(1) (2)	5	28(3)				pF
HCT TYPES							
t_{pd}	$n\overline{CLK}_A$ to nQ_A	4.5	17(3)	40	50	60	ns
	$n\overline{CLK}_B$ to nQ_B	4.5		43	51	65	ns
	$n\overline{CLK}_B$ to nQ_C	4.5		55	69	83	ns
	$n\overline{CLK}_B$ to nQ_D	4.5	18(3)	42	53	63	ns
	$n\overline{CLK}_A$ to nQ_C	4.5		84	105	126	ns
	CLR to Q_n	4.5	18(3)	42	53	63	ns
t_t	Output Transition Times	4.5		15	19	22	ns
C_{IN}	Input Capacitance			10(4)	10(4)	10(4)	pF
C_{PD}	Power Dissipation Capacitance(1) (2)	5	32(3)				pF

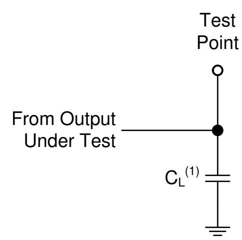
(1) C_{PD} is used to determine the dynamic power consumption, per package.
(2) $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.
(3) C_L = 15 pF and V_{CC} = 5 V.
(4) C_L = 15 pF

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

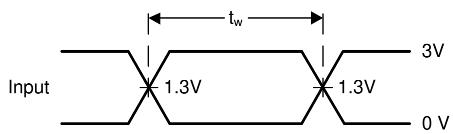


Figure 6-2. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

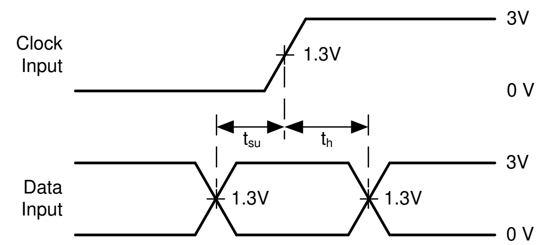
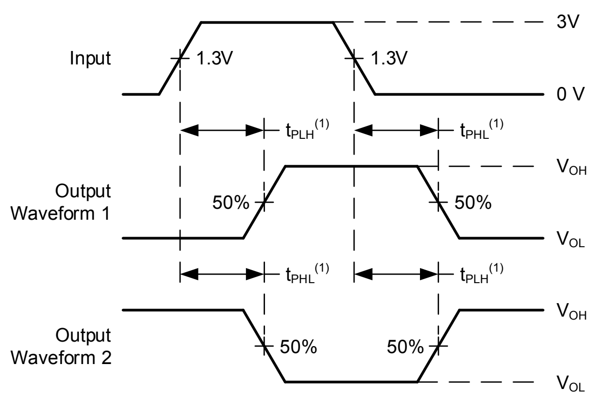


Figure 6-3. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-4. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays

7 Detailed Description

7.1 Overview

The CD74HC390 and ’HCT390 dual 4-bit decade ripple counters are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL). These devices are divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common controller reset (nCLR). If the two controller reset inputs (1CLR and 2CLR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clock inputs (n$\overline{CLK}_A$ and n$\overline{CLK}_B$) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50, or 100. Each section is triggered by the High-to-Low transition of the input pulses (n$\overline{CLK}_A$ and n$\overline{CLK}_B$).

For BCD decade operation, the nQ_A output is connected to the n$\overline{CLK}_B$ input of the divide-by-5 section. For bi-quinary decade operation, the nQ_D output is connected to the n$\overline{CLK}_A$ input and nQ_A becomes the decade output.

The controller reset inputs (1CLR and 2CLR) are active-High asynchronous inputs to each decade counter which operates on the portion of the counter identified by the “1” and “2” prefixes in the pin configuration. A High level on the nCLR input overrides the clock and sets the four outputs Low.

7.2 Functional Block Diagram

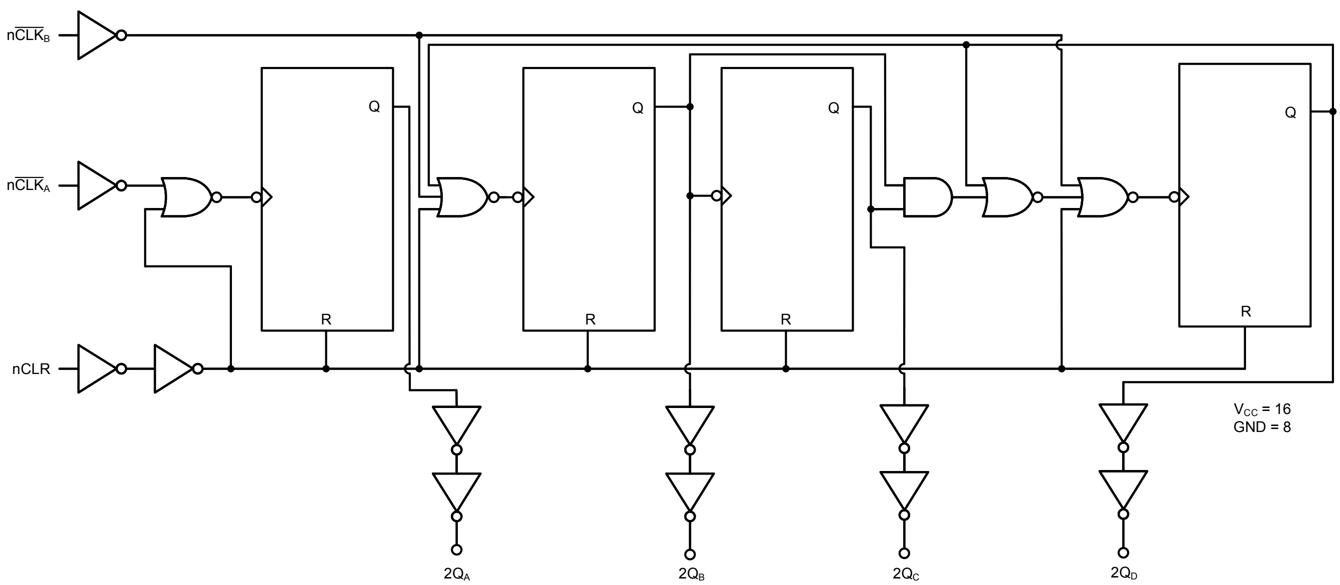


Figure 7-1. Functional Block Diagram

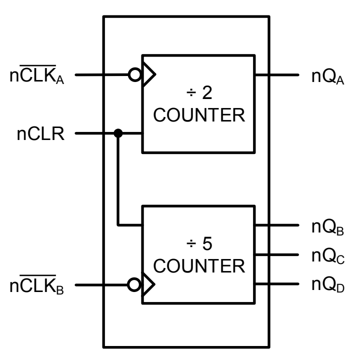


Figure 7-2. Functional Pinout

7.3 Device Functional Modes

Table 7-1. Truth Table[(1)]

INPUTS		ACTION
$\overline{CLK}$	CLR	
↑	L	No Change
↓	L	Count
X	H	All Qs Low

(1) H = High voltage level.
L = Low voltage level.
X = Dont care.
↑ = Transition from low to high level.
↓ = Transition from high to low.

Table 7-2. BCD Count Sequence For ½ the 390[(1)]

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

(1) Ouput nQ_A connected to $n\overline{CLK}_B$ with counter input on $n\overline{CLK}_A$.

Table 7-3. B-Quinary Count Sequence For ½ the 390[(1)]

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	H	L
2	L	H	L	L
3	L	H	H	L
4	H	L	L	L
5	L	L	L	H
6	L	L	H	H
7	L	H	L	H
8	L	H	H	H
9	H	L	L	H

(1) Output nQ_D connected to $n\overline{CLK}_A$ with counter input on $n\overline{CLK}_B$.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9098401MEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9098401ME A CD54HCT390F3A
CD54HCT390F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9098401ME A CD54HCT390F3A
CD54HCT390F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9098401ME A CD54HCT390F3A
CD74HC390E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC390E
CD74HC390E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC390E
CD74HC390EE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC390E
CD74HC390M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC390M
CD74HC390M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC390M
CD74HC390M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC390M
CD74HCT390E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT390E
CD74HCT390E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT390E
CD74HCT390EE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT390E
CD74HCT390M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT390M
CD74HCT390M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT390M
CD74HCT390M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT390M
CD74HCT390MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT390M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HCT390, CD74HCT390 :

- Catalog : CD74HCT390

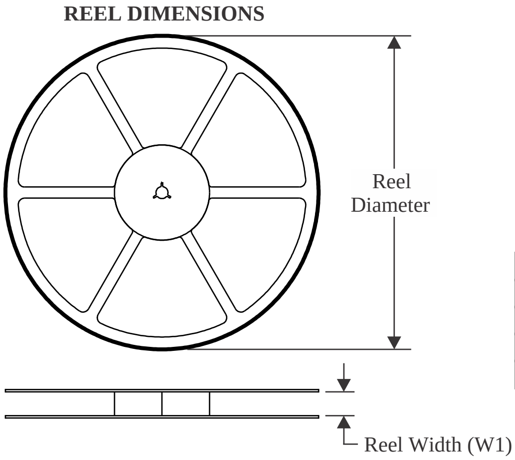
- Military : CD54HCT390

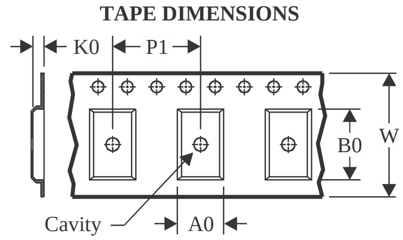
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

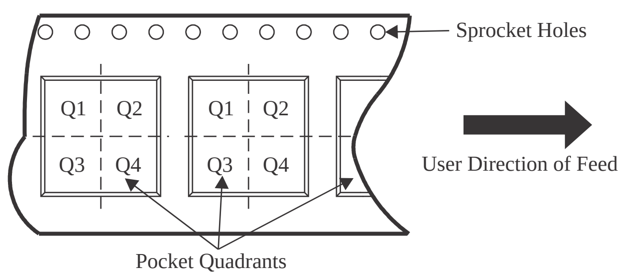
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION





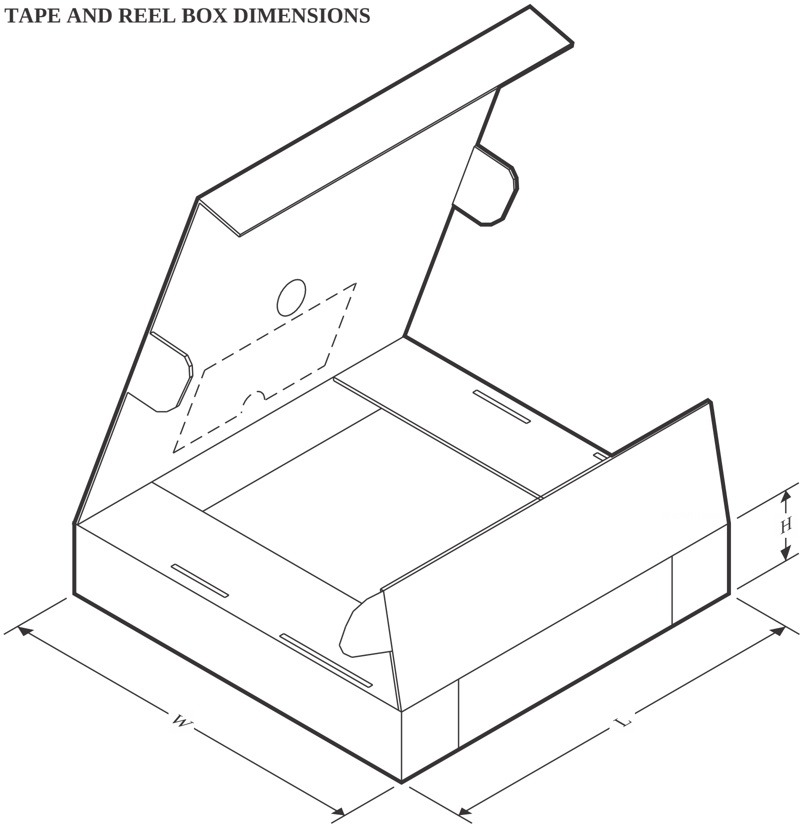
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC390M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT390M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

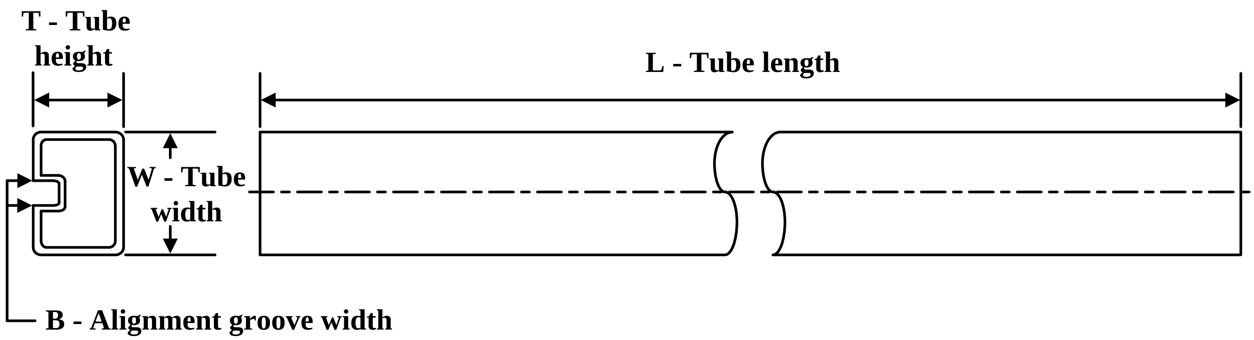
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC390M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT390M96	SOIC	D	16	2500	353.0	353.0	32.0

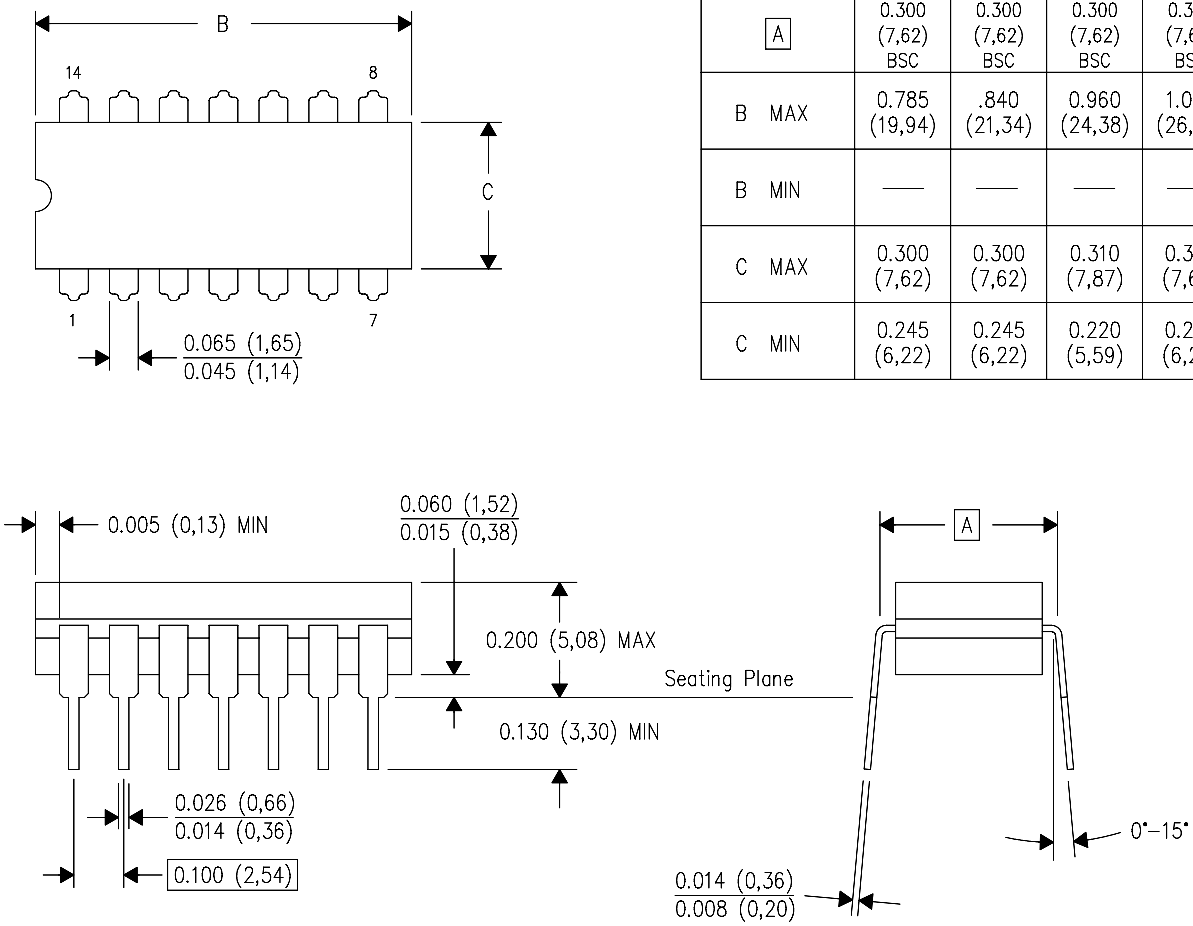
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC390E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC390E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC390E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC390E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC390EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC390EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390EE4	N	PDIP	16	25	506	13.97	11230	4.32

14 LEADS SHOWN



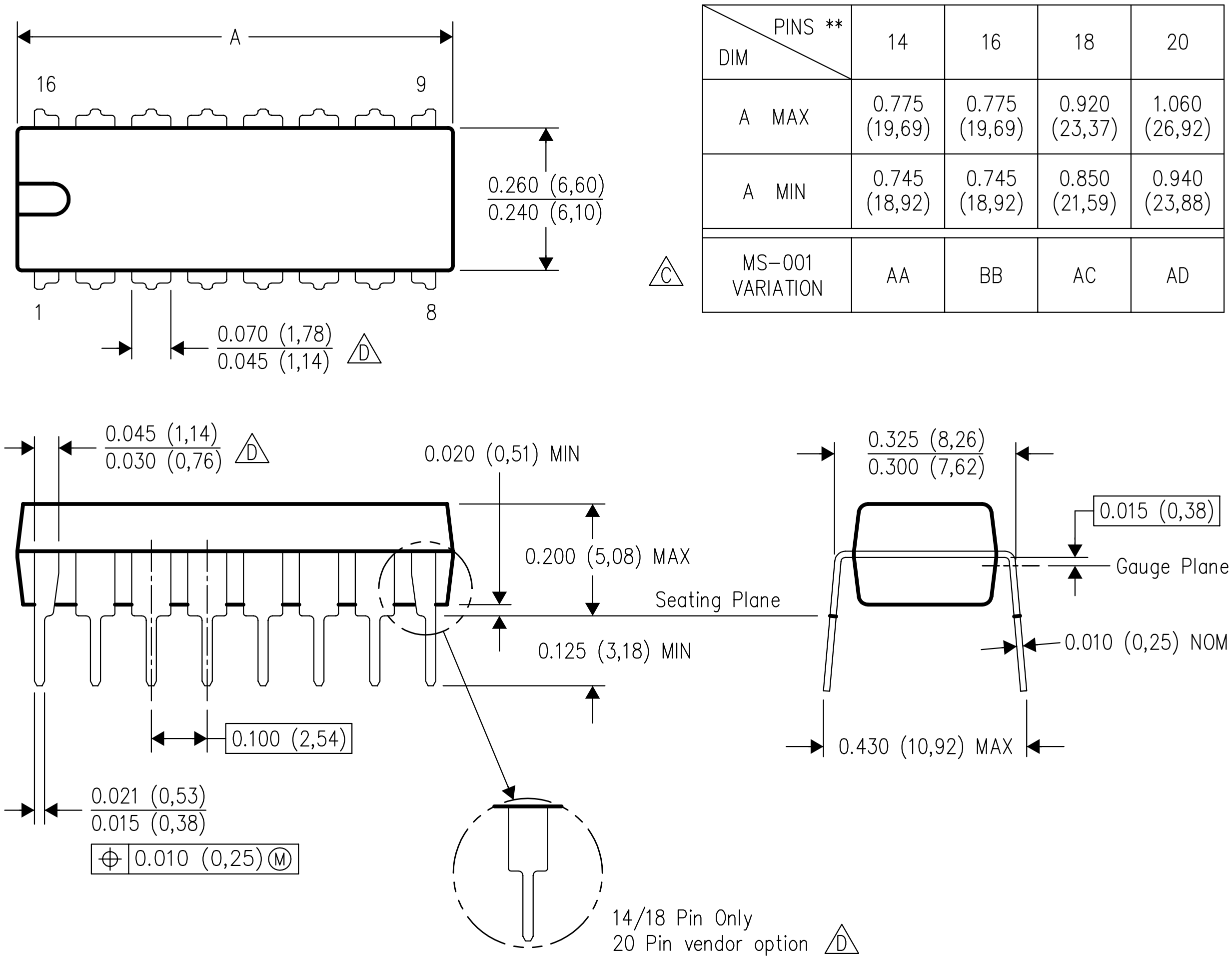
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

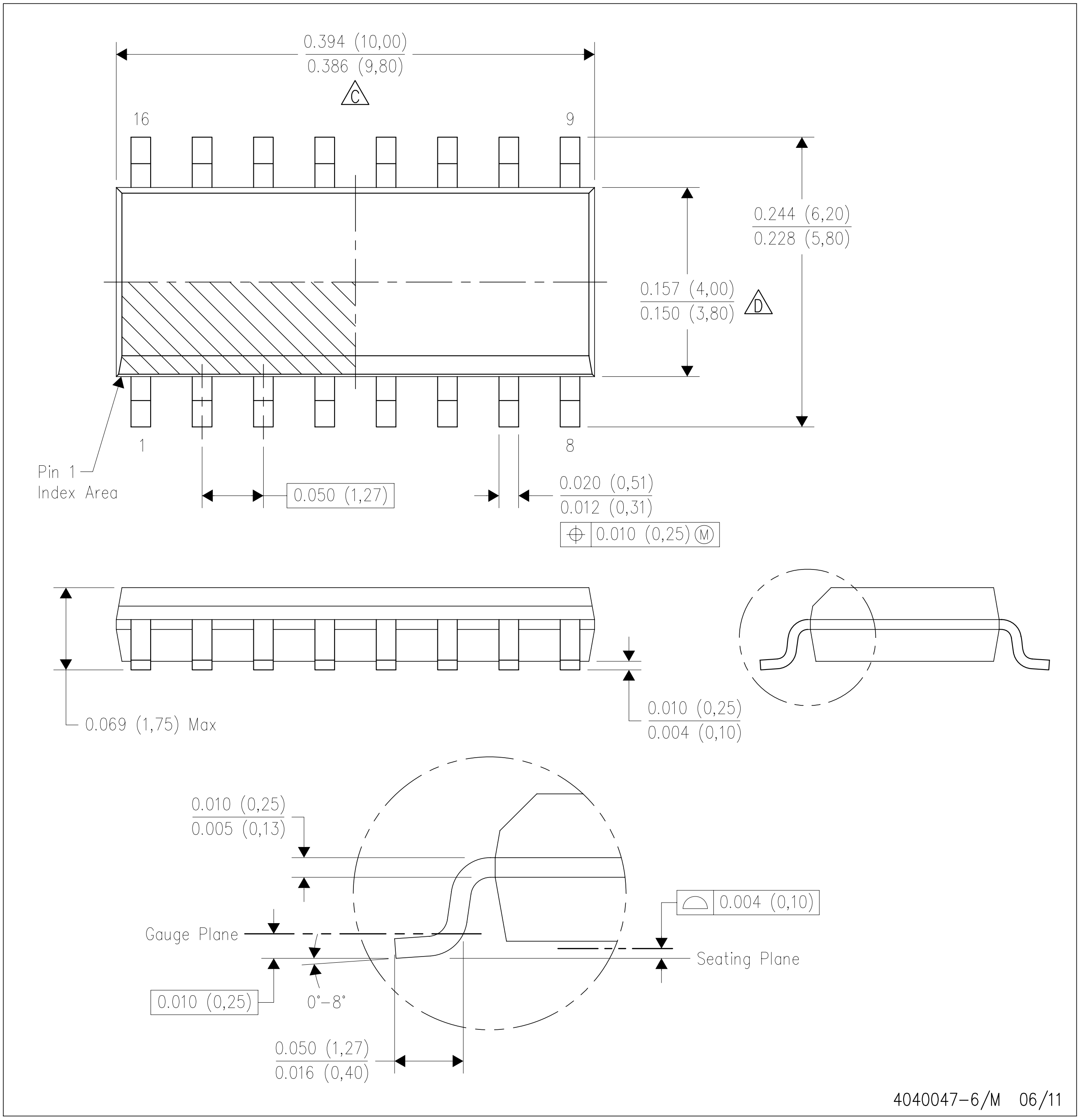


PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265