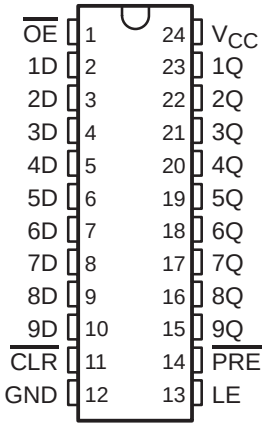
- **BiCMOS Technology With Low Quiescent Power**
- **Buffered Inputs**
- **Noninverted Outputs**
- **Input/Output Isolation From V_{CC}**
- **Controlled Output Edge Rates**
- **48-mA Output Sink Current**
- **Output Voltage Swing Limited to 3.7 V**
- **SCR Latch-Up-Resistant BiCMOS Process and Circuit Design**
- **Packaged in Plastic Small-Outline Package**

M PACKAGE
(TOP VIEW)



description

The CD74FCT843A is a 9-bit, bus-interface, D-type latch with 3-state outputs, designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device uses a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below V_{CC}. This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 mA.

The CD74FCT843A outputs are transparent to the inputs when the latch-enable (LE) input is high. The latches are transparent D-type latches. When LE goes low, the data is latched. The output-enable ($\overline{OE}$) input controls the 3-state outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state. The latch operation is independent of the state of the output enable. This device, having preset ($\overline{PRE}$) and clear ($\overline{CLR}$), are ideal for parity-bus interfacing. When $\overline{PRE}$ is low, the outputs are high if $\overline{OE}$ is low. $\overline{PRE}$ overrides $\overline{CLR}$. When $\overline{CLR}$ is low, the outputs are low if $\overline{OE}$ is low. When $\overline{CLR}$ is high, data can be entered into the latch. The device provides noninverted outputs.

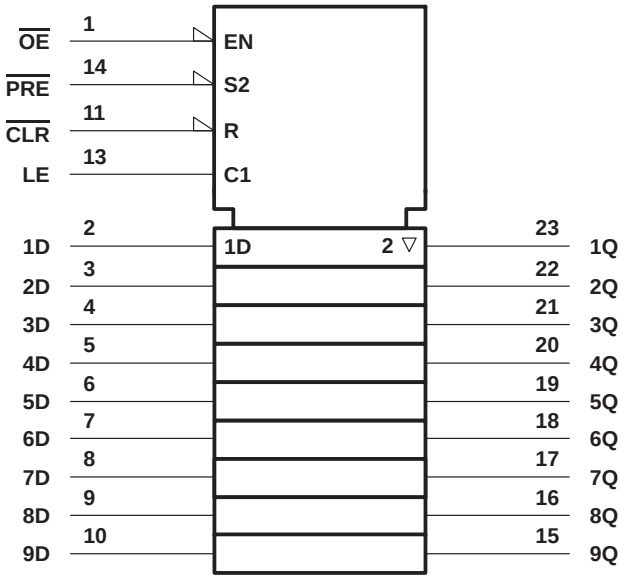
$\overline{OE}$ does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The CD74FCT843A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each latch)

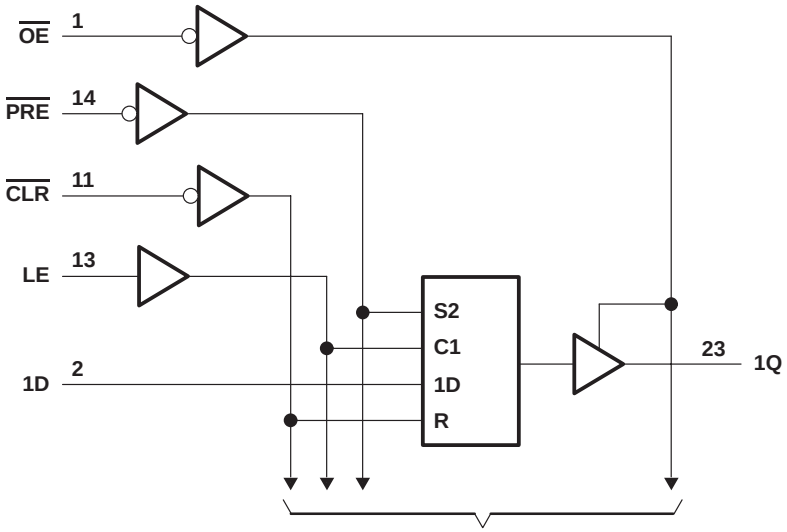
INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

DC supply voltage range, V_{CC} . . . . . –0.5 V to 6 V
DC input clamp current, I_{IK} (V_I < –0.5 V) . . . . . –20 mA
DC output clamp current, I_{OK} (V_O < –0.5 V) . . . . . –50 mA
DC output sink current per output pin, I_{OL} . . . . . 70 mA
DC output source current per output pin, I_{OH} . . . . . –30 mA
Continuous current through V_{CC}, (I_{CC}) . . . . . 237 mA
Continuous current through GND . . . . . 453 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 46°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
V_{IK}	I_I = –18 mA	4.75 V		–1.2		–1.2	V
V_{OH}	I_{OH} = –15 mA	4.75 V	2.4		2.4		V
V_{OL}	I_{OL} = 48 mA	4.75 V		0.55		0.55	V
I_I	V_I = V_{CC} or GND	5.25 V		±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.25 V		±0.5		±10	μA
I_{OS}‡	V_I = V_{CC} or GND, V_O = 0	5.25 V	–75		–75		mA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.25 V		8		80	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at V_{CC} or GND	5.25 V		1.6		1.6	mA
C_i	V_I = V_{CC} or GND			10		10	pF
C_o	V_O = V_{CC} or GND			15		15	pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

§ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

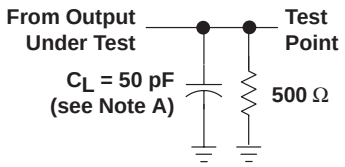
timing requirements over recommended operating temperature conditions (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
t_w	Pulse duration	CLR low	8		ns
		$\overline{PRE}$ low	8		
		LE low	4		
t_{su}	Setup time	Data before LE↓	2.5		ns
		$\overline{PRE}$ inactive	1.4		
		$\overline{CLR}$ inactive	1.4		
t_h	Hold time	Data before LE↓	2.5		ns
t_{rec}	Recovery time	$\overline{PRE}$, $\overline{CLR}$	14		ns

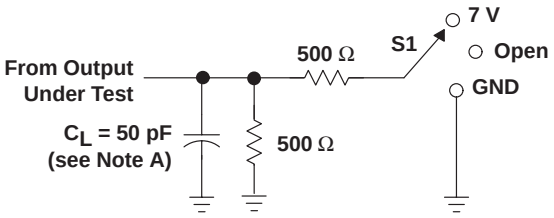
switching characteristics over recommended operating temperature conditions (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C	MIN	MAX	UNIT
			TYP			
t_{pd}	D	Q	6.8	1.5	9	ns
	LE		9	1.5	12	
t_{PLH}	$\overline{PRE}$	Q	9	1.5	12	ns
t_{PHL}	$\overline{CLR}$	Q	9.8	1.5	13	ns
t_{en}	$\overline{OE}$	Q	10.5	1.5	14	ns
t_{dis}	$\overline{OE}$	Q	6	1.5	8	ns

PARAMETER MEASUREMENT INFORMATION

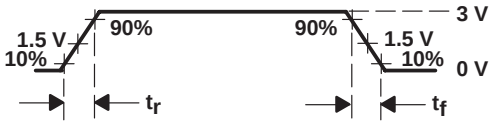


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

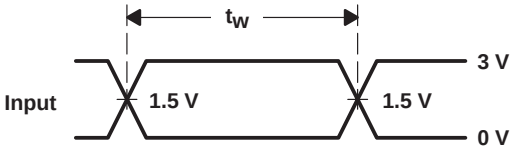


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
Open Drain	7 V

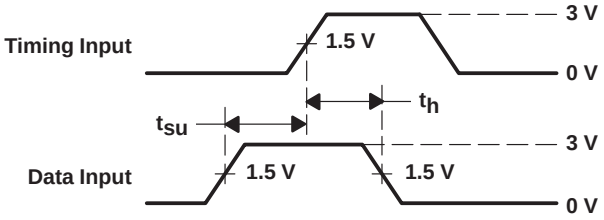
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



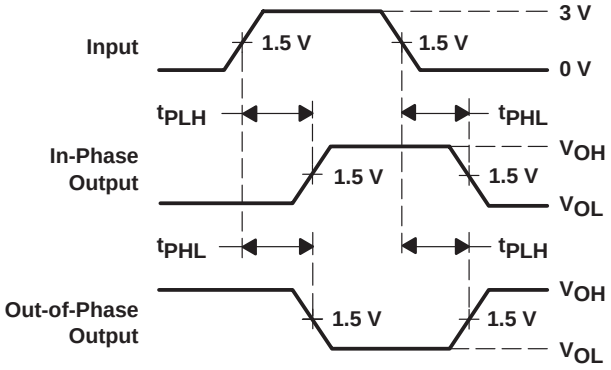
VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



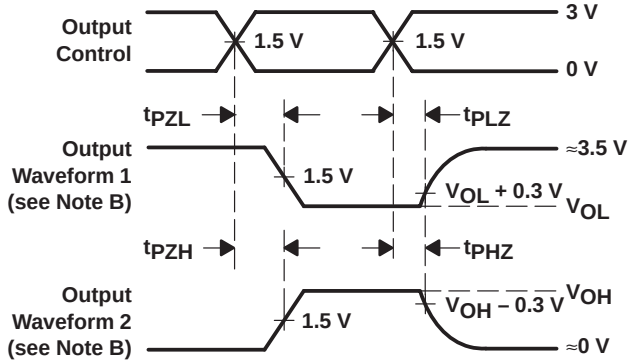
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r and t_f = 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74FCT843AM	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74FCT843AM
CD74FCT843AM.A	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74FCT843AM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

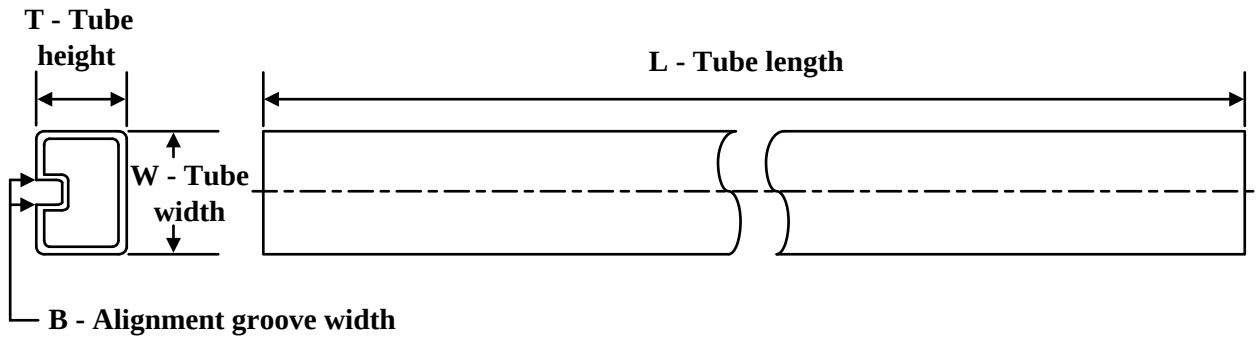
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

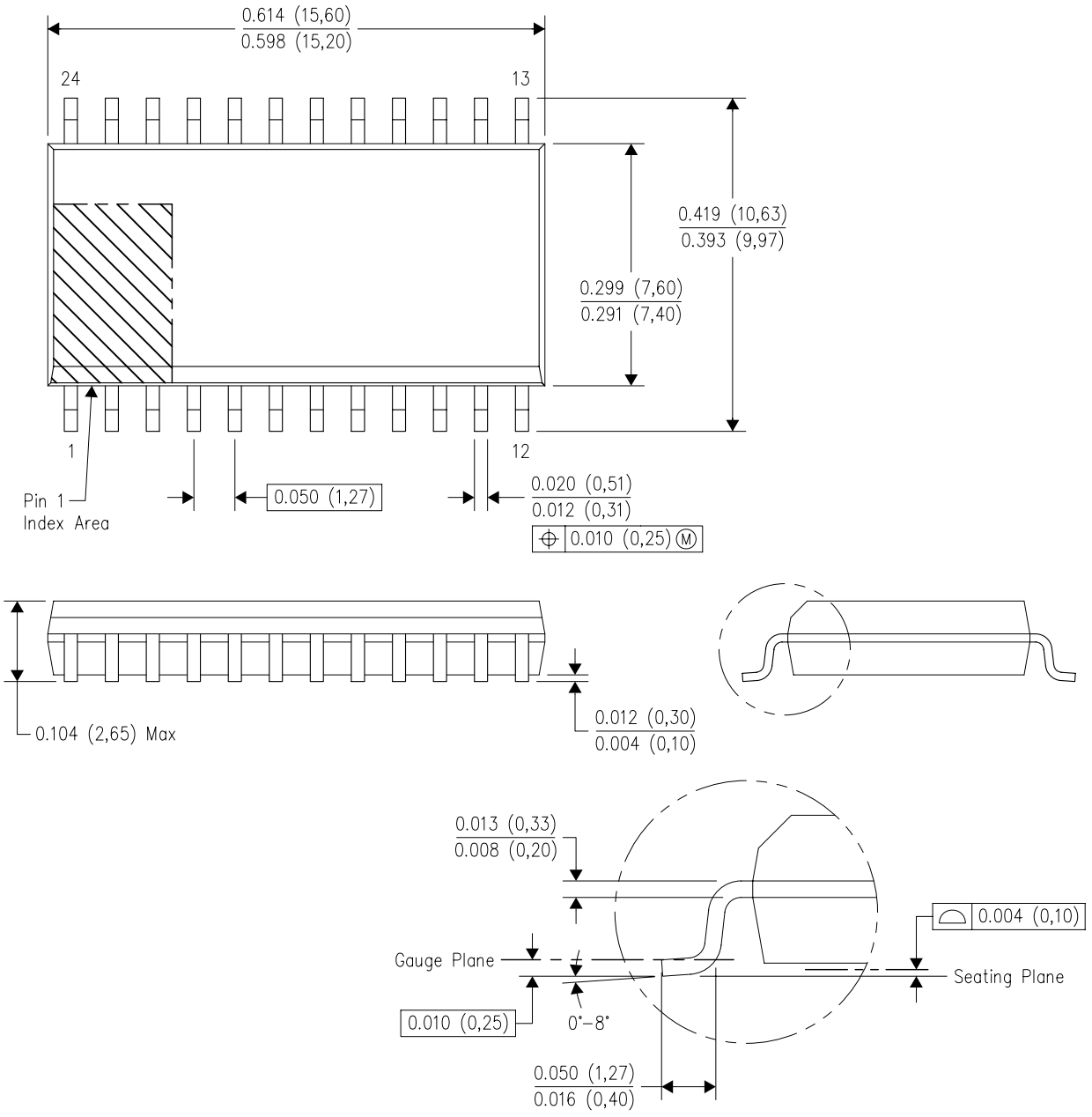
TUBE



*All dimensions are nominal

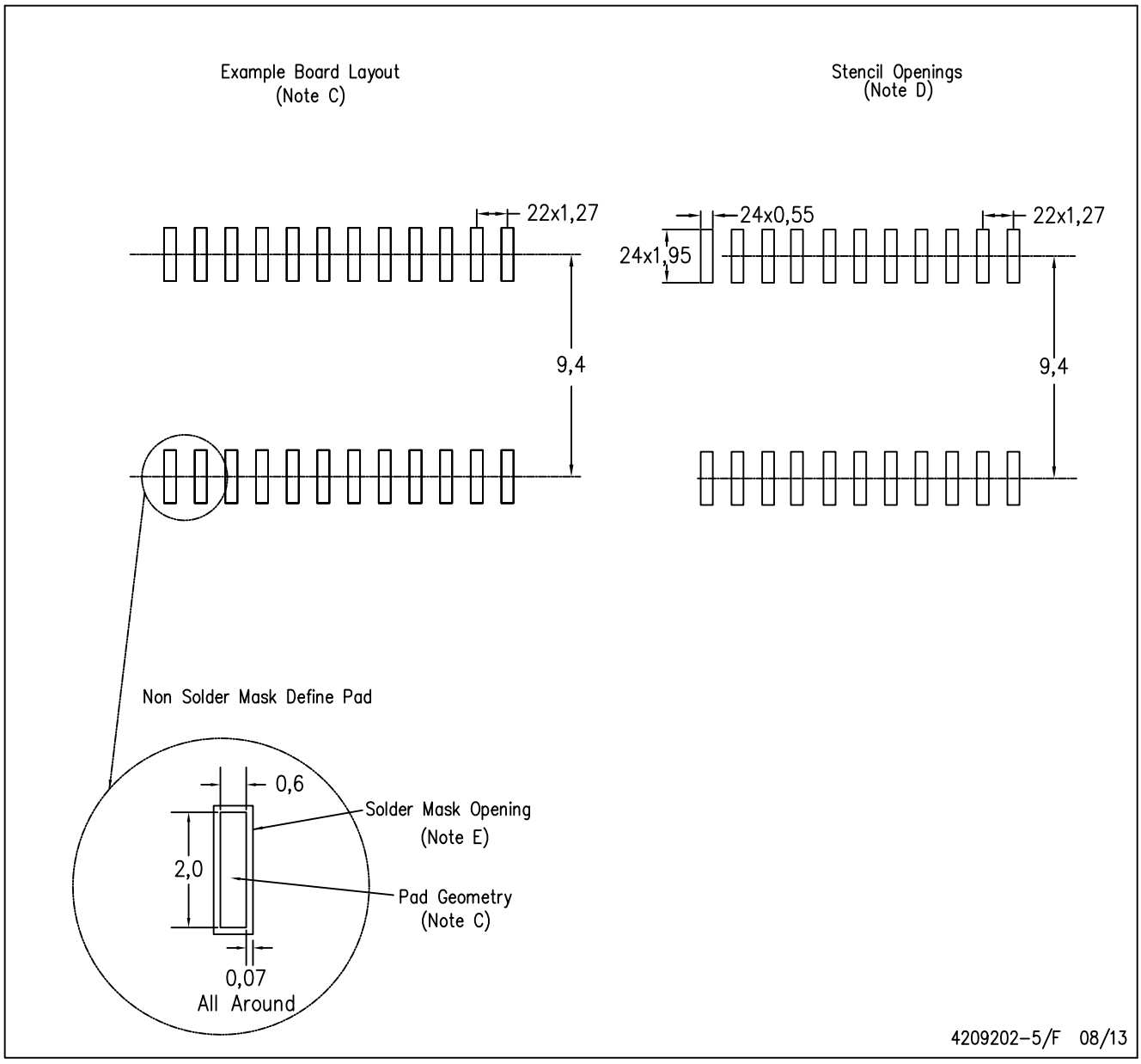
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74FCT843AM	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD74FCT843AM.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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