

CDx4HC165, CDx4HCT165 High-Speed CMOS Logic 8-Bit Parallel-In/Serial-Out Shift Register

1 Features

- Buffered inputs
- Asynchronous parallel load
- Complementary outputs
- Fanout (over temperature range)
 - Standard outputs: 10 LSTTL Loads
 - Bus driver outputs: 15 LSTTL Loads
- Wide operating temperature range: -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC Types
 - 2 V to 6 V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5 V to 5.5 V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8 V$ (Max), $V_{IH} = 2 V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1 \mu A$ at V_{OL} , V_{OH}

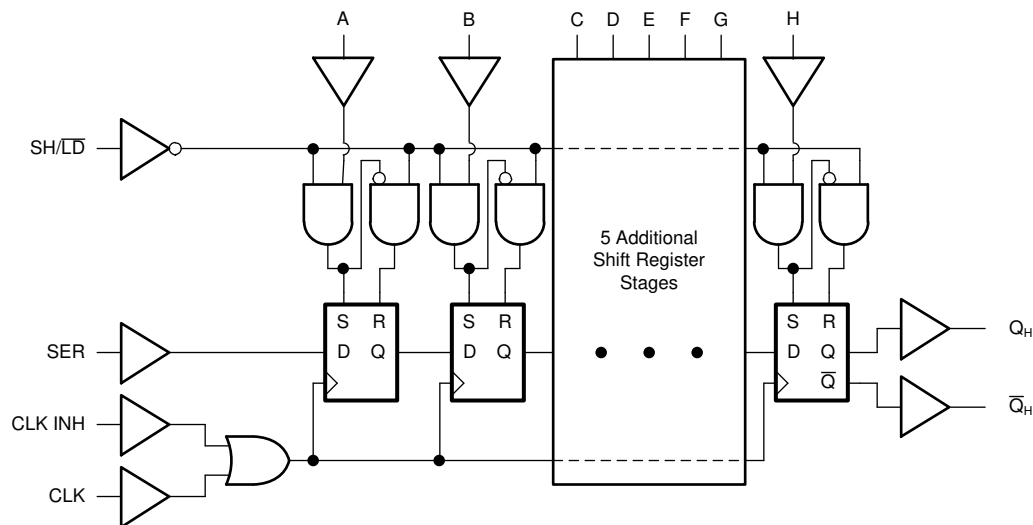
2 Description

The 'HC165 and 'HCT165 are 8-bit parallel or serial-in shift registers with complementary serial outputs (Q_H and \bar{Q}_H) available from the last stage. When the parallel load (SH/\bar{LD}) input is LOW, parallel data from the A to H inputs are loaded into the register asynchronously. When the SH/\bar{LD} is HIGH, data enters the register serially at the SER input and shifts one place to the right ($A \rightarrow B \rightarrow C$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by connecting the Q_H output to the SER input of the succeeding device.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|---------------|------------------------|--------------------|
| CD54HC165F3A | CDIP (16) | 24.38 mm × 6.92 mm |
| CD74HC165M | SOIC (16) | 9.90 mm × 3.90 mm |
| CD74HC165E | PDIP (16) | 19.31 mm × 6.35 mm |
| CD54HCT165F3A | CDIP (16) | 24.38 mm × 6.92 mm |
| CD74HCT165M | SOIC (16) | 9.90 mm × 3.90 mm |
| CD74HCT165E | PDIP (16) | 19.31 mm × 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Diagram



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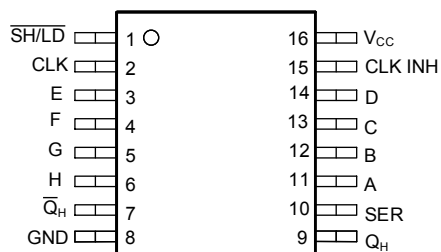
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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (October 2003) to Revision D (November 2021) | Page |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards..... | 1 |
| • Updated pin names to match current TI naming conventions. \overline{PL} is now SH/LD, CP is now CLK, D4 is now E, D5 is now F, D6 is now G, D7 is now H, $\overline{Q_7}$ is now $\overline{Q_H}$, Q_7 is now Q_H , DS is now SER, D0 is now A, D1 is now B, D2 is now C, D3 is now D, \overline{CE} is now CLK INH..... | 1 |

4 Pin Configuration and Functions



J, N, or D package
16-Pin CDIP, PDIP, SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------|---------------------------------------------------------|------------------------------------------------------------|------|----------|------|
| V_{CC} | Supply voltage | | -0.5 | 7 | V |
| I_{IK} | Input diode current | For $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | | ± 20 | mA |
| I_{OK} | Output diode current | For $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | | ± 20 | mA |
| I_O | Drain current per output | For $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | | ± 25 | mA |
| I_O | Output source or sink current per output pin | For $V_O > -0.5\text{ V}$ or $V_O < V_{CC} + 0.5\text{ V}$ | | ± 25 | mA |
| | Continuous current through V_{CC} or GND | | | ± 50 | mA |
| T_J | Junction temperature | | | 150 | °C |
| T_{stg} | Storage temperature | | -65 | 150 | °C |
| | Lead temperature (Soldering 10s) (SOIC- Lead tips only) | | | 300 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|------------|--------------------------|-----------|-----|----------|------|
| V_{CC} | Supply voltage range | HC Types | 2 | 6 | V |
| | | HCT Types | 4.5 | 5.5 | |
| V_I, V_O | Input or output voltage | | 0 | V_{CC} | V |
| t_t | Input rise and fall time | 2 V | | 1000 | ns |
| | | 4.5 V | | 500 | |
| | | 6 V | | 400 | |
| T_A | Temperature range | | -55 | 125 | °C |

5.3 Thermal Information

| THERMAL METRIC | | CD74HC165, CD74HCT165 | | UNIT |
|-----------------|-------------------------------------------------------|-----------------------|----------|------|
| | | D (SOIC) | N (PDIP) | |
| | | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ⁽¹⁾ | 73 | 67 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

| PARAMETER | | TEST CONDITIONS ⁽²⁾ | V _{CC} (V) | 25°C | | | -40°C to 85°C | | -55°C to 125°C | | UNIT |
|---------------------------------|---------------------------------------------------|----------------------------------------------------|---------------------|---------|-----|-----|---------------|-----|----------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| V _{IH} | High level input voltage | | 2 | 1.5 | | | 1.5 | | 1.5 | | V |
| | | | 4.5 | 3.15 | | | 3.15 | | 3.15 | | V |
| | | | 6 | 4.2 | | | 4.2 | | 4.2 | | V |
| V _{IL} | Low level input voltage | | 2 | 0.5 | | | 0.5 | | 0.5 | | V |
| | | | 4.5 | 1.35 | | | 1.35 | | 1.35 | | V |
| | | | 6 | 1.8 | | | 1.8 | | 1.8 | | V |
| V _{OH} | High level output voltage | I _{OH} = − 20 μA | 2 | 1.9 | | | 1.9 | | 1.9 | | V |
| | | I _{OH} = − 20 μA | 4.5 | 4.4 | | | 4.4 | | 4.4 | | V |
| | | I _{OH} = − 20 μA | 6 | 5.9 | | | 5.9 | | 5.9 | | V |
| | High level output voltage | I _{OH} = − 4 mA | 4.5 | 3.98 | | | 3.84 | | 3.7 | | V |
| | | I _{OH} = − 5.2 mA | 6 | 5.48 | | | 5.34 | | 5.2 | | V |
| | | | | | | | | | | | |
| V _{OL} | Low level output voltage | I _{OL} = 20 μA | 2 | 0.1 | | | 0.1 | | 0.1 | | V |
| | | I _{OL} = 20 μA | 4.5 | 0.1 | | | 0.1 | | 0.1 | | V |
| | | I _{OL} = 20 μA | 6 | 0.1 | | | 0.1 | | 0.1 | | V |
| | Low level output voltage | I _{OL} = 4 mA | 4.5 | 0.26 | | | 0.33 | | 0.4 | | V |
| | | I _{OL} = 5.2 mA | 6 | 0.26 | | | 0.33 | | 0.4 | | V |
| | | | | | | | | | | | |
| I _I | Input leakage current | V _I = V _{CC} or GND | 6 | ±0.1 | | | ±1 | | ±1 | | μA |
| I _{CC} | Supply current | V _I = V _{CC} or GND | 6 | 8 | | | 80 | | 160 | | μA |
| HCT TYPES | | | | | | | | | | | |
| V _{IH} | High level input voltage | | 4.5 to 5.5 | 2 | | | 2 | | 2 | | V |
| V _{IL} | Low level input voltage | | 4.5 to 5.5 | 0.8 | | | 0.8 | | 0.8 | | V |
| V _{OH} | High level output voltage | I _{OH} = − 20 μA | 4.5 | 4.4 | | | 4.4 | | 4.4 | | V |
| | High level output voltage | I _{OH} = − 4 mA | 4.5 | 3.98 | | | 3.84 | | 3.7 | | V |
| V _{OL} | Low level output voltage | I _{OL} = 20 μA | 4.5 | 0.1 | | | 0.1 | | 0.1 | | V |
| | Low level output voltage | I _{OL} = 4 mA | 4.5 | 0.26 | | | 0.33 | | 0.4 | | V |
| I _I | Input leakage current | V _I = V _{CC} or GND | 5.5 | ±0.1 | | | ±1 | | ±1 | | μA |
| I _{CC} | Supply current | V _I = V _{CC} or GND | 5.5 | 8 | | | 80 | | 160 | | μA |
| ΔI _{CC} ⁽¹⁾ | Additional quiescent device current per input pin | SER, A to H inputs held at V _{CC} − 2.1 | 4.5 to 5.5 | 100 126 | | | 157.5 | | 171.5 | | μA |
| | | CLK and SH/ŁD inputs held at V _{CC} − 2.1 | 4.5 to 5.5 | 100 234 | | | 292.5 | | 318.5 | | |

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

(2) V_I = V_{IH} or V_{IL}.

5.5 Prerequisite for Switching Characteristics

| PARAMETER | | V _{CC} (V) | 25°C | | -40°C to 85°C | | -55°C to 125°C | | UNIT |
|-----------------------------------|----------------------------------------------------|---------------------|------|-----|---------------|-----|----------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{WL} , t _{WH} | CLK Pulse Width | 2 | 80 | | 100 | | 120 | | ns |
| | | 4.5 | 16 | | 20 | | 24 | | |
| | | 6 | 14 | | 17 | | 20 | | |
| t _{WL} | SH/ $\overline{\text{LD}}$ Pulse Width | 2 | 80 | | 100 | | 120 | | ns |
| | | 4.5 | 16 | | 20 | | 24 | | |
| | | 6 | 14 | | 17 | | 20 | | |
| t _{SU} | Set-up Time SER to CLK | 2 | 80 | | 100 | | 120 | | ns |
| | | 4.5 | 16 | | 20 | | 24 | | |
| | | 6 | 14 | | 17 | | 20 | | |
| t _{SU(L)} | CLK INH to CLK | 2 | 80 | | 100 | | 120 | | ns |
| | | 4.5 | 16 | | 20 | | 24 | | |
| | | 6 | 14 | | 17 | | 20 | | |
| t _{SU} | A-H to SH/ $\overline{\text{LD}}$ | 2 | 80 | | 100 | | 120 | | ns |
| | | 4.5 | 16 | | 20 | | 24 | | |
| | | 6 | 14 | | 17 | | 20 | | |
| t _H | Hold Time SER to CLK or CLK INH | 2 | 35 | | 45 | | 55 | | ns |
| | | 4.5 | 7 | | 9 | | 11 | | |
| | | 6 | 6 | | 8 | | 9 | | |
| t _H | CLK INH to CLK | 2 | 0 | | 0 | | 0 | | ns |
| | | 4.5 | 0 | | 0 | | 0 | | |
| | | 6 | 0 | | 0 | | 0 | | |
| t _{REC} | Recovery Time SH/ $\overline{\text{LD}}$ to CLK | 2 | 100 | | 125 | | 150 | | ns |
| | | 4.5 | 20 | | 25 | | 30 | | |
| | | 6 | 17 | | 21 | | 26 | | |
| f _{MAX} | Maximum Clock Pulse Frequency | 2 | 6 | | 5 | | 4 | | MHz |
| | | 4.5 | 30 | | 24 | | 20 | | |
| | | 6 | 35 | | 28 | | 24 | | |
| HCT TYPES | | | | | | | | | |
| t _{WL} , t _{WH} | CLK Pulse Width | 4.5 | 18 | | 23 | | 27 | | ns |
| t _{WL} | SH/ $\overline{\text{LD}}$ Pulse Width | 4.5 | 20 | | 25 | | 30 | | ns |
| t _{SU} | Set-up Time SER to CLK | 4.5 | 20 | | 25 | | 30 | | ns |
| t _{SU(L)} | CLK INH to CLK | 4.5 | 20 | | 25 | | 30 | | ns |
| t _{SU} | A-H to SH/ $\overline{\text{LD}}$ | 6 | 20 | | 25 | | 30 | | ns |
| t _H | Hold Time SER to CLK or CLK INH | 4.5 | 7 | | 9 | | 11 | | ns |
| t _S , t _H | CLK INH to CLK | 4.5 | 0 | | 0 | | 0 | | ns |
| t _{REC} | Recovery Time SH/ $\overline{\text{LD}}$ to CLK | 4.5 | 20 | | 25 | | 30 | | ns |
| f _{MAX} | Maximum Clock Pulse Frequency | 4.5 | 27 | | 22 | | 18 | | MHz |

5.6 Switching Characteristics

Input t_r , t_f = 6 ns. Unless otherwise specified, C_L = 50pF

| PARAMETER | | V _{CC} (V) | 25°C | | -40°C to 85°C | -55°C to 125°C | UNIT |
|-----------------|-----------------------------------------------------------|---------------------|-------------------|-----|---------------|----------------|------|
| | | | TYP | MAX | MAX | MAX | |
| HC TYPES | | | | | | | |
| t _{pd} | CLK or CLK INH to Q _H or \overline{Q}_H | 2 | | 165 | 205 | 250 | ns |
| | | 4.5 | 13 ⁽³⁾ | 33 | 41 | 50 | ns |
| | | 6 | | 28 | 35 | 43 | ns |
| | SH/ \overline{LD} to Q _H or \overline{Q}_H | 2 | | 175 | 220 | 265 | ns |
| | | 4.5 | 14 ⁽³⁾ | 35 | 44 | 53 | ns |
| | | 6 | | 30 | 37 | 45 | ns |
| | H to Q _H or \overline{Q}_H | 2 | | 150 | 190 | 225 | ns |
| | | 4.5 | 12 ⁽³⁾ | 30 | 38 | 45 | ns |
| | | 6 | | 26 | 33 | 38 | ns |
| t _t | Output Transition Times | 2 | | 75 | 95 | 110 | ns |
| | | 4.5 | | 15 | 19 | 22 | ns |
| | | 6 | | 13 | 16 | 19 | ns |
| C _{IN} | Input Capacitance | | | 10 | 10 | 10 | pF |
| C _{PD} | Power Dissipation Capacitance ^{(1) (2)} | 5 | 17 | | | | pF |
| HCT TYPES | | | | | | | |
| t _{pd} | CLK or CLK INH to Q _H or \overline{Q}_H | 4.5 | 17 ⁽³⁾ | 40 | 50 | 60 | ns |
| | SH/ \overline{LD} to Q _H or \overline{Q}_H | 4.5 | 17 ⁽³⁾ | 40 | 50 | 60 | ns |
| | H to Q _H or \overline{Q}_H | 4.5 | 14 ⁽³⁾ | 35 | 44 | 53 | ns |
| t _t | Output Transition Times | 4.5 | | 15 | 19 | 22 | ns |
| C _{IN} | Input Capacitance | | | 10 | 10 | 10 | pF |
| C _{PD} | Power Dissipation Capacitance ^{(1) (2)} | 5 | 24 | | | | pF |

(1) C_{PD} is used to determine the dynamic power consumption, per package.

(2) $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_o)$ where f_i = Input Frequency, f_o = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

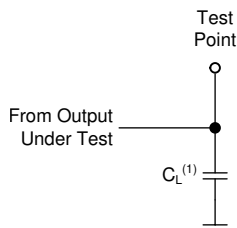
(3) C_L = 15 pF and V_{CC} = 5 V.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

For clock inputs, f_{\max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

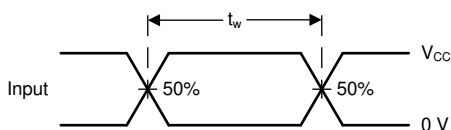


Figure 6-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

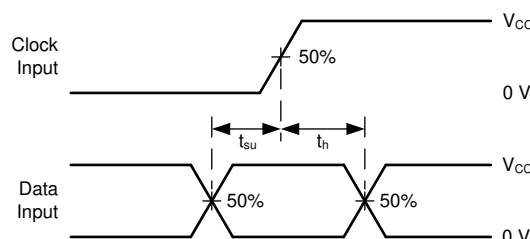
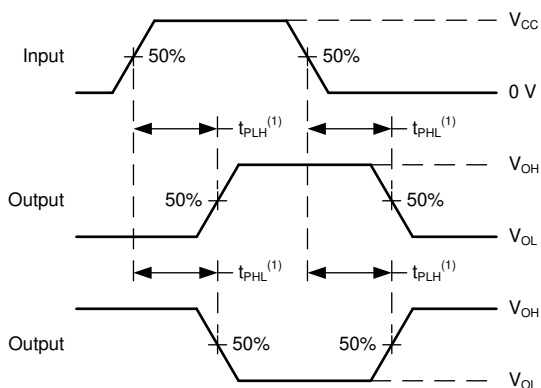
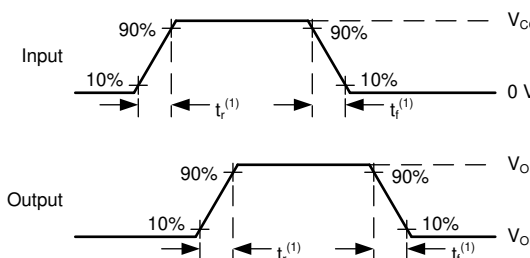


Figure 6-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-4. Voltage Waveforms, Standard CMOS Inputs Setup Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Input Devices

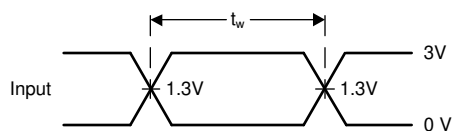


Figure 6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

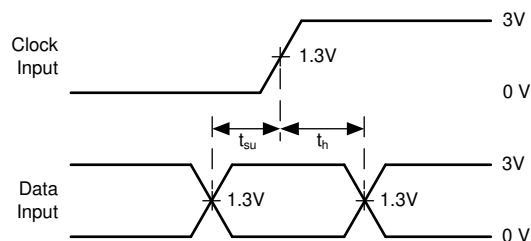
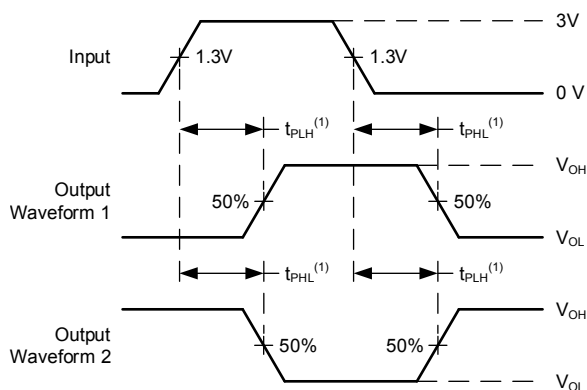


Figure 6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-8. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays

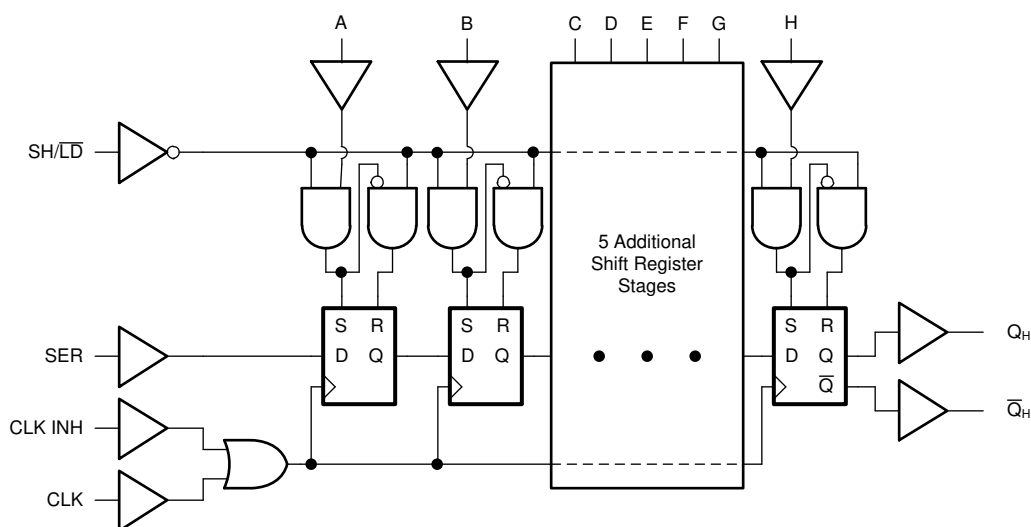
7 Detailed Description

7.1 Overview

The 'HC165 and 'HCT165 are 8-bit parallel or serial-in shift registers with complementary serial outputs (Q_H and \bar{Q}_H) available from the last stage. When the parallel load (SH/\bar{LD}) input is LOW, parallel data from the A to H inputs are loaded into the register asynchronously. When the SH/\bar{LD} is HIGH, data enters the register serially at the SER input and shifts one place to the right ($A \rightarrow B \rightarrow C$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by connecting the Q_H output to the SER input of the succeeding device.

For predictable operation the LOW-to-HIGH transition of CLK INH should only take place while CLK is HIGH. Also, CLK and CLK INH should be LOW before the LOW-to-HIGH transition of SH/\bar{LD} to prevent shifting the data when SH/\bar{LD} goes HIGH.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Truth Table⁽¹⁾

| OPERATING MODE | INPUTS | | | | | QnREGISTER | | OUTPUTS | |
|-------------------|--------|---------|-----|-----|-------|----------------|---------------------------------|----------------|-------------|
| | SH/LD | CLK INH | CLK | SER | A - H | Q _A | Q _B - Q _G | Q _H | \bar{Q}_H |
| Parallel Load | L | X | X | X | L | L | L-L | L | H |
| | L | X | X | X | H | H | H-H | H | L |
| Serial Shift | H | L | ↑ | l | X | L | q _A - q _F | q _G | \bar{q}_G |
| | H | L | ↑ | h | X | H | q _A - q _F | q _G | \bar{q}_G |
| Hold (Do Nothing) | H | H | X | X | X | q _A | q _B - q _G | q _H | \bar{q}_H |

- (1) H = High voltage level.
h = High voltage level one set-up time prior to the low-to-high clock transition.
l = Low voltage level one set-up time prior to the low-to-high clock transition.
L = Low voltage level.
X = Don't care.
↑ = Transition from low to high level.
q_n = Lower case letters indicate the state of the reference output clock transition.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------------|
| 5962-8685501EA | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8685501EA CD54HCT165F3A |
| CD54HC165F3A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8409501EA CD54HC165F3A |
| CD54HC165F3A.A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8409501EA CD54HC165F3A |
| CD54HCT165F3A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8685501EA CD54HCT165F3A |
| CD54HCT165F3A.A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8685501EA CD54HCT165F3A |
| CD74HC165E | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC165E |
| CD74HC165E.A | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC165E |
| CD74HC165M | Obsolete | Production | SOIC (D) 16 | - | - | Call TI | Call TI | -55 to 125 | HC165M |
| CD74HC165M96 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU SN NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC165M |
| CD74HC165M96.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC165M |
| CD74HC165MT | Obsolete | Production | SOIC (D) 16 | - | - | Call TI | Call TI | -55 to 125 | HC165M |
| CD74HCT165E | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT165E |
| CD74HCT165E.A | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT165E |
| CD74HCT165M | Obsolete | Production | SOIC (D) 16 | - | - | Call TI | Call TI | -55 to 125 | HCT165M |
| CD74HCT165M96 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -55 to 125 | HCT165M |
| CD74HCT165M96.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT165M |
| CD74HCT165M96G4 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT165M |
| CD74HCT165M96G4.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT165M |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54HC165, CD54HCT165, CD74HC165, CD74HCT165 :

- Catalog : [CD74HC165](#), [CD74HCT165](#)
- Military : [CD54HC165](#), [CD54HCT165](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

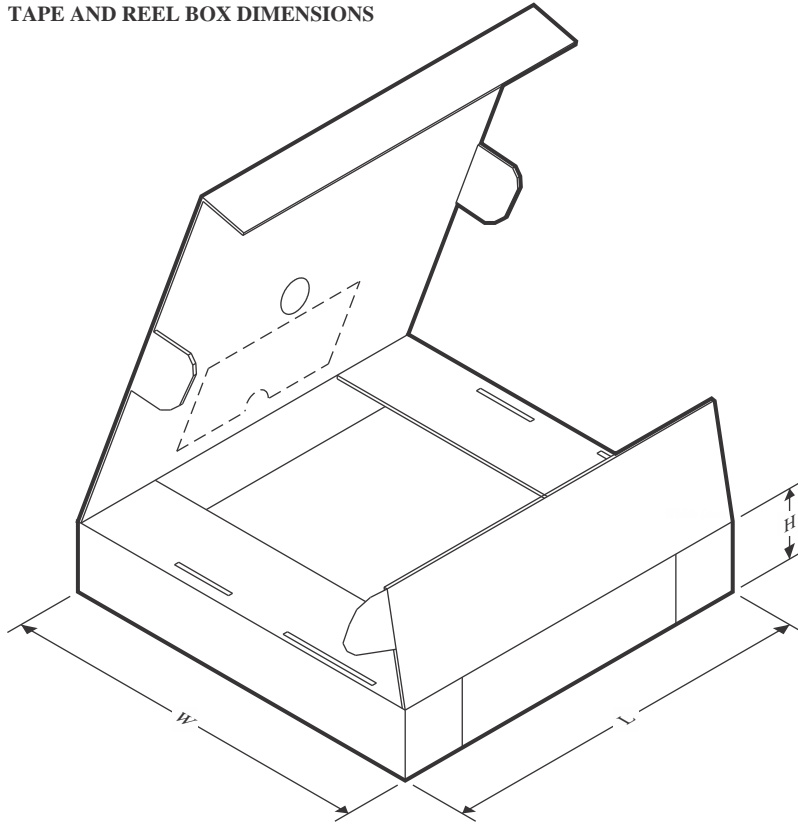
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC165M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC165M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT165M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT165M96G4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC165M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| CD74HC165M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| CD74HCT165M96 | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| CD74HCT165M96G4 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE

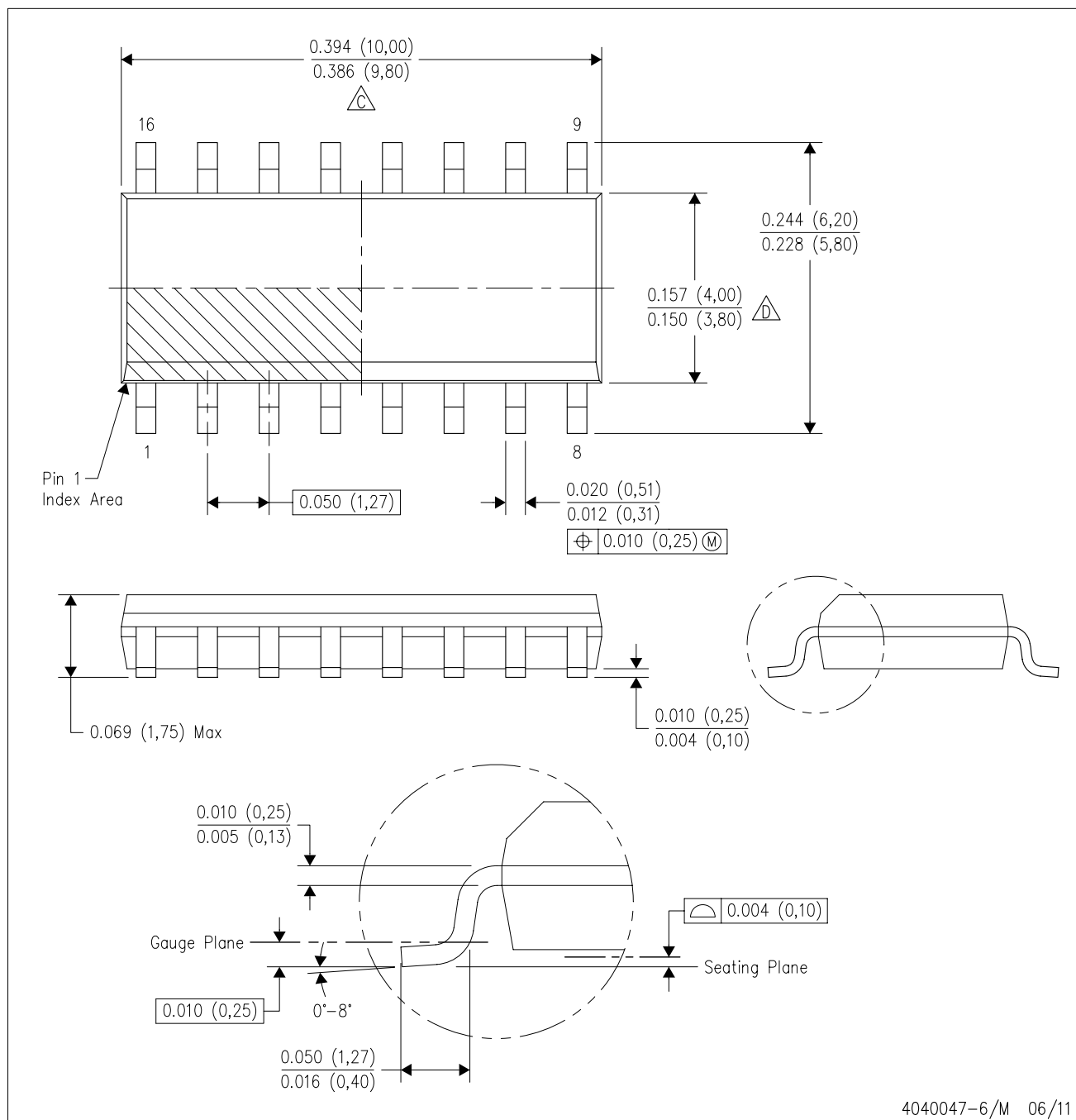


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC165E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC165E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC165E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC165E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT165E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT165E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT165E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT165E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



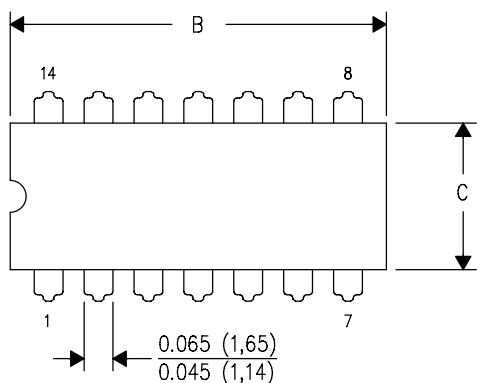
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

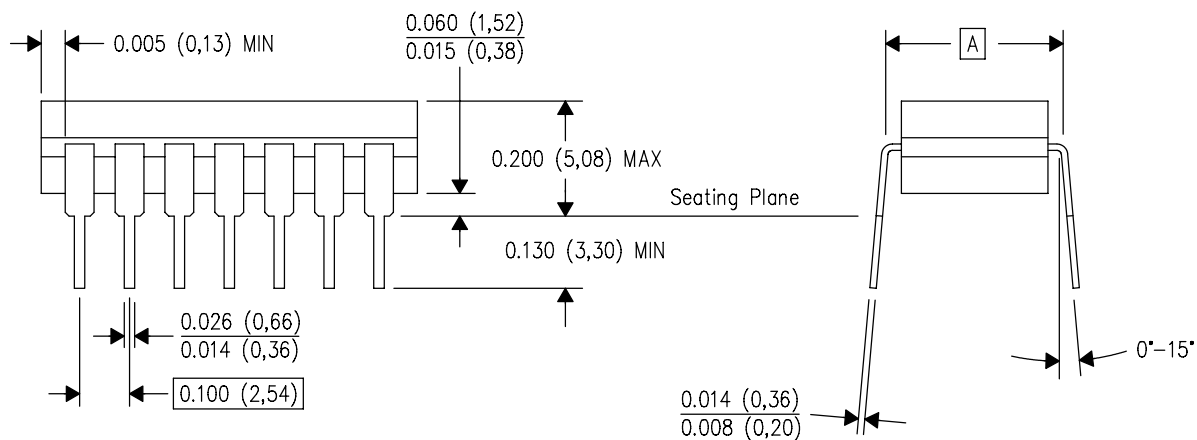
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



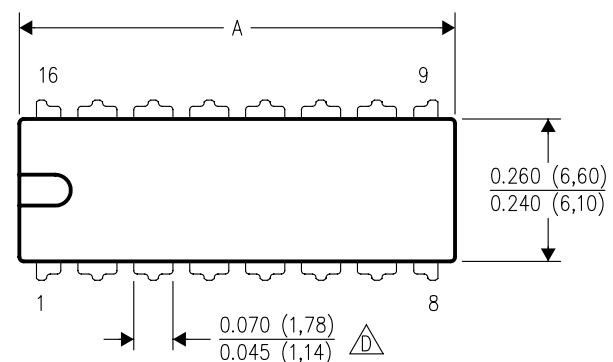
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

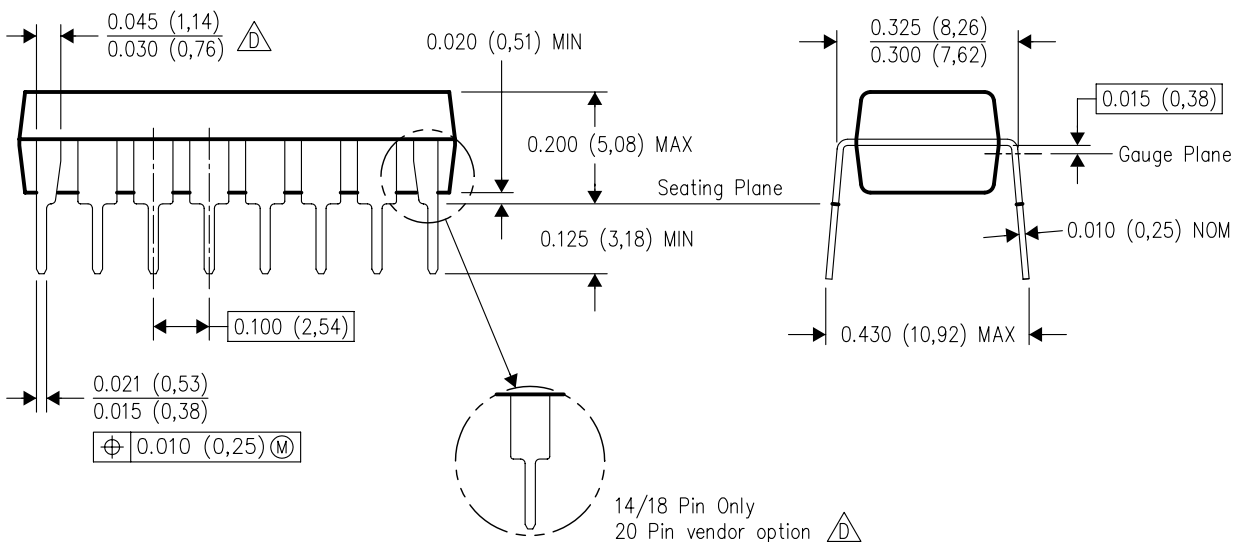
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE





| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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