# CDx4ACT74 Dual Positive-Edge-Triggered D-type Flip-flops with Clear and Preset

## 1 Features

- Inputs are TTL-voltage compatible
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Balanced propagation delays
- ±24mA output drive current
  - Fanout to 15 F devices
- SCR-latchup-resistant CMOS process and circuit design
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

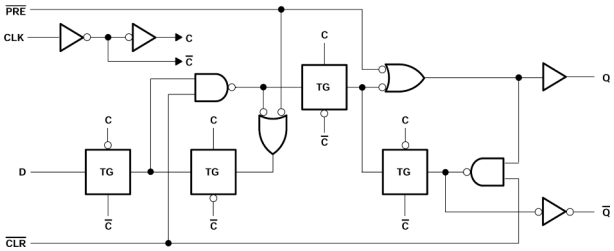
## 2 Description

The ’ACT74 dual positive-edge-triggered devices are D-type flip-flops.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| CDx4ACT74 | D (SOIC, 14) | 8.65mm × 6mm | 8.65mm × 3.9mm |
| | N (PDIP, 14) | 19.3mm × 9.4mm | 19.3mm × 6.35mm |
| | J (CDIP, 14) | 19.56mm x 7.9mm | 19.56mm × 6.67mm |

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram, Each Flip-flop (Positive Logic)**

# Table of Contents

## 3 Pin Configuration and Functions

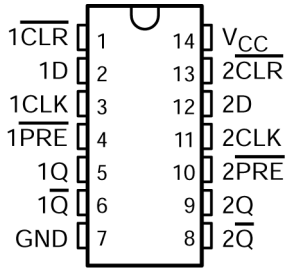



**Figure 3-1. D, N, or J Package**
**14-Pin SOIC, PDIP, or CDIP**
**(Top View)**

**Table 3-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1$\overline{CLR}$ | 1 | I | Asynchronous clear for channel 1, active low |
| 1D | 2 | I | Data for channel 1 |
| 1CLK | 3 | I | Clock for channel 1, rising edge triggered |
| 1$\overline{PRE}$ | 4 | I | Asynchronous preset for channel 1, active low |
| 1Q | 5 | O | Output for channel 1 |
| 1$\overline{Q}$ | 6 | O | Inverted output for channel 1 |
| GND | 7 | G | Ground |
| 2$\overline{Q}$ | 8 | O | Inverted output for channel 2 |
| 2Q | 9 | O | Output for channel 2 |
| 2$\overline{PRE}$ | 10 | I | Asynchronous preset for channel 2, active low |
| 2CLK | 11 | I | Clock for channel 2, rising edge triggered |
| 2D | 12 | I | Data for channel 2 |
| 2$\overline{CLR}$ | 13 | I | Asynchronous clear for channel 2, active low |
| $V_{CC}$ | 14 | P | Positive supply |

1. Signal Types: I = Input, O = Output, I/O = Input or Output.

# 4 Specifications

## 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range, | | –0.5 | 6 | V |
| $I_{IK}$ (2) | Input clamp current | ($V_I$ < 0 or $V_I$ > $V_{CC}$) | | ±20 | mA |
| $I_{OK}$ (2) | Output clamp current | ($V_O$ < 0 or $V_O$ > $V_{CC}$) | | ±50 | mA |
| $I_O$ | Continuous output current | ($V_O$ = 0 to $V_{CC}$) | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 4.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | $T_A$ = 25 °C | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | -24 | | -24 | | -24 | mA |
| $I_{OL}$ | Low-level output current | | 24 | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | | 10 | ns/V |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 4.4 Thermal Information

| THERMAL METRIC(1) | | CD74ACT74 | | UNIT |
|---|---|---|---|---|
| | | N (PDIP) | D (SOIC) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 80 | 119.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -50 µA | 4.5 V | 4.4 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = -24 mA | 4.5 V | 3.94 | | 3.7 | | 3.8 | | |
| | | $I_{OH}$ = -50 mA(1) | 5.5 V | | | 3.85 | | | | |
| | | $I_{OH}$ = -75 mA(1) | 5.5 V | | | | | 3.85 | | |
| $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 µA | 4.5 V | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 24 mA | 4.5 V | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 50 mA(1) | 5.5 V | | | | 1.65 | | | |
| | | $I_{OL}$ = 75 mA(1) | 5.5 V | | | | | | 1.65 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | | 5.5 V | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | 4 | | 80 | | 40 | µA |
| $\Delta I_{CC}$ (2) | $V_I$ = $V_{CC}$ - 2.1 V | | 4.5 V to 5.5 V | | 2.4 | | 3 | | 2.8 | mA |
| $C_i$ | | | | | 10 | | 10 | | 10 | pF |

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.
(2) Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

**Table 4-1. Act Input Load Table**

| INPUT | UNIT LOAD |
|---|---|
| Data | 0.53 |
| $\overline{PRE}$ or $\overline{CLR}$ | 0.58 |
| CLK | 1 |

## 4.6 Timing Requirements

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | 85 | | 97 | MHz |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 5 | | 4.4 | | ns |
| | | CLK | 5.7 | | 5 | | |
| $t_{su}$ | Setup time | Data | 4 | | 3.5 | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | | | | | ns |
| $t_h$ | Hold time | Data after CLK↑ | 0 | | 0 | | ns |
| $t_{rec}$ | Recovery time, before CLKT | $\overline{CL}$ R↑ or $\overline{PRE}$↑ | 2.7 | | 2.4 | | ns |

## 4.7 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 85 | | 97 | | MHz |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | 2.4 | 9.5 | 2.5 | 8.6 | ns |
| $t_{PHL}$ | | | 2.4 | 9.5 | 2.5 | 8.6 | |

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

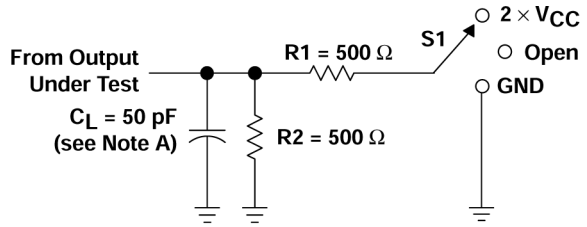
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 2.9 | 11.5 | 3 | 10.5 | ns |
| $t_{PHL}$ | | | 3.1 | 12.5 | 3.2 | 11.4 | |

## 4.8 Operating Characteristics

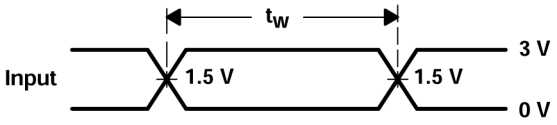
$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | TYP | UNIT |
|---|---|---|
| $C_{pd}$ Power dissipation capacitance | 55 | pF |

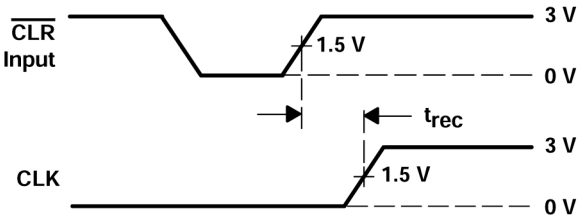
## 5 Parameter Measurement Information



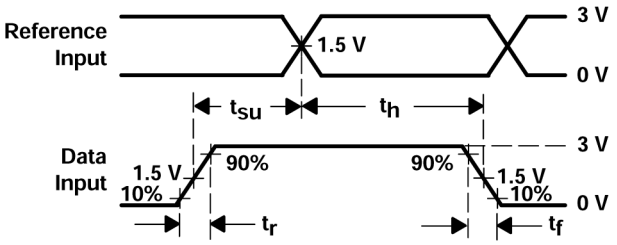

LOAD CIRCUIT



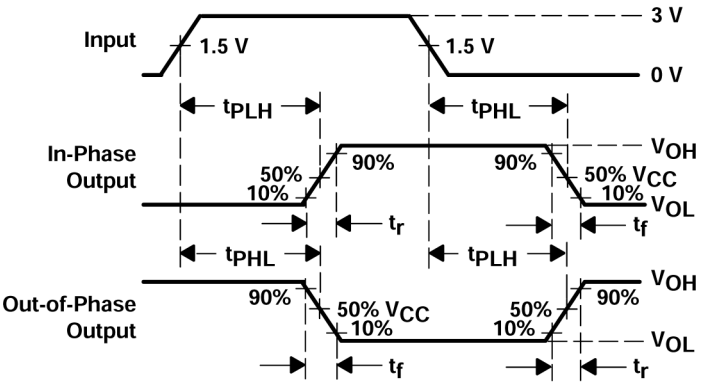

VOLTAGE WAVEFORMS
PULSE DURATION



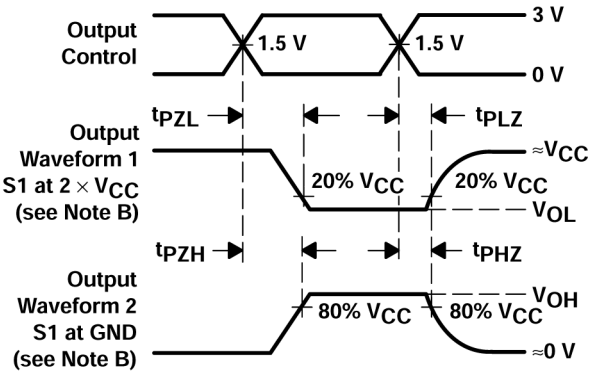

VOLTAGE WAVEFORMS
RECOVERY TIME




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES




VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, $f_{max}$ is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
G. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
H. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

**Figure 5-1. Load Circuit and Voltage Waveforms**

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |

| TEST | S1 |
|---|---|
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

# 6 Detailed Description

## 6.1 Overview

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

## 6.2 Functional Block Diagram

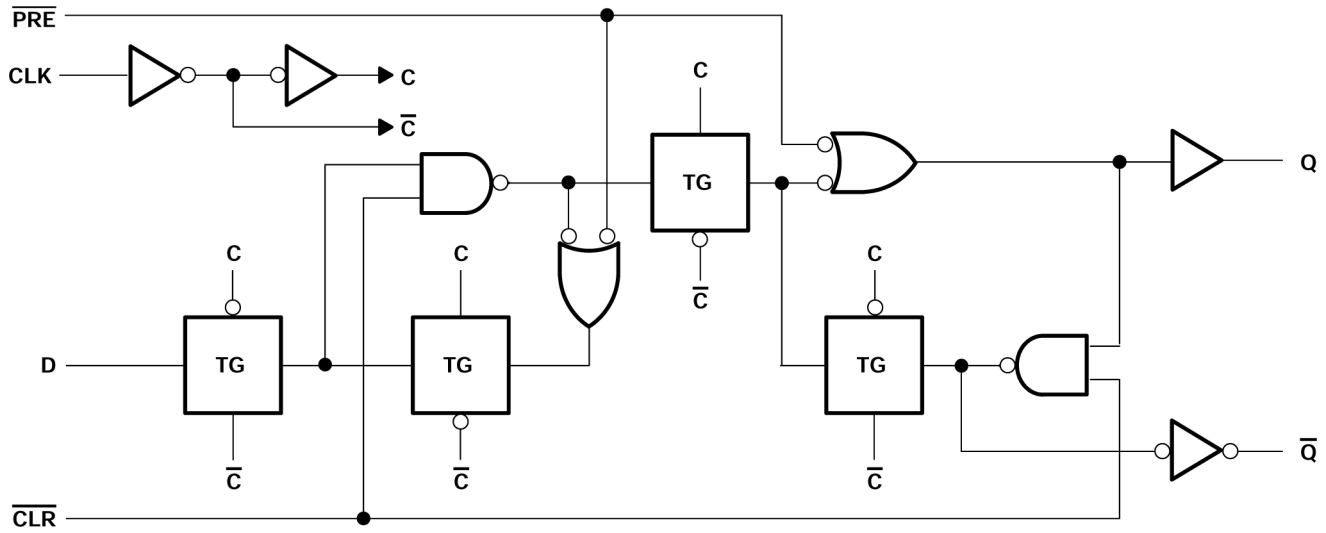



**Figure 6-1. Logic Diagram, Each Flip-flop (Positive Logic)**

## 6.3 Device Functional Modes

Function Table (Each Flip-Flop)

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H(1) | H(1) |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Section 4.3*. Each $V_{CC}$ terminal should have a bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 7.2 Layout

### *7.2.1 Layout Guidelines*

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

### *7.2.2 Layout Example*

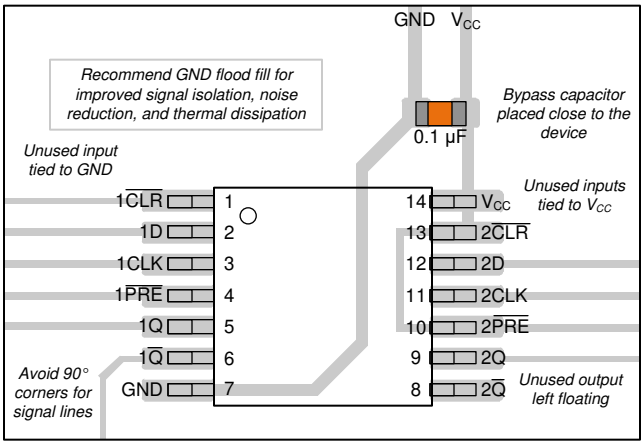



**Figure 7-1. Example layout for the CD74ACT74**

# 8 Device and Documentation Support

## 8.1 Documentation Support (Analog)

### *8.1.1 Related Links*

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| CD54ACT74 | Click here | Click here | Click here | Click here | Click here |
| CD74ACT74 | Click here | Click here | Click here | Click here | Click here |

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (December 2002) to Revision A (July 2024) | Page |
|---|---|
| • Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,*Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Updated RθJA values: D = 86 to 119.9, all values in °C/W | 4 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CD54ACT74F3A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54ACT74F3A |
| CD54ACT74F3A.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54ACT74F3A |
| CD74ACT74E | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74ACT74E |
| CD74ACT74E.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74ACT74E |
| CD74ACT74M | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | -55 to 125 | ACT74M |
| CD74ACT74M96 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT74M |
| CD74ACT74M96.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT74M |
| CD74ACT74M96G4.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT74M |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54ACT74, CD74ACT74 :**

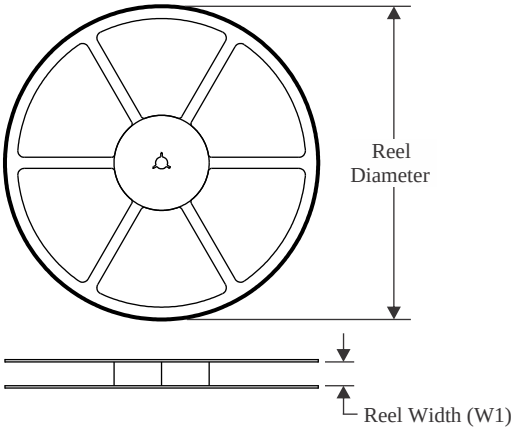
- Catalog : CD74ACT74
- Automotive : CD74ACT74-Q1, CD74ACT74-Q1
- Military : CD54ACT74

NOTE: Qualified Version Definitions:

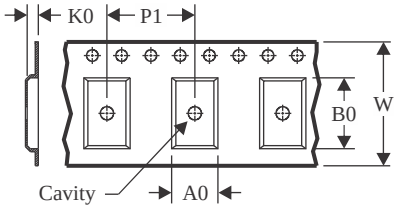
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

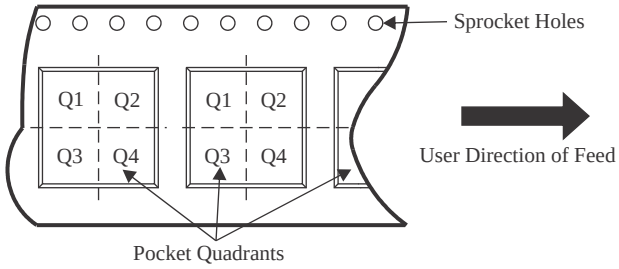



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

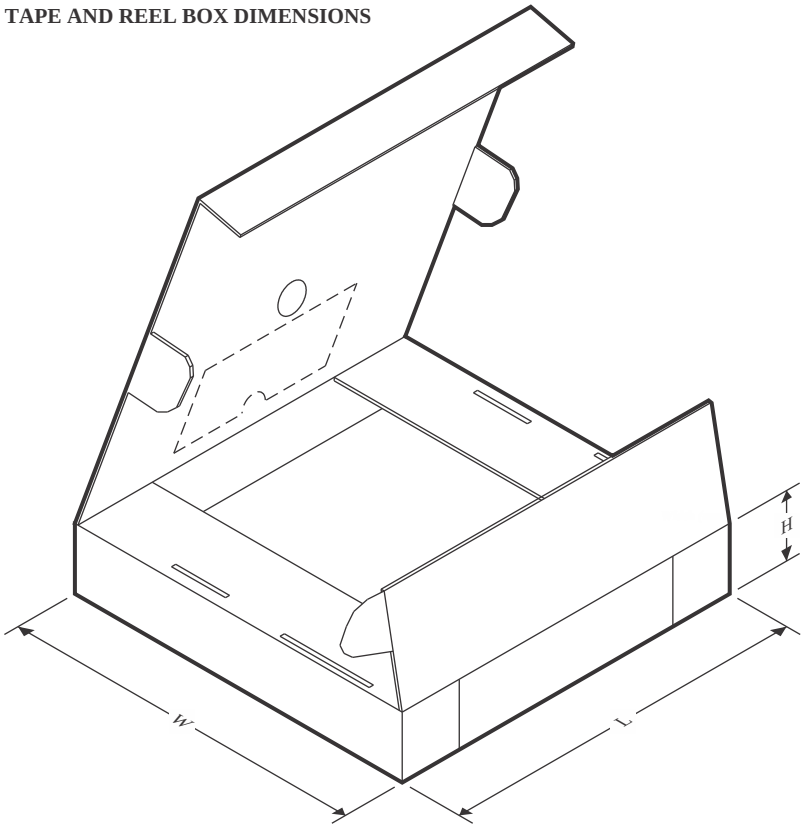
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74ACT74M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74ACT74M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

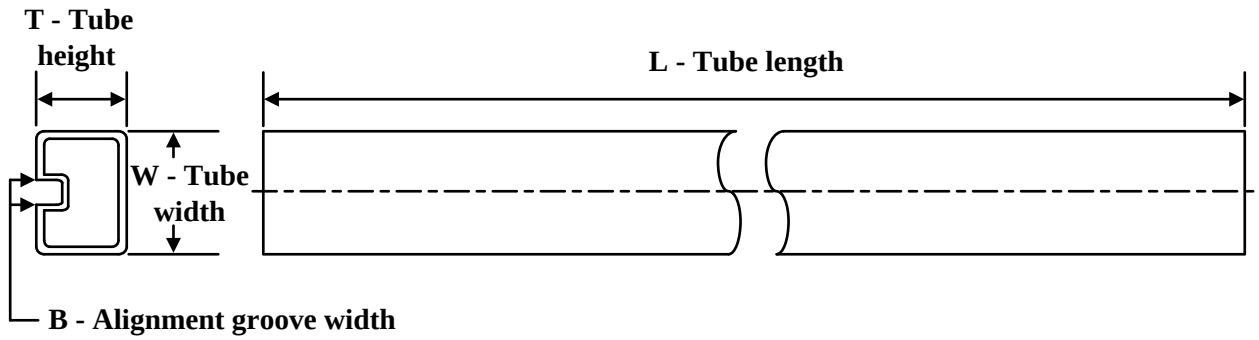
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74ACT74M96 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74ACT74M96 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |

## TUBE



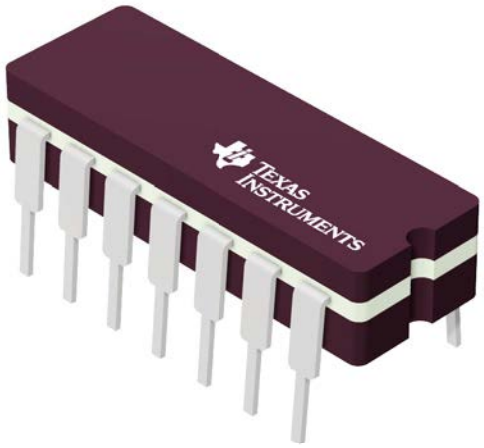

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74ACT74E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT74E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT74E.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT74E.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

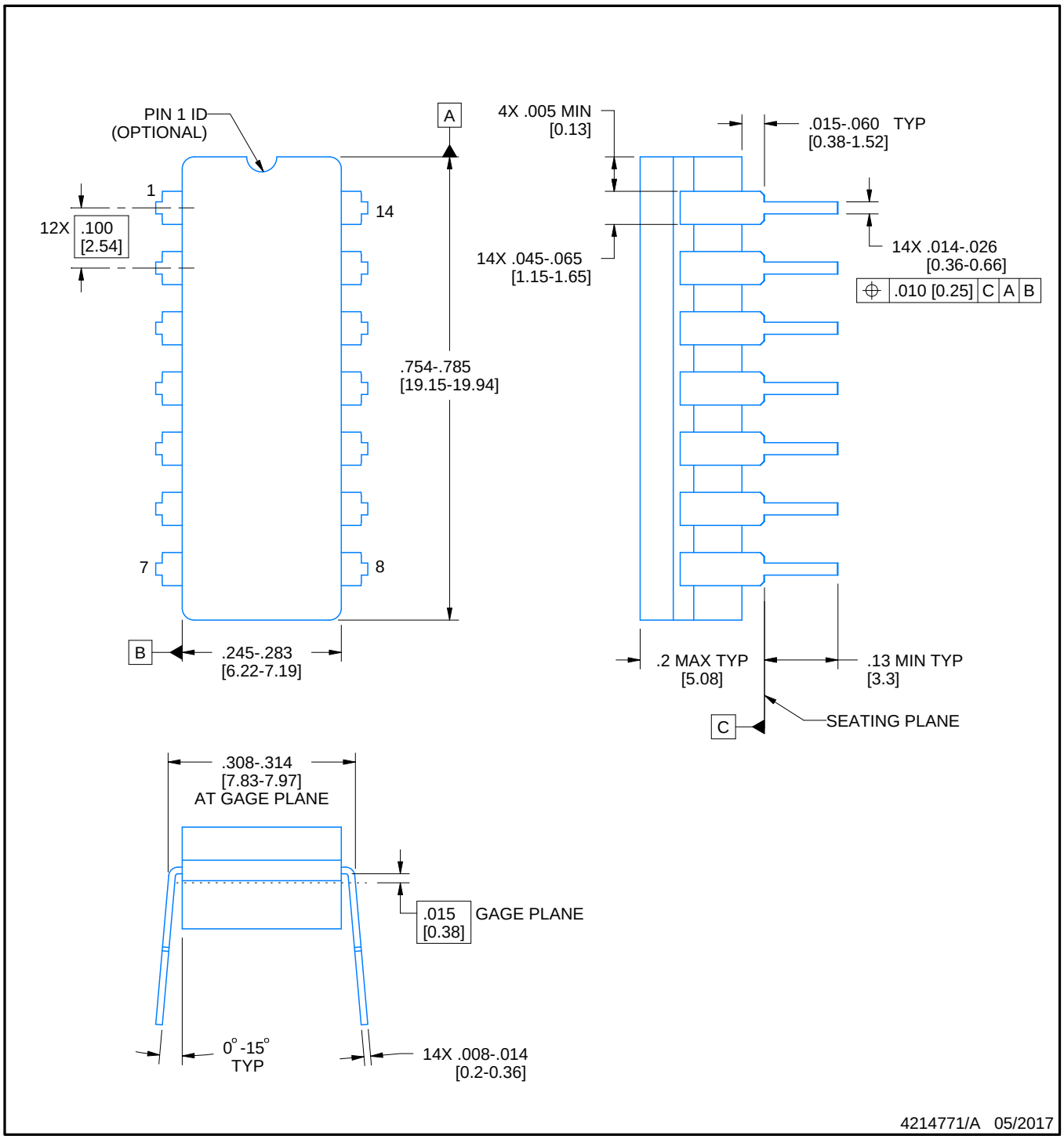
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

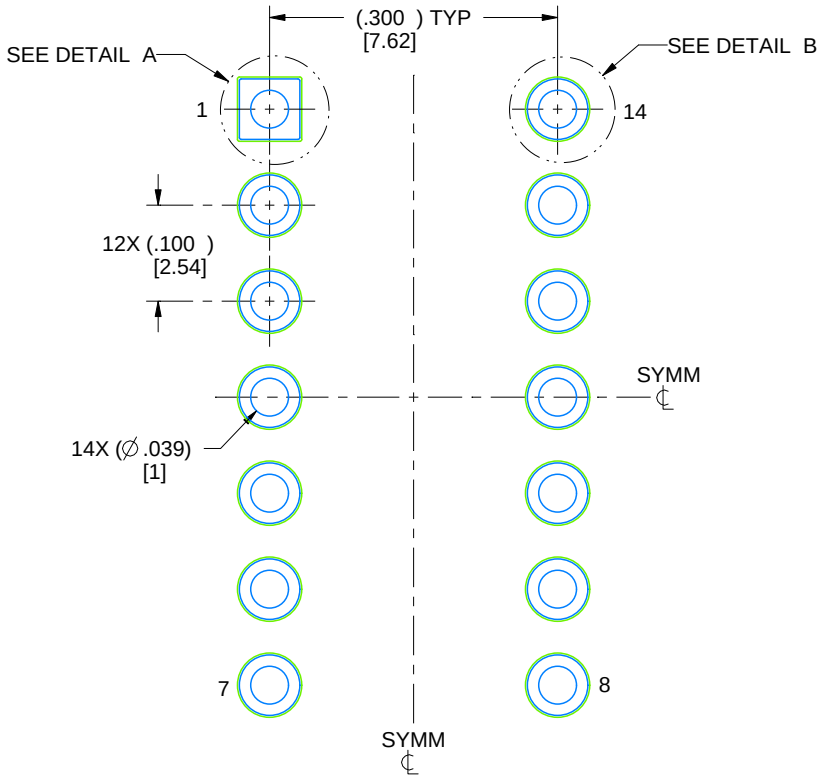
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

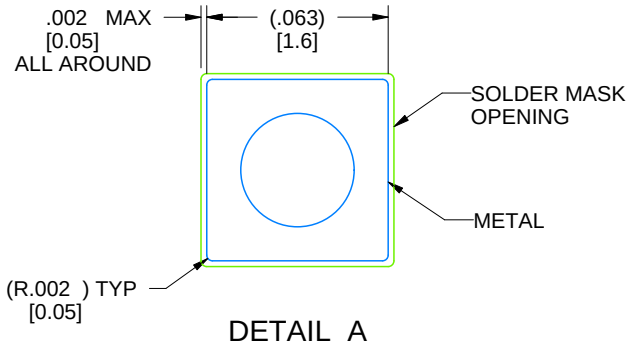
## J0014A

## CDIP - 5.08 mm max height

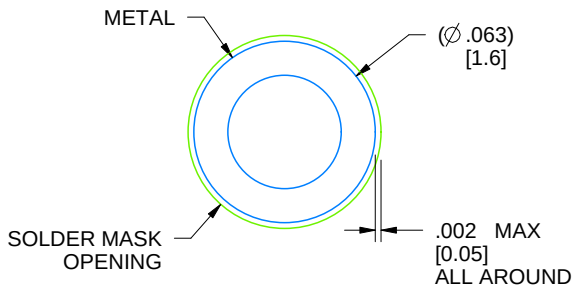
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X



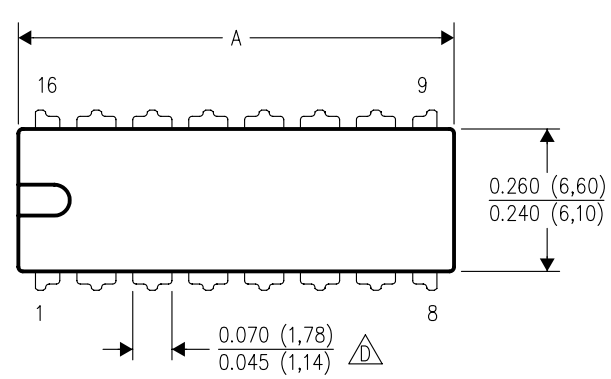

DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

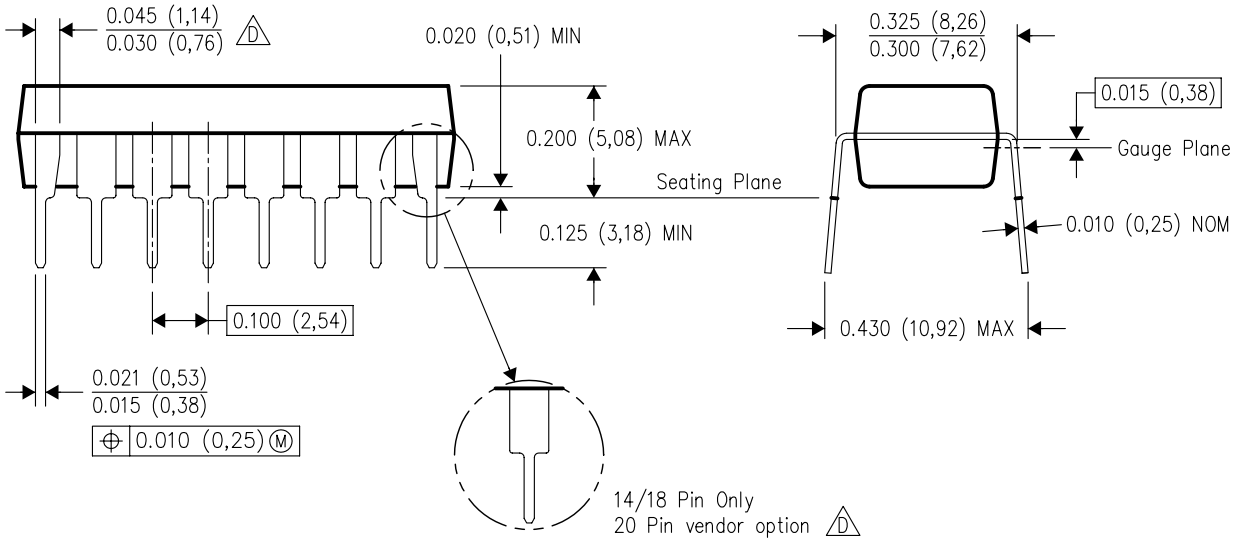
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

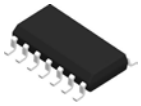



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

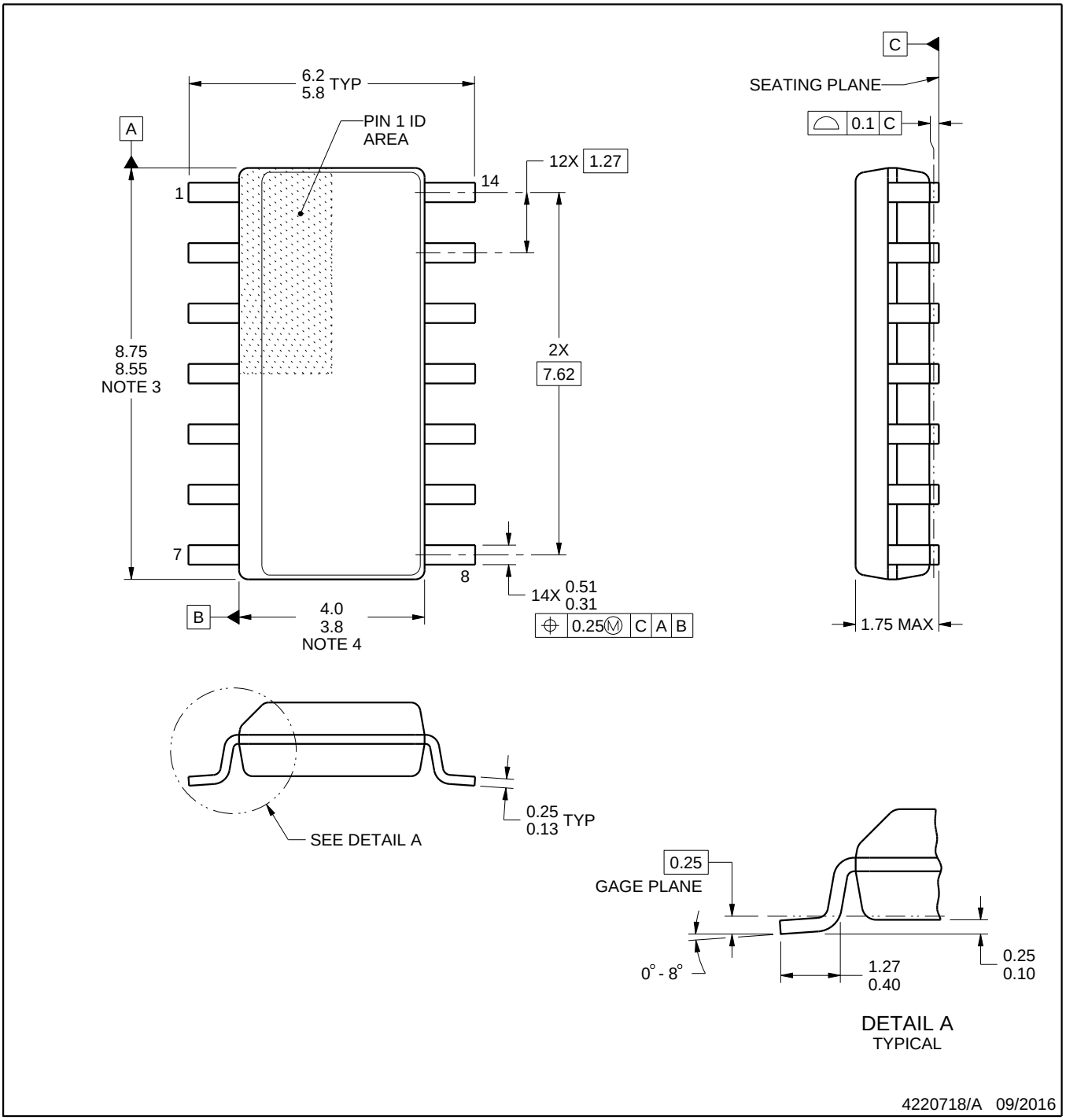


# PACKAGE OUTLINE

## D0014A

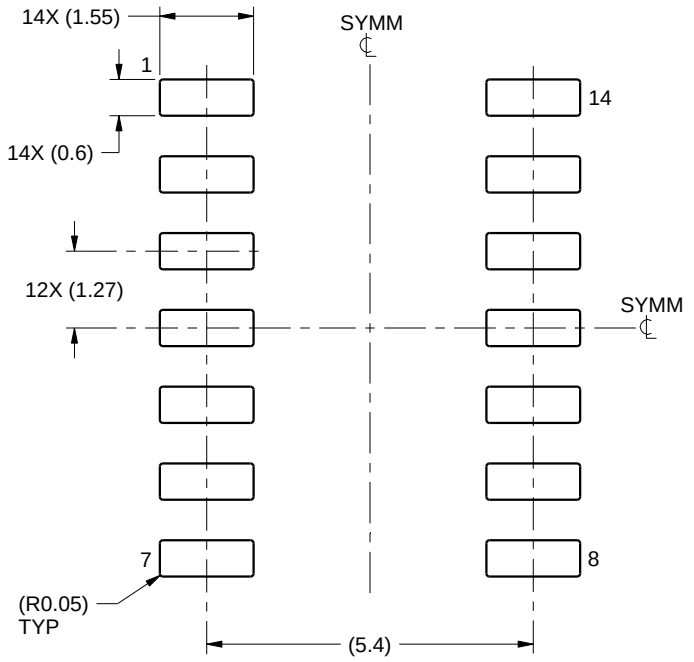
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

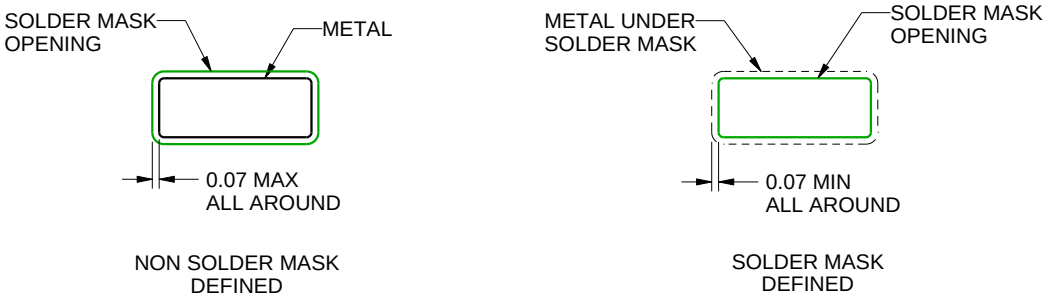



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

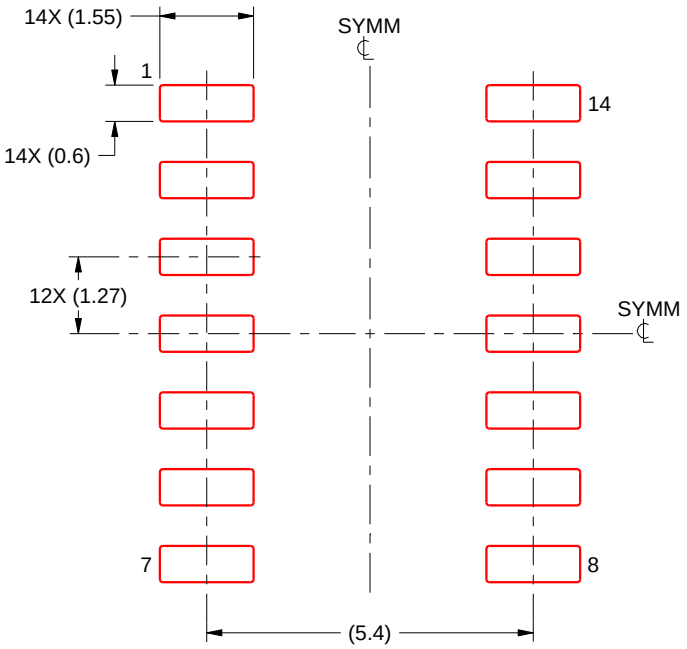
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265