CDx4AC164, CDx4ACT164 8-Bit Serial-In/Parallel-Out Shift Register

1 Features

- Buffered inputs
- Typical propagation delay
  - 6ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- SCR-latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST™/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- ±24mA output drive current
  - Fanout to 15 FAST™ ICs
  - Drives 50Ω transmission lines

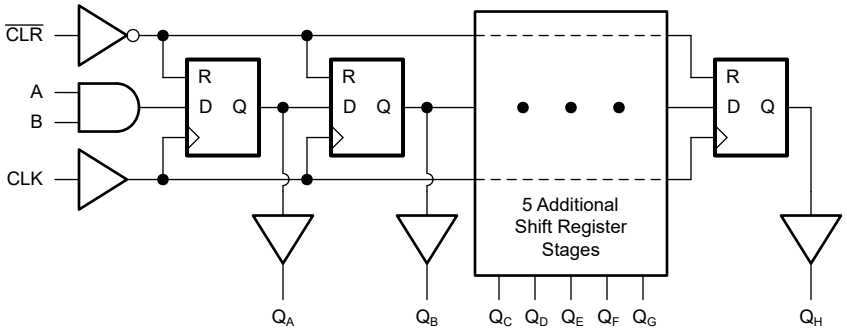
2 Description

The ’AC164 and ’ACT164 are 8-bit serial-in/parallel-out shift registers with asynchronous reset that utilize Advanced CMOS Logic technology.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
CDx4AC(T)164	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	N (PDIP, 14)	19.3mm x 9.4mm	19.3mm x 6.35mm
	PW (TSSOP, 14)	5mm x 6.4mm	5mm x 4.4mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Diagram

Table of Contents

3 Pin Configuration and Functions

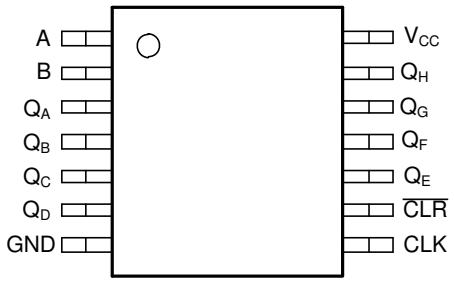


Figure 3-1. CD54AC(T)164 J Package; 14-Pin CDIP; CD74AC(T)164 D, N, or PW Package; 14-Pin SOIC, PDIP, or TSSOP (Top View)

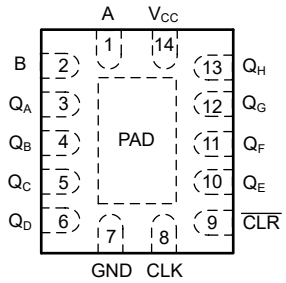


Figure 3-2. CD74AC(T)164 BQA Package; 14-Pin WQFN (Top View)

Table 3-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A	1	I	Gated serial input A
B	2	I	Gated serial input B
Q_A	3	O	Parallel output A
Q_B	4	O	Parallel output B
Q_C	5	O	Parallel output C
Q_D	6	O	Parallel output D
GND	7	G	Ground
CLK	8	I	Clock input, rising edge triggered
$\overline{CLR}$	9	I	Asynchronous register clear input, active low
Q_E	10	O	Parallel output E
Q_F	11	O	Parallel output F
Q_G	12	O	Parallel output G
Q_H	13	O	Parallel output H
V_{CC}	14	P	Positive supply
Thermal pad[2]		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

1. Signal Types: I = Input, O = Output, P = Power, G = Ground.
2. BQA package only.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	DC Supply Voltage		-0.5	6	V
I_{IK}	DC Input Diode Current	(V_I < -0.5V or V_I > V_{CC} + 0.5V)		± 20	mA
I_{OK}	DC Output Diode Current	(V_O < -0.5V or V_O > V_{CC} + 0.5V)		±50	mA
I_O	DC Output Source or Sink Current per Output Pin	(V_O > -0.5V or V_O < V_{CC} + 0.5V)		±50	mA
I_{CC} or I_{GND} (2)	DC V_{CC} or Ground Current			±100	mA

(1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
(2) For up to 4 outputs per device, add ±25mA for each additional output.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
T_A	Temperature Range		-55	125	°C
V_{CC} (1)	Supply Voltage Range				
	AC Types		1.5	5.5	V
	ACT Types		4.5	5.5	V
V_I, V_O	DC Input or Output Voltage		0	V_{CC}	V
dt/dv	Input Rise and Fall Slew Rate				
	AC Types	1.5V to 3V		50	ns
	AC Types	3.6V to 5.5V		20	ns
	ACT Types	4.5V to 5.5V		10	ns

(1) Unless otherwise specified, all voltages are referenced to ground.

4.4 Thermal Information

THERMAL METRIC(1)		CD74AC(T)164				UNIT
		BQA (WQFN)	D (SOIC)	N (PDIP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.3	106.6	90	148.0	°C/W

(1) θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

4.5 DC Electrical Specifications

PARAMETER		TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85 °C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
V_{IH}	High Level Input Voltage	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
V_{IL}	Low Level Input Voltage	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
V_{OH}	High Level Output Voltage	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (1) (2)	5.5	-	-	3.85	-	-	-	V
			-50 (1) (2)	5.5	-	-	-	-	3.85	-	V
V_{OL}	Low Level Output Voltage	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (1) (2)	5.5	-	-	-	1.65	-	-	V
			50(1) (2)	5.5	-	-	-	-	-	1.65	V
I_I	Input Leakage Current	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
I_{CC}	Quiescent Supply Current MSI	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA
ACT TYPES											
V_{IH}	High Level Input Voltage	-	-	4.5 to 5.5	2	-	2	-	2	-	V
V_{IL}	Low Level Input Voltage	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
V_{OH}	High Level Output Voltage	V_{IH} or V_{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75(1) (2)	5.5	-	-	3.85	-	-	-	V
			-50 (1) (2)	5.5	-	-	-	-	3.85	-	V
V_{OL}	Low Level Output Voltage	V_{IH} or V_{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (1) (2)	5.5	-	-	-	1.65	-	-	V
			50 (1) (2)	5.5	-	-	-	-	-	1.65	V
I_I	Input Leakage Current	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
I_{CC}	Quiescent Supply Current MSI	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA

PARAMETER		TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85 °C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC}	Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	V_{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

Table 4-1. ACT Input Load Table

INPUT	UNIT LOAD
A, B	0.5
$\overline{CLR}$	0.74
CLK	0.71

Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

4.6 Prerequisite for Switching Function

PARAMETER		V_{CC} (V)	-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	
	AC TYPES						
f_{MAX}	Max. Clock Frequency	1.5	7	-	6	-	MHz
		3.3(1)	62	-	54	-	MHz
		5(2)	86	-	75	-	MHz
t_W	$\overline{MR}$ Pulse Width	1.5	49	-	56	-	ns
		3.3	5.5	-	6.3	-	ns
		5	3.9	-	4.5	-	ns
t_W	CP Pulse Width	1.5	73	-	84	-	ns
		3.3	8.2	-	9.4	-	ns
		5	5.9	-	6.7	-	ns
t_{SU}	Set-up Time	1.5	27	-	31	-	ns
		3.3	3.1	-	3.5	-	ns
		5	2.2	-	2.5	-	ns
t_H	Hold Time	1.5	27	-	31	-	ns
		3.3	3.1	-	3.5	-	ns
		5	2.2	-	2.5	-	ns
t_{REM}	$\overline{MR}$ to CP Removal Time	1.5	1	-	1	-	ns
		3.3	1	-	1	-	ns
		5	1	-	1	-	ns
	ACT TYPES						
f_{MAX}	Max. Clock Frequency	5(2)	80	-	70	-	MHz
t_W	$\overline{MR}$ Pulse Width	5	3.9	-	4.5	-	ns
t_W	CP Pulse Width	5	6.2	-	7.1	-	ns
t_{SU}	Set-up Time	5	2.2	-	2.5	-	ns
t_H	Hold Time	5	2.6	-	3	-	ns
t_{REM}	$\overline{MR}$ to CP Removal Time	5	0	-	0	-	ns

(1) 9. 3.3V Min at 3.6V, Max at 3V.
(2) 10. 5V Min at 5.5V, Max at 4.5V.

4.7 Switching Specifications

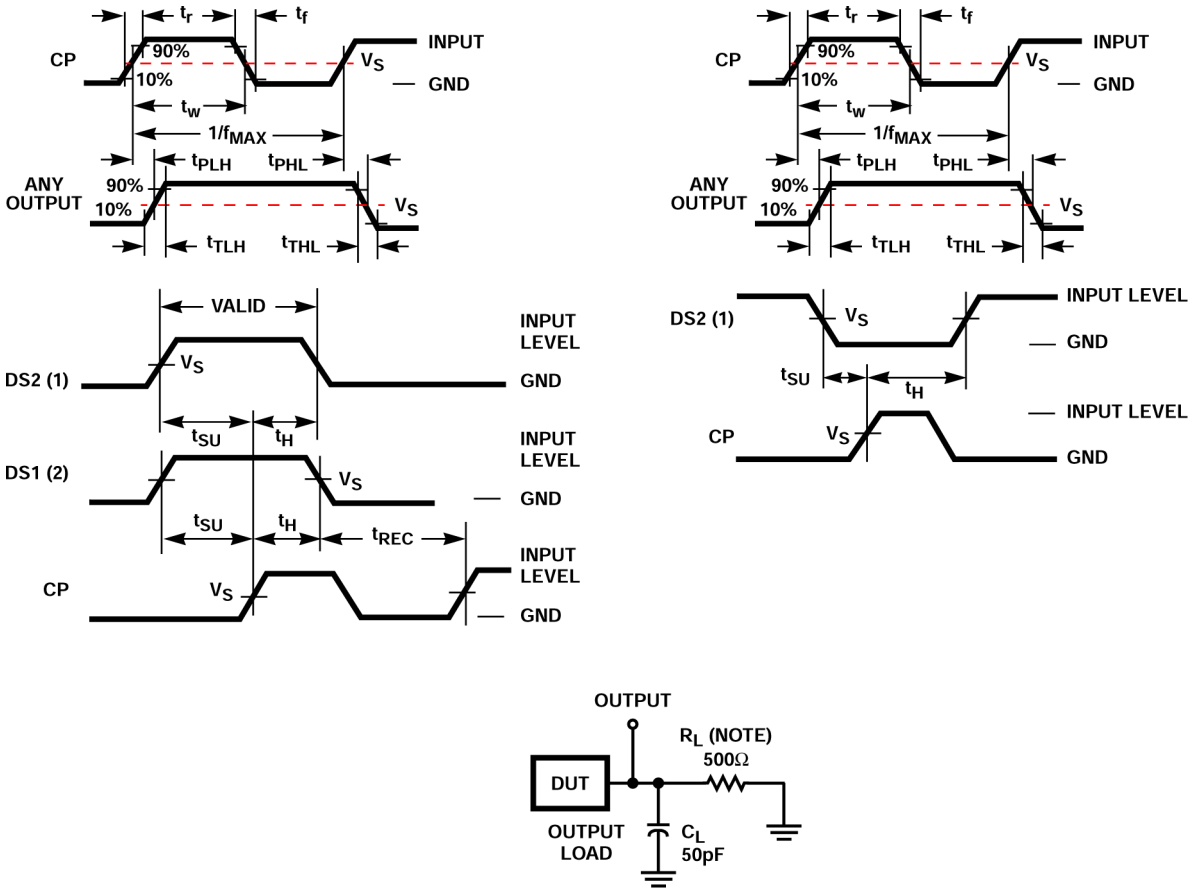
Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER		V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
t_{PLH}, t_{PHL}	Propagation Delay, CP to Qn	1.5	-	-	143	-	-	157	ns
		3.3 (1)	4.5	-	15.9	4.4	-	17.5	ns
		5 (2)	3.2	-	11.4	3.1	-	12.5	ns
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{MR}$ to Qn	1.5	-	-	158	-	-	174	ns
		3.3	5	-	17.7	4.9	-	19.5	ns
		5	3.6	-	12.6	3.5	-	13.9	ns
C_I	Input Capacitance	-	-	-	10	-	-	10	pF
C_{PD} (3)	Power Dissipation Capacitance	-	-	150	-	-	150	-	pF
ACT TYPES									
t_{PLH}, t_{PHL}	Propagation Delay, CP to Qn	5 (2)	3.8	-	13.5	3.7	-	14.9	ns
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{MR}$ to Qn	5	4.1	-	14.4	4	-	15.8	ns
C_I	Input Capacitance	-	-	-	10	-	-	10	pF
C_{PD} (3)	Power Dissipation Capacitance	-	-	150	-	-	150	-	pF

(1) 3.3V Min at 3.6V, Max at 3V.
(2) 5V Min at 5.5V, Max at 4.5V.
(3) C_{PD} is used to determine the dynamic power consumption per device.

5 Parameter Measurement Information

Load Circuit And Voltage Waveforms



For AC Series Only: When VCC = 1.5V, RL = 1kΩ.For AC Series Only: When VCC = 1.5V, RL = 1kΩ.For AC Series Only: When VCC = 1.5V, RL = 1kΩ.

Figure 5-1. Propagation Delay Times

Table 5-1. Propagation Delay Times

	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

6 Detailed Description

6.1 Overview

The CDx4AC(T)164 is an 8-bit shift register with 2 serial inputs (A and B) connected through an AND gate, as well as an asynchronous clear ($\overline{CLR}$). The device requires a high signal on both A and B to set the input data line high; a low signal on either input will set the input data line low. Data at A and B can be changed while CLK is high or low, provided that the minimum set-up time requirements are met.

The CLK pin of the CDx4AC(T)164 is rising-edge triggered, activating on the transition from LOW to HIGH. Upon a positive-edge trigger, the device will store the result of the (A ● B) input data line in the first register and propagate each register's data to the next register. The data of the last register, Q_H, will be discarded at each clock trigger. If a low signal is applied to the $\overline{CLR}$ pin, then the CDx4AC(T)164 will set all registers to a logical low value immediately.

6.2 Functional Block Diagram

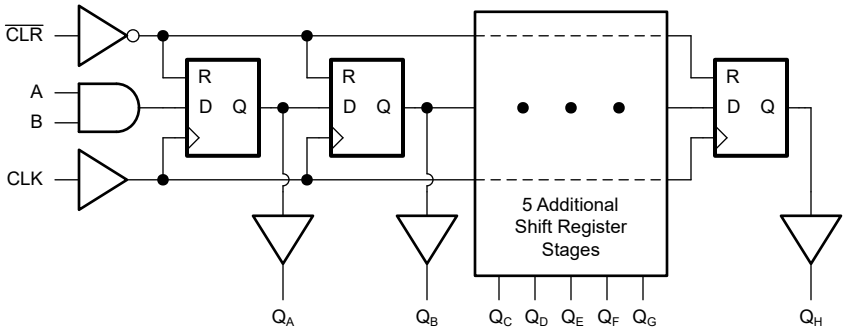


Figure 6-1. Logic Diagram (Positive Logic) for CDx4AC(T)164

6.3 Feature Description

6.3.1 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

6.3.2 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this

specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and typically will meet all requirements.

6.4 Device Functional Modes

Table 6-1 lists the functional modes of the CDx4AC(T)164.

Table 6-1. Function Table

INPUTS(1)				FUNCTION
A	B	$\overline{CLR}$	CLK	
X	X	L	X	Shift register is cleared.
L	X	H	↑	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
X	L	H	↑	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	H	H	↑	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

In this application, the CDx4AC(T)164 is used to control seven-segment displays. Unlike other I/O expanders, the CDx4AC(T)164 does not need a communication interface for control. It can easily operate with simple GPIO pins. Additional control is provided with two serial inputs that feed into an AND gate.

At power-up, the initial state of the shift registers is unknown. To give them a defined state, the shift register needs to be cleared. An RC can be connected to the $\overline{CLR}$ pin as shown in Figure 7-1 to initialize the shift register to all zeros.

7.2 Typical Application

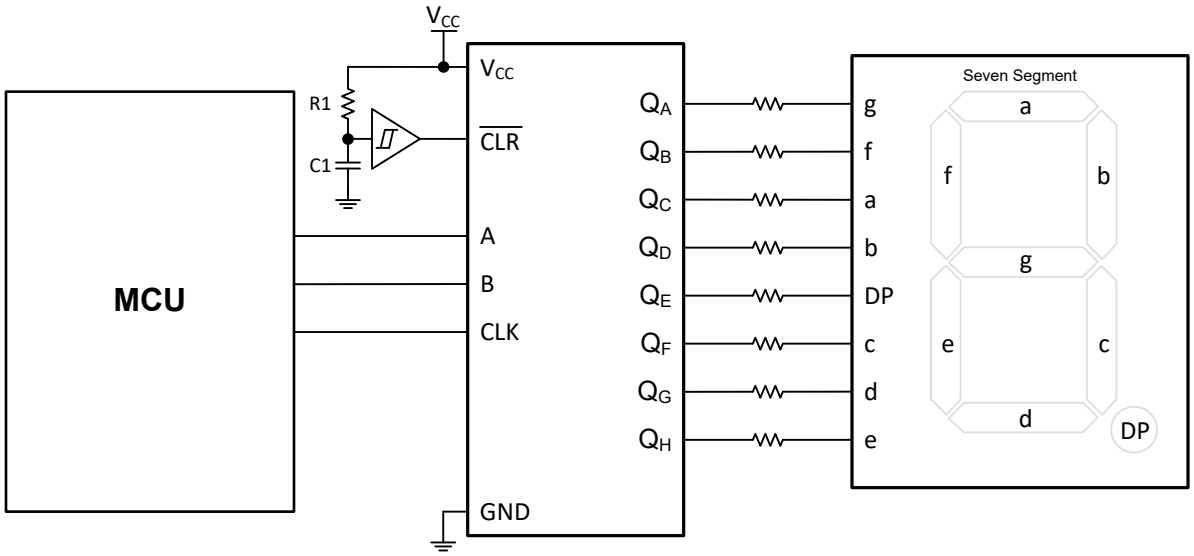


Figure 7-1. Typical Application Block Diagram

7.2.1 Design Requirements

7.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the CDx4AC(T)164 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The CDx4AC(T)164 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The CDx4AC(T)164 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

7.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the CDx4AC(T)164 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The CDx4AC(T)164 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

7.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

7.2.1.4 Application Curve

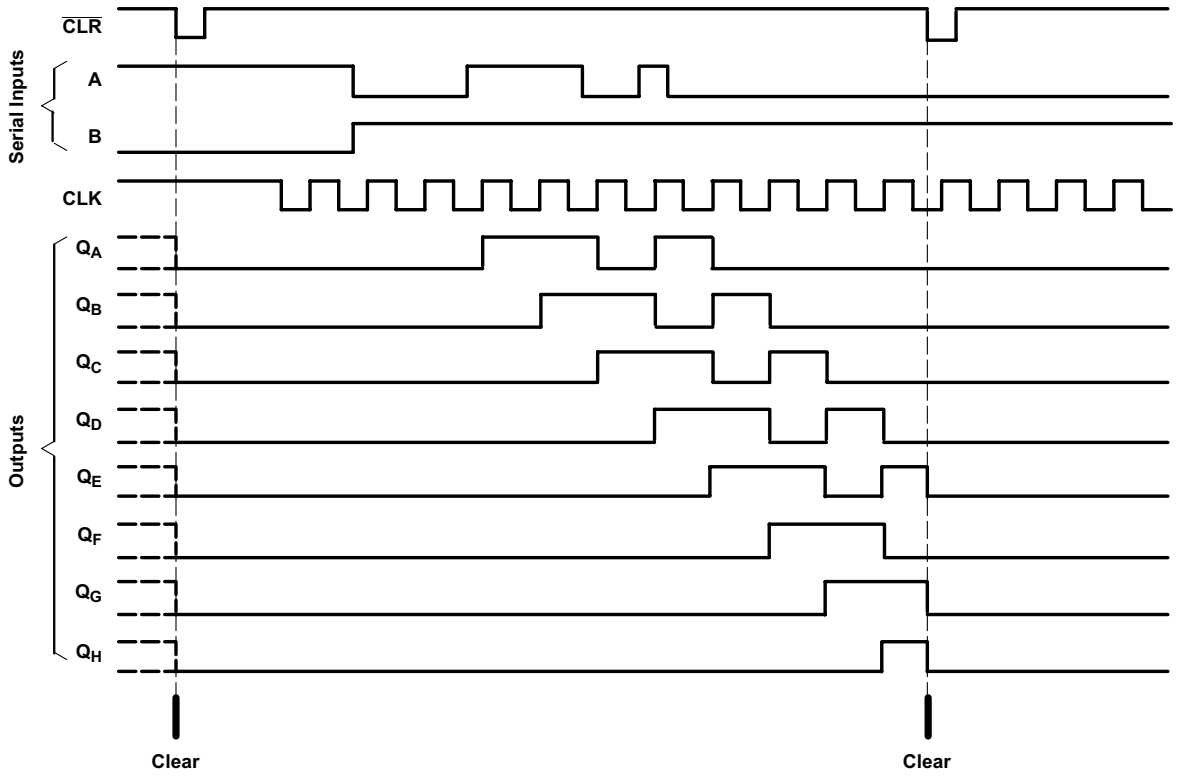


Figure 7-2. Application Timing Diagram

7.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent

power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.4 Layout

7.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

7.4.2 Layout Example

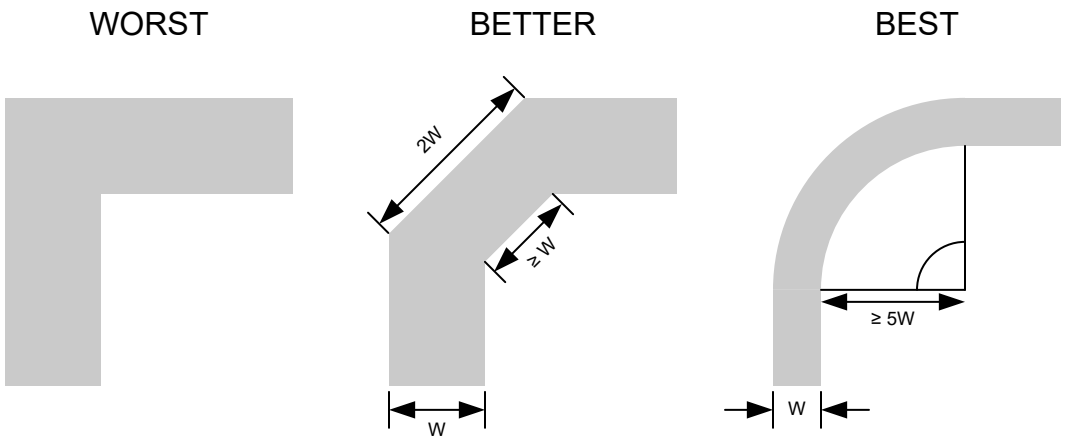


Figure 7-3. Example Trace Corners for Improved Signal Integrity

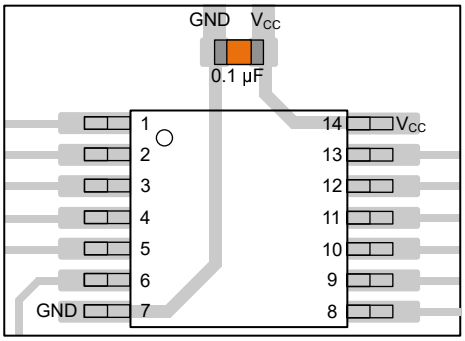


Figure 7-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

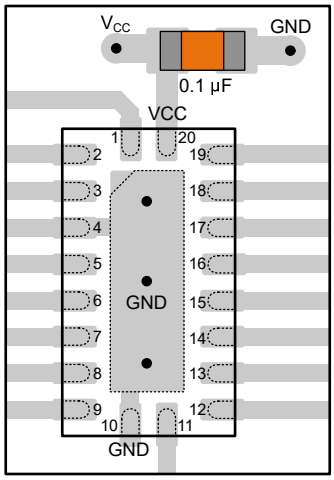


Figure 7-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

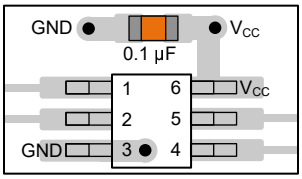


Figure 7-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

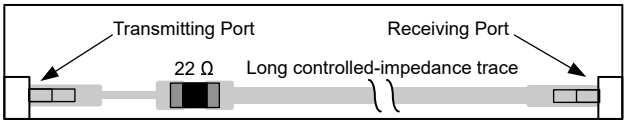


Figure 7-7. Example Damping Resistor Placement for Improved Signal Integrity

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC164	Click here	Click here	Click here	Click here	Click here
CD74AC164	Click here	Click here	Click here	Click here	Click here
CD54ACT164	Click here	Click here	Click here	Click here	Click here
CD74ACT164	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2024) to Revision D (October 2024) — **Page**

- Added BQA and PW packages to *Device Information* table, *Pin Configuration and Functions* section, and *Thermal Information* table....1
- Added *Feature Descriptions* section, *Typical Application* section, and *Layout Example* diagram....1

- Changed pin names throughout data sheet: DS1 → A, DS2 → B, Q0 → Q_A, Q1 → Q_B, Q2 → Q_C, Q3 → Q_D, CP → CLK, !MR → $\overline{CLR}$,, Q4 → Q_E, Q5 → Q_F, Q7 → Q_G, → Q_H, → V_{CC} 1

Changes from Revision B (November 2023) to Revision C (April 2024) **Page**

- Updated RθJA values: D = 175 to 106.6, all values in °C/W 4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54AC164F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC164F3A
CD54AC164F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC164F3A
CD54ACT164F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT164F3A
CD54ACT164F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT164F3A
CD74AC164BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC164
CD74AC164BQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC164
CD74AC164E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC164E
CD74AC164E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC164E
CD74AC164M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	AC164M
CD74AC164M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC164M
CD74AC164M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC164M
CD74AC164M96G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC164M
CD74AC164M96G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC164M
CD74AC164PWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	AC164
CD74AC164PWR.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC164
CD74ACT164BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AD164
CD74ACT164BQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AD164
CD74ACT164E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT164E
CD74ACT164E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT164E
CD74ACT164M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	ACT164M
CD74ACT164M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT164M
CD74ACT164M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT164M
CD74ACT164M96G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT164M
CD74ACT164M96G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT164M
CD74ACT164PWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	AD16
CD74ACT164PWR.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AD16

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54AC164, CD54ACT164, CD74AC164, CD74ACT164 :

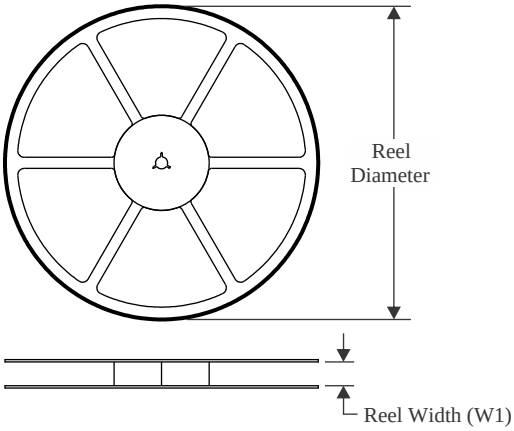
- Catalog : CD74AC164, CD74ACT164
- Military : CD54AC164, CD54ACT164

NOTE: Qualified Version Definitions:

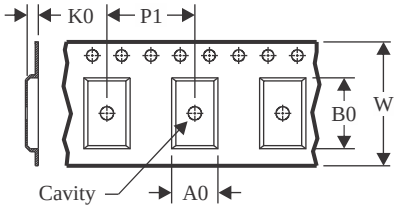
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

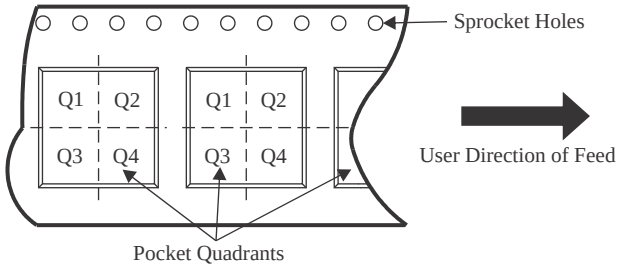


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

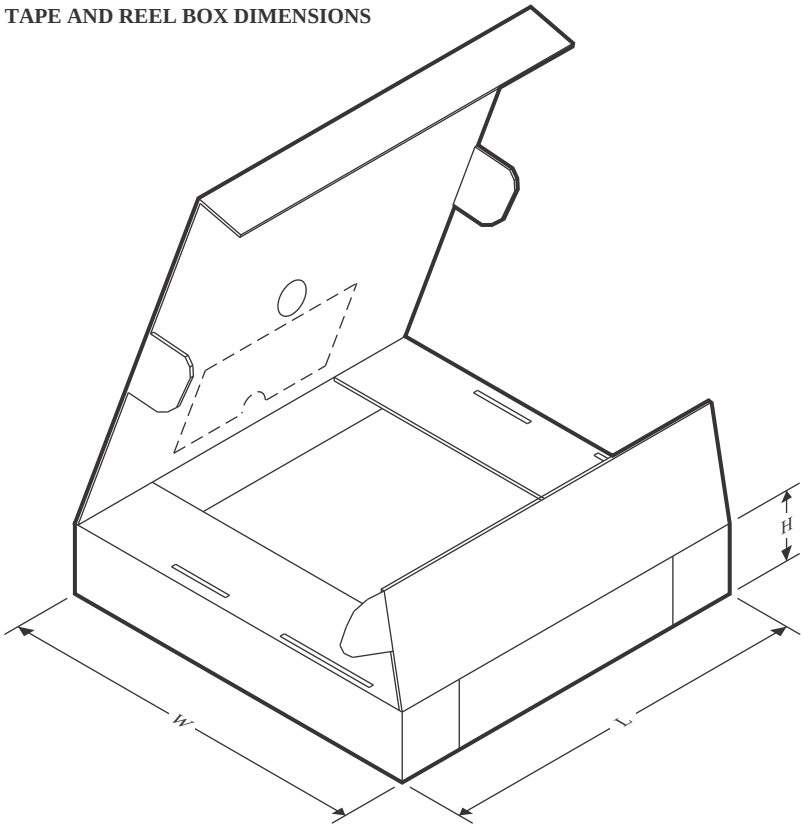
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC164BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
CD74AC164PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74AC164PWR	TSSOP	PW	14	3000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
CD74ACT164BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
CD74ACT164PWR	TSSOP	PW	14	3000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
CD74ACT164PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

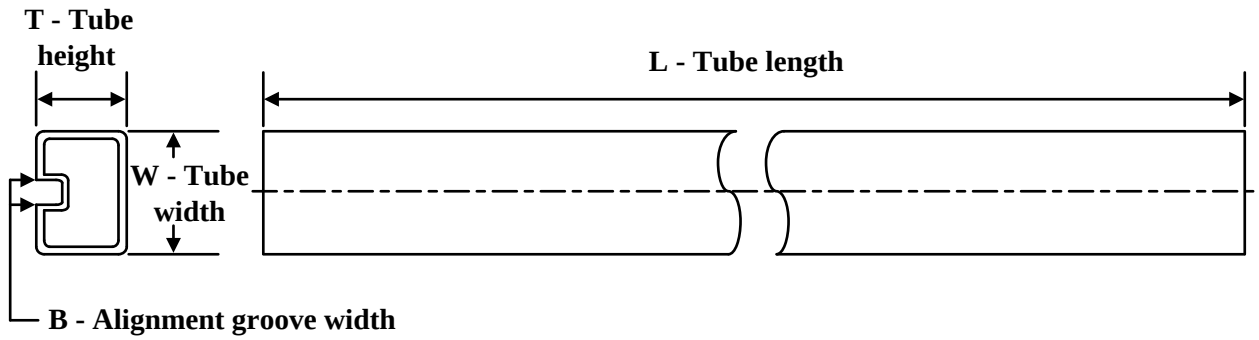
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

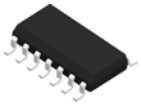
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC164BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
CD74AC164PWR	TSSOP	PW	14	3000	353.0	353.0	32.0
CD74AC164PWR	TSSOP	PW	14	3000	366.0	364.0	50.0
CD74ACT164BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
CD74ACT164PWR	TSSOP	PW	14	3000	366.0	364.0	50.0
CD74ACT164PWR	TSSOP	PW	14	3000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC164E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC164E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT164E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT164E.A	N	PDIP	14	25	506	13.97	11230	4.32

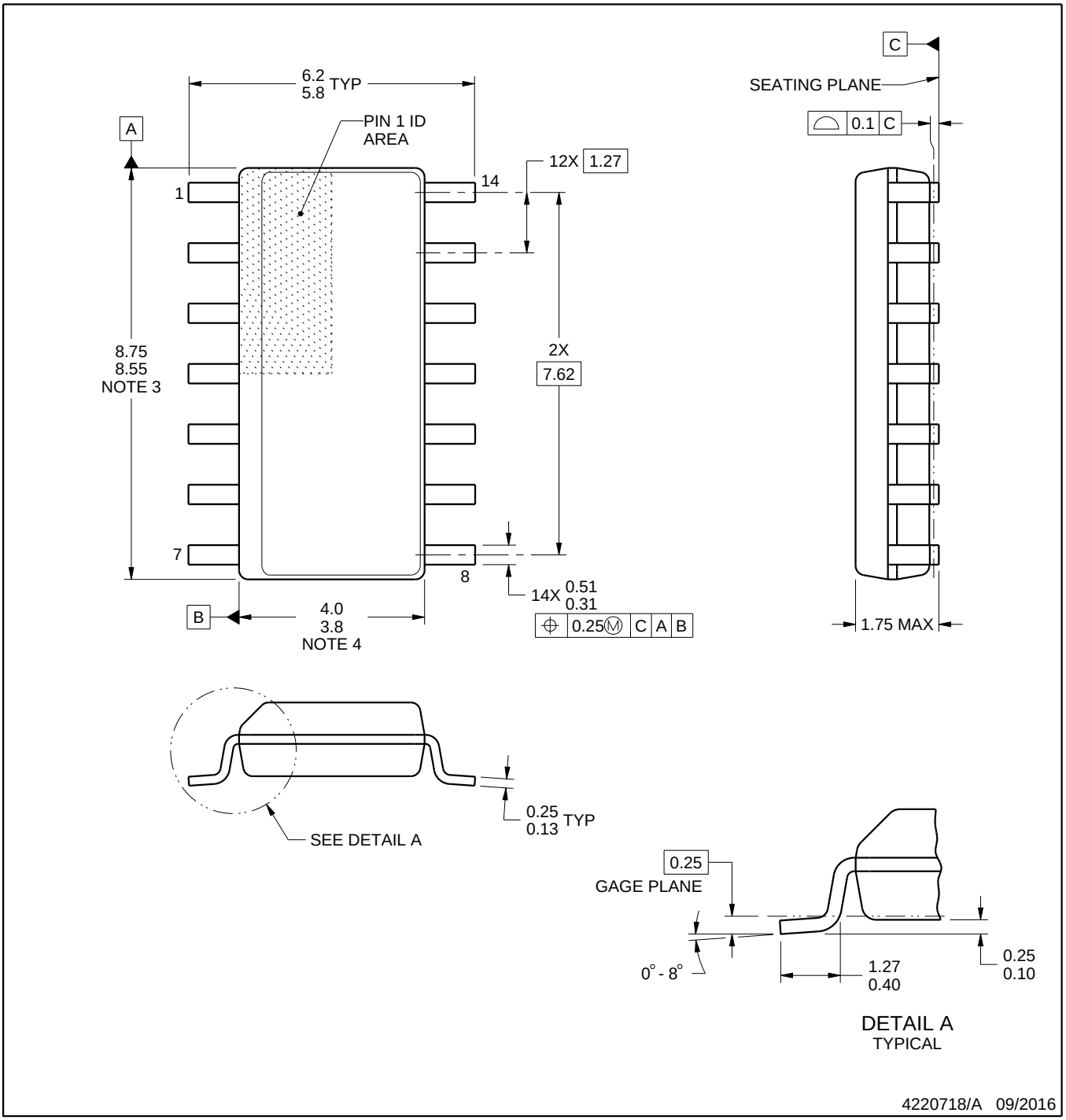


PACKAGE OUTLINE

D0014A

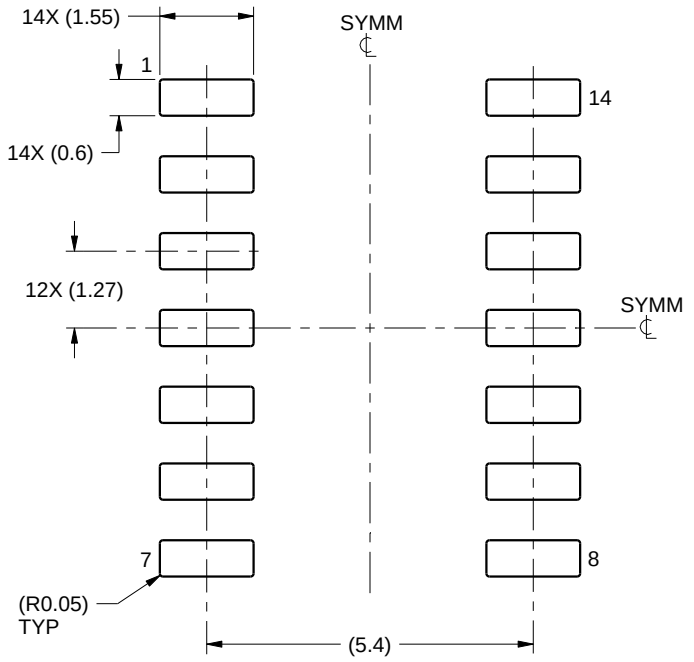
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

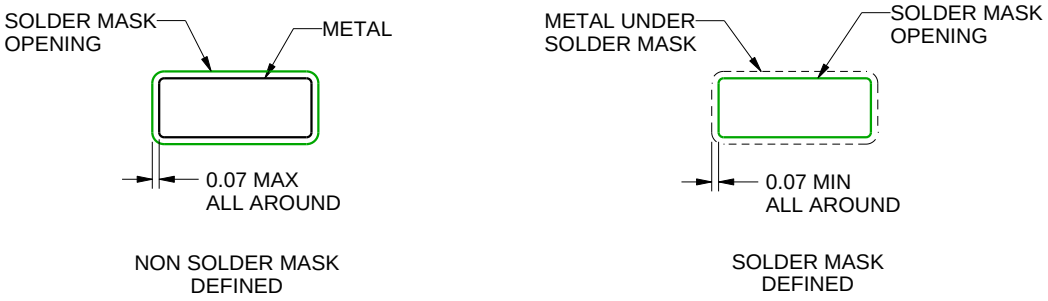


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

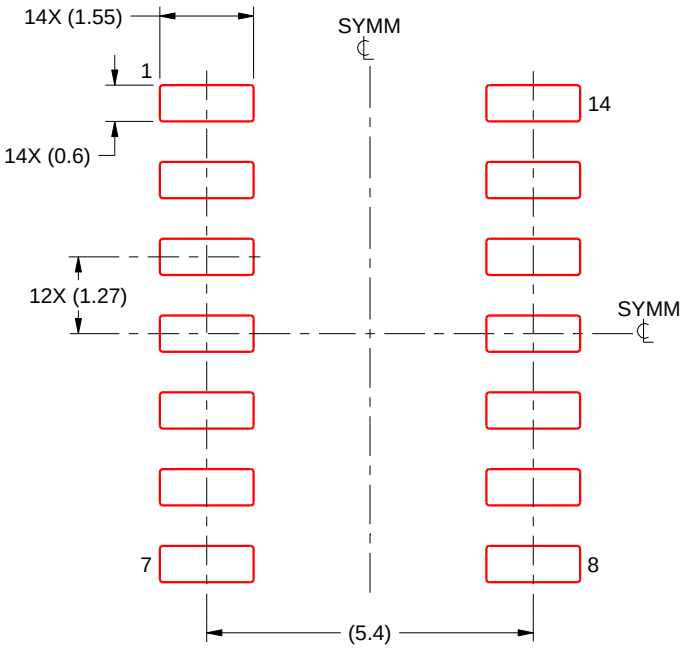
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

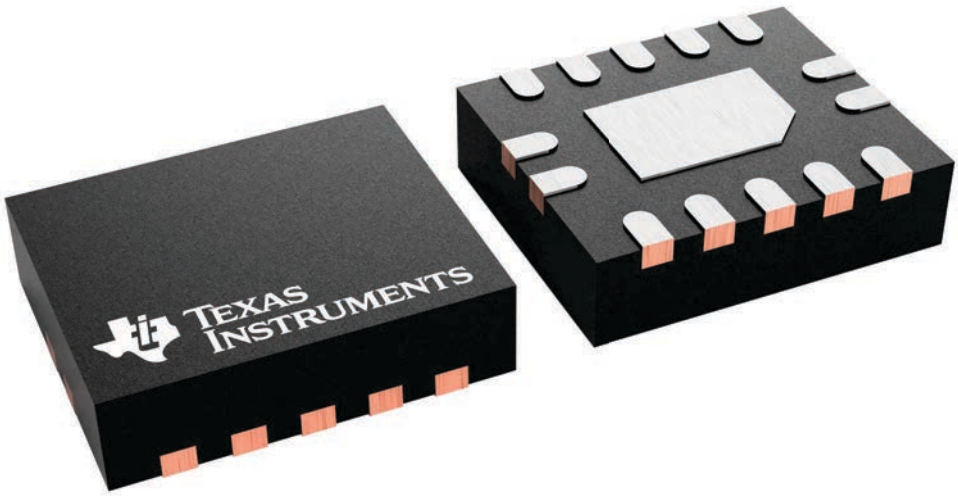
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

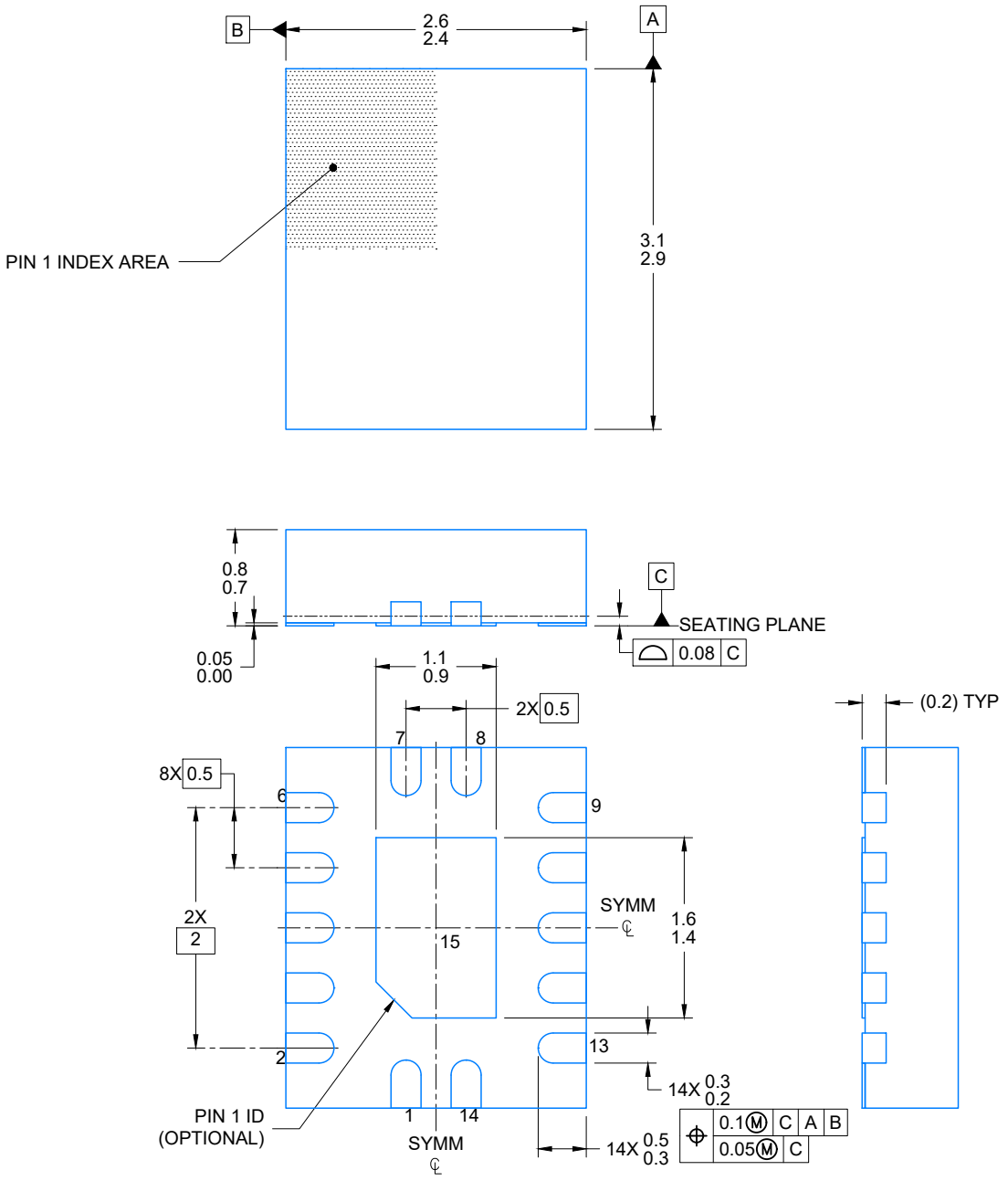


PACKAGE OUTLINE

BQA0014A

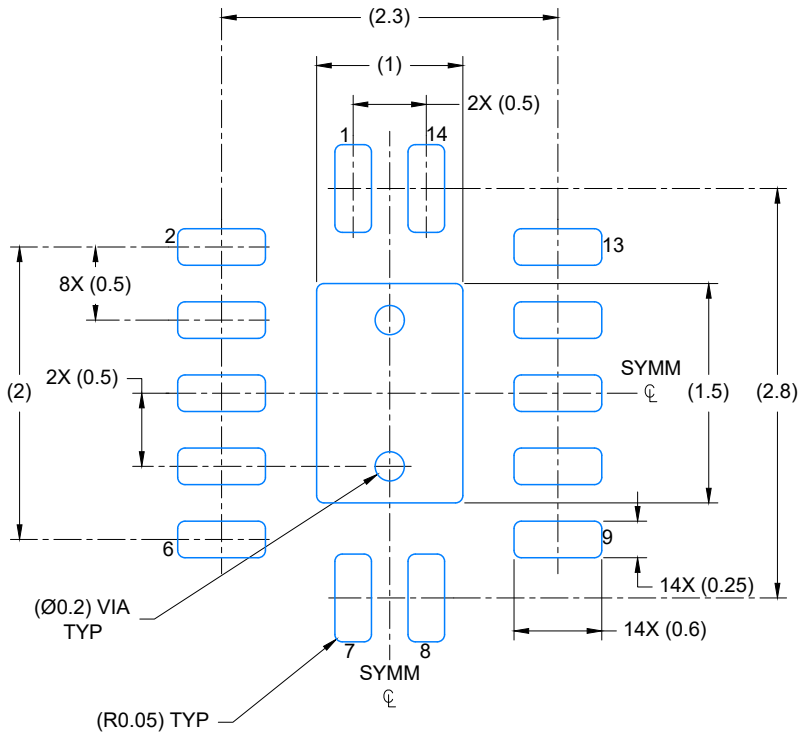
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

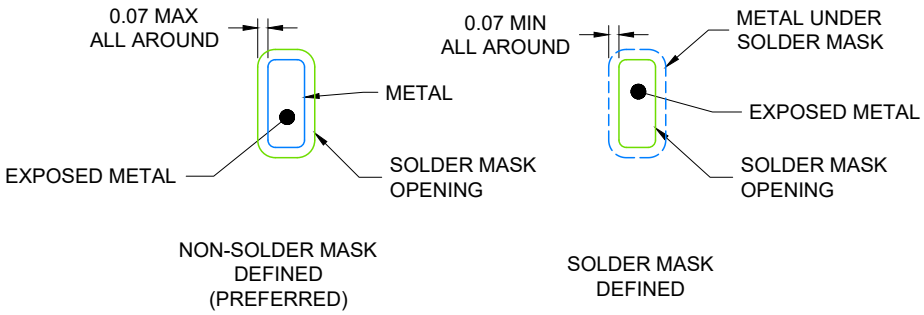


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



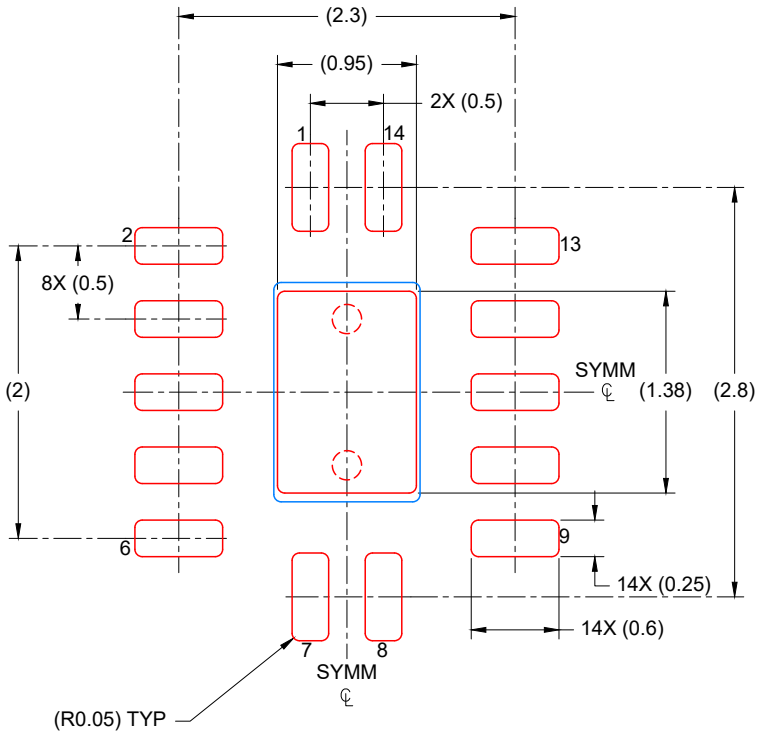
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

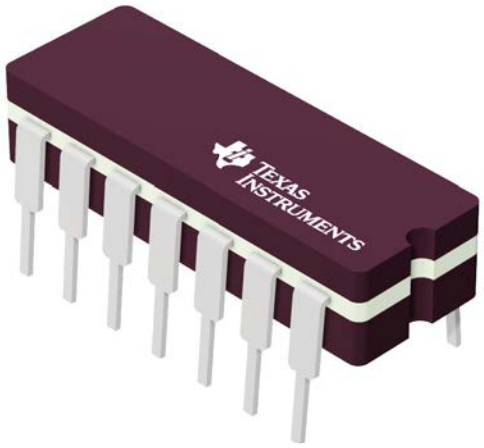
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

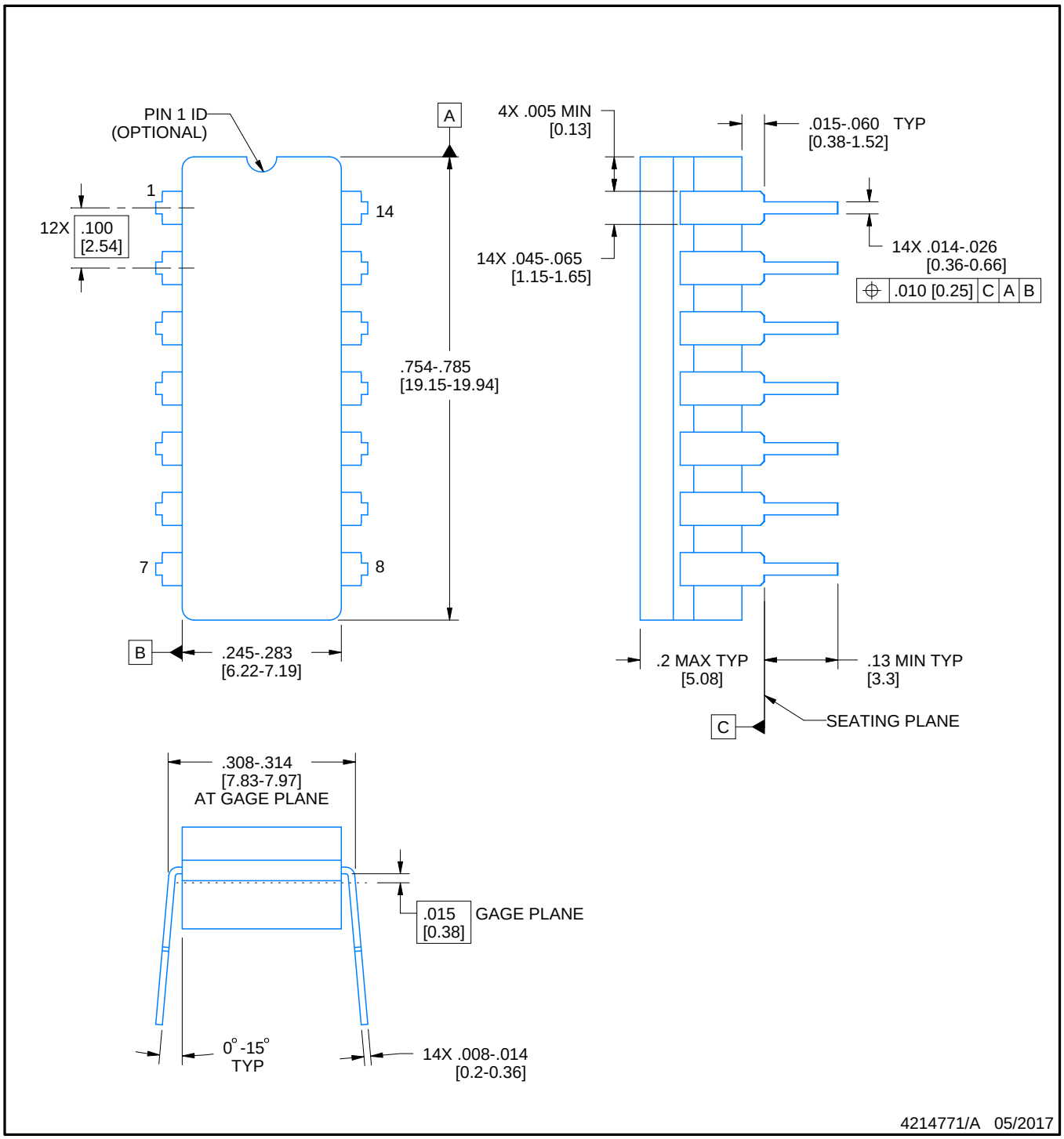
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

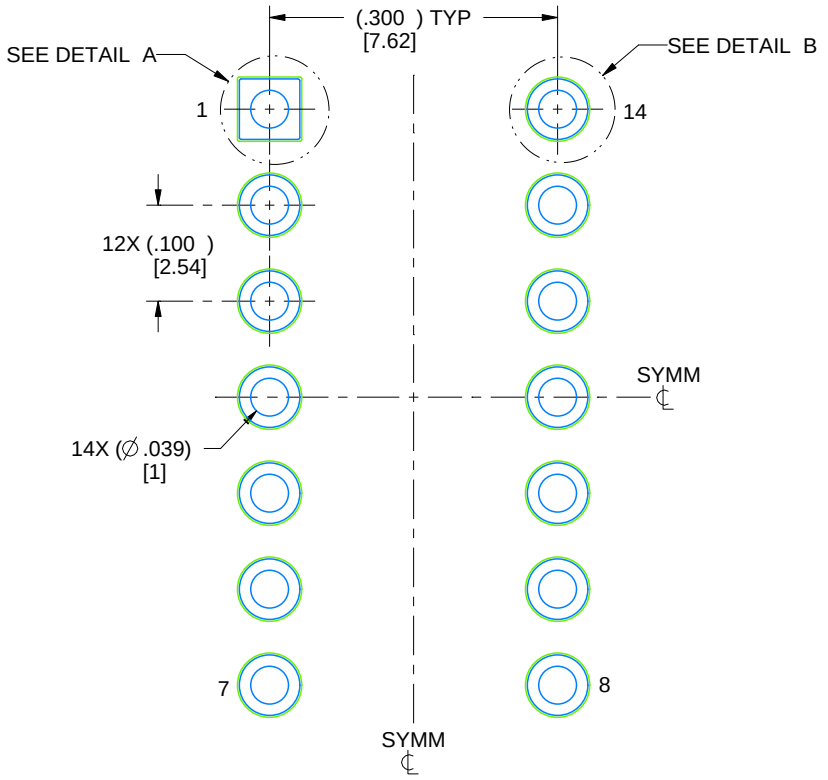
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

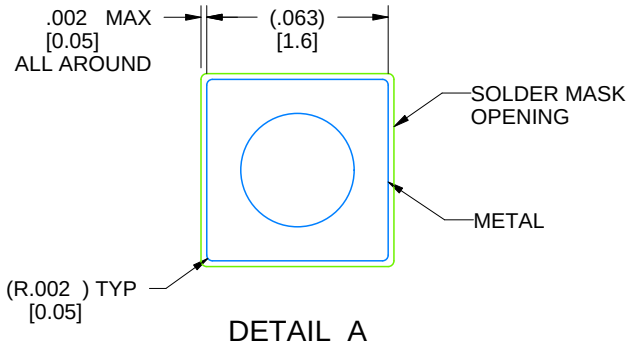
J0014A

CDIP - 5.08 mm max height

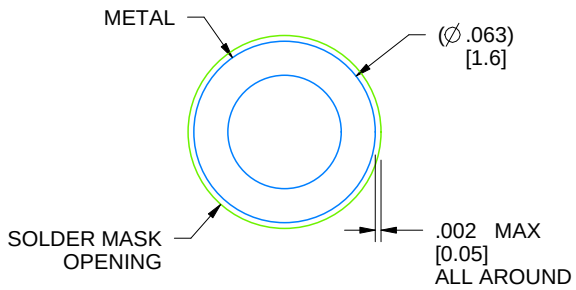
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



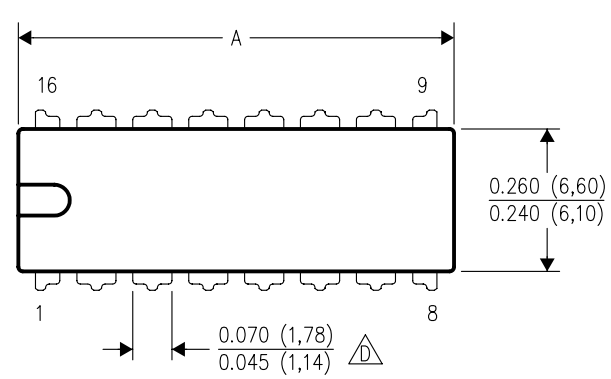
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

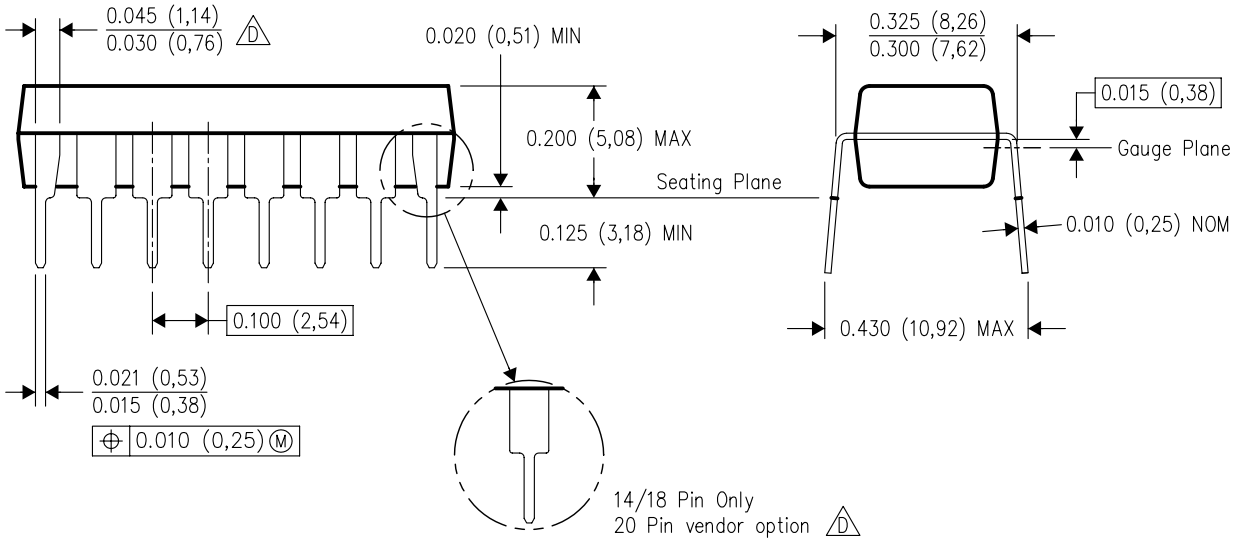
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

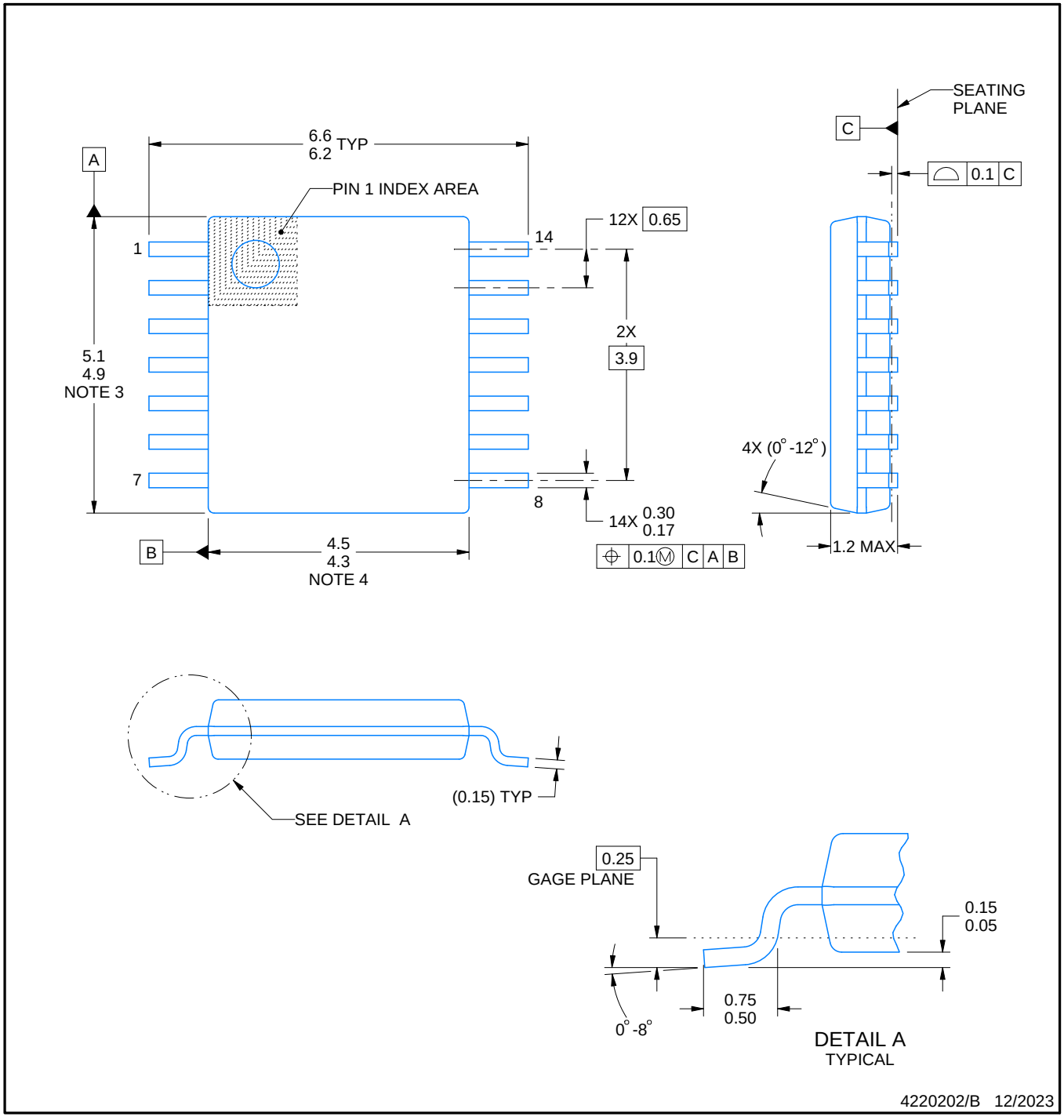
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

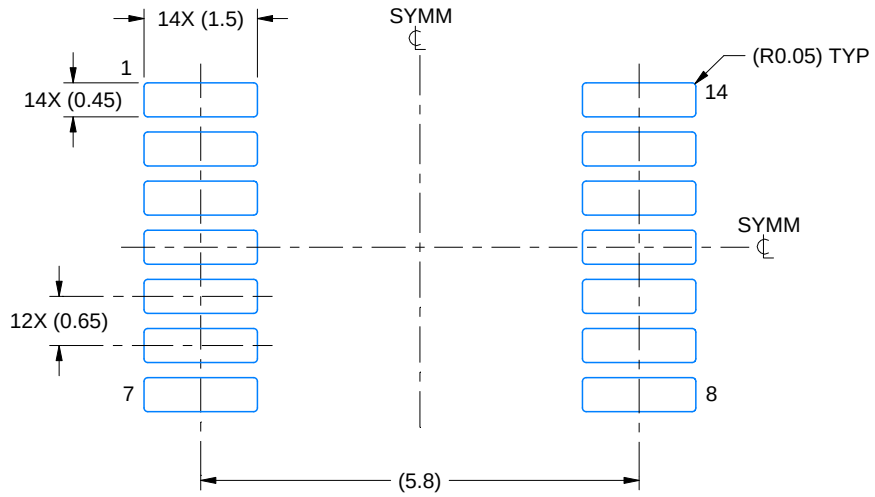
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

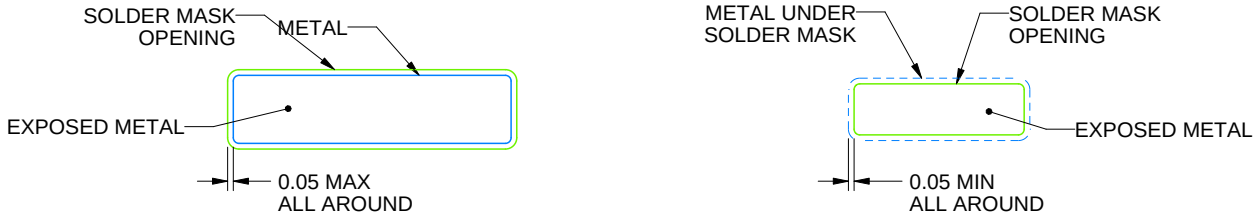


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

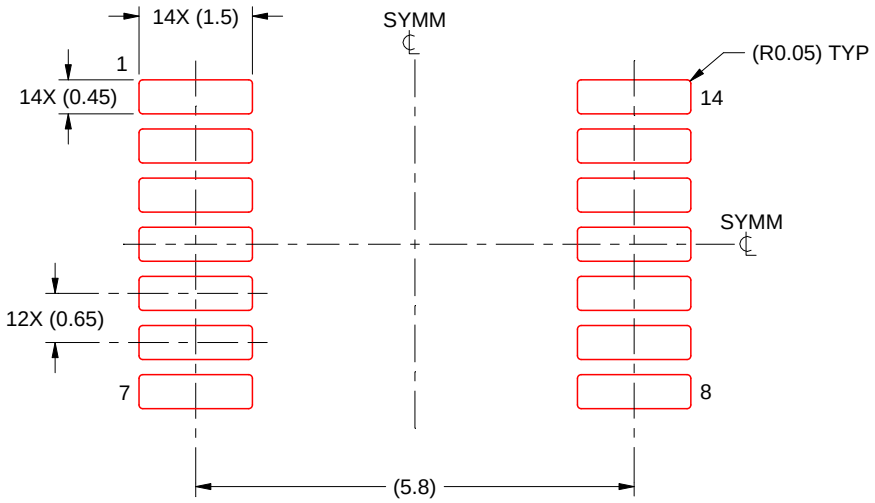


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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