7-SEGMEN

12

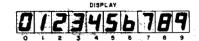


Data sheet acquired from Harris Semiconductor SCHS072B – Revised July 2003

CMOS BCD-to-7-Segment Latch Decoder Drivers

High-Voltage Types (20-Volt Rating)





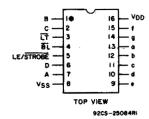
220 - 25087

CD4511B types are BCD-to-7-segment latch decoder drivers constructed with CMOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of RCA CMOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B types to drive LED's and other displays directly.

Lamp Test (\overline{LT}), Blanking (\overline{BL}), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used.

The CD4511B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

These devices are similar to the type MC14511.



CD4511B TERMINAL ASSIGNMENT

Features:

- High-output-sourcing capability up to 25 mA
- Input latches for BCD Code storage
- Lamp Test and Blanking capability
- 7-segment outputs blanked for BCD input codes > 1001
- 100% tested for quiescent current at 20 V
- Max. input current of 1 μA at 18 V, over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings

Applications:

Driving common-cathode LED displays

V_{SS}=8 V_{DD}=16

FUNCTIONAL DIAGRAM

- Multiplexing with common-cathode LED displays
- Driving incandescent displays

CD4511B Types

■ Driving low-voltage fluorescent displays

MAXIMUM RATINGS, Absolute-Maximum Values: DC SUPPLY-VOLTAGE RANGE, (VDD) Voltages referenced to VSS Terminal) -0.5V to +20V INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to VDD +0.5V DC INPUT CURRENT, ANY ONE INPUT # 10mA POWER DISSIPATION PER PACKAGE (PD): For TA = -55°C to +100°C FOR TA = +100°C to +125°C Derate Linearity at 12mW/°C to 200mW DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW OPERATING-TEMPERATURE RANGE (Tag) STORAGE TEMPERATURE RANGE (Tag) -65°C to +125°C LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

OPERATING CONDITIONS AT TA = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

Characteristic	V _{DD}	Min.	Max.	Units
Supply Voltage Range (T _A): (Full Package-Temperature Range)		3	18	٧
	5	150	-	ns
Set-Up Time (tg)	10	70	_	ns
	15	40		ns
	5	0	_	ns
Hold Time (t _H)	10	0	_	ns
	15	0	-	ns
	5	400	_	ns
Strobe Pulse Width (t _W)	10	160	_	ns
	15	100	_	ns

CD4511B Types

STATIC ELECTRICAL CHARACTERISTICS

	TE	ST CON	DITIO	NS								
					LI	IMITS AT	T INDIÇA	ATED TE	EMPER#	TURES	(oc)	
CHARACTERISTIC	Іон	v _o	VIN	V _{DD}		ſ	Γ		Ι	+25	•	Units
	(mA)	(V)	(V)	(V)	-55	-40	+85	+125	Min.	Тур.	Max.	
Quiescent Device		_	_	5	5	5	150	150	_	0.04	5	
Current: IDD			_	10	10	10	300	300	_	0.04	10	μА
Max,			_	15	20	20	600	600		0.04	20	۳.
			_	20	100	100	3000	3000	-	0.08	100	
Output Voltage:				_			0.05					
Law Lavel Ma			0,5	5 10			0.05 0.05		· -	0	0.05	١,,
Low-Level VOL Max.		<u> </u>	0,10	15			0.05		-	0	0.05	: V
IVIGA.	<u> </u>	<u> </u>							<u> </u>		0.05.	<u> </u>
11: 1 1 1 1	<u> </u>	-	0,5	5	4	4	4.2	4.2	4.1	4.55		
High-Level VOH	_	_	0,10	10 15	9	9	9.2	9.2	9.1	9.55		٧
Min.			0.15	15	14	14	14.2.	14.2	14.1	14.55		
Input Low	_	0.5,3.8		5			1.5		_	1.5		
Voltage, VIL	-	1,8.8	-	10			3		-		3	v
Max.		1.5,13.8		15			4		-	_	4	
Input High	-	0.5,3.8		5			3.5		3.5	-	_	
Voltage, V _{IH}	_	1,8.8		10	7				7	_	_	1 v
Min.		1.5,13.8		15			11		11		-	
	0			4	4.0	4.0	4.20	4.20	4.10	4.55	-	
	5	-						_		4.25		
	10			5	3.80	3.80	3.90	3.90	3.90	4.10	_	v
	15		-			-	3.50	3.50		3.95	_	
	20				3.55	3.55	3.30	_	3.40	3.75	_	
	25				3.40	3.40	-		3.10	3.55	~	
	0			•	9.0	9.0	9.20	9.20	9.10	9.55	-	
Output Drive	5					-				9.25	-	i
Voltage:	10	-	-	ļ I ,	8.85	8.85	9.00	9.00	9.00	9.15	,	v
High Level VOH	15	-	-	10	-			'	_	9.05		-
Min.	20	_	-		8.70	8.70	8.40	8.40	8.60	8.90		
	25	-	_	•	8.60	8.60		_	8.30	8.75	· –	
	0			🛊	14.0	14.0	14.20	14.20	14.10	14.55	-	
	5							-		14.30		
	10			15	13.90	13.90	14.0	14.0	14.0	14.20		V
	15 20					- 12.75	1250	- 12.50		14.10	_	
	25				13.75 13.65	13.75 13.65	13.50	13.50	13.70 13.50	13.95 13.80	-	
	25		_		13.05	13.65			13.50	13.80		
Output Low												
(Sink) Current,	_	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	_	
l _{OL}		0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	_	mA
Min.	-	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8		
Input Current, I _{IN} Max.	-	0,18	0,18	18	±0.1	±0.1	±1	±1	-	±10-5	±0.1	μΑ

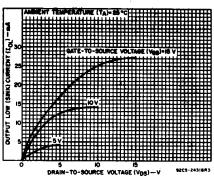


Fig. 1 — Typical output low (sink) current characteristics.

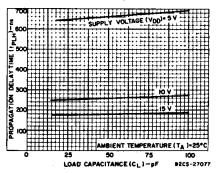


Fig. 2 — Typical data-to-output, low-to-high-level propagation dalay time as a function of load capacitance.

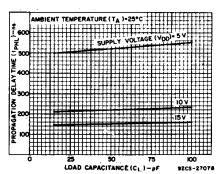


Fig. 3 — Typical data-to-output, high-to-low-level propagation delay time as a function of load capacitance.

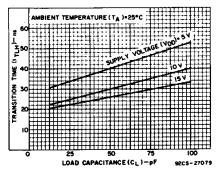


Fig. 4 — Typical low-to-high-level transition time as a function of load capacitance.

CD4511B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^{\circ}C$, Input t_r , $t_f = 20$ ns, C_L = 50 pF, R_L = 200 k Ω

CHARACTERISTIC	Test Conditions	A	UNITS		
X	Y _{DD} Volts	Min.	Тур.	Max.	
Propagation Delay Time:	5	_	520	1040	
(Data)	10	_	210	420	ns
High-to-Low Level, tpHL	15	-	150	300	
	5	_	660	1320	
Low-to-High Level, tPLH	10	l –	260	520	ns
	15	_	180	360	<u>.</u>
Propagation Delay Time:	5	_	350	700	
(BL)	10	-	175	350	ns
High-to-Low Level, tpHL	15	_	125	250	
	5		400	800	
> Low-to-High Level, tpLH	10	_	175	350	ns
	15	- ,	150	300	
Propagation Delay Time:	5	-	250	500	
(LT)	10	-	125	250	ns
High-to-Low Level, tpHL	15		85	170	
	5	_	150	300	
Low-to-High Level, tpLH	10	_	75	150	ns
	15	_	50	100	
Transition Time:	5	_	40	80	
	10	-	30	60	пѕ
Low-to-High Level, tTLH	15		25	50	
	5	-	125	310	
	10	_	75	185	ns
High-to-Low Level, tTHL	15	_	65	160	
Minimum Coulde Ti	5	150	75	_	
Minimum Set-Up Time, tS	10	70	35	-	ns
	15	40	20	_	
	5	0	-75	_	
Minimum Hold Time, tH	10	0	-35	_	ns
	15	0	-20	_	
6. I B. W	5	400	200	_	
Strobe Pulse Width, t _W	10	160	80	. —	ns
	15	100	50		
Input Capacitance, CIN			5	7.5	pF

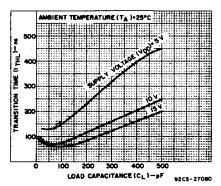


Fig. 5 - Typical high-to-low transition time as a function of load capacitance.

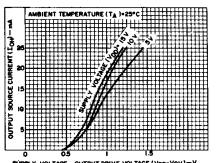


Fig. 6 - Typical voltage drop (V_{DD} to output) vs. output source current as a function of supply.

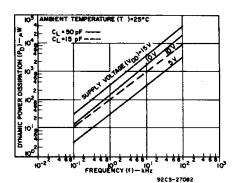
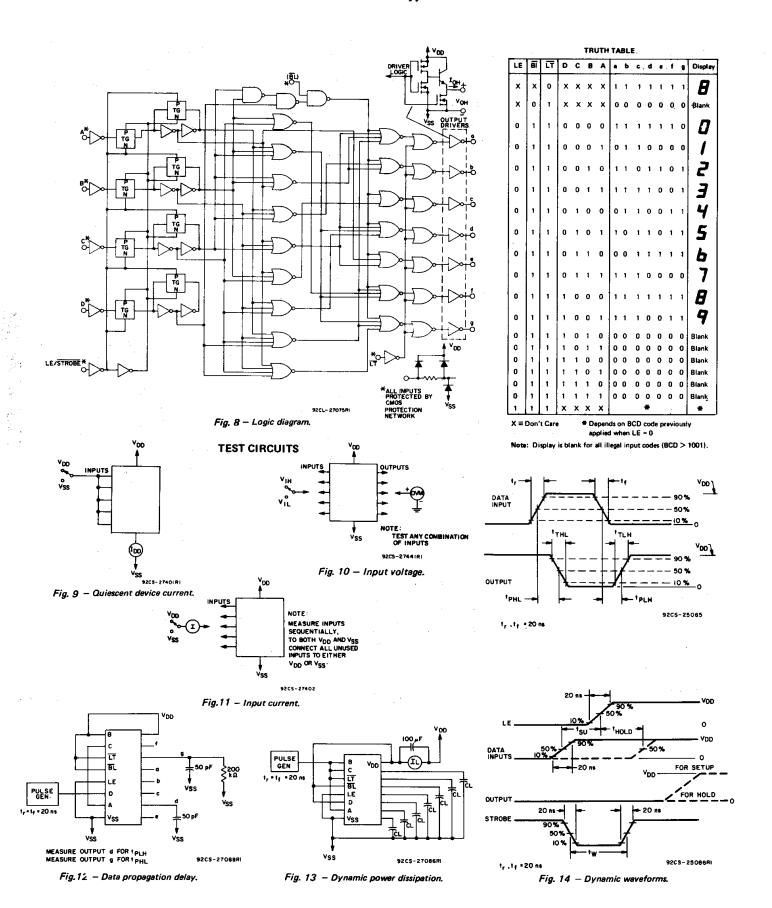
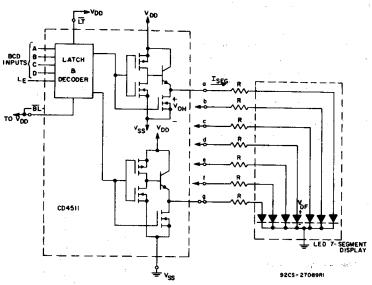


Fig. 7 - Typical dynamic power dissipation characteristics.

CD4511B Types



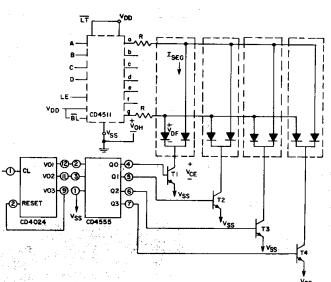
APPLICATIONS Interfacing with Various Displays



Duty Cycle = 100%

ISEG = IDIODEAVG. = 20 mA at Luminous Intensity/Segment = 250 microcandles

Fig. 15 - Driving common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7740).



Multiplexing Scheme Showing 2 of 7 Segments Connected

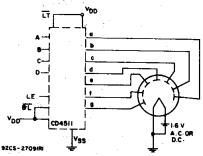
Transistors T₁-T₄ (RCA-2N3053 or 2N2102) have I_C Max.rating >7xI_{SEG}

Duty Cycle = 25% I SEG = $^{[I]}$ DIODE_{AVG} I × 4 $_{R}$ = $^{(V}$ OH - V DF - V CE I

ISEG

All unused inputs on CD4555 are connected to V_{DD} or V_{SS}

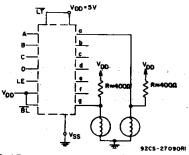
Fig. 18 — Multiplexing with common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7404 4 character display or 4 discrete Monosanto Man 3 displays).



A medium-brightness intensity display can be obtained with low-voltage fluorescent displays such as the Tung-Sol Digivac S/G** Series.

**Trademark Tung-Sol Division Wagner Electric Co.

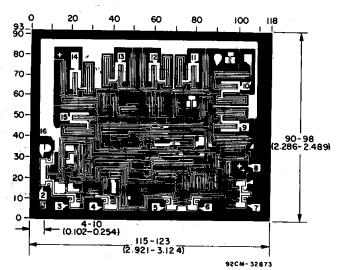
Fig. 16 — Driving low-voltage fluorescent displays.



2 of 7 Segments Shown Connected

Resistors R from V_{DD} to each 7-segment driver output are chosen to keep all Numitron segments slightly on and warm.

Fig. 17 — Driving incandescent displays (RCA Numitron DR2000 series displays).



Dimensions and pad layout for CD45118 chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3}) inch).

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Bell metalial Beals mellans		Op temp (°C)	Part marking (6)
	(1)	(2)			(0)	(4)	(5)		(0)
CD4511BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4511BE
CD4511BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4511BE
CD4511BEE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4511BE
CD4511BF	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4511BF
CD4511BF.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4511BF
CD4511BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4511BF3A
CD4511BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4511BF3A
CD4511BNSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4511B
CD4511BNSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4511B
CD4511BNSRG4	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4511B
CD4511BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM511B
CD4511BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	CM511B
CD4511BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM511B
CD4511BPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM511B

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD4511B, CD4511B-MIL:

Catalog : CD4511B

Military: CD4511B-MIL

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

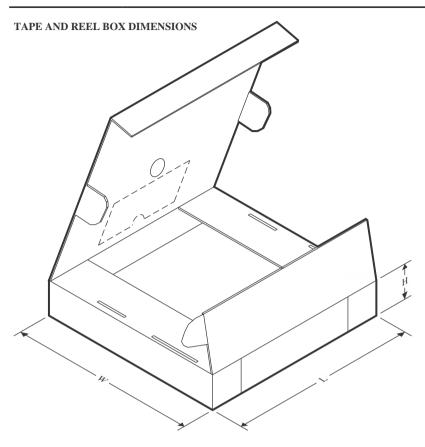


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4511BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4511BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4511BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4511BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4511BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD4511BPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4511BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4511BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4511BEE4	N	PDIP	16	25	506	13.97	11230	4.32

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOP



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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