

## CMOS 8-STAGE STATIC SHIFT REGISTER

Check for Samples: [CD4021B-Q1](#)

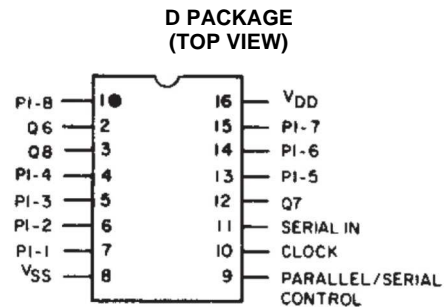
### FEATURES

- Qualified for Automotive Applications
- Medium-Speed Operation: 12-MHz (Typ) Clock Rate at  $V_{DD} - V_{SS} = 10\text{ V}$
- Fully Static Operation
- Eight Master-Slave Flip-Flops Plus Output Buffering and Control Gating
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1  $\mu\text{A}$  at 18 V Over Full Package-Temperature Range: 100 nA at 18 V and 25°C
- Noise Margin (Full Package-Temperature Range):
  - 1 V at  $V_{DD} = 5\text{ V}$
  - 2 V at  $V_{DD} = 10\text{ V}$
  - 2.5 V at  $V_{DD} = 15\text{ V}$
- Standardized Symmetrical Output Characteristics
- 5-V, 10-V, and 15-V Parametric Ratings

- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Latch-Up Performance Meets 50 mA per JESD 78, Class I

### APPLICATIONS

- Parallel Input/Serial Output Data Queuing
- Parallel-to-Serial Data Conversion
- General-Purpose Register



### DESCRIPTION

CD4021B series types are 8-stage parallel- or serial-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the CD4014B. In the CD4021B serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the CD4021B, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

The CD4021B series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	CD4010BQDRQ1	CD4021BQ

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



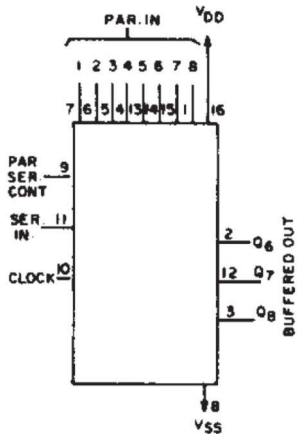
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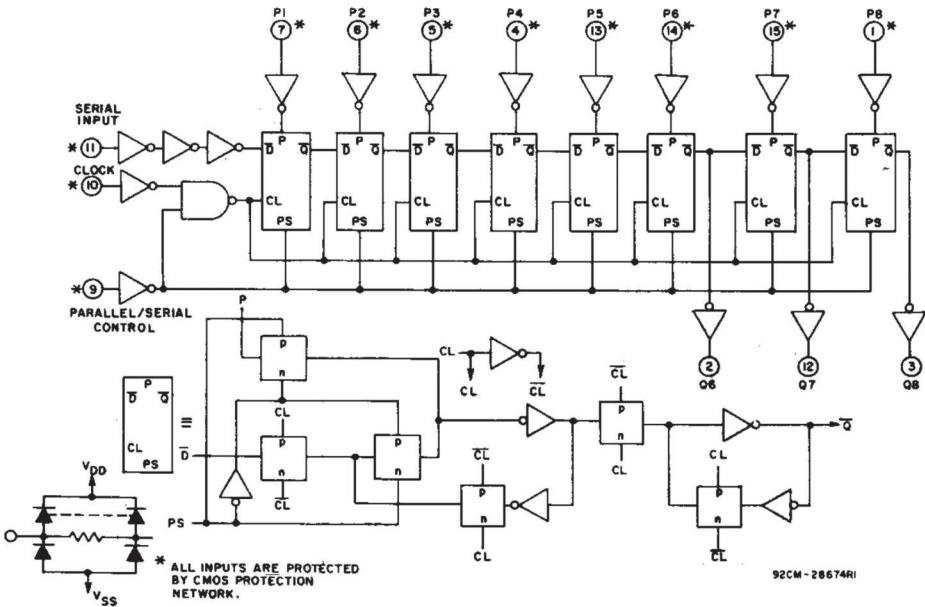
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Functional Diagram



Logic Diagram



TRUTH TABLE – CD4021B

CL	Serial Input	Parallel/Serial Control	PI-1	PI-n	Q1 (Internal)	Qn
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
0	0	0	X	X	0	Q <sub>n-1</sub>
1	0	0	X	X	1	Q <sub>n-1</sub>
X	X	0	X	X	Q <sub>1</sub>	Q <sub>n</sub>

X = DON'T CARE CASE

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V <sub>DD</sub>	DC supply voltage range (voltage referenced to V <sub>SS</sub> terminal)		−0.5 to +20	V
	Input voltage range, all inputs		−0.5 to V <sub>DD</sub> +0.5	V
	DC input current, any one input		±10	mA
P <sub>D</sub>	Power dissipation per package	T <sub>A</sub> = −40°C to +100°C	500	mW
		T <sub>A</sub> = +100°C to +125°C	Derate Linearity at 12mW/°C to 20 mW	
P <sub>D</sub>	Device dissipation per output transistor		100	mW
T <sub>A</sub>	Operating temperature range		−40 to +125	°C
T <sub>stg</sub>	Storage temperature range		−65 to +150	°C
ESD	Electrostatic discharge rating <sup>(2)</sup>	Human-body model (HBM)	2000	V
		Machine model (MM)	200	
		Charged-Device Model (CDM)	1000	
Latch-up performance per JESD 78, Class I			50	mA

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Tested in accordance with AEC-Q100.

## RECOMMENDED OPERATING CONDITIONS

At  $T_A = 25^\circ\text{C}$ , unless other wise specified. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

		$V_{DD}$	MIN	MAX	UNIT
	Supply voltage range ( $T_A$ = full package-temperature range)		3	18	V
$t_W$	Clock pulse width	5	180		ns
		10	80		
		15	50		
$f_{CL}$	Clock frequency	5		3	MHz
		10		6	
		15		8.5	
$t_{CL}$ , $t_{fCL}$	Clock rise and fall time	5		15	$\mu\text{s}$
		10		15	
		15		15	
$t_s$	Serial input (referred to CL)	5	120		ns
		10	80		
		15	60		
	Parallel inputs CD4014B (referred to CL)	5	80		ns
		10	50		
		15	40		
	Parallel inputs CD4021B (referred to P/S)	5	50		ns
		10	30		
		15	20		
	Parallel/Serial Control CD4014B (referred to CL)	5	180		ns
		10	80		
		15	60		
$t_W$	Parallel/serial pulse width	5	160		ns
		10	80		
		15	50		
$t_{REM}$	Parallel/serial removal time	5	280		ns
		10	140		
		15	100		

## STATIC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNIT	
		V <sub>D</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	−40	+85	+125	+25				
								5	150	150		
I <sub>DD</sub> Max	Quiescent device current		0.5	5	10	300	300	0.04			5	μA
			0.10	10	20	600	600	0.04			10	
			0.15	15	100	3000	3000	0.04			20	
			0.20	20	0.61	0.42	0.36	0.08			100	
I <sub>OL</sub> Min	Output low (sink) current	0.4	0.5	5	1.5	1.1	0.9	0.51	1		mA	
		0.5	0.10	10	4	2.8	2.4	1.3	2.6			
		1.5	0.15	15	−0.61	−0.42	−0.36	3.4	6.8			
I <sub>OH</sub> Min	Output high (source) current	4.6	0.5	5	−1.8	−1.3	−1.15	−0.51	−1		mA	
		2.5	0.5	5	−1.5	−1.1	−0.9	−1.6	−3.2			
		9.5	0.10	10	−4	−2.8	−2.4	−1.3	−2.6			
		13.5	0.15	15	−4.2			−3.4	−6.8			
V <sub>OL</sub> Max	Output voltage: low level		0.5	5	0.05			0		0.05	V	
			0.10	10	0.05			0		0.05		
			0.15	15	0.05			0		0.05		
V <sub>OH</sub> Min	Output voltage: high level		0.5	5	4.95			4.95	5		V	
			0.10	10	9.95			9.95	10			
			0.15	15	14.95			14.95	15			
V <sub>IL</sub> Max	Input low voltage	0.5, 4.5		5	1.5			1.5			V	
		1, 9		10	3			3				
		1.5, 13.5		15	4			4				
V <sub>IH</sub> Min	Input high voltage	0.5, 4.5		5	3.5			3.5			V	
		1, 9		10	7			7				
		1.5, 13.5		15	11			11				
I <sub>IN</sub> Max	Input current		0, 18	18	±0.1	±1	±1	±10 <sup>−5</sup>		±0.1	μA	

## DYNAMIC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ , Input  $t_r/t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

PARAMETER	TEST CONDITIONS	$V_{DD}$	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$ Propagation delay time		5		160	320	ns
		10		80	160	
		15		30	120	
$t_{THL}$ , $t_{TLH}$ Transition time		5		100	200	ns
		10		50	100	
		15		40	80	
$f_{CL}$ Maximum clock input <sup>(1)</sup>		5	3	6		MHz
		10	6	12		
		15	8.5	17		
$t_W$ Minimum clock pulse width <sup>(1)</sup>		5		90	180	ns
		10		40	80	
		15		25	50	
$t_{rCL}$ , $t_{fCL}$ Clock rise and fall time <sup>(2)(1)</sup>		5			15	$\mu\text{s}$
		10			15	
		15			15	
$t_s$ Minimum setup time <sup>(1)</sup>	Serial input (referred to CL)	5		60	120	ns
		10		40	80	
		15		30	60	
	Parallel inputs (referred to CL)	5		40	80	
		10		25	50	
		15		20	40	
	Parallel inputs (referred to P/S)	5		25	50	
		10		15	30	
		15		10	20	
	Serial in, Parallel in, Parallel/Serial Control	5		90	180	
		10		40	80	
		15		30	60	
$t_H$ Minimum hold time <sup>(1)</sup>		5			0	ns
		10			0	
		15			0	
$t_{WH}$ Minimum P/S pulse width <sup>(1)</sup>		5		80	160	ns
		10		40	80	
		15		25	50	
$t_{REM}$ Minimum P/S removal time <sup>(1)</sup>		5		140	280	ns
		10		70	140	
		15		50	100	
$C_I$ Average input capacitance <sup>(1)</sup>				5	7.5	pF

(1) Not production tested

(2) If more than one unit is cascaded,  $t_{rCL}$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.



## Typical Characteristics

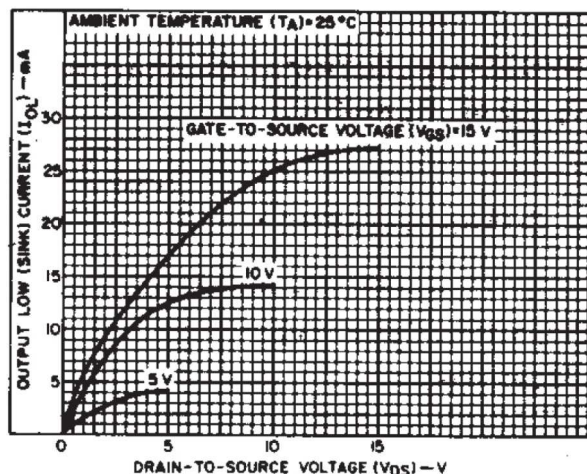


Figure 1. Typical Output Low (Sink) Current Characteristics

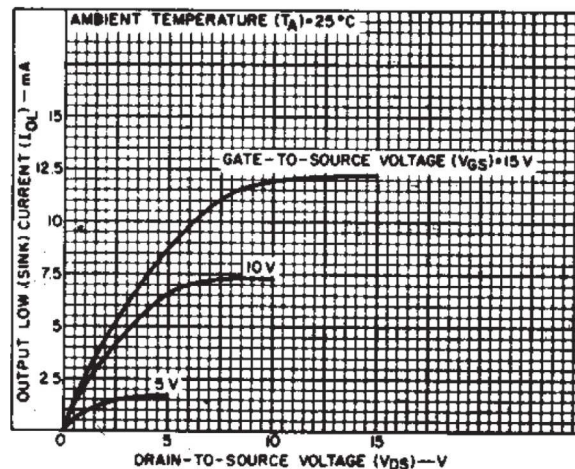


Figure 2. Minimum Output Low (Sink) Current Characteristics

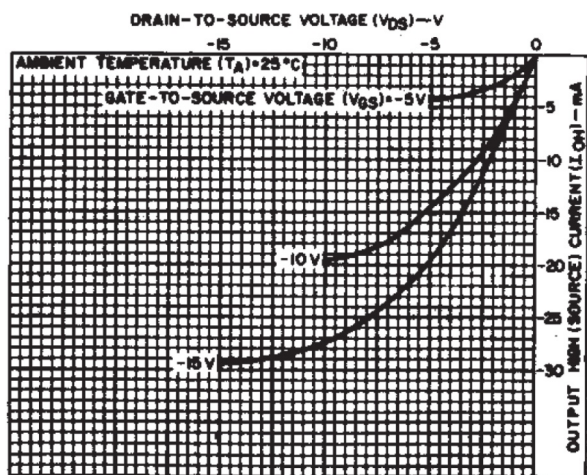


Figure 3. Typical Output High (Source) Current Characteristics

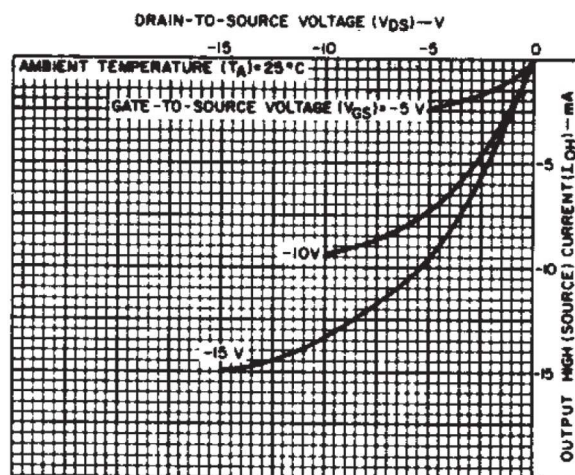


Figure 4. Minimum Output High (Source) Current Characteristics

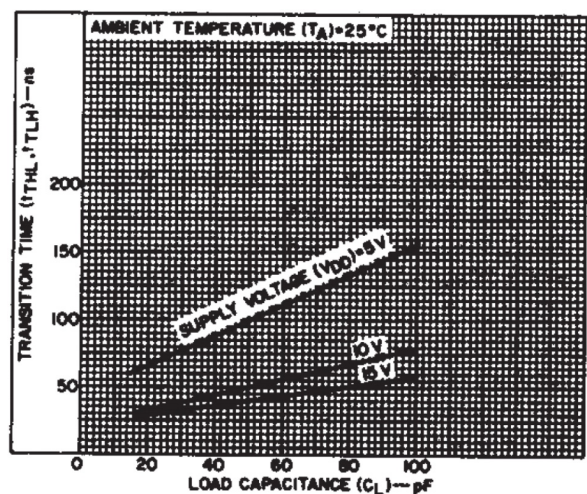


Figure 5. Typical Transition Time as a Function of Load Capacitance

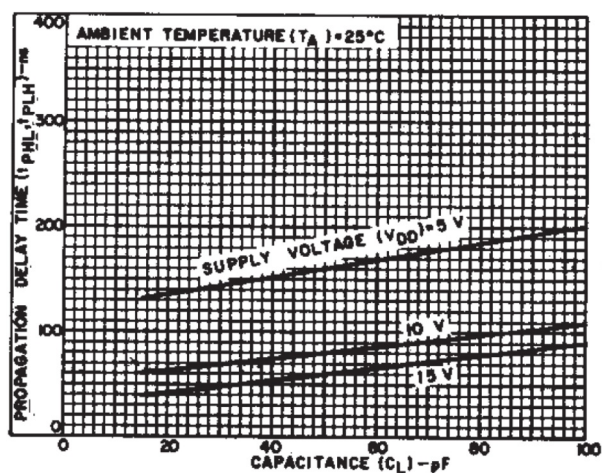


Figure 6. Typical Propagation Delay Times as a Function of Load Capacitance

### Typical Characteristics (continued)

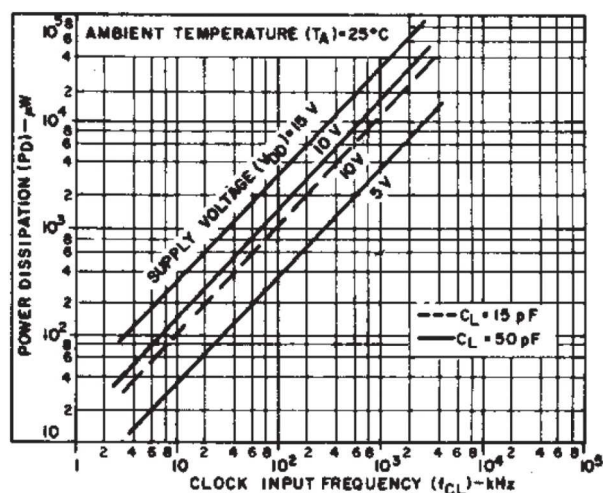
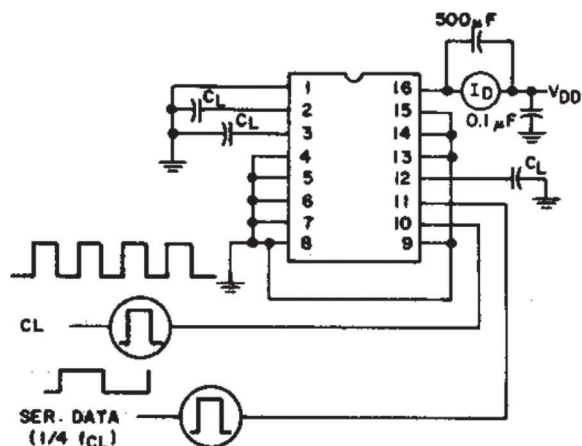


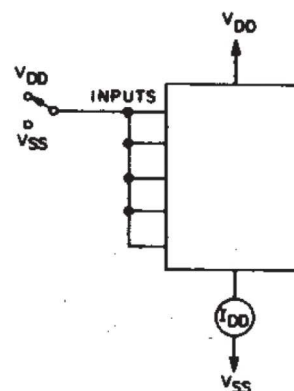
Figure 7. Typical Dynamic Power Dissipation as a Function of Clock Input Frequency



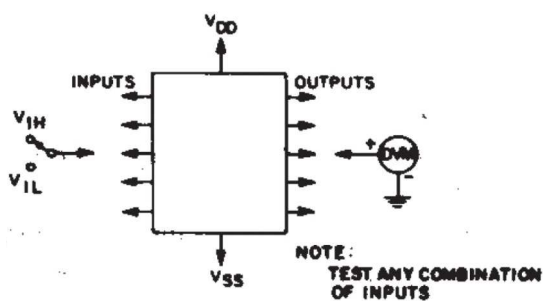
## PARAMETER MEASUREMENT INFORMATION



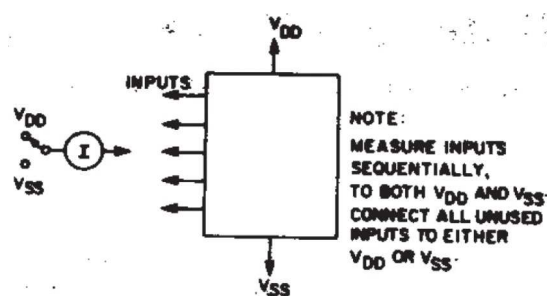
### Figure 8. Dynamic Power Dissipation Test Circuit



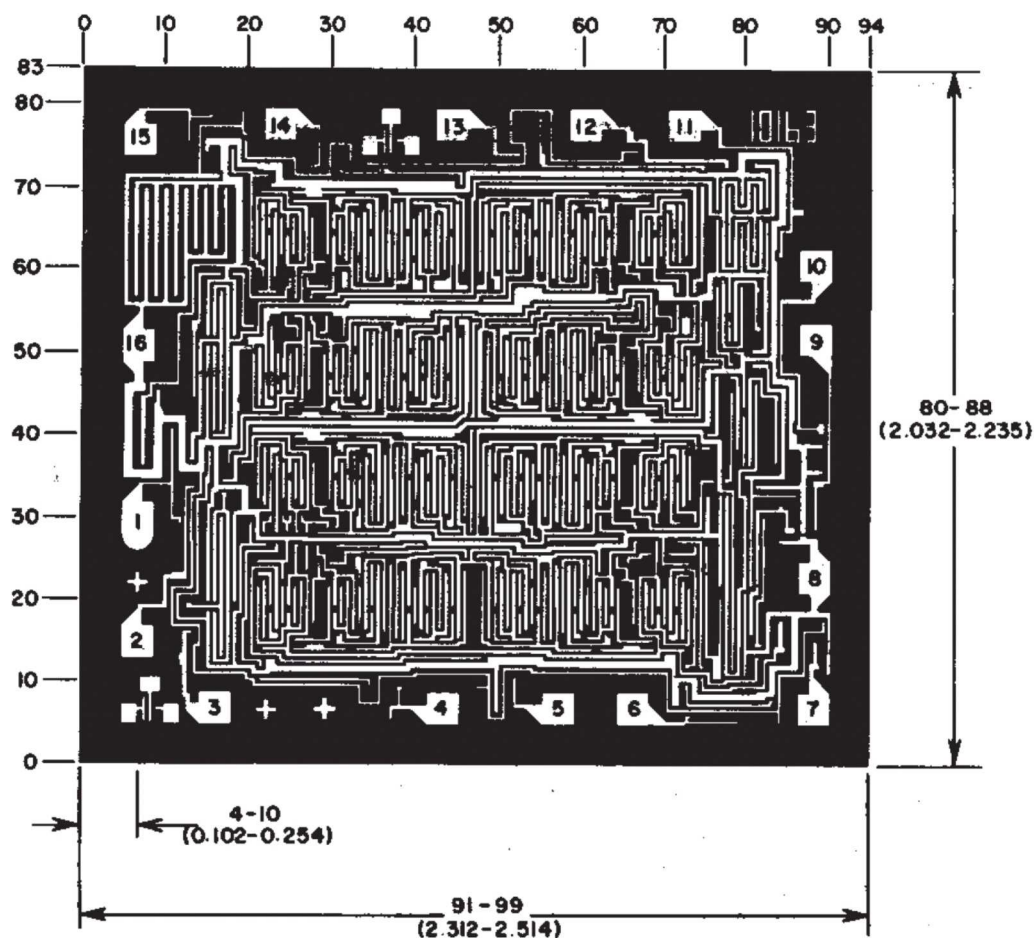
### Figure 9. Quiescent Device Current Test Circuit



### Figure 10. Input Voltage Test Circuit



**Figure 11. Input Current Test Circuit**



Note: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduation are in mils ( $10^{-3}$  inch).

**Figure 12. Dimensions and Pad Layout**

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4021BQDRQ1	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4021BQ
CD4021BQDRQ1.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4021BQ

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF CD4021B-Q1 :

- Catalog : [CD4021B](#)

- Military : [CD4021B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

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