











## **CD4016B Types CMOS Quad Bilateral Switch**

#### 1 Features

- 20V digital or ± 10V peak-to-peak switching
- 280Ω typical on-state resistance for 15V operation
- Switch on-state resistance matched to within  $10\Omega$ typ over 15V signal-input range
- High on/off output-voltage ratio: 65dB typ at  $f_{is} = 10kHz$ ,  $R_L = 10k\Omega$
- High degree of linearity: <0.5% distortion typ at f  $_{is}$ = 1kHz, V  $_{is}$ = 5V $_{p-p}$ , V  $_{DD}$  -V  $_{SS}$   $\square$  10V, R  $_{L}$  =  $10k\Omega$
- Extremely low off-state switch leakage resulting in very low offset current and high effective offstate resistance: 100pA typ. at V <sub>DD</sub> -V <sub>SS</sub> =18V,  $T_A=25^{\circ}C$
- Extremely high control input impedance (control circuit isolated from signal circuit: 10  $^{12}\,\Omega$  typ.
- Low crosstalk between switches: -50dB typ at f is = 0.9MHz,  $R_{\perp} = 1k\Omega$
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch on = 40MHz (typical)
- 100% tested for guiescent current at 20V
- Maximum control input current of 1µA at 18V over full package temperature range; 100nA at 18V at 25°C
- 5V, 10V, and 15V parametric ratings

#### 2 Applications

- Analog signal switching/multiplexing signal gating
- Modulator squelch control
- Demodulator chopper
- Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital and digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

### 3 Description

For transmission or multiplexing of analog or digital signals high-voltage types (20V rating).

CD4016B B Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch on or off.

The CD4016B B Series types are supplied in 14lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

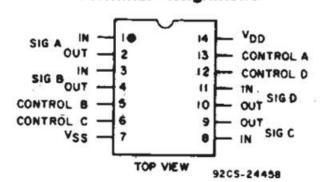
#### **Package Information**

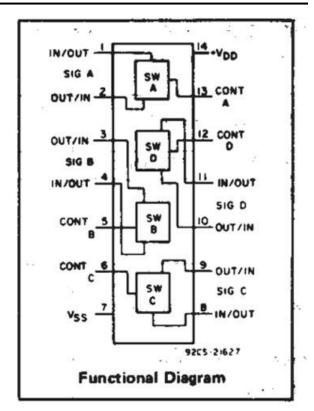
PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
CD4016B	N (PDIP, 14)	19.3mm × 9.4mm
CD4010B	D (SOIC, 14)	8.65mm × 6mm

- For more information, see Section 8.
- The package size (length × width) is a nominal value and includes pins, where applicable.



# Terminal Assignment





Schematic Diagram - 1 of 4 Identical Sections

Product Folder Links: CD4016B



## **Table of Contents**

1 Features1	4.5 Electrical Characteristics
2 Applications 1	4.6 Electrical Characteristics
3 Description1	
4 Specifications4	
4.1 Absolute Maximum Ratings4	6 Device and Documentation Support13
4.2 ESD Ratings4	6.1 Documentation Support13
4.3 Recommended Operating Conditions4	7 Revision History13
	8 Mechanical, Packaging, and Orderable Information 13

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

, J	,	MIN	MAX	UNIT
V <sub>DD</sub> – V <sub>SS</sub>			20	V
$V_{DD}$	Supply voltage	-0.5	20	V
V <sub>SS</sub>		-20	0.5	V
I <sub>SEL</sub> or I <sub>EN</sub>	Logic control input pin current (EN, Ax, SELx)	-30	30	mA
V <sub>S</sub> or V <sub>D</sub>	Source or drain voltage (Sx, D)	V <sub>SS</sub> -0.5	V <sub>DD</sub> +0.5	V
I <sub>S</sub> or I <sub>D (CONT)</sub>	Source or drain continuous current (Sx, D)	-20	20	mA
TJ	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 4.2 ESD Ratings

			VALUE	UNIT
V	Floatrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±500	
V(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1500	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
V <sub>DD</sub> – V <sub>SS</sub> (1)	Power supply voltage differential	3	18	V
$V_{DD}$	Positive power supply voltage	3	18	V
V <sub>S</sub> or V <sub>D</sub>	Signal path input/output voltage (source or drain pin) (Sx, D)	V <sub>SS</sub>	$V_{DD}$	V
V <sub>SEL</sub> or V <sub>EN</sub>	Address or enable pin voltage	0	$V_{DD}$	V
I <sub>S</sub> or I <sub>D (CONT)</sub>	Source or drain continuous current (Sx, D)	-10	10	mA
T <sub>A</sub>	Ambient temperature	<b>–</b> 55	125	°C

(1)  $V_{DD}$  and  $V_{SS}$  can be any value as long as  $3V \le (V_{DD} - V_{SS}) \le 24V$ , and the minimum  $V_{DD}$  is met.

Product Folder Links: CD4016B

<sup>(2)</sup> All voltages are with respect to ground, unless otherwise specified.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 4.4 Thermal Information

		CD	CD4016				
	THERMAL METRIC <sup>(1)</sup>	N (PDIP)	D (SOIC)	UNIT			
		14 PINS	14 PINS				
R <sub>0JA</sub>	Junction-to-ambient thermal resistance	93.7	109.7	°C/W			
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	72.5	69.4	°C/W			
R <sub>0JB</sub>	Junction-to-board thermal resistance	68.0	67.9	°C/W			
$\Psi_{JT}$	Junction-to-top characterization parameter	50.3	25.8	°C/W			
$\Psi_{JB}$	Junction-to-board characterization parameter	67.3	67.1	°C/W			

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 4.5 Electrical Characteristics

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5V$ , and  $R_1 = 100\Omega$ , (unless otherwise noted)<sup>(1)</sup>

	PARAMETER		TEST CONDITIONS	MIN TYP MAX	UNIT
SIGNAL	. INPUTS (V <sub>IS</sub> ) AND OUTPUTS (V	'os)			•
			T <sub>A</sub> = -55°C	5	
			T <sub>A</sub> = -40°C	5	
		$V_{is} = 0 \text{ to } 5V$ $V_{DD} = 5V$	T <sub>A</sub> = 25°C	4.5 6	
		TOD ST	T <sub>A</sub> = 85°C	7.5	
			T <sub>A</sub> = 125°C	7.5	
			T <sub>A</sub> = -55°C	6	
			T <sub>A</sub> = -40°C	6	
	$V_{is} = 0 \text{ to } 10V$ $V_{DD} = 10V$	T <sub>A</sub> = 25°C	5 7		
	TOD 101	T <sub>A</sub> = 85°C	15		
	Quiescent Device Current		T <sub>A</sub> = 125°C	15	
DD			T <sub>A</sub> = -55°C	7	μA
			T <sub>A</sub> = -40°C	7.2	
		$V_{is} = 0 \text{ to } 15V$ $V_{DD} = 15V$	T <sub>A</sub> = 25°C	6 8	
		TOD 101	T <sub>A</sub> = 85°C	30	
			T <sub>A</sub> = 125°C	30	
			T <sub>A</sub> = -55°C	8.5	
		T <sub>A</sub> = -40°C	8.5		
		$V_{is} = 0 \text{ to } 20V$ $V_{DD} = 20V$	T <sub>A</sub> = 25°C	6.5 9	]
		700 201	T <sub>A</sub> = 85°C	150	]
			T <sub>A</sub> = 125°C	150	1

Copyright © 2024 Texas Instruments Incorporated



## 4.5 Electrical Characteristics (continued)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5V$ , and  $R_L = 100\Omega$ , (unless otherwise noted)(1)

	erating free-air temperature rang PARAMETER			ONDITIONS		MIN TYP	MAX	UNIT	
				T <sub>A</sub> = -55°C			600		
			V <sub>DD</sub> = 10V	T <sub>A</sub> = -40°C			610		
			$V_{is} = V_{SS}$ or	T <sub>A</sub> = 25°C		250	660		
			$V_{DD}$	T <sub>A</sub> = 85°C			840		
				T <sub>A</sub> = 125°C			960		
				T <sub>A</sub> = -55°C			1870		
			V <sub>DD</sub> = 10V	T <sub>A</sub> = -40°C			1900		
			$V_{is} = 4.75 \text{ to}$	T <sub>A</sub> = 25°C			2000		
	ON Resistance I <sub>ON</sub> wax	to	5.75V	T <sub>A</sub> = 85°C			2380		
		(V <sub>DD</sub> +V <sub>SS</sub> )/2,		T <sub>A</sub> = 125°C			2600		
r <sub>ON</sub>		$V_C = V_{DD}$		T <sub>A</sub> = -55°C			360	Ω	
		$RL = 10k\Omega$	V <sub>DD</sub> = 15V	T <sub>A</sub> = -40°C			370		
			$V_{is} = V_{SS}$ or	T <sub>A</sub> = 25°C		200	400		
			$V_{DD}$	T <sub>A</sub> = 85°C			520		
				T <sub>A</sub> = 125°C			600		
				T <sub>A</sub> = -55°C			775	-	
			V <sub>DD</sub> = 15V	T <sub>A</sub> = -40°C			790		
			$V_{is} = 7.25 \text{ to}$	T <sub>A</sub> = 25°C			850		
			7.75V	T <sub>A</sub> = 85°C			1080		
				T <sub>A</sub> = 125°C			1230		
				$\begin{vmatrix} V_{DD} = 5V \\ V_{SS} = 0V \end{vmatrix} T_A =$	T <sub>A</sub> = 25°C		580	7000	
r	ON Resistance r <sub>ON</sub> Max	to (V <sub>DD</sub> +V <sub>SS</sub> )/2	N Resistance row May (V <sub>DD</sub> +V <sub>SS</sub> )/2 ,	$V_{DD} = 7.5V$ $V_{SS} = -7.5V$	T <sub>A</sub> = 25°C		200	280	Ω
r <sub>ON</sub>	ON Resistance ION Max	$V_C = V_{DD},$ RL = $10k\Omega$	$V_{DD} = 5V$ $V_{SS} = -5V$	T <sub>A</sub> = 25°C		250	580	1 22	
			$V_{DD} = 2.5V$ $V_{SS} = -2.5V$	T <sub>A</sub> = 25°C		520	30000		
			V <sub>DD</sub> = 5V	1		15	5		
∆R <sub>ON</sub>	On-state resistance difference between any two switches	$R_L = 10k\Omega$ , $V_C = V_{DD}$	V <sub>DD</sub> = 10V			10	)	Ω	
	between any two switches	VC VDD	V <sub>DD</sub> = 15V			5	5		
THD	Total Harmonic Distortion	V <sub>C</sub> = V <sub>DD</sub> = 5\ on 0V), R <sub>L</sub> = 1	$V_{SS} = -5V, V_{is}$ $V_{SS} = -5V, V_{is}$ $V_{SS} = -5V, V_{is}$	sine wave	ave centered	0.4	ļ	%	
BW	-3-dB cutoff frequency (switch on)	V <sub>C</sub> = V <sub>DD</sub> = 5\ on 0V), R <sub>L</sub> = 1		s(p-p) = 5V (sine wa	ave centered	40	)	MHz	
OISO	-50-dB feedthrough frequency (switch off)	V <sub>C</sub> = V <sub>DD</sub> = 5\ on 0V), R <sub>L</sub> = 1		s(p-p) = 5V (sine wa	ave centered	1.25	5	MHz	
				T <sub>A</sub> = -55°C		-0.1	0.1		
		V <sub>DD</sub> = 18V		T <sub>A</sub> = -40°C		-0.1	0.1		
is	Input/Output Leakage Current V <sub>C</sub> = 0V	$V_C = 0V$ $V_{is} = 18V, V_{os}$				0.000		μA	
		$V_{is} = 0V, V_{os} =$		T <sub>A</sub> = 85°C		-1	1		
			T <sub>A</sub> =			-1	1		
XTALK	-50-dB crosstalk frequency	V <sub>C</sub> = V <sub>DD</sub> = 5\ on 0V), R <sub>L</sub> = 1		s(p-p) = 5V (sine wa	ave centered	0.9	)	MHz	

Product Folder Links: CD4016B



## 4.5 Electrical Characteristics (continued)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5V$ , and  $R_L = 100\Omega$ , (unless otherwise noted)<sup>(1)</sup>

	PARAMETER		TEST C	ONDITIONS	MIN	TYP	MAX	UNIT
		$V_C = V_{DD}, V_{SS}$	V <sub>DD</sub> = 5V			40	100	
		= GND V <sub>IS</sub> = Square	V <sub>DD</sub> = 10V			20	40	
t <sub>pd</sub>	Propagation delay	Wave 0 to $V_{DD}$ , $C_L = 50$ pF, $R_L = 200$ k $\Omega$	V <sub>DD</sub> = 15V			15	30	ns
C <sub>IS</sub>	Input capacitance	V <sub>DD</sub> = 5V, VC =	V <sub>SS</sub> = -5V			4		pF
Cos	Output capacitance	V <sub>DD</sub> = 5V, VC =	= V <sub>SS</sub> = -5V			4		pF
C <sub>IOS</sub>	Feed through	V <sub>DD</sub> = 5V, VC =	= V <sub>SS</sub> = -5V			0.2		pF
				T <sub>A</sub> = -55°C			0.9	
		$ I_{is}  < 10\mu A,$ $V_{is} = V_{SS}, V_{OS}$	V = 5V	T <sub>A</sub> = -40°C			0.9	
$V_{ILC}$	Control input, low voltage (ma	$= V_{DD}$ , and $V_{is}$	$V_{DD} = 10V$	T <sub>A</sub> = 25°C			0.7	V
	$=$ $V_{DD}$ , $V_{OS}$ =	$=$ $V_{DD}$ , $V_{OS}$ $=$ $V_{SS}$	V <sub>DD</sub> = 15V	T <sub>A</sub> = 85°C			0.4	
		vss		T <sub>A</sub> = 125°C			0.4	
			V <sub>DD</sub> = 5V		3.5			V
$V_{IHC}$	Control input, high voltage	See Figure 10	See Figure 10 V <sub>DD</sub> = 10V		7			V
			V <sub>DD</sub> = 15V		11			V
I <sub>IH</sub>	Input High Lekaage		V <sub>DD</sub> = 18V			0.5	1	μA
I <sub>IL</sub>	Input Low Leakage		V <sub>DD</sub> = 18V		-1	-0.1		μA
<u></u>	Crosstalk (control input to sig output)	$\begin{array}{c} V_C = 10V\\ \text{(square}\\ \text{nal} & \text{wave), } t_r \text{, } t_f = \\ 20\text{ns, } R_L = \\ 10k\Omega \ V_{DD} = \\ 10V \end{array}$	V <sub>DD</sub> = 10V			50		mV
		$t_{r}$ , $t_{f} = 20 \text{ns}$	V <sub>DD</sub> = 5V			35	70	ns
	Turn-on propagation delay	$C_L = 50pF$	V <sub>DD</sub> = 10V			20	40	ns
		$R_L = 1k\Omega$	V <sub>DD</sub> = 15V			15	30	ns
	Maximum control input repetir	$\begin{aligned} & V_{IN} = V_{DD}, \ C_L \\ &= 50 \text{pF}, \ R_L = \\ 1 \text{k} \Omega & V_C = 10 \text{V} \\ \text{tion} & \text{(square wave centered on 5V), } t_r \ , t_f = \\ 20 \text{ns}, \ V_{os} = \\ 1 / 2 V_{os} \ \text{at} \\ 1 \text{kHz} \end{aligned}$	V <sub>DD</sub> = 10V			10		MHz
			I.			5		pF

Copyright © 2024 Texas Instruments Incorporated

Submit Document Feedback



## 4.5 Electrical Characteristics (continued)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5V$ , and  $R_L = 100\Omega$ , (unless otherwise noted)<sup>(1)</sup>

	PARAMETER		TEST CONDITIONS	MIN TYP MAX	UNIT	
			T <sub>A</sub> = -55°C	0.25		
			T <sub>A</sub> = -40°C	0.2		
		$V_{DD} = 5V$ $V_{is} = 0V$	T <sub>A</sub> = 25°C	0.2	mA	
		V IS	T <sub>A</sub> = 85°C	0.12		
			T <sub>A</sub> = 125°C	0.14		
			T <sub>A</sub> = -55°C	-0.25		
			T <sub>A</sub> = -40°C	-0.2		
		$V_{DD} = 5V$ $V_{is} = 5V$	T <sub>A</sub> = 25°C	-0.2	mA	
		V IS	T <sub>A</sub> = 85°C	-0.12		
			T <sub>A</sub> = 125°C	-0.14		
			T <sub>A</sub> = -55°C	0.62		
			T <sub>A</sub> = -40°C	0.5		
		$V_{DD} = 10V$ $V_{is} = 0V$	T <sub>A</sub> = 25°C	0.5	mA	
		V IS	T <sub>A</sub> = 85°C	0.3		
	Consider the second and second		T <sub>A</sub> = 125°C	0.35		
I <sub>IS</sub>	Switch input current		T <sub>A</sub> = -55°C	-0.62		
			T <sub>A</sub> = -40°C	-0.5		
		$V_{DD} = 10V$ $V_{is} = 10V$	T <sub>A</sub> = 25°C	-0.5	mA	
		V IS TO V	T <sub>A</sub> = 85°C	-0.3		
			T <sub>A</sub> = 125°C	-0.35		
			T <sub>A</sub> = -55°C	1.8		
			T <sub>A</sub> = -40°C	1.4		
		$V_{DD} = 15V$ $V_{is} = 0V$	T <sub>A</sub> = 25°C	1.5	mA	
		V IS	T <sub>A</sub> = 85°C	1		
			T <sub>A</sub> = 125°C	1.1		
			T <sub>A</sub> = -55°C	-1.8		
			T <sub>A</sub> = -40°C	-1.4		
		$V_{DD} = 15V$ $V_{is} = 15V$	T <sub>A</sub> = 25°C	-1.5	mA	
		V <sub>IS</sub>	T <sub>A</sub> = 85°C	-1		
			T <sub>A</sub> = 125°C	-1.1		
		V <sub>DD</sub> = 5V V <sub>is</sub> = 0V		0.4	V	
		V <sub>DD</sub> = 5V V <sub>is</sub> = 5V		4.6	V	
\ <i>/</i>	Switch output valtees	V <sub>DD</sub> = 10V V <sub>is</sub> = 0V		0.5	V	
V <sub>OS</sub>	OS Switch output voltage	V <sub>DD</sub> = 10V V <sub>is</sub> = 10V		9.5	V	
		$V_{DD} = 15V$ $V_{is} = 0V$		1.5	٧	
		V <sub>DD</sub> = 15V V <sub>is</sub> = 15V		13.5	V	

<sup>(1)</sup> Peak-to-Peak voltage symmetrical about  $(V_{DD}-V_{EE})$  / 2.

Product Folder Links: CD4016B



## **4.6 Electrical Characteristics**

		TEST CONDIT	TIONS		LIMITS AT INDICATED TEMPERATURES (°C)						
CHARACTERISTIC			V <sub>IN</sub> (V) V <sub>DD</sub> (V)						+25		UNIT
			V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	TYP	MAX	
			0,5	5	025	0.25	7.5	7.5	0.01	0.25	
Quiescent Device			0,10	10	0.5	0.5	15	15	0.01	0.5	μA
Current, I <sub>DD</sub>			0,15	15	1	1	30	30	0.01	1	μΑ
			0,20	20	5	5	150	150	0.02	5	
Signal Inputs (V <sub>is</sub> ) and 0	Output (V <sub>os</sub> )		•					•			•
	V <sub>C</sub> =V <sub>DD</sub>	V <sub>is</sub> =V <sub>DD</sub> or V <sub>SS</sub>		10	600	610	840	960	-	660	
On-State	R <sub>L</sub> =10kΩ Returned to	V <sub>is</sub> =4.75 to 5.75V		10	1870	1900	2380	2600	-	2000	Ω
Resistance, r <sub>on</sub> MAX	V <sub>DD</sub> -V <sub>SS</sub>	$V_{is}$ = $V_{DD}$ or $V_{SS}$		15	360	370	520	600	-	400	122
	2	V <sub>is</sub> =7.25 to 7.75V		15	775	790	1080	1230	_	850	
ΔOn-State				5	-	-	-	_	15	-	
Resistance Between	$R_L=10k\Omega$ , $V_C=V_{DD}$			10	-	-	-	-	10	-	Ω
Any 2 Switches, Δr <sub>on</sub>				15	_	_	-	-	5	-	
Total Harmonic	$V_C = V_{DD} = 5V$ , $V_{SS} = -5V$ , $V_{is(p-p)} = 5V$ (Sine wave centered of			on 0V) $R_L = 10k\Omega$ ,					0.4		%
Distortion, THD	f <sub>is</sub> = 1kHz sine wave	(			_	_	_	_	0.4	_	70
-3dB Cutoff Frequency (Switch on)	V <sub>C</sub> =V <sub>DD</sub> =5V, V <sub>SS</sub> =-5V,	$V_{is(p-p)}$ (Sine wave o	centered on 0V)	R <sub>L</sub> =1kΩ,	-	_	_	-	40	-	MHz
-50dB Feed-through Frequency (Switch off)	$V_C = V_{SS} = -5V$ , $V_{is(p-p)} = 5V$ (Sine wave centered on 0V) $R_L = 1 \text{ lk}\Omega$			1 ΙκΩ	_	_	_	-	1.25	-	MHz
Input/Output	V <sub>C</sub> = 0V										
Leakage Current	$V_{is} = 18V, V_{OS} = 0V;$			18	±0.1	±0.1	±1	±1	10 <sup>-4</sup>	±0.1	μΑ
(Switch off) I <sub>is</sub> MAX	$V_{is} = 0V, V_{OS} = 18V$										
	$V_{C}(A) = V_{DD} = +5V, V_{C}(I)$	$V_{\rm C}({\rm B}) = V_{\rm SS} = -5 {\rm V}, \ V_{\rm is}({\rm A}) = 5 {\rm V}_{\rm p-p}, \ 50 {\rm \Omega}$									
-50dB Crosstalk Frequency	source				_	_	_	_	0.9	-	MHz
Troquonoy	R <sub>L</sub> = 1kΩ										
	$R_1 = 200k\Omega$			5	_	-	-	-	40	100	
Propagation	$V_C = V_{DD}, V_{SS} = GND,$	C <sub>L</sub> = 50pF		10	_	-	-	-	20	40	
Delay (Signal Input to	V <sub>is</sub> = Square Wave 0 to								1		ns
Signal Output) t <sub>pd</sub>	t <sub>r</sub> , t <sub>f</sub> = 20ns			15	-	-	-	-	15	30	
Capacitance:					_	_	_	_	4	_	
Input, C <sub>is</sub> Output, C <sub>OS</sub>	V <sub>DD</sub> = +5V				_	_	_	_	4	_	pF
Feed-through, C <sub>ios</sub>	V <sub>C</sub> =V <sub>SS</sub> =-5V				_	_	_	_	0.2	_	-
Control (V <sub>C</sub> )									1		
	I <sub>is</sub>  < 10 μA										
Control Input Low Voltage, V <sub>ILC</sub> (MAX)	$V_{is} = V_{SS}, V_{OS} = V_{DD}$ ar	nd V <sub>is</sub> = V <sub>DD</sub> , V <sub>OS</sub> =	$V_{SS}$	5,10, 15	0.9	0.9	0.4	0.4	-	0.7	V
				5					3	.5 (Min.)	
Control Input High Voltage, V <sub>IHC</sub>	See Figure 4-8			10						7 (Min.)	V
voltage, v <sub>IHC</sub>				15						11 (Min.)	
	Input Current, I <sub>IN</sub> (MAX)	V <sub>is</sub> □ V <sub>DD</sub>									
Input Current, I <sub>IN</sub> (MAX)	nput Current, I <sub>IN</sub> $V_{DD} - V_{SS} = 18V$			18	±0.1	±0.1	±1	±1	±10 <sup>-5</sup>	±0.1	μΑ
(Will DA)	V <sub>CC</sub> □ V <sub>DD</sub> - V <sub>SS</sub>										
	V <sub>C</sub> = 10V (Sq. Wave)										
Crosstalk (Control Input to Signal Output)	t <sub>r</sub> , t <sub>f</sub> = 20ns			10	_	_	_	_	50	_	mV
pat to Signal Output)	$R_L = 10k\Omega$										
	Turn-On Propagation D	elay t <sub>r</sub> , t <sub>f</sub> = 20ns		5	_	-	-	-	35	70	
Turn-On Propagation	C <sub>L</sub> = 50pF			10	_	-	-	-	20	40	ns
Delay	R <sub>L</sub> = 1kΩ			15	_	_	-	1_	15	30	



#### 4.6 Electrical Characteristics (continued)

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						
		V <sub>IN</sub> (V)	V <sub>DD</sub> (V)					+25		UNITS
		VIN (V)		-55	-40	+85	+125	TYP	MAX	
Repetition Rate	Maximum Control Input Repetition Rate $V_{is} = V_{DD} < V_{SS} = \text{GND},  R_L = 1 \text{k}\Omega \text{ to GND},  C_L = 50 \text{pF},  V_C = 10 \text{V}(\text{Square wave centered on 5V})}$ $t_r,  t_f = 20 \text{ns},  V_{OS} = \frac{1}{2}  V_{OS} \text{ at 1kHz}$		10	_	_	_	_	10	_	MHz
Input Capacitance, C <sub>IN</sub>				-	_	_	_	5	7.5	μF

### 4.7 Typical Characteristics

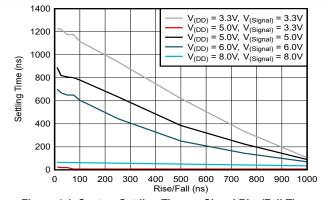


Figure 4-1. System Settling Time vs Signal Rise/Fall Time

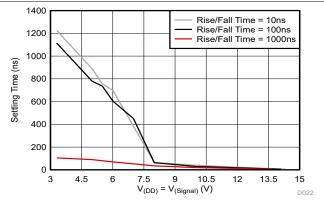


Figure 4-2. System Settling Time vs Signal Voltage

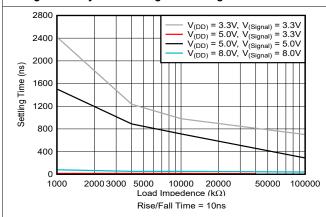


Figure 4-3. System Settling Time vs Signal Voltage

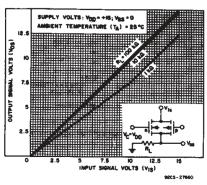


Figure 4-4. On-state Characteristics for 1 of 4 Switches with vDD = +15V,  $v_{SS}$  = 0V.

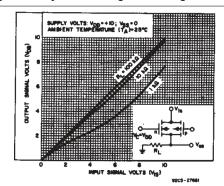
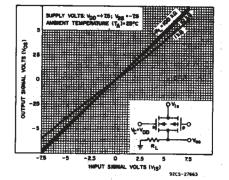


Figure 4-5. On-state Characteristics for 1 of 4 Switches with v<sub>DD</sub> | Figure 4-6. On-state Characteristics for 1 of 4 Switches with v<sub>DD</sub> =+10V,  $v_{SS} = 0V$ .

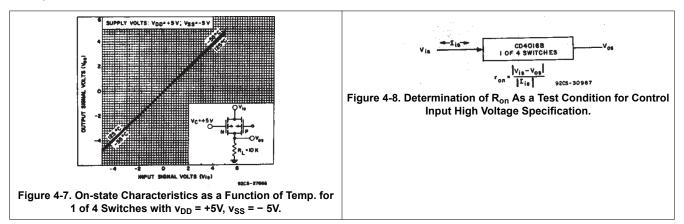


= +7.5V,  $v_{SS} = -7.5V$ .

Submit Document Feedback

Copyright © 2024 Texas Instruments Incorporated

## 4.7 Typical Characteristics (continued)



#### **5 Parameter Measurement Information**

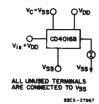


Figure 5-1. Off-state Switch Input or Output Leakage Current Test Circuit.

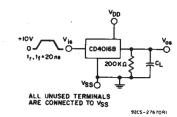


Figure 5-3. Propagation Delay Time Signal Input (v<sub>IS</sub>) To Signal Output (v<sub>OS</sub>)

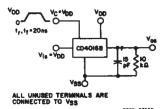


Figure 5-2. Test Circuit for Square-wave Response.

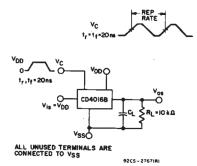


Figure 5-4. MAX Control-input Repetition Rate.



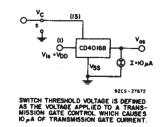


Figure 5-5. Switch Threshold Voltage.

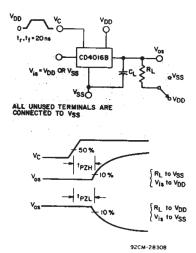


Figure 5-6. Turn-On Propagation Delay-control Input.

Submit Document Feedback

Product Folder Links: CD4016B

12

## 6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

#### **6.1 Documentation Support**

#### 6.1.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 6.1.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 6.1.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 6.1.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 6.1.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2024) to Revision E (August 2024)	Page
Added Settling Time plots	10
Changes from Revision C (September 2003) to Revision D (May 2024)	Page
Increased IDD max/typ for the lower Temperature cases	
Changed typical IIH to 0.5µA	5
Changed typical IIL to -0.1µA	5

### 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2024 Texas Instruments Incorporated

8-Nov-2025

www.ti.com

#### **PACKAGING INFORMATION**

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
						(4)	(5)		
5962-9064001CA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A
CD4016BE	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4016BE
CD4016BE.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4016BE
CD4016BEE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4016BE
CD4016BF	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4016BF
CD4016BF.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4016BF
CD4016BF3A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A
CD4016BF3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A
CD4016BM	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	CD4016BM
CD4016BM96	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM
CD4016BM96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM
CD4016BMT	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	CD4016BM
CD4016BNSR	NRND	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016B
CD4016BNSR.A	NRND	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016B
CD4016BPW	NRND	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B
CD4016BPW.A	NRND	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B
CD4016BPWR	NRND	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B
CD4016BPWR.A	NRND	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B

 $<sup>^{(1)}</sup>$  Status: For more details on status, see our product life cycle.

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

## **PACKAGE OPTION ADDENDUM**

www.ti.com 8-Nov-2025

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF CD4016B, CD4016B-MIL:

Catalog: CD4016B

Military: CD4016B-MIL

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

### TAPE AND REEL INFORMATION





	-
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4016BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4016BNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4016BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

www.ti.com 24-Jul-2025



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4016BM96	SOIC	D	14	2500	353.0	353.0	32.0
CD4016BNSR	SOP	NS	14	2000	353.0	353.0	32.0
CD4016BPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4016BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4016BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4016BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4016BPW	PW	TSSOP	14	90	530	10.2	3600	3.5
CD4016BPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5



SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



## **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



#### NOTES:

- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SMALL OUTLINE PACKAGE



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025