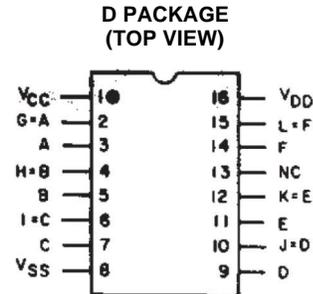


CMOS HEX BUFFER/CONVERTER

 Check for Samples: [CD4010B-Q1](#)

FEATURES

- Qualified for Automotive Applications
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1 μ A at 18 V Over Full Package-Temperature Range:
100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V Parametric Ratings
- Latch-Up Performance Meets 100 mA per JESD 78, Class I



APPLICATIONS

- CMOS to DTL/TTL Hex Converter
- CMOS Current "Sink" or "Source" Driver
- CMOS High-to-Low Logic-Level Converter
- Multiplexer: 1-to-6 or 6-to-1

DESCRIPTION

CD4010B hex buffer/converter may be used as CMOS to TTL or DTL logic-level converters or CMOS high-sink-current drivers.

The CD4050B is the preferred hex buffer replacement for the CD4010B in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069UB hex inverter is recommended.

The CD4010B is supplied in 16-lead hermetic dual-in-line ceramic (D) packages.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	CD4010BQDRQ1	CD4010BQ

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

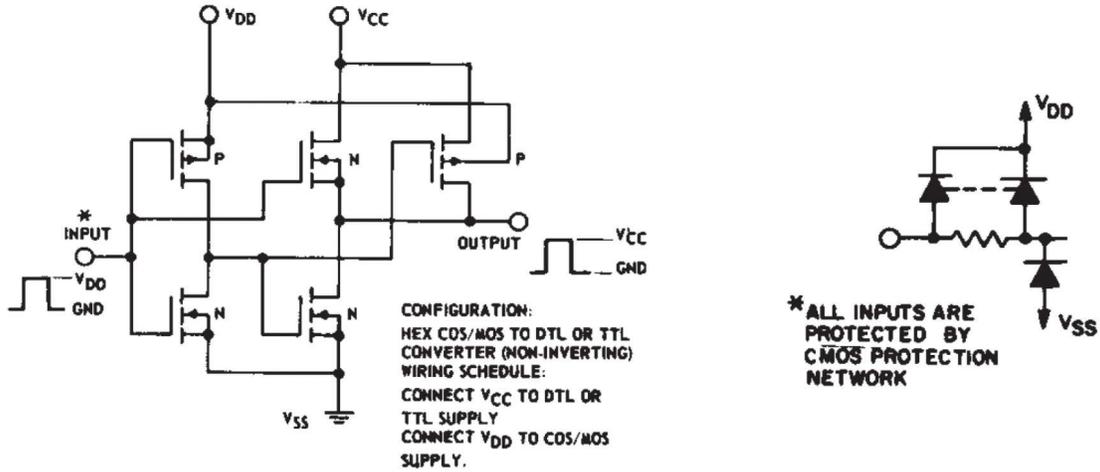
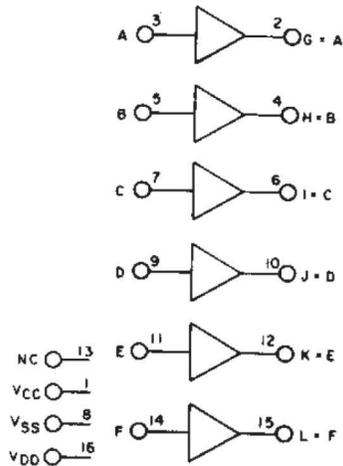


Figure 1. Schematic Diagram – One of Six Identical Stages

Functional Diagram



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{DD}	DC supply voltage range, voltages referenced to V_{SS} terminal	–0.5 to +20	V
	Input voltage range, all inputs	–0.5 to $V_{DD} + 0.5$	V
	DC input current, any one input	±10	mA
P_D	Power dissipation per package	$T_A = -40^\circ\text{C}$ to $+100^\circ\text{C}$	500
		$T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate linearly at 12 mW/°C to 200 mW
	Device dissipation per output transistor	$T_A =$ full package-temperature range (all packages types)	100
T_A	Operating temperature range	–40 to +125	°C
T_{stg}	Storage temperature range	–65 to +150	°C
	Latch-up performance per JESD 78, Class I	100	mA
ESD	Electrostatic discharge rating ⁽²⁾	Human-body model (HBM)	500
		Machine model (MM)	100
		Charged-Device Model (CDM)	1000

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Tested in accordance with AEC-Q100.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{DD}	Supply voltage range ⁽¹⁾	3	18	V
V_{CC}		3	V_{DD}	
V_I	Input voltage range	V_{CC}	V_{DD}	V

(1) The CD4010B has high-to-low level voltage conversion capability, but not low-to-high level; therefore, it is recommended that $V_{DD} > V_I > V_{CC}$.

STATIC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNIT
	V _O	V _{IN}	V _{DD}	-40	+85	+125	+25			
							MIN	TYP	MAX	
I _{DD} Max Quiescent device current		0, 5	5	1	30	30	0.02			μA
		0, 10	10	2	60	60	0.02			
		0, 15	15	4	120	120	0.02			
		0,20	20	20	600	600	0.04			
I _{OL} Min Output low (sink) current	0.4	0, 5	4.5	3.1	2.1	1.8	2.6	3.4		mA
	0.4	0, 5	5	3.6	2.4	2.1	3	4		
	0.5	0, 10	10	9.6	6.4	5.6	8	10		
	1.5	0, 15	15	40	19	16	24	36		
I _{OH} Min Output high (source) current	4.6	0, 5	5	-0.23	-0.18	-0.15	-0.2	-0.4		mA
	2.5	0, 5	5	-0.9	-0.65	-0.58	-0.8	-1.6		
	9.5	0, 10	10	-0.5	-0.38	-0.33	-0.45	-0.9		
	13.5	0, 15	15	-1.6	-1.25	-1.1	-1.5	-3		
V _{OL} Max Output voltage: Low-level		0, 5	5	0.05			0 0.05		V	
		0, 10	10	0.05			0 0.05			
		0, 15	15	0.05			0 0.05			
V _{OH} Min Output voltage: High-level		0, 5	5	4.95			4.95	5		V
		0, 10	10	9.95			9.95	10		
		0, 15	15	14.95			14.95	15		
V _{IL} Max Input low voltage	0.5		5	1.5			1.5		V	
	1		10	3			3			
	1.5		15	4			4			
V _{IH} Min Input high voltage	4.5		5	3.5			3.5		V	
	9		10	7			7			
	13.5		15	11			11			
I _{IN} Max Input current		0, 18	18	±0.1	±1	±1	±10 ⁻⁵		±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS
 $T_A = 25^\circ\text{C}$, Input $t_r/t_f = 20\text{ ns}$, $C_L = 50\text{ pf}$, $R_L = 200\text{ k}\Omega$

PARAMETER	TEST CONDITIONS			LIMITS ALL PKGS		UNIT
	V_{DD} (V)	V_I (V)	V_{CC} (V)	TYP	MAX	
t_{PLH} Propagation delay time: low-to-high	5	5	5	100	200	ns
	10	10	10	50	100	
	10	10	5	50	100	
	15	15	15	35	70	
	15	15	5	35	70	
t_{PHL} Propagation time: high-to-low	5	5	5	65	130	ns
	10	10	10	35	70	
	10	10	5	30	70	
	15	15	15	25	50	
	15	15	5	20	40	
t_{TLH} Transition time: low-to-high	5	5	5	150	350	ns
	10	10	10	75	150	
	15	15	15	55	110	
t_{THL} Transition time: high-to-low	5	5	5	35	90	ns
	10	10	10	20	45	
	15	15	15	15	40	
C_{IN} Input capacitance				5	7.5	pF

TYPICAL CHARACTERISTICS

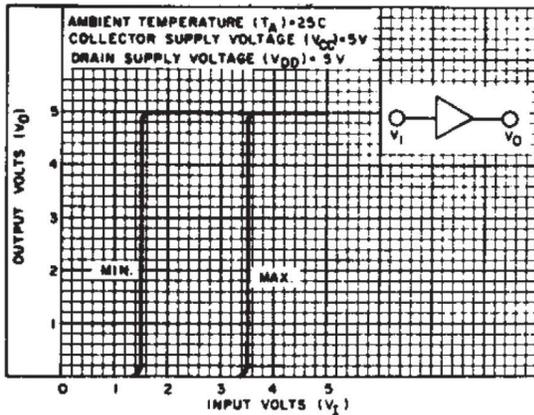


Figure 2. Minimum and Maximum Voltage Transfer Characteristics ($V_{DD} = 5\text{ V}$)

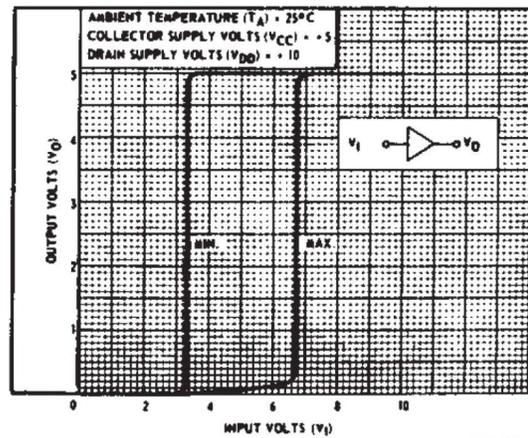


Figure 3. Minimum and Maximum Voltage Transfer Characteristics ($V_{DD} = 10\text{ V}$)

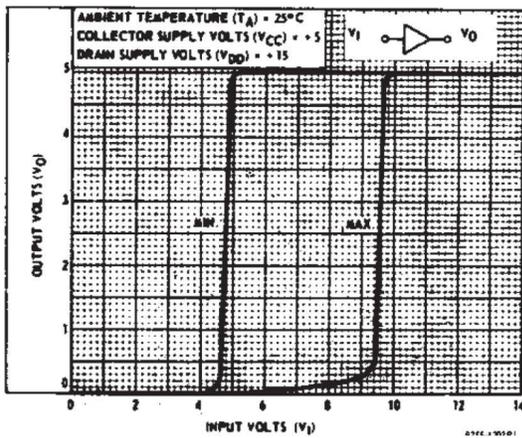


Figure 4. Minimum and Maximum Voltage Transfer Characteristics ($V_{DD} = 15\text{ V}$)

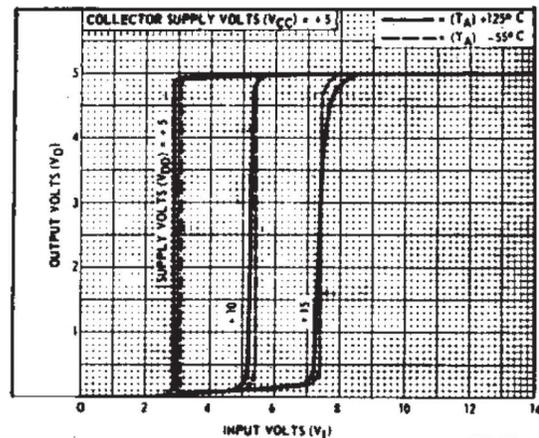


Figure 5. Typical Voltage Transfer Characteristics as a Function of Temperature

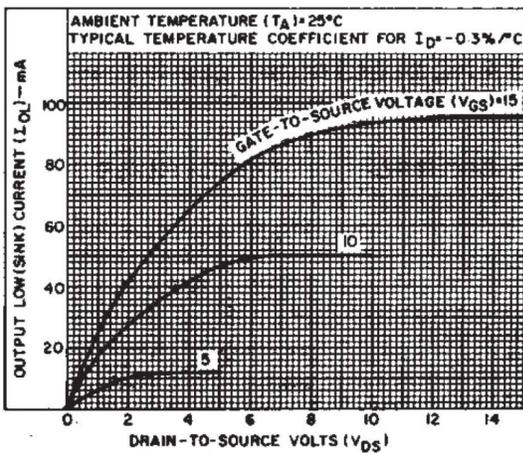


Figure 6. Typical Output Low (Sink) Current Characteristics

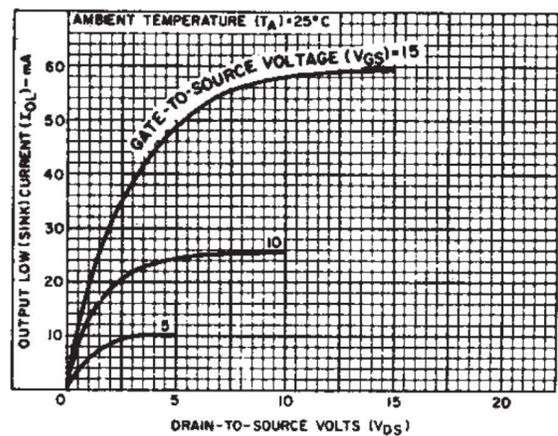


Figure 7. Minimum Output Low (Sink) Current Characteristics

TYPICAL CHARACTERISTICS (continued)

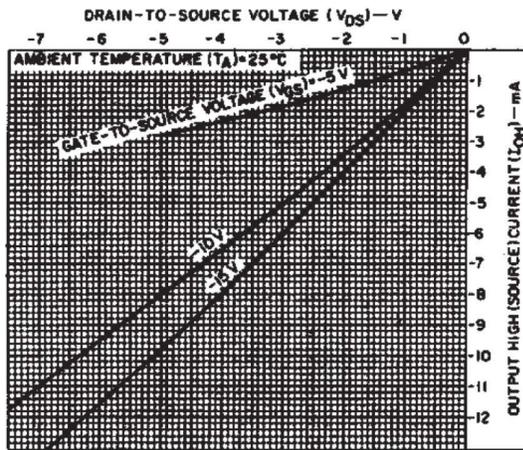


Figure 8. Typical Output High (Source) Current Characteristics

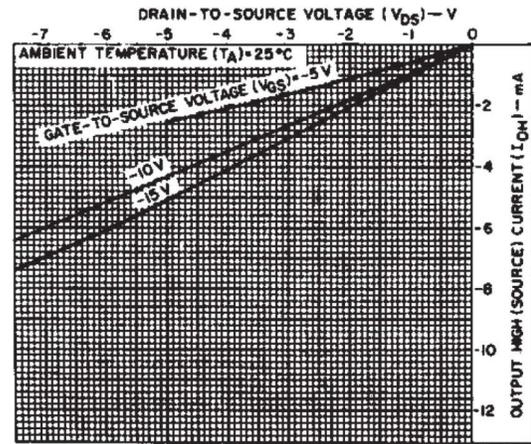


Figure 9. Minimum Output High (Source) Current Characteristics

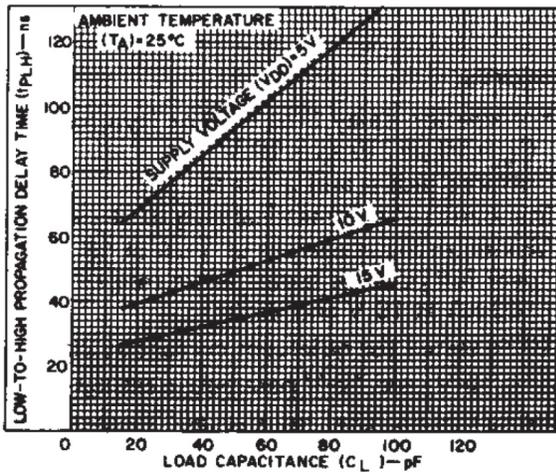


Figure 10. Typical Low-to-High Propagation Delay Time vs Load Capacitance

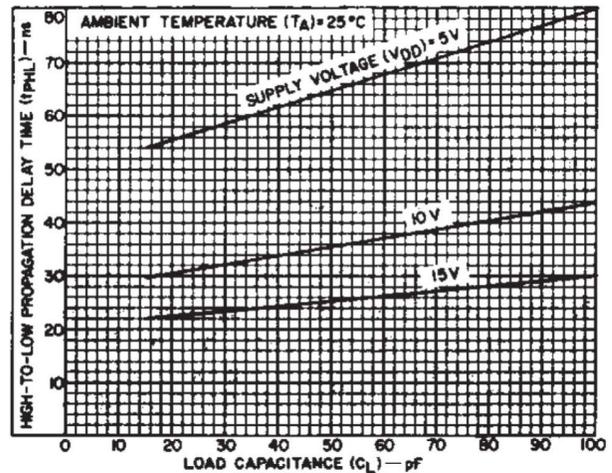


Figure 11. Typical High-to-Low Propagation Delay Time vs Load Capacitance

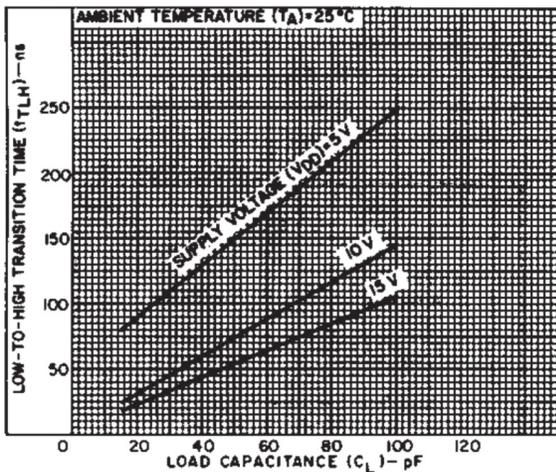


Figure 12. Typical Low-to-High Transition Time vs Load Capacitance

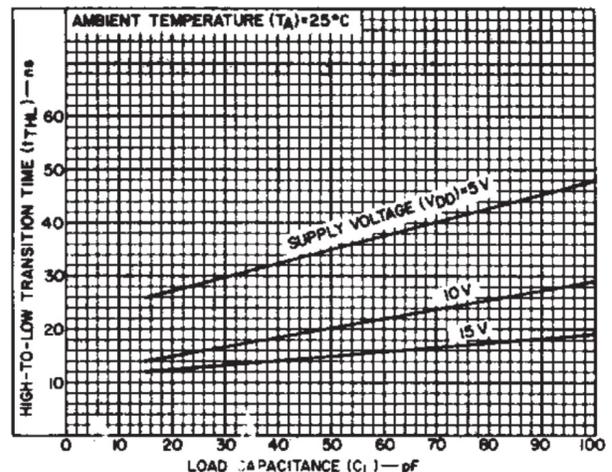


Figure 13. Typical High-to-Low Transition Time vs Load Capacitance

TYPICAL CHARACTERISTICS (continued)

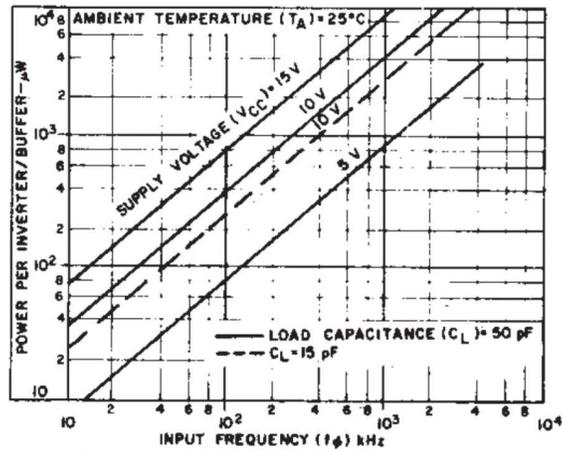


Figure 14. Typical Dissipation Characteristics

PARAMETER MEASUREMENT INFORMATION

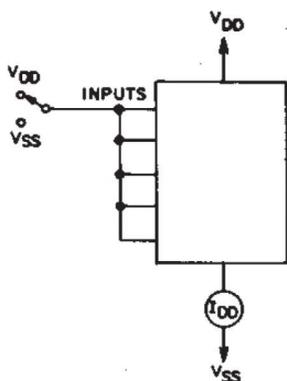


Figure 15. Quiescent Device Current Test Circuit

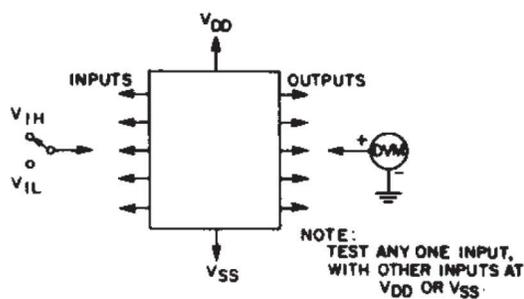


Figure 16. Noise Immunity Test Circuit

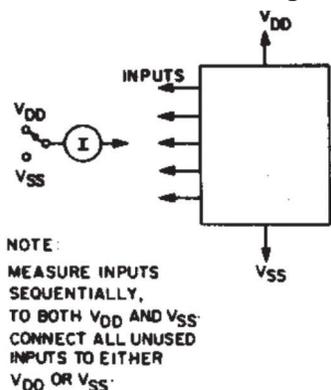
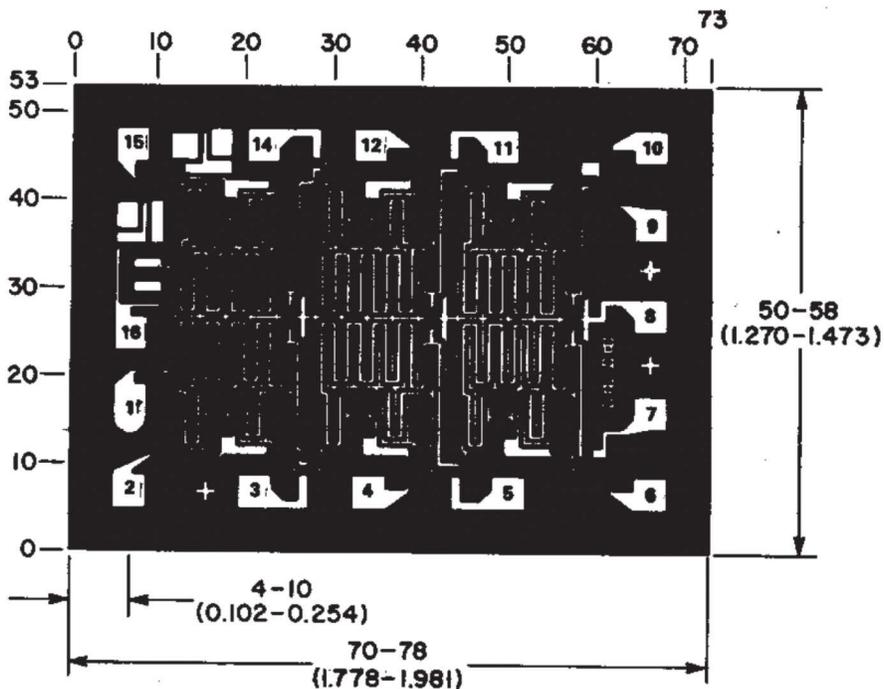


Figure 17. Input Current Test Circuit



Note: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduation are in mils (10^{-3} inch).

Figure 18. Dimensions and Layout

REVISION HISTORY

Changes from Original (March 2010) to Revision A	Page
• Changed STATIC ELECTRICAL CHARACTERISTICS table to correct typos and misplaced data	4

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4010BQDRQ1	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4010BQ
CD4010BQDRQ1.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4010BQ

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4010B-Q1 :

- Catalog : [CD4010B](#)

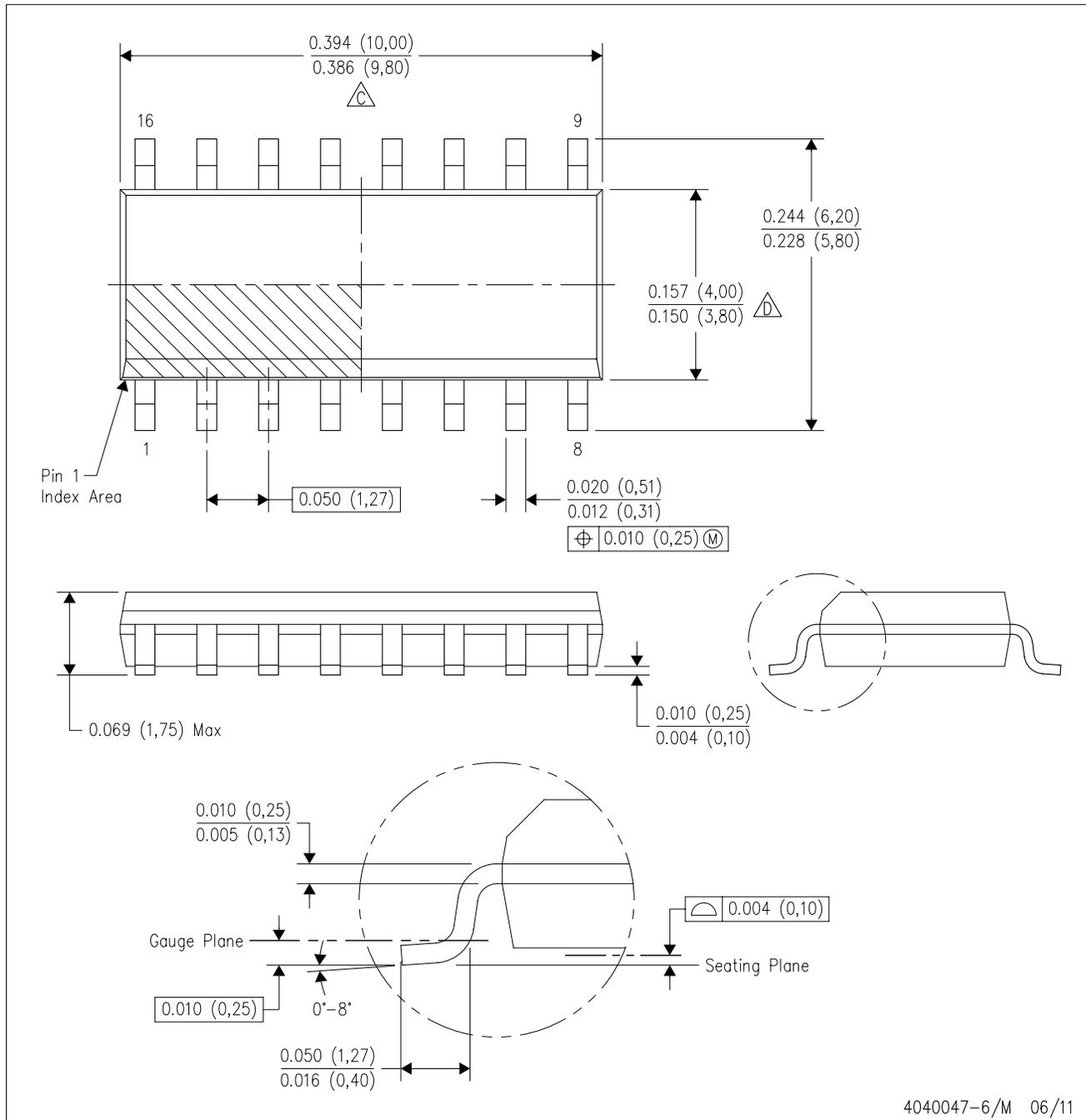
- Military : [CD4010B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated