CC2592 2.4-GHz Range Extender

1 Introduction

1.1 Features

- Seamless Interface to 2.4-GHz Low-Power RF Devices from Texas Instruments
- +22-dBm Output Power
- 3-dB Typical Improved Sensitivity on CC2520, CC253X, and CC85XX
- Very Few External Components
  - Integrated Switches
  - Integrated Matching Network
  - Integrated Balun
  - Integrated Inductors
  - Integrated PA
  - Integrated LNA
- Digital Control of LNA Gain by HGM Terminal
- 100 nA in Power Down (LNA_EN = PA_EN = 0)
- Low-Transmit Current Consumption
  - 155 mA at 3 V for +22 dBm, PAE = 34%
- Low-Receive Current Consumption
  - 4.0-mA for High-Gain Mode
  - 1.9-mA for Low-Gain Mode
- 4.7-dB LNA Noise Figure, Including T/R Switch and External Antenna Match
- RoHS Compliant 4-mm × 4-mm QFN-16 Package
- 2.0-V to 3.7-V Operation
- –40°C to +125°C Operation

1.2 Applications

- All 2.4-GHz ISM Band Systems
- Wireless Sensor Networks
- Wireless Industrial Systems
- IEEE 802.15.4 and ZigBee® Metering Systems
- IEEE 802.15.4 and ZigBee Gateways
- Wireless Consumer Systems
- Wireless Audio Systems

1.3 Description

The CC2592 device is a cost-effective and high-performance RF front end for low-power and low-voltage 2.4-GHz wireless applications.

The CC2592 device is a range extender for all CC25XX 2.4-GHz low-power RF transceivers, transmitters, and system-on-chip products from Texas Instruments.

To increase the link budget, the CC2592 device provides a power amplifier for increased output power and an LNA with a low-noise figure for improved receiver sensitivity.

The CC2592 device provides a very small size, high-output power RF design with its 4-mm × 4-mm QFN-16 package.

The CC2592 device contains PA, LNA, switches, RF-matching, and balun for simple design of high-performance wireless applications.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

1.4 Functional Block Diagram

Figure 1-1 shows a simplified block diagram of the CC2592 device.

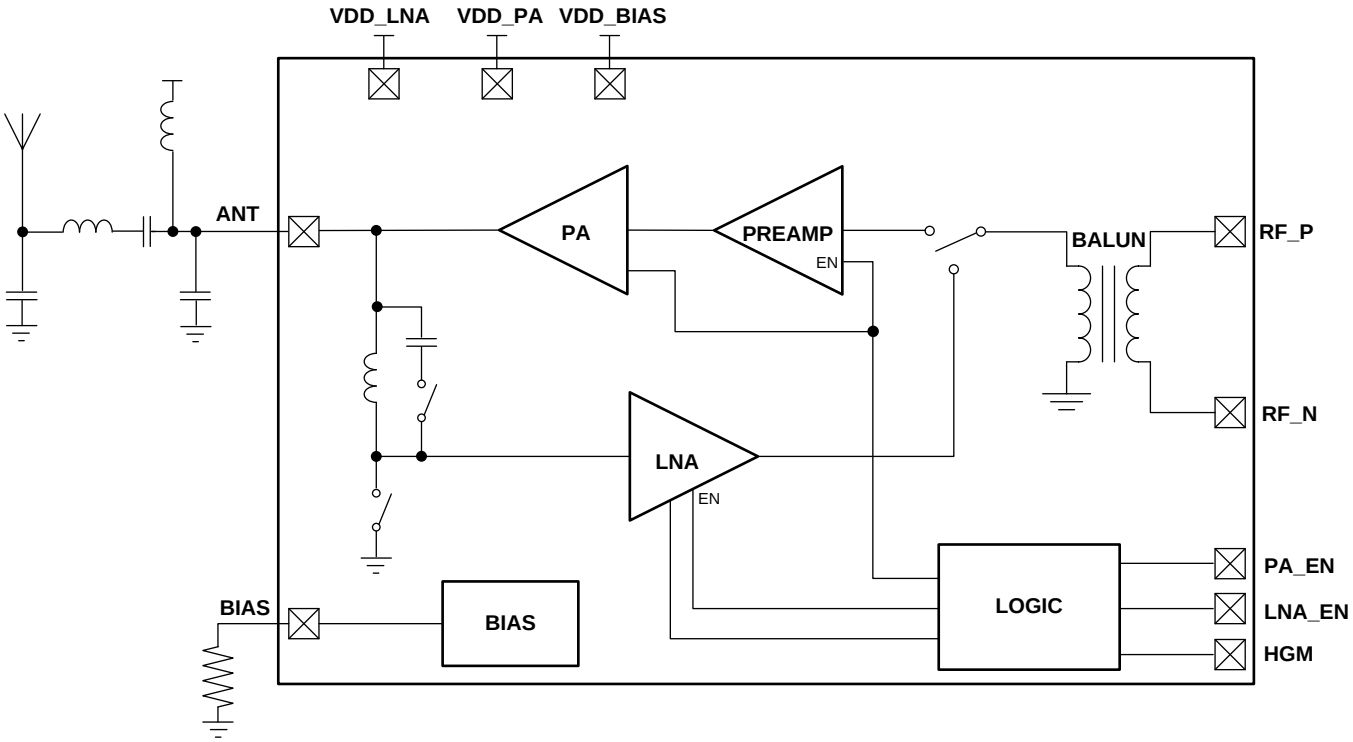

Figure 1-1. CC2592 Simplified Block Diagram

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Revision History

Date	Literature Number	Changes
February 2014	SWRS159	Initial release

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2 Device Characteristics

2.1 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Conditions	Value	Unit
Supply voltage	All supply terminals must have the same voltage	–0.3 to 3.8	V
Voltage on any digital terminal		–0.3 to VDD+0.3, max 3.8	V
Input RF level		+10	dBm

2.2 Handling Ratings

Under no circumstances must the handling ratings be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Conditions	Value	Unit
Storage temperature range		–50 to 150	°C
ESD	Human Body Model	2000	V
	Charge Device Model	1000	V

2.3 Recommended Operating Conditions

The operating conditions for the CC2592 device are listed below.

Parameter	Conditions	Min	Max	Unit
Ambient temperature range		–40	125	°C
Operating supply voltage		2.0	3.7	V
Operating frequency range		2400	2483.5	MHz

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2.4 Electrical Characteristics

T_c = 25°C, VDD = 3.0 V, f_{RF} = 2440 MHz (unless otherwise noted). Measured on CC2592EM reference design including external matching components.

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive current, high-gain mode	HGM = 1		4		mA
Receive current, low-gain mode	HGM = 0		1.9		mA
Transmit current	P_{OUT} = 20 dBm		123		mA
	P_{OUT} = 22 dBm		155		
Transmit current	No input signal		50		mA
Power down current	EN = 0		0.1	0.3	µA
High-input level (control terminals)	PA_EN, LNA_EN, HGM	1.3		Vdd	V
Low-input level (control terminals)	PA_EN, LNA_EN, HGM			0.3	V
Power down - Receive mode switching time			1		µs
Power down - Transmit mode switching time			1		µs
RF Receive					
Gain, high-gain mode	HGM = 1		11		dB
Gain, low-gain mode	HGM = 0		6		dB
Gain variation over frequency	2400 to 2483.5 MHz, HGM = 1		2		dB
Gain variation over power supply	2.0 V to 3.7 V, HGM = 1		1.5		dB
Gain variation over temperature	–40°C to 85°C, HGM = 1		1.7		dB
Gain variation over temperature	85°C to 125°C, HGM = 1		1		dB
Noise figure, high-gain mode	HGM = 1, including internal T/R switch and external antenna match		4.7		dB
Input 1-dB compression, high-gain mode	HGM = 1		–18		dBm
Input IP3, high-gain mode	HGM = 1		–9		dBm
Input reflection coefficient, S11	HGM = 1, measured at antenna port		–15		dB
RF Transmit					
Gain			24		dB
Output power, P_{OUT}	P_{IN} = 0.0 dBm		20.3		dBm
	P_{IN} = 4.0 dBm		21.9		
Power added efficiency, PAE	P_{OUT} = 22 dBm		34		%
Output 1-dB compression			15		dBm
Output power variation over frequency	2400 to 2483.5 MHz, P_{IN} = 4 dBm		0.5		dB
Output power variation over power supply	2.0 V to 3.7 V, P_{IN} = 4 dBm		3.8		dB
Output power variation over temperature	–40°C to 125°C, P_{IN} = 4 dBm		1.7		dB
Second harmonic power	FCC requirement			–41.2	dBm
Third harmonic power	FCC requirement			–41.2	dBm
VSWR	No damage	20:1			
	Stability	7.5:1			

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3 Device Information

3.1 Terminal and I/O Configuration

Figure 3-1 and Table 3-1, provide the terminal layout and description for the CC2592 device.

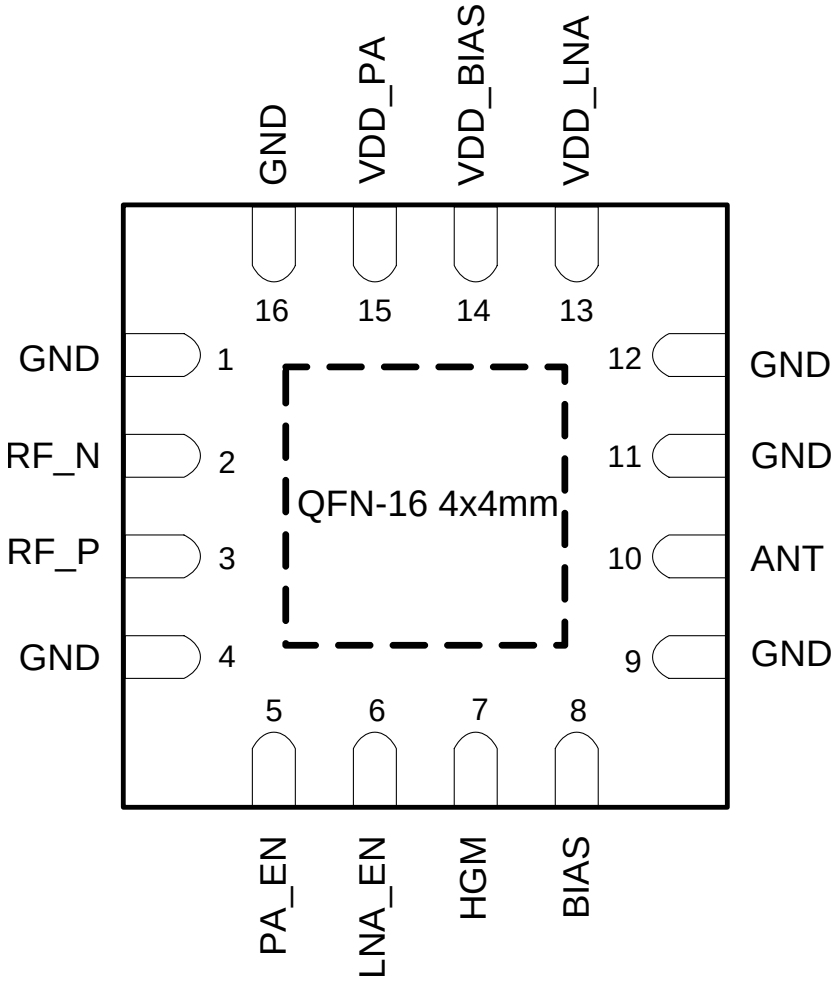

Figure 3-1. Terminal Top View

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Table 3-1. Terminal Functions

Terminal		Type	Description
No.	Name		
–	GND	Ground	The exposed die attach pad must be connected to a solid ground plane. See CC2592EM reference design for the recommended layout.
1, 4, 9, 11, 12, 16	GND	Ground	Ground connections. Only terminals 9, 11, and 12 should be shorted to the die attach pad on the top PCB layer.
2	RF_N	RF	RF interface toward CC25xx device
3	RF_P	RF	RF interface toward CC25xx device
5	PA_EN	Digital input	Digital control terminal. See Table 9-1 for details.
6	LNA_EN	Digital input	Digital control terminal. See Table 9-1 or details.
7	HGM	Digital input	Digital control terminal HGM = 1 → Device in High Gain Mode HGM = 0 → Device in Low Gain Mode
8	BIAS	Analog	Biasing input. Resistor between this node and ground sets bias current for PA and LNA.
10	ANT	RF	Antenna interface
13	VDD_LNA	Power	2.0- to 3.7-V power
14	VDD_BIAS	Power	2.0- to 3.7-V power
15	VDD_PA	Power	2.0- to 3.7-V power

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4 Sensitivity Improvement Example

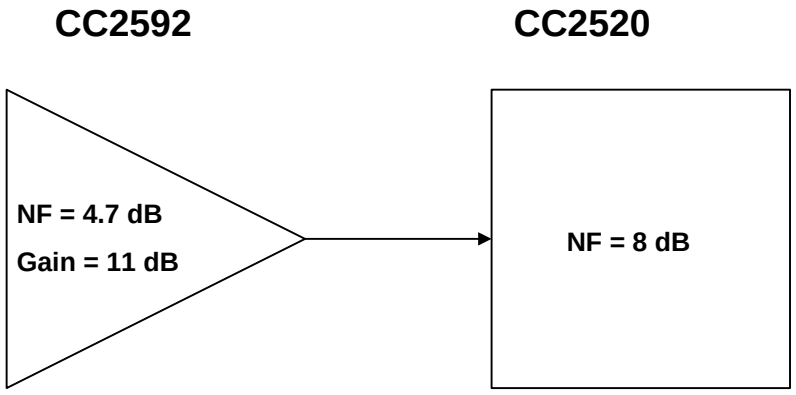

Figure 4-1.

The noise factor of a system consisting of the CC2592 device and a CC2520 device, as seen in Figure 4-1 is given by:

$$F = F_1 + \frac{F_2 - 1}{G_1} = 10^{\frac{4.7}{10}} + \frac{10^{\frac{8}{10}} - 1}{10^{\frac{11}{10}}} = 3.37 \quad (1)$$

The noise figure is:

$$NF = 10\log(F) = 10\log(3.37) = 5.28 \text{ dB} \quad (2)$$

The noise figure is reduced from 8 dB for the CC2520 standalone to 5.28 dB for the CC2592 and CC2520 device combination, leading to a 2.72-dB theoretical improvement in sensitivity.

In practice, tests on the CC2592 and CC25XX devices show around 3-dB improvement in sensitivity. For the CC2538 and CC2592 devices, the improvement is almost 4 dB (approximately –97 dBm to –101 dBm)

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5 CC2592EM Evaluation Module

Figure 5-1 shows an evaluation module circuit of the CC2592 device.

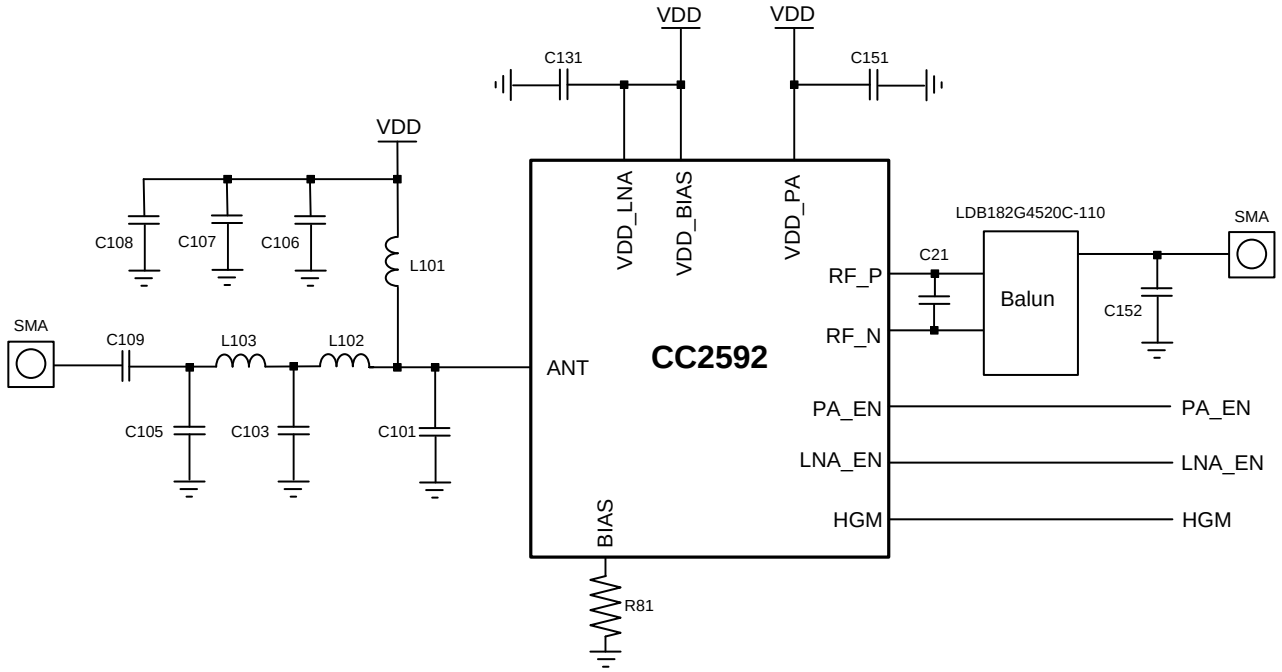

Figure 5-1. CC2592 Evaluation Module

Table 5-1 lists the materials in the CC2592 evaluation module circuit.

Table 5-1. List of Materials

Device	Function	Value
L101	PA bias inductor	4.7 nH, Multilayer chip inductor
L102	Part of antenna match	1 nH, Multilayer chip inductor
L103	Part of antenna match	1.8 nH, Multilayer chip inductor
C101	Part of antenna match	2.2-pF 0402 Chip capacitor
C103	Part of antenna match	2.2-pF 0402 Chip capacitor
C105	Part of antenna match	0.1-pF 0402 Chip capacitor
C106	Decoupling	12-pF 0402 Chip capacitor
C107	Decoupling	1-nF 0402 Chip capacitor
C108	Decoupling	1-µF 0402 Chip capacitor
C109	DC block	18-pF 0402 Chip capacitor
C21	Balun matching capacitor	0.2-pF 0402 Chip capacitor
C152	Balun matching capacitor	0.3-pF 0402 Chip capacitor
C131	Decoupling	1-nF 0402 Chip capacitor
C151	Decoupling	12-pF 0402 Chip capacitor
R81	Bias resistor	3.9 kΩ, 0402 resistor

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6 Typical Characteristics

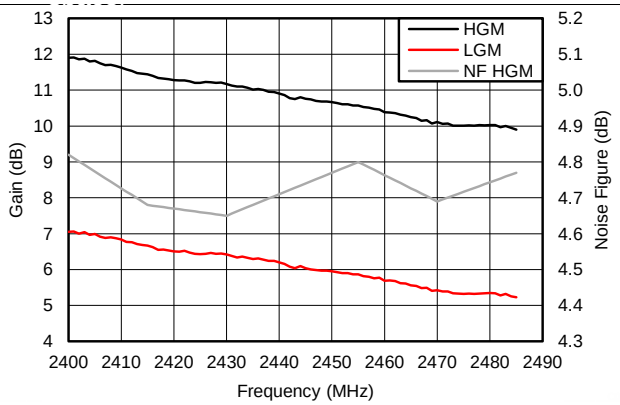

Figure 1. LNA Gain and Noise Figure Versus Frequency

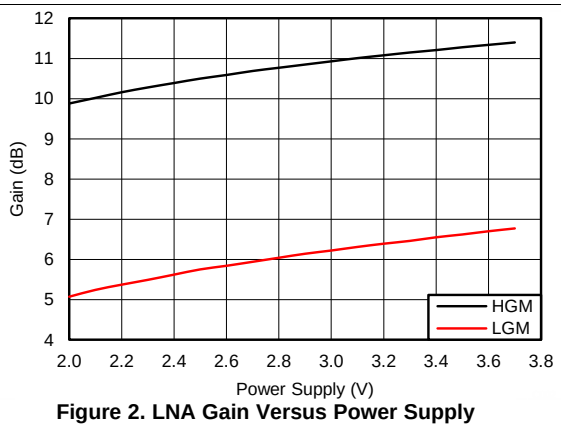

Figure 2. LNA Gain Versus Power Supply

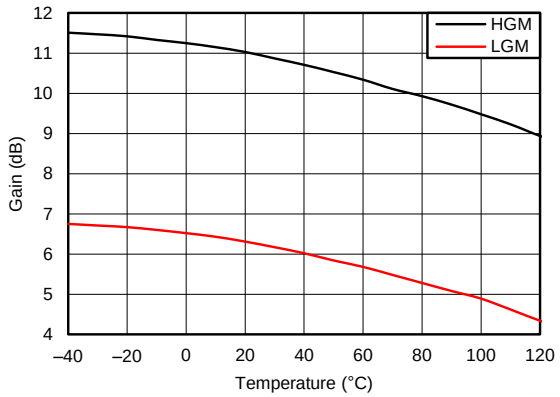

Figure 3. LNA Gain Versus Temperature

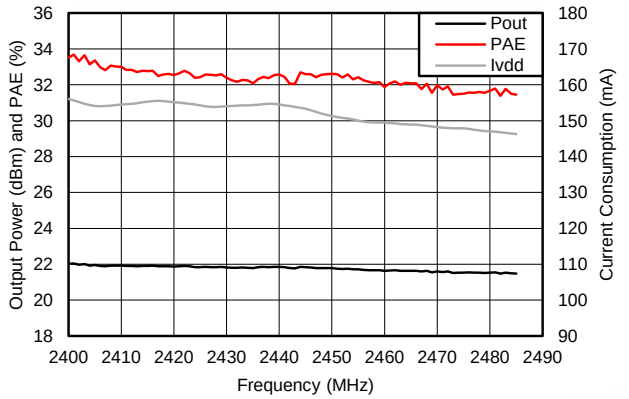

Figure 4. Output Power, PAE, and Current Consumption Versus Frequency
Input Power Level = +4 dBm

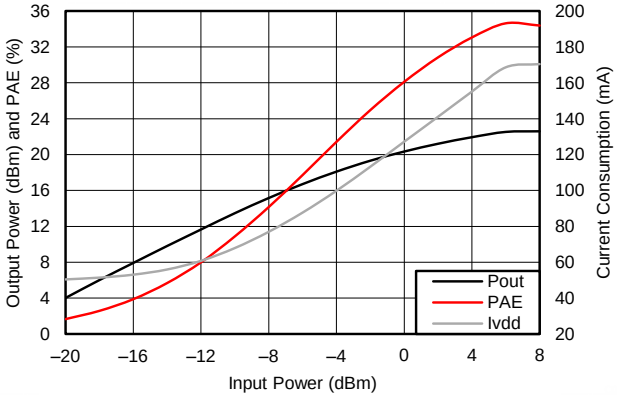

Figure 5. Output Power, PAE, and Current Consumption Versus Input Power

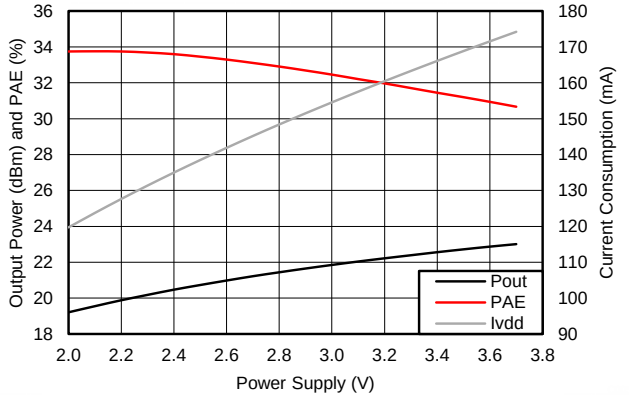

Figure 6. Output Power, PAE, and Current Consumption Versus Power Supply
Input Power Level = +4 dBm

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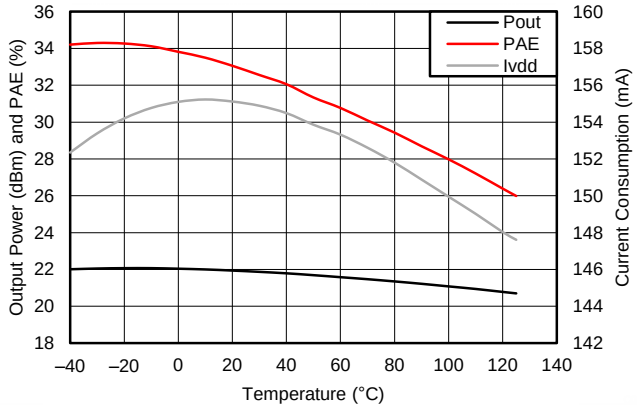

Figure 7. Output Power, PAE, and Current Consumption Versus Temperature Input Power Level = +4 dBm

7 Controlling the Output Power from CC2592

The output power of the CC2592 device is controlled by controlling the input power. The CC2592 PA is designed to work in compression (class AB).

Driving the CC2592 device too far into saturation might result in spurious emissions and harmonics above regulatory limits. This caution should especially be considered for systems targeting a wide operating temperature range, where a combination of low temperature, low supply voltage, and a transceiver that increases output power (drive level) at low temperature, can result in high spurious emissions.

Figure 7-1 shows the maximum recommended drive level versus temperature and supply voltage.

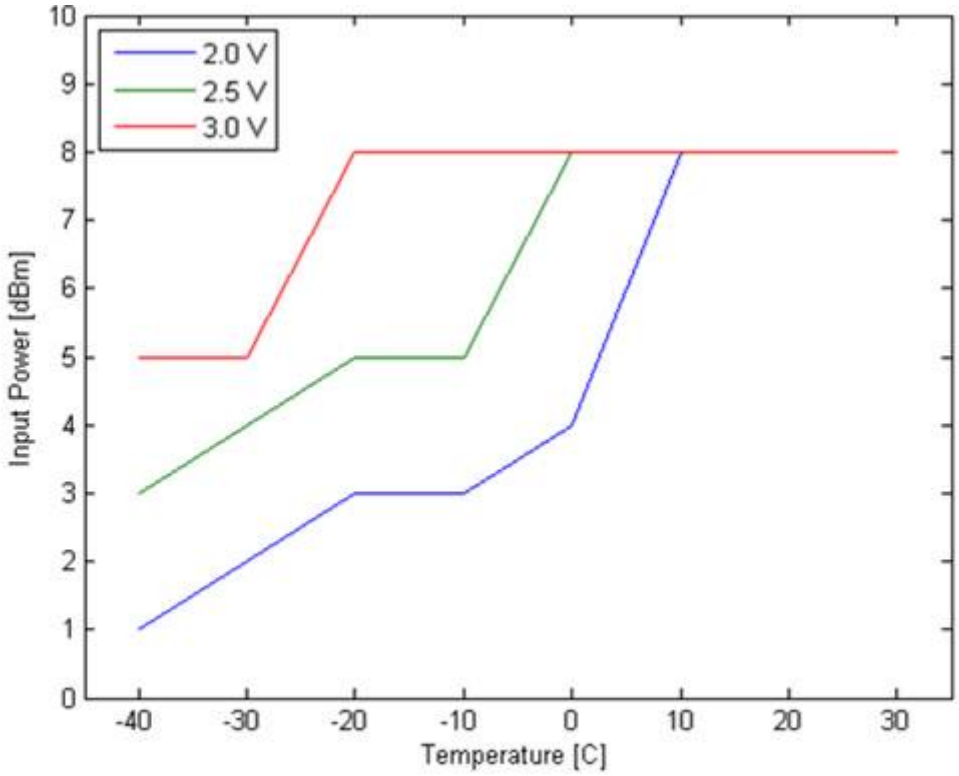

Figure 7-1. Maximum Recommended Drive Level

8 Input Levels on Control Terminals

The three digital control terminals (PA_EN, LNA_EN, and HGM) have built-in level-shifting functionality, meaning that if the CC2592 device operates off a 3.7-V supply voltage, the control terminals still sense 1.6- to 1.8-V signals as a logical 1. However, the input voltages should not have a logical 1 level that is higher than the supply.

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9 Connecting the CC2592 Device to a CC25xx Device

Table 9-1 shows the control logic for connecting CC2592 to a CC25xx device.

Table 9-1. Control Logic for Connecting CC2592 to a CC25xx Device

PA_EN	LNA_EN	HGM	Mode of Operation
0	0	X	Power Down
X	1	0	RX Low-Gain Mode
X	1	1	RX High-Gain Mode
1	0	X	TX

Figure 9-1 shows the application circuit for the CC2592 and CC253X devices.

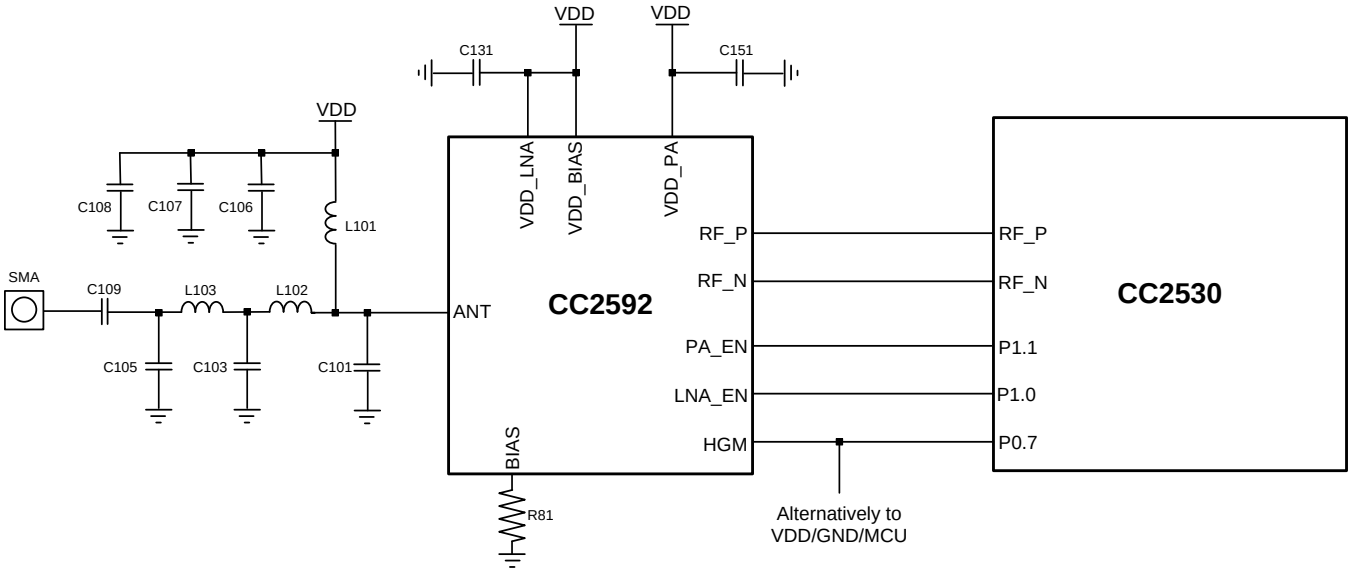

Figure 9-1. Application Circuit Example for CC2530 + CC2592

10 Device and Documentation Support

10.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CC2592	Click here	Click here	Click here	Click here	Click here

10.2 Trademarks

ZigBee is a registered trademark of ZigBee Alliance.

10.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC2592RGVR	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CC2592
CC2592RGVR.B	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CC2592
CC2592RGVRG4	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CC2592
CC2592RGVRG4.B	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CC2592
CC2592RGVT	Active	Production	VQFN (RGV) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CC2592
CC2592RGVT.B	Active	Production	VQFN (RGV) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CC2592

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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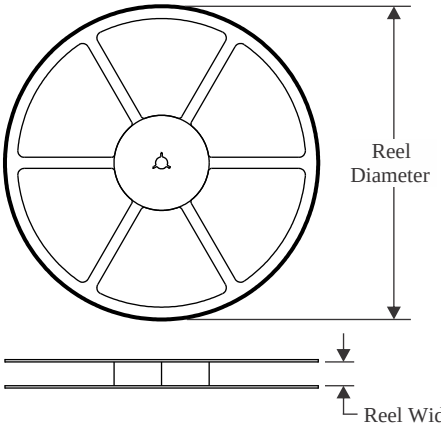
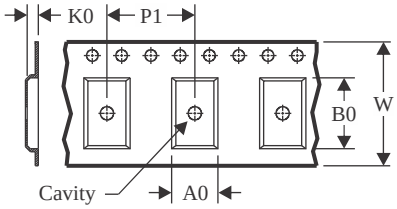
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

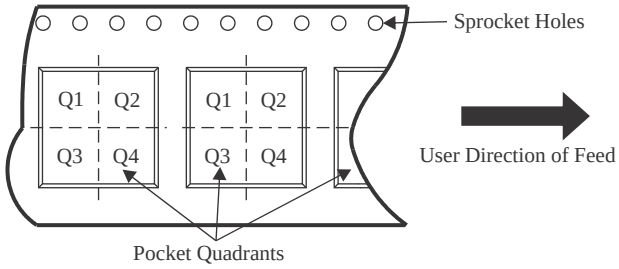


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

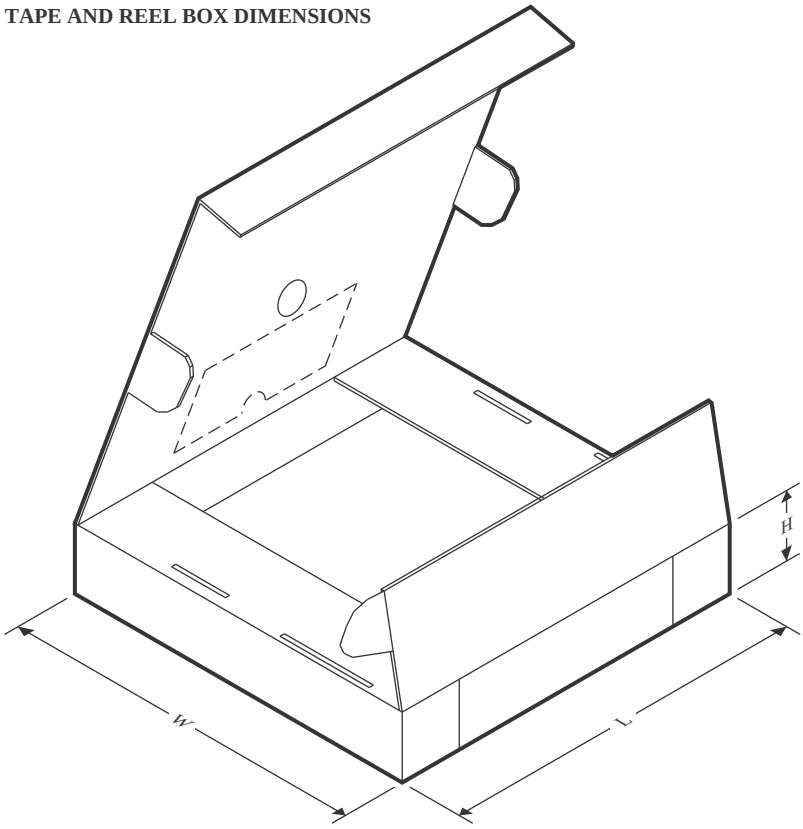
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2592RGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC2592RGVRG4	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC2592RGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC2592RGVT	VQFN	RGV	16	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2592RGVR	VQFN	RGV	16	2500	367.0	367.0	35.0
CC2592RGVRG4	VQFN	RGV	16	2500	367.0	367.0	35.0
CC2592RGVT	VQFN	RGV	16	250	210.0	185.0	35.0
CC2592RGVT	VQFN	RGV	16	250	210.0	185.0	35.0

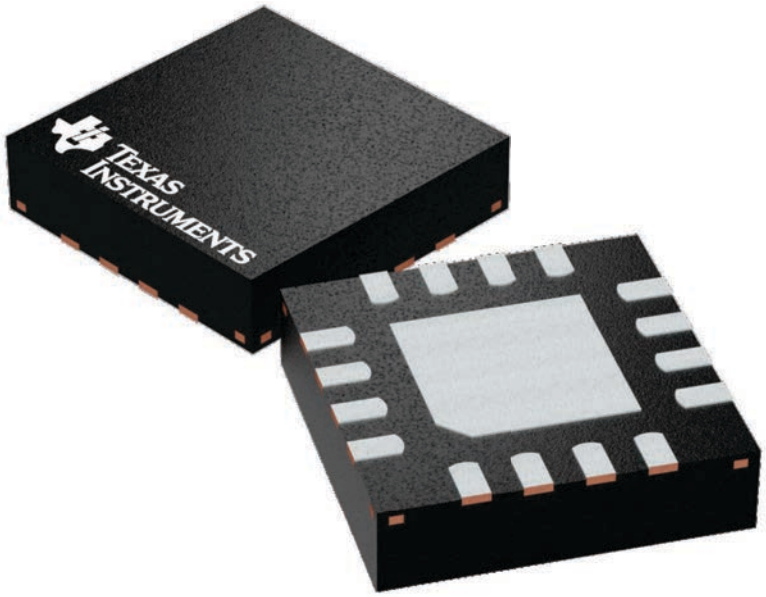
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

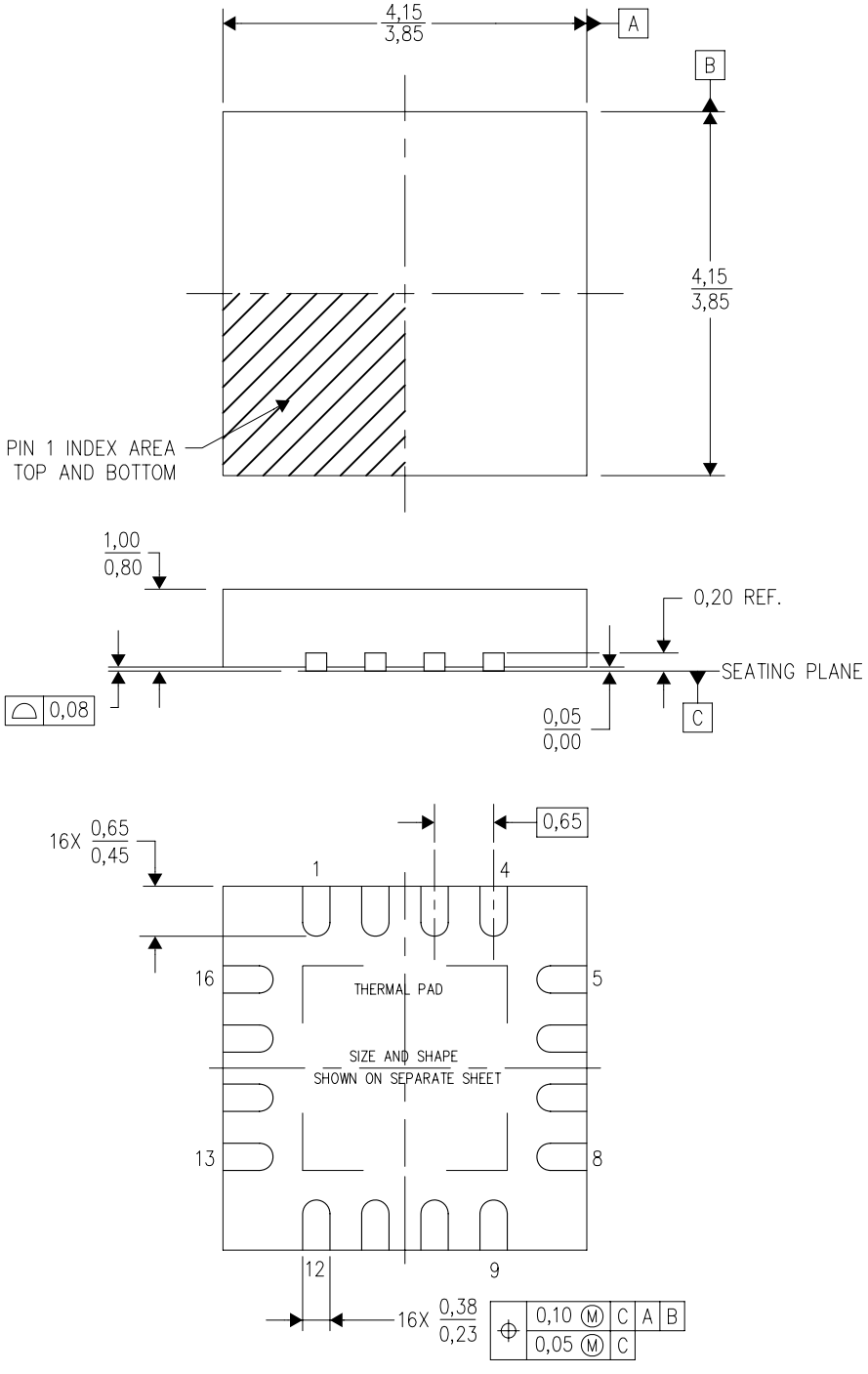
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224748/A

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

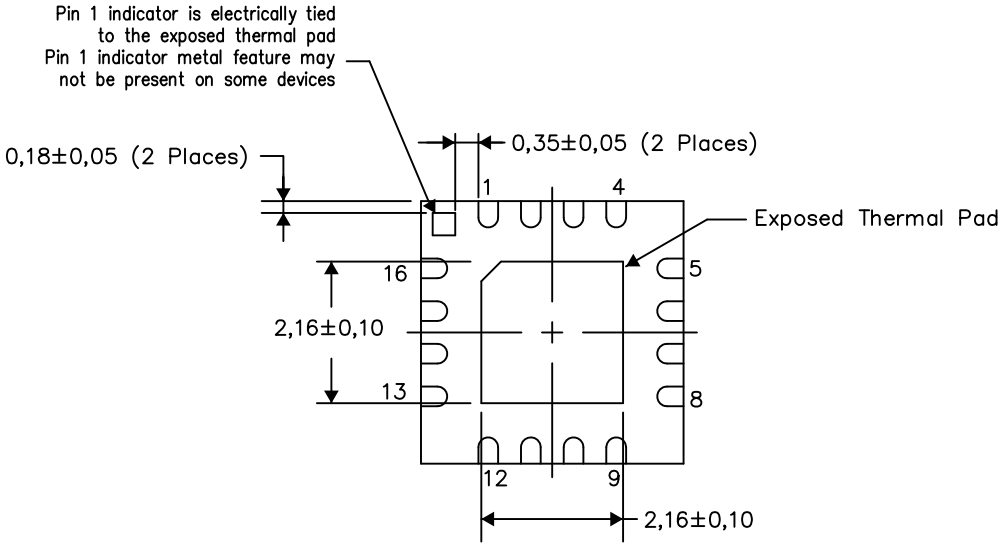
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



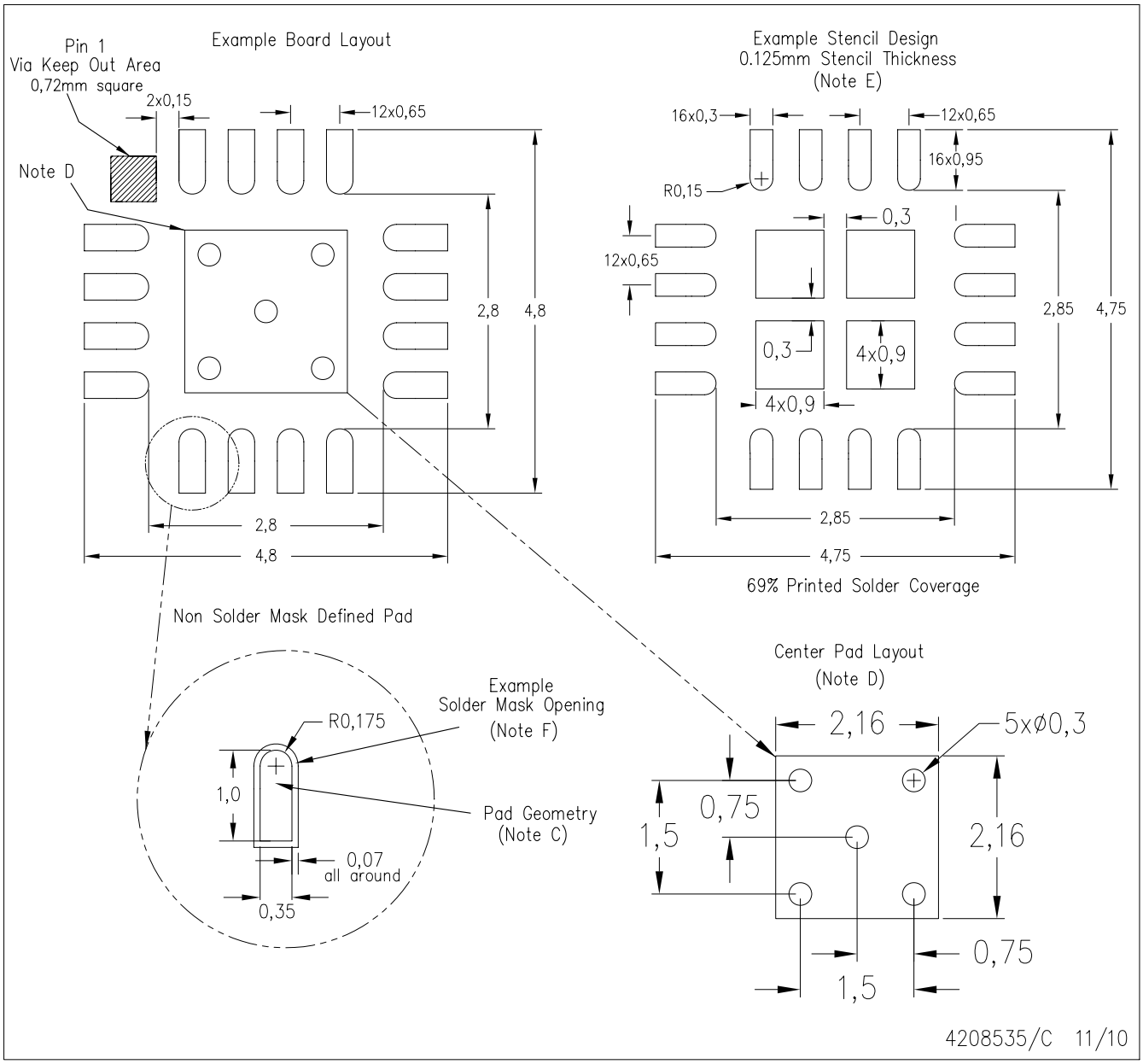
Bottom View

Exposed Thermal Pad Dimensions

4206351–2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



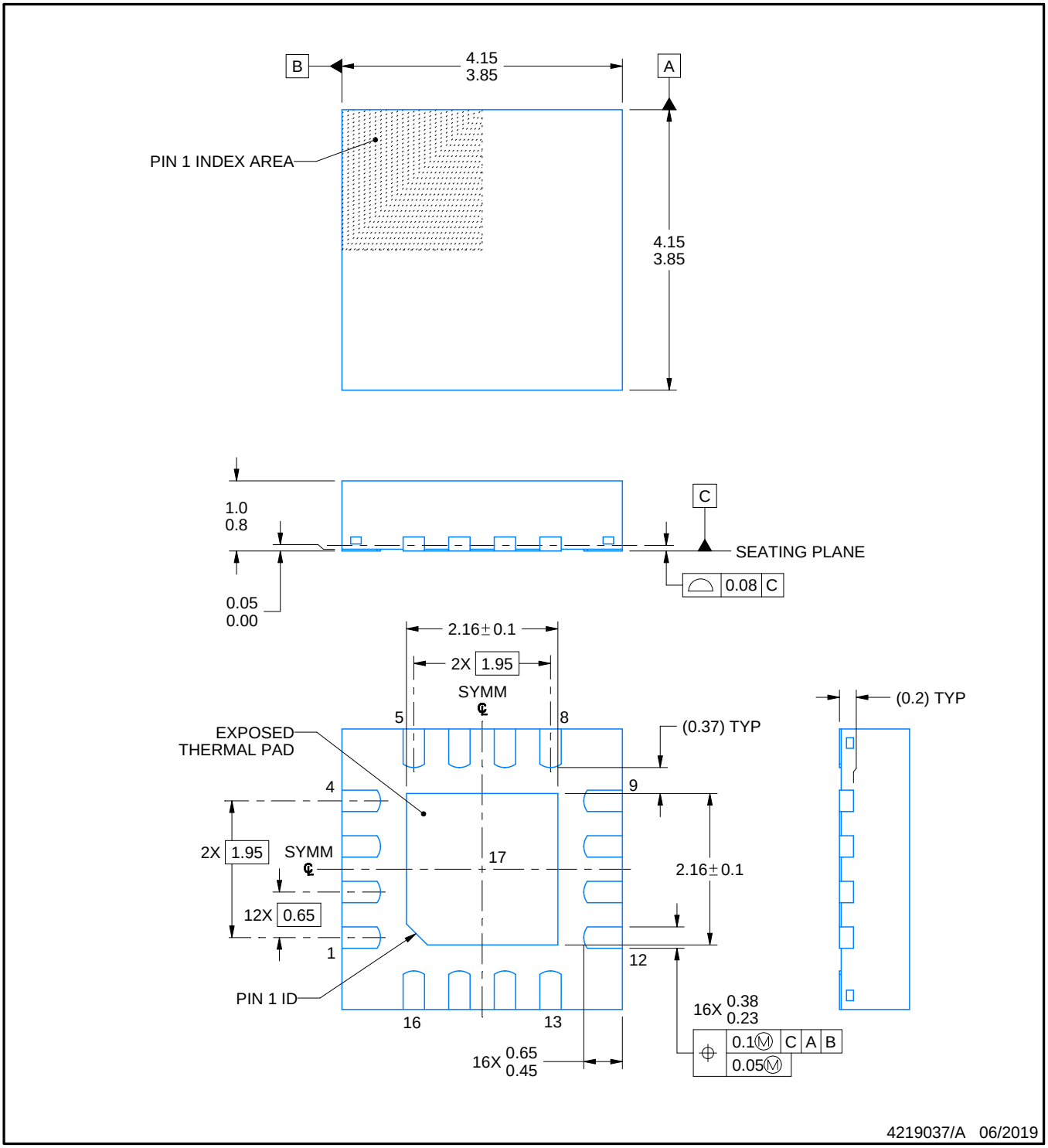
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

RGV0016A

PACKAGE OUTLINE

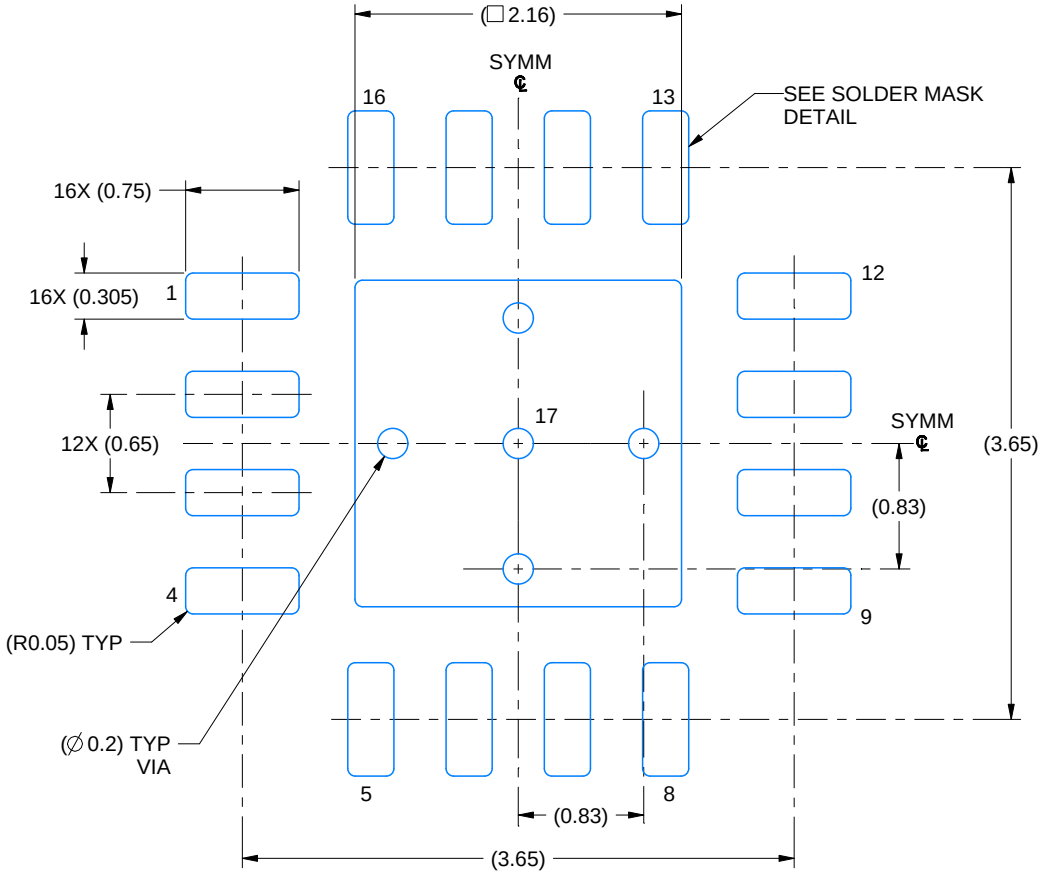
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

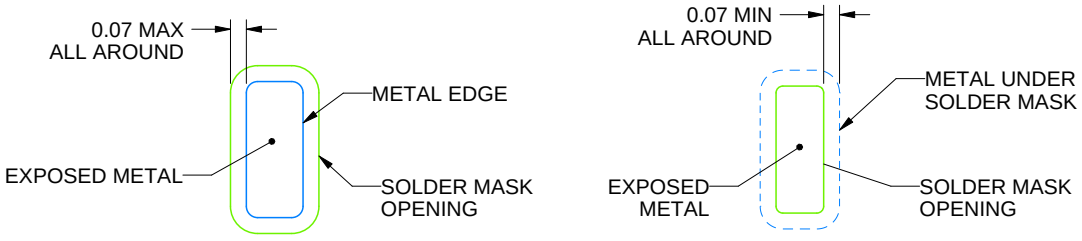


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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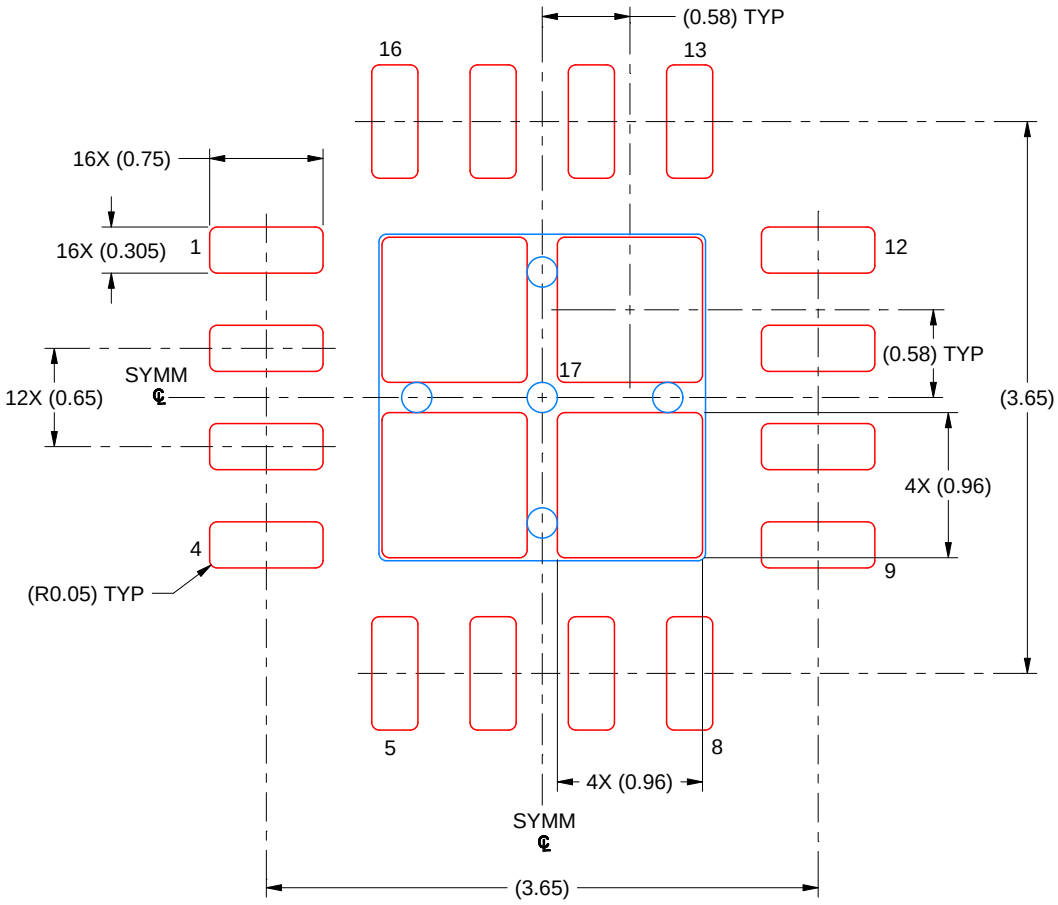
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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