BQ40Z80 2-Series to 6-Series Li-Ion Battery Pack Manager

1 Features

- Fully integrated 2-series to 6-series Li-ion or Li-polymer cell battery pack manager and protection
- Next-generation patented Impedance Track™ technology accurately measures available charge in Li-ion and Li-polymer batteries
- Configurable multifunction pins to support a variety of applications
- Supports either elliptic curve cryptography (ECC) or SHA-1 authentication
- High-side N-channel protection FET drive
- Integrated cell balancing while charging or at rest
- Supports 29Ah batteries natively, and larger capacities with scaling
- Full array of programmable protection features
  - Voltage
  - Current
  - Temperature
  - Charge timeout
  - CHG/DSG FETs
  - AFE
- Sophisticated charge algorithms
  - JEITA
  - Enhanced charging
  - Adaptive charging
  - Cell balancing
- Supports TURBO Mode 2.0/Intel® Dynamic Battery Power Technology (DBPTv2)
- Diagnostic lifetime data monitor and black box recorder
- LED display
- Supports two-wire SMBus v1.1 interface
- IATA support
- Compact package: 32-lead QFN (RSM)

2 Applications

- Industrial appliances and robots
- Handheld garden and power tools
- Battery powered vacuums
- Energy storage systems and UPS

3 Description

The BQ40Z80 device is a fully integrated, single-chip option that incorporates patented Impedance Track technology. The BQ40Z80 device provides a range of features for gas gauging, protection, and authentication, supporting 2-series to 6-series cell Li-ion and Li-polymer battery packs.

Using integrated high-performance analog peripherals, the BQ40Z80 device measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-ion or Li-polymer batteries. The record is reported to the system host controller over an SMBus v1.1 compatible interface.

Elliptic curve cryptography (ECC) or SHA-1 authentication with secure memory for authentication keys enables identification of genuine battery packs.

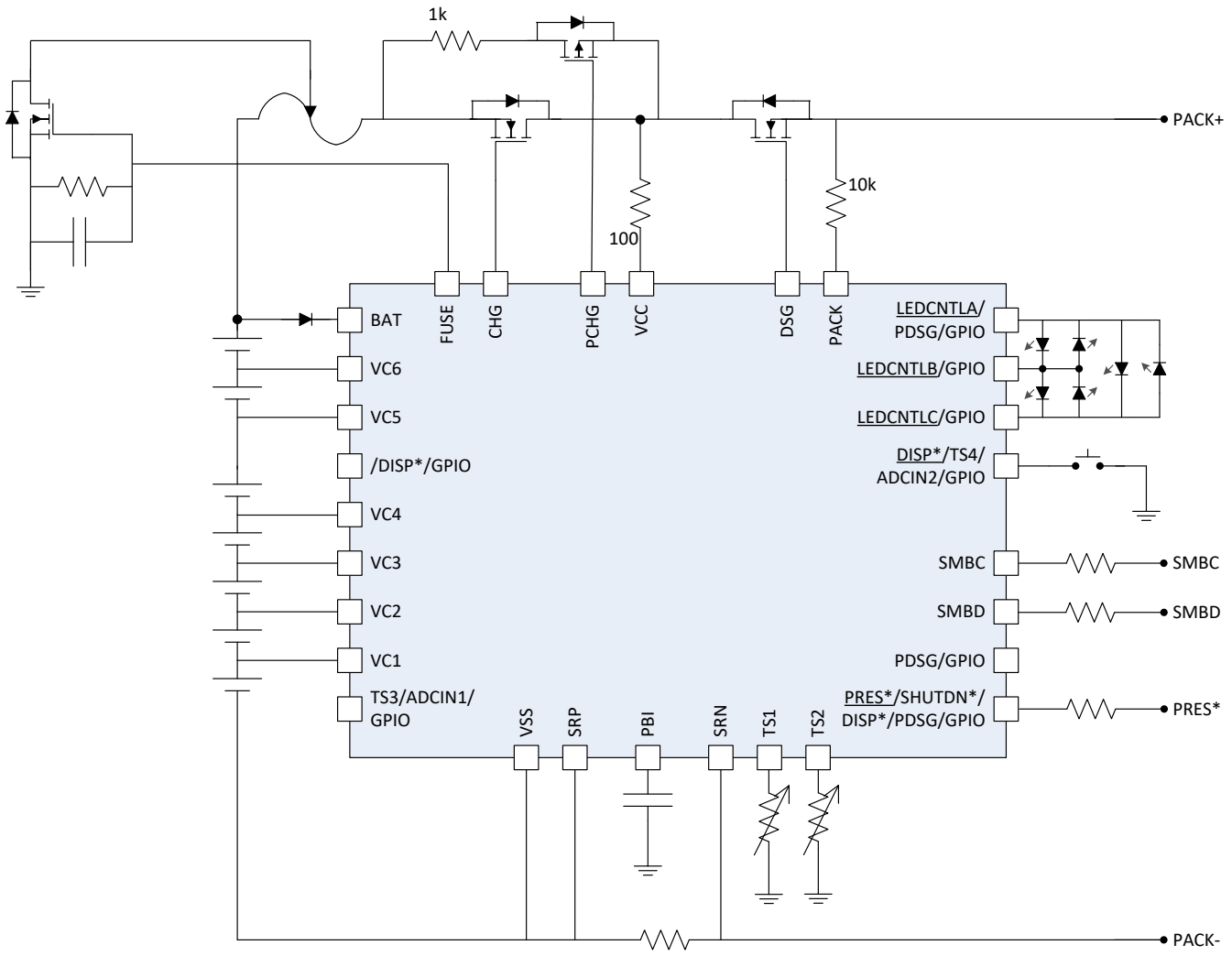
The BQ40Z80 device supports TURBO Mode 2.0/ Intel Dynamic Battery Power Technology (DBPTv2) by providing the available max power and max current to the host system. The device has eight multifunction pins that can be configured as thermal inputs, ADC inputs, general purpose input/output (GPIO) pins, a presence pin, LED functions, display button input, or other functions. Status and flag registers are mappable to the GPIOs and used as interrupts to the host processor.

The BQ40Z80 device provides software-based 1st- and 2nd-level safety protection against overvoltage, undervoltage, overcurrent, short-circuit current, overload, and overtemperature conditions, as well as other pack-related and cell-related faults. The compact 32-lead QFN package minimizes the cost and size for smart batteries, while providing maximum functionality and safety for battery gauging applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
BQ40Z80	VQFN (RSM, 32)	4.00mm × 4.00mm

(1) For more information, see Mechanical, Packaging, and Orderable Information
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

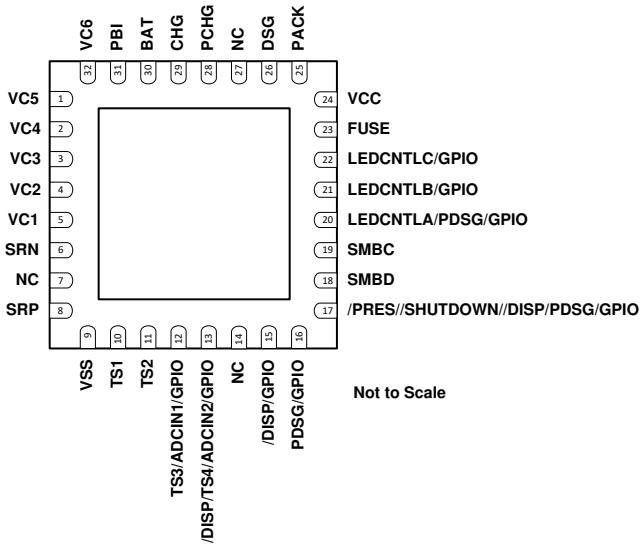


Figure 4-1. RSM Package 32-Pin VQFN with Exposed Thermal Pad Top View

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
VC5	1	AI[(1)]	Sense voltage input pin for the fifth cell from the bottom of the stack, balance current input for the fifth cell from the bottom of the stack, and return balance current for the sixth cell from the bottom of the stack. Connect to the positive terminal of the fifth cell from the bottom of stack with a 100Ω series resistor and a 0.1µF capacitor to VC4. If not used, connect to VC4.
VC4	2	AI	Sense voltage input pin for the fourth cell from the bottom of the stack, balance current input for the fourth cell from the bottom of the stack, and return balance current for the fifth cell from the bottom of the stack. Connect to the positive terminal of the fourth cell from the bottom of stack with a 100Ω series resistor and a 0.1µF capacitor to VC3. If not used, connect to VC3.

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
VC3	3	AI	Sense voltage input pin for the third cell from the bottom of the stack, balance current input for the third cell from the bottom of the stack, and return balance current for the fourth cell from the bottom of the stack. Connect to the positive terminal of the third cell from the bottom of stack with a 100Ω series resistor and a 0.1µF capacitor to VC2. If not used, connect to VC2.
VC2	4	AI	Sense voltage input pin for the second cell from the bottom of the stack, balance current input for the second cell from the bottom of the stack, and return balance current for the third cell from the bottom of the stack. Connect to the positive terminal of the second cell from the bottom of stack with a 100Ω series resistor and a 0.1µF capacitor to VC1. If not used, connect to VC1.
VC1	5	AI	Sense voltage input pin for the first cell from the bottom of the stack, balance current input for the first cell from the bottom of the stack, and return balance current for the second cell from the bottom of the stack. Connect to the positive terminal of the first cell from the bottom of stack with a 100Ω series resistor and a 0.1µF capacitor to VSS.
SRN	6	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor and charging current flows from SRP to SRN. Connect through an RC filter to the sense resistor terminal connected to PACK– (not CELL–).
NC	7	—	Not internally connected
SRP	8	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor and charging current flows from SRP to SRN. Connect through an RC filter to the sense resistor positive terminal, which is connected to the least-positive cells negative terminal.
VSS	9	P	Device ground
TS1	10	AI	Temperature sensor 1 thermistor input pin. Connect to thermistor-1. If not used, connect directly to VSS and configure data flash accordingly.
TS2	11	AI	Temperature sensor 2 thermistor input pin. Connect to thermistor-2. If not used, connect directly to VSS and configure data flash accordingly.
TS3/ADCIN1/ GPIO	12	IO	Multifunction pin for TS3, ADCIN1, and GPIO. Can be configured in the control registers. If not used, connect directly to VSS and configure data flash accordingly. TS3: Temperature sensor 3 thermistor input pin. Connect to thermistor-3. ADCIN1: General-purpose ADCIN pin. Connect properly scaled input to this pin. GPIO: Customizable GPIO
$\overline{\text{DISP}}$/TS4/ADCIN2/GPIO	13	IO	Multifunction pin for the display button, temperature sensor input, ADC input, or GPIO. Can be configured in the control registers. If not used, connect directly to VSS and configure data flash accordingly. $\overline{\text{DISP}}$: Connect to the display button or LED. TS4: Temperature sensor 4 thermistor input pin. Connect to thermistor-4. ADCIN2: General-purpose ADCIN pin. Connect properly scaled input to this pin. GPIO: Customizable GPIO
NC	14	—	Not internally connected
$\overline{\text{DISP}}$/GPIO	15	I/OD	Multifunction pin for the display button, or GPIO. Can be configured in the control registers. If not used, connect directly to VSS and configure data flash accordingly. $\overline{\text{DISP}}$: Connect to the display button or LED. GPIO: Customizable GPIO
PDSG/GPIO	16	I/OD	Multifunction pin for pre-discharge FET control, or GPIO. Can be configured in the control registers. If not used, connect directly to VSS and configure data flash accordingly. PDSG: Connect to the N-channel FET to control PRE-DISCHARGE mode. GPIO: Customizable GPIO

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
PRES/ SHUTDN/ DISP/ PDSG/GPIO	17	I/OD	Multifunction pin for host system present input, emergency system shutdown, LED button control, pre-discharge control, or GPIO. Can be configured in the control registers. If not used, connect directly to VSS and configure data flash accordingly. PRES: Connect to host to detect system present input for a removable battery pack. Do not pullup this pin. SHUTDN: Emergency shutdown input for an embedded battery pack DISP: Connect to the display button or LED. PDSG: Connect to the N-channel FET to control PRE-DISCHARGE mode. GPIO: Customizable GPIO
SMBD	18	I/OD	SMBus data pin
SMBC	19	I/OD	SMBus clock pin
LEDCNTLA/PDSG/GPIO	20	O	Multifunction pin for LED display, pre-discharge, or GPIO. If not used, connect to VSS with a 20-kΩ resistor. LEDCNTLA: LED display segment that drives the external LEDs, depending on the firmware configuration. PDSG: Connect to the N-channel FET to control PRE-DISCHARGE mode. GPIO: Customizable GPIO
LEDCNTLB/GPIO	21	O	Multifunction pin for LED display or GPIO. If not used, connect to VSS with a 20-kΩ resistor. LEDCNTLB: LED display segment that drives the external LEDs, depending on the firmware configuration. GPIO: Customizable GPIO
LEDCNTLC/GPIO	22	O	Multifunction pin for LED display or GPIO. If not used, connect to VSS with a 20-kΩ resistor. LEDCNTLC: LED display segment that drives the external LEDs, depending on the firmware configuration GPIO: Customizable GPIO
FUSE	23	O	Fuse drive output pin. Can be OR'ed together into the fuse N-channel FET gate drive with secondary protector. If not used, connect directly to VSS.
VCC	24	P	Secondary power supply input. Connect to the middle of protection FETs through the series resistor.
PACK	25	AI	Pack sense input pin. Connect through the series resistor to PACK+.
DSG	26	O	NMOS discharge FET drive output pin. Connect to the DSG FET gate.
NC	27	—	Not internally connected.
PCHG	28	O	PMOS precharge FET drive output pin. Connect to the PCHG FET gate if the precharge function is used. Leave floating if not used.
CHG	29	O	NMOS charge FET drive output pin. Connect to the CHG FET gate.
BAT	30	P	Primary power supply input pin. Connect through the diode and series resistor to the top of the cell stack.
PBI	31	P	Power supply backup input pin. Connect to the 2.2µF capacitor to VSS.
VC6	32	AI	Sense voltage input pin for the sixth cell from the bottom of the stack, balance current input for the sixth cell from the bottom of the stack. Connect to the positive terminal of the sixth cell from the bottom of stack with 100Ω series resistor and a 0.1µF capacitor to VC5. If not used, connect to VC5.

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

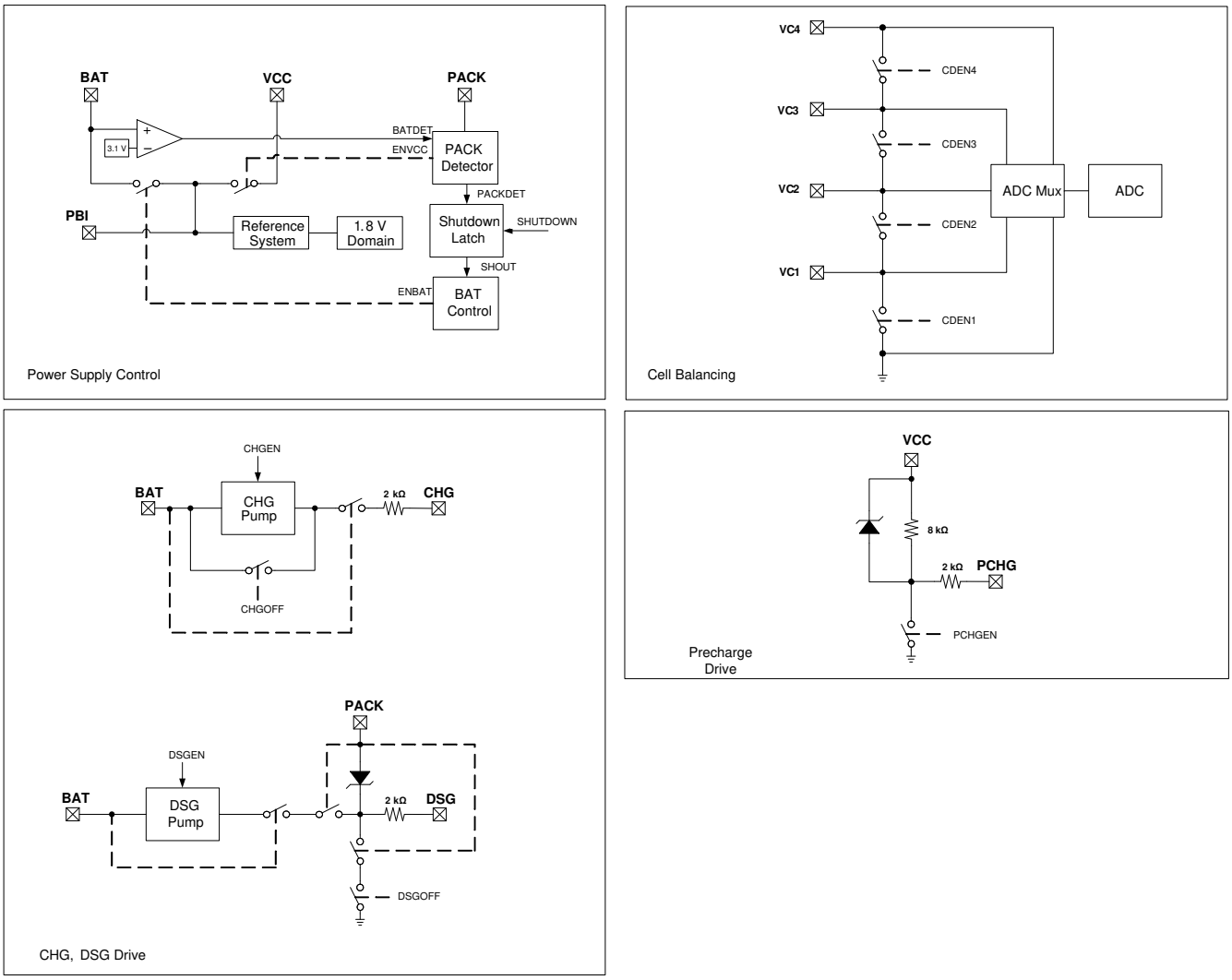


Figure 4-2. Pin Equivalent Diagram 1

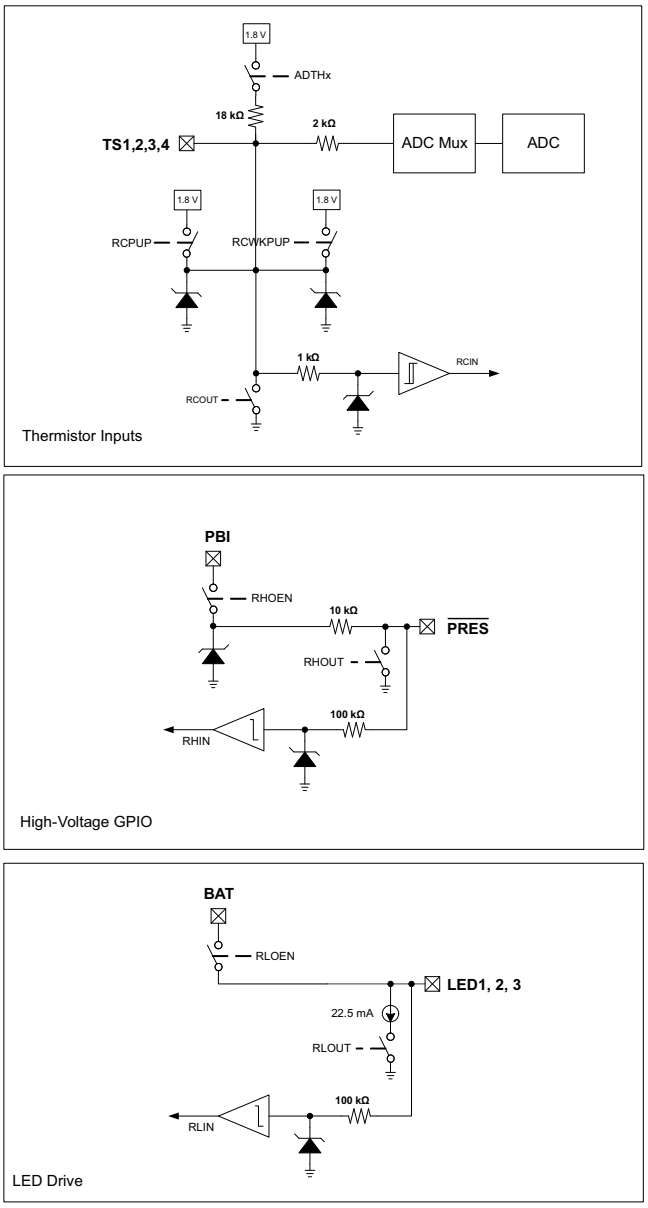


Figure 4-3. Pin Equivalent Diagram 2

5 Specifications

5.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{CC}	BAT(2), VCC(2), PBI(2), PACK(2)	–0.3	35	V
Input voltage range, V_{IN}	SMBC, SMBD, $\overline{DISP}$/GPIO, PDSG/GPIO, $\overline{PRES}$/ $\overline{SHUTDN}$/ $\overline{DISP}$/ PDSG/GPIO(2)	–0.3	35	V
	TS1, TS2, TS3/ADCIN1/GPIO, $\overline{DISP}$/TS4/ADCIN2/GPIO	–0.3	V_{REG} + 0.3	V
	LEDCNTLA/PDSG/GPIO, LEDCNTLB/GPIO, LEDCNTLC/GPIO(2)	–0.3	V_{BAT} + 0.3	V
	SRP, SRN	–0.3	V_{REG} + 0.3	V
	VC6	VC5 – 0.3	VSS + 35	V
	VC5	VC4 – 0.3	VSS + 35	V
	VC4	VC3 – 0.3	VSS + 35	V
	VC3	VC2 – 0.3	VSS + 35	V
	VC2	VC1 – 0.3	VSS + 35	V
	VC1	VSS – 0.3	VSS + 35	V
Output voltage range, V_O	CHG, DSG(2)	–0.3	43	
	PCHG, FUSE	–0.3	35	V
Maximum VSS current, I_{SS}			50	mA
Functional temperature T_{FUNC}		–40	110	
Storage temperature, T_{STG}		–65	150	°C
Lead temperature (soldering, 10s), T_{SOLDER}			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) A series 50Ω or larger resistor is needed when voltage is applied beyond 28V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and VCC = 25.2V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	BAT(1), VCC(1), PBI(1), PACK(1)	2.2		32	V
$V_{SHUTDOWN–}$	Shutdown voltage	V_{PACK} < $V_{SHUTDOWN\ –}$	1.8	2.0	2.2	V
$V_{SHUTDOWN+}$	Start-up voltage	V_{PACK} > $V_{SHUTDOWN–}$ + V_{HYS}	2.05	2.25	2.45	V
V_{HYS}	Shutdown voltage hysteresis	$V_{SHUTDOWN+}$ – $V_{SHUTDOWN–}$		250		mV

5.3 Recommended Operating Conditions (continued)

Typical values stated where T_A = 25°C and VCC = 25.2V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	SMBC, SMBD, $\overline{DISP}$/GPIO, PDSG/GPIO, $\overline{PRES}$/ $\overline{SHUTDN}$/, $\overline{DISP}$/PDSG/GPIO(1)			32	V
		TS1, TS2, TS3/ADCIN1/GPIO, $\overline{DISP}$/TS4/ADCIN2/GPIO			V_{REG}	
		LEDCNTLA/PDSG/GPIO, LEDCNTLB/GPIO, LEDCNTLC/ GPIO(1)			V_{BAT}	
		SRP, SRN	–0.2		0.2	
		VC6	V_{VC5}		VC5 + 5	
		VC5	V_{VC4}		VC4 + 5	
		VC4	V_{VC3}		VC3 + 5	
		VC3	V_{VC2}		VC2 + 5	
		VC2	V_{VC1}		VC1 + 5	
		VC1	V_{VSS}		VSS + 5	
V_O	Output voltage range	PCHG, FUSE(1)			32	V
C_{PBI}	External PBI capacitor		2.2			µF
T_{OPR}	Operating temperature		–40		85	°C

(1) A series 50Ω or larger resistor is needed when voltage is applied beyond 28V.

5.4 Thermal Information

THERMAL METRIC(1)		BQ40Z80 RSM (QFN) 32 PINS	UNIT
$R_{\theta JA, High K}$	Junction-to-ambient thermal resistance	47.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	40.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.4	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VCC = 21.6V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Supply Currents						
I_{NORMAL}	NORMAL mode	CPU not active, CHG on. DSG on, High Frequency Oscillator on, Low Frequency Oscillator on, REG18 on, ADC on, ADC_Filter on, CC_Filter on, CC on, LED/Buttons/GPIOs off, SMBus not active, no Flash write		663		µA

5.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_{SLEEP}	SLEEP mode	CPU not active, CHG on, DSG on, High Frequency Oscillator off, Low Frequency Oscillator on, REG18 on, ADC off, ADC_Filter off, CC_Filter off, LED/ Buttons/GPIOs off, SMBus not active, no Flash write		96		µA
		CPU not active, CHG off. DSG on, High Frequency Oscillator off, Low Frequency Oscillator on, REG18 on, ADC off, ADC_Filter off, CC_Filter off, LED/ Buttons/GPIOs off, SMBus not active, no Flash write, BAT = 14.4V		90		µA
$I_{SHUTDOWN}$	SHUTDOWN mode	CPU not active, CHG off. DSG off, High Frequency Oscillator off, Low Frequency Oscillator off, REG18 off, ADC off, ADC_Filter off, CC_Filter off, LED/ Buttons/GPIOs off, SMBus not active, no Flash write, BAT = 14.4V		1.4		µA
Power Supply Control						
$V_{SWITCHOVER–}$	BAT to VCC switchover voltage	$V_{BAT} < V_{SWITCHOVER–}$	1.95	2.1	2.2	V
$V_{SWITCHOVER+}$	VCC to BAT switchover voltage	$V_{BAT} > V_{SWITCHOVER–} + V_{HYS}$	2.9	3.1	3.25	V
V_{HYS}	Switchover voltage hysteresis	$V_{SWITCHOVER+} – V_{SWITCHOVER–}$		1000		mV
I_{LKG}	Input Leakage Current	BAT pin, BAT = 0V, VCC = 32V, PACK = 32V			1	µA
		PACK pin, BAT = 32V, VCC = 0V, PACK = 0V			1	
		BAT and PACK terminals, BAT = 0V, VCC = 0V, PACK = 0V, PBI = 32V			1	
R_{PD}	Internal pulldown resistance	PACK	30	40	50	kΩ
AFE Power-On Reset						
$V_{REGIT–}$	Negative-going voltage input	V_{REG}	1.51	1.55	1.59	V
V_{HYS}	Power-on reset hysteresis	$V_{REGIT+} – V_{REGIT–}$	70	100	130	mV
t_{RST}	Power-on reset time		200	300	400	µs
AFE Watchdog Reset and Wake Timer						
t_{WDT}	AFE watchdog timeout	t_{WDT} = 500	372	500	628	ms
		t_{WDT} = 1000	744	1000	1256	ms
		t_{WDT} = 2000	1488	2000	2512	ms
		t_{WDT} = 4000	2976	4000	5024	ms
t_{WAKE}	AFE wake timer	t_{WAKE} = 250	186	250	314	ms
		t_{WAKE} = 500	372	500	628	ms
		t_{WAKE} = 1000	744	1000	1256	ms
		t_{WAKE} = 2000	1488	2000	2512	ms
t_{FETOFF}	FET off delay after reset	t_{FETOFF} = 512	409	512	614	ms
Internal 1.8V LDO						
V_{REG}	Regulator voltage		1.6	1.8	2	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	$\Delta V_{REG} / \Delta T_A$, I_{REG} = 10mA		±0.25%		
$\Delta V_{O(LINE)}$	Line regulation	$\Delta V_{REG} / \Delta V_{BAT}$, I_{BAT} = 10mA	–0.6%		0.5%	
$\Delta V_{O(LOAD)}$	Load regulation	$\Delta V_{REG} / \Delta I_{REG}$, I_{REG} = 0mA to 10mA	–1.5%		1.5%	

5.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_{REG}	Regulator output current limit	V_{REG} = 0.9 × $V_{REG(NOM)}$, V_{IN} > 2.2V	20			mA
I_{SC}	Regulator short-circuit current limit	V_{REG} = 0 × $V_{REG(NOM)}$	25	40	55	mA
$PSRR_{REG}$	Power supply rejection ratio	ΔV_{BAT} / ΔV_{REG}, I_{REG} = 10mA, V_{IN} > 2.5V, f = 10Hz		40		dB
V_{SLEW}	Slew rate enhancement voltage threshold	V_{REG}	1.58	1.65		V
Voltage Reference 1						
V_{REF1}	Internal reference voltage	T_A = 25°C, after trim	1.215	1.22	1.225	V
$V_{REF1(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		PPM/°C
Voltage Reference 2						
V_{REF2}	Internal reference voltage	T_A = 25°C, after trim	1.22	1.225	1.23	V
$V_{REF2(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		PPM/°C
VC1, VC2, VC3, VC4, VC5, VC6, BAT, PACK						
K	Scaling factor	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3, VC5–VC4, VC6–VC5	0.198	0.2	0.202	–
		VC6–VSS	0.032	0.0333	0.034	
		BAT–VSS, PACK–VSS	0.0275	0.0286	0.0295	
		V_{REF2}	0.49	0.5	0.51	
V_{IN}	Input voltage range	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3, VC5–VC4, VC6–VC5	–0.2		5	V
		VC6–VSS	–0.2		30	
		PACK–VSS	–0.2		32	
I_{LKG}	Input leakage current	VC1, VC2, VC3, VC4, VC5, VC6, cell balancing off, cell detach detection off, ADC multiplexer off			1	µA
Cell Balancing and Cell Detach Detection						
R_{CB}	Internal cell balance resistance	$R_{DS(ON)}$ for internal FET switch at 2V < VDS < 4V			200	Ω
I_{CD}	Internal cell detach check current	VCx > VSS + 0.8V	30	50	70	µA
ADC						
V_{IN}	Input voltage range	Internal reference (V_{REF1})	–0.2		1	V
		External reference (V_{REG})	–0.2		0.8 × V_{REG}	
	Full scale range	V_{FS} = V_{REF1} or V_{REG}	$-V_{FS}$		V_{FS}	V
INL	Integral nonlinearity (1LSB = $V_{REF1}/(10 \times 2^N)$ = $1.225/(10 \times 2^{15})$ = 37.41µV)	16-bit, best fit, –0.1V to 0.8 × V_{REF1}			±8.5	LSB
		16-bit, best fit, –0.2V to –0.1V			±13.1	
OE	Offset error	16-bit, post calibration, V_{FS} = V_{REF1}		±67	±157	µV
OED	Offset error drift	16-bit, post calibration, V_{FS} = V_{REF1}		0.6	3	µV/°C
GE	Gain error	16-bit, –0.1V to 0.8 × V_{FS}		±0.2%	±0.8%	/FSR
GED	Gain error drift	16-bit, –0.1V to 0.8 × V_{FS}			150	PPM/°C
EIR	Effective input resistance		8			MΩ

5.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ADC Digital Filter						
t_{CONV}	Conversion time	ADCTL[SPEED1, SPEED0] = 0, 0		31.25		ms
		ADCTL[SPEED1, SPEED0] = 0, 1		15.63		
		ADCTL[SPEED1, SPEED0] = 1, 0		7.81		
		ADCTL[SPEED1, SPEED0] = 1, 1		1.95		
Res	Resolution	No missing codes, ADCTL[SPEED1, SPEED0] = 0, 0	16			Bits
Eff_Res	Effective Resolution	With sign, ADCTL[SPEED1, SPEED0] = 0, 0	14	15		Bits
		With sign, ADCTL[SPEED1, SPEED0] = 0, 1	13	14		
		With sign, ADCTL[SPEED1, SPEED0] = 1, 0	11	12		
		With sign, ADCTL[SPEED1, SPEED0] = 1, 1	9	10		
Current Wake Comparator						
V_{WAKE}	Wake voltage threshold	$V_{WAKE} = V_{SRP} – V_{SRN}$= ± 0.625mV	±0.3	±0.625	±0.9	mV
		$V_{WAKE} = V_{SRP} – V_{SRN}$ = ± 1.25mV	±0.6	±1.25	±1.8	
		$V_{WAKE} = V_{SRP} – V_{SRN}$ = ± 2.5mV	±1.2	±2.5	±3.6	
		$V_{WAKE} = V_{SRP} – V_{SRN}$ = ± 5mV	±2.4	±5.0	±7.2	
$V_{WAKE(DRIFT)}$	Temperature drift of V_{WAKE} accuracy			0.5%		/°C
t_{WAKE}	Time from application of current to wake interrupt			250	700	µs
$t_{WAKE(SU)}$	Wake comparator startup time			500	1000	µs
Coulomb Counter						
V_{INPUT}	Input voltage range		–0.1		0.1	V
V_{RANGE}	Full scale range		$–V_{REF1}$ / 10		V_{REF1} / 10	V
INL	Integral nonlinearity (1LSB = $V_{REF1}/(10 \times 2^N)$ = $1.215/(10 \times 2^{15})$ = 3.71µV)	16-bit, best fit over input voltage range		±5.2	±22.3	LSB
OE	Offset error	16-bit, post calibration		±5.0	±10	µV
OED	Offset error drift	15-bit + sign, post calibration		0.2	0.3	µV/°C
GE	Gain error	15-bit + sign, Over input voltage range		±0.2%	±0.8%	/FSR
GED	Gain error drift	15-bit + sign, Over input voltage range			150	PPM/°C
EIR	Effective input resistance		2.5			MΩ
t_{CONV}	Conversion Time	Single conversion		250		ms
Eff_Res	Effective Resolution	Single conversion	15			Bits
Current Protection Thresholds						
V_{OCD}	OCD detection threshold voltage range	$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–16.6		–100	mV
		$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–8.3		–50	mV
ΔV_{OCD}	OCD detection threshold voltage program step	$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–5.56		mV
		$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–2.78		mV

5.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{SCC}	SCC detection threshold voltage range	$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	44.4		200	mV
		$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	22.2		100	mV
ΔV_{SCC}	SCC detection threshold voltage program step	$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		22.2		mV
		$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		11.1		mV
V_{SCD1}	SCD1 detection threshold voltage range	$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–22.2		–100	mV
ΔV_{SCD1}	SCD1 detection threshold voltage program step	$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–11.1		mV
V_{SCD2}	SCD2 detection threshold voltage range	$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–22.2		–100	mV
ΔV_{SCD2}	SCD2 detection threshold voltage program step	$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–11.1		mV
V_{OFFSET}	OCD, SCC, and SCDx offset error	Post-trim	–2.5		2.5	mV
V_{SCALE}	OCD, SCC, and SCDx scale error	No trim	–10%		10%	
		Post-trim	–5%		5%	
Current Protection Timing						
t_{OCD}	OCD detection delay time		1		31	ms
Δt_{OCD}	OCD detection delay time program step			2		ms
t_{SCC}	SCC detection delay time		0		915	µs
Δt_{SCC}	SCC detection delay time program step			61		µs
t_{SCD1}	SCD1 detection delay time	PROTECTION_CONTROL[SCDDx2] = 0	0		915	µs
		PROTECTION_CONTROL[SCDDx2] = 1	0		1850	µs
Δt_{SCD1}	SCD1 detection delay time program step	PROTECTION_CONTROL[SCDDx2] = 0		61		µs
		PROTECTION_CONTROL[SCDDx2] = 1		121		µs
t_{SCD2}	SCD2 detection delay time	PROTECTION_CONTROL[SCDDx2] = 0	0		458	µs
		PROTECTION_CONTROL[SCDDx2] = 1	0		915	µs
Δt_{SCD2}	SCD2 detection delay time program step	PROTECTION_CONTROL[SCDDx2] = 0		30.5		µs
		PROTECTION_CONTROL[SCDDx2] = 1		61		µs
t_{DETECT}	Current fault detect time	$V_{SRP} – V_{SRN} = V_T – 3mV$ for OCD, SCD1 and SCD2, $V_{SRP} – V_{SRN}$ = VT – 3mV for SCC			160	µs
t_{ACC}	Current fault delay time accuracy	Max delay setting	–10%		10%	
Internal Temperature Sensor						

5.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{TEMPT}	Internal temperature sensor voltage drift	V_{TEMPP}	–1.9		–2.1	mV/°C
		$V_{TEMPP} – V_{TEMPN}$, established by design	0.177	0.178	0.179	mV/°C
NTC Thermistor Measurement Support (TS1, TS2, Pins 12 and 13 configured as TS3 and TS4)						
$R_{NTC(PU)}$	Internal pullup resistance	TS1	14.4	18	21.6	kΩ
		TS2	14.4	18	21.6	kΩ
		TS3	14.4	18	21.6	kΩ
		TS4	14.4	18	21.6	kΩ
$R_{NTC(DRIFT)}$			–360	–280	–200	PPM/°C
Low-Voltage General Purpose I/O (Multifunction Pins 12 and 13 configured as GPIO)						
V_{IH}	High-level input		0.65 × V_{REG}			V
V_{IL}	Low-level input				0.35 × V_{REG}	V
V_{OH}	Output voltage high	Output high, pullup enabled, I_{OH} = –1.0mA	0.75 × V_{REG}			V
		Output high, pullup enabled, I_{OH} = –10µA				
V_{OL}	Output voltage low	Output Low, I_{OL} = 1mA			0.2 × V_{REG}	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
High-Voltage General Purpose I/O (multifunction pins 15, 16, 17 configured as GPIO, $\overline{PRES}$, $\overline{DISP}$, or $\overline{SHUTDN}$ Pin 15 configured as GPIO; Pin 16 configured as PDSG)						
V_{IH}	High-level input		1.3			V
V_{IL}	Low-level input				0.55	V
V_{OH}	Output voltage high	Output enabled, V_{BAT} > 5.5V, I_{OH} = –0µA	3.5			V
		Output enabled, V_{BAT} > 5.5V, I_{OH} = –10µA	1.8			
V_{OL}	Output voltage low	Output disabled, I_{OL} = 1.5mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				3	µA
R_O	Output reverse resistance	Between GPIO, $\overline{PRES}$, $\overline{DISP}$, $\overline{SHUTDN}$, PDSG, and PBI	8			kΩ
General Purpose I/O with Constant Current Sink (Multifunction Pins 20, 21, 22 configured as LEDCNTLx)						
V_{IH}	High-level input	LEDCNTLx	1.45			V
V_{IL}	Low-level input	LEDCNTLx			0.55	V
V_{OH}	Output voltage high	LEDCNTLx, Output Enabled, V_{BAT} > 3.0V, I_{OH} = –22.5mA	V_{BAT} – 1.6			V
V_{OL}	Output voltage low	LEDCNTLx, Output Disabled, V_{BAT} > 3.0V, I_{OH} = 3mA			0.4	V
I_{SC}	High level output current protection	LEDCNTLx	–30	–45	–60	mA
I_{OL}	Low level output current	LEDCNTLx, V_{BAT} > 3.0V, V_{OL} > 0.4V	15.75	22.5	29.25	mA
$I_{LEDCNTLx}$	Current matching between outputs	LEDCNTLx, V_{BAT} = V_{LED} + 2.5V		+/–1%		
C_{IN}	Input capacitance	LEDCNTLx		20		pF
I_{LKG}	Input leakage current	LEDCNTLx			1	µA
f_{LED}	Frequency of LED pattern	LEDCNTLx		124		Hz
$t_{SHUTDOWN}$	Thermal shutdown	LEDCNTLx, established by design	120	135	150	°C

5.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
General Purpose I/O (Multifunction Pins 20, 21, 22 configured as GPIO) (Pin 20 configured as PDSG)						
V_{IH}	High-level input		1.45			V
V_{IL}	Low-level input				0.55	V
V_{OH}	Output voltage high	Output enabled, V_{BAT} > 3.0V, I_{OH} = –22.5mA	V_{BAT} – 1.6			V
		Output disabled, I_{OL} = 3mA			0.4	V
I_{SC}	High level output current protection		–30	–45	–60	mA
I_{OL}	Low level output current	V_{BAT} > 3.0V, V_{OL} > 0.4V	15.75	22.5	29.25	mA
C_{IN}	Input capacitance			20		pF
I_{LKG}	Input leakage current				1	uA
SMBD, SMBC High Voltage I/O						
V_{IH}	Input voltage high	SMBC, SMBD, V_{REG} = 1.8V	1.3			V
V_{IL}	Input voltage low	SMBC, SMBD, V_{REG} = 1.8V			0.8	V
V_{OL}	Output low voltage	SMBC, SMBD, V_{REG} = 1.8V, I_{OL} = 1.5mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_{PD}	Pulldown resistance		0.7	1	1.3	MΩ
SMBus						
f_{SMB}	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	MASTER mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD(START)}$	Hold time after (repeated) start		4			µs
$t_{SU(START)}$	Repeated start setup time		4.7			µs
$t_{SU(STOP)}$	Stop setup time		4			µs
$t_{HD(DATA)}$	Data hold time		300			ns
$t_{SU(DATA)}$	Data setup time		250			ns
$t_{TIMEOUT}$	Error signal detect time		25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period		4		50	µs
t_R	Clock rise time	10% to 90%			1000	ns
t_F	Clock fall time	90% to 10%			300	ns
$t_{LOW(SEXT)}$	Cumulative clock low slave extend time				25	ms
$t_{LOW(MEXT)}$	Cumulative clock low master extend time				10	ms
SMBus XL						
f_{SMBXL}	SMBus XL operating frequency	SLAVE mode, SMBC 50% duty cycle	40		400	kHz
t_{BUF}	Bus free time between start and stop		4.7			µs

5.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$t_{HD(START)}$	Hold time after (repeated) start		4			µs
$t_{SU(START)}$	Repeated start setup time		4.7			µs
$t_{SU(STOP)}$	Stop setup time		4			µs
$t_{TIMEOUT}$	Error signal detect time		5		20	ms
t_{LOW}	Clock low period				20	µs
t_{HIGH}	Clock high period				20	µs
FUSE Drive (AFEFUSE)						
V_{OH}	Output voltage high	V_{BAT} ≥ 8V, C_L = 1nF, $I_{AFEFUSE}$ = 0µA	6	7	8.65	V
		V_{BAT} < 8V, C_L = 1nF, $I_{AFEFUSE}$ = 0µA	V_{BAT} – 0.1		V_{BAT}	V
V_{IH}	High-level input		1.5	2	2.5	V
$I_{AFEFUSE(PU)}$	Internal pullup current	V_{BAT} < 8V, $V_{AFEFUSE}$ = VSS		150	330	nA
$R_{AFEFUSE}$	Output impedance		2	2.6	3.2	kΩ
C_{IN}	Input capacitance			5		pF
t_{DELAY}	Fuse trim detection delay		128		256	µs
t_{RISE}	Fuse output rise time			5	20	µs
N-channel FET Drive (CHG, DSG)						
	Output voltage ratio	$Ratio_{DSG}$ = (V_{DSG} – V_{BAT}) / V_{BAT}, 2.2V < V_{BAT} < 4.92V, 10MΩ between PACK and DSG	2.133	2.333	2.45	—
		$Ratio_{CHG}$ = (V_{CHG} – V_{BAT}) / V_{BAT}, 2.2V < V_{BAT} < 4.92V, 10MΩ between BAT and CHG	2.133	2.333	2.433	—
V_{FETON}	Output voltage, CHG and DSG on	$V_{DSG(ON)}$ = (V_{DSG} – V_{BAT}), V_{BAT} ≥ 4.92V (up to 32V), 10MΩ between PACK and DSG	10.5	11.5	12.5	V
		$V_{CHG(ON)}$ = (V_{CHG} – V_{BAT}), V_{BAT} ≥ 4.92V (up to 32V), 10MΩ between BAT and CHG	10.5	11.5	12.5	V
V_{FETOFF}	Output voltage, CHG and DSG off	$V_{DSG(OFF)}$ = (V_{DSG} – V_{PACK}), 10MΩ between PACK and DSG	–0.4		0.4	V
		$V_{CHG(OFF)}$ = (V_{CHG} – V_{BAT}), 10MΩ between BAT and CHG	–0.4		0.4	V
t_R	Rise time	V_{DSG} from 0% to 35% $V_{DSG(ON)(TYP)}$, V_{BAT} ≥ 2.2V, C_L = 4.7nF between DSG and PACK, 5.1kΩ between DSG and C_L, 10MΩ between PACK and DSG		200	500	µs
		V_{CHG} from 0% to 35% $V_{CHG(ON)(TYP)}$, V_{BAT} ≥ 2.2V, C_L = 4.7nF between CHG and BAT, 5.1kΩ between CHG and C_L, 10MΩ between BAT and CHG		200	500	µs
t_F	Fall time	V_{DSG} from $V_{DSG(ON)(TYP)}$ to 1V, V_{BAT} ≥ 2.2V, C_L = 4.7nF between DSG and PACK, 5.1kΩ between DSG and C_L, 10MΩ between PACK and DSG		40	300	µs
		V_{CHG} from $V_{CHG(ON)(TYP)}$ to 1V, V_{BAT} ≥ 2.2V, C_L = 4.7nF between CHG and BAT, 5.1kΩ between CHG and C_L, 10MΩ between BAT and CHG		40	200	µs
P-channel FET Drive (PCHG)						
V_{FETON}	Output voltage, PCHG on	$V_{PCHG(ON)}$ = V_{CC} – V_{PCHG}, 10MΩ between VCC and CHG, V_{BAT} ≥ 8V	6	7	8	V
V_{FETOFF}	Output voltage, PCHG off	$V_{PCHG(OFF)}$ = V_{CC} – V_{PCHG}, 10MΩ between VCC and CHG	–0.4		0.4	V

5.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	V_{PCHG} from 10% to 90% $V_{PCHG(ON)(TYP)}$, V_{SS} ≥ 8V, C_L = 4.7nF between PCHG and VCC, 5.1kΩ between PCHG and C_L, 10MΩ between VCC and CHG		40	200	µs
t_F	Fall time	V_{PCHG} from 90% to 10% $V_{PCHG(ON)(TYP)}$, V_{SS} ≥ 8V, C_L = 4.7nF between PCHG and VCC, 5.1kΩ between PCHG and C_L, 10MΩ between VCC and CHG		40	200	µs
High-Frequency Oscillator						
f_{HFO}	Operating frequency			16.78		MHz
$f_{HFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–2.5%	±0.25%	2.5%	
		T_A = –40°C to 85°C, includes frequency drift	–3.5%	±0.25%	3.5%	
$t_{HFO(SU)}$	Start-up time	T_A = –20°C to 85°C, ***CLKCTL[HFRAMP]*** = 1, oscillator frequency within ±3% of nominal			4	ms
		T_A = –20°C to 85°C, ***CLKCTL[HFRAMP]*** = 0, oscillator frequency within ±3% of nominal			100	µs
Low-Frequency Oscillator						
f_{LFO}	Operating frequency			262.144		kHz
$f_{LFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C, includes frequency drift	–2.5%	±0.25%	2.5%	
$t_{LFO(FAIL)}$	Failure detection frequency		30	80	100	kHz
Instruction Flash						
	Data retention		10			Years
	Flash programming write cycles		1000			Cycles
$t_{PROGWORD}$	Word programming time				40	µs
$t_{MASSERASE}$	Mass-erase time				40	ms
$t_{PAGEERASE}$	Page-erase time				40	ms
$t_{FLASHREAD}$	Flash-read current				2	mA
$t_{FLASHWRITE}$	Flash-write current				5	mA
$I_{FLASHERASE}$	Flash-erase current				15	mA
Data Flash						
	Data retention		10			Years
	Flash programming write cycles		20000			Cycles
$t_{PROGWORD}$	Word programming time				40	µs
$t_{MASSERASE}$	Mass-erase time				40	ms
$t_{PAGEERASE}$	Page-erase time				40	ms
$t_{FLASHREAD}$	Flash-read current				1	mA
$t_{FLASHWRITE}$	Flash-write current				5	mA
$I_{FLASHERASE}$	Flash-erase current				15	mA
ECC Authentication						
$I_{NORMAL+AUTH}$	NORMAL mode + Authentication	CPU active, CHG on. DSG on, High Frequency Oscillator on, Low Frequency Oscillator on, REG18 on, ADC on, ADC_Filter on, CC_Filter on, CC on, SMBus not active, Authentication Start		1350		µA

5.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2V to 32V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_{SIGN}	EC-KCDSA signature signing time	3.8V < VCC or BAT < 32V		375		ms
	Number of Authentication operations		20000			Operations

5.6 Typical Characteristics

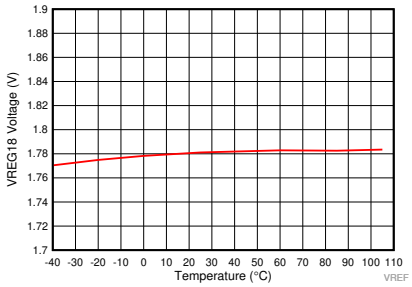


Figure 5-1. VREG 1.8V Voltage vs Temperature

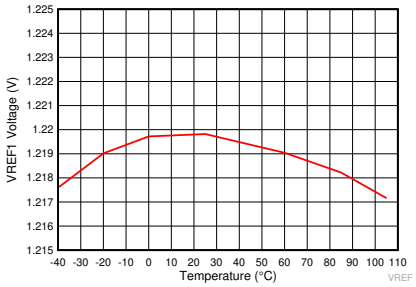


Figure 5-2. VREF 1 Voltage vs Temperature

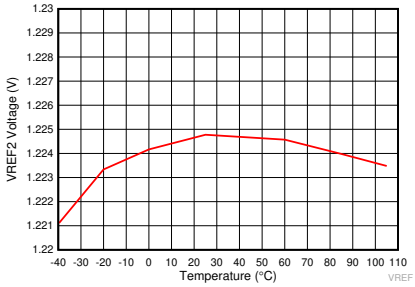


Figure 5-3. VREF 2 Voltage vs Temperature

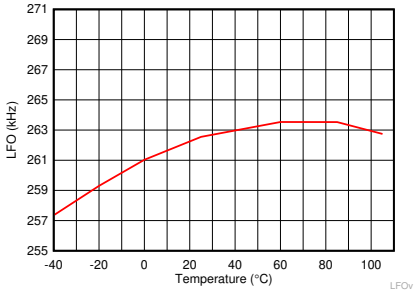


Figure 5-4. Low-Frequency Oscillator vs Temperature

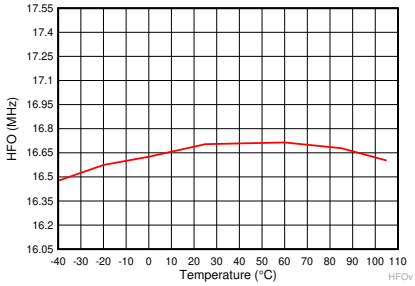


Figure 5-5. High-Frequency Oscillator vs Temperature

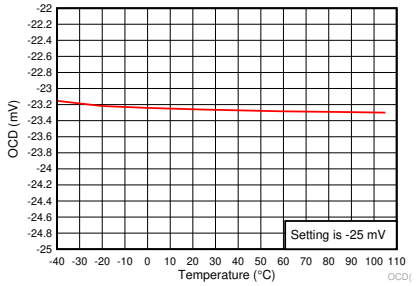


Figure 5-6. Overcurrent Discharge Protection Threshold vs Temperature

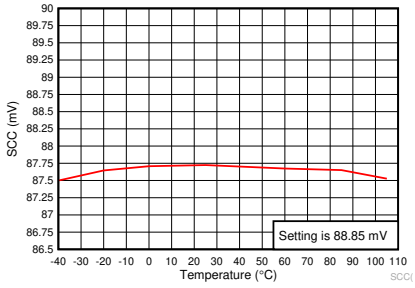


Figure 5-7. Short Circuit Charge Protection Threshold vs Temperature

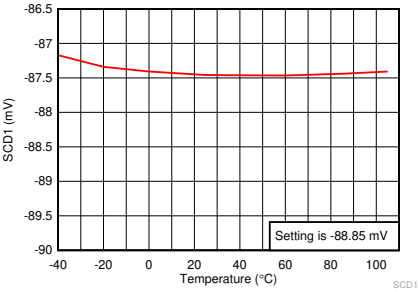
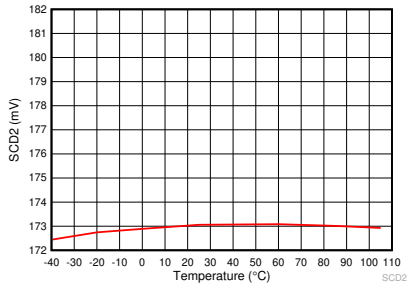


Figure 5-8. Short Circuit Discharge 1 Protection Threshold vs Temperature



Threshold setting is –177.7mV.

Figure 5-9. Short Circuit Discharge 2 Protection Threshold vs Temperature

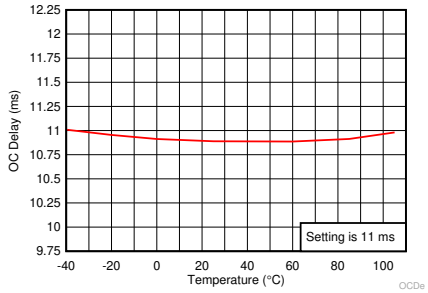


Figure 5-10. Overcurrent Delay Time vs Temperature

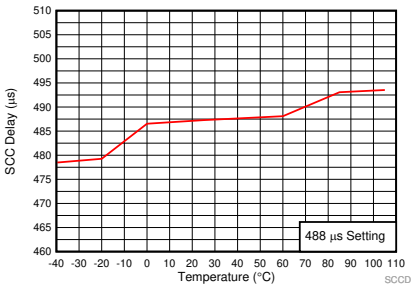


Figure 5-11. Short Circuit Charge Current Delay Time vs Temperature

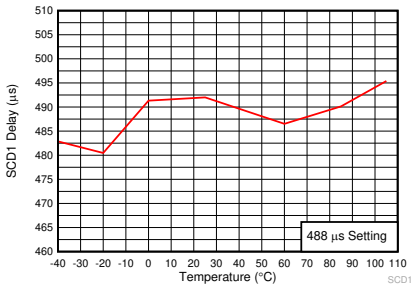


Figure 5-12. Short Circuit Discharge 1 Delay Time vs Temperature

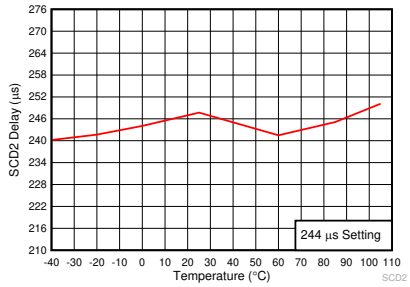


Figure 5-13. Short Circuit Discharge 2 Delay Time vs Temperature

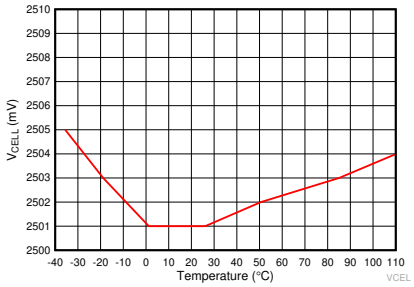
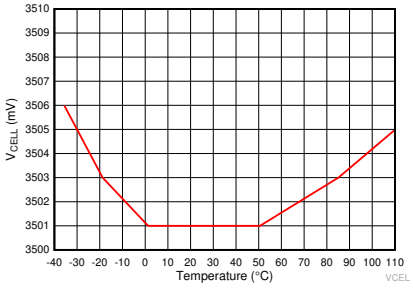
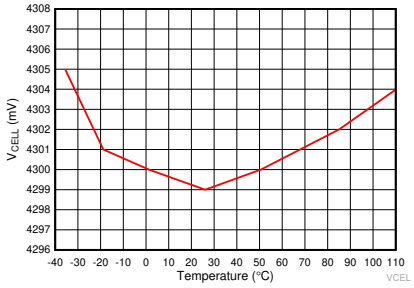


Figure 5-14. V_{CELL} Measurement at 2.5V vs Temperature



This is the V_{CELL} average for single cell.

Figure 5-15. V_{CELL} Measurement at 3.5V vs Temperature



This is the V_{CELL} average for single cell.

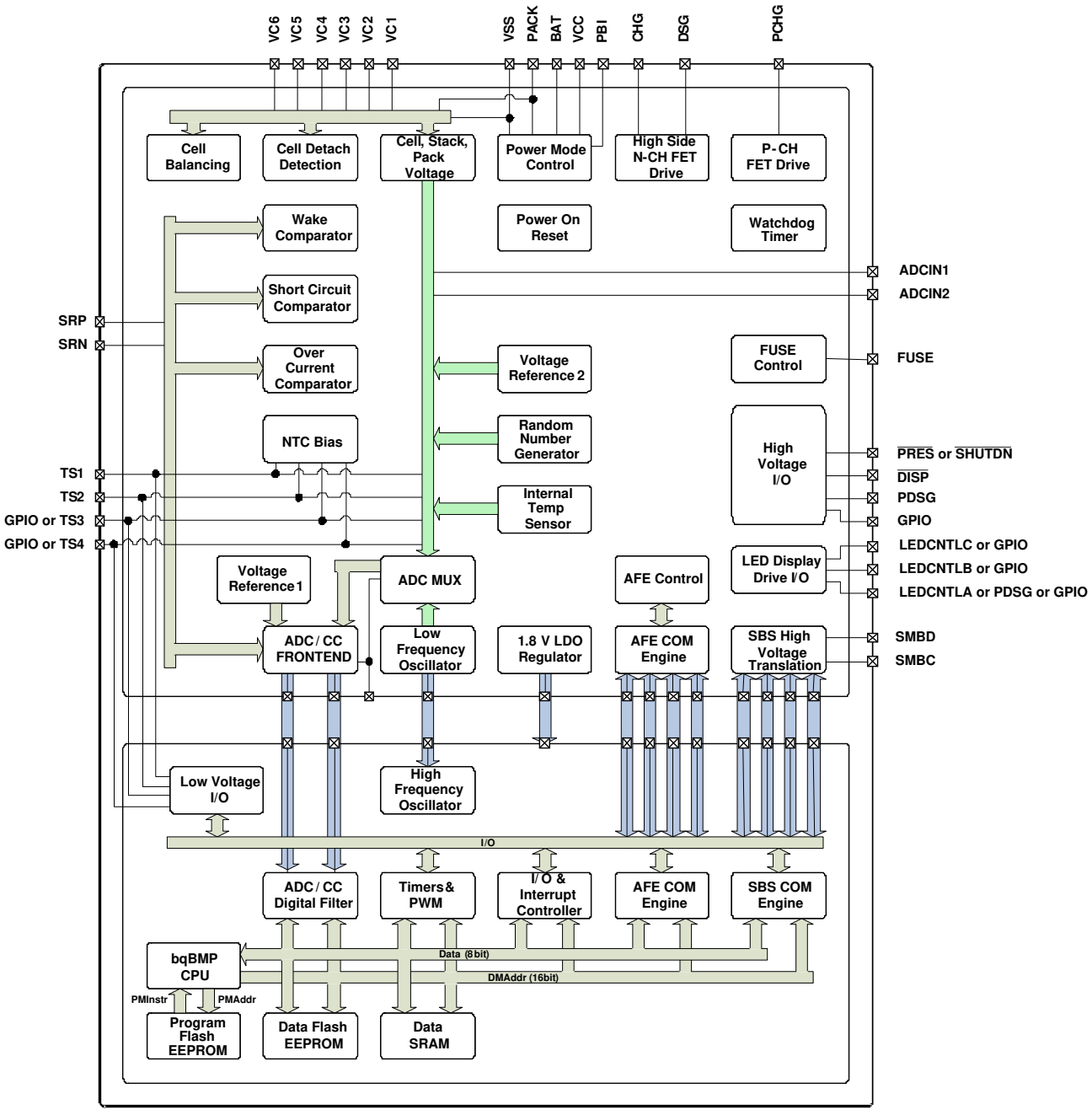
Figure 5-16. V_{CELL} Measurement at 4.3V vs Temperature

6 Detailed Description

6.1 Overview

The BQ40Z80 device, incorporating patented Impedance Track technology, provides cell balancing while charging or at rest. This fully integrated, single-chip, PACK-based choice provides a rich array of features for gas gauging, protection, and authentication for 2-series to 7-series cell Li-Ion and Li-Polymer battery packs, including a diagnostic lifetime data monitor and black box recorder.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Primary (1st Level) Safety Features

The BQ40Z80 supports a wide range of battery and system protection features that can easily be configured. See the *BQ40Z80 Technical Reference Manual* (SLUUBT5) for detailed descriptions of each protection function.

The primary safety features include:

- Cell overvoltage protection
- Cell undervoltage protection
- Cell undervoltage protection compensated
- Overcurrent in charge protection
- Overcurrent in discharge protection
- Overload in discharge protection
- Short circuit in charge protection
- Short circuit in discharge protection
- Overtemperature in charge protection
- Overtemperature in discharge protection
- Undertemperature in charge protection
- Undertemperature in discharge protection
- Overtemperature FET protection
- Precharge timeout protection
- Host watchdog timeout protection
- Fast charge timeout protection
- Overcharge protection
- Overcharging voltage protection
- Overcharging current protection
- Over Precharge current protection

6.3.2 Secondary (2nd Level) Safety Features

The secondary safety features of the BQ40Z80 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. See the *BQ40Z80 Technical Reference Manual* (SLUUBT5) for detailed descriptions of each protection function.

The secondary safety features provide protection against:

- Safety overvoltage permanent failure
- Safety undervoltage permanent failure
- Safety overtemperature permanent failure
- Safety FET overtemperature permanent failure
- Qmax imbalance permanent failure
- Impedance imbalance permanent failure
- Capacity degradation permanent failure
- Cell balancing permanent failure
- Fuse failure permanent failure
- Voltage imbalance at rest permanent failure
- Voltage imbalance active permanent failure
- Charge FET permanent failure
- Discharge FET permanent failure
- AFE register permanent failure
- AFE communication permanent failure
- Second level protector permanent failure
- Instruction flash checksum permanent failure
- Open cell connection permanent failure
- Data flash permanent failure
- Open thermistor permanent failure

6.3.3 Charge Control Features

The BQ40Z80 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduces the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicates charge status via charge and discharge alarms

6.3.4 Gas Gauging

The BQ40Z80 uses the Impedance Track algorithm to measure and calculate the available capacity in battery cells. The BQ40Z80 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The BQ40Z80 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature. The device also has TURBO Mode 2.0/DBPTv2 support, which enables the BQ40Z80 to provide the necessary data for the MCU to determine what level of peak power consumption can be applied without causing a system reset or transient battery voltage level spike to trigger termination flags. See the *BQ40Z80 Technical Reference Manual* (SLUUBT5) for further details.

6.3.5 Multifunction Pins

The BQ40Z80 includes several multifunction pins that firmware uses to implement different functions. Figure 6-1 is a simplified schematic of an example system implementation that uses a 6-series pack with PRECHARGE mode, six LEDs, two thermistors, and system-present functionality.

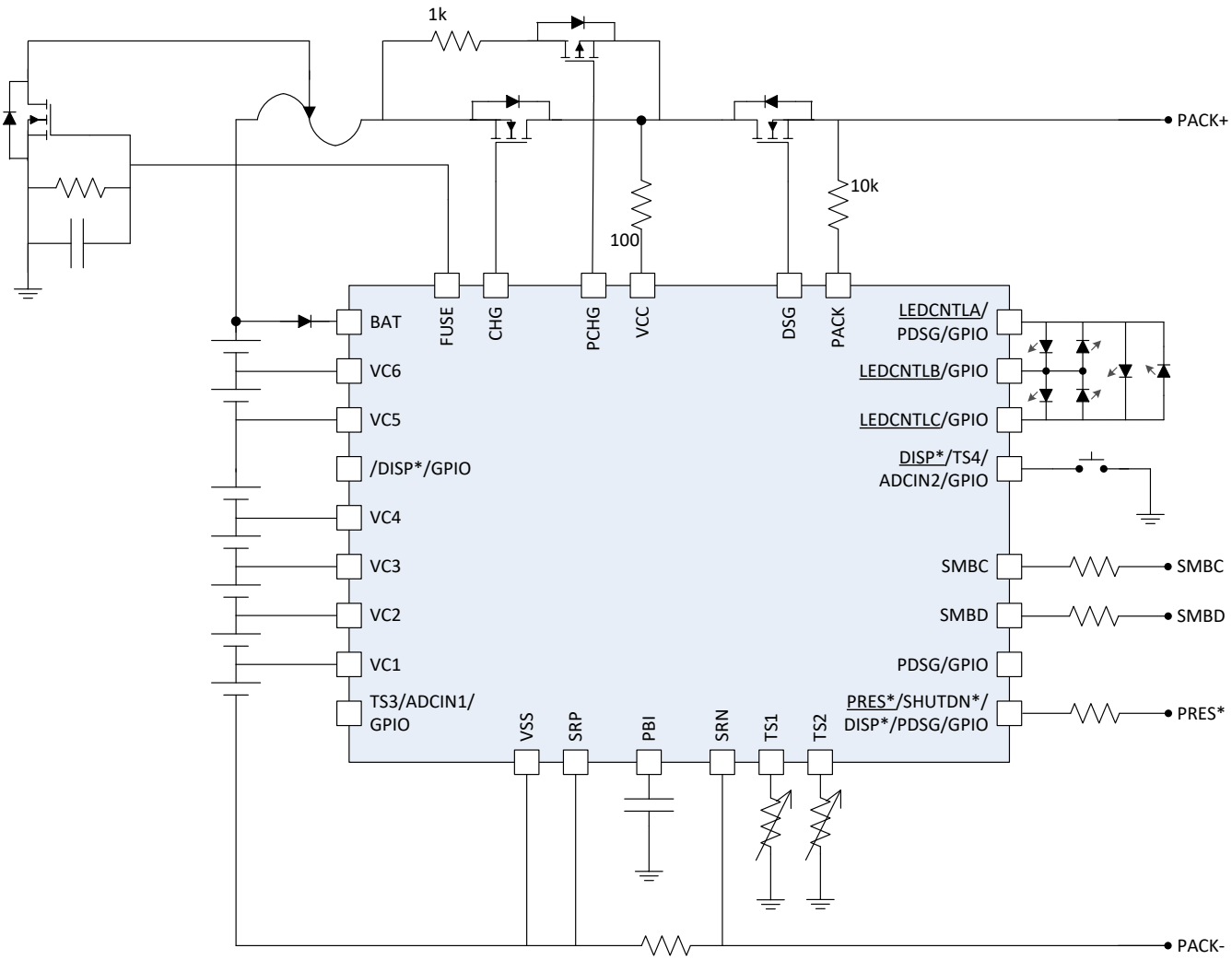


Figure 6-1. Simplified Schematic of a BQ40Z80 Configuration

Table 6-1 shows a summary of other common configurations.

Table 6-1. BQ40Z80 Multifunction Pin Combinations

Number of Cells (with Balancing)	Number of Thermistors	LEDs	LED Button	Pre-Discharge	SYSPRES
2S–6S	4	Yes	Yes (use $\overline{\text{DISP}}$)	Yes (uses PDSG)	Yes

6.3.6 Configuration

6.3.6.1 Oscillator Function

The BQ40Z80 fully integrates the system oscillators and does not require any external components to support this feature.

6.3.6.2 System Present Operation

The BQ40Z80 checks the $\overline{\text{PRES}}$ pin periodically (1s). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the BQ40Z80 detects this as system present.

6.3.6.3 Emergency Shutdown

For battery maintenance, the emergency shutdown feature enables a push button action connecting the $\overline{\text{SHUTDN}}$ pin to shut down an embedded battery pack system before removing the battery. A high-to-low

transition of the $\overline{\text{SHUTDN}}$ pin signals the BQ40Z80 to turn off both CHG and DSG FETs, disconnecting the power from the system to safely remove the battery pack. The CHG and DSG FETs can be turned on again by another high-to-low transition detected by the $\overline{\text{SHUTDN}}$ pin or when a data flash configurable timeout is reached.

6.3.6.4 2-Series, 3-Series, 4-Series, 5-Series, or 6-Series Cell Configuration

In a 2-series cell configuration, VC6 is shorted to VC5, VC4, VC3, and VC2. In a 3-series cell configuration, VC6 is shorted to VC5, VC4, and VC3. In a 4-series cell configuration, VC6 is shorted to VC5 and VC4. In a 5-series cell configuration, VC6 is shorted to VC5.

6.3.6.5 Cell Balancing

For up to a 6-series cell configuration, the device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device's internal bypass is used, up to 10mA can be bypassed and multiple cells can be bypassed at the same time. A higher cell balance current can be achieved by using an external cell balancing circuit. In EXTERNAL CELL BALANCING mode, only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge needed to be bypassed to balance the capacity of all cells.

6.3.7 Battery Parameter Measurements

6.3.7.1 Charge and Discharge Counting

The BQ40Z80 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

The integrating delta-sigma ADC measures the charge and discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN terminals. The integrating ADC measures bipolar signals from –0.1V to 0.1V. The BQ40Z80 detects charge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is negative. The BQ40Z80 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.26nVh.

6.3.8 Lifetime Data Logging Features

The BQ40Z80 offers lifetime data logging for several critical battery parameters. The following parameters are updated every 10 hours if a difference is detected between values in RAM and data flash:

- Maximum and minimum cell voltages
- Maximum delta cell voltage
- Maximum charge current
- Maximum discharge current
- Maximum average discharge current
- Maximum average discharge power
- Maximum and minimum cell temperature
- Maximum delta cell temperature
- Maximum and minimum internal sensor temperature
- Maximum FET temperature
- Number of safety events occurrences and the last cycle of the occurrence
- Number of valid charge termination and the last cycle of the valid charge termination
- Number of Qmax and Ra updates and the last cycle of the Qmax and Ra updates
- Number of shutdown events
- Cell balancing time for each cell, this data is updated every two hours if a difference is detected
- Total FW runtime and time spent in each temperature range, this data is updated every two hours if a difference is detected

6.3.9 Authentication

To support host authentication, the BQ40Z80 uses Elliptic Curve Cryptography (ECC), which requires a strong 163-bit key system for the authentication process. Additionally, the private key is required to be stored only in

the BQ40Z80 Battery Pack Manager, which makes key management more simple and secure. See the *BQ40Z80 Technical Reference Manual* (SLUUBT5) for further details.

6.3.10 Tamper Protection

The BQ40Z80 device contains the Tamper Protection safety feature, which is intended to prevent the hacking of security keys used in battery authentication. This safety feature is triggered if the absolute maximum voltage is exceeded on the TS1, TS2, TS3, or TS4 pins, resulting in erasing the device data flash and terminating communication with the device. The Tamper Protection safety feature is only triggered if this voltage is observed for at least 1us.

6.3.11 LED Display

The BQ40Z80 drives a 3-, 4-, or 5-segment LED display for remaining capacity indication, or a permanent fail (PF) error code indication.

6.3.12 IATA Support

The BQ40Z80 supports IATA with several new commands and procedures. See the *BQ40Z80 Technical Reference Manual* for further details.

6.3.13 Voltage

The BQ40Z80 updates the individual series cell voltages at a 1-second interval. The internal ADC of the BQ40Z80 measures the voltage, and is designed to scale and calibrate the voltage. This data is also used to calculate the impedance of the cell for the Impedance Track gas gauging.

6.3.14 Current

The BQ40Z80 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 1mΩ to 3mΩ typ. sense resistor.

6.3.15 Temperature

The BQ40Z80 contains an internal temperature sensor and inputs for up to four external temperature sensors. All five temperature sensor options can be individually enabled and configured for cell or FET temperature usage. Two configurable thermistor models are provided to allow the monitoring of cell temperature in addition to FET temperature, which use a different thermistor profile.

6.3.16 Communications

The BQ40Z80 uses SMBus v1.1 with MASTER mode and packet error checking (PEC) options per the SBS specification.

6.3.16.1 SMBus On and Off State

The BQ40Z80 detects an SMBus off state when SMBC and SMBD are low for two or more seconds. Clearing the off state requires either SMBC or SMBD to transition high. The communication bus resumes activity within 1ms.

6.3.16.2 SBS Commands

See the *BQ40Z80 Technical Reference Manual* (SLUUBT5) for further details.

6.4 Device Functional Modes

The BQ40Z80 supports three power modes to reduce power consumption:

- In NORMAL mode, the BQ40Z80 performs measurements, calculations, protection decisions, and data updates in 250ms intervals. Between these intervals, the BQ40Z80 is in a reduced power stage.
- In SLEEP mode, the BQ40Z80 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the BQ40Z80 is in a reduced power stage. The BQ40Z80 has a wake function that enables exit from SLEEP mode when current flow or failure is detected.
- In SHUTDOWN mode, the BQ40Z80 is completely disabled.

7 Applications and Implementation

7.1 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.2 Application Information

The BQ40Z80 is a gas gauge with primary protection support, and can be used with a 2-series to 6-series Li-ion/Li-polymer battery pack. To implement and design a comprehensive set of parameters for a specific battery pack, install the Battery Management Studio (BQSTUDIO) graphical user-interface tool on a PC during development.

7.3 Typical Applications

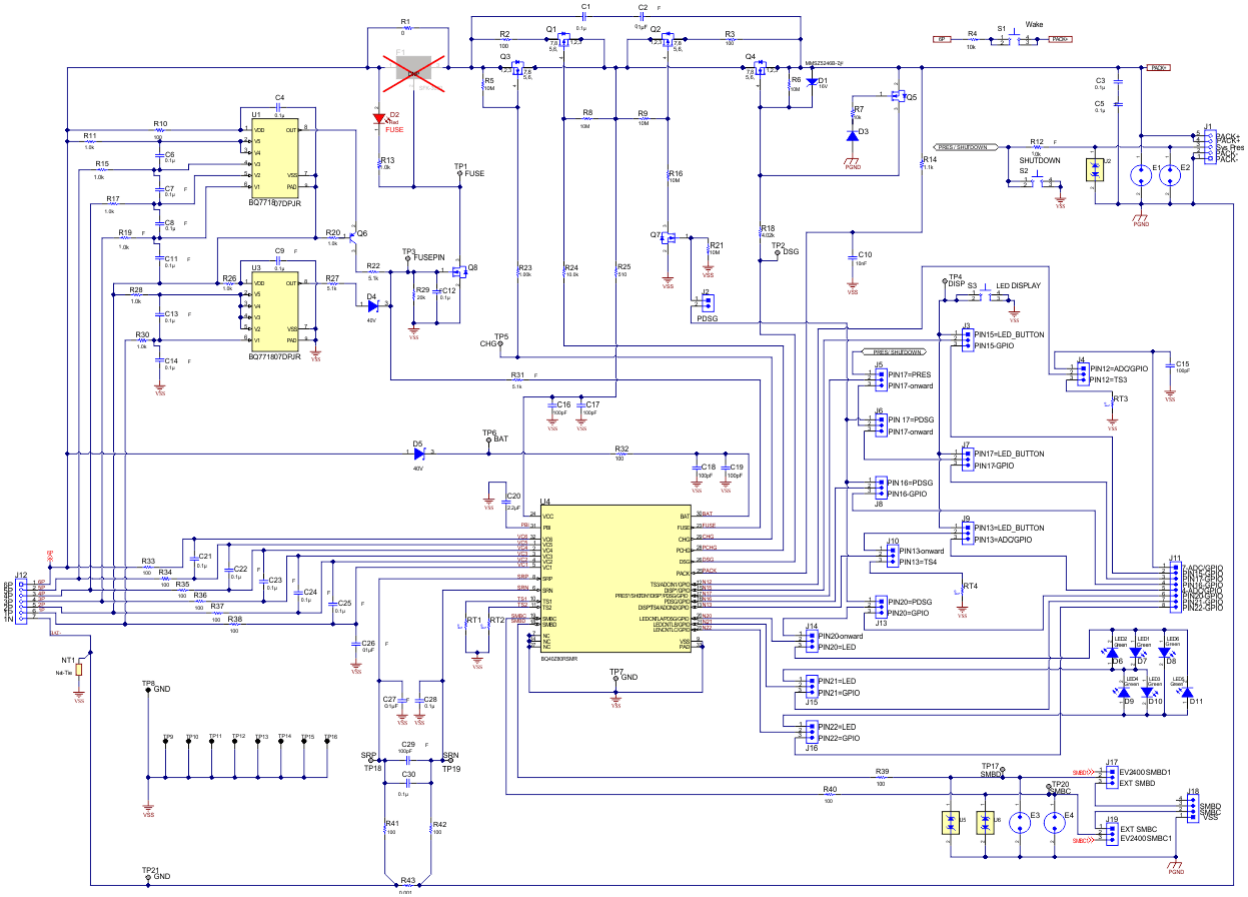


Figure 7-1. BQ40Z80EVM Gauge and Protector Schematic

7.3.1 Design Requirements

Table 7-1 shows the default settings for the main parameters. Use the BQSTUDIO tool to update the settings to meet the specific application or battery pack configuration requirements.

Calibrate the device before any gauging test. Follow the BQSTUDIO *Calibration* page to calibrate the device, and use the BQSTUDIO *Chemistry* page to update the match chemistry profile to the device. *Design Parameters* shows all of the settings that are configurable in BQSTUDIO and in the BQ40Z80 firmware.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE
Cell configuration	6s (6-series)(1)
Design capacity	6000mAh
Device chemistry	1210 ($LiCoO_2$/graphitized carbon)
Cell overvoltage at standard temperature	4300mV
Cell undervoltage	2500mV
Shutdown voltage	2300mV
Overcurrent in CHARGE mode	6000mA
Overcurrent in DISCHARGE mode	–6000mA
Short circuit in CHARGE mode	0.1V/Rsense across SRP, SRN
Short circuit in DISCHARGE mode	0.1V/Rsense across SRP, SRN
Safety overvoltage	4500mV
Cell balancing	Disabled
Internal and external temperature sensor	External temperature sensor is used
Undertemperature charging	0°C
Undertemperature discharging	0°C
BROADCAST mode	Disabled

(1) When using the device the first time with a 1s or 2s battery pack, connect a charger or power supply to the PACK+ terminal to prevent device shutdown. Then update the cell configuration (see the *BQ40Z80 Technical Reference Manual*] for details) before removing the charger connection.

7.3.2 Detailed Design Procedure

This application section uses the *BQ40Z80 Li-Ion Battery Pack Manager Evaluation Module* EVM user's guide and jumper configurations to allow the user to evaluate many of the BQ40Z80 features.

7.3.2.1 Using the BQ40Z80EVM with BQSTUDIO

The firmware installed on the BQSTUDIO tool uses BQ40Z80 default values; a summary is provided in the *BQ40Z80 Technical Reference Manual* (SLUUBT5). Using the BQSTUDIO tool, change the default values to cater to specific application requirements during development once the system parameters are known. System parameter options include fault trigger thresholds for protection, enable and disable of certain features for operation, configuration of cells, and chemistry that best matches the cell.

7.3.2.2 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, the charge current continues through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, and the sense resistor, and then returns to the PACK– terminal. In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

7.3.2.2.1 Protection FETs

Select the N-channel charge and discharge FETs for a given application. For a 7-series cell application, the charge FET must be rated above the max voltage, and for this reason the TI CSD18504Q5A is used. The TI CSD18504Q5A is a 50A, 40V device with Rds(on) of 5.3mΩ when the gate drive voltage is 10V. The discharge

FET may undergo a higher voltage; use the TI CSD18540Q5B. The TI CSD18540Q5B is a 100A, 60V device with Rds(on) of 1.8mΩ when the gate drive voltage is 10V.

If a precharge FET is used, R2 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to $(V_{CHARGER} – V_{BAT})/R2$ and maximum power dissipation is $(V_{CHARGER} – V_{BAT})^2/R2$.

The gates of all protection FETs are pulled to the source with a high-value resistor between the gate and source to confirm the FETs are turned off if the gate drive is open.

Capacitors C1 and C2 help protect the FETs during an ESD event. Using two devices provides normal operation if one device is shorted. Design the copper trace inductance of the capacitor leads to be as short and wide as possible for good ESD protection. Confirm that the voltage rating of both C1 and C2 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

7.3.2.2.2 Chemical Fuse

The chemical fuse (Dexerials, Uchihashi, and so forth) is ignited under command from either the bq771800 secondary voltage protection IC or from the FUSE pin of the gas gauge. Either of these ignition events applies a positive voltage to the gate of Q9, which then sinks current from the third terminal of the fuse, causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-channel FET. Verify that the proper voltage, current, and Rds(on) ratings are used for this device. The fuse control circuit is discussed in detail in *Section 7.3.2.3.5*.

7.3.2.2.3 Lithium-Ion Cell Connections

The important part about the cell connections is that high current flows through the top and bottom connections; therefore, the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. The location marked 6P indicates the Kelvin connection of the most positive directly measured battery node. The single-point connection at 1N to the low-current ground is needed to avoid an undesired voltage drop through long traces while the gas gauge is measuring the bottom cell voltage.

7.3.2.2.4 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50ppm to minimize current measurement drift with temperature. Select the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the BQ40Z80. Select the smallest value possible to minimize the negative voltage generated on the BQ40Z80 V_{SS} nodes during a short circuit. This pin has an absolute minimum of –0.3V. Parallel resistors can be used as long as good Kelvin sensing is maintained. The device is designed to support a 1mΩ to 3mΩ sense resistor, and a 1mΩ sense resistor is used, shown as R52. When using 1mΩ, large currents during a short circuit event can cause the voltage across the sense resistor to exceed the absolute maximum of the pin. Therefore, placing 100Ω series resistors R47 and R48 are required, as shown in the schematic.

7.3.2.2.5 ESD Mitigation

A pair of series 0.1µF ceramic capacitors is placed across the PACK+ and PACK– terminals to mitigate external electrostatic discharges. The two devices in series provide continued operation of the pack if one of the capacitors is shorted.

Optionally, place a transorb such as the SMBJ2A across the terminals to improve ESD immunity.

7.3.2.3 Gas Gauge Circuit

The gas gauge circuit includes the BQ40Z80 and peripheral components. The peripheral components are divided into the following groups:

- Differential low-pass filter
- PBI
- System present

- SMBus communication
- FUSE circuit
- LED

7.3.2.3.1 Coulomb-Counting Interface

The BQ40Z80 uses an integrating delta-sigma ADC for current measurements. Add a 100Ω resistor from the sense resistor to the SRP and SRN inputs of the device. Place a 100pF (C29) filter capacitor across the SRP and SRN inputs. Add 0.1µF filter capacitors (C26 and C27) for additional noise filtering, if required for the circuit.

7.3.2.3.2 Power Supply Decoupling and PBI

The BQ40Z80 has an internal LDO that is internally compensated and does not require an external decoupling capacitor.

The PBI pin is used as a power supply backup input pin providing power during brief transient power outages. A standard 2.2µF ceramic capacitor is connected from the PBI pin to ground.

7.3.2.3.3 System Present

The System Present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The $\overline{\text{PRES}}$ pin of the BQ40Z80 is used if J5[1, 2] jumper is installed, and is occasionally sampled to test for system present. To save power, an internal pullup is provided by the gas gauge during a 4µs sampling pulse once per second. Use a resistor to pull the signal low; the resistance must be 20kΩ or lower to verify that the test pulse is lower than the VIL limit. The pullup current source is typically 10µA to 20µA.

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. An integrated ESD protection on the $\overline{\text{PRES}}$ device pin reduces the external protection requirement to R12 for an 8kV ESD contact rating. If it is possible that the System Present signal shorts to PACK+, include an E2 spark gap for high-voltage protection.

7.3.2.3.4 SMBus Communication

The SMBus clock and data pins have integrated high-voltage ESD protection circuits; however, adding a ESD protection device, TPD1E10B06D (U5 and U6) and series resistor (R50 and R51), provides more robust ESD performance.

The SMBus clock and data lines have an internal pulldown. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into SLEEP mode to conserve power.

7.3.2.3.5 FUSE Circuitry

The FUSE pin of the BQ40Z80 is designed to ignite the chemical fuse if one of the various safety criteria is violated. The FUSE pin also monitors the state of the secondary-voltage protection IC. Q9 ignites the chemical fuse when the Q9 gate is high. The output of the bq7718xx is divided by R22 and R30, which provides adequate gate drive for Q9 while guarding against excessive back current into the bq7718xx if the FUSE signal is high.

Using C8 is generally a good practice, especially for RFI immunity. C8 can be removed because the chemical fuse is a comparatively slow device and is not affected by any sub-microsecond glitches that come from the FUSE output during the cell connection process.

If the AFEFUSE output is not used, connect the output to the VSS.

When the BQ40Z80 is commanded to ignite the chemical fuse, the FUSE pin activates to release a typical 8V output.

7.3.2.4 Secondary-Current Protection

The BQ40Z80 provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, and voltage translation. The following discussion examines cell and battery inputs, pack and FET control, temperature output, and cell balancing.

7.3.2.4.1 Cell and Battery Inputs

Each cell input is conditioned with a simple RC filter, which provides ESD protection during cell connect and acts to filter unwanted voltage transients. The resistor value allows some trade-off for cell balancing versus safety protection.

The BQ40Z80 has integrated cell balancing FETs The internal cell balancing FETs allow the AFE to bypass cell current around a given cell or numerous cells. External series resistors placed between the cell connections and the VCx I/O pins set the balancing current magnitude. The internal FETs provide a 200Ω resistance (2V < VDS < 4V). Series input resistors between 100Ω and 1kΩ are recommended for effective cell balancing.

The BAT input uses a diode (D6) to isolate and decouple the input from the cells, in the event of a transient dip in voltage caused by a short-circuit event.

7.3.2.4.2 External Cell Balancing

Internal cell balancing can only support up to 10mA. External cell balancing provides another option for faster cell balancing. For details, refer to the *Fast Cell Balancing Using External MOSFET* application note.

7.3.2.4.3 PACK and FET Control

The PACK and V_{CC} inputs provide power to the BQ40Z80 from the charger. The PACK input also provides a method to measure and detect the presence of a charger. The PACK input uses a 100Ω resistor. The V_{CC} input uses a diode to guard against input transients and prevents misoperation of the date driver during short-circuit events.

The N-channel charge and discharge FETs are controlled with 10kΩ series gate resistors, which provide a switching time constant of a few microseconds. The 10MΩ resistors confirm that the FETs are off in the event of an open connection to the FET drivers. Q4 is provided to protect the discharge FET (Q3) in the event of a reverse-connected charger. Without Q4, Q3 can be driven into its linear region and suffer severe damage if the PACK+ input becomes slightly negative. Q4 turns on in that case to protect Q3 by shorting its gate to source. To use the simple ground gate circuit, the FET must have a low gate turn-on threshold. If it is desired to use a more standard device, such as the 2N7002, as the reference schematic, bias the gate up to 3.3V with a high-value resistor. The BQ40Z80 device has the capability to provide a current-limited charging path typically used for low battery voltage or low temperature charging. The BQ40Z80 device uses an external P-channel and precharge FET, controlled by PCHG.

7.3.2.4.4 Pre-Discharge Control

Some applications have a large capacitive load that requires a pre-discharge feature that slowly charges the cap and avoids a large current that is capable of tripping the OC protection. The BQ40Z80 device can be configured to use the PDSG output of Pins 16, 17, or 20 to drive the N-channel FET Q7 to turn on the pre-discharge P-channel FET Q5. Adjust the resistor R9 to set the precharge rate.

7.3.2.4.5 Temperature Output

For the BQ40Z80 device, up to four thermistor inputs can be configured. TS1, TS2, TS3, and TS4 provide thermistor drive-under program control. Each pin can be enabled with an integrated 18kΩ (typical) linearization pullup resistor to support the use of a 10kΩ at 25°C (103) NTC external thermistor, such as a Mitsubishi™ BN35-3H103. The reference design includes four 10kΩ thermistors:

- RT1
- RT2
- RT3
- RT4

7.3.2.4.6 LEDs

Multifunction Pins 20, 21, and 22 can be configured as three LED control outputs that provide constant current sinks for driving external LEDs. These outputs are configured to provide voltage and control for up to six LEDs. No external bias voltage is required. Unused LEDCNTL pins can remain open or connect to V_{SS}. If the LED feature is not used, connect the $\overline{DISP}$ pin to the V_{SS}.

7.3.3 Application Curve

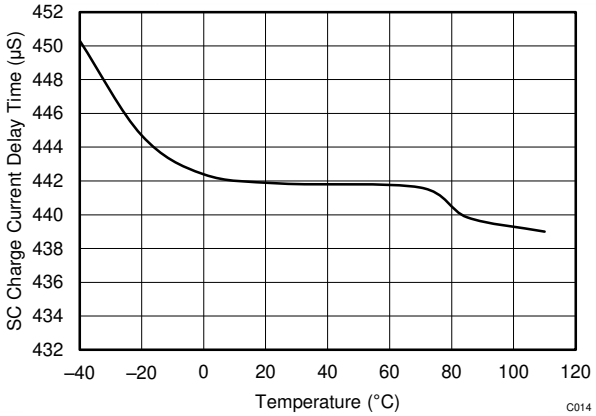


Figure 7-2. Short Circuit Charge Current Delay Time vs Temperature

7.4 Power Supply Recommendations

The device manages the supply voltage dynamically according to the operation conditions. Normally, the BAT input is the primary power source to the device. Connect the BAT pin to the positive termination of the battery stack. The input voltage for the BAT pin ranges from 2.2V to 32V.

The VCC pin is the secondary power input, which activates when the BAT voltage falls below minimum V_{CC}. The activation enables the device to source power from a charger (if present) connected to the PACK pin. Connect the VCC pin to the common drain of the CHG and DSG FETs. Connect the charger input to the PACK pin.

7.5 Layout

7.5.1 Layout Guidelines

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high-current traces and ultra-low current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement, where the high-current section is on the opposite side of the board from the electronic devices. Component placement is shown in Figure 7-3. This component placement is not possible in many situations due to mechanical constraints. Make every attempt to route high-current traces away from signal traces which enter the BQ40Z80 directly. IC references and registers can be disturbed and in rare cases damaged due to magnetic and capacitive coupling from the high-current path.

Note

During surge current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics, as shown in Figure 7-4.

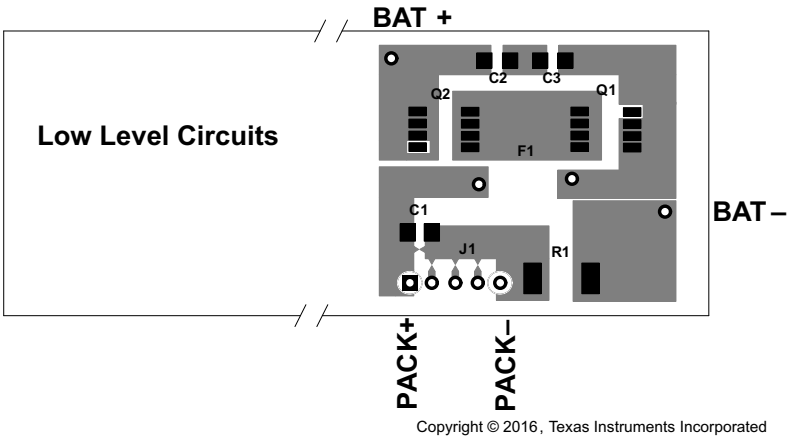


Figure 7-3. Separating High- and Low-Current Sections Provides an Advantage in Noise Immunity

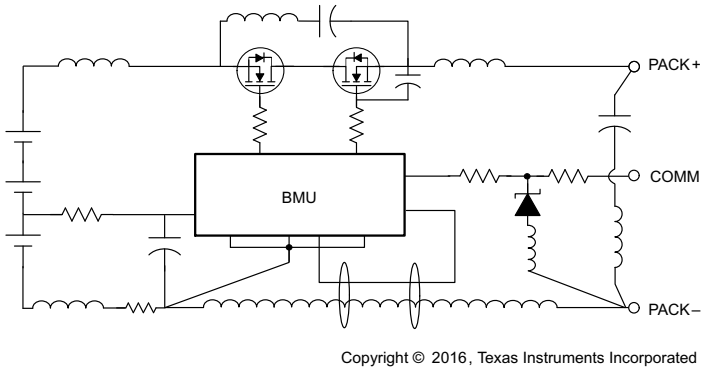


Figure 7-4. Avoid Close Spacing Between High-Current and Low-Level Signal Lines

Kelvin voltage sensing is important to accurately measure current and top and bottom cell voltages. Place all filter components as close as possible to the device. Route the traces from the sense resistor in parallel to the filter circuit. Adding a ground plane around the filter network can add additional noise immunity. Figure 7-5 and Figure 7-6 demonstrate correct kelvin current sensing.

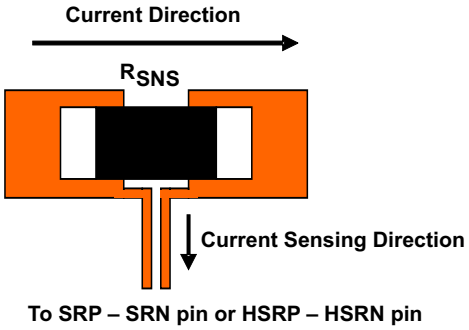


Figure 7-5. Sensing Resistor PCB Layout

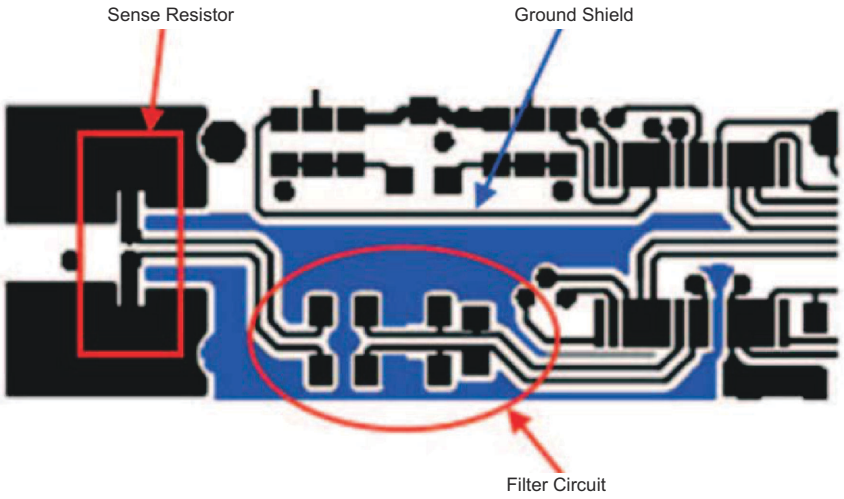


Figure 7-6. Sense Resistor, Ground Shield, and Filter Circuit Layout

7.5.1.1 Protector FET Bypass and Pack Terminal Bypass Capacitors

Use wide copper traces to lower the inductance of the bypass capacitor circuit. This technique is shown in the example layout in Figure 7-7. Note that in the *BQ40Z80EVM-Rev A Schematic*, these capacitors are C1, C2, C3, and C4.

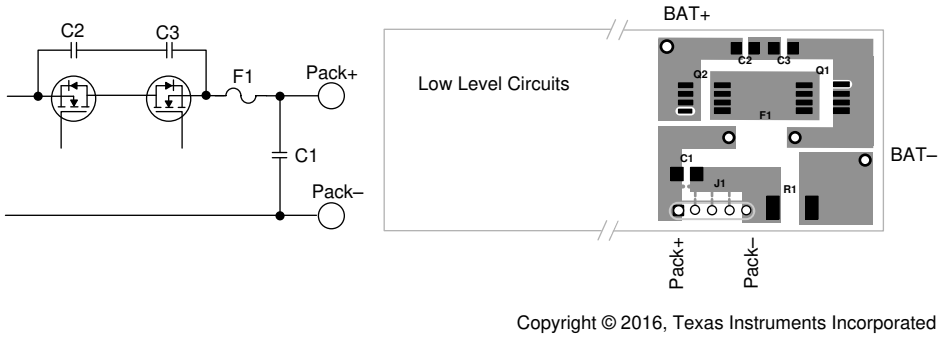


Figure 7-7. Wide Copper Traces Lower the Inductance of Bypass Capacitors C1, C2, and C3

7.5.1.2 ESD Spark Gap

Protect the SMBus clock, data, and other communication lines from ESD with a spark gap at the connector. The pattern in Figure 7-8 is recommended, with 0.2mm spacing between the points.

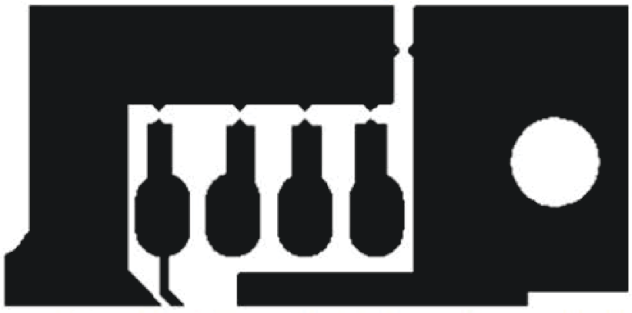


Figure 7-8. Recommended Spark-Gap Pattern Helps Protect Communication Lines from ESD

7.5.2 Layout Examples

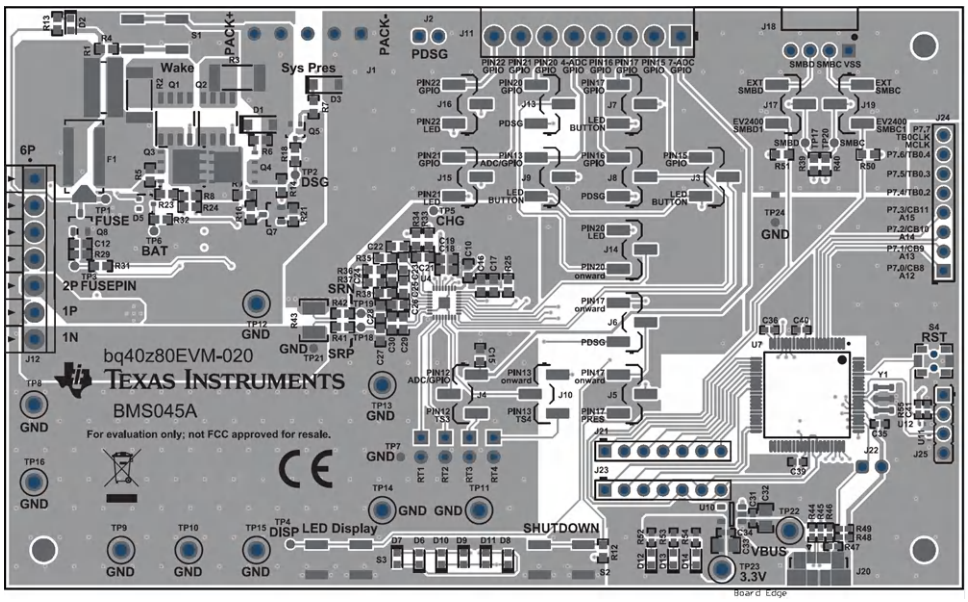


Figure 7-9. BQ40Z80EVM Top Composite

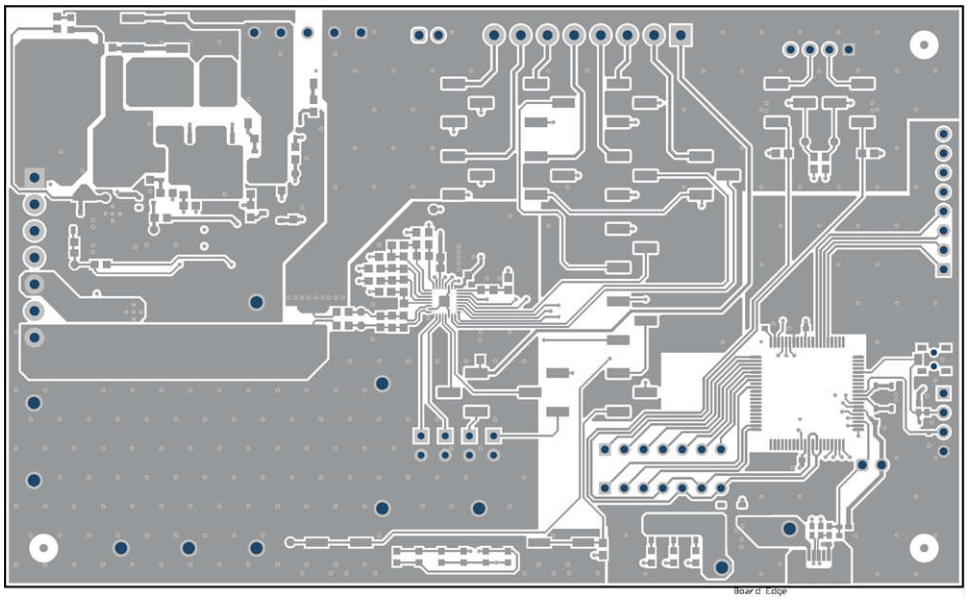


Figure 7-10. BQ40Z80EVM Top Layer

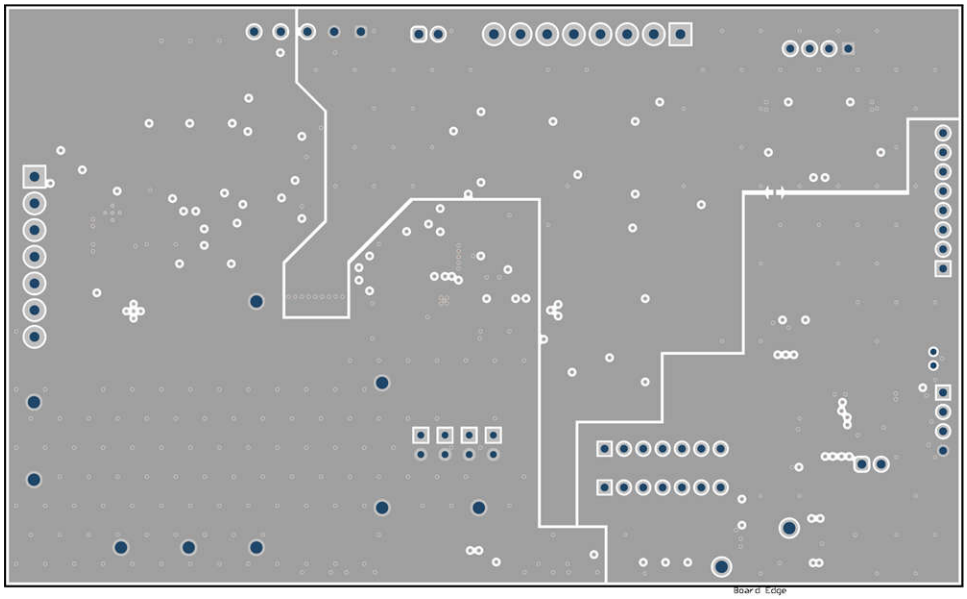


Figure 7-11. BQ40Z80EVM GND Layer

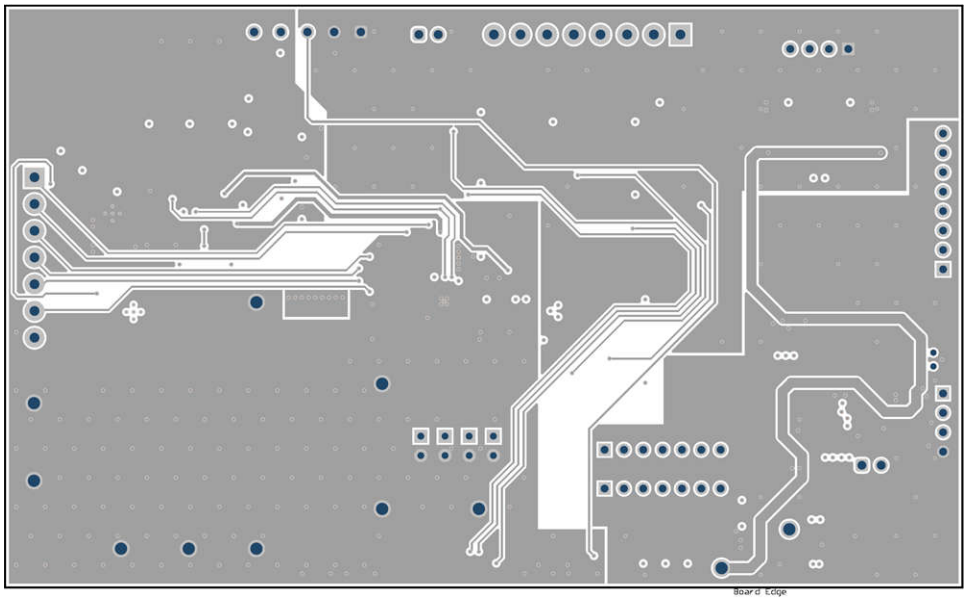


Figure 7-12. BQ40Z80EVM Signal Layer

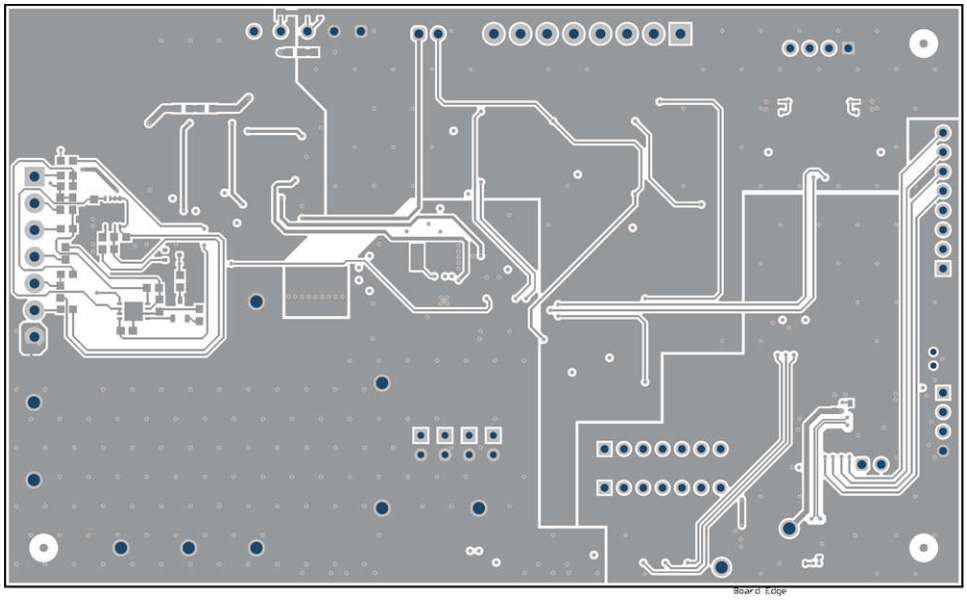


Figure 7-13. BQ40Z80EVM Bottom Layer

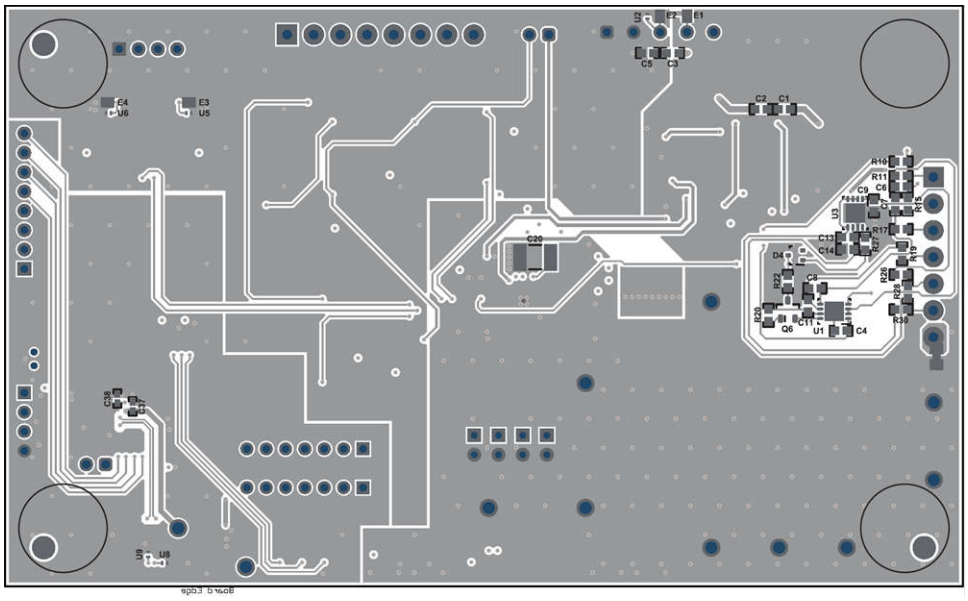


Figure 7-14. BQ40Z80EVM Bottom Layer Composite

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *BQ40Z80 Technical Reference Manual*
- Texas Instruments, *BQ40Z80 Manufacture, Production, and Calibration* application note
- Texas Instruments, *BQ40Z80EVM Li-Ion Battery Pack Manager Evaluation Module* EVM user's guide
- Texas Instruments, *How to Complete a Successful Learning Cycle for the BQ40Z80* application note
- Texas Instruments, *TI Fuel Gauge Authentication Key Packager and Programmer Tools* user's guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

Impedance Track™ and TI E2E™ are trademarks of Texas Instruments.
Mitsubishi™ is a trademark of Mitsubishi Corporation.
Intel® is a registered trademark of Intel Corporation.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2020) to Revision C (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the document to reflect TI technical writing standards	1

- Added *Tamper Protection* section....26

Changes from Revision A (June 2018) to Revision B (September 2020) **Page**

- Deleted the 7-series device option in the data sheet....1
- Changed high-voltage GPIO default from 7-series cell option to GPIO....9
- Deleted 7-series cell option and BQ40Z80 multifunction pin combinations....23
- Changed the 7-series EVM schematic for the 6-series EVM schematic....28
- Updated the layout examples....36

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, package, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ40Z80RSMR	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z80
BQ40Z80RSMR.A	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z80
BQ40Z80RSMR.B	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
BQ40Z80RSMT	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z80
BQ40Z80RSMT.A	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z80
BQ40Z80RSMT.B	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
BQ40Z80RSMTG4	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z80
BQ40Z80RSMTG4.A	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z80
BQ40Z80RSMTG4.B	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

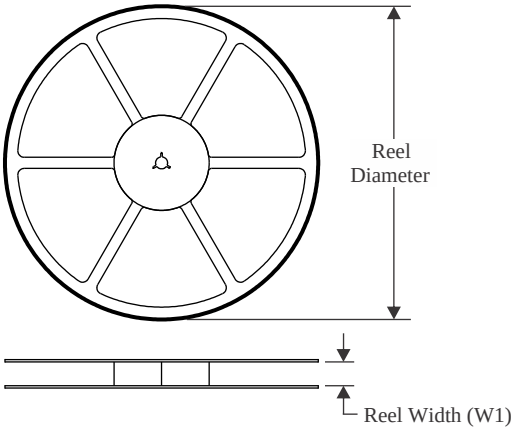
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

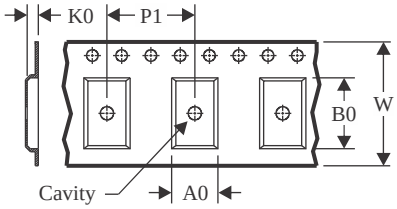
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

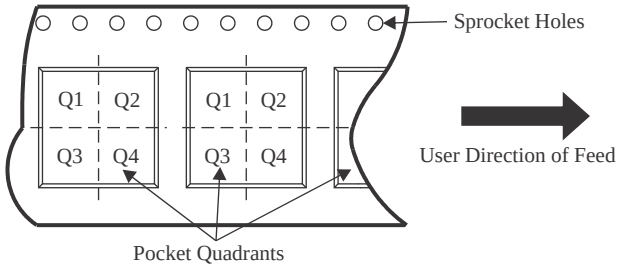


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

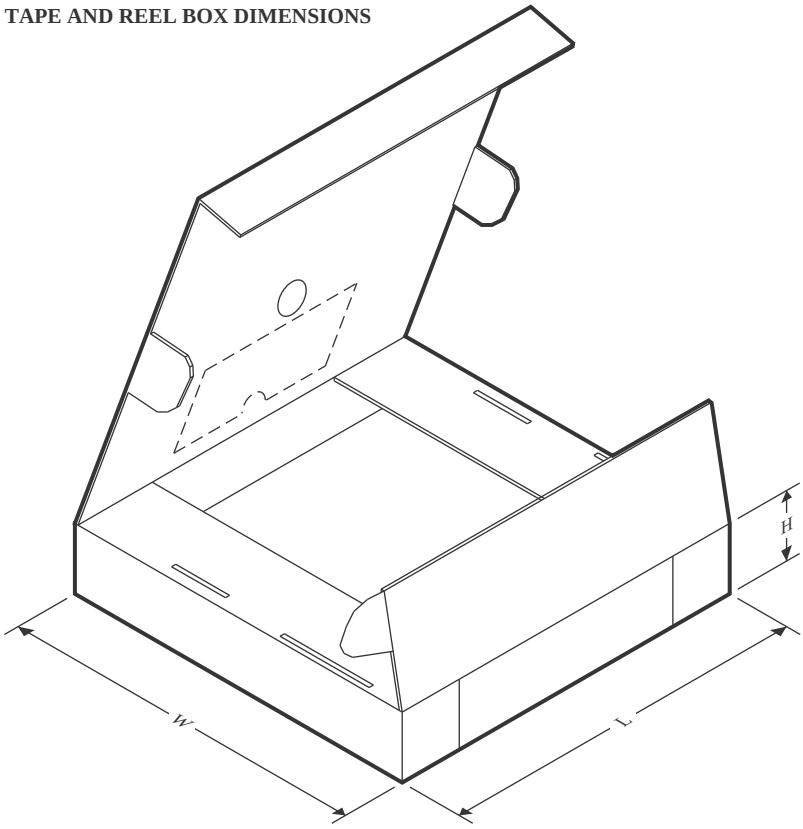
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ40Z80RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ40Z80RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ40Z80RSMTG4	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ40Z80RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
BQ40Z80RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
BQ40Z80RSMTG4	VQFN	RSM	32	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

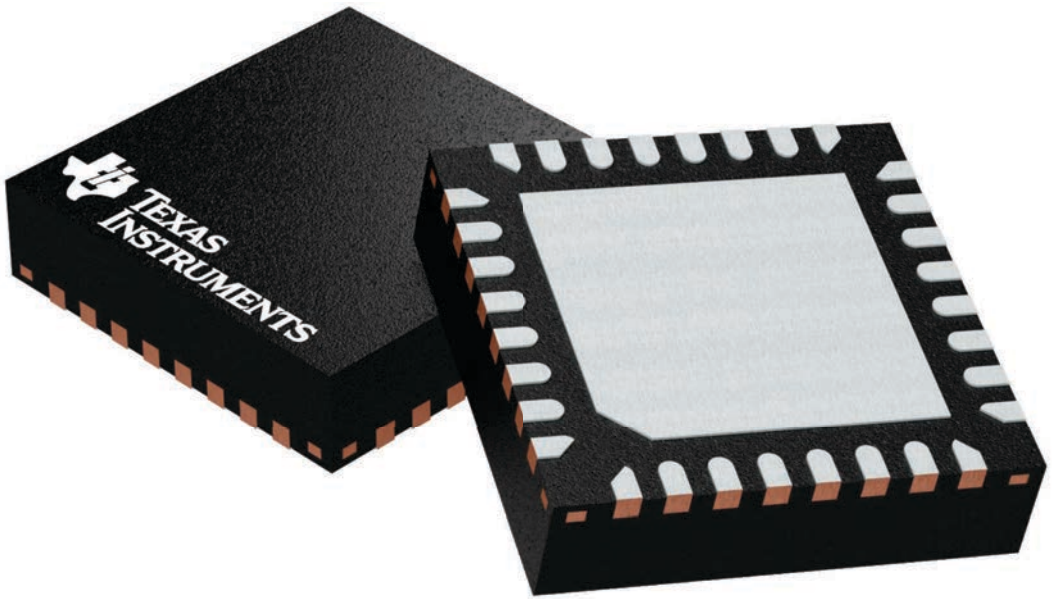
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



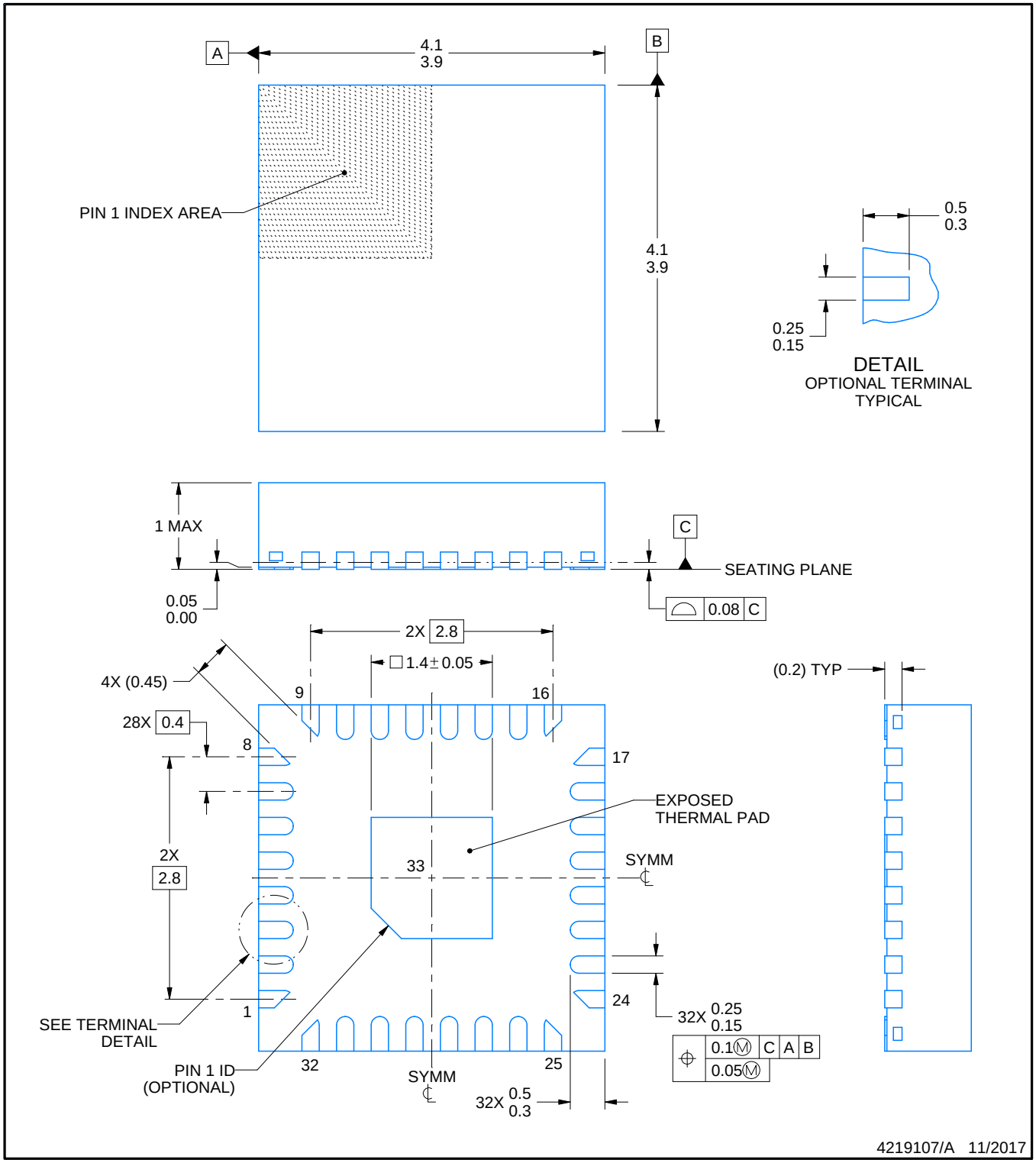
4224982/A

PACKAGE OUTLINE

RSM0032A

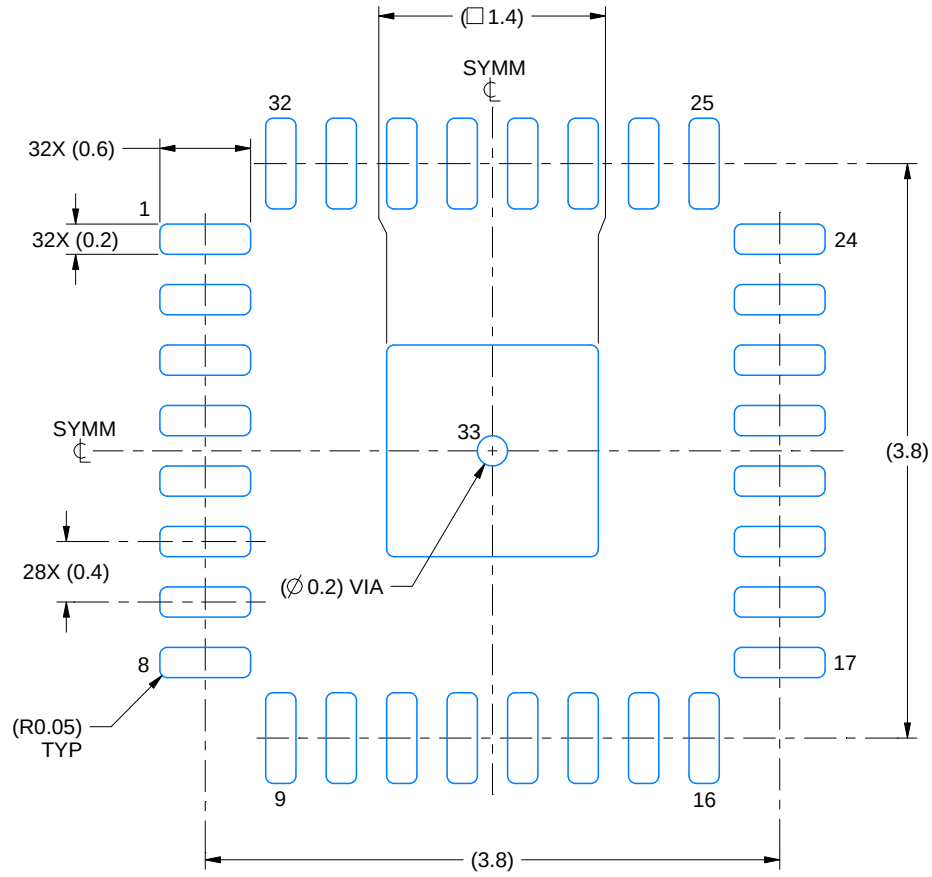
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

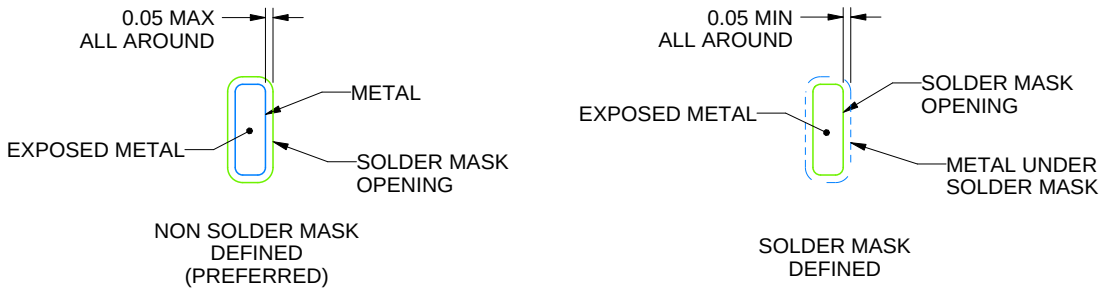


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

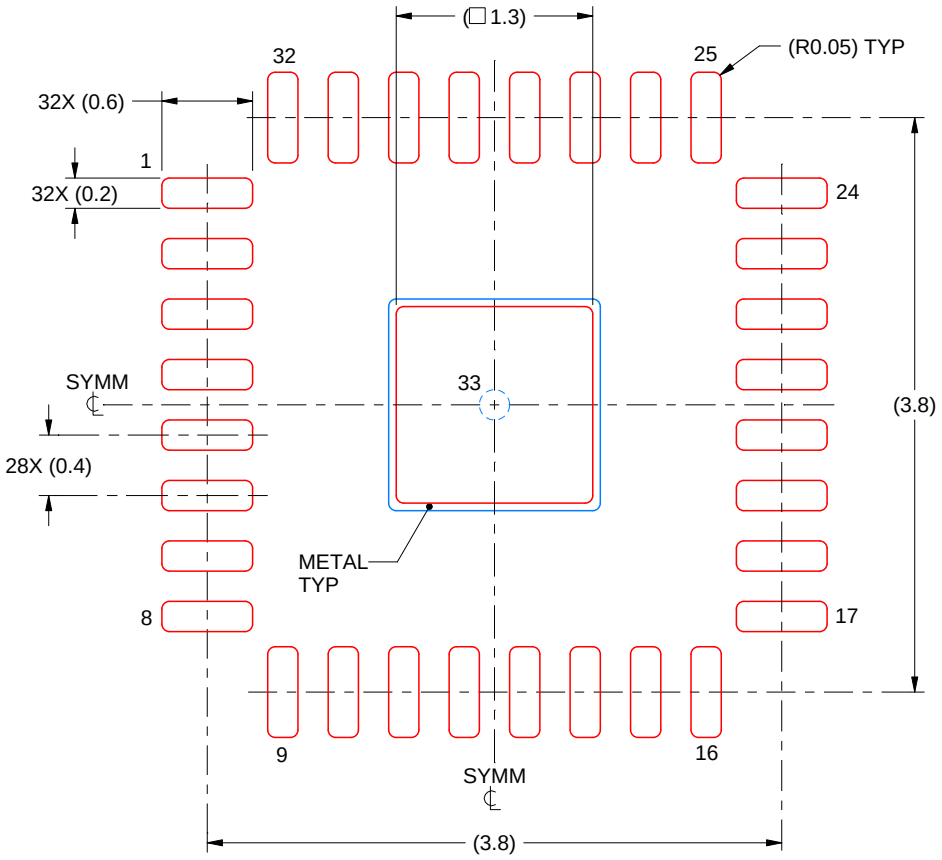


SOLDER MASK DETAILS

4219107/A 11/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219107/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265