











SLUS900E - DECEMBER 2008 - REVISED AUGUST 2015

bq32000

bq32000 Real-Time Clock (RTC)

Features

- Automatic Switchover to Backup Supply
- I²C Interface Supports Serial Clock up to 400 kHz
- Uses 32.768-kHz Crystal With -63-ppm to +126-ppm Adjustment
- Integrated Oscillator-Fail Detection
- 8-Pin SOIC Package
- -40°C to 85°C Ambient Operating Temperature

Applications

General Consumer Electronics

3 Description

The bq32000 device is a compatible replacement for industry standard real-time clocks.

The bq32000 features an automatic backup supply with integrated trickle charger. The backup supply can be implemented using a capacitor or nonrechargeable battery. The bq32000 programmable calibration adjustment from -63 ppm to +126 ppm. The bq32000 registers include an OF (oscillator fail) flag indicating the status of the RTC oscillator, as well as a STOP bit that allows the host processor to disable the oscillator. The time registers are normally updated once per second, and all the registers are updated at the same time to prevent a timekeeping glitch. The bq32000 includes automatic leap-year compensation.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq32000	SOIC (8)	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

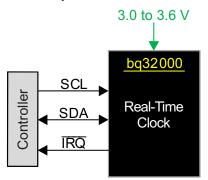




Table of Contents

1	Features 1		7.4 Device Functional Modes	10
2	Applications 1		7.5 Programming	10
3	Description 1		7.6 Register Maps	
4	Revision History2	8	Application and Implementation	19
5	Pin Configuration and Functions		8.1 Application Information	19
5 6	Specifications4		8.2 Typical Application	
U	6.1 Absolute Maximum Ratings 4	9	Power Supply Recommendations	23
	6.2 ESD Ratings		Layout	
	6.3 Recommended Operating Conditions		10.1 Layout Guidelines	
	6.4 Thermal Information		10.2 Layout Example	
	6.5 Electrical Characteristics	11	Device and Documentation Support	
	6.6 I ² C Timing Requirements		11.1 Device Support	
	6.7 Typical Characteristics		11.2 Community Resources	2 ⁴
7	Detailed Description		11.3 Trademarks	
•	7.1 Overview		11.4 Electrostatic Discharge Caution	
	7.2 Functional Block Diagram		11.5 Glossary	24
	7.3 Feature Description		Mechanical, Packaging, and Orderable Information	24

4 Revision History

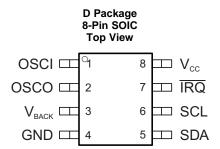
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2011) to Revision E

Page



5 Pin Configuration and Functions



Pin Functions

PIN	PIN		DECODINE		
NAME	NO.	1/0	DESCRIPTION		
POWER AND G	ROUND	•			
GND	4	-	Ground		
V _{BACK}	3	-	Backup device power		
V _{CC}	8	-	Main device power		
SERIAL INTERF	SERIAL INTERFACE				
SCL	6	I	I ² C serial interface clock		
SDA	5	I/O	I ² C serial data		
INTERRUPT		•			
ĪRQ	7	0	Configurable interrupt output. Open-drain output.		
OSCILLATOR	OSCILLATOR				
OSCI	1	-	Oscillator input		
OSCO	2	-	Oscillator output		



6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Innut voltage V	V _{CC} to GND		-0.3	4	V
Input voltage, V _{IN}	All other pins to GND		-0.3	$V_{CC} + 0.3$	V
Operating junction temperature	Operating junction temperature, T _J			150	°C
Storage temperature, T _{stg}			-60	150	°C

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT	
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	2000		
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	500	V	

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, V _{CC} to GND	3		3.6	V
T_A	Operating free-air temperature	-40		85	°C
fo	Crystal resonant frequency		32.768		kHz
R_S	Crystal series resistance			70	kΩ
C _L	Crystal load capacitance	10.8	12	13.2	рF

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

		bq32000	
	THERMAL METRIC ⁽¹⁾	D (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.9	°C/W
ΨЈТ	Junction-to-board characterization parameter	55	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

Product Folder Links: bq32000

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWE	R SUPPLY					
I _{CC}	V _{CC} supply current			100		μΑ
V _{BACK} Backup supply voltage	Operating	1.4		V _{CC}	V	
V_{BACK}	Backup supply voltage	Switchover	2.0		V _{CC}	V
I _{BACK}	Backup supply current	V _{CC} needs a pulse ⁽¹⁾ , V _{BACK} = 3 V, Oscillator on, T _A = 25°C		1.2	1.5	μA
LOGIC	LEVEL INPUTS					
V_{IL}	Input low voltage				0.3 V _{CC}	V
V _{IH}	Input high voltage		0.7 V _{CC}			V
I _{IN}	Input current	$0 \text{ V} \leq \text{V}_{\text{IN}} \leq \text{V}_{\text{CC}}$	-1		1	μA
LOGIC	LEVEL OUTPUTS					
V_{OL}	Output low voltage	$I_{OL} = 3 \text{ mA}$			0.4	V
IL	Leakage current		-1		1	μΑ
REAL-	TIME CLOCK CHARACTER	RISTICS				
	Pre-calibration accuracy	V _{CC} = 3.3 V, V _{BACK} = 3 V, Oscillator on, T _A = 25°C		±35 ⁽²⁾		ppm

6.6 I²C Timing Requirements

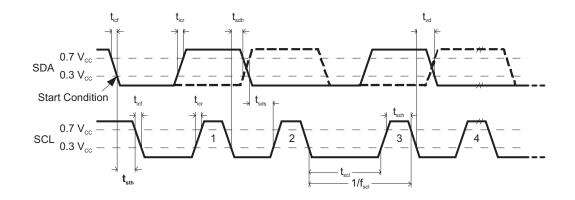
		STANDARD	MODE	FAST MODE		LINUT
		MIN	MAX	MIN	MAX	UNIT
f _{scl}	I ² C clock frequency	0	100	0	400	kHz
t _{sch}	I ² C clock high time	4		0.6		μs
t _{scl}	I ² C clock low time	4.7		1.3		μs
t _{sp}	I ² C spike time	0	50	0	50	ns
t _{sds}	I ² C serial data setup time	250		100		ns
t _{sdh}	I ² C serial data hold time	0		0		ns
t _{icr}	I ² C input rise time		1000	20 + 0.1C _b ⁽¹⁾	300	ns
t _{icf}	I ² C input fall time		300	20 + 0.1C _b ⁽¹⁾	300	ns
t _{ocf}	I ² C output fall time		300	20 + 0.1C _b ⁽¹⁾	300	μs
t _{buf}	I ² C bus free time	4.7		1.3		μs
t _{sts}	I ² C Start setup time	4.7		0.6		μs
t _{sth}	I ² C Start hold time	4		0.6		μs
t _{sps}	I ² C Stop setup time	4		0.6		μs
t _{vd(data)}	Valid data time (SCL low to SDA valid)		1		1	μs
t _{vd(ack)}	Valid data time of ACK (ACK signal from SCL low to SDA low)		1		1	μs

Product Folder Links: bq32000

The currents measured after issuing a pulse on V_{CC}. The pulse amplitude 0-V_{CC}; pulse width min 1 ms.
 Typical accuracy is measured using reference board design and KDS DMX-26S surface-mount 32.768-kHz crystal. Variation in board design and crystal section results in different typical accuracy.

⁽¹⁾ $C_b = total$ capacitance of one bus line in pF





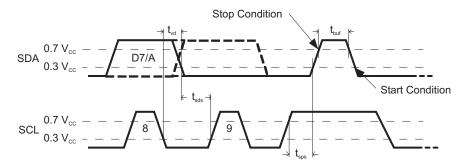
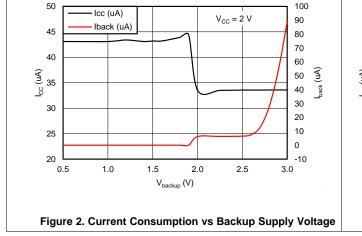


Figure 1. I²C Timing Diagram

6.7 Typical Characteristics



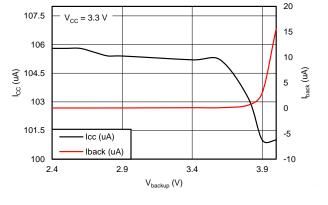


Figure 3. Current Consumption vs Backup Supply Voltage

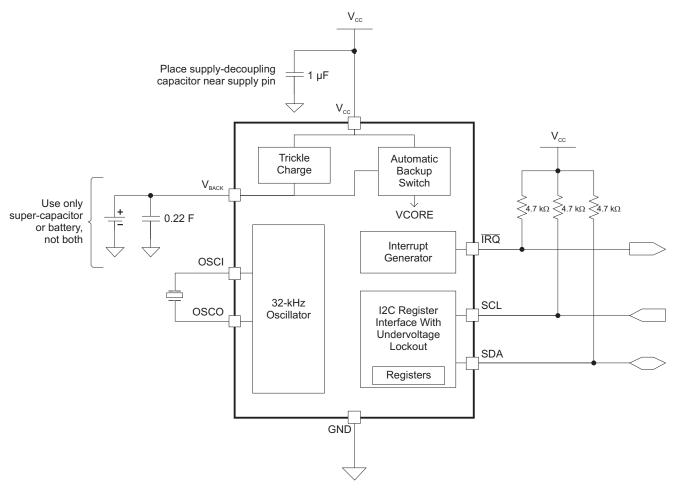


7 Detailed Description

7.1 Overview

The bq32000 is a real-time clock that features an automatic backup supply with an integrated trickle charger.

7.2 Functional Block Diagram



NOTE: All pullup resistors should be connected to V_{CC} such that no pullup is applied during backup supply operation.

7.3 Feature Description

7.3.1 IRQ Function

The \overline{IRQ} pin of the bq32000 functions as a general-purpose output or a frequency test output. The function of \overline{IRQ} is configurable in the device register space by setting the FT, FTF, and OUT bits. On initial power cycles, the OUT bit is set to one, and the FTF and FT bits are set to zero. On subsequent power-ups, with backup supply present, the \overline{OUT} bit remains unchanged, and the FTF and FT bits are set to zero. When operating on backup supply, the \overline{IRQ} pin function is unused. \overline{IRQ} pullup resistor should be tied to V_{CC} to prevent \overline{IRQ} operation when operating on backup supply. The effect of the calibration logic is not normally observable when \overline{IRQ} is configured to output 1 Hz. The calibration logic functions by periodically adjusting the width of the 1-Hz clock. The calibration effect is observable only every eight or sixteen minutes, depending on the sign of the calibration.



Feature Description (continued)

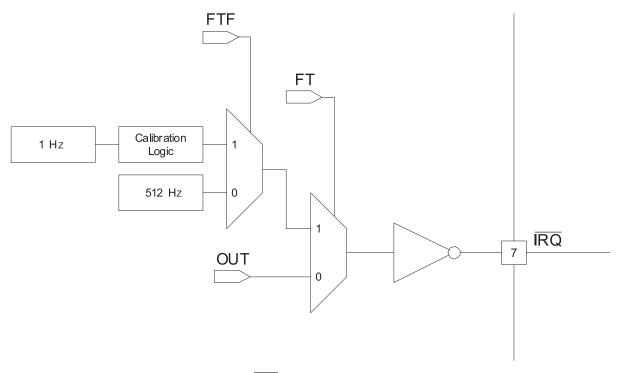


Figure 4. IRQ Pin Functional Diagram

Table 1. IRQ Function

FT	OUT	FTF	IRQ STATE
1	X	1	1 Hz
1	X	0	512 Hz
0	1	X	1
0	0	Х	0



7.3.2 V_{BACK} Switchover

The bq32000 has an internal switchover circuit that causes the device to switch from main power supply to backup power supply when the voltage of the main supply pin V_{CC} drops below a minimum threshold. The V_{BACK} switchover circuit uses an internal reference voltage V_{REF} derived from the on-chip bandgap reference; V_{REF} is approximately 2.8 V. The device switches to the V_{BACK} supply when V_{CC} is less than the lesser of V_{BACK} or V_{REF} . Similarly, the device switches to the V_{CC} supply when V_{CC} is greater than either V_{BACK} or V_{REF} .

Some registers are reset to default values when the RTC switches from main power supply to backup power supply. Please see the register definitions to determine what register bits are effected by a backup switchover (effected bits have their reset value (1/0) shown for 'Cycle', bits that are unchanged by backup are marked 'UC').

The time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

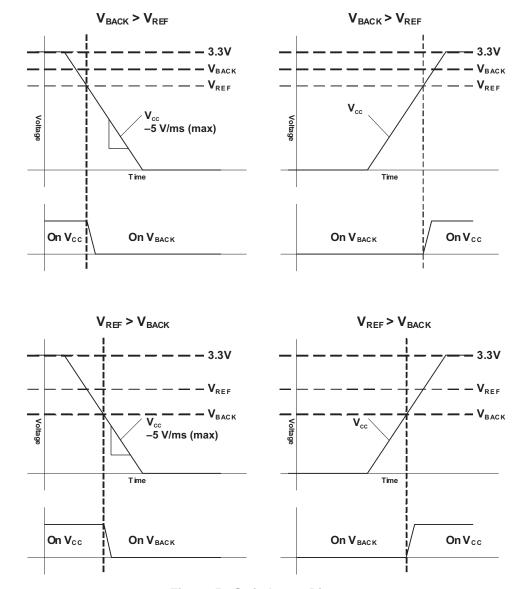


Figure 5. Switchover Diagram

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7.3.3 Trickle Charge

The bq32000 includes a trickle charge circuit to maintain the charge of the backup supply when a super capacitor is used. The trickle charge circuit is implemented as a series of three switches that are independently controlled by setting the TCHE[3:0], TCH2, and TCFE bits in the register space.

TCHE[3:0] must be written as 0x5h and TCH2 as 1 to close the trickle charge switches and enable charging of the backup supply from V_{CC} . Additionally, TCFE can be set to 1 to bypass the internal diode and boost the charge voltage of the backup supply. All trickle charge switches are opened when the device is initially powered on and each time the device switches from the main supply to the backup supply. The trickle charge circuit is intended for use with super capacitors; however, it can be used with a rechargeable battery under certain conditions. Care must be taken not to overcharge a rechargeable battery when enabling trickle charge. Follow all charging guidelines specific to the rechargeable battery or super capacitor when enabling trickle charge.

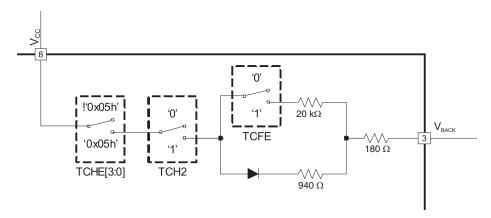


Figure 6. Trickle Charge Switch Functional Diagram

7.4 Device Functional Modes

When the device switches from the main power supply to backup supply, the Time keeping register Registers [0-9] cannot be accessed via the I2C. The access to these registers are only when $V_{CC} > V_{ref}$.

The Time keeping registers can take up to 1 second to update after the device switches from backup power supply to main power supply.

7.5 Programming

7.5.1 I²C Serial Interface

The I²C interface allows control and monitoring of the RTC by a microcontroller. I²C is a two-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000).

The bus consists of a data line (SDA) and a clock line (SCL) with off-chip pullup resistors. When the bus is idle, both SDA and SCL lines are pulled high.

A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer.

A slave device receives and/or transmits data on the bus under control of the master device. This device operates only as a slave device.

 I^2C communication is initiated by a master sending a start condition, a high-to-low transition on the SDA I/O while SCL is held high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/W). After receiving a valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. This device responds to the I^2C slave address 11010000b for write commands and slave address 11010001b for read commands.

This device does not respond to the general call address.



Programming (continued)

A data byte follows the address acknowledge. If the R/\overline{W} bit is low, the data is written from the master. If the R/\overline{W} bit is high, the data from this device are the values read from the register previously selected by a write to the subaddress register. The data byte is followed by an acknowledge sent from this device. Data is output only if complete bytes are received and acknowledged.

A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the master to terminate the transfer. A master device must wait at least 60 µs after the RTC exits backup mode to generate a START condition.

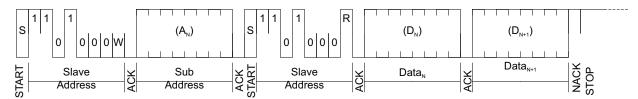


Figure 7. I²C Read Mode

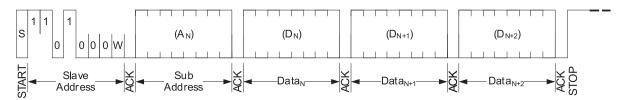


Figure 8. I²C Write Mode

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7.6 Register Maps

Table 2. Normal Registers

REGISTER	ADDRESS (HEX)	REGISTER NAME	DESCRIPTION
0	0x00	SECONDS	Clock seconds and STOP bit
1	0x01	MINUTES	Clock minutes
2	0x02	CENT_HOURS	Clock hours, century, and CENT_EN bit
3	0x03	DAY	Clock day
4	0x04	DATE	Clock date
5	0x05	MONTH	Clock month
6	0x06	YEARS	Clock years
7	0x07	CAL_CFG1	Calibration and configuration
8	0x08	TCH2	Trickle charge enable
9	0x09	CFG2	Configuration 2

Table 3. Special Function Registers

REGISTER	ADDRESS (HEX)	REGISTER NAME	DESCRIPTION
32	0x20	SF KEY 1	Special function key 1
33	0x21	SF KEY 2	Special function key 2
34	0x22	SFR	Special function register

7.6.1 I²C Read After Backup Mode

The time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply. An I^2C read of the RTC that starts before the update has completed will return the time when the RTC enters backup mode. To ensure that the correct time is read after backup mode, the host should wait longer than 1 second after the main supply is greater than 2.8 V and V_{BACK} .

7.6.2 Normal Register Descriptions

7.6.2.1 SECONDS Register (address = 0x00) [reset = 0XXXXXXb]

Description - Clock seconds and STOP bit

Figure 9. SECONDS Register

7	6	5	4	3	2	1	0	BIT(S)	
STOP		10_SECOND			1_SECOND				
r/w	r/w					Read/Write			
0	Х	X X X			Х	X	X	Initial	
UC	UC	UC	UC	UC	UC	UC	UC	Cycle	

STOP

Oscillator stop. The STOP bit is used to force the oscillator to stop oscillating. STOP is set to 0 on initial application of power, on all subsequent power cycles STOP remains unchanged. On initial power application STOP can be written to 1 and then written to 0 to force start the oscillator.

0 Normal

1 Stop

10_SECOND

BCD of tens of seconds. The 10_SECOND bits are the BCD representation of the number of tens of seconds on the clock. Valid values are 0 to 5. If invalid data is written to 10_SECOND, the clock will update with invalid data in 10_SECOND until the counter rolls over; thereafter, the data in 10_SECOND is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

1 SECOND

BCD of seconds. The 1_SECOND bits are the BCD representation of the number of seconds on the clock. Valid values are 0 to 9. If invalid data is written to 1_SECOND, the clock will update with invalid data in 1_SECOND until the counter rolls over; thereafter, the data in 1_SECOND is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

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7.6.2.2 MINUTES Register (address = 0x01) [reset = 1XXXXXXb]

Description - Clock minutes

Figure 10. MINUTES Register

7	6	5	4	3	2	1	0	BIT(S)
OF		10_MINUTE			Name			
r/w	r/w					Read/Write		
1	X X X			Х	X	X	X	Initial
0	UC	UC	UC	UC	UC	UC	UC	Cycle

OF

Oscillator fail flag. The OF bit is a latched flag indicating when the 32.768-kHz oscillator has dropped at least four consecutive pulses. The OF flag is always set on initial power-up, and it can be cleared through the serial interface. When OF is 0, no oscillator failure has been detected. When OF is 1, the oscillator fail detect circuit has detected at least four consecutive dropped pulses.

0 No failure detected

1 Failure detected

10_MINUTE

BCD of tens of minutes. The 10_MINUTE bits are the BCD representation of the number of tens of minutes on the clock. Valid values are 0 to 5. If invalid data is written to 10_MINUTE, the clock will update with invalid data in 10_MINUTE until the counter rolls over; thereafter, the data in 10_MINUTE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

1_MINUTE

BCD of minutes. The 1_MINUTE bits are the BCD representation of the number of minutes on the clock. Valid values are 0 to 9. If invalid data is written to 1_MINUTE, the clock will update with invalid data in 1_MINUTE until the counter rolls over; thereafter, the data in 1_MINUTE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

7.6.2.3 CENT HOURS Register (address = 0x02) [reset = XXXXXXXXXb]

Description - Clock hours, century, and CENT_EN bit

Figure 11. CENT_HOURS Register

7	6	5	4	3	2	1	0	BIT(S)		
CENT_EN	CENT	10_H	IOUR		1_HOUR					
r/w	r/w	r/	w			Read/Write				
X	X	X	Х	X	X	X	X	Initial		
UC	UC	UC	UC	UC	UC	UC	UC	Cycle		

CENT_EN

Century enable. The CENT_EN bit enables the century timekeeping feature. If CENT_EN is set to 1, then the clock tracks the century using the CENT bit. If CENT_EN is set to 0, the clock ignores the CENT bit.

0 Century disabled

1 Century enabled

CENT

Century. The CENT bit tracks the century when century timekeeping is enabled. The clock toggles the CENT bit when the year count rolls from 99 to 00. Because the clock compliments the CENT bit, the user can define the meaning of CENT (1 for current century and 0 for next century, or 0 for current century and 1 for next century).

10_HOUR

BCD of tens of hours (24-hour format). The 10_HOUR bits are the BCD representation of the number of tens of hours on the clock, in 24-hour format. Valid values are 0 to 2. If invalid data is written to 10_HOUR, the clock will update with invalid data in 10_HOUR until the counter rolls over; thereafter, the data in 10_HOUR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

1_HOUR

BCD of hours (24-hour format). The 1_HOUR bits are the BCD representation of the number of hours on the clock, in 24-hour format. Valid values are 0 to 9. If invalid data is written to 1_HOUR, the clock will update with invalid data in 1_HOUR until the counter rolls over; thereafter, the data in 1_HOUR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.



7.6.2.4 DAY Register (address = 0x03) [reset = 00000XXXb]

Description - Clock day

Figure 12. DAY Register

7	6	5	4	3	2	1	0	BIT(S)
		RSVD			Name			
		r/w			Read/Write			
0	0	0	0	X	X	X	Initial	
0	0	0	0	0	UC	UC	UC	Cycle

RSVD DAY Reserved. The RSVD bits should always be written as 0.

BCD of the day of the week. The DAY bits are the BCD representation of the day of the week. Valid values are 1 to 7 and represent the days from Sunday to Saturday. DAY updates if set to 0 until the counter rolls over; thereafter, the data in DAY is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

- 1 Sunday
- 2 Monday
- 3 Tuesday
- 4 Wednesday
- 5 Thursday
- 6 Friday
- 7 Saturday

7.6.2.5 DATE Register (address = 0x04) [reset = 00XXXXXXb]

Description - Clock date

Figure 13. DATE Register

7	6	5	4	3	2	1	0	BIT(S)
RS	SVD	10_0	ATE	1_DATE				Name
r/	r/w r/w					Read/Write		
0	0	X	X	X	X X X			Initial
0	0	UC	UC	UC	UC	UC	UC	Cycle

RSVD

Reserved. The RSVD bits should always be written as 0.

10_DATE

BCD of tens of date. The 10_DATE bits are the BCD representation of the tens of date on the clock. Valid values are 0 to 3⁽¹⁾. If invalid data is written to 10_DATE, the clock will update with invalid data in 10_DATE until the counter rolls over; thereafter, the data in 10_DATE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

1_DATE

BCD of date. The 1_DATE bits are the BCD representation of the date on the clock. Valid values are 0 to $9^{(1)}$. If invalid data is written to 1_DATE, the clock will update with invalid data in 1_DATE until the counter rolls over; thereafter, the data in 1_DATE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

(1) 10_DATE and 1_DATE must form a valid date, 01 to 31, dependent on month and year.



7.6.2.6 MONTH Register (address = 0x05) [reset = 000XXXXXXb]

Description - Clock month

Figure 14. MONTH Register

7	6	5	4	3	2	1	0	BIT(S)
	RSVD		10_MONTH		Name			
	r/w					Read/Write		
0	0	0	X	X	X X X X			Initial
0	0	0	UC	UC	UC	UC	UC	Cycle

RSVD Reserved. The RSVD bits should always be written as 0.

BCD of tens of month. The 10_MONTH bits are the BCD representation of the tens of month on the clock. Valid values 10_MONTH

are 0 to 1 (1). If invalid data is written to 10_MONTH, the clock will update with invalid data in 10_MONTH until the counter rolls over; thereafter, the data in 10 MONTH is valid.

BCD of month. The 1_MONTH bits are the BCD representation of the month on the clock. Valid values are 0 to 9⁽¹⁾. If invalid data is written to 1_MONTH, the clock will update with invalid data in 1_MONTH until the counter rolls over;

thereafter, the data in 1_MONTH is valid.

(1) 10_MONTH and 1_MONTH must form a valid date, 01 to 12.

7.6.2.7 YEARS Register (address = 0x06) [reset = XXXXXXXXXb]

Description - Clock year

Figure 15. YEARS Register

7	6	5	4	3	2	1	0	BIT(S)
	10_Y	ÆAR			Name			
	r/	w			Read/Write			
X	X X X X				Х	Х	Х	Initial
UC	UC	UC	UC	UC	UC	UC	UC	Cycle

10_YEAR

1_MONTH

BCD of tens of years. The 10_YEAR bits are the BCD representation of the tens of years on the clock. Valid values are 0 to 9. If invalid data is written to 10 YEAR, the clock will update with invalid data in 10 YEAR until the counter rolls over; thereafter, the data in 10_YEAR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

1_YEAR

BCD of year. The 1_YEAR bits are the BCD representation of the years on the clock. Valid values are 0 to 9. If invalid data is written to 1 YEAR, the clock will update with invalid data in 1 YEAR until the counter rolls over; thereafter, the data in 1_YEAR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.



7.6.2.8 CAL_CFG1 Register (address = 0x07) [reset = 10000000b]

Description - Calibration and control

Figure 16. CAL_CFG1 Register

7	6	5	4	3	2	1	0	BIT(S)		
OUT	FT	S			CAL			Name		
r/w	r/w	r/w		r/w						
1	0	0	0	0	0	0	0	Initial		
UC	UC	UC	UC	UC	UC	UC	UC	Cycle		

OUT Logic output, when FT = 0. When FT is zero, the logic output of IRQ pin reflects the value of OUT.

0 IRQ is logic 0 1 IRQ is logic 1

FT Frequency test. The FT bit is used to enable the frequency test signal on the $\overline{\text{IRQ}}$ pin. When FT is 1, a square wave is produced on the $\overline{\text{IRQ}}$ pin. The FTF bit in the SFR register determines the frequency of the test signal.

0 Disable1 Enable

S Calibration sign. The S bit determines the polarity of the calibration applied to the oscillator. If S is 0, then the calibration slows the RTC. If S is 1, then the calibration speeds the RTC.

0 Slowing (+) 1 Speeding (-)

CAL Calibration. The CAL bits along with S determine the calibration amount as shown in Table 4.

Table 4. Calibration

CAL (DEC)	S = 0	S = 1
0	+0 ppm	–0 ppm
1	+2 ppm	–4 ppm
N	+N / 491520 (per minute)	–N / 245760 (per minute)
30	+61 ppm	-122 ppm
31	+63 ppm	–126 ppm

7.6.2.9 TCH2 Register (address = 0x08) [reset = 10010000b]

Description - Trickle charge TCH2 control

Figure 17. TCH2 Register

7	6	5	4	3	2	1	0	BIT(S)
RS	VD	TCH2		RSVD				Name
r/	w	r/w		r/w				Read/Write
1	0	0	1	1 0 0 0 0				Initial
UC	0	0	1	UC	UC	UC	UC	Cycle

RSVD Reserved. The RSVD bits should always be written as 0.

Trickle charge switch two. The TCH2 bit determines if the internal trickle charge switch is closed or open. All the trickle charge switches must be closed in order for trickle charging to occur. If TCH2 is 0, then the TCH2 switch is open. If TCH2 is 1, then the TCH2 switch is closed.

0 Open1 Closed

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TCH2



7.6.2.10 CFG2 Register (address = 0x09) [reset = 10101010b]

Description - Configuration 2

Figure 18. CFG2 Register

7	6	5	4	3	2	1	0	BIT(S)		
RSVD	TCFE	RS	RSVD		TCHE					
r/w	r/w	r/	w			Read/Write				
1	0	1	0	1	0	1	0	Initial		
1	0	UC	UC	1	0	1	0	Cycle		

RSVD Reserved. The RSVD bits should always be written as 0.

TCFE Trickle charge FET bypass. The TCFE bit is used to enable the trickle charge FET. When TCFE is 0, the FET is off.

When TCFE is 1, the FET is on.

0 Open

1 Closed

TCHE Trickle charge enable. The TCHE bits determine if the trickle charger is active. If TCHE is 0x5, then the trickle charger is active, otherwise, the trickle charger is inactive.

7.6.3 Special Function Registers

7.6.3.1 SF KEY 1 Register (address = 0x20) [reset = 000000000b]

Description - Special function key 1

Figure 19. SF KEY 1 Register

7	6	5	4	3	2	1	0	BIT(S)		
	SF KEY B1									
r/w										
0	0	0	0	0	0	0	0	Initial		
0	0	0	0	0	0	0	0	Cycle		

SF KEY B1 Special function access key byte 1. Reads as 0x00, and key is 0x5E.

The SF KEY 1 and SF KEY 2 registers are used to enable access to the main special function register (SFR). Access to SFR is granted only after the special function keys are written sequentially to SF KEY 1 and SF KEY 2. Each write to the SFR must be preceded by writing the SF keys to the SF key registers, in order, SF KEY 1 then SF KEY 2.

7.6.3.2 SF KEY 2 Register (address = 0x21) [reset = 00000000b]

Description - Special function key 2

Figure 20. SF KEY 2 Register

7	6	5	4	3	2	1	0	BIT(S)	
SF KEY 2									
r/w									
0	0	0	0	0	0	0	0	Initial	
0	0	0	0	0	0	0	0	Cycle	

SF KEY 2 Special function access key byte 2. Reads as 0x00, and key is 0xC7.

The SF KEY 1 and SF KEY 2 registers are used to enable access to the main special function register (SFR). Access to SFR is granted only after the special function keys are written sequentially to SF KEY 1 and SF KEY 2. Each write to the SFR must be preceded by writing the SF keys to the SF key registers, in order, SF KEY 1 then SF KEY 2.

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Product Folder Links: bq32000



7.6.3.3 SFR Register (address = 0x22) [reset = 00000000b]

Description - Special function register 1

Figure 21. SFR Register

7	6	5	4	3	2	1	0	BIT(S)	
	RSVD								
	r/w								
0	0	0	0	0	0	0	0	Initial	
0	0	0	0	0	0	0	0	Cycle	

RSVD

Reserved. The RSVD bits should always be written as 0.

FTF

Force calibration to 1 Hz. FTF allows the frequency of the calibration output to be changed from 512 Hz to 1 Hz. By default, FTF is cleared, and the RTC outputs a 512-Hz calibration signal. Setting FTF forces the calibration signal to 1 Hz, and the calibration tracks the internal ppm adjustment. Note: The default 512-Hz calibration signal does not include the effect of the ppm adjustment.

- 0 Normal 512-Hz calibration
- 1 1-Hz calibration



8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The typical application for the bq32000 is to provide precise time and date to a system. The backup power supply provides additional reliability by automatically switching over from the main supply when it drops under the voltage threshold.

8.2 Typical Application

The following design is a common application of the bq32000.

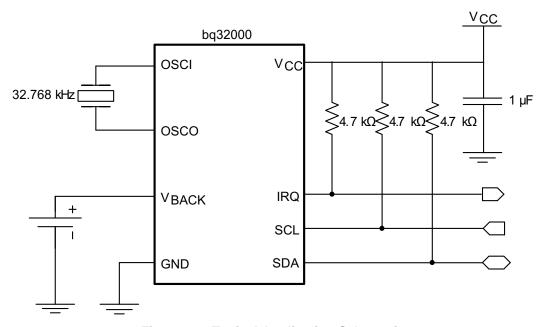


Figure 22. Typical Application Schematic

8.2.1 Design Requirements

The design requirement parameters are listed in the following table.

Table 5. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	V _{CC}	3.3 V
Backup Supply	V _{BACK}	BR1225
Crystal Oscillator	XT	32.768 kHz

Product Folder Links: bq32000



8.2.2 Detailed Design Procedure

8.2.2.1 Reading From a Register

The report details the read-back of the SECONDS register. Figure 23 depicts the first condition that will be used as a benchmark to compare the values taken from the SECONDS register in the bq32000, to the oscilloscope's internal PC time. In this example two modes of operation are demonstrated.

Condition 1. The main power supply, V_{CC} , is greater than the backup power supply, V_{BACK} , and the internal reference voltage, V_{REF} . In this mode, the device's internal registers are fully operational with READ and WRITE access. Analyzing Figure 23, the known register values are compared to the system clock; in this case, the PC clock which is shown at the bottom of the screen capture.

The bq32000 during this condition is reading back [101][0010]= [5][2], which corresponds to 52 seconds at PC time of 2:22:43 PM.

Condition 2. V_{CC} is now lowered to 2 V ($V_{BACK} > V_{CC}$). In this mode, the I2C communications are halted. However, the internal time keeping registers maintain full functional operation and accuracy which will be available to be reliably read by the controller 1 second after the RTC switches from V_{BACK} to V_{CC} supply.

Condition 3. During this final test condition, the RTC is restored to operate from the main power supply and I2C communications are now fully functional.

Figure 24 demonstrates a read-back value from the SECONDS register of [100][0101]= [4][5], or 45 seconds at PC time of 2:23:36 PM. This proves that the bq32000 managed to accurately maintain the time keeping registers functional while the V_{CC} dropped below V_{BACK} .

8.2.2.2 Leap Year Compensation

The BQ32000 classifies a leap year as any year that is evenly divisible by 4. Using this rule allows for reliable leap year compensation until 2100. Years that fall outside this rule will need to be compensated for by the external controller.

8.2.2.3 Utilizing the Backup Supply

In order for the bq32000 to achieve a low backup supply current as specified in the *Electrical Characteristics*, the V_{CC} pin must be initialized after every total power loss situation. Initialization Is achieved by powering on V_{CC} with a voltage between 3 to 3.6 V for at least 1 ms immediately after the backup supply is connected. If the V_{CC} is not powered on while connecting the backup supply, then the expected leakage current from V_{BACK} will be much greater than specified.



8.2.3 Application Curves

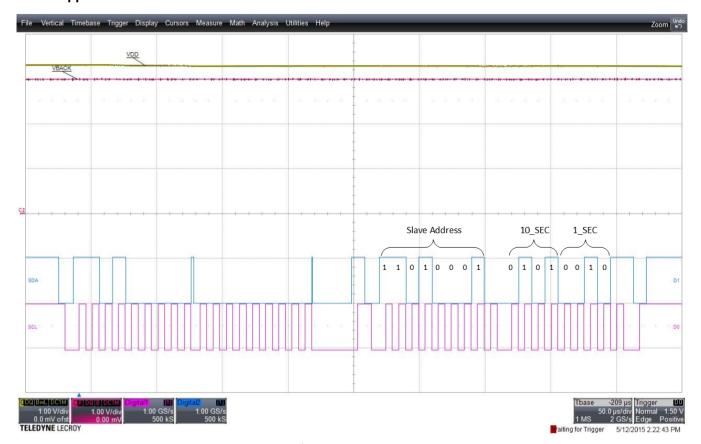


Figure 23. Master and Slave I²C Communication for the SECONDS Register





Figure 24. Master and Slave I²C Communication for the SECONDS Register After Recovering From the Backup Supply

22



9 Power Supply Recommendations

The bq32000 is designed to operate from an input voltage supply, V_{CC} , range between 3.0 and 3.6 V. The user must place a minimum of 1- μ F ceramic bypass capacitor rated for at least the maximum voltage as close as possible to V_{CC} and GND pin.

10 Layout

10.1 Layout Guidelines

The V_{CC} pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a minimum recommended value of 1- μ F. This capacitor should be placed as close to the V_{CC} and GND pins as possible with thick trace or ground plane connection to the device GND pin.

Locate the 32.768-kHz crystal oscillator as close as possible to the OSCI and OSCO pins. This will minimize stray capacitance.

10.2 Layout Example

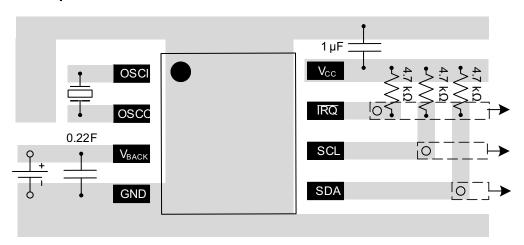


Figure 25. Recommended PCB Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.3 Trademarks

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All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: bg32000

www.ti.com 10-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
BQ32000D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	32000
BQ32000D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	32000
BQ32000DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	32000
BQ32000DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	32000
BQ32000DRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	32000
BQ32000DRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	32000

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

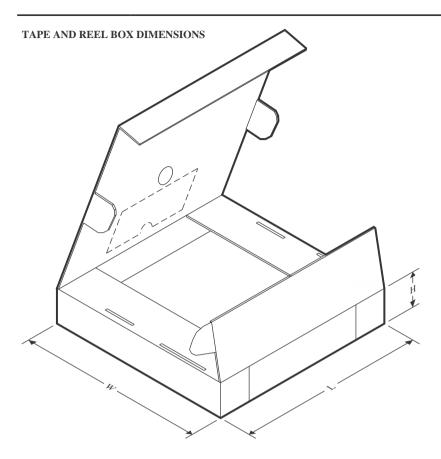
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ32000DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
BQ32000DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ32000DR	SOIC	D	8	2500	353.0	353.0	32.0
BQ32000DRG4	SOIC	D	8	2500	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ32000D	D	SOIC	8	75	506.6	8	3940	4.32
BQ32000D.A	D	SOIC	8	75	506.6	8	3940	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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