

BQ27Z758 Impedance Track™ Technology Battery Gas Gauge and Protection Solution for 1-Series Cell Li-Ion Battery Packs

1 Features

- Integrated battery gas gauge and protector
- Flash-programmable custom BQBMP RISC CPU
 - SHA-256 authentication
 - 400kHz I²C bus communications interface
- Low-voltage (2.0V) operation
- Zero volt charging with no inhibit (ZVCHG) for systems with secondary protectors
- Two independent precision 16-bit ADCs
 - Coulomb counting ADC with current sense resistor down to 1mΩ
 - Voltage ADC for cell voltage and external and internal temperature sensors
- Battery fuel gauging based on patented Impedance Track™ technology
 - Models battery discharge curve for accurate time-to-empty predictions
 - Automatically adjusts for aging, temperature, and rate-induced effects on the battery
- Battery Kelvin sense differential analog output pins with built-in protection
- High-side or low-side current sensing
- Programmable hardware-based protection
 - High-side FET gate drivers
 - Overvoltage and undervoltage (OVP and UVP)
 - Overcurrent in discharge and overcurrent in charge (OCD and OCC)
 - Short circuit in discharge (SCD)
 - Firmware-based overtemperature (OT)
- Reduced typical power modes
 - SLEEP mode: 20μA
 - SHIP mode: 10μA
 - SHELF mode: 5μA
 - SHUTDOWN mode: 0.2μA
- Ultra-compact, 15-ball NanoFree™ DSBGA

2 Applications

- Any end equipment with 1-series rechargeable batteries:
 - [Smartphones](#)
 - [Tablets](#)
 - [Cameras](#)
 - [Portable wearables/medical](#)
 - [Industrial handhelds](#)

3 Description

The Texas Instruments BQ27Z758 Impedance Track™ gas gauge solution is a highly integrated, accurate 1-series cell gas gauge and protection solution.

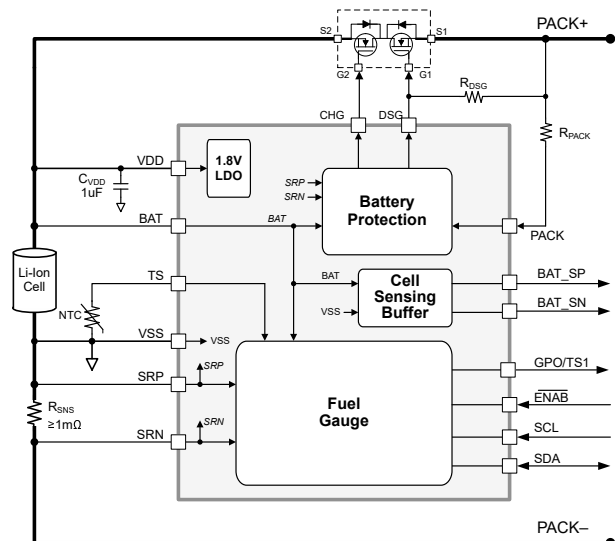
The BQ27Z758 device provides a fully integrated, pack-based solution with a flash programmable custom reduced instruction-set CPU (RISC), safety protection, differential battery sensing analog output, and authentication for 1-series cell Li-ion and Li-polymer battery packs.

The BQ27Z758 gas gauge communicates through an I²C compatible interface and combines an ultra-low power TI BQBMP processor, high accuracy analog measurement capabilities, integrated flash memory, N-CH high-side FET drive, and a SHA-2 Authentication transform responder into a complete, high-performance battery management solution.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
BQ27Z758	DSBGA (YAH, 15)	1.71mm × 2.59mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



BQ27Z758 Simplified Schematic



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4 Pin Configurations and Functions

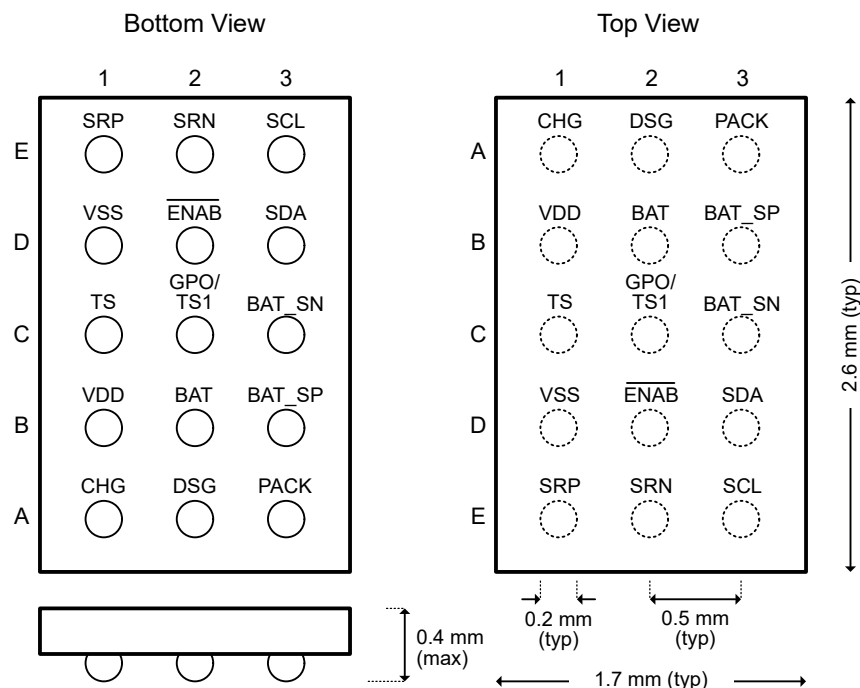


Figure 4-1. Pinout Diagram

Table 4-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE ⁽¹⁾	
CHG	A1	AO	Charge FET (CHG) driver
DSG	A2	AO	Discharge FET (DSG) driver. Connect a series 10MΩ typical resistor (R_{DSG}) between DSG pin and PACK+ positive terminal.
PACK	A3	AI	Pack input voltage sensing pin. Connect a series 5kΩ typical resistor (R_{PACK}) between PACK pin and PACK+ positive terminal.
VDD	B1	P	LDO regulator input. Connect a 1μF typical capacitor (C_{VDD}) between VDD and VSS. Place the capacitor close to the gauge.
BAT	B2	AI	Battery voltage measurement sense input
BAT_SP	B3	AO	Cell sense output, positive
BAT_SN	C3	AO	Cell sense output, negative
TS	C1	AI	Thermistor input to ADC with internal 18kΩ pullup resistor
GPO/TS1	C2	I/O	General purpose output. Optional TS1 ADC input channel with internal 18kΩ pullup resistor
VSS	D1	P	Device ground
ENAB	D2	I	Active low digital input with weak internal pullup to VDD. If enabled for ultra-low power SHELFB mode, driving this signal low will enable the device to wake up.
SDA	D3	I/O	Digital input, open drain output for I ² C serial data. Use with a typical 10kΩ pullup resistor.
SCL	E3	I/O	Digital input, open drain output for I ² C serial clock. Use with a typical 10kΩ pullup resistor.
SRP	E1	AI	This is the positive analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP (positive side) and SRN (negative side).
SRN	E2	AI	This is the negative analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP (positive side) and SRN (negative side).

(1) I/O = Digital input/output, AI = Analog input, AO = Analog output, P = Power connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range	VDD	−0.3	6	V
Input voltage range	PACK (limited to 4mA max)	−0.3	8	V
	PACK+ external battery pack input terminal with 5kΩ resistor in series to device PACK input pin	−0.3	24	
	PACK+ external battery pack input terminal with a 5kΩ resistor (R _{PACK}) in series to device PACK pin and a 10MΩ resistor (R _{DSG}) to device DSG pin	−12	24	
	BAT	−0.3	6	
	SDA, SCL, $\overline{\text{ENAB}}$	−0.3	6	
	TS	−0.3	2	
	SRP, SRN	−0.3	V _{BAT} + 0.3	
Output voltage range	BAT_SP, BAT_SN	−0.3	6	V
	CHG, DSG	−0.3	12	
Operating junction temperature, T _J		−40	85	°C
Storage temperature, T _{stg}		−65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM) on all pins, per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM) on all pins, per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage range	VDD	2.0		5.5	V
Input voltage range	PACK (with 5kΩ R _{PACK} current limit)	0		12	V
	PACK (no R _{PACK} current limit)	0		5.5	
	BAT	1.5		5.5	
	SDA, SCL, $\overline{\text{ENAB}}$	−0.3		VDD	
	TS	VSS		1.8	
	SRN, SRP	V _{CC_CM} − 0.1		V _{CC_CM} + 0.1	
Output voltage range	BAT_SP, BAT_SN	2		VDD + V _{OFFS}	V
	GPO	VSS		1.8	
	CHG, DSG	VSS		VDD+ (VDD × A _{FETON})	
C _{VDD}	External Decoupling Capacitor on VDD pin	1			μF

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
C _{TS}	External Decoupling Capacitor on TS pin			0.01	μF
R _{PACK}	External Sense Resistor from PACK+ terminal to device PACK pin	5			kΩ
R _{DSG}	External Sense Resistor from PACK+ terminal to device DSG pin	10			MΩ
R _{SNS}	External Sense Resistor from SRN to SRP pins	1		20	mΩ
T _A	Operating Temperature	-40		85	°C

5.4 Thermal Information

Over-operating free-air temperature range (unless otherwise noted)

THERMAL METRIC ⁽¹⁾		YAH (DSBGA) (15 PINS)	UNIT
R _{θJA}	Junction-to-ambient thermal resistance	70	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	17	
R _{θJB}	Junction-to-board thermal resistance	20	
ψ _{JT}	Junction-to-top characterization parameter	1	
ψ _{JB}	Junction-to-board characterization parameter	18	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	NA	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

5.5 Electrical Characteristics

5.5.1 Supply Current

Unless otherwise noted, characteristics noted under conditions of T_A = -40 to 85°C, no host communications, PROT On⁽¹⁾, V_{CHG} and V_{DSG} > 5V, C_{LOAD} = 8nF (typical 20nA), VDD = 4V, Average current over 30s with default firmware settings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{NORMAL}	Standard operating conditions		86		μA
I _{SLEEP}	Measured current ≤ sleep current threshold		20		μA
I _{SHIP}	V _{BAT} = 3.0V, Firmware SHIP mode enabled, 60s average		10		μA
I _{SHELF}	V _{BAT} = 3.0V, Firmware SHELF mode enabled. PROT Off, 60s average		5		μA
I _{SHUT}	Firmware SHUTDOWN mode enabled OR V _{BAT} ≤ V _{SHUT} , PROT Off		0.2	1	μA

(1) PROT On/Off. Protector block enabled with both DSG and CHG pins On or Off.

5.5.2 Common Analog (LDO, LFO, HFO, REF1, REF2, I-WAKE)

Unless otherwise noted, characteristics noted under conditions of T_A = -40 to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL 1.8V LDO (REG18)					
V _{REG18}	Regulator output voltage	1.6	1.8	2.0	V
ΔV _{REG18TEMP}	Regulator output change with temperature	ΔV _{BAT} /ΔT _A , I _{REG18} = 10mA		-1.2%	+1.2%
ΔV _{REG18LINE}	Line regulation			-0.8%	0.8%

5.5.2 Common Analog (LDO, LFO, HFO, REF1, REF2, I-WAKE) (continued)

Unless otherwise noted, characteristics noted under conditions of $T_A = -40$ to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{\text{REG18LOAD}}$	Load regulation	$I_{\text{REG18}} = 16\text{mA}$	−1.5%		1.5%	
I_{SHORT}	Short Circuit Current Limit	$V_{\text{REG18}} = 0\text{V}$	18		60	mA
$\text{PSRR}_{\text{REG18}}$	Power Supply Rejection Ratio	$\Delta V_{\text{BAT}}/\Delta V_{\text{REG18}}$, $I_{\text{REG18}} = 10\text{mA}$, $V_{\text{BAT}} > 2.5\text{V}$, $f = 10\text{Hz}$		50		dB
V_{PORth}	POR threshold	Rising Threshold	1.55	1.65	1.75	V
V_{PORhy}	POR hysteresis			0.1		V
V_{ENAB}	$\overline{\text{ENAB}}$ turn-on voltage for LDO ⁽¹⁾	Active low falling threshold			0.4	V
R_{ENAB}	$\overline{\text{ENAB}}$ pin pullup resistance ⁽¹⁾	Internal pull-up to VDD	0.7	1	1.3	MΩ
V_{STARTUP}	Minimum PACK pin turn-on voltage for LDO ⁽¹⁾			2		V
LOW FREQUENCY INTERNAL OSCILLATOR (LFO)						
f_{LFO}	LFO Operating frequency	Normal operating mode	65.536			kHz
$f_{\text{LFO(ERR)}}$	LFO Frequency error		−2.5%	+2.5%		
f_{LFO32}	LFO operating frequency	Low power mode	32.768			kHz
$f_{\text{LFO32(ERR)}}$	LFO frequency error		−5%	+5%		
HIGH FREQUENCY INTERNAL OSCILLATOR (HFO)						
f_{HFO}	HFO operating frequency		16.78			MHz
$f_{\text{HFO(ERR)}}$	HFO frequency error	$T_{\text{A}} = -20^{\circ}\text{C}$ to 70°C	−2.5%	2.5%		
		$T_{\text{A}} = -40^{\circ}\text{C}$ to 85°C	−3.5%	3.5%		
t_{HFSTART}	HFO start-up time	$T_{\text{A}} = -40^{\circ}\text{C}$ to 85°C , $\text{CLKCTL}[\text{HFRAMP}] = 1$, oscillator frequency within +/- 3% of nominal frequency or a power-on reset		4		ms
VOLTAGE REFERENCE1 (VREF1)						
V_{REF1}	Internal reference voltage	REF1 is for protection circuits, LDO, and CC	1.195	1.21	1.227	V
$V_{\text{REF1_DRIFT}}$	Internal Reference Voltage Drift		−80	+80		PPM/°C
VOLTAGE REFERENCE2 (VREF2)						
V_{REF2}	Internal Reference Voltage	REF2 is for the ADC	1.2	1.21	1.22	V
$V_{\text{REF2_DRIFT}}$	Internal Reference Voltage Drift		−20	+20		PPM/°C
WAKE-UP COMPARATOR (I-WAKE)						
V_{WAKE}	Sense resistor voltage threshold range to wake-up gauge from low-power states ⁽²⁾	500μV step. Data Flash firmware default is 2mV typical	−1.5	−2.0	−2.5	mV
I_{WAKE}	Effective wake-up current threshold range	Ideal $R_{\text{SNS}} = 1\text{m}\Omega$	−1000	−3000		mA
		Ideal $R_{\text{SNS}} = 2\text{m}\Omega$	−500	−1500		
		Ideal $R_{\text{SNS}} = 5\text{m}\Omega$	−200	−600		
$V_{\text{WAKE_ACC}}$	Wake-up detection accuracy ⁽²⁾		−250	250		μV
t_{WAKE}	I-WAKE detection delay options ⁽¹⁾	Configurable with two delay options. Data Flash firmware default is 12ms typical	9.6	12	14.4	ms
			19.2	24	28.8	

(1) Specified by design

(2) Data flash is configurable in FULL ACCESS mode and locked in SEALED. Accuracy is certified by factory trim at specified default threshold. A change in the factory threshold requires device calibration in the field.

5.5.3 Battery Protection (CHG, DSG)

Protection hardware circuits operating over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
N-CH FET DRIVER, CHG AND DSG							
V _{DRIVER}	Gate Driver Voltage, V _{CHG} or V _{DSG}	C _{LOAD} = 8nF	2 × VDD			V	
A _{FETON}	FET driver gain factor, V _{gs} voltage to FET	A _{FETON} = (V _{driver} – VDD)/VDD, C _{LOAD} = 8nF, UVP < VDD < 3.8V	0.9	1.0	1.2	V/V	
V _{DSGOFF}	DSG FET driver off output voltage	V _{DSGOFF} = V _{DSG} – PACK, C _L = 8nF	0.2			V	
V _{CHGOFF}	CHG FET driver off output voltage	V _{CHGOFF} = V _{CHG} – VSS, C _L = 8nF	0.2			V	
t _{rise}	FET driver rise time ⁽¹⁾	C _L = 8nF, (V _{driver} – VDD)/VDD = 1× V _{FETON} changes from VDD to 2×VDD	400			800	us
t _{fall}	FET driver fall time ⁽¹⁾	CL = 8nF, V _{FETON} changes from V _{FETMAX} to V _{FETOFF}	50			200	us
V _{FET_SHUT}	Firmware FET driver shut down voltage ^{(2) (4)}	Configurable with 1mV steps	2000	2100	5000	mV	
V _{FET_SHUT_REL}	Firmware FET driver shut down release ^{(2) (4)}		2000	2300	5000	mV	
I _{LOAD}	FET driver maximum loading				10	uA	
VOLTAGE PROTECTION							
V _{OVP}	Hardware overvoltage protection (OVP) detection range ⁽³⁾	Recommended threshold range.	3500		5000	mV	
	Factory default trimmed threshold ⁽³⁾	Factory trimmed in 50mV steps	4525				
V _{OVP_ACC}	Hardware OVP detection accuracy ⁽³⁾	TA = 25°C, C _{LOAD} at CHG/DSG < 1μA	–15		15	mV	
		TA = 0°C to 60°C, C _{LOAD} at CHG/DSG < 1μA	–25		25	mV	
		TA = –40°C to 85°C, C _{LOAD} at CHG/DSG < 1μA	–50		50	mV	
V _{FW_OVP}	Firmware OVP detection range ⁽⁴⁾	Configurable with 1mV steps	2000	4490	5000	mV	
V _{FW_OVP_REL}	Firmware OVP release range ⁽⁴⁾		2000	4290	5000	mV	
V _{UVP}	Hardware undervoltage (UVP) detection range ⁽³⁾	Recommended threshold range.	2000		4000	mV	
	Factory default trimmed threshold ⁽³⁾	Factory trimmed in 50mV steps	2300				
V _{UVP_ACC}	Hardware UVP detection accuracy ⁽³⁾	TA = 25°C, C _{LOAD} at CHG/DSG < 1μA	–20		20	mV	
		TA = 0°C to 60°C, C _{LOAD} at CHG/DSG < 1uA	–30		30	mV	
		TA = –40°C to 85°C, C _{LOAD} at CHG/DSG < 1uA	–50		50	mV	
V _{FW_UVP}	Firmware UVP detection range ⁽⁴⁾	Configurable with 1mV steps	2000	2500	5000		
V _{FW_UVP_REL}	Firmware UVP release range ⁽⁴⁾		2000	2900	5000	mV	
R _{PACK-VSS}	Resistance between PACK and VSS	SHUTDOWN mode only	100	300	550	kΩ	
V _{RCP}	Reverse Charge Protection limit	–10V Continuous Operating, –12V ABS MAX	–10			V	
CURRENT PROTECTION							
V _{OCC}	Sense voltage threshold range for overcurrent in charge (OCC) ^{(3) (4)}	Recommended threshold range.	4		100	mV	
	Factory default trimmed threshold ⁽³⁾	Factory trimmed in 1mV steps	14				
V _{OCC}	OCC 2mV step design option	2mV step configuration option	2		256	mV	
I _{OCC}	Effective OCC current threshold range from V _{OCC} ^{(1) (4)}	Ideal R _{SNS} = 1mΩ	4		14	100	A
		Ideal R _{SNS} = 2mΩ	2		7	50	
		Ideal R _{SNS} = 5mΩ	0.8		2.8	20	

5.5.3 Battery Protection (CHG, DSG) (continued)

Protection hardware circuits operating over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{FW_OCC}	Firmware OCC detection range ⁽⁴⁾	Configurable with 1mA steps	0	12000	+I _{CC_IN}	mA
V _{OCD}	Sense voltage threshold range for overcurrent in discharge (OCD) ^{(3) (4)}	Recommended threshold range.	−4		−100	mV
	Factory default trimmed threshold ⁽³⁾	Factory trimmed in 1mV steps		−16		
V _{OCD}	OCD 2mV step design option	±2mV step configuration option	−2		−256	mV
I _{OCD}	Effective OCD current threshold range from V _{OCD} ^{(1) (4)}	Ideal R _{SNS} = 1mΩ	−4	−16	−100	A
		Ideal R _{SNS} = 2mΩ	−2	−8	−50	
		Ideal R _{SNS} = 5mΩ	−0.8	−3.2	−20	
I _{FW_OCD}	Firmware OCD detection range ⁽⁴⁾	Configurable with 1mA steps	−I _{CC_IN}	−7000	0	mA
V _{SCD}	Sense voltage threshold range for short circuit current in discharge (SCD) ^{(3) (4)}	Threshold factory trimmed with 1mV steps	−5		−120	mV
	Factory default trimmed threshold ⁽³⁾			−20		
I _{SCD}	Effective SCD current threshold range from V _{SCD} ^{(1) (4)}	Ideal R _{SNS} = 1mΩ	−5	−20	−120	A
		Ideal R _{SNS} = 2mΩ	−2.5	−10	−60	
		Ideal R _{SNS} = 5mΩ	−1	−4	−24	
V _{OC_ACC}	Overcurrent (OCC, OCD, SCD) detection accuracy ⁽³⁾	<20mV, TA = −25°C to 60°C	−2.1		2.1	mV
		<20mV	−2.1		2.1	
		20mV–55mV	−3		3	
		56mV–100mV	−5		5	
		>100mV	−12		12	
I _{PACK-VDD}	Current sink between PACK and VDD during current fault	Load removal detection in firmware		15		μA
V _{OC_REL}	OCC fault release threshold	(V _{PACK} − V _{BAT})		100		mV
	OCD, SCD fault release threshold			−400		mV
OVERTEMPERATURE PROTECTION						
T _{OTC_TRIP}	OTC trip/release threshold ^{(2) (4)}	Firmware-based and configurable in 0.1°C steps	−40.0	55.0	150.0	°C
T _{OTC_REL}			−40.0	50.0	150.0	°C
T _{OTD_TRIP}	−40.0		60.0	150.0	°C	
T _{OTD_REL}	−40.0		55.0	150.0	°C	
T _{UTC_TRIP}	−40.0		0.0	150.0	°C	
T _{UTC_REL}	−40.0		5.0	150.0	°C	
T _{UTD_TRIP}	−40.0		0.0	150.0	°C	
T _{UTD_REL}	−40.0		5.0	150.0	°C	
PROTECTION DELAY ⁽¹⁾						
t _{OVP}	OVP detection delay (debounce) options ^{(1) (4)}	Configurable with 4095 delay options in 1.953ms steps. Factory default = 1000ms (512 counts) typical	1.953	1000	7998	ms
t _{UVP}	UVP detection delay (debounce) options ^{(1) (4)}	Configurable with 127-delay options in 1.953ms steps. Factory default = 127ms (65 counts) typical	1.953	127	248	ms
t _{OCC}	OCC detection delay (debounce) options ^{(1) (4)}	Configurable with 31 delay options in 1.953ms steps. Factory default = 7.8ms (4 counts) typical	1.953	7.8	60.5	ms
t _{OCD}	OCD detection delay (debounce) options ^{(1) (4)}	Configurable with 255 delay options in 0.244ms steps. Factory default = 15.9ms (65 counts) typical	0.244	15.9	62.3	ms

5.5.3 Battery Protection (CHG, DSG) (continued)

Protection hardware circuits operating over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{SCD}	SCD detection delay (debounce) options ^{(1) (4)}	Configurable with seven delay options in 122μs steps. Factory default = 244μs (2 counts) typical	122	244	854	μs
T _{OTC_DLY}	OTC trip delay ^{(2) (4)}	Firmware-based and configurable in 1s steps. The typical value is the data flash factory default.	0	2	255	s
T _{OTD_DLY}	OTD trip delay ^{(2) (4)}		0	2	255	s
T _{UTC_DLY}	UTC trip delay ^{(2) (4)}		0	2	255	s
T _{UTD_DLY}	UTD trip delay ^{(2) (4)}		0	2	255	s
ZERO VOLT (LOW VOLTAGE) CHARGING						
V _{0CHGR}	Charger voltage required to start zero-volt charging	V _{0CHGR} = V _{PACK} – V _{SS}	1.6			V

- (1) Specified by design. Not production tested.
(2) Firmware-based parameter. Not production tested.
(3) Accuracy assured by factory trim at specified default threshold. A change from the default threshold requires device calibration in the field. Refer to the [BQ27Z746R1 and BQ27Z758 Technical Reference Manual](#).
(4) Specified typical value is the factory default. Not production tested. The data flash configuration value can be changed in FULL ACCESS mode and is locked in SEALED mode. Refer to the [BQ27Z746R1 and BQ27Z758 Technical Reference Manual](#).

5.5.4 Cell Sensing Output (BAT_SP, BAT_SN)

Unless otherwise noted, characteristics noted under conditions of $T_A = -40$ to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC RESPONSE						
V_{BUFACC}	Buffer accuracy (BAT_SP – BAT_SN)	V_{BAT} at 1500mV and 2400mV DC, $V_{PACK} - BAT_SP \geq 200\text{mV}$, BAT_SP load: Hi-Z to 1k Ω , BAT_SN load: 1k Ω to 10k Ω	1450	1500	1550	mV
			2350	2400	2450	
$V_{BUFOFFS}$	BAT_SN common mode shift (BAT_SN – VSS)	400mV option, $V_{BAT} = 1.5\text{V}$ to 2.5V	370	400	430	mV
		200mV option, $V_{BAT} = 2.0\text{V}$ to 2.5V	170	200	230	
		0mV option, $V_{BAT} = 2.0\text{V}$ to 2.5V	–30	0	30	
		600mV option, $V_{BAT} = 2.0$ to 2.5V	550	600	650	
ΔV_{BUF_LINE}	Buffer line regulation	$V_{BAT} = 1.5$ to 2.5V , no load, BAT_SP – BAT_SN, $V_{PACK} - V_{BAT} = 1.0\text{V}$		10		mV
ΔV_{BUF_LOAD}	Buffer load regulation	$V_{BAT} = 2.4\text{V}$, load = 1mA, BAT_SP – BAT_SN, $V_{PACK} - V_{BAT} = 1.0\text{V}$		1.2		mV
V_{RLOACC}	RLO mode accuracy (BAT_SP – BAT_SN)	$V_{BAT} = 3000\text{mV}$ to 5000mV DC, For stability, 0mV buffer option enabled, BAT_SP load: Hi-Z to 1k Ω , BAT_SN load: 1k Ω to 10k Ω	–7		+7	mV
$V_{RLOACCP}$	RLO mode accuracy (BAT_SP – VSS)		–5		+5	
$V_{RLOACCN}$	RLO mode accuracy (BAT_SN – VSS)		–5		+5	
R_{LO_SP}	BAT_SP low resistance mode	200 Ω option, DSG FET = ON	160	200	260	Ω
		510 Ω option, DSG FET = ON	459	510	561	
R_{LO_SN}	BAT_SN low resistance mode	200 Ω option, DSG FET = ON	160	200	260	Ω
		510 Ω option, DSG FET = ON	459	510	561	
R_{HIZ_SP}	BAT_SP high impedance mode	CHG FET = OFF	0.6	1.0	1.3	M Ω
R_{HIZ_SN}	BAT_SN high impedance mode		0.6	1.0	1.3	
t_{BUF_OFF}	Buffer turn-off timing ⁽¹⁾	Buffer disable timing respect to DSG FET turn-on		500		μ s

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5.5.4 Cell Sensing Output (BAT_SP, BAT_SN) (continued)

Unless otherwise noted, characteristics noted under conditions of $T_A = -40$ to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{BUF_SP}	Max external capacitance for stable operation ⁽¹⁾	BAT_SP to SRN (PACK-)			150	pF
C_{BUF_SN}		BAT_SN to SRN (PACK-)			150	
B_{BUF_BW}	Buffer unity gain bandwidth ⁽¹⁾	Buffer enabled		30		kHz
V_{BCP}	BAT_SP – BAT +Fault (BCP) Threshold Range ⁽¹⁾	Recommended threshold range.	+100		+250	mV
	Factory default trimmed threshold ⁽³⁾	Factory trimmed in $\approx 2\text{mV}$ steps		+200		
V_{BCP_ACC}	BAT_SP – BAT +Fault Accuracy ⁽³⁾	RLO mode enabled, Step size 10mV	-10		+10	
V_{BDP}	BAT_SP – BAT –Fault (BDP) Threshold Range ⁽¹⁾	Recommended threshold range.	-250		-100	mV
	Factory default trimmed threshold ⁽³⁾	Factory trimmed in $\approx 2\text{mV}$ steps		-200		
V_{BDP_ACC}	BAT_SP – BAT –Fault Accuracy ⁽³⁾	RLO mode enabled, Step size 10mV	-10		+10	
V_{BCN}	BAT_SN – VSS +Fault (BCN) Threshold Range ⁽¹⁾	Recommended threshold range.	+100		+250	mV
	Factory default trimmed threshold ⁽³⁾	Factory trimmed in $\approx 2\text{mV}$ steps		+200		
V_{BCN_ACC}	BAT_SN – VSS +Fault Accuracy ⁽³⁾	RLO mode enabled, Step size 10mV	-10		+10	
V_{BDN}	BAT_SN – VSS –Fault (BDN) Threshold Range ⁽¹⁾	Recommended threshold range.	-250		-100	mV
	Factory default trimmed threshold ⁽³⁾	Factory trimmed in $\approx 2\text{mV}$ steps		-200		
V_{BDN_ACC}	BAT_SN – VSS –Fault Accuracy ⁽³⁾	RLO mode enabled, Step size 10mV	-10		+10	
$t_{LO_FAULT_DLY}$	BAT_SP / BAT_SN fault comparator delay ⁽¹⁾	8ms delay		8		ms
		100ms delay		100		ms
$t_{LO_FAULT_STRT}$	BAT_SP / BAT_SN fault restart time ^{(1) (2)}			1000		ms
TRANSIENT RESPONSE						
V_{LOAD_SP}	BAT_SP load transient ⁽¹⁾	No load $\geq 1\text{K}\Omega \geq$ No load, Transition time 1 μs	-300		300	mV
V_{LOAD_SN}	BAT_SN load transient ⁽¹⁾		-200		200	mV
V_{LINE_SN}	BAT_SN line transient ⁽¹⁾	$V_{BAT} = 1.5\text{V} \geq 2.4\text{V} \geq 1.5\text{V}$, Transition slope 500mV / 10 μs	-30		30	mV
V_{TRANS}	(BAT_SP – BAT_SN) transition transient ⁽¹⁾	Firmware commanded transition from BUF mode to RLO mode	-700		50	mV

(1) Specified by Design. Not production tested.

(2) Firmware-based parameter. Not production tested.

(3) Accuracy assured by factory trim at specified default threshold. A change from the default threshold requires device calibration in the field. Refer to the [BQ27Z746R1 and BQ27Z758 Technical Reference Manual](#).

5.5.5 Gauge Measurements (ADC, CC, Temperature)

Unless otherwise noted, characteristics noted under conditions of $T_A = -40$ to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG DIGITAL CONVERTER (ADC)					

5.5.5 Gauge Measurements (ADC, CC, Temperature) (continued)

Unless otherwise noted, characteristics noted under conditions of $T_A = -40$ to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{BAT_RES}	Battery Voltage ADC Resolution (bits)	Signed data format, ±15 bits		16		bits
V _{BAT_FS}	Battery Measurement Full Scale Range		−0.2		5.5	V
V _{BAT_ERR}	Battery Voltage ADC Error	T _A = +25°C, V _{BAT} = 4.0VDC		±1		mV
		V _{BAT} = 2.5 to 5.0VDC		±2		
R _{BAT}	Effective input resistance		8			MΩ
t _{BAT}	Battery Voltage Conversion Time			11.7		ms
V _{ADC_RES}	Effective Resolution	V _{BAT}	14	15		bits
Coulomb Counter (CC)						
V _{CC_CM}	Common mode voltage range	V _{SS} = 0V, 2V ≤ V _{BAT} ≤ 5V	V _{SS}		V _{BAT}	V
V _{CC_IN}	Input voltage range		V _{CC_CM} −0.1		V _{CC_CM} +0.1	V
I _{CC_IN}	Effective input current sense range ⁽¹⁾ ⁽²⁾	Ideal R _{SNS} = 1mΩ (16-bit data limited)	±32,768			mA
		Ideal R _{SNS} = 2mΩ (16-bit data limited)				
		Ideal R _{SNS} = 5mΩ	±20,000			
t _{CC_CONV}	Conversion time	Single conversion		1000		ms
CC _{ADC_RES}	Effective Resolution			16		bits
		1LSB = VREF1/10/(±2 ¹⁵)		±3.7		μV
I _{CC_ERR}	Effective current measurement error	Ideal R _{SNS} = 1.0mΩ, 10.0A, T _A = 25 °C		26		mA
		Ideal R _{SNS} = 1.0mΩ, −10.0A, T _A = 25 °C		29		
CC _{OSE}	Offset error	16- bit Post-Calibration	−2.6	1.3	+2.6	LSB
CC _{OSE_DRIFT}	Offset error drift	15-bit + sign, Post Calibration		0.04	0.07	LSB/°C
CC _{GE}	Gain Error	15-bit + sign, Over input voltage range	−492	131	+492	LSB
R _{CC_IN}	Effective input resistance		7			MΩ
NTC THERMISTOR MEASUREMENT						
R _{NTC(PU)}	Internal Pullup Resistance	Factory Trimmed, firmware compensated	14.4	18	21.6	kΩ
R _{NTC(DRIFT)}	Resistance drift over temperature	Firmware compensated	−250	−120	0	PPM/°C
R _{NTC_ERR}	External NTC Thermistor Temperature Measurement Error with Linearization	Ideal 10KΩ 103AT NTC, TA = −10 to 70°C	−2	±1	+2	°C
		Ideal 10KΩ 103AT NTC, TA = −40 to 85°C	−3	±2	+3	
INTERNAL TEMPERATURE SENSOR						
V _(TEMP)	Internal Temperature sensor voltage drift	V _{TEMPP}	1.65	1.73	1.8	mV/°C
V _(TEMP)	Internal Temperature sensor voltage drift	V _{TEMPP} − V _{TEMPN} (specified by design)	0.17	0.18	0.19	mV/°C

(1) Firmware-based parameter. Not production tested.

(2) Limited by 16-bit two's-complement numeric format

5.5.6 Flash Memory

Unless otherwise noted, characteristics noted under conditions of $T_A = -40$ to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data retention		10	100		Years
Flash programming write cycles	Data Flash	20000			Cycles
	Instruction Flash	1000			Cycles
$t_{(\text{ROWPROG})}$	Row programming time			40	μs
$t_{(\text{MASSERASE})}$	Mass-erase time	$T_A = -40^\circ\text{C}$ to 85°C		40	ms
$t_{(\text{PAGEERASE})}$	Page-erase time	$T_A = -40^\circ\text{C}$ to 85°C		40	ms
$I_{\text{FLASHREAD}}$	Flash Read Current	$T_A = -40^\circ\text{C}$ to 85°C		1	mA
$I_{\text{FLASHWRTIE}}$	Flash Write Current	$T_A = -40^\circ\text{C}$ to 85°C		5	mA
$I_{\text{FLASHERASE}}$	Flash Erase Current	$T_A = -40^\circ\text{C}$ to 85°C		15	mA

5.6 Digital I/O: DC Characteristics

Unless otherwise noted, characteristics noted under conditions of $T_A = -40$ to 85°C , $V_{\text{REG18}} = 1.8\text{V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I²C PINS (SCL, SDA/HDQ)					
V_{IH}	High-level input voltage	SCL, SDA pins	1.26		V
V_{IL}	Low-level input voltage low	SCL, SDA pins		0.54	V
V_{OL}	Low-level output voltage	SCL, SDA pins, $I_{\text{OL}} = 1\text{mA}$		0.36	V
C_{I}	Input capacitance	SCL, SDA pins		10	pF
I_{IKg}	Input leakage current	SCL, SDA pins	1		μA
PUSH-PULL PINS (GPO)					
V_{IH}	High-level input voltage	Push-Pull pins	1.15		V
V_{IL}	Low-level input voltage low	Push-Pull pins		0.54	V
V_{OH}	Output voltage high	Push-Pull pins, $I_{\text{OH}} = -1\text{mA}$	1.08		V
V_{OL}	Output voltage low	Push-Pull pins, $I_{\text{OL}} = 1\text{mA}$		0.36	V
C_{I}	Input capacitance	Push-Pull pins		10	pF
I_{IKg}	Input leakage current	Push-Pull pins	1		μA

5.7 Digital I/O: Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
I²C TIMING — 100kHz					
f_{SCL}	Clock Operating Frequency	SCL duty cycle = 50%		100	kHz
$t_{\text{HD:STA}}$	START Condition Hold Time		4.0		μs
t_{LOW}	Low period of the SCL Clock		4.7		μs
t_{HIGH}	High period of the SCL Clock		4.0		μs
$t_{\text{SU:STA}}$	Setup repeated START		4.7		μs
$t_{\text{HD:DAT}}$	Data hold time (SDA input)		0		ns
$t_{\text{SU:DAT}}$	Data setup time (SDA input)		250		ns
t_{r}	Clock Rise Time	10% to 90%		1000	ns
t_{f}	Clock Fall Time	90% to 10%		300	ns
$t_{\text{SU:STO}}$	Setup time STOP Condition		4.0		μs
t_{BUF}	Bus free time STOP to START		4.7		μs
I²C TIMING — 400kHz					

5.7 Digital I/O: Timing Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f _{SCL}	Clock Operating Frequency	SCL duty cycle = 50%			400	kHz
t _{HD:STA}	START Condition Hold Time		0.6			μs
t _{LOW}	Low period of the SCL Clock		1.3			μs
t _{HIGH}	High period of the SCL Clock		600			ns
t _{SU:STA}	Setup repeated START		600			ns
t _{HD:DAT}	Data hold time (SDA input)		0			ns
t _{SU:DAT}	Data setup time (SDA input)		100			ns
t _r	Clock Rise Time	10% to 90%			300	ns
t _f	Clock Fall Time	90% to 10%			300	ns
t _{SU:STO}	Setup time STOP Condition		0.6			μs
t _{BUF}	Bus free time STOP to START		1.3			μs
HDQ Timing						
t _B	Break Time		190			μs
t _{BR}	Break Recovery Time		40			μs
t _{HW1}	Host Write 1 Time	Host drives HDQ	0.5		50	μs
t _{HW0}	Host Write 0 Time	Host drives HDQ	86		145	μs
t _{CYCH}	Cycle Time, Host to device	device drives HDQ	190			μs
t _{CYCD}	Cycle Time, device to Host	device drives HDQ	190	205	250	μs
t _{DW1}	Device Write 1 Time	device drives HDQ	32		50	μs
t _{DW0}	Device Write 0 Time	device drives HDQ	80		145	μs
t _{RSPS}	Device Response Time	device drives HDQ	190		950	μs
t _{TRND}	Host Turn Around Time	Host drives HDQ after device drives HDQ	250			μs
t _{RISE}	HDQ Line Rising Time to Logic 1				1.8	μs
t _{RST}	HDQ Reset	Host drives HDQ low before device reset	2.2			s

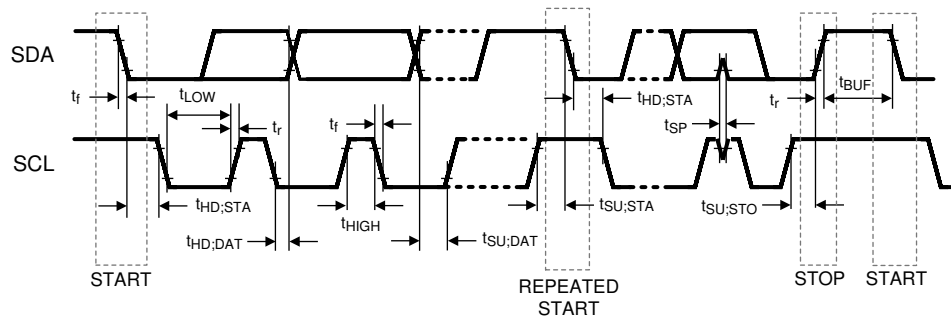
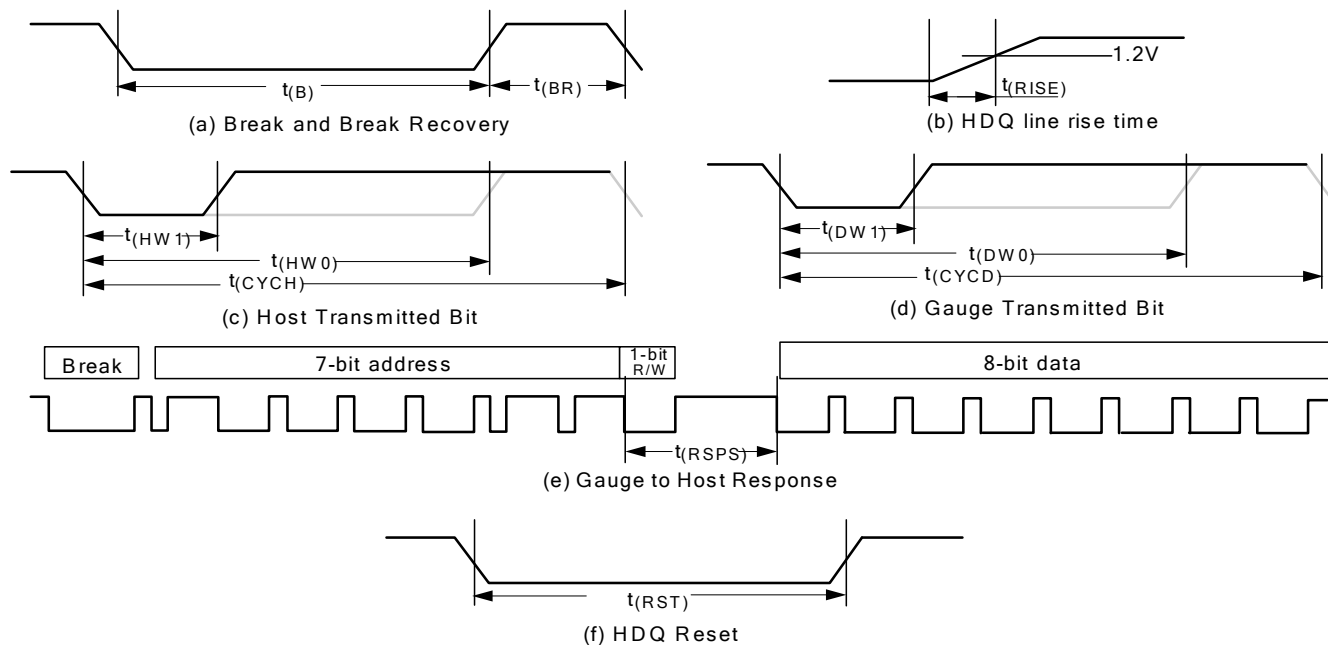


Figure 5-1. I²C Timing



- HDQ Breaking
- Rise time of HDQ line
- HDQ Host to fuel gauge communication
- Fuel gauge to Host communication
- Fuel gauge to Host response format
- HDQ Host to fuel gauge

Figure 5-2. HDQ Timing

5.8 Typical Characteristics

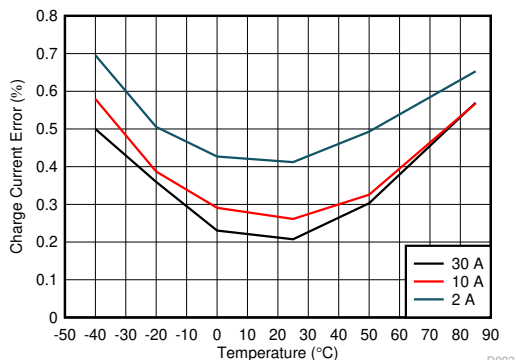


Figure 5-3. Charge Current Error vs Temperature and Charger Current with 1mΩ sense, No Calibration

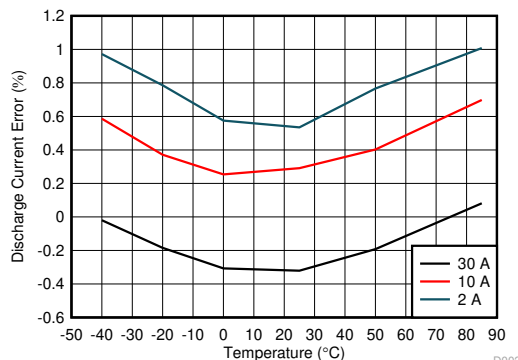


Figure 5-4. Discharge Current Error vs Temperature and Load Current with 1mΩ Sense, No Calibration

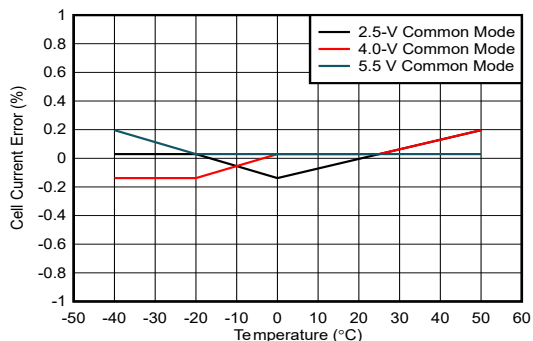


Figure 5-5. 2.2A Current Error vs CC ADC Input Common Mode Voltage and Temperature, No Calibration

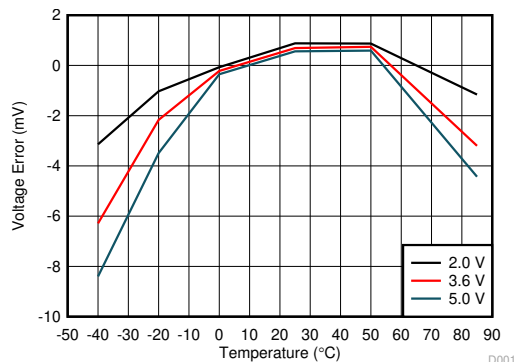


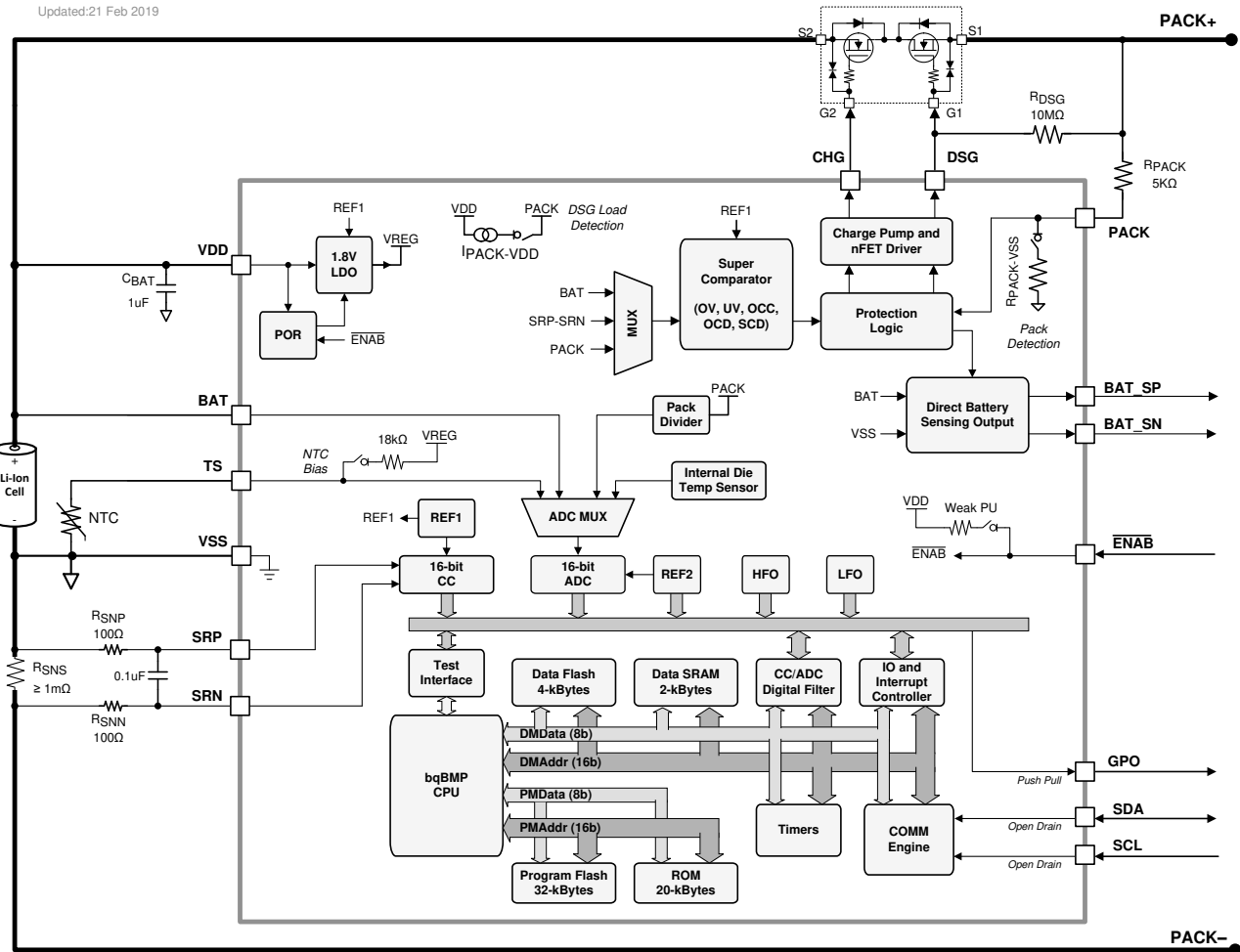
Figure 5-6. Cell Voltage Error vs Battery Voltage and Temperature

6 Detailed Description

6.1 Overview

The BQ27Z758 gas gauge is a fully integrated battery manager that employs flash-based firmware to provide a complete solution for battery-stack architectures composed of 1-series cells. The BQ27Z758 device interfaces with a host system through an I²C or HDQ protocol. High-performance, integrated analog peripherals enable support for a sense resistor down to 1mΩ, and simultaneous current/voltage data conversion for instant power calculations. The following sections detail all of the major component blocks included as part of the BQ27Z758 device.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 BQ27Z758 Processor

The BQ27Z758 device uses a custom TI-proprietary processor design that features a Harvard architecture and operates at frequencies up to 4.2MHz. Using an adaptive, three-stage instruction pipeline, the BQ27Z758 processor supports variable instruction lengths of 8, 16, or 24 bits.

6.3.2 Battery Parameter Measurements

The BQ27Z758 device measures cell voltage and current simultaneously, and also measures temperature to calculate the information related to remaining capacity, full charge capacity, state-of-health, and other gauging parameters.

6.3.2.1 Coulomb Counter (CC) and Digital Filter

The first ADC is an integrating analog-to-digital converter designed specifically for tracking charge and discharge activity, or coulomb counting, of a rechargeable battery. It features a single-channel differential input that converts the voltage difference across a sense resistor between the SRP and SRN terminals with a resolution of 3.74μV. The differential input common mode voltage range is from V_{SS} to V_{BAT} and supports a 1-series cell high-side or low-side sensing option with ± 0.1 -V input range. The CC digital filter generates a 16-bit conversion value from the delta-sigma CC front-end. New conversions are available every 1s.

6.3.2.2 ADC Multiplexer

The ADC multiplexer provides selectable connections to the external pins, BAT and TS, as well as the internal temperature sensor. In addition, the multiplexer can independently enable the TS input connection to the internal thermistor biasing circuitry, and enables the user to short the multiplexer inputs for test and calibration purposes.

6.3.2.3 Analog-to-Digital Converter (ADC)

The second ADC is a 16-bit delta-sigma converter designed for general-purpose measurements. The ADC automatically scales the input voltage range during sampling based on channel selection. The converter resolution is a function of its full-scale range and number of bits, yielding a 38μV resolution.

6.3.2.4 Internal Temperature Sensor

An internal temperature sensor is available on the BQ27Z758 device to reduce the cost, power, and size of the external components necessary to measure temperature. It is available for connection to the ADC using the multiplexer, and is ideal for quickly determining pack temperature under a variety of operating conditions.

6.3.2.5 External Temperature Sensor Support

The TS input is enabled with an internal 18kΩ (Typ.) linearization pull-up resistor to support the use of a 10kΩ (25°C) NTC external thermistor, such as the Semitec 103AT-2. The NTC thermistor should be connected between V_{SS} and the individual TS pin. The analog measurement is then taken by the ADC through its input multiplexer. If a different thermistor type is required, then changes to configurations may be required.

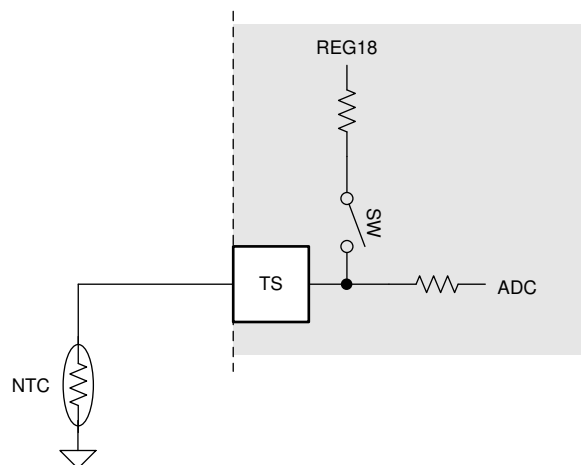


Figure 6-1. External Thermistor Biasing

6.3.3 Power Supply Control

The BQ27Z758 device uses the VDD pin as its power source. VDD powers the internal voltage sources that supply references for the device. The BAT pin is a non-current carrying path and used as a Kelvin sense connection to the battery cell.

6.3.4 \overline{ENAB} Pin

The BQ27Z758 device can use the active low digital input \overline{ENAB} pin to exit the device's SHELFB and SHUTDOWN power modes. The digital input is connected to a weak internal pullup to VDD. A push-button

can be connected to the $\overline{\text{ENAB}}$ pin to drive the pin to a low state for the device to exit SHELFB or SHUTDOWN mode.

If the $\overline{\text{ENAB}}$ pin is connected directly to the device's GND reference (VSS), the BQ27Z758 device will not be able to enter SHELFB or SHUTDOWN mode.

The $\overline{\text{ENAB}}$ pin can be left floating if using a push-button to exit SHELFB or SHUTDOWN mode is not needed. The $\overline{\text{ENAB}}$ pin can also be left floating if the device needs the capability to enter SHELFB or SHUTDOWN mode.

6.3.5 Bus Communication Interface

The BQ27Z758 device has an I²C bus communication interface. Alternatively, the device can be configured to communicate through the HDQ pin (shared with SDA). When performing operations while the device firmware is not actively executing (such as programming authentication keys or firmware onto the device), communicate to the device with 100KHz I2C clock frequency.

Note

Once the device is switched to the HDQ protocol, it is not reversible.

6.3.6 Low Frequency Oscillator

The BQ27Z758 device includes a low frequency oscillator (LFO) running at 65.536kHz.

6.3.7 High Frequency Oscillator

The BQ27Z758 includes a high frequency oscillator (HFO) running at 16.78MHz. It is frequency locked to the LFO output and scaled down to 8.388MHz with a 50% duty cycle.

6.3.8 1.8V Low Dropout Regulator

The BQ27Z758 device contains an integrated capacitor-less 1.8V LDO (REG18) that provides regulated supply voltage for the device CPU and internal digital logic.

6.3.9 Internal Voltage References

The BQ27Z758 device provides two internal voltage references. REF1 is used by REG18, oscillators, and CC. REF2 is used by the ADC.

6.3.10 Overcurrent in Discharge Protection

The overcurrent in discharge (OCD) function detects abnormally high current in the discharge direction. The overload in discharge threshold and delay time are configurable through the firmware register. The thresholds and timing can be fine-tuned even further based on a sense resistor with lower resistance or wider tolerance through calibration. When an OCD event occurs, the **Safety Status** flag is set to 1 and is latched until it is cleared and the fault condition is removed.

6.3.11 Overcurrent in Charge Protection

The overcurrent in charge (OCC) function detects abnormally high current in the charge direction. The overload in charge threshold and delay time are configurable through the firmware register. The thresholds and timing can be fine-tuned even further based on a sense resistor with lower resistance or wider tolerance through calibration. When an OCC event occurs, the **Safety Status** flag bit is set to 1 and is latched until it is cleared and the fault condition is removed.

6.3.12 Short-Circuit Current in Discharge Protection

The short-circuit current in discharge (SCD) function detects catastrophic current conditions in the discharge direction. The short-circuit in discharge thresholds and delay times are configurable through the firmware register. The thresholds and timing can be fine-tuned even further based on a sense resistor with lower resistance or wider tolerance with calibration. The detection circuit also incorporates a delay before disabling the CHG and DSG FETs. When an SCD event occurs, the **Safety Status** flag bit is set to 1 and is latched until it is cleared and the fault condition is removed.

6.3.13 Primary Protection Features

The BQ27Z758 gas gauge supports the following battery and system level protection features, which can be configured using firmware:

- Cell Undervoltage Protection
- Cell Overvoltage Protection
- Overcurrent in CHARGE Mode
- Overcurrent in DISCHARGE Mode
- Overload in DISCHARGE Mode
- Short Circuit in DISCHARGE Mode
- Overtemperature in CHARGE Mode
- Overtemperature in DISCHARGE Mode
- Precharge Timeout
- Fast Charge Timeout

6.3.14 Battery Sensing

The BQ27Z758 offers direct battery sensing through differential battery sensing pins BAT_SP and BAT_SN for accurate battery voltage measurement and detection. BQ27Z758 battery sensing path includes protection and isolation to minimize any leakage and coupling issue. The cell isolation includes a combination of buffered and resistive options. Firmware configuration allows seamless auto-transition between the two sensing schemes. The battery sensing buffer is powered from the PACK pin.

For accurate battery voltage sensing when using the sensing buffer, the PACK pin must be powered and $V_{PACK} > V_{BAT} + 0.7V$. The sensing protection thresholds (BCP, BCN, BDP, and BDN) provide short detection for the battery sensing output pins, and places the battery sensing output pins in a high impedance state when triggered. The BQ27Z758 battery sensing has firmware programmable offset options for applications where differential output voltage needs to be shifted to overcome an input range limitation. The offset voltage selected should never exceed the sensing protection thresholds, because this causes false battery sensing faults.

6.3.15 Gas Gauging

This device uses the Impedance Track™ technology to measure and determine the available charge in battery cells. See the [Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm Application Report](#) for further details.

6.3.16 Zero Volt Charging (ZVCHG)

ZVCHG (0V charging) is a special function that allows charging a severely depleted battery that is below the FET driver charge pump shutdown voltage (V_{FET_SHUT}). The BQ27Z758 has ZVCHG enabled with no inhibit. This means a severely depleted battery with a voltage as low as 0V can be charged. If $V_{BAT} < V_{FET_SHUT}$ and the charger voltage at PACK+ is $> V_{0CHGR}$, then the CHG output will be driven to the voltage of the PACK pin, allowing charging. ZVCHG mode in the BQ27Z758 is exited when $V_{BAT} > V_{FET_SHUT_REL}$, at which point the charge pump is enabled, and CHG transitions to being driven by the charge pump.

CAUTION

Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to have the ZVCHG battery charger function.

For safety purposes, the BQ27Z758 is specifically designed to be used in battery systems with at least 1 additional protector unit with an inhibited zero volt charging feature. This prevents unwanted battery self-discharge to severely low voltage levels or initiating charging at very low battery voltages that can cause irreversible damage to the battery.

6.3.17 Charge Control Features

This device supports charge control features, such as:

- Reports charging voltage and charging current based on the active temperature range—JEITA temperature ranges T1, T2, T3, T4, T5, and T6
- Provides more complex charging profiles, including sub-ranges within a standard temperature range
- Reports the appropriate charging current required for constant current charging, and the appropriate charging voltage needed for constant voltage charging to a smart charger, using the bus communication interface
- Selects the chemical state-of-charge of each battery cell using the Impedance Track method
- Provides pre-charging/zero-volt charging
- Employs charge inhibit and charge suspend if battery pack temperature is out of programmed range
- Activates charge and discharge alarms to report charging faults and to indicate charge status

6.3.18 Authentication

This device supports security with the following features, which can be enabled if desired:

- Authentication by the host using the SHA-256 method
- The gas gauge requires SHA-256 authentication before the device can be unsealed or allow full access.

6.4 Device Functional Modes

This device supports five modes, but the current consumption varies, based on firmware control of certain functions and modes of operation:

- **NORMAL mode:** In this mode, the device performs measurements, calculations, protections, and data updates every 250ms intervals. Between these intervals, the device operates in a reduced power state to minimize total average current consumption. Battery protections are continuously monitored and both protection NFETs are typically on.
- **SLEEP mode:** In this mode, the device performs measurements, calculations, and data updates in adjustable time intervals. Between these intervals, the device operates in a reduced power stage to minimize total average current consumption. Battery protections are continuously monitored and both protection NFETs are typically on.
- **SHIP mode:** In this mode, the device measures voltage and temperature very infrequently and at shorter ADC conversion times, and current is not measured or coulomb counted. Current is assumed to be, and reported as, 0mA. Therefore, the device tracks the battery's state-of-charge from OCVs. The measurements performed each interval are cell voltage, temperature, and PACK voltage (every fourth interval). Processing is minimized by reducing the number of calculations. Some calculations are performed less frequently: only after voltage and temperature are measured. These less frequent calculations include updating firmware-based protections, lifetime data, and the voltage and temperature ranges of the advanced charge algorithm. Other calculations, such as updating *RemainingCapacity()* and *FullChargeCapacity()*, are not performed at all with the assumption the system is off and will not communicate with the gauge. Battery protections are continuously monitored and both protection NFETs remain on, typically.
- **SHELF mode:** In this mode, power consumption is reduced even further from SHIP mode by turning off the CHG and DSG NFETs and all hardware-based protections. Due to this, no external power is available to the system in SHELF mode. The device measures voltage and temperature very infrequently and at shorter ADC conversion times, and current is not measured or coulomb counted. Current is assumed to be, and reported as, 0mA. Therefore, the device tracks the battery's state-of-charge from voltage measurements. The measurements performed each interval are cell voltage, temperature and PACK voltage (every fourth interval). Processing is minimized by reducing the number of calculations. Some calculations are performed less frequently: only after voltage and temperature are measured. These less frequent calculations include updating firmware-based protections, lifetime data, and the voltage and temperature ranges of the advanced charge algorithm. Other calculations, such as updating *RemainingCapacity()* and *FullChargeCapacity()*, are not performed at all with the assumption the system is off and will not communicate with the gauge.
- **SHUTDOWN mode:** In this mode, the device is completely disabled to minimize power consumption and to avoid depleting the battery.

6.4.1 Lifetime Logging Features

The device supports data logging of several key parameters for warranty and analysis:

- Maximum and minimum cell temperature

- Maximum current in CHARGE or DISCHARGE mode
- Maximum and minimum cell voltages
- Safety events and number of occurrences

6.4.2 Configuration

The device supports accurate data measurements and data logging of several key parameters.

6.4.2.1 Coulomb Counting

The device uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement. The ADC measures charge/discharge flow of the battery by measuring the voltage across a very small external sense resistor. The integrating ADC measures a bipolar signal from a range of -100mV to 100mV , with a positive value when $V_{(\text{SRP})} - V_{(\text{SRN})}$, indicating charge current and a negative value indicating discharge current.

The current measurement is performed by measuring the voltage drop across the external sense resistor, which can be as low as $1\text{m}\Omega$, and the polarity of the differential voltage determines if the cell is in the CHARGE or DISCHARGE mode.

6.4.2.2 Cell Voltage Measurements

The BQ27Z758 gas gauge measures the cell voltage at 1s intervals using the ADC. This measured value is internally scaled for the ADC and is calibrated to reduce any errors due to offsets. This data is also used for calculating the impedance of the cell for Impedance Track gas gauging.

6.4.2.3 Auto Calibration

The auto-calibration feature helps to cancel any voltage offset across the SRP and SRN pins for accurate measurement of the cell voltage, charge/discharge current, and thermistor temperature. The auto-calibration is performed when there is no communication activity for a minimum of 5s on the bus lines.

6.4.2.4 Temperature Measurements

This device has an internal sensor for on-die temperature measurements, and the ability to support an external temperature measurement through the external NTC on the TS pin. These two measurements are individually enabled and configured.

7 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The BQ27Z758 can be used with a 1-series Li-ion/Li polymer battery pack. To implement and design a comprehensive set of parameters for a specific battery pack, the user needs Battery Management Studio (BQStudio), which is a graphical user-interface tool installed on a PC during development. The firmware installed in the product has default values, which are summarized in the associated [BQ27Z746-R1](#) and [BQ27Z758 Technical Reference Manual](#). Using the BQStudio tool, these default values can be changed to cater to specific application requirements during development once the system parameters, such as enable or disable certain features for operation, cell configuration, chemistry that best matches the cell used, and more. The final flash image, which is extracted once configuration and testing are complete, is used for mass production and is referred to as the "golden image."

7.2 Typical Applications

The following are example BQ27Z758 application schematics for a single-cell battery pack.

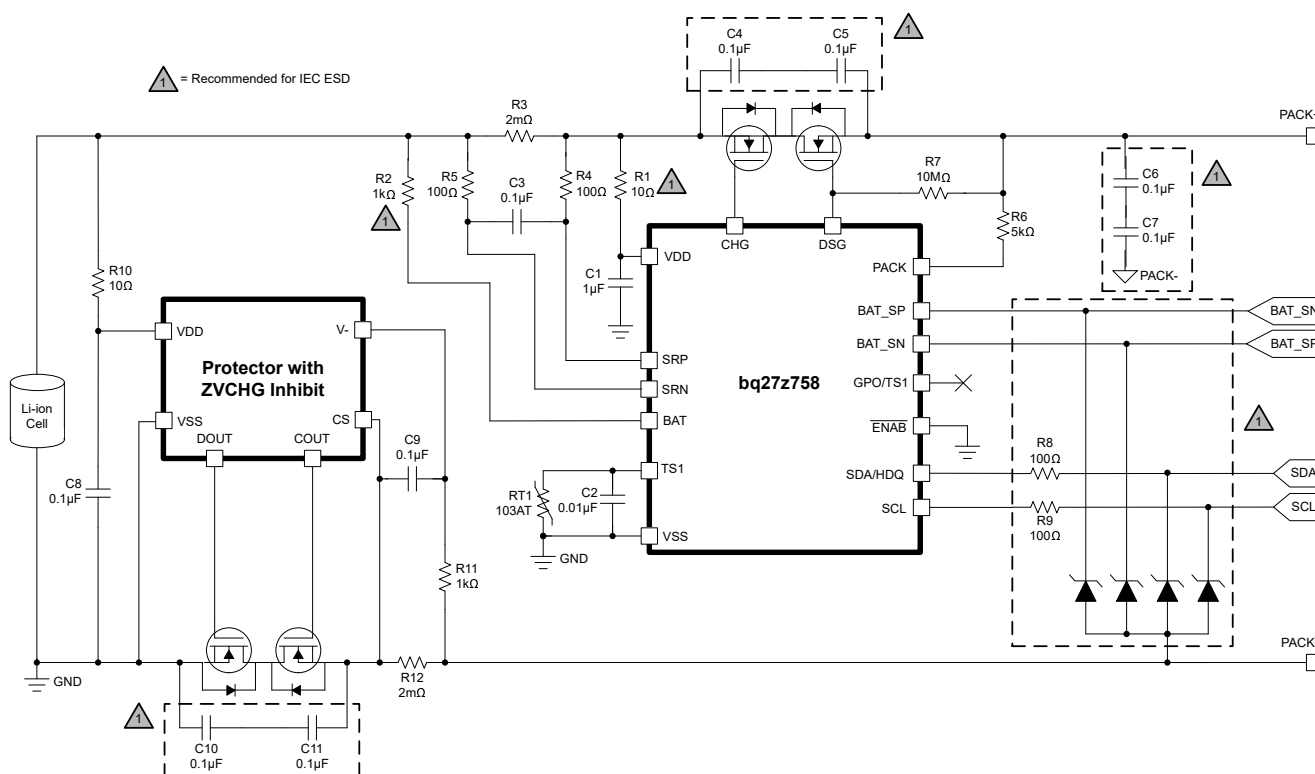


Figure 7-1. BQ27Z758 1-Series Cell High Side Current Sensing with Additional Protector Typical Implementation (Recommended)

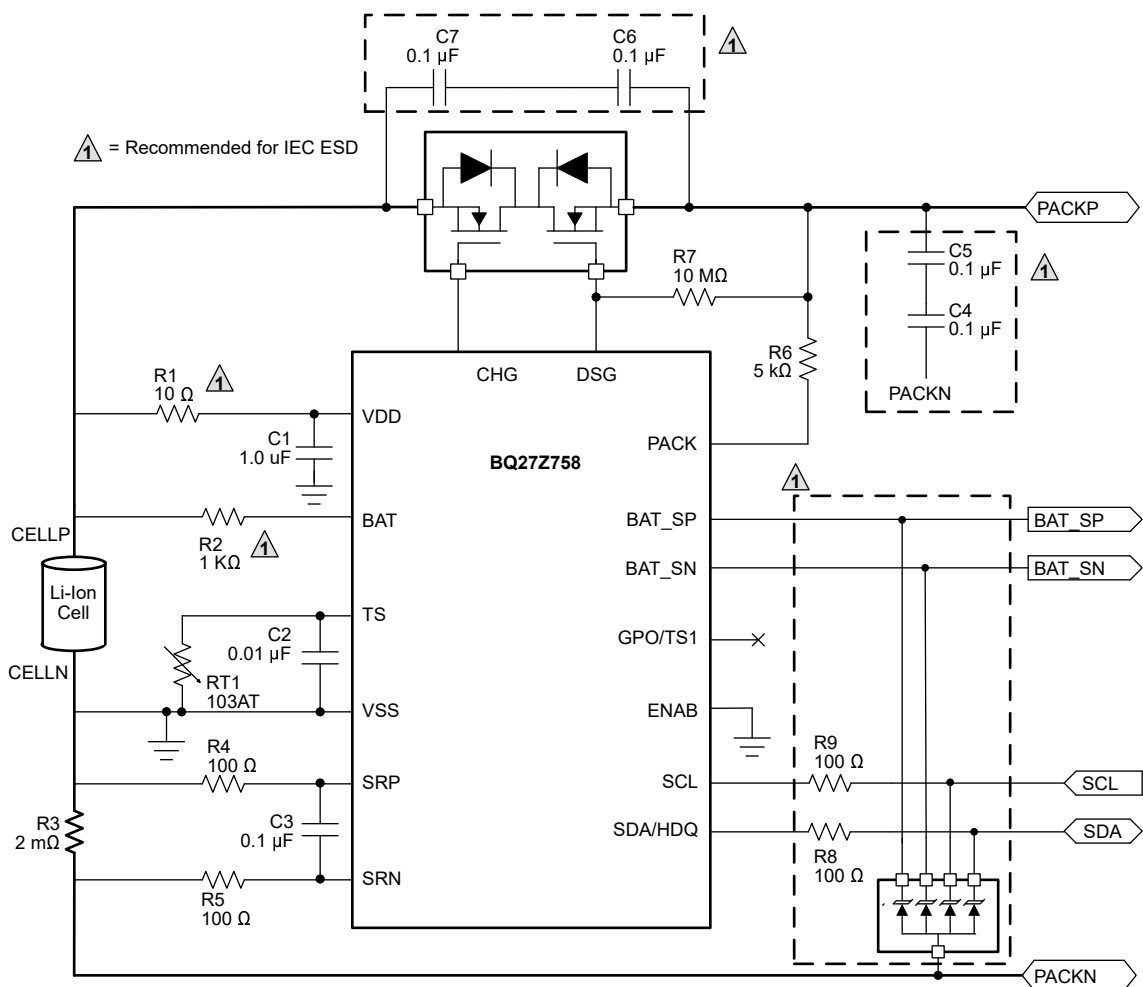


Figure 7-2. BQ27Z758 1-Series Cell Low Side Current Sensing Typical Implementation

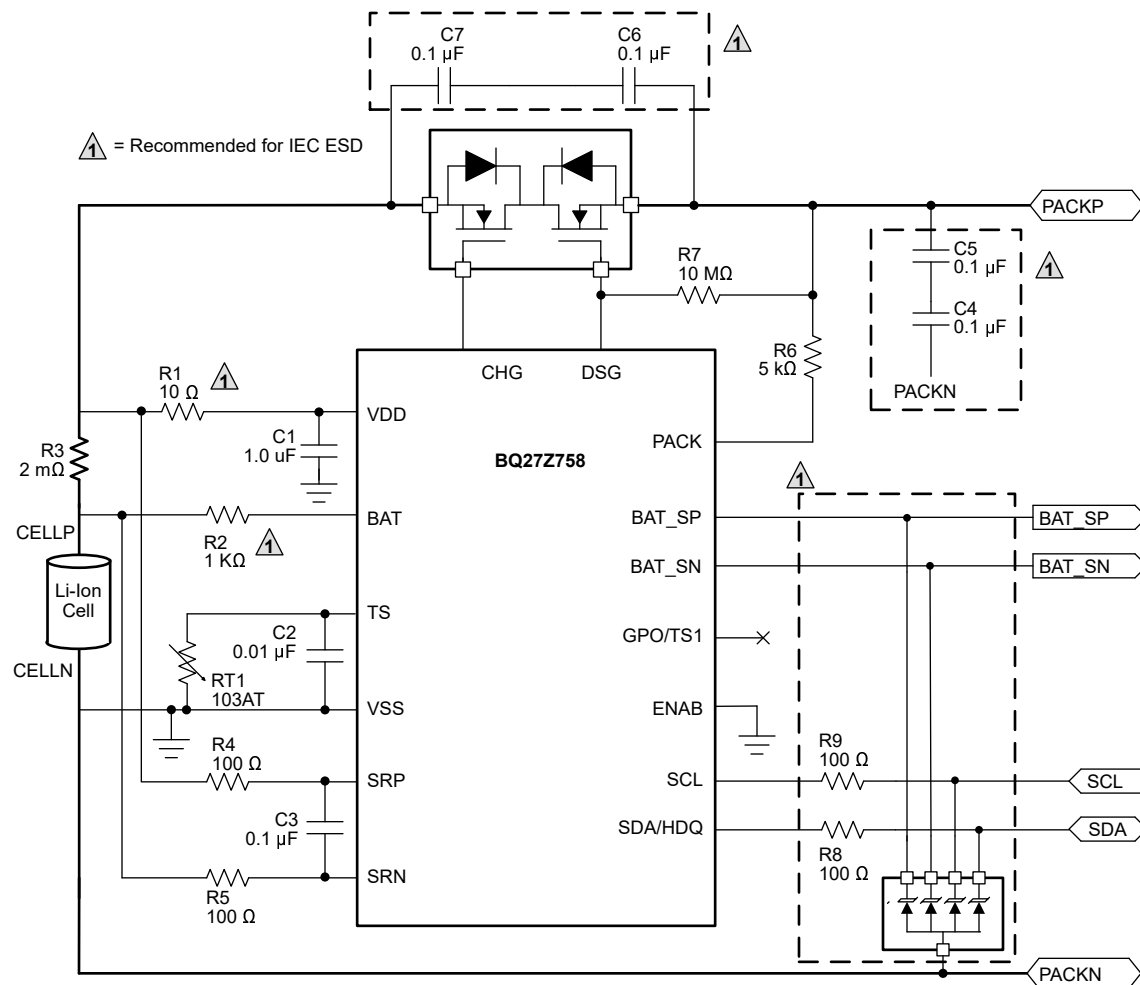


Figure 7-3. BQ27Z758 1-Series Cell High Side Current Sensing Typical Implementation

7.2.1 Design Requirements (Default)

Design Parameter	Example
Cell Configuration	1s1p (1 series with 1 parallel)
Design Capacity	5300mAh
Device Chemistry	Li-Ion
Design Voltage	4000mV
Cell Low Voltage	2500mV

7.2.2 Detailed Design Procedure

7.2.2.1 Changing Design Parameters

For the firmware settings needed for the design requirements, refer to the [BQ27Z746 Technical Reference Manual](#).

- To change design capacity, set the data flash value (in mAh) in the **Gas Gauging: Design: Design Capacity** register.
- To set device chemistry, go to the data flash **I²C Configuration: Data: Device Chemistry** . The BQStudio software automatically populates the correct chemistry identification. This selection is derived from using the BQCHEM feature in the tools and choosing the option that matches the device chemistry from the list.
- To set the design voltage, go to **Gas Gauging: Design: Design Voltage** register.

- To set the cell **Low Voltage** or clear the cell **Low Voltage**, use **Settings: Configuration: Init Voltage Low Set** or **Clear**. This is used to set the cell voltage level that will set (clear) the [VOLT_LO] bit in the *Interrupt Status* register.
- To enable the internal temperature and the external temperature sensors: Set **Settings: Configuration: Temperature Enable**: Bit 0 (TSInt) = 1 for the internal sensor; set Bit 1 (TS1) = 1 for the external sensor.

7.2.3 Calibration Process

The calibration of current, voltage, and temperature readings is accessible by writing 0xF081 or 0xF082 to *ManufacturerAccess()*. A detailed procedure is included in the [BQ27Z746R1 and BQ27Z758 Technical Reference Manual](#) in the *Calibration* section. The description allows for calibration of cell voltage measurement offset, battery voltage, current calibration, coulomb counter offset, PCB offset, CC gain/capacity gain, and temperature measurement for both internal and external sensors.

7.2.4 Gauging Data Updates

When a battery pack enabled with the BQ27Z758 gas gauge is cycled, the value of *FullChargeCapacity()* updates several times, including the onset of charge or discharge, charge termination, temperature delta, resistance updates during discharge, and relaxation. [Figure 7-4](#) shows actual battery voltage, load current, and *FullChargeCapacity()* when some of those updates occur during a single application cycle.

Update points from the plot include:

- Charge termination at 7900s
- Relaxation at 9900s
- Resistance update at 11500s

7.2.4.1 Application Curve

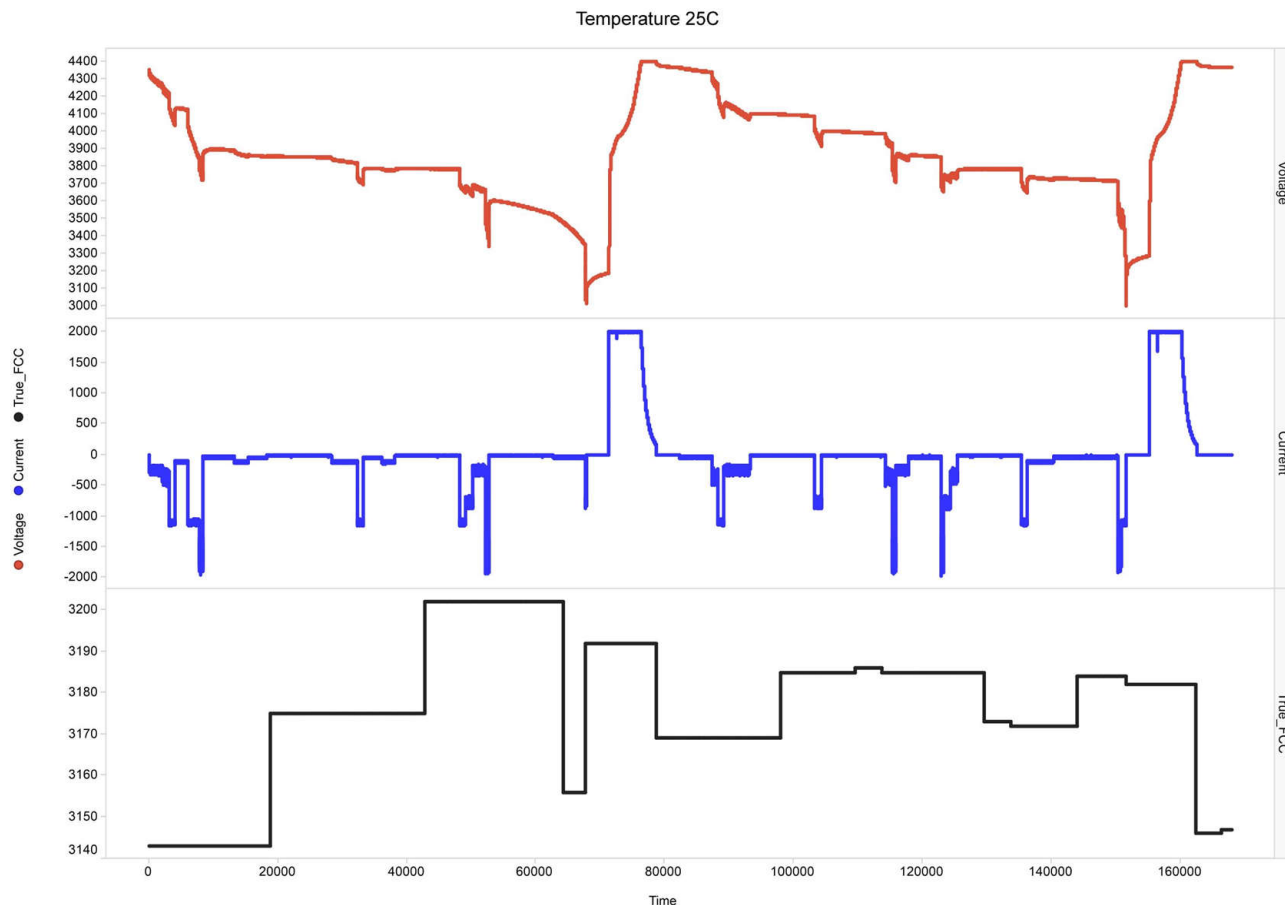


Figure 7-4. Full Charge Capacity Tracking (X-Axis is in Seconds)

7.2.5 ESD Mitigation

Optionally, to potentially improve ESD performance when the BQ27Z758 device is used in high side current sensing configuration, one recommendation is to use 500Ω resistors instead of 100Ω for the coulomb counter filter resistors (R4 and R5).

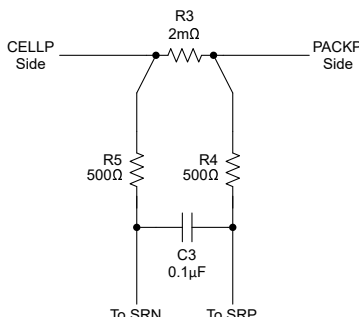


Figure 7-5. Coulomb Counter Filter with Recommended 500Ω Resistor for ESD Mitigation

7.3 Power Supply Requirements

The BQ27Z758 device uses the VDD pin as its power source. VDD pin powers the internal voltage sources that supply references for the device. The VDD pin connects to 1-series battery cells' positive terminal and supports a minimum of 2V to a maximum of 5V. The BAT pin is a non-current carrying path and is used as a battery voltage Kelvin sense connection to the 1-series battery cells positive terminal.

7.4 Layout

7.4.1 Layout Guidelines

- The quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50ppm to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the BQ27Z758 gas gauge. Select the smallest value possible to minimize thermal dissipation and still maintain required measurement accuracy. The value of the sense resistor impacts the differential voltage generated across the BQ27Z758 SRP and SRN nodes during a short circuit. These pins have a differential voltage should not exceed V_{CC_IN} of $\pm 0.1V$ for normal operation. Parallel sense resistors can be used as long as good Kelvin sensing is maintained. The device is designed to support a 1mΩ to 20mΩ sense resistor.
- BAT should be tied directly to the positive connection of the battery with a series 1kΩ resistor. It should not share a path with the VDD pin and its 10Ω series resistor.
- In reference to the gas gauge circuit, the following features require attention for component placement and layout: VDD bypass capacitor, SRN and SRP differential low-pass filter, and I²C communication ESD external protection.
- The BQ27Z758 gas gauge uses an integrating delta-sigma ADC for current measurements. Add a 100Ω resistor from the sense resistor to the SRP and SRN inputs of the device. Place a 0.1μF filter capacitor across the SRP and SRN inputs. Place all filter components as close as possible to the device. Route the traces from the sense resistor as differential pairs to the filter circuit. Adding a ground plane around the filter network can provide additional noise immunity.
- The BQ27Z758 has an internal LDO that is internally compensated and does not require an external decoupling capacitor.
- The I²C clock and data pins have integrated high-voltage ESD protection circuits; however, adding a Zener diode and series resistor provides more robust ESD performance. The I²C clock and data lines have an internal pulldown. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into SLEEP mode to conserve power.

7.4.2 Layout Example

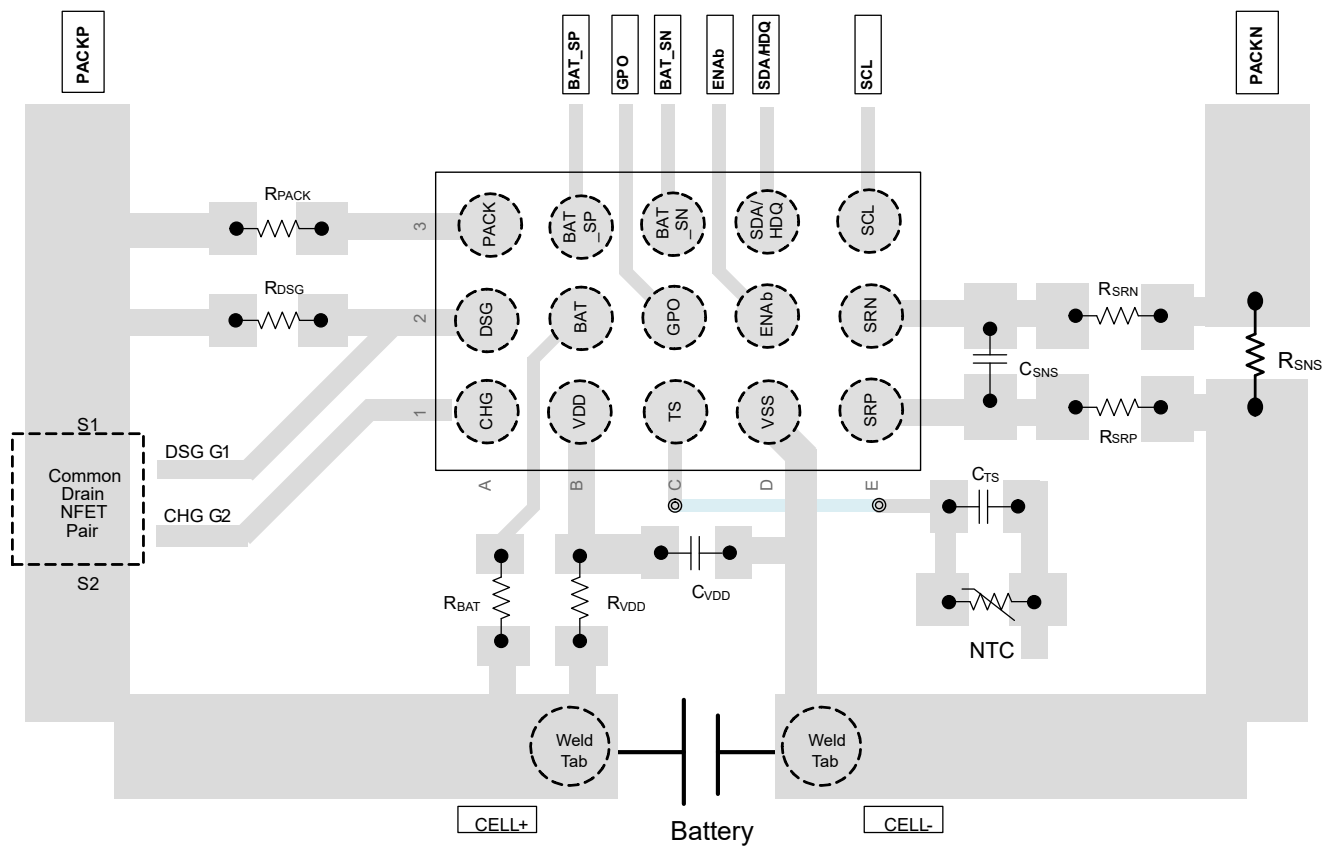


Figure 7-6. BQ27Z758 Key Trace Board Layout

8 Device and Documentation Support

8.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, [BQ27Z746-R1 and BQ27Z758 Technical Reference Manual](#)
- Texas Instruments, [Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm application note](#)

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Trademarks

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2025) to Revision C (September 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added <i>System-Level ESD Recommendations</i> section.....	26

Changes from Revision A (May 2025) to Revision B (May 2025)**Page**

- Added "...100KHz I2C clock frequency" sentence..... **18**

10 Mechanical, Orderable, and Packaging Information

The following pages include mechanical, orderable, and packaging information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

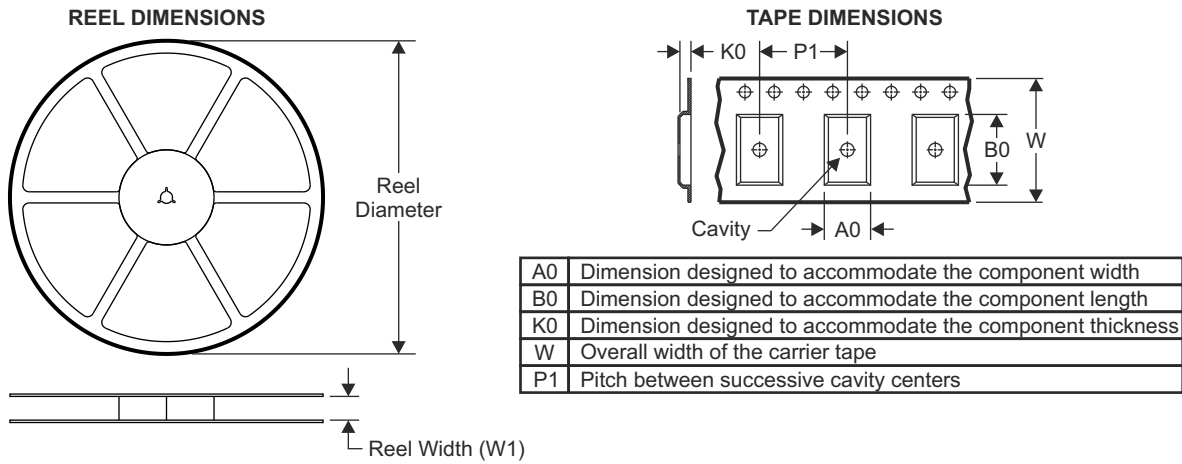
Orderable part number	Status ⁽¹⁾	Material type ⁽²⁾	Package Pins	Package qty Carrier	RoHS ⁽³⁾	Lead finish/Ball material ⁽⁴⁾	MSL rating/Peak reflow ⁽⁵⁾	Op temp (°C)	Part marking ⁽⁶⁾
BQ27Z758YAHR	Active	Production	DSBGA (YAH) 15	3000 LARGE T&R	Y	SAC396	Level-1-260C-UNLIM	-40 to 85	BQ27Z758
BQ27Z758YAHR.A	Active	Production	DSBGA (YAH) 15	3000 LARGE T&R	Y	SAC396	Level-1-260C-UNLIM	See BQ27Z758YAHR	BQ27Z758

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part. Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

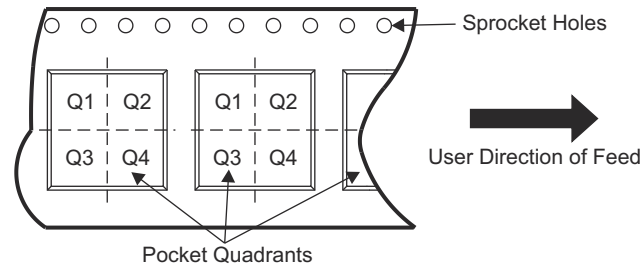
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10.1 Tape and Reel Information

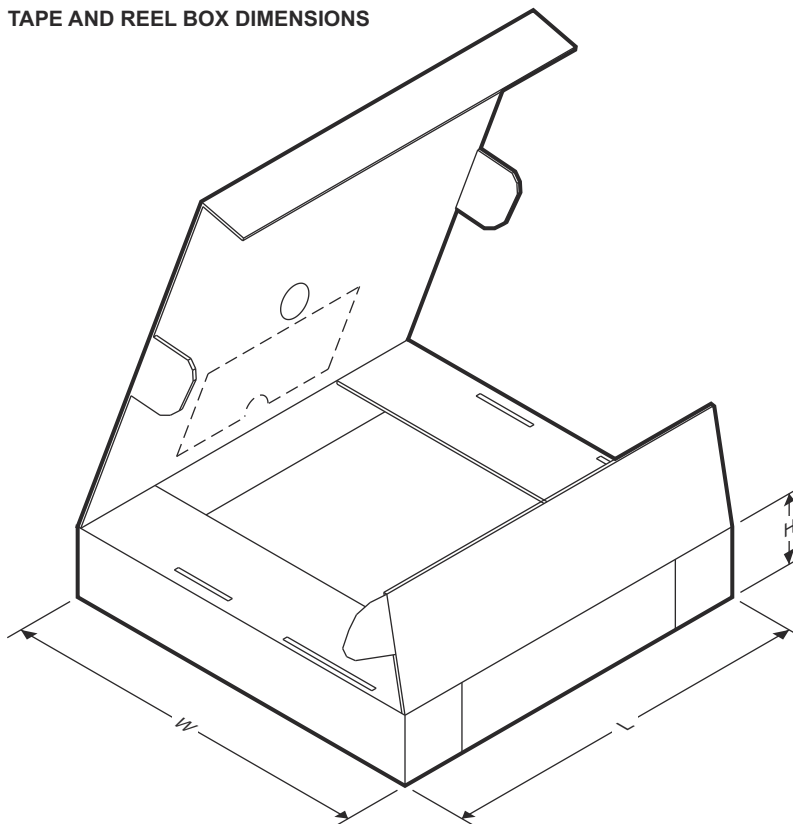


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



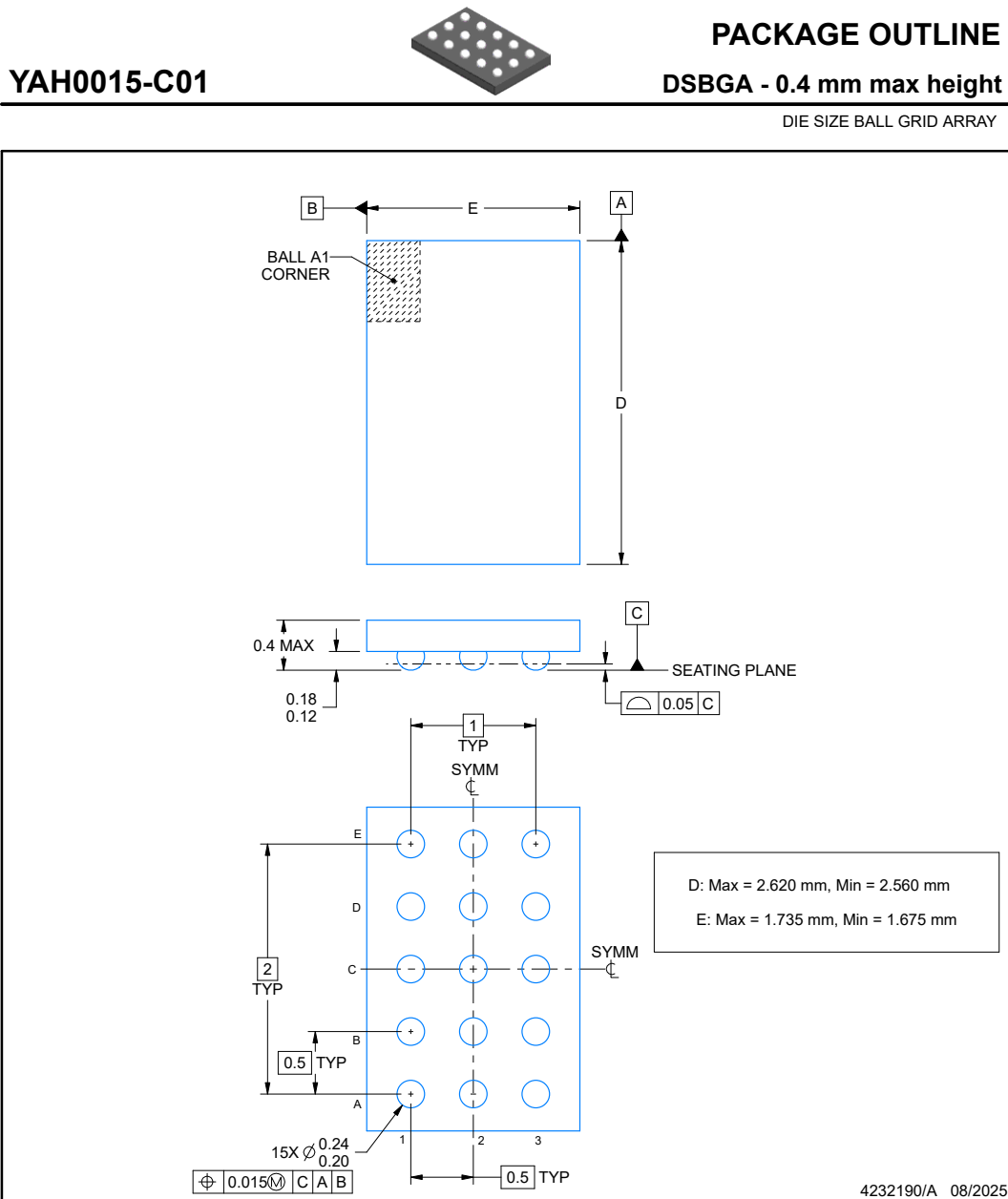
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27Z758YAHR	DSBGA	YAH	15	3000	180.0	12.4	1.88	2.76	0.55	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



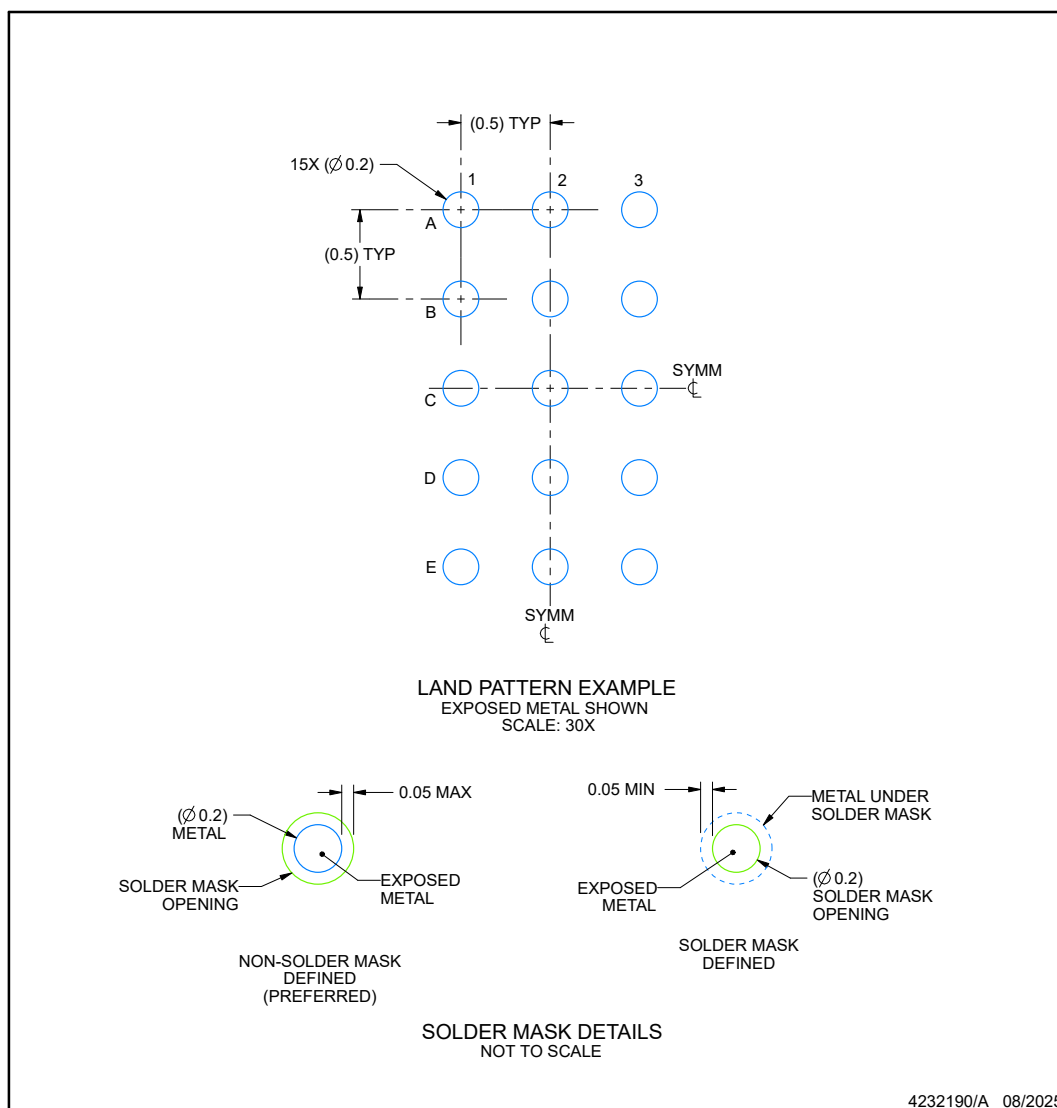
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27Z758YAHR	DSBGA	YAH	15	3000	182.0	182.0	20.0

10.2 Mechanical Data



EXAMPLE BOARD LAYOUT**YAH0015-C01****DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

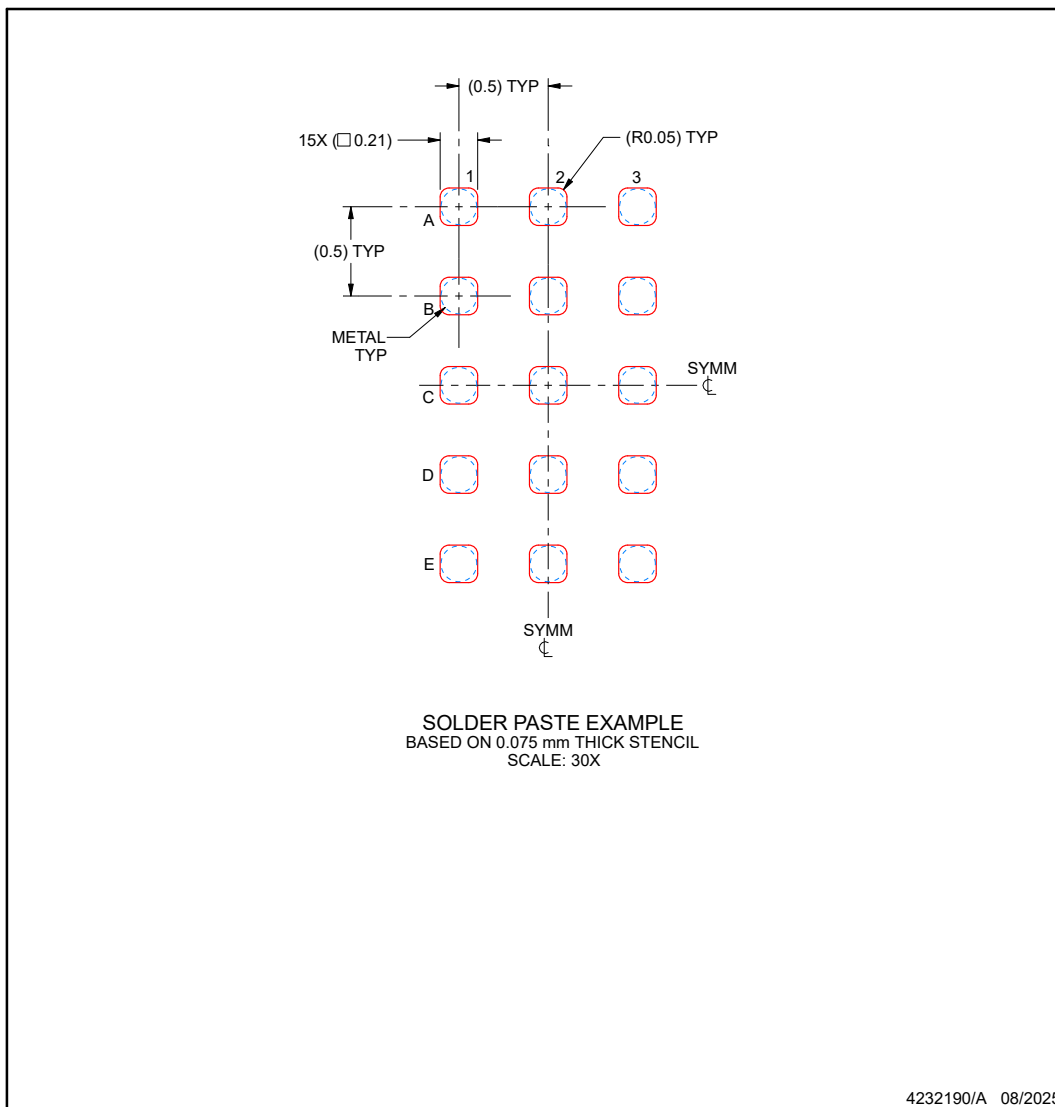
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YAH0015-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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