

# **bq25898, bq25898D I<sup>2</sup>C Controlled Single Cell 4-A Fast Charger with MaxCharge™ Technology for High Input Voltage and Adjustable Voltage USB On-the-Go Boost Mode**

## 1 Features

- High Efficiency 4-A, 1.5-MHz Switch Mode Buck Charge
  - 92% Charge Efficiency at 3 A and 91% Charge Efficiency at 4 A Charge Current
  - Optimize for High Voltage Input (9 V / 12 V)
  - Low Power PFM mode for Light Load Operations
- USB On-the-Go (OTG) with Adjustable Output from 4.5 V to 5.5 V
  - Selectable 500-KHz / 1.5-MHz Boost Converter with up-to 2.4 A Output
  - 94% Boost Efficiency at 5 V at 1 A Output
  - Accurate Hiccup Mode Overcurrent Protection
- Single Input to Support USB Input and Adjustable High Voltage Adapters
  - Support 3.9-V to 14-V Input Voltage Range
  - Input Current Limit (100 mA to 3.25 A with 50-mA resolution) to Support USB2.0, USB3.0 standard and High Voltage Adapters
  - Maximum Power Tracking by Input Voltage Limit up-to 14V for Wide Range of Adapters
  - Auto Detect USB SDP, CDP, DCP, and Non-Standard Adapters (bq25898)
  - Programmable D+/D- Drivers for Non-Standard Adapter Handshake
- Remote Battery Sensing
- Input Current Optimizer (ICO) to Maximize Input Power without Overloading Adapters
- Resistance Compensation (IRCOMP) from Charger Output to Cell Terminal
- Highest Battery Discharge Efficiency with 5-mΩ Battery Discharge MOSFET up to 9 A
- Integrated ADC for System Monitor (Voltage, Temperature, Charge Current)
- Narrow VDC (NVDC) Power Path Management
  - Instant-on Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- BATFET Control to Support Ship Mode, Wake Up, and Full System Reset
- Flexible Autonomous and I<sup>2</sup>C Mode for Optimal System Performance

- High Integration includes all MOSFETs, Current Sensing and Loop Compensation
- 12-μA Low Battery Leakage Current to Support Ship Mode
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% Charge Current Regulation
  - ±7.5% Input Current Regulation
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Thermal Regulation and Thermal Shutdown
- Available in 2.8-mm x 2.5-mm 42-Ball DSBGA Package

## 2 Applications

- Smart Phone
- Tablet PC
- Portable Internet Devices

## 3 Description

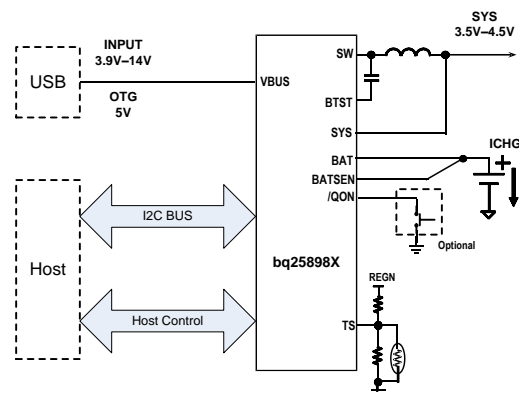
The bq25898, bq25898D are highly-integrated 4-A switch-mode battery charge management and system power path management devices for single cell Li-Ion and Li-polymer battery. The devices support high input voltage fast charging.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq25898	DSBGA (42)	2.80 mm x 2.50 mm
bq25898D	DSBGA (42)	2.80 mm x 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



Copyright © 2016, Texas Instruments Incorporated



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	9.4 Register Map.....	<b>34</b>
<b>2 Applications</b> .....	<b>1</b>	<b>10 Application and Implementation</b> .....	<b>51</b>
<b>3 Description</b> .....	<b>1</b>	10.1 Application Information.....	<b>51</b>
<b>4 Revision History</b> .....	<b>2</b>	10.2 Typical Application Diagram .....	<b>51</b>
<b>5 Description (Continued)</b> .....	<b>3</b>	10.3 System Example .....	<b>56</b>
<b>6 Device Comparison Table</b> .....	<b>4</b>	<b>11 Power Supply Recommendations</b> .....	<b>57</b>
<b>7 Pin Configuration and Functions</b> .....	<b>5</b>	<b>12 Layout</b> .....	<b>57</b>
<b>8 Specifications</b> .....	<b>7</b>	12.1 Layout Guidelines .....	<b>57</b>
8.1 Absolute Maximum Ratings .....	<b>7</b>	12.2 Layout Example .....	<b>57</b>
8.2 ESD Ratings.....	<b>7</b>	<b>13 Device and Documentation Support</b> .....	<b>58</b>
8.3 Recommended Operating Conditions.....	<b>8</b>	13.1 Device Support .....	<b>58</b>
8.4 Thermal Information .....	<b>8</b>	13.2 Related Links .....	<b>58</b>
8.5 Electrical Characteristics.....	<b>8</b>	13.3 Receiving Notification of Documentation Updates .....	<b>58</b>
8.6 Timing Requirements.....	<b>12</b>	13.4 Community Resources.....	<b>58</b>
8.7 Typical Characteristics .....	<b>14</b>	13.5 Trademarks .....	<b>58</b>
<b>9 Detailed Description</b> .....	<b>16</b>	13.6 Electrostatic Discharge Caution.....	<b>58</b>
9.1 Functional Block Diagram .....	<b>16</b>	13.7 Glossary .....	<b>58</b>
9.2 Feature Description.....	<b>17</b>	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>58</b>
9.3 Device Functional Modes.....	<b>33</b>		

## 4 Revision History

Changes from Revision A (December 2016) to Revision B	Page
• Full data sheet to product folder .....	<b>1</b>
Changes from Original (March 2016) to Revision A	Page
• Changed 93% to 94% in Features .....	<b>1</b>
• Changed anode to cathode in BTST .....	<b>6</b>
• Changed cathode to anode in REGN.....	<b>6</b>
• Changed falling to rising in $t_{ACOV\_RISING}$ test conditions in Electrical Characteristics .....	<b>9</b>
• Deleted USB SDP (USB100) and the OTG Pin column from <a href="#">Table 3</a> and <a href="#">Table 4</a> .....	<b>19</b>
• Changed VREF to VREGN in <a href="#">Equation 2</a> .....	<b>25</b>
• Changed VREF to VREGN in <a href="#">Figure 18</a> .....	<b>26</b>
• Changed 260 $\Omega$ to 232 $\Omega$ in <a href="#">Input Current Limit on ILIM</a> .....	<b>28</b>
• Added note to <a href="#">Figure 49</a> .....	<b>51</b>

## 5 Description (Continued)

The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I<sup>2</sup>C Serial interface with charging and system settings makes the device a truly flexible solution.

The bq25898/98D is a highly-integrated 4-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smartphone, tablet and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. It also integrates Input Current Optimizer (ICO) and Resistance Compensation (IRCOMP) to deliver maximum charging power to battery. The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive and battery monitor for simplified system design. The I<sup>2</sup>C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant adjustable high voltage adapter. To support fast charging using adjustable high voltage adapter, the bq25898D provides support for MaxCharge™ handshake using D+/D- pins and DSEL pin for USB switch control. In addition, both bq25898D and bq25898 include interface to support adjustable high voltage adapter using input current pulse protocol. To set the default input current limit, device uses the built-in USB interface (bq25898D) or takes the result from detection circuit in the system (bq25898), such as USB PHY device. The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. In addition, the Input Current Optimizer (ICO) supports the detection of maximum power point detection of the input source without overload. The device also meets USB On-the-Go (OTG) operation power rating specification by supplying 5 V (Adjustable 4.5V-5.5V) on VBUS with current limit up to 2.4 A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This operation prevents overloading the input source.

The device initiates and completes a charging cycle without software control. It automatically detects the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

The charger provides various safety features for battery charging and system operations, including battery temperature negative thermistor monitoring, charging safety timer and overvoltage/overcurrent protections. The thermal regulation reduces charge current when the junction temperature exceeds 120°C (programmable). The STAT output reports the charging status and any fault conditions. The  $\overline{\text{PG}}$  output (bq25898) indicates if a good power source is present. The INT immediately notifies host when fault occurs.

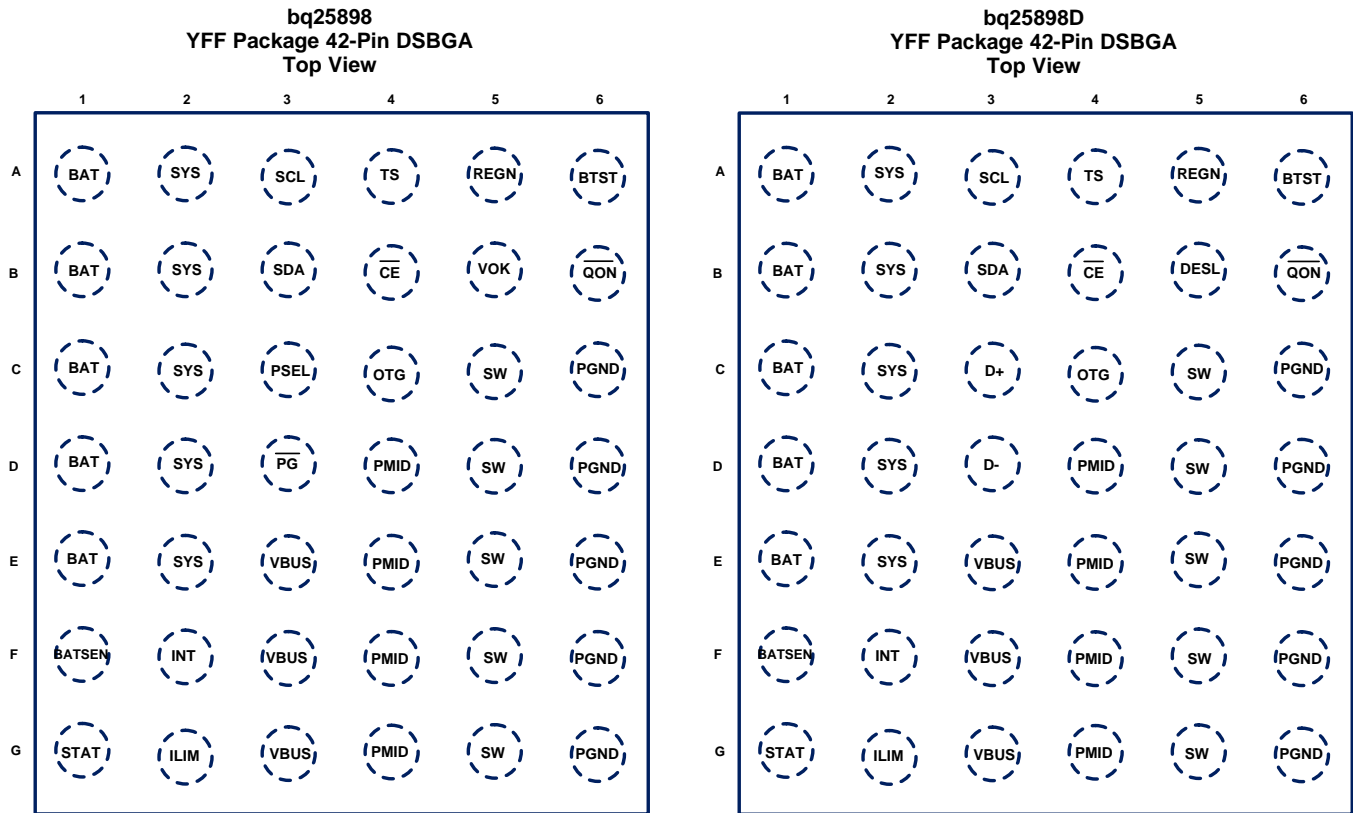
The device also provides a 7-bit analog-to-digital converter (ADC) for monitoring charge current and input/battery/system (VBUS, BAT, SYS, TS) voltages. The QON pin provides BATFET enable/reset control to exit low power ship mode or full system reset function.

The devices are available in a 42-ball, 2.8 mm x 2.5 mm DSBGA package.

## 6 Device Comparison Table

	<b>bq25898D</b>	<b>bq25898</b>
I <sup>2</sup> C Address	6AH (1101010B + R $\overline{W}$ )	6BH (1101011B + R $\overline{W}$ )
Charge Mode Frequency	1.5 MHz	1.5 MHz
Boost Mode Frequency	1.5 MHz (default) / 500 KHz	1.5 MHz (default) / 500 KHz
USB Detection	D+/D–	PSEL/OTG
VBUS Overvoltage	14.0 V	14.0 V
REGN LDO	6 V	6 V
Default Adapter Current Limit	3.25 A	3.25 A
Default Battery Charge Voltage	4.208 V	4.208 V
Maximum Charge Current	4.032 A	4.032 A
Default Charge Current	2.048 A	2.048 A
Default Pre-charge Current	128 mA	128 mA
Maximum Pre-charge Current	1.024 A	1.024A
Maximum Boost Mode Output Current	2.4A	2.4A
Charging Temperature Profile	JEITA	JEITA
Status Output	STAT	STAT, $\overline{PG}$

## 7 Pin Configuration and Functions



### Pin Functions

PIN			TYPE <sup>(1)</sup>	DESCRIPTION
NAME	bq25898	bq25898D		
VBUS	E3-G3	E3-G3	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-μF ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
D+	–	C3	AIO	Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter.
PSEL	C3	–	DI	Power source selection input. High indicates a USB host source and Low indicates an adapter source.
D–	–	D3	AIO	Negative line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter.
$\overline{\text{PG}}$	D3	–	DO	Open drain active low power good indicator. Connect to the pull up rail via 10-kΩ resistor. LOW indicates a good input source if the input voltage is within $V_{\text{VBUS\_OP}}$ , above SLEEP mode threshold ( $V_{\text{SLEEP2}}$ ), and current limit is above $I_{\text{BATSRC}}(30 \text{ mA})$ .
STAT	G1	G1	DO	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10-kΩ resistor. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin blinks in 1 Hz. The STAT pin function can be disabled when STAT_DIS bit is set.
SCL	A3	A3	DI	I2C Interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	B3	B3	DIO	I2C Interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
INT	F2	F2	DO	Open-drain Interrupt Output. Connect the INT to a logic rail via 10-kΩ resistor. The INT pin sends active low, 256-μs pulse to host to report charger device status and fault.
OTG	C4	C4	DI	Active high enable pin during boost mode. Deleted text from the OTG pin Description "OTG = High, IINLIM is set to USB500 mode". The boost mode is activated when OTG_CONFIG = 1 and OTG pin is high.Changed the Description of the OTG pin in the Pin Functions table.

(1) DI (Digital Input), DO (Digital Output), DIO (Digital Input/Output), AI (Analog Input), AO (Analog Output), AIO (Analog Input/Output)

### Pin Functions (continued)

PIN			TYPE <sup>(1)</sup>	DESCRIPTION
NAME	bq25898	bq25898D		
$\overline{\text{CE}}$	B4	B4	DI	Active low Charge Enable pin. Battery charging is enabled when CHG_CONFIG = 1 and CE pin = Low. CE pin must be pulled High or Low.
ILIM	G2	G2	AI	Input current limit Input. ILIM pin sets the maximum input current and can be used to monitor input current. ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 0.8 V. A resistor is connected from ILIM pin to ground to set the maximum limit as $I_{INMAX} = K_{ILIM}/R_{ILIM}$ . The actual input current limit is the lower limit set by ILIM pin (when EN_ILIM bit is high) or IILIM register bits. Input current limit of less than 500 mA is not support on ILIM pin. ILIM pin can also be used to monitor input current when the voltage is below 0.8V. The input current is proportional to the voltage on ILIM pin and can be calculated by $I_{IN} = (K_{ILIM} \times V_{ILIM}) / (R_{ILIM} \times 0.8)$ . The ILIM pin function can be disabled when EN_ILIM bit is 0.
TS	A4	A4	AI	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor.
$\overline{\text{QON}}$	B6	B6	DI	BATFET enable/reset control input. When BATFET is in ship mode, a logic low of $t_{SHIPMODE}$ (typical 1sec) duration turns on BATFET to exit shipping mode. . When VBUS is not plugged-in, a logic low of $t_{QON\_RST}$ (typical 19.5sec) duration resets SYS (system power) by turning BATFET off for $t_{BATFET\_RST}$ (typical 0.325sec) and then re-enable BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic
BAT	A1-E1	A1-E1	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10uF closely to the BAT pin.
SYS	A2-E2	A2-E2	P	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. Connect a 20uF closely to the SYS pin.
PGND	C6-G6	C6-G6	P	Power ground connection for high-current power converter node.
SW	C5-G5	C5-G5	P	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047μF bootstrap capacitor from SW to BTST.
BTST	A6	A6	P	PWM high side driver positive supply. Internally, the BTST is connected to the cathode of the boost-strap diode. Connect the 0.047μF bootstrap capacitor from SW to BTST.
REGN	A5	A5	P	PWM low side driver positive supply output. Internally, REGN is connected to the anode of the boost-strap diode. Connect a 4.7 μF (10 V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
PMID	D4-G44	D4-G4	DO	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Given the total input capacitance, put 1μF on VBUS to PGND, and the rest capacitance on PMID to PGND.
DSEL	–	B5	DO	Active high D+/D- multiplexer selection control. Connect a 47-nF (6V rating) ceramic capacitor from DSEL to analog GND. The pin is normally low. During input source type detection, the pin drives high to indicate the bq25890 D+/D- detection is in progress and needs to take control of D+, D- signals. When detection is completed, the pin keeps high when DCP, MaxCharge or HVDGP is detected. The pin returns to low when other input source type is detected
VOK	B5	–	DO	LDO output to driver USB PHY/MUX. Connect a 47nF ceramic capacitor from VOK to analog GND.
BATSEN	F1	F1	AI	Remote battery sense input. The typical pin resistance is 800 kΩ. Connect as close to battery as possible.

## 8 Specifications

### 8.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	VALUE
Voltage range (with respect to GND)	VBUS (converter not switching)	–2	22	V
	PMID (converter not switching)	–0.3	22	V
	STAT	–0.3	20	V
	$\overline{\text{PG}}$ (bq25898)	–0.3	7	V
	PSEL (bq25898)	–0.3	7	V
	VOK (bq25898)	–0.3	7	V
	DSEL (bq25898D)	–0.3	7	V
	D+, D– (bq25898D)	–0.3	7	V
	BTST	–0.3	20	V
	SW	–3	16	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SDA, SCL, INT, OTG, REGN, TS, $\overline{\text{CE}}$ , $\overline{\text{QON}}$	–0.3	7	V
	BTST TO SW	–0.3	7	V
	PGND to GND	–0.3	0.3	V
	BATSEN	–0.3	7	V
	ILIM	–0.3	5	V
Output sink current	INT, STAT		6	mA
	$\overline{\text{PG}}$ (bq25898)		6	mA
	DSEL (bq25898D)		5	mA
	VOK (bq25898)		5	mA
Junction temperature		–40	150	°C
Storage temperature range, T <sub>stg</sub>		–65	150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

### 8.2 ESD Ratings

			VALUE	UNIT
V <sub>ESD</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{IN}$	Input voltage	3.9	14 <sup>(1)</sup>	V
$I_{IN}$	Input current (VBUS)		3.25	A
$I_{SYS}$	Output current (SW)		4	A
$V_{BAT}$	Battery voltage		4.608	V
$I_{BAT}$	Fast charging current		4	A
	Discharging current with internal MOSFET		Up to 6 (continuous)	A
			9 (peak) (Up to 1 sec duration)	A
$T_A$	Operating free-air temperature range	–40	85	°C

- (1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

### 8.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		bq25898, bq25898D	UNIT
		YFF (DSBGA)	
		42-BALL	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.5	°C/W
$R_{\theta JCTop}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.2	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	8.2	°C/W
$R_{\theta JCBot}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 8.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>QUIESCENT CURRENTS</b>					
$I_{BAT}$	Battery discharge current (BAT, SW, SYS) in buck mode	$V_{BAT} = 4.2\text{ V}$ , $V_{(VBUS)} < V_{(UVLO)}$ , leakage between BAT and VBUS		5	μA
		High-Z Mode, No VBUS, BATFET Disabled (REG09[5] = 1), Battery Monitor Disabled, $T_J < 85^{\circ}\text{C}$	12	23	μA
		High-Z Mode, No VBUS, BATFET Enabled (REG09[5] = 0), Battery Monitor Disabled, $T_J < 85^{\circ}\text{C}$	32	60	μA
$I_{(VBUS\_HIZ)}$	Input supply current (VBUS) in buck mode when High-Z mode is enabled	$V_{(VBUS)} = 5\text{ V}$ , High-Z Mode, No Battery, Battery Monitor Disabled	15	35	μA
		$V_{(VBUS)} = 12\text{ V}$ , High-Z Mode, No Battery, Battery Monitor Disabled	25	50	μA
$I_{(VBUS)}$	Input supply current ( $V_{BUS}$ ) in buck mode	$V_{BUS} > V_{(UVLO)}$ , $V_{BUS} > V_{BAT}$ , Converter not switching	1.5	3	mA
		$V_{BUS} > V_{(UVLO)}$ , $V_{BUS} > V_{BAT}$ , Converter switching, $V_{BAT} = 3.2\text{ V}$ , $I_{SYS} = 0\text{ A}$	3		mA
		$V_{BUS} > V_{(UVLO)}$ , $V_{BUS} > V_{BAT}$ , Converter switching, $V_{BAT} = 3.8\text{ V}$ , $I_{SYS} = 0\text{ A}$	3		mA
$I_{(BOOST)}$	Battery discharge current in boost mode	$V_{BAT} = 4.2\text{ V}$ , Boost mode, $I_{(VBUS)} = 0\text{ A}$ , Converter switching	5		mA
<b>VBUS/BAT POWER UP</b>					
$V_{(VBUS\_OP)}$	VBUS operating range	3.9		14	V
$V_{(VBUS\_UVLOZ)}$	VBUS for active $I^2\text{C}$ , no battery	3.6			V
$V_{(SLEEP)}$	Sleep mode falling threshold	25	65	120	mV
$V_{(SLEEPZ)}$	Sleep mode rising threshold	130	250	370	mV



## Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(ACOV)}$	VBUS over-voltage rising threshold		13.9		14.6	V
	VBUS over-voltage falling threshold		13.3		13.9	V
$t_{ACOV\_RISING}$	ACOV rising deglitch	$V_{VBUS}$ rising		1		$\mu\text{s}$
$t_{ACOV\_FALLING}$	ACOV falling deglitch	$V_{VBUS}$ falling		1		ms
$V_{BAT(UVLOZ)}$	Battery for active $I^2\text{C}$ , no VBUS		2.3			V
$V_{BAT(DPL)}$	Battery depletion falling threshold		2.15		2.5	V
$V_{BAT(DPLZ)}$	Battery depletion rising threshold		2.35		2.7	V
$V_{(VBUSMIN)}$	Bad adapter detection threshold			3.8		V
$I_{(BADSRC)}$	Bad adapter detection current source			30		mA
<b>POWER-PATH MANAGEMENT</b>						
$V_{SYS}$	Typical system regulation voltage	$I_{(SYS)} = 0\text{ A}$ , $V_{BAT} > V_{SYS(MIN)}$ , BATFET Disabled (REG09[5]=1)		$V_{BAT} + 50\text{ mV}$		V
		$I_{SYS} = 0\text{ A}$ , $V_{BAT} < V_{SYS(MIN)}$ , BATFET Disabled (REG09[5]=1)		$V_{SYS(MIN)} + 250\text{ mV}$		V
$V_{SYS(MIN)}$	Minimum DC system voltage output	$V_{BAT} < V_{SYS(MIN)}$ , $SYS\_MIN = 3.5\text{ V}$ (REG03[3:1] = 101), $I_{SYS} = 0\text{ A}$	3.60	3.75		V
$V_{SYS(MAX)}$	Maximum DC system voltage output	$V_{BAT} = 4.35\text{ V}$ , $SYS\_MIN = 3.5\text{ V}$ (REG03[3:1] = 101), $I_{SYS} = 0\text{ A}$		4.40	4.42	V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET (RBFET) on-resistance between VBUS and PMID	$T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$		28	40	$\text{m}\Omega$
		$T_J = -40^{\circ}\text{C} - 125^{\circ}\text{C}$		28	47	$\text{m}\Omega$
$R_{ON(HSFET)}$	Top switching MOSFET (HSFET) on-resistance between PMID and SW	$T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$		24	33	$\text{m}\Omega$
		$T_J = -40^{\circ}\text{C} - 125^{\circ}\text{C}$		24	40	$\text{m}\Omega$
$R_{ON(LSFET)}$	Bottom switching MOSFET (LSFET) on-resistance between SW and GND	$T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$		12	18	$\text{m}\Omega$
		$T_J = -40^{\circ}\text{C} - 125^{\circ}\text{C}$		12	21	$\text{m}\Omega$
$V_{(FWD)}$	BATFET forward voltage in supplement mode	BAT discharge current 10 mA		30		mV
<b>BATTERY CHARGER</b>						
$V_{BAT(REG\_RANGE)}$	Typical charge voltage range		3.840		4.608	V
$V_{BAT(REG\_STEP)}$	Typical charge voltage step			16		mV
$V_{BAT(REG)}$	Charge voltage resolution accuracy	$V_{BAT} = 4.208\text{ V}$ (REG06[7:2] = 010111) or $V_{BAT} = 4.352\text{ V}$ (REG06[7:2] = 100000) $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$	-0.5%		0.5%	
$I_{(CHG\_REG\_RANGE)}$	Typical fast charge current regulation range		0		4032	mA
$I_{(CHG\_REG\_STEP)}$	Typical fast charge current regulation step			64		mA
$I_{(CHG\_REG\_ACC)}$	Fast charge current regulation accuracy	$V_{BAT} = 3.1\text{ V}$ or $3.8\text{ V}$ , $I_{CHG} = 256\text{ mA}$ $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$	-20%		20%	
		$V_{BAT} = 3.1\text{ V}$ or $3.8\text{ V}$ , $I_{CHG} = 1792\text{ mA}$ $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$	-5%		5%	
$V_{BAT(LOWV)}$	Battery LOWV falling threshold	Fast charge to precharge, BATLOWV (REG06[1]) = 1	2.6	2.8	2.9	V
	Battery LOWV rising threshold	Precharge to fast charge, BATLOWV (REG06[1]) = 1 (Typical 200-mV hysteresis)	2.8	3.0	3.15	V
	Battery LOWV falling threshold	Fast charge to precharge, BATLOWV (REG06[1]) = 0	2.5	2.6	2.7	V
	Battery LOWV rising threshold	Precharge to fast charge, BATLOWV (REG06[1]) = 0 (Typical 200-mV hysteresis)	2.7	2.8	2.9	V
$I_{(PRECHG\_RANGE)}$	Precharge current range		64		1024	mA
$I_{(PRECHG\_STEP)}$	Typical precharge current step			64		mA
$I_{(PRECHG\_ACC)}$	Precharge current accuracy	$V_{BAT} = 2.6\text{ V}$ , $I_{PRECHG} = 256\text{ mA}$	-20%		20%	
$I_{(TERM\_RANGE)}$	Termination current range		64		1024	mA
$I_{(TERM\_STEP)}$	Typical termination current step			64		mA
$I_{(TERM\_ACC)}$	Termination current accuracy	$I_{TERM} = 256\text{ mA}$ , $I_{CHG} \leq 1344\text{ mA}$ $T_J = -20^{\circ}\text{C} - 85^{\circ}\text{C}$	-20%		20%	
		$I_{TERM} = 256\text{ mA}$ , $I_{CHG} > 1344\text{ mA}$ $T_J = -20^{\circ}\text{C} - 85^{\circ}\text{C}$	-20%		20%	
$V_{(SHORT)}$	Battery short voltage	VBAT falling		2.0		V
$V_{(SHORT\_HYST)}$	Battery short voltage hysteresis	VBAT rising		200		mV
$I_{(SHORT)}$	Battery short current	VBAT < 2.2 V		110		mA

## Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>(RECHG)</sub>	Recharge threshold below V <sub>BATREG</sub>	V <sub>BAT</sub> falling, VRECHG (REG06[0] = 0) = 0		100		mV
		V <sub>BAT</sub> falling, VRECHG (REG06[0] = 0) = 1		200		mV
I <sub>BAT(LOAD)</sub>	Battery discharge load current	V <sub>BAT</sub> = 4.2 V	15			mA
I <sub>SYS(LOAD)</sub>	System discharge load current	V <sub>SYS</sub> = 4.2 V	30			mA
R <sub>ON(BATFET)</sub>	SYS-BAT MOSFET (BATFET) on-resistance	T <sub>J</sub> = 25°C		5	7	mΩ
		T <sub>J</sub> = -40°C - 125°C		5	10	mΩ
R <sub>BATSEN</sub>	BATSEN input resistance			800		kΩ
INPUT VOLTAGE / CURRENT REGULATION						
V <sub>IN(DPM_RANGE)</sub>	Typical input voltage regulation range		3.9		15.3	V
V <sub>IN(DPM_STEP)</sub>	Typical input voltage regulation step			100		mV
V <sub>IN(DPM_ACC)</sub>	Input voltage regulation accuracy	VINDPM = 4.4 V, 7.8 V, 10.8 V	-3%		3%	
I <sub>IN(DPM_RANGE)</sub>	Typical input current regulation range		100		3250	mA
I <sub>IN(DPM_STEP)</sub>	Typical input current regulation step			50		mA
I <sub>IN(DPM100_ACC)</sub>	Input current 100mA regulation accuracy V <sub>BAT</sub> = 5V, current pulled from SW	IINLIM (REG00[5:0]) = 100 mA	85	90	100	mA
I <sub>IN(DPM_ACC)</sub>	Input current regulation accuracy V <sub>BAT</sub> = 5V, current pulled from SW	USB150, IINLIM (REG00[5:0]) = 150 mA	125	135	150	mA
		USB500, IINLIM (REG00[5:0]) = 500 mA	440	470	500	mA
		USB900, IINLIM (REG00[5:0]) = 900 mA	750	825	900	mA
		Adapter 1.5 A, IINLIM (REG00[5:0]) = 1500 mA	1300	1400	1500	mA
I <sub>IN(START)</sub>	Input current regulation during system start up	V <sub>SYS</sub> = 2.2 V, IINLIM (REG00[5:0]) ≥ 200 mA			200	mA
K <sub>ILIM</sub>		I <sub>INMAX</sub> = K <sub>ILIM</sub> /R <sub>ILIM</sub> , Input Current regulation by ILIM pin = 1.5 A	290	320	350	A x Ω
VOK (bq25898)/DSEL (bq25898D)						
V <sub>VOK_OH</sub>	Voltage	VBUS > 6 V I(VOK) = 20 mA and I(REGN) = 30 mA	4.75		5.25	V
		VBUS = 5 V I(VOK) = 5 mA and I(REGN) = 30 mA	4.35		4.8	V
V <sub>VOK_OL</sub>	Voltage	Battery only VBAT = 3.8 V, I(VOK) = -10 mA			0.4	V
V <sub>DSEL_OH</sub>	Voltage	I(DSEL) = 20 mA and I(REGN) = 30 mA, VBUS = 5 V	1.3			V
V <sub>DSEL_OL</sub>	Voltage	I(DSEL) = -10 mA and I(REGN) = 30 mA, VBUS = 5 V			0.4	V
D+/D- DETECTION (bq25898D)						
I <sub>(10UA_ISRC)</sub>	D+ connection check current source		7	10	14	μA
I <sub>(100UA_ISINK)</sub>	D+/D- current sink (100 μA)		50	100	150	μA
I <sub>(DPDM_LKG)</sub>	D+/D- Leakage current	D-, switch open	-1		1	μA
		D+, switch open	-1		1	μA
I <sub>(1P6MA_ISINK)</sub>	D+/D- current sink (1.6 mA)		1.35	1.60	1.75	mA
R <sub>(D-_DWN)</sub>	D- pulldown for connection check		14.25		24.8	kΩ
V <sub>FLOAT_VDPSRC</sub>	D+/D- Voltage source (HIZ)	REG01[7:5] = 000 (default) or REG01[4:2] = 000 (default)		HIZ		V
V <sub>0P0_VDSRC</sub>	D+/D- Voltage source (0 V)	REG01[7:5] = 001 or REG01[4:2] = 001	0		0.15	V
V <sub>0P6_VDSRC</sub>	D+/D- Voltage source (0.6 V)	REG01[7:5] = 010 or REG01[4:2] = 010	0.5	0.6	0.7	V
V <sub>1P2_DPVSRC</sub>	D+/D- Voltage source (1.2 V)	REG01[7:5] = 011 or REG01[4:2] = 011	1.075	1.2	1.325	V
V <sub>2P0_DPVSRC</sub>	D+/D- Voltage source (2.0 V)	REG01[7:5] = 100 or REG01[4:2] = 100	1.875	2	2.125	V
V <sub>2P7_DPVSRC</sub>	D+/D- Voltage source (2.7 V)	REG01[7:5] = 101 or REG01[4:2] = 101	2.575	2.7	2.825	V
V <sub>3P3_DPVSRC</sub>	D+/D- Voltage source (3.3 V)	REG01[7:5] = 110 or REG01[4:2] = 110 or REG01[4:2] = 111	3.15	3.3	3.45	V
R <sub>DPDM_SHORT</sub>	D+/D- Short REG01[7:5] = 111				200	Ω
V <sub>(0P4_VTH)</sub>	D+/D- low comparator threshold		250		400	mV
V <sub>(0P8_VTH)</sub>	D+ low comparator threshold				0.8	V
V <sub>(2P7_VTH)</sub>	D+/D- comparator threshold for non-standard adapter detection (Divider 1, 3, or 4)		2.55		2.85	V
V <sub>(2P0_VTH)</sub>	D+/D- comparator threshold for non-standard adapter detection (Divider 1, 3)		1.85		2.15	V
V <sub>(1P2_VTH)</sub>	D+/D- comparator threshold for non-standard adapter detection (Divider 2)		1.05		1.35	V

## Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>BAT OVER-VOLTAGE/CURRENT PROTECTION</b>						
$V_{BAT(OVP)}$	Battery over-voltage threshold	$V_{BAT}$ rising, as percentage of $V_{BAT(REG)}$		104%		
$V_{BAT(OVP\_HYST)}$	Battery over-voltage hysteresis	$V_{BAT}$ falling, as percentage of $V_{BAT(REG)}$		2%		
$I_{BAT(FET\_OCP)}$	System over-current threshold		9			A
<b>THERMAL REGULATION AND THERMAL SHUTDOWN</b>						
$T_{REG}$	Junction temperature regulation accuracy	REG08[1:0] = 11		120		$^{\circ}\text{C}$
$T_{SHUT}$	Thermal shutdown rising temperature	Temperature rising		160		$^{\circ}\text{C}$
$T_{SHUT(HYS)}$	Thermal shutdown hysteresis	Temperature falling		30		$^{\circ}\text{C}$
<b>JEITA THERMISTOR COMPARATOR (BUCK MODE)</b>						
$V_{(T1)}$	T1 ( $0^{\circ}\text{C}$ ) threshold, charge suspended T1 below this temperature.	As percentage to $V_{(REGN)}$	72.75%	73.25%	73.75%	
$V_{(T1\_HYS)}$	Charge back to ICHG/2 (REG04[6:0]) and VREG (REG06[7:2]) above this temperature.	As Percentage to $V_{(REGN)}$		1.4%		
$V_{(T2)}$	T2 ( $10^{\circ}\text{C}$ ) threshold, charge back to ICHG/2 (REG04[6:0]) and VREG (REG06[7:2]) below this temperature.	As Percentage to $V_{(REGN)}$	67.75%	68.25%	68.75%	
$V_{(T2\_HYS)}$	Charge back to ICHG (REG04[6:0]) and VREG (REG06[7:2]) above this temperature.	As Percentage to $V_{(REGN)}$		1.4%		
$V_{(T3)}$	T3 ( $45^{\circ}\text{C}$ ) threshold, charge back to ICHG (REG04[6:0]) and VREG-200mV (REG06[7:2]) above this temperature.	As percentage to $V_{(REGN)}$	44.25v	44.75%	45.25%	
$V_{(T3\_HYS)}$	Charge back to ICHG (REG04[6:0]) and VREG (REG06[7:2]) below this temperature.	As Percentage to $V_{(REGN)}$		1%		
$V_{(T5)}$	T5 ( $60^{\circ}\text{C}$ ) threshold, charge suspended above this temperature.	As Percentage to $V_{(REGN)}$	33.875%	34.375%	34.875%	
$V_{(T5\_HYS)}$	Charge back to ICHG (REG04[6:0]) and VREG-200mV (REG06[7:2]) below this temperature.	As Percentage to $V_{(REGN)}$		1.25%		
<b>COLD/HOT THERMISTOR COMPARATOR (BOOST MODE)</b>						
$V_{(BCOLD1)}$	Cold temperature threshold 1, TS pin voltage rising threshold	As percentage to $V_{REGN}$ REG01[5] = 1 (Approx. $-20^{\circ}\text{C}$ w/ 103AT)	79.5%	80%	80.5%	
$V_{(BCOLD1\_HYS)}$	Cold temperature threshold 1, TS pin voltage falling threshold	As percentage to $V_{REGN}$ REG01[5] = 1		1%		
$V_{(BHOT2)}$	Hot temperature threshold 2, TS pin voltage falling threshold	As percentage to $V_{REGN}$ REG01[7:6] = 10 (Approx. $65^{\circ}\text{C}$ w/ 103AT)	30.75%	31.25%	31.75%	
$V_{(BHOT2\_HYS)}$	Hot temperature threshold 2, TS pin voltage rising threshold	As percentage to $V_{REGN}$ REG01[7:6] = 10		3%		
<b>PWM</b>						
$F_{SW}$	PWM switching frequency, and digital clock	Oscillator frequency	1.32		1.68	MHz
$D_{MAX}$	Maximum PWM duty cycle			97%		
<b>BOOST MODE OPERATION</b>						
$V_{(OTG\_REG\_RANGE)}$	Typical boost mode regulation voltage range		4.55		5.55	V
$V_{(OTG\_REG\_STEP)}$	Typical boost Mode Regulation voltage step			64		mV
$V_{(OTG\_REG\_ACC)}$	Boost mode regulation voltage accuracy	$I_{(VBUS)} = 0\text{ A}$ , BOOSTV = 4.998 V (REG0A[7:4] = 0111)	-3%		3%	
$V_{(OTG\_BAT)}$	Battery voltage exiting boost mode	BAT falling, REG03[0] = 0	2.7		2.9	V
		BAT falling, REG03[0] = 1	2.4		2.6	V
$I_{(OTG)}$	Typical boost mode output current range		0.5		2.45	A
$I_{(OTG\_OCP\_ACC)}$	Boost mode RBFET over-current protection accuracy	BOOST_LIM = 1.5 A (REG0A[2:0] = 100)	1.5		2.0	A
$V_{(OTG\_OVP)}$	Boost mode over-voltage threshold	Rising threshold	5.8	6		V
<b>REGN LDO</b>						
$V_{(REGN)}$	REGN LDO output voltage	$V_{(VBUS)} = 9\text{ V}$ , $I_{(REGN)} = 40\text{ mA}$	5.6	6	6.4	V
		$V_{(VBUS)} = 5\text{ V}$ , $I_{(REGN)} = 20\text{ mA}$	4.7	4.8		V
$I_{(REGN)}$	REGN LDO current limit	$V_{(VBUS)} = 9\text{ V}$ , $V_{(REGN)} = 3.8\text{ V}$	50			mA
<b>ANALOG-TO-DIGITAL CONVERTER (ADC)</b>						
RES	Resolution	Rising threshold		7		bits
$V_{BAT(RANGE)}$	Typical battery voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ or OTG mode is enabled	2.304		4.848	V
		$V_{(VBUS)} < V_{BAT} + V_{(SLEEP)}$ and OTG mode is disabled	$V_{SYS\_MIN}$		4.848	V
$V_{BAT\_RES}$	Typical battery voltage resolution			20		mV

## Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SYS\_RANGE)}$ Typical system voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ or OTG mode is enabled	2.304		4.848	V
	$V_{(VBUS)} < V_{BAT} + V_{(SLEEP)}$ and OTG mode is disabled	$V_{SYS\_MIN}$		4.848	V
$V_{(SYS\_RES)}$ Typical system voltage resolution			20		mV
$V_{(VBUS\_RANGE)}$ Typical $V_{VBUS}$ voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ or OTG mode is enabled	2.6		15.3	V
$V_{(VBUS\_RES)}$ Typical $V_{VBUS}$ voltage resolution			100		mV
$I_{BAT(RANGE)}$ Typical battery charge current range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ and $V_{BAT} > V_{BAT(SHORT)}$	0		4.032	A
$I_{BAT(RES)}$ Typical battery charge current resolution			50		mA
$V_{(TS\_RANGE)}$ Typical TS voltage range		21%		80%	
$V_{(TS\_RES)}$ Typical TS voltage resolution			0.47%		
<b>LOGIC I/O PIN (OTG, CE, PSEL, QON)</b>					
$V_{IH}$ Input high threshold level		1.3			V
$V_{IL}$ Input low threshold level				0.4	V
$I_{IN(BIAS)}$ High level leakage current	Pull-up rail 1.8 V			1	$\mu\text{A}$
$V_{(QON)}$ Internal /QON pull-up	Battery only mode		BAT		V
	$V_{(VBUS)} = 9\text{ V}$		5.8		V
	$V_{(VBUS)} = 5\text{ V}$		4.3		V
$R_{(QON)}$ Internal /QON pull-up resistance			200		k $\Omega$
<b>LOGIC I/O PIN (INT, STAT, PG)</b>					
$V_{OL}$ Output low threshold level	Sink Current = 5 mA, Sink current			0.4	V
$I_{OUT\_BIAS}$ High level leakage current	Pull-up rail 1.8 V			1	$\mu\text{A}$
<b>I2C INTERFACE (SCL, SDA)</b>					
$V_{IH}$ Input high threshold level, SCL and SDA	Pull-up rail 1.8 V	1.3			V
$V_{IL}$ Input low threshold level	Pull-up rail 1.8 V			0.4	V
$V_{OL}$ Output low threshold level	Sink Current = 5 mA, Sink current			0.4	V
$I_{BIAS}$ High level leakage current	Pull-up rail 1.8 V			1	$\mu\text{A}$

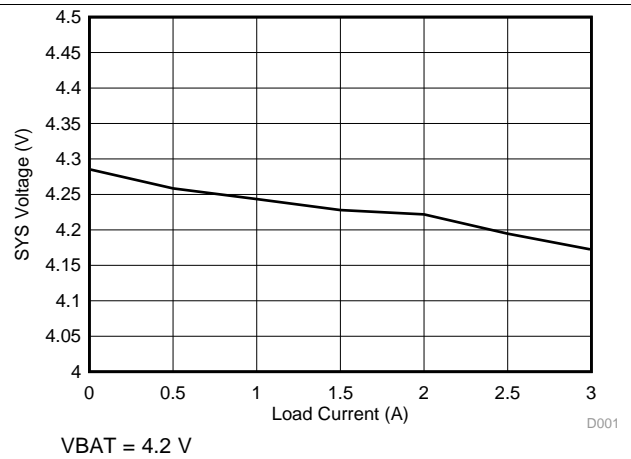
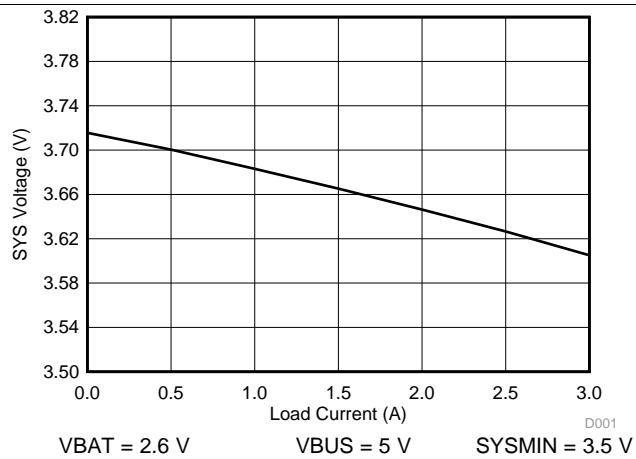
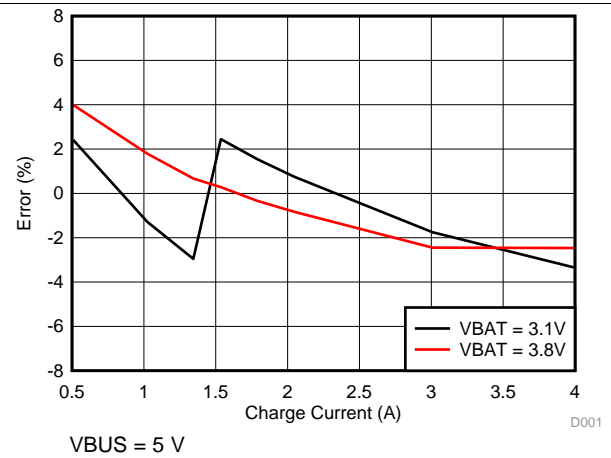
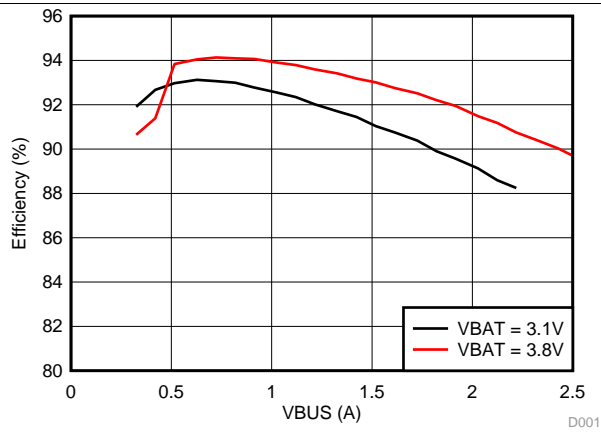
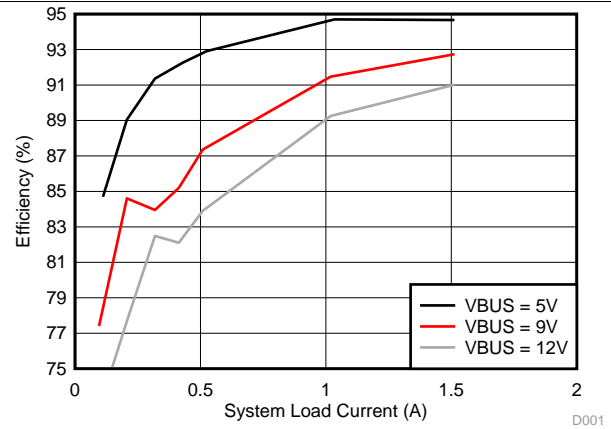
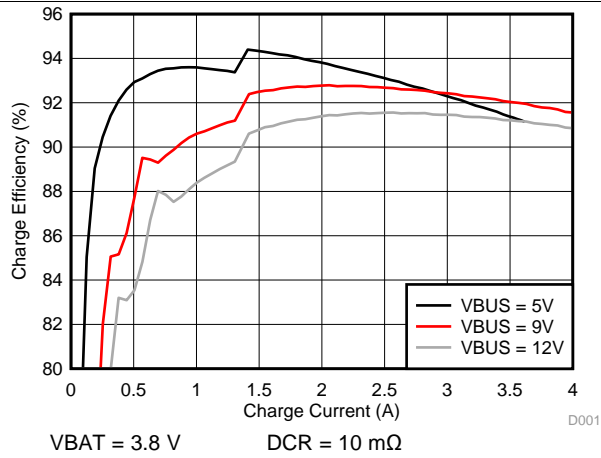
## 8.6 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>VBUS/BAT POWER UP</b>					
$t_{BADSRC}$ Bad adapter detection duration			30		msec
<b>BAT OVER-VOLTAGE PROTECTION</b>					
$t_{BATOVP}$ Battery over-voltage deglitch time to disable charge			1		$\mu\text{s}$
<b>BATTERY CHARGER</b>					
$t_{RECHG}$ Recharge deglitch time			20		msec
<b>Current Pulse Control</b>					
$t_{PUMPX\_STOP}$ Current pulse control stop pulse		430		570	msec
$t_{PUMPX\_ON1}$ Current pulse control long on pulse		240		360	msec
$t_{PUMPX\_ON2}$ Current pulse control short on pulse		70		130	msec
$t_{PUMPX\_OFF}$ Current pulse control off pulse		70		130	msec
$t_{PUMPX\_DLY}$ Current pulse control stop start delay		80		225	msec
<b>BATTERY MONITOR</b>					
$t_{CONV}$ Conversion time	CONV_RATE(REG02[6]) = 0		8	1000	msec
<b>QON and SHIPMODE TIMING</b>					
$t_{SHIPMODE}$ $\overline{\text{QON}}$ low time to turn on BATFET and exit ship mode	$T_J = -10^{\circ}\text{C} - 60^{\circ}\text{C}$	0.8		1.3	sec
$t_{QON\_RST}$ $\overline{\text{QON}}$ low time to enable full system reset	$T_J = -10^{\circ}\text{C} - 60^{\circ}\text{C}$	15.5		23	sec
$t_{BATFET\_RST}$ BATFET off time during full system reset	$T_J = -10^{\circ}\text{C} - 60^{\circ}\text{C}$	250		400	msec

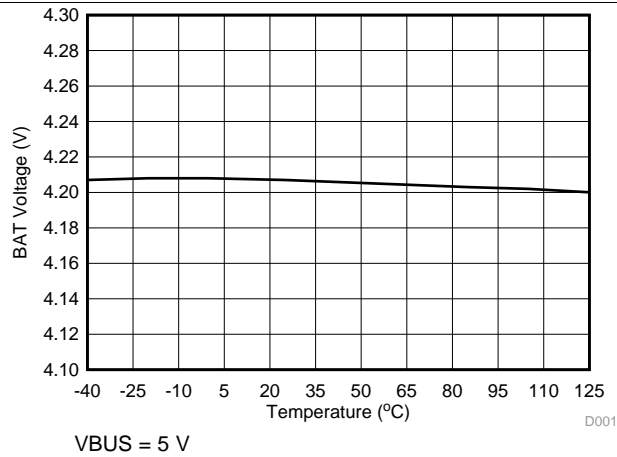
## Timing Requirements (continued)

			MIN	NOM	MAX	UNIT
t <sub>SM_DLY</sub>	Enter ship mode delay	T <sub>J</sub> = -10°C - 60°C	10		15	sec
<b>I2C INTERFACE</b>						
f <sub>SCL</sub>	SCL clock frequency				400	KHz
<b>DIGITAL CLOCK and WATCHDOG TIMER</b>						
f <sub>LPDIG</sub>	Digital low power clock	REGN LDO disabled	18	30	45	KHz
f <sub>DIG</sub>	Digital clock	REGN LDO enabled	1320	1500	1680	KHz
t <sub>WDT</sub>	Watchdog reset time	WATCHDOG (REG07[5:4])=11, REGN LDO disabled	100	160		sec
		WATCHDOG (REG07[5:4])=11, REGN LDO enabled	136	160		sec

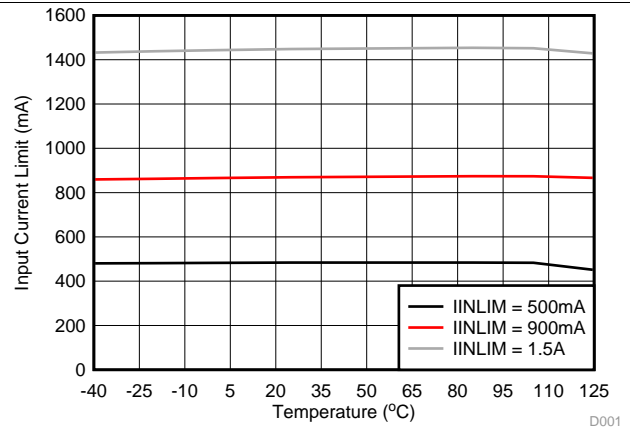
## 8.7 Typical Characteristics



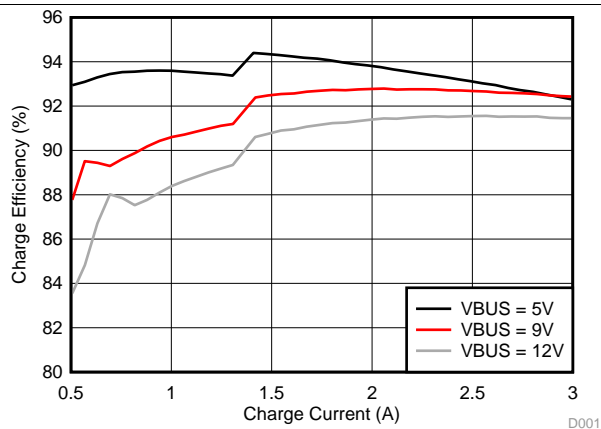
## Typical Characteristics (continued)



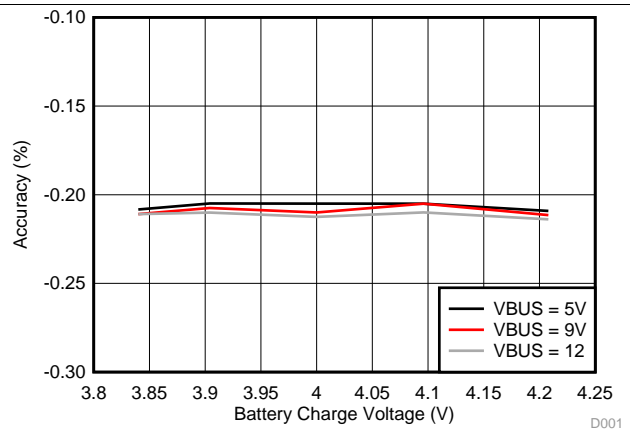
**Figure 7. BAT Voltage vs Temperature**



**Figure 8. Input Current Limit vs Temperature**



**Figure 9. Charge Efficiency**

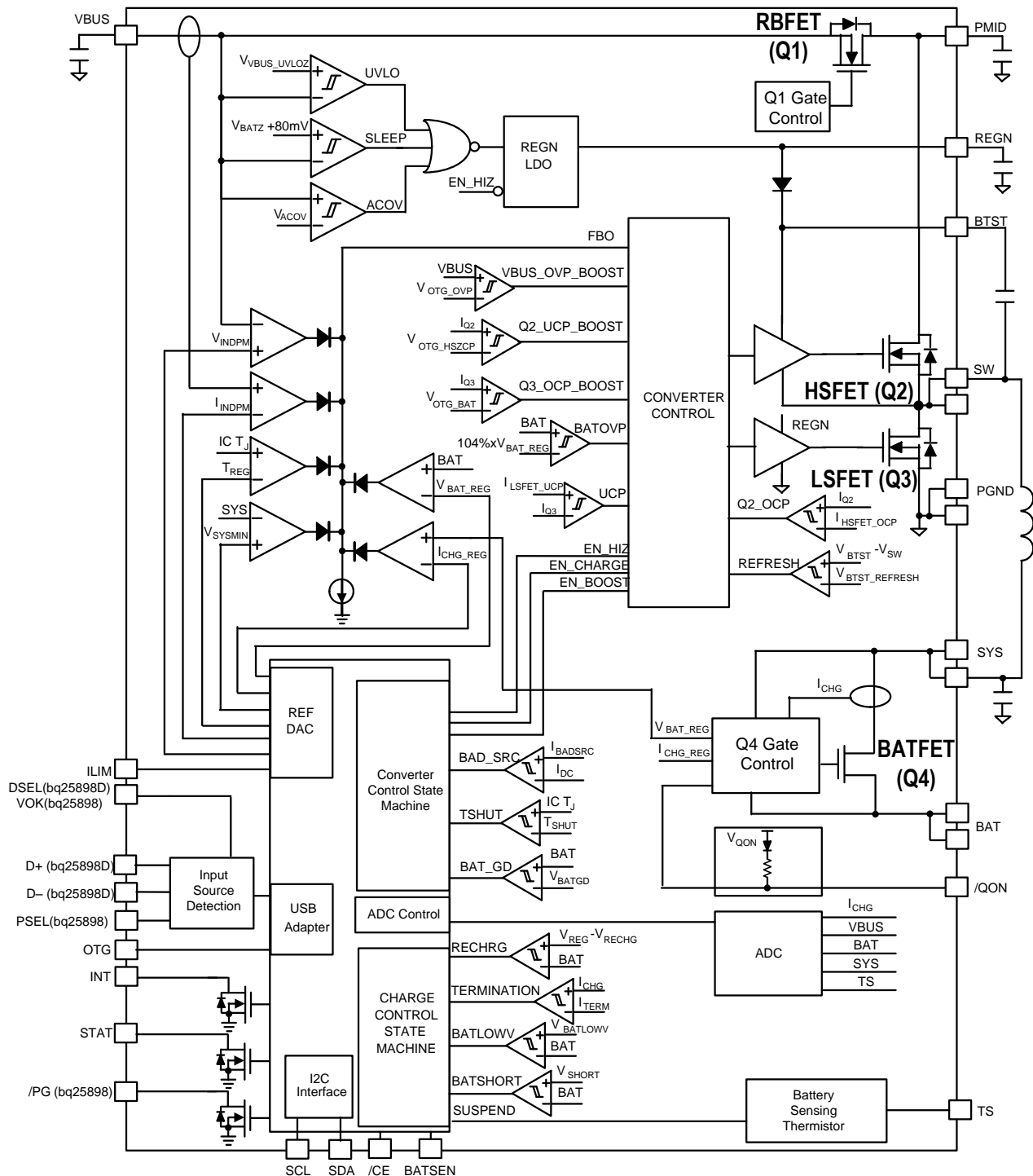


**Figure 10. Charge Voltage Accuracy**

## 9 Detailed Description

The device is a highly integrated 4-A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It is highly integrated with the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4). The device also integrates the bootstrap diode for the high-side gate drive.

### 9.1 Functional Block Diagram





## 9.2 Feature Description

### 9.2.1 Device Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS rises above  $V_{VBUS\_UVLOZ}$  or BAT rises above  $V_{BAT\_UVLOZ}$ , the sleep comparator, battery depletion comparator and BATFET driver are active. I<sup>2</sup>C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

### 9.2.2 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold ( $V_{BAT\_DPLZ}$ ), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low  $R_{DS(ON)}$  of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET (see [Supplement Mode](#)). When the system is overloaded or shorted ( $IBAT > I_{BATFET\_OCP}$ ), the device turns off BATFET immediately and sets BATFET\_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods describe in [BATFET Enable \(Exit Shipping Mode\)](#) is applied to re-enable BATFET.

### 9.2.3 Device Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started when AUTO\_DPDM\_EN bit is set. The power up sequence from input source is as listed:

1. Power Up REGN LDO
2. Poor Source Qualification
3. [Input Source Type Detection](#) based on D+/D- (bq25898D) or PSEL (bq25898) to set default Input Current Limit (IINLIM) register and input source type
4. Input Voltage Limit Threshold Setting (VINDPM threshold)
5. Converter Power-up

#### 9.2.3.1 Power Up REGN Regulation (LDO)

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to TS external resistors. The pull-up rail of STAT and PG can be connected to REGN as well. The REGN is enabled when all the below conditions are valid.

1. VBUS above  $V_{VBUS\_UVLOZ}$
2. VBUS above  $V_{BAT} + V_{SLEEPZ}$  in buck mode or VBUS below  $V_{BAT} + V_{SLEEP}$  in boost mode
3. After 220 ms delay is completed

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than  $I_{VBUS\_HIZ}$  from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

#### 9.2.3.2 Poor Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to start the buck converter.

1. VBUS voltage below  $V_{ACOV}$
2. VBUS voltage above  $V_{VBUSMIN}$  when pulling  $I_{BADSRC}$  (typical 30mA)

Once the input source passes all the conditions above, the status register bit VBUS\_GD is set high and the INT pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

#### 9.2.3.3 Input Source Type Detection

After the VBUS\_GD bit is set and REGN LDO is powered, the charger device runs [Input Source Type Detection](#) when AUTO\_DPDM\_EN bit is set.

## Feature Description (continued)

The bq25898D follows the USB Battery Charging Specification 1.2 (BC1.2) and to detect input source (SDP/CDP/DCP) and non-standard adapter through USB D+/D- lines. In addition, when USB DCP is detected, it initiates adjustable high voltage adapter handshake on D+/D-. The device supports MaxCharge™ handshake when MAXC\_EN or HVDCP\_EN is set. The bq25898 sets input current limit through PSEL and OTG pins.

After input source type detection, an INT pulse is asserted to the host. In addition, the following registers and pin are changed:

1. Input Current Limit (IINLIM) register is changed to set current limit
2. PG\_STAT bit is set
3.  $\overline{\text{PG}}$  pin goes low (bq25898)

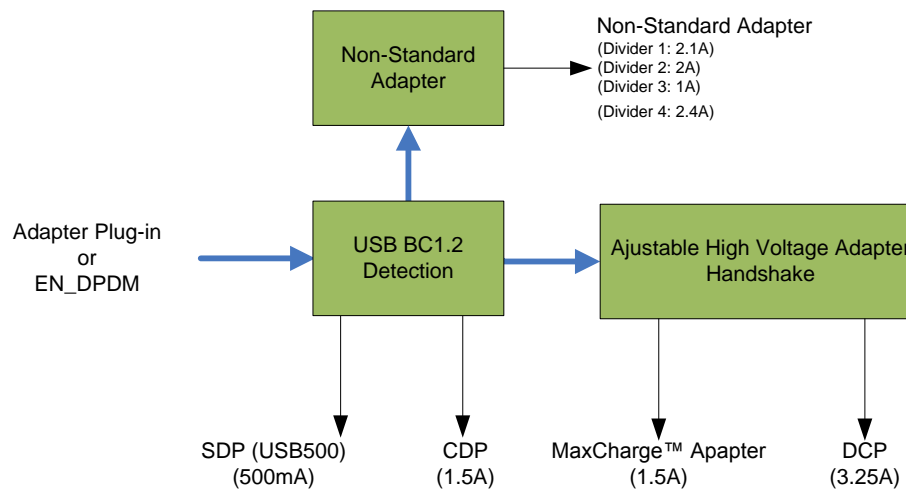
The host can over-write IINLIM register to change the input current limit if needed. The charger input current is always limited by the lower of IINLIM register or ILIM pin at all-time regardless of Input Current Optimizer (ICO) is enable or disabled.

When AUTO\_DPDM\_EN is disabled, the [Input Source Type Detection](#) is bypassed. The Input Current Limit (IINLIM) register, VBUS\_STAT, and SPD\_STAT bits are unchanged from previous values.

### 9.2.3.3.1 D+/D- Detection Sets Input Current Limit (bq25898D)

The bq25898D contains a D+/D- based input source detection to set the input current limit automatically. The D+/D- detection includes standard USB BC1.2, non-standard adapter, and adjustable high voltage adapter detections. When input source is plugged-in, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer of 500ms is expired, the non-standard adapter detection is applied to set the input current limit.

When DCP is detected, the device initiates adjustable high voltage adapter handshake including MaxCharge™, etc. The handshake connects combinations of voltage source(s) and/or current sink on D+/D- to signal input source to raise output voltage from 5 V to 9 V / 12 V. The adjustable high voltage adapter handshake can be disabled by clearing MAXC\_EN and/or HVDCP\_EN bits .



**Figure 11. USB D+/D- Detection**

**Table 1. Non-Standard Adapter Detection**

NON-STANDARD ADAPTER	D+ THRESHOLD	D- THRESHOLD	INPUT CURRENT LIMIT
Divider 1	$V_{D+}$ within $V_{2P7\_VTH}$	$V_{D-}$ within $V_{2P0\_VTH}$	2.1A
Divider 2	$V_{D+}$ within $V_{1P2\_VTH}$	$V_{D-}$ within $V_{1P2\_VTH}$	2A
Divider 3	$V_{D+}$ within $V_{2P0\_VTH}$	$V_{D-}$ within $V_{2P7\_VTH}$	1A
Divider 4	$V_{D+}$ within $V_{2P7\_VTH}$	$V_{D-}$ within $V_{2P7\_VTH}$	2.4A

**Table 2. Adjustable High Voltage Adapter D+/D- Output Configurations**

ADJUSTABLE HIGH VOLTAGE HANDSHAKE	D+	D-	OUTPUT
MaxCharge (12V)	$I_{1P6MA\_ISINK}$	$V_{3p45\_VSR}$	12 V
MaxCharge (9V)	$V_{3p45\_VSR}$	$I_{1P6MA\_ISINK}$	9 V

After the [Input Source Type Detection](#) is done, an INT pulse is asserted to the host. In addition, the following registers including Input Current Limit register (IINLIM), VBUS\_STAT, and SDP\_STAT are updated as below:

**Table 3. bq25898D Result**

D+/D- DETECTION	INPUT CURRENT LIMIT (IINLIM)	SDP_STAT	VBUS_STAT
USB SDP (USB500)	500 mA	1	001
USB CDP	1.5 A	1	010
USB DCP	3.25 A	1	011
Divider 3	1 A	1	110
Divider 1	2.1 A	1	110
Divider 4	2.4 A	1	110
Divider 2	2 A	1	110
MaxCharge	1.5 A	1	100
Unknown Adapter	500 mA	1	101

#### 9.2.3.3.2 PSEL Pin Sets Input Current Limit (bq25898)

The bq25898 has PSEL interface for input current limit setting to interface with USB PHY. It directly takes the USB PHY device output to decide whether the input is USB host or charging port. To implement USB100 in the system, the host can enter HiZ mode by setting EN\_HIZ bit after 2 min charging with 500 mA input current limit.

**Table 4. bq25898 Result**

INPUT DETECTION	BAT VOLTAGE	PSEL PIN	INPUT CURRENT LIMIT (IINLIM)	SDP_STAT	VBUS_STAT
USB SDP (USB500)	X	High	500 mA	1	001
Adapter	X	Low	3.25 A	1	010

#### 9.2.3.3.3 Force Input Current Limit Detection

In host mode, the host can force the device to run by setting FORCE\_DPDM bit. After the detection is completed, FORCE\_DPDM bit returns to 0 by itself and Input Result is updated.

#### 9.2.3.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9 V – 14 V) for high voltage charging and provides two methods to set Input Voltage Limit (VINDPM) threshold to facilitate autonomous detection.

##### 1. Absolute VINDPM (FORCE\_VINDPM=1)

By setting FORCE\_VINDPM bit to 1, the VINDPM threshold setting algorithm is disabled. Register VINDPM is writable and allows host to set the absolute threshold of VINDPM function.

##### 2. Relative VINDPM based on VINDPM\_OS registers (FORCE\_VINDPM=0) (Default)

When FORCE\_VINDPM bit is 0 (default), the VINDPM threshold setting algorithm is enabled. The VINDPM register is read only and the charger controls the register by using VINDPM Threshold setting algorithm. The algorithm allows a wide range of adapter ( $V_{VBUS\_OP}$ ) to be used with flexible VINDPM threshold.

After Input Voltage Limit Threshold is set, an INT pulse is generated to signal to the host.

### 9.2.3.5 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current limit is forced to the lower of 200 mA or IINLIM register setting. After the system rises above 2.2 V, the device limits input current to the lower value of ILIM pin and IILIM register (ICO\_EN = 0) or IDPM\_LIM register (ICO\_EN = 1).

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

### 9.2.4 Input Current Optimizer (ICO)

The device provides innovative Input Current Optimizer (ICO) to identify maximum power point without overload the input source. The algorithm automatically identify maximum input current limit of power source without entering VINDPM to avoid input source overload.

This feature is enabled by default (ICO\_EN=1) and can be disabled by setting ICO\_EN bit to 0. After DCP or MaxCharge type input source is detected based on the procedures previously described ([Input Source Type Detection](#)). The algorithm runs automatically when ICO\_EN bit is set. The algorithm can also be forced to execute by setting FORCE\_ICO bit regardless of input source type detected.

The actual input current limit used by the [Dynamic Power Management](#) is reported in IDPM\_LIM register while Input Current Optimizer is enabled (ICO\_EN = 1) or set by IINLIM register when the algorithm is disabled (ICO\_EN = 0). In addition, the current limit is clamped by ILIM pin unless EN\_ILIM bit is 0 to disable ILIM pin function.

### 9.2.5 Boost Mode Operation from Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500 mA (BOOST\_LIM bits = 000) output requirement. The maximum output current is up to 2.4 A. The boost operation can be enabled if the conditions are valid:

1. BAT above  $BAT_{LOWV}$
2. VBUS less than  $BAT + V_{SLEEP}$  (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH and OTG\_CONFIG bit =1)
4. Voltage at TS (thermistor) pin is within range configured by Boost Mode Temperature Monitor as configured by BHOT and BCOLD bits
5. After 30 ms delay from boost mode enable

In boost mode, the device employs a 500 KHz or 1.5 MHz (selectable using BOOST\_FREQ bit) step-up switching regulator based on system requirements. To avoid frequency change during boost mode operations, write to boost frequency configuration bit (BOOST\_FREQ) is ignored when OTG\_CONFIG is set.

During boost mode, the status register VBUS\_STAT bits is set to 111, the VBUS output is 5V by default (selectable via BOOSTV register bits) and the output current can reach up to 2.4 A, selected via I<sup>2</sup>C (BOOST\_LIM bits). The boost output is maintained when BAT is above  $V_{OTG\_BAT}$  threshold.

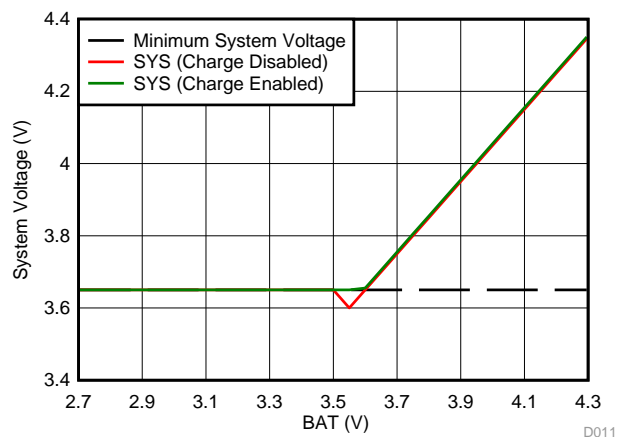
## 9.2.6 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

### 9.2.6.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS\_MIN bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5 V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the  $V_{DS}$  of BATFET. The status register VSYS\_STAT bit goes high when the system is in minimum system voltage regulation.



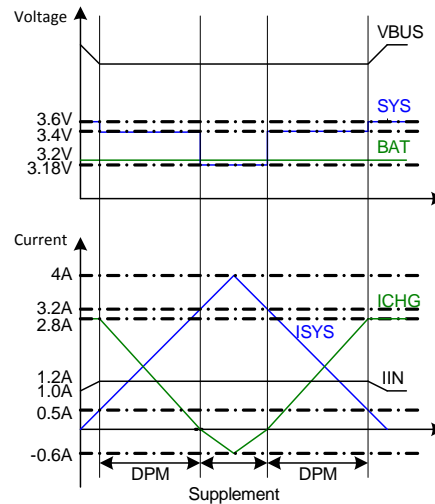
**Figure 12. V(SYS) vs V(BAT)**

### 9.2.6.2 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IINLIM or IDPM\_LIM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the [Supplement Mode](#) where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

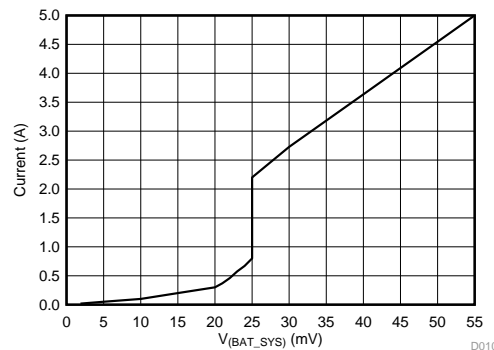
During DPM mode, the status register bits VDPM\_STAT (VINDPM) and/or IDPM\_STAT (IINDPM) is/are set high. [Figure 13](#) shows the DPM response with 9V/1.2A adapter, 3.2-V battery, 2.8-A charge current and 3.4-V minimum system voltage setting.



**Figure 13. DPM Response**

### 9.2.6.3 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET VDS stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the [Supplement Mode](#). As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce  $R_{DS(ON)}$  until the BATFET is in full conduction. At this point onwards, the BATFET VDS linearly increases with discharge current. [Figure 14](#) shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit [Supplement Mode](#) when the battery is below battery depletion threshold.



**Figure 14. BATFET V-I Curve**

## 9.2.7 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 4-A charge current for high capacity battery. The 5-m $\Omega$  BATFET improves charging efficiency and minimize the voltage drop during discharging.

### 9.2.7.1 Autonomous Charging Cycle

With battery charging enabled (CHG\_CONFIG bit = 1 and  $\overline{CE}$  pin is low), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in [Table 5](#). The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I<sup>2</sup>C.

**Table 5. Charging Parameter Default Setting**

DEFAULT MODE	bq25898D	bq25898
Charging Voltage	4.208 V	4.208 V
Charging Current	2.048 A	2.048 A
Pre-charge Current	128 mA	128 mA
Termination Current	256 mA	256 mA
Temperature Profile	JEITA	JEITA
Safety Timer	12 hour	12 hour

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by setting CHG\_CONFIG bit, /CE pin is low and ICHG register is not 0 mA
- No thermistor fault on TS pin
- No safety timer fault
- BATFET is not forced to turn off (BATFET\_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device not in DPM mode or thermal regulation. When a full battery voltage is discharged below recharge threshold (threshold selectable via VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, either toggle CE pin or CHG\_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting STAT\_DIS bit. In addition, the status register (CHRG\_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

#### 9.2.7.2 Battery Charging Profile

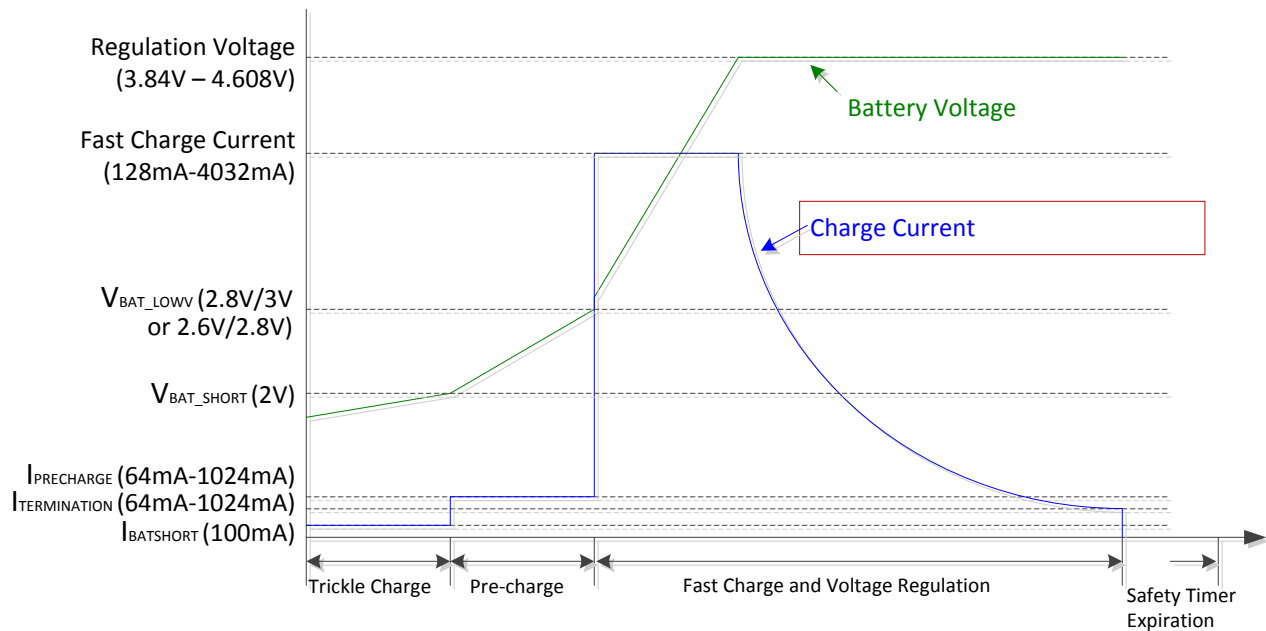
The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and regulates current / voltage.

**Table 6. Charging Current Setting**

VBAT	CHARGING CURRENT	REG DEFAULT SETTING	CHRG_STAT
< 2 V	I <sub>BATSHORT</sub>	–	01
2 V – 3 V	I <sub>PRECHG</sub>	0 mA (precharge disabled)	01
> 3 V	I <sub>CHG</sub>	2048 mA	10



If the charger device is in DPM regulation or thermal regulation during charging, the charging current can be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.



**Figure 15. Battery Charging Profile**

### 9.2.7.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage [Supplement Mode](#).

When termination occurs, the status register CHRG\_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN\_TERM bit prior to charge termination.

### 9.2.7.4 Resistance Compensation (IRCOMP)

For high current charging system, resistance between charger output and battery cell terminal such as board routing, connector, MOSFETs and sense resistor can force the charging process to move from constant current to constant voltage too early and increase charge time. To speed up the charging cycle, the device provides resistance compensation (IRCOMP) feature which can extend the constant current charge time to delivery maximum power to battery.

The device allows the host to compensate for the resistance by increasing the voltage regulation set point based on actual charge current and the resistance as shown below. For safe operation, the host should set the maximum allowed regulation voltage register ( $V_{CLAMP}$ ) and the minimum resistance compensation (BATCOMP).

$$V_{REG\_ACTUAL} = V_{REG} + \min(I_{CHRG\_ACTUAL} \times BATCOMP, V_{CLAMP}) \quad (1)$$

### 9.2.7.5 Thermistor Qualification

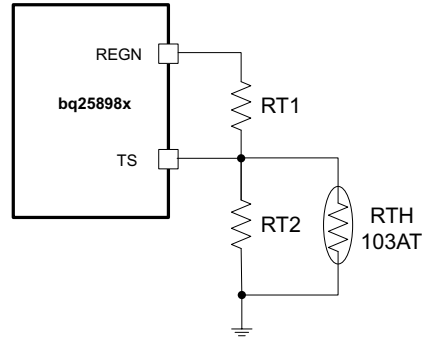
#### 9.2.7.5.1 JEITA Guideline Compliance in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

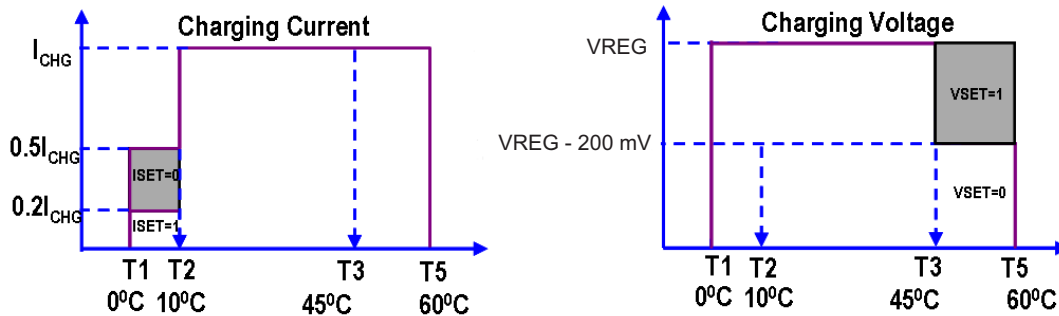


The device continuously monitors battery temperature by measuring the voltage between the TS pins and ground, typically determined by a negative temperature coefficient thermistor (NTC) and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the voltage on TS pin must be within the  $V_{T1}$  to  $V_{T5}$  thresholds. If TS voltage exceeds the T1–T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range. At cool temperature (T1–T2), JEITA recommends the charge current to be reduced to at least half of the charge current or lower. At warm temperature (T3–T5), JEITA recommends charge voltage below nominal charge voltage.

The device provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3–T5) can be 200 mV below charge voltage (JEITA\_VSET=0). The current setting at cool temperature (T1–T2) can be further reduced to 20% or 50% of fast charge current (JEITA\_ISET bit).



**Figure 16. TS Resistor Network**



**Figure 17. Charging Values**

Assuming a 103AT NTC thermistor on the battery pack as shown in [Figure 16](#), the value RT1 and RT2 can be determined by using [Equation 2](#):

$$RT2 = \frac{V_{VREGN} \times RTH_{COLD} \times RTH_{HOT} \times \left( \frac{1}{VT1} - \frac{1}{VT5} \right)}{RTH_{HOT} \times \left( \frac{V_{VREGN}}{VT5} - 1 \right) - RTH_{COLD} \times \left( \frac{V_{VREGN}}{VT1} - 1 \right)}$$

$$RT1 = \frac{\frac{V_{VREGN}}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

(2)

Select 0°C to 60°C range for Li-ion or Li-polymer battery,

$RTH_{T1} = 27.28 \text{ k}\Omega$

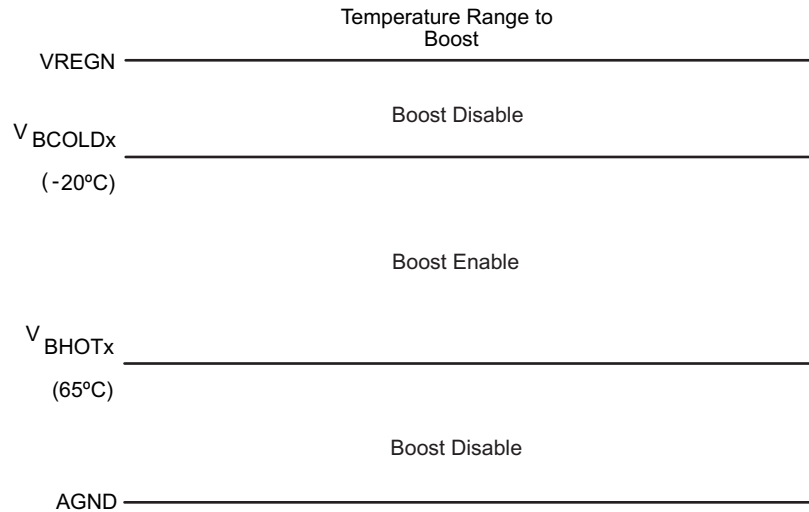
$RTH_{T5} = 3.02 \text{ k}\Omega$

$RT1 = 5.24 \text{ k}\Omega$ 
 $RT2 = 30.31 \text{ k}\Omega$ 

During JEITA cool, the bq25898x terminates when the charge current has reached 20% or 50% of termination current setting, depending on the JT\_IREDUCE bit. During JEITA warm, the bq25898x terminates when the charge current reaches the termination current setting.

#### 9.2.7.5.2 Cold/Hot Temperature Window in Boost Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the  $V_{BCOLD1}$  to  $V_{BHOT2}$  thresholds unless boost mode temperature is disabled by setting BHOT bits to 11. When temperature is outside of the temperature thresholds, the boost mode is suspended. Once temperature is within thresholds, the boost mode is recovered.



**Figure 18. TS Pin Thermistor Sense Thresholds in Boost Mode**

#### 9.2.7.6 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 4 hours when the battery is below  $V_{BATLOWV}$  threshold. The user can program fast charge safety timer through I<sup>2</sup>C (CHG\_TIMER bits). When safety timer expires, the fault register CHRG\_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled via I2C by setting EN\_TIMER bit.

During input voltage, current or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM\_STAT = 1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X\_EN bit.

#### 9.2.8 Battery Monitor

The device includes a battery monitor to provide measurements of VBUS voltage, battery voltage, system voltage, thermistor ratio, and charging current, and charging current based on the device's modes of operation. The measurements are reported in Battery Monitor Registers (REG0E-REG12). The battery monitor can be configured as two conversion modes by using CONV\_RATE bit: one-shot conversion (default) and 1 second continuous conversion.

For one-shot conversion (CONV\_RATE = 0), the CONV\_START bit can be set to start the conversion. During the conversion, the CONV\_START is set and it is cleared by the device when conversion is completed. The conversion result is ready after  $t_{CONV}$  (maximum 1 second).

For continuous conversion (CONV\_RATE = 1), the CONV\_RATE bit can be set to initiate the conversion. During active conversion, the CONV\_START is set to indicate conversion is in progress. The battery monitor provides conversion result every 1 second automatically. The battery monitor exits continuous conversion mode when CONV\_RATE is cleared.

When battery monitor is active, the REGN power is enabled and can increase device quiescent current.

**Table 7. Battery Monitor Modes of Operation**

PARAMETER	REGISTER	MODES OF OPERATION			
		CHARGE MODE	BOOST MODE	DISABLE CHARGE MODE	BATTERY ONLY MODE
Battery Voltage ( $V_{BAT}$ )	REG0E	Yes	Yes	Yes	Yes
System Voltage ( $V_{SYS}$ )	REG0F	Yes	Yes	Yes	Yes
Temperature (TS) Voltage ( $V_{TS}$ )	REG10	Yes	Yes	Yes	Yes
VBUS Voltage ( $V_{VBUS}$ )	REG11	Yes	Yes	Yes	NA
Charge Current ( $I_{BAT}$ )	REG12	Yes	NA	NA	NA

## 9.2.9 Status Outputs ( $\overline{PG}$ , STAT, and INT)

### 9.2.9.1 Power Good Indicator ( $\overline{PG}$ )

In bq25898, the  $\overline{PG}$  goes LOW to indicate a good input source when:

1. VBUS above  $V_{VBUS\_UVLO}$
2. VBUS above battery (not in sleep)
3. VBUS below  $V_{ACOV}$  threshold
4. VBUS above  $V_{VBUSMIN}$  (typical 3.8 V) when  $I_{BADSRC}$  (typical 30 mA) current is applied (not a poor source)
5. Completed [Input Source Type Detection](#)

### 9.2.9.2 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED as shown in [Figure 49](#). The STAT pin function can be disable by setting STAT\_DIS bit.

**Table 8. STAT Pin State**

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input overvoltage, TS fault, timer fault, input or system overvoltage) Boost Mode suspend (due to TS Fault)	blinking at 1 Hz

### 9.2.9.3 Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 256- $\mu$ s INT pulse.

- USB/adaptor source identified (through PSEL or DPDM detection, with OTG pin)
- Good input source detected
  - VBUS above battery (not in sleep)
  - VBUS below  $V_{ACOV}$  threshold
  - VBUS above  $V_{VBUSMIN}$  (typical 3.8 V) when  $I_{BADSRC}$  (typical 30 mA) current is applied (not a poor source)
- Input removed
- Charge Complete
- Any FAULT event in REG0C

When a fault occurs, the charger device sends out INT and keeps the fault state in REG0C until the host reads the fault register. Before the host reads REG0C and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG0C two times consecutively. The 1<sup>st</sup> read reports the pre-existing fault register status and the 2<sup>nd</sup> read reports the current fault register status.

## 9.2.10 BATFET (Q4) Control

### 9.2.10.1 BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set BATFET\_DIS bit, the charger can turn off BATFET immediately or delay by  $t_{SM\_DLY}$  as configured by BATFET\_DLY bit.

### 9.2.10.2 BATFET Enable (Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET\_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. Clear BATFET\_DIS bit
3. Set REG\_RST bit to reset all registers including BATFET\_DIS bit to default (0)
4. A logic high to low transition on  $\overline{QON}$  pin with  $t_{SHIPMODE}$  deglitch time to enable BATFET to exit shipping mode

### 9.2.10.3 BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged-in. By changing the state of BATFET from off to on, system connects to SYS can be effectively have a power-on-reset. The  $\overline{QON}$  pin supports push-button interface to reset system power without host by change the state of BATFET.

When the  $\overline{QON}$  pin is driven to logic low for  $t_{QON\_RST}$  (typical 15 seconds) while input source is not plugged in and BATFET is enabled (BATFET\_DIS=0), the BATFET is turned off for  $t_{BATFET\_RST}$  and then it is re-enabled to reset system power. This function can be disabled by setting BATFET\_RST\_EN bit to 0.

## 9.2.11 Current Pulse Control Protocol

The device provides the control to generate the VBUS current pulse protocol to communicate with adjustable high voltage adapter in order to signal adapter to increase or decrease output voltage. To enable the interface, the EN\_PUMPX bit must be set. Then the host can select the increase/decrease voltage pulse by setting one of the PUMPX\_UP or PUMPX\_DN bit (but not both) to start the VBUS current pulse sequence. During the current pulse sequence, the PUMPX\_UP and PUMPX\_DN bits are set to indicate pulse sequence is in progress and the device pulses the input current limit between current limit set forth by IINLIM or IDPM\_LIM register and the 100mA current limit ( $I_{INDPM100\_ACC}$ ). When the pulse sequence is completed, the input current limit is returned to value set by IINLIM or IDPM\_LIM register and the PUMPX\_UP or PUMPX\_DN bit is cleared. In addition, the EN\_PUMPX can be cleared during the current pulse sequence to terminate the sequence and force charger to return to input current limit as set forth by the IINLIM or IDPM\_LIM register immediately. When EN\_PUMPX bit is low, write to PUMPX\_UP and PUMPX\_DN bit would be ignored and have no effect on VBUS current limit.

## 9.2.12 Input Current Limit on ILIM

For safe operation, the device has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{NMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

The actual input current limit is the lower value between ILIM setting and register setting (IINLIM). For example, if the register setting is 111111 for 3.25 A, and ILIM has a 232- $\Omega$  resistor ( $K_{ILIM} = 350$  max.) to ground for 1.5 A, the input current limit is 1.5 A. ILIM pin can be used to set the input current limit rather than the register settings when EN\_ILIM bit is set. The device regulates ILIM pin at 0.8 V. If ILIM voltage exceeds 0.8 V, the device enters input current regulation (Refer to [Dynamic Power Management](#) section).

The ILIM pin can also be used to monitor input current when EN\_ILIM is enabled. The voltage on ILIM pin is proportional to the input current. ILIM pin can be used to monitor the input current following [Equation 4](#):

$$I_N = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8 \text{ V}} \quad (4)$$

For example, if ILIM pin is set with 260-Ω resistor, and the ILIM voltage is 0.4 V, the actual input current 0.557 A - 0.67 A (based on KILM specified). If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 0.8 V. If ILIM pin is short, the input current limit is set by the register.

The ILIM pin function can be disabled by setting EN\_ILIM bit to 0. When the pin is disabled, both input current limit function and monitoring function are not available.

## 9.2.13 Thermal Regulation and Thermal Shutdown

### 9.2.13.1 Thermal Protection in Buck Mode

The device monitors the internal junction temperature  $T_J$  to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds the preset thermal regulation limit (TREG bits), the device lowers down the charge current. The wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM\_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds  $T_{SHUT}$ . The fault register CHRG\_FAULT is set to 10 and an INT is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is below  $T_{SHUT\_HYS}$ .

#### 9.2.13.1.1 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC surface temperature exceeds  $T_{SHUT}$ , the boost mode is disabled (converter is turned off) by setting OTG\_CONFIG bit low and BATFET is turned off. When IC surface temperature is below  $T_{SHUT\_HYS}$ , the BATFET is enabled automatically to allow system to restore and the host can re-enable OTG\_CONFIG bit to recover.

## 9.2.14 Voltage and Current Monitoring in Buck and Boost Mode

### 9.2.14.1 Voltage and Current Monitoring in Buck Mode

The device closely monitors the input and system voltage, as well as HSFET current for safe buck and boost mode operations.

#### 9.2.14.1.1 Input Overvoltage (ACOV)

The input voltage for buck mode operation is  $V_{VBUS\_OP}$ . If VBUS voltage exceeds  $V_{ACOV}$ , the device stops switching immediately. During input over voltage (ACOV), the fault register CHRG\_FAULT bits sets to 01. An INT is asserted to the host.

#### 9.2.14.1.2 System Overvoltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. When SYSOVP is detected, the converter stops immediately to clamp the overshoot.

### 9.2.14.2 Voltage and Current Monitoring in Boost Mode

The device closely monitors the VBUS voltage, as well as RBFET and LSFET current to ensure safe boost mode operation.

#### 9.2.14.2.1 VBUS Overcurrent Protection

The charger device closely monitors the RBFET (Q1), and LSFET (Q3) current to ensure safe boost mode operation. During overcurrent condition when output current exceed ( $I_{OTG\_OCP}$ ) the device operates in hiccup mode for protection. While in hiccup mode cycle, the device turns off RBFET for  $t_{OTG\_OCP\_OFF}$  (30 ms typical) and turns on RBFET for  $t_{OTG\_OCP\_ON}$  (250 μs typical) in an attempt to restart. If the overcurrent condition is removed, the boost converter returns to normal operation. When overcurrent condition continues to exist, the device repeats the hiccup cycle until overcurrent condition is removed. When overcurrent condition is detected the fault register bit BOOST\_FAULT is set high to indicate fault in boost operation. An INT is also asserted to the host.

### 9.2.14.2.2 Boost Mode Overvoltage Protection

When the VBUS voltage rises above regulation target and exceeds  $V_{OTG\_OVP}$ , the device enters overvoltage protection which stops switching, clears OTG\_CONFIG bit and exits boost mode. During the overvoltage duration, the fault register bit (BOOST\_FAULT) is set high to indicate fault in boost operation. An INT is also asserted to the host.

## 9.2.15 Battery Protection

### 9.2.15.1 Battery Overvoltage Protection (BATOVF)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register BAT\_FAULT bit goes high and an INT is asserted to the host.

### 9.2.15.2 Battery Over-Discharge Protection

When battery is discharged below  $V_{BAT\_DPL}$ , the BATFET is turned off to protect battery from over discharge. To recover from over-discharge, an input source is required at VBUS. When an input source is plugged in, the BATFET turns on. The battery is charged with  $I_{BATSHORT}$  (typically 100 mA) current when the  $V_{BAT} < V_{SHORT}$ , or precharge current as set in IPRECHG register when the battery voltage is between  $V_{SHORT}$  and  $V_{BATLOWV}$ .

### 9.2.15.3 System Overcurrent Protection

When the system is shorted or significantly overloaded ( $I_{BAT} > I_{BATOP}$ ) so that its current exceeds the overcurrent limit, the device latches off BATFET. Section [BATFET Enable \(Exit Shipping Mode\)](#) can reset the latch-off condition and turn on BATFET.

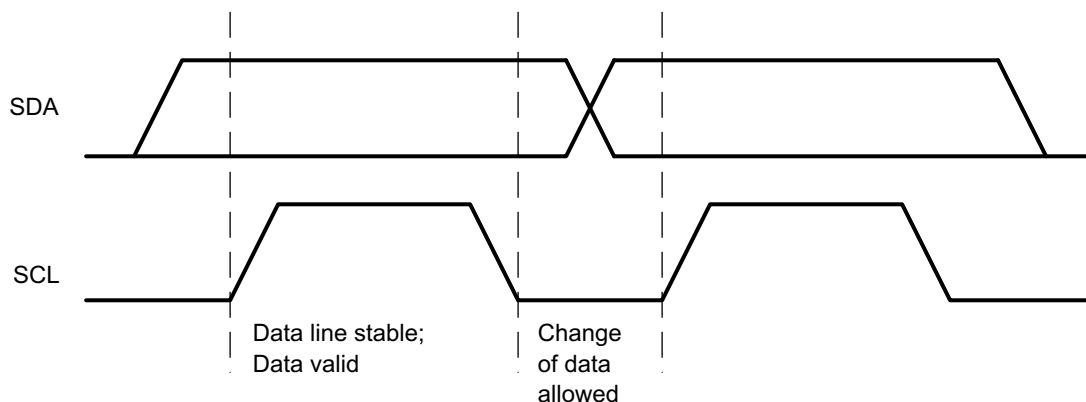
## 9.2.16 Serial Interface

The device uses I<sup>2</sup>C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I<sup>2</sup>C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG14. Register read beyond REG14 (0x14) returns 0xFF. The I<sup>2</sup>C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

### 9.2.16.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

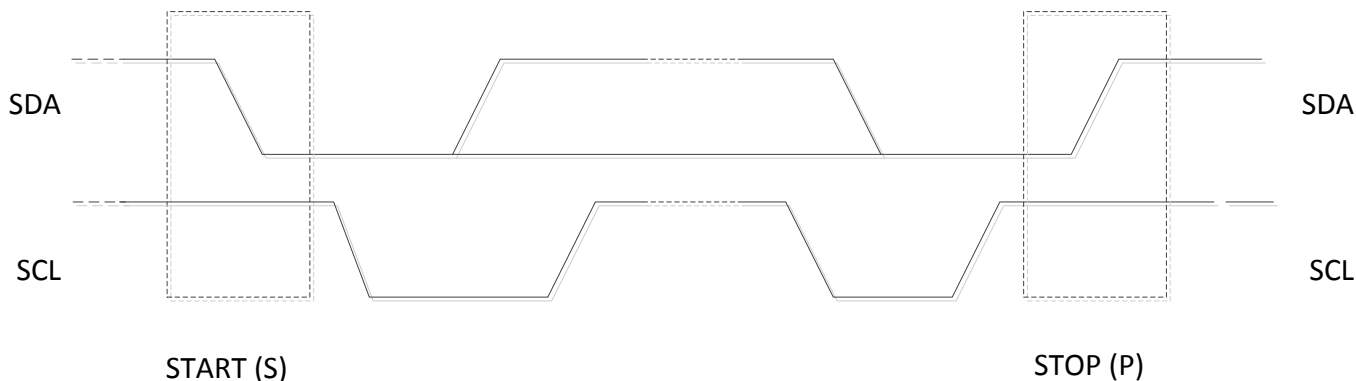


**Figure 19. Bit Transfer on the I<sup>2</sup>C Bus**

### 9.2.16.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

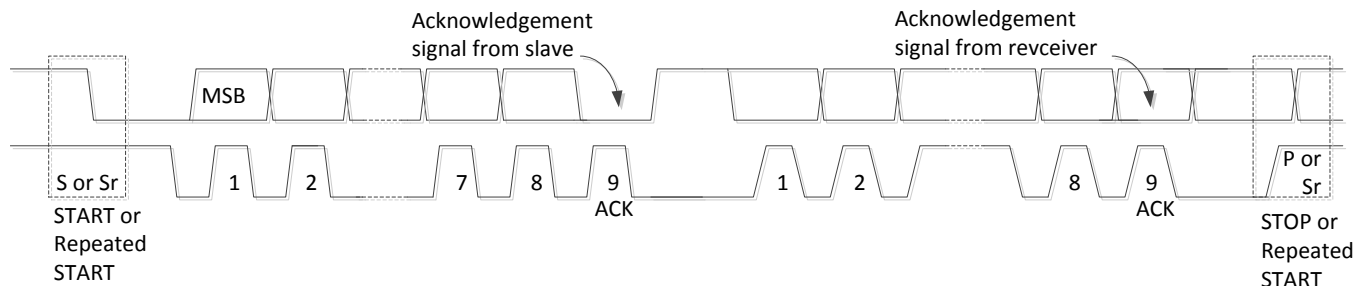
START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.



**Figure 20. START and STOP conditions**

### 9.2.16.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.



**Figure 21. Data Transfer on the I<sup>2</sup>C Bus**

### 9.2.16.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9<sup>th</sup> clock pulse, are generated by the master.

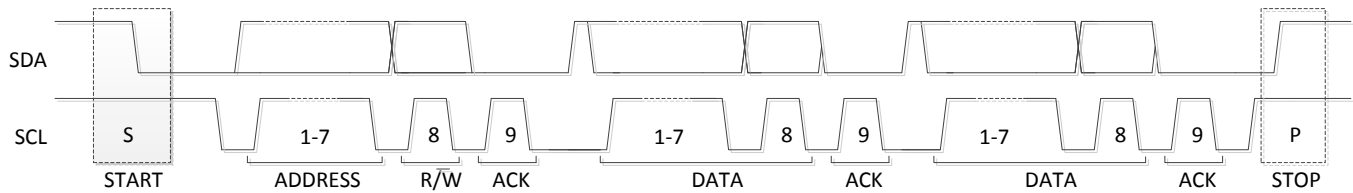
The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9<sup>th</sup> clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

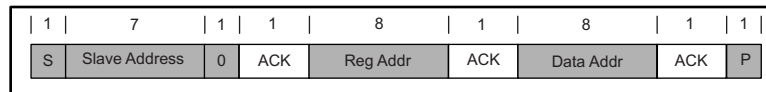
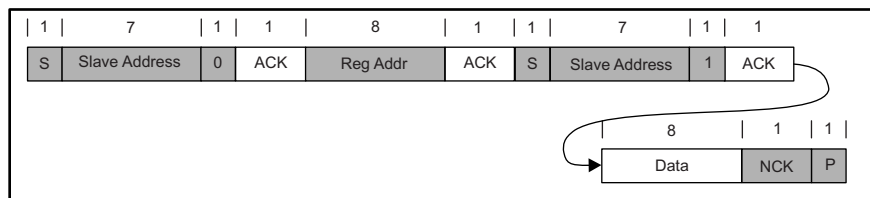
### 9.2.16.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).




**Figure 22. Complete Data Transfer**

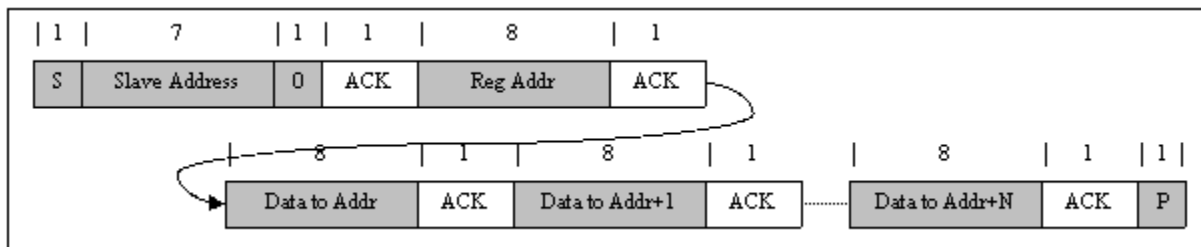
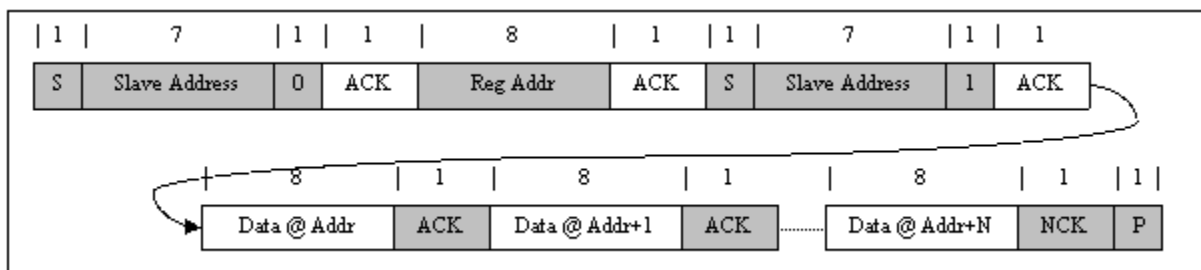
### 9.2.16.6 Single Read and Write


**Figure 23. Single Write**

**Figure 24. Single Read**

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

### 9.2.16.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG14 except REG0C.


**Figure 25. Multi-Write**

**Figure 26. Multi-Read**



REG0C is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG0C reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG0C for the second time. The only exception is NTC\_FAULT which always reports the actual condition on the TS pin. In addition, REG0C does not support multi-read and multi-write.

## 9.3 Device Functional Modes

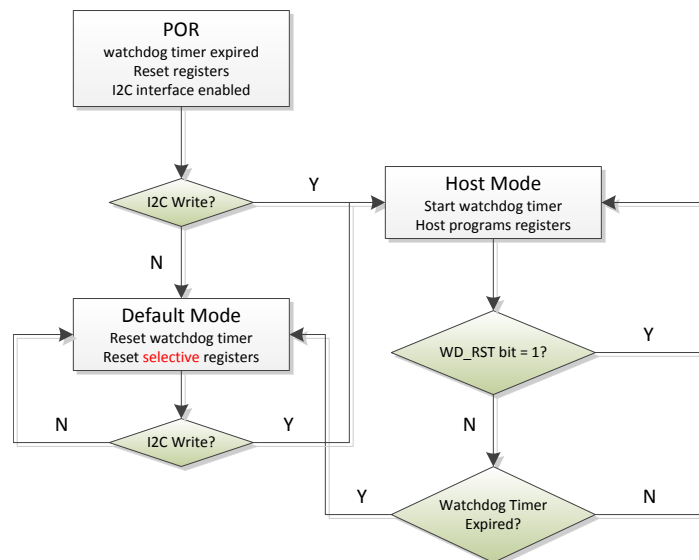
### 9.3.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG\_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG\_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

In default mode, the device keeps charging the battery with 12-hour fast charging safety timer. At the end of the 12-hour, the charging is stopped and the buck converter continues to operate to supply system load. Any write command to device transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD\_RST bit before the watchdog timer expires (WATCHDOG\_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits=00.

When the watchdog timer (WATCHDOG\_FAULT bit = 1) is expired, the device returns to default mode and all registers are reset to default values except IINLIM, VINDPM, VINDPM\_OS, BATFET\_RST\_EN, BATFET\_DLY, and BATFET\_DIS bits.



**Figure 27. Watchdog Timer Flow Chart**

**bq25898, bq25898D**

SLUSCA6B – MARCH 2016 – REVISED MARCH 2017

[www.ti.com](http://www.ti.com)

## 9.4 Register Map

I2C Slave Address: 6AH (1101010B +  $\overline{R/\overline{W}}$ ) (bq25898D)

I2C Slave Address: 6BH (1101011B +  $\overline{R/\overline{W}}$ ) (bq25898)

### 9.4.1 REG00

**Figure 28. REG00**

7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9. REG00**

Bit	Field	Type	Reset	Description
7	EN_HIZ	R/W	by REG_RST by Watchdog	Enable HIZ Mode 0 – Disable (default) 1 – Enable
6	EN_ILIM	R/W	by REG_RST by Watchdog	Enable ILIM Pin 0 – Disable 1 – Enable (default: Enable ILIM pin (1))
5	IINLIM[5]	R/W	by REG_RST	Input Current Limit bq25898D USB Host SDP = 500mA USB CDP = 1.5A USB DCP = 3.25A Adjustable High Voltage (MaxCharge) DCP = 1.5A Unknown Adapter = 500mA Non-Standard Adapter = 1A/2A/2.1A/2.4A bq25898 PSEL= Hi (USB500) = 500mA PSEL= Lo = 3.25A
4	IINLIM[4]	R/W	by REG_RST	
3	IINLIM[3]	R/W	by REG_RST	
2	IINLIM[2]	R/W	by REG_RST	
1	IINLIM[1]	R/W	by REG_RST	
0	IINLIM[0]	R/W	by REG_RST	

## 9.4.2 REG01

**Figure 29. REG01**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 10. REG01**

Bit	Field	Type	Reset	Description
7	DPLUS_DAC[2]	R/W	by Software	D+ Output Driver (default 000) 000 – HiZ 001 – 0V 010 – 0.6V 011 – 1.2V 100 – 2.0V 101 – 2.7V 110 – 3.3V 111 – D+/D- Short (D+ and D- driver are disabled)
6	DPLUS_DAC[1]	R/W	by Software	
5	DPLUS_DAC[0]	R/W	by Software	
4	DPLUS_DAC[2]	R/W	by Software	
3	DPLUS_DAC[1]	R/W	by Software	D- Output Driver (default 000) 000 – HiZ 001 – 0V 010 – 0.6V 011 – 1.2V 100 – 2.0V 101 – 2.7V 110 or 111 – 3.3V
2	DPLUS_DAC[0]	R/W	by Software	
1	EN_12V	R/W	by Software	
0	VDPM_OS[0]	R/W	by Software	

### 9.4.3 REG02

**Figure 30. REG02**

7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 11. REG02**

Bit	Field	Type	Reset	Description
7	CONV_START	R/W	by REG_RST by Watchdog	ADC Conversion Start Control 0 – ADC conversion not active (default). 1 – Start ADC Conversion This bit is read-only when CONV_RATE = 1. The bit stays high during ADC conversion and during input source detection.
6	CONV_RATE	R/W	by REG_RST by Watchdog	ADC Conversion Rate Selection 0 – One shot ADC conversion (default) 1 – Start 1s Continuous Conversion
5	BOOST_FREQ	R/W	by REG_RST by Watchdog	Boost Mode Frequency Selection 0 – 1.5MHz (default) 1 – 500KHz Note: Write to this bit is ignored when OTG_CONFIG is enabled.
4	ICO_EN	R/W	by REG_RST	Input Current Optimizer (ICO) Enable 0 – Disable ICO Algorithm 1 – Enable ICO Algorithm (default)
3	HVDCP_EN	R/W	by REG_RST	High Voltage DCP Enable (bq25898D only) 0 – Disable HVDCP handshake 1 – Enable HVDCP handshake (default)
2	MAXC_EN	R/W	by REG_RST	MaxCharge Adapter Enable (bq25898D only) 0 – Disable MaxCharge handshake 1 – Enable MaxCharge handshake (default)
1	FORCE_DPDM	R/W	by REG_RST by Watchdog	Force D+/D- Detection 0 – Not in D+/D- or PSEL detection (default) 1 – Force D+/D- detection
0	AUTO_DPDM_EN	R/W	by REG_RST	Automatic D+/D- Detection Enable 0 –Disable D+/D- or PSEL detection when VBUS is plugged-in 1 –Enable D+/D- or PEL detection when VBUS is plugged-in (default)

#### 9.4.4 REG03

**Figure 31. REG03**

7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 12. REG03**

Bit	Field	Type	Reset	Description
7	VOK_OTG_EN (bq25898 only)	R/W	by Software	0 – Disabled, VOK = 0 (default) 1 – Enabled, VOK = 1 1. Adapter Plug-in VOK_OTG_EN = x and VOK = 1 2. OTG if VOK_OTG_EN = 1 ≥ VOK = 1 if VOK_OTG_EN = 0 ≥ VOK = 0 3. Battery Only (non-OTG) VOK_OTG_EN = x and VOK = 0
	FORCE_DSEL (bq25898D only)	R/W	by Software	0 – Allow DSEL = 0 (default) 1 – Force DSEL = 1 1. Adaptor Plug-in DSEL = 1 when: 1) During AUTO_DPDM, FORCE_DPDM, DCP, HVDSP, MaxCharge and FORCE_DSEL = x or 2) Other input source and FORCE_DSEL = 1 DSEL = 0 when other input source and FORCE_DSEL = 0 2. OTG if FORCE_DSEL = 1 ≥ DSEL = 1 if FORCE_DSEL = 0 ≥ DSEL = 0 3. Battery only (non-OTG) DSEL = 0 and FORCE_DSEL = x
6	WD_RST	R/W	by Software by Watchdog	I2C Watchdog Timer Reset 0 – Normal (default) 1 – Reset (Back to 0 after timer reset)
<b>Charger Configuration</b>				
5	OTG_CONFIG	R/W	by REG_RST by Watchdog	Boost (OTG) Mode Configuration 0 – OTG Disable (default) 1 – OTG Enable
4	CHG_CONFIG	R/W	by REG_RST by Watchdog	Charge Enable Configuration 0 - Charge Disable 1- Charge Enable (default)
<b>Minimum System Voltage Limit</b>				
3	SYS_MIN[2]	R/W	by REG_RST	0.4V
2	SYS_MIN[1]	R/W	by REG_RST	0.2V
1	SYS_MIN[0]	R/W	by REG_RST	0.1V
0	MIN_VBAT_SEL	R/W	by REG_RST	0 – 2.9V BAT falling (default = 0) 1 – 2.5V BAT falling

### 9.4.5 REG04

**Figure 32. REG04**

7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 13. REG04**

Bit	Field	Type	Reset	Description
7	EN_PUMPX	R/W	by REG_RST by Watchdog	Current pulse control Enable 0 - Disable Current pulse control (default) 1- Enable Current pulse control (PUMPX_UP and PUMPX_DN)
6	ICHG[6]	R/W	by REG_RST by Watchdog	4096mA
5	ICHG[5]	R/W	by REG_RST by Watchdog	2048mA
4	ICHG[4]	R/W	by REG_RST by Watchdog	1024mA
3	ICHG[3]	R/W	by REG_RST by Watchdog	512mA
2	ICHG[2]	R/W	by REG_RST by Watchdog	256mA
1	ICHG[1]	R/W	by REG_RST by Watchdog	128mA
0	ICHG[0]	R/W	by REG_RST by Watchdog	64mA

## 9.4.6 REG05

**Figure 33. REG05**

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 14. REG05**

Bit	Field	Type	Reset	Description
7	IPRECHG[3]	R/W	by REG_RST by Watchdog	512mA
6	IPRECHG[2]	R/W	by REG_RST by Watchdog	256mA
5	IPRECHG[1]	R/W	by REG_RST by Watchdog	128mA
4	IPRECHG[0]	R/W	by REG_RST by Watchdog	64mA
3	ITERM[3]	R/W	by REG_RST by Watchdog	512mA
2	ITERM[2]	R/W	by REG_RST by Watchdog	256mA
1	ITERM[1]	R/W	by REG_RST by Watchdog	128mA
0	ITERM[0]	R/W	by REG_RST by Watchdog	64mA

## 9.4.7 REG06

**Figure 34. REG06**

7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 15. REG06**

Bit	Field	Type	Reset	Description
7	VREG[5]	R/W	by REG_RST by Watchdog	512mV
6	VREG[4]	R/W	by REG_RST by Watchdog	256mV
5	VREG[3]	R/W	by REG_RST by Watchdog	128mV
4	VREG[2]	R/W	by REG_RST by Watchdog	64mV
3	VREG[1]	R/W	by REG_RST by Watchdog	32mV
2	VREG[0]	R/W	by REG_RST by Watchdog	16mV
1	BATLOWV	R/W	by REG_RST by Watchdog	Battery Precharge to Fast Charge Threshold 0 – 2.8V 1 – 3.0V (default)
0	VRECHG	R/W	by REG_RST by Watchdog	Battery Recharge Threshold Offset (below Charge Voltage Limit) 0 – 100mV ( $V_{RECHG}$ ) below VREG (REG06[7:2]) (default) 1 – 200mV ( $V_{RECHG}$ ) below VREG (REG06[7:2])



### 9.4.8 REG07

**Figure 35. REG07**

7	6	5	4	3	2	1	0
1	0	0	1	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 16. REG07**

Bit	Field	Type	Reset	Description
7	EN_TERM	R/W	by REG_RST by Watchdog	Charging Termination Enable 0 – Disable 1 – Enable (default)
6	STAT_DIS	R/W	by REG_RST by Watchdog	STAT Pin Disable 0 – Enable STAT pin function (default) 1 – Disable STAT pin function
5	WATCHDOG[1]	R/W	by REG_RST by Watchdog	I2C Watchdog Timer Setting 00 – Disable watchdog timer 01 – 40s (default) 10 – 80s 11 – 160s
4	WATCHDOG[0]	R/W	by REG_RST by Watchdog	
3	EN_TIMER	R/W	by REG_RST by Watchdog	Charging Safety Timer Enable 0 – Disable 1 – Enable (default)
2	CHG_TIMER[1]	R/W	by REG_RST by Watchdog	Fast Charge Timer Setting 00 – 5 hrs 01 – 8 hrs 10 – 12 hrs (default) 11 – 20 hrs
1	CHG_TIMER[0]	R/W	by REG_RST by Watchdog	
0	JEITA_ISET (0C-10C)	R/W	by REG_RST by Watchdog	JEITA Low Temperature Current Setting 0 – 50% of ICHG (REG04[6:0]) 1 – 20% of ICHG (REG04[6:0]) (default)

### 9.4.9 REG08

**Figure 36. REG08**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 17. REG08**

Bit	Field	Type	Reset	Description
7	BAT_COMP[2]	R/W	by REG_RST by Watchdog	80mΩ
6	BAT_COMP[1]	R/W	by REG_RST by Watchdog	40mΩ
5	BAT_COMP[0]	R/W	by REG_RST by Watchdog	20mΩ
4	VCLAMP[2]	R/W	by REG_RST by Watchdog	128mV
3	VCLAMP[1]	R/W	by REG_RST by Watchdog	64mV
2	VCLAMP[0]	R/W	by REG_RST by Watchdog	32mV
1	TREG[1]	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold 00 – 60°C 01 – 80°C
0	TREG[0]	R/W	by REG_RST by Watchdog	10 – 100°C 11 – 120°C (default)

## 9.4.10 REG09

**Figure 37. REG09**

7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 18. REG09**

Bit	Field	Type	Reset	Description
7	FORCE_ICO	R/W	by REG_RST by Watchdog	Force Start Input Current Optimizer (ICO) 0 – Do not force ICO (default) 1 – Force ICO Note: This bit is can only be set only and always returns to 0 after ICO starts
6	TMR2X_EN	R/W	by REG_RST by Watchdog	Safety Timer Setting during DPM or Thermal Regulation 0 – Safety timer not slowed by 2X during input DPM or thermal regulation 1 – Safety timer slowed by 2X during input DPM or thermal regulation (default)
5	BATFET_DIS	R/W	by REG_RST	Force BATFET off to enable ship mode with $t_{SM\_DLY}$ delay time 0 – Allow BATFET turn on (default) 1 – Force BATFET off
4	JEITA_VSET (45C-60C)	R/W	by REG_RST by Watchdog	JEITA High Temperature Voltage Setting 0 – Set Charge Voltage to VREG-200mV during JEITA hig temperature (default) 1 – Set Charge Voltage to VREG during JEITA high temperature
3	BATFET_DLY	R/W	by REG_RST	BATFET turn off delay control 0 – BATFET turn off immediately when BATFET_DIS bit is set (default) 1 – BATFET turn off delay by $t_{SM\_DLY}$ when BATFET_DIS bit is set
2	BATFET_RST_EN	R/W	by REG_RST	BATFET full system reset enable 0 – Disable BATFET full system reset 1 – Enable BATFET full system reset (default)
1	PUMPX_UP	R/W	by REG_RST by Watchdog	Current pulse control voltage up enable 0 – Disable (default) 1 – Enable Note: This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed
0	PUMPX_DN	R/W	by REG_RST by Watchdog	Current pulse control voltage down enable 0 – Disable (default) 1 – Enable Note: This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed

## 9.4.11 REG0A

**Figure 38. REG0A**

7	6	5	4	3	2	1	0
0	1	1	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 19. REG0A**

Bit	Field	Type	Reset	Description
7	BOOSTV[3]	R/W	by REG_RST by Watchdog	512mV
6	BOOSTV[2]	R/W	by REG_RST by Watchdog	256mV
5	BOOSTV[1]	R/W	by REG_RST by Watchdog	128mV
4	BOOSTV[0]	R/W	by REG_RST by Watchdog	64mV
3	PFM_OTG_DIS	R/W	by REG_RST	0 – Enable (default = 0) 1 – Disable
<b>Boost Current Limit</b>				
2	BOOST_LIM[2]	R/W	by REG_RST by Watchdog	000: 0.5A 001: 0.8A 010: 1.0A 011: 1.2A 100: 1.5A
1	BOOST_LIM[1]	R/W	by REG_RST by Watchdog	101: 1.8A 110: 2.1A 111: 2.4A
0	BOOST_LIM[0]	R/W	by REG_RST by Watchdog	

## 9.4.12 REG0B

**Figure 39. REG0B**

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 20. REG0B**

Bit	Field	Type	Reset	Description
7	VBUS_STAT[2]	R	N/A	VBUS Status register bq25898D 000: No Input 001: USB Host SDP 010: USB CDP (1.5A) 011: USB DCP (3.25A) 100: Adjustable High Voltage DCP (MaxCharge) (1.5A) 101: Unknown Adapter (500mA) 110: Non-Standard Adapter (1A/2A/2.1A/2.4A) 111: OTG bq25898 000: No Input 001: USB Host SDP 010: Adapter (3.25A) 111: OTG Note: Software current limit is reported in IINLIM register
6	VBUS_STAT[1]	R	N/A	
5	VBUS_STAT[0]	R	N/A	
4	CHRG_STAT[1]	R	N/A	Charging Status 00 – Not Charging 01 – Pre-charge ( < V <sub>BATLOWV</sub> ) 10 – Fast Charging 11 – Charge Termination Done
3	CHRG_STAT[0]	R	N/A	
2	PG_STAT	R	N/A	Power Good Status 0 – Not Power Good 1 – Power Good
1	Reserved	R	N/A	Reserved: Always reads 1
0	VSYS_STAT	R	N/A	VSYS Regulation Status 0 – Not in VSYSMIN regulation (BAT > VSYSMIN) 1 – In VSYSMIN regulation (BAT < VSYSMIN)

### 9.4.13 REG0C

**Figure 40. REG0C**

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 21. REG0C**

Bit	Field	Type	Reset	Description
7	WATCHDOG_FAULT	R	N/A	Watchdog Fault Status Status 0 – Normal 1- Watchdog timer expiration
6	BOOST_FAULT	R	N/A	Boost Mode Fault Status 0 – Normal 1 – VBUS overloaded in OTG, or VBUS OVP, or battery is too low in boost mode
5	CHRG_FAULT[1]	R	N/A	Charge Fault Status 00 – Normal
4	CHRG_FAULT[0]	R	N/A	01 – Input fault ( $V_{BUS} > V_{ACOV}$ or $V_{BAT} < V_{BUS} < V_{VBUSMIN}$ (typical 3.8V) 10 - Thermal shutdown 11 – Charge Safety Timer Expiration
3	BAT_FAULT	R	N/A	Battery Fault Status 0 – Normal 1 – BATOVP ( $V_{BAT} > V_{BATOVP}$ )
2	NTC_FAULT[2]	R	N/A	NTC Fault Status Buck Mode: 000 – Normal 010 – TS Warm 011 – TS Cool 101 – TS Cold 110 – TS Hot Boost Mode: 000 – Normal 101 – TS Cold 110 – TS Hot
1	NTC_FAULT[1]	R	N/A	
0	NTC_FAULT[0]	R	N/A	

## 9.4.14 REG0D

**Figure 41. REG0D**

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 22. REG0D**

Bit	Field	Type	Reset	Description
7	FORCE_VINDPM	R/W	by REG_RST	VINDPM Threshold Setting Method 0 – Run Relative VINDPM Threshold (default) 1 – Run Absolute VINDPM Threshold
6	VINDPM[6]	R/W	by REG_RST	6400mV
5	VINDPM[5]	R/W	by REG_RST	3200mV
4	VINDPM[4]	R/W	by REG_RST	1600mV
3	VINDPM[3]	R/W	by REG_RST	800mV
2	VINDPM[2]	R/W	by REG_RST	400mV
1	VINDPM[1]	R/W	by REG_RST	200mV
0	VINDPM[0]	R/W	by REG_RST	100mV

## 9.4.15 REG0E

**Figure 42. REG0E**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 23. REG0E**

Bit	Field	Type	Reset	Description
7	THERM_STAT	R	N/A	Thermal Regulation Status 0 – Normal 1 – In Thermal Regulation
6	BATV[6]	R	N/A	1280mV
5	BATV[5]	R	N/A	640mV
4	BATV[4]	R	N/A	320mV
3	BATV[3]	R	N/A	160mV
2	BATV[2]	R	N/A	80mV
1	BATV[1]	R	N/A	40mV
0	BATV[0]	R	N/A	20mV

## 9.4.16 REG0F

**Figure 43. REG0F**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 24. REG0F**

Bit	Field	Type	Reset	Description
7	Reserved	R	N/A	Reserved: Always reads 0
6	SYSV[6]	R	N/A	1280mV
5	SYSV[5]	R	N/A	640mV
4	SYSV[4]	R	N/A	320mV
3	SYSV[3]	R	N/A	160mV
2	SYSV[2]	R	N/A	80mV
1	SYSV[1]	R	N/A	40mV
0	SYSV[0]	R	N/A	20mV

ADC conversion of System Voltage ( $V_{SYS}$ )  
Offset: 2.304V  
Range: 2.304V (0000000) – 4.848V (1111111)  
Default: 2.304V (0000000)

## 9.4.17 REG10

**Figure 44. REG10**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 25. REG10**

Bit	Field	Type	Reset	Description
7	Reserved	R	N/A	Reserved: Always reads 0
6	TSPCT[6]	R	N/A	29.76%
5	TSPCT[5]	R	N/A	14.88%
4	TSPCT[4]	R	N/A	7.44%
3	TSPCT[3]	R	N/A	3.72%
2	TSPCT[2]	R	N/A	1.86%
1	TSPCT[1]	R	N/A	0.93%
0	TSPCT[0]	R	N/A	0.465%

ADC conversion of TS Voltage (TS) as percentage of REGN  
Offset: 21%  
Range 21% (0000000) – 80% (1111111)  
Default: 21% (0000000)



## 9.4.18 REG11

**Figure 45. REG11**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 26. REG11**

Bit	Field	Type	Reset	Description
7	VBUS_GD	R	N/A	VBUS Good Status 0 – Not VBUS attached 1 – VBUS Attached
6	VBUSV[6]	R	N/A	6400mV
5	VBUSV[5]	R	N/A	3200mV
4	VBUSV[4]	R	N/A	1600mV
3	VBUSV[3]	R	N/A	800mV
2	VBUSV[2]	R	N/A	400mV
1	VBUSV[1]	R	N/A	200mV
0	VBUSV[0]	R	N/A	100mV

ADC conversion of VBUS voltage ( $V_{BUS}$ )  
Offset: 2.6V  
Range 2.6V (0000000) – 15.3V (1111111)  
Default: 2.6V (0000000)

## 9.4.19 REG12

**Figure 46. REG12**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 27. REG12**

Bit	Field	Type	Reset	Description
7	Unused	R	N/A	Always reads 0
6	ICHGR[6]	R	N/A	3200mA
5	ICHGR[5]	R	N/A	1600mA
4	ICHGR[4]	R	N/A	800mA
3	ICHGR[3]	R	N/A	400mA
2	ICHGR[2]	R	N/A	200mA
1	ICHGR[1]	R	N/A	100mA
0	ICHGR[0]	R	N/A	50mA

ADC conversion of Charge Current ( $I_{BAT}$ ) when  $V_{BAT} > V_{BATSHORT}$   
Offset: 0mA  
Range 0mA (0000000) – 6350mA (1111111)  
Default: 0mA (0000000)  
Note:  
This register returns 0000000 for  $V_{BAT} < V_{BATSHORT}$

## 9.4.20 REG13

**Figure 47. REG13**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 28. REG13**

Bit	Field	Type	Reset	Description
7	VDPM_STAT	R	N/A	VINDPM Status 0 – Not in VINDPM 1 – VINDPM
6	IDPM_STAT	R	N/A	IINDPM Status 0 – Not in IINDPM 1 – IINDPM
5	IDPM_LIM[5]	R	N/A	1600mA
4	IDPM_LIM[4]	R	N/A	800mA
3	IDPM_LIM[3]	R	N/A	400mA
2	IDPM_LIM[2]	R	N/A	200mA
1	IDPM_LIM[1]	R	N/A	100mA
0	IDPM_LIM[0]	R	N/A	50mA

Input Current Limit in effect while Input Current Optimizer (ICO) is enabled  
Offset: 100mA (default)  
Range 100mA (0000000) – 3.25mA (1111111)

## 9.4.21 REG14

**Figure 48. REG14**

7	6	5	4	3	2	1	0
0	0	X	X	X	1	0	1
R/W	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 29. REG14**

Bit	Field	Type	Reset	Description
7	REG_RST	R/W	N/A	Register Reset 0 – Keep current register setting (default) 1 – Reset to default register value and reset safety timer Note: Reset to 0 after register reset is completed
6	ICO_OPTIMIZED	R	N/A	Input Current Optimizer (ICO) Status 0 – Optimization is in progress 1 – Maximum Input Current Detected
5	PN[2]	R	N/A	Device Configuration 010: bq25898D 000: bq25898
4	PN[1]	R	N/A	
3	PN[0]	R	N/A	
2	TS_PROFILE	R	N/A	Temperature Profile 1- JEITA (default)
1	DEV_REV[1]	R	N/A	Device Revision: 01
0	DEV_REV[0]	R	N/A	

## 10 Application and Implementation

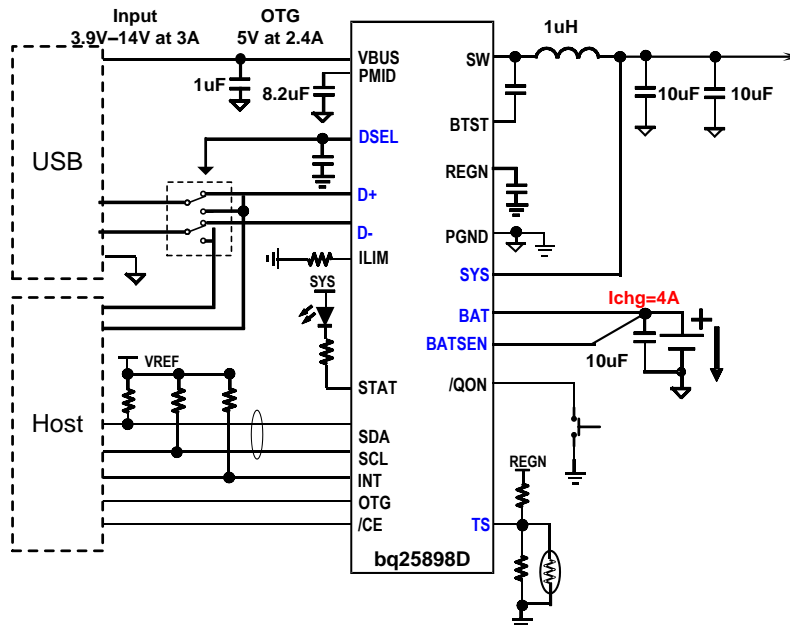
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

A typical application consists of the device configured as an I<sup>2</sup>C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

### 10.2 Typical Application Diagram



Copyright © 2016, Texas Instruments Incorporated

VREF is the pull up voltage of I2C communication interface

**Figure 49. bq25898D Application Diagram with PSEL with Interface and USB On-The-Go (OTG)**

#### 10.2.1 Design Requirements

For this design example, use the parameters shown in [Table 30](#).

**Table 30. Design Parameters**

PARAMETER	VALUE
Input voltage range	3.9 V to 14 V
Input current limit	1.5 A
Fast charge current	4032 mA
Output voltage	4.208 V

## 10.2.2 Detailed Design Procedure

### 10.2.2.1 Inductor Selection

The device has 1.5 MHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current ( $I_{CHG}$ ) plus half the ripple current ( $I_{RIPPLE}$ ):

$$I_{BAT} \geq I_{CHG} + (1/2) I_{RIPPLE} \quad (5)$$

The inductor ripple current depends on input voltage ( $V_{BUS}$ ), duty cycle ( $D = V_{BAT}/V_{BUS}$ ), switching frequency ( $f_s$ ) and inductance ( $L$ ):

$$I_{RIPPLE} = \frac{V_{BUS} \times D \times (1-D)}{f_s \times L} \quad (6)$$

The maximum inductor ripple current happens with  $D = 0.5$  or close to 0.5. Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

### 10.2.2.2 Buck Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current  $I_{PMID}$  occurs where the duty cycle is closest to 50% and can be estimated by [Equation 7](#):

$$I_{PMID} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (7)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25 V rating or higher capacitor is preferred for up to 14-V input voltage. 8.2- $\mu$ F capacitance is suggested for typical of 3 A – 5 A charging current.

### 10.2.2.3 System Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current  $I_{COUT}$  is given:

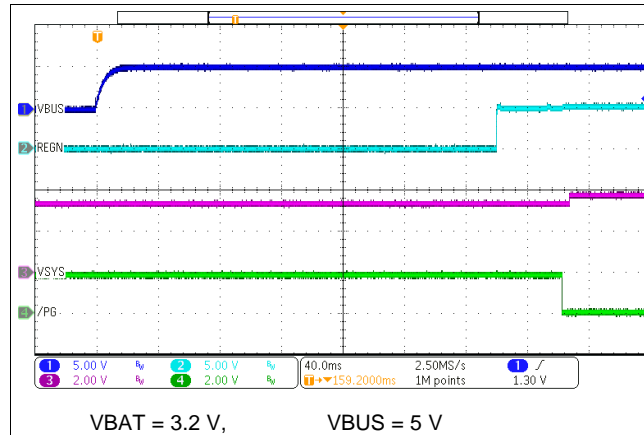
$$I_{CSYS} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (8)$$

The output capacitor voltage ripple can be calculated as follows:

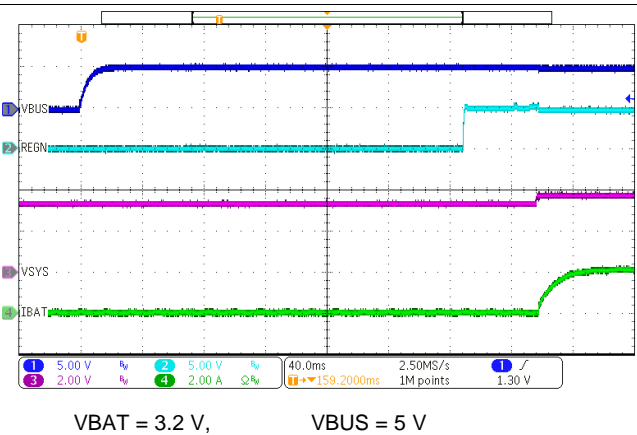
$$\Delta V_O = \frac{V_{SYS}}{8 L C_{SYS} f_s^2} \left( 1 - \frac{V_{SYS}}{V_{BUS}} \right) \quad (9)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC. The charger device has internal loop compensator. To get good loop stability, 1- $\mu$ H and minimum of 20- $\mu$ F output capacitor is recommended. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.

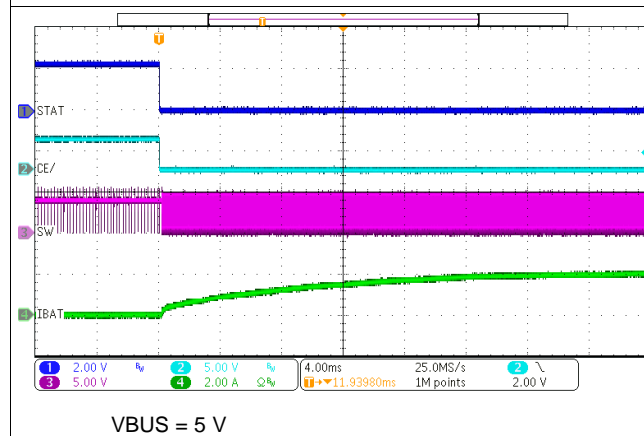
## 10.2.3 Application Curves



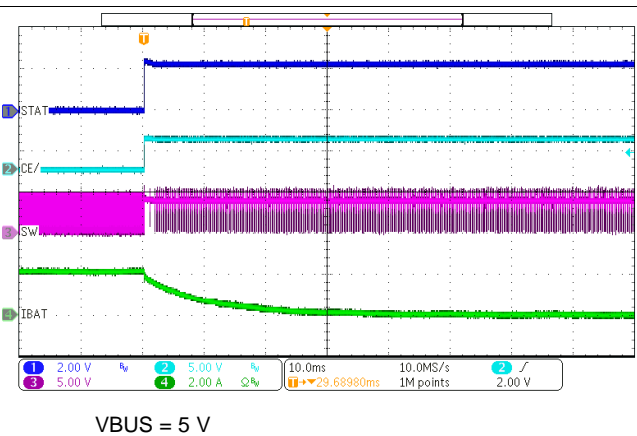
**Figure 50. Power Up with Charge Disabled**



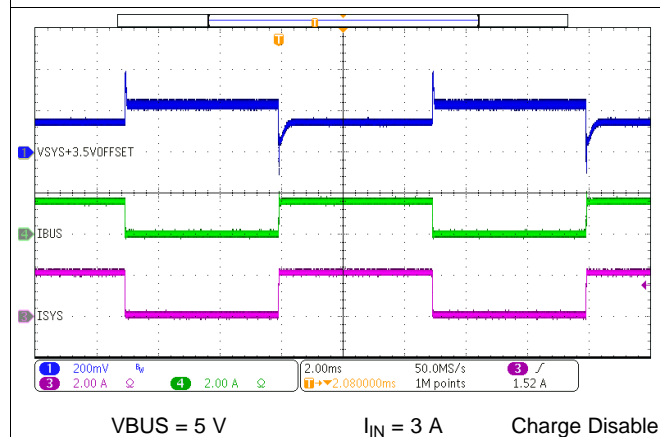
**Figure 51. Power Up with Charge Enabled**



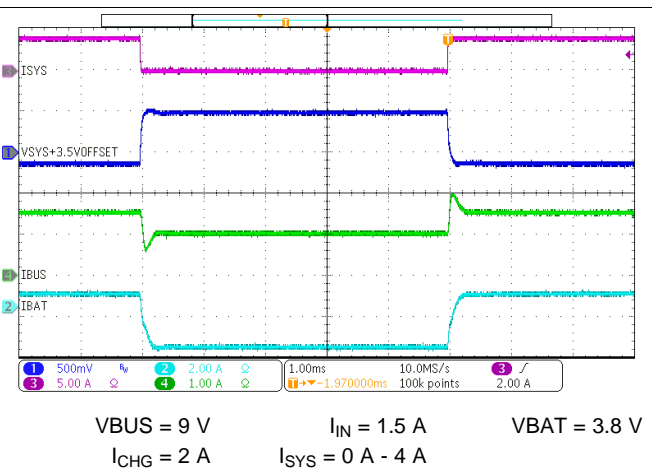
**Figure 52. Charge Enable**



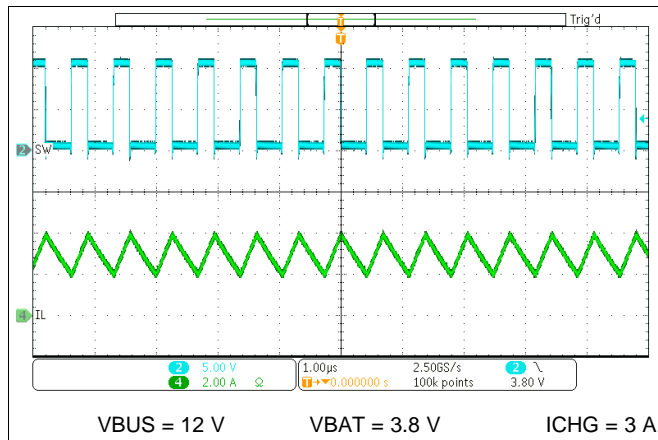
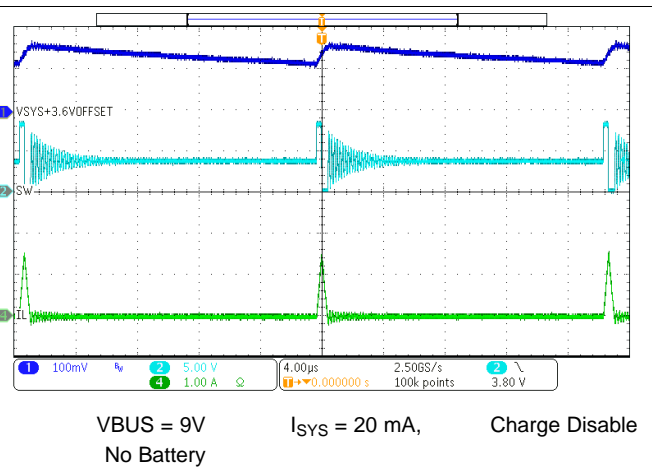
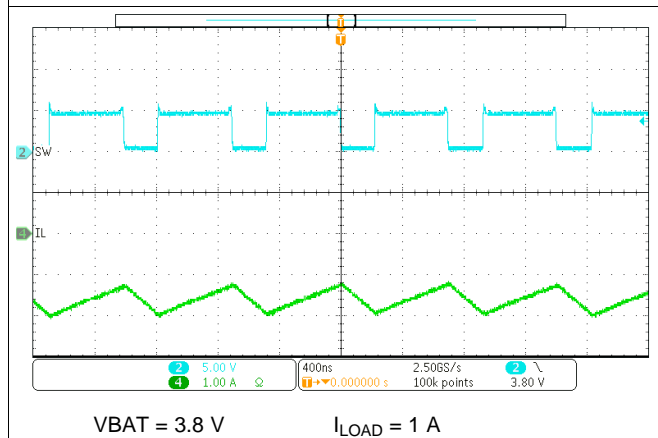
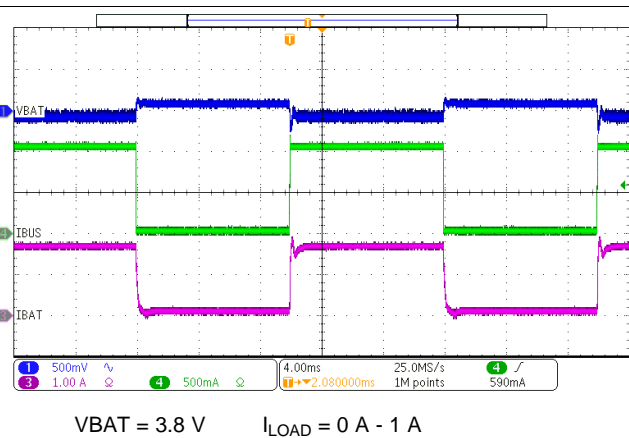
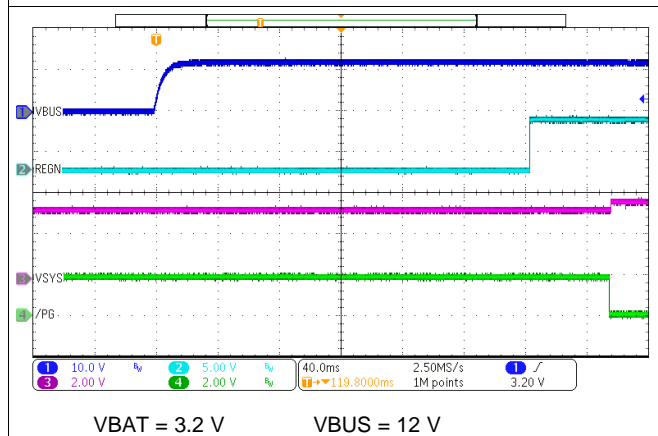
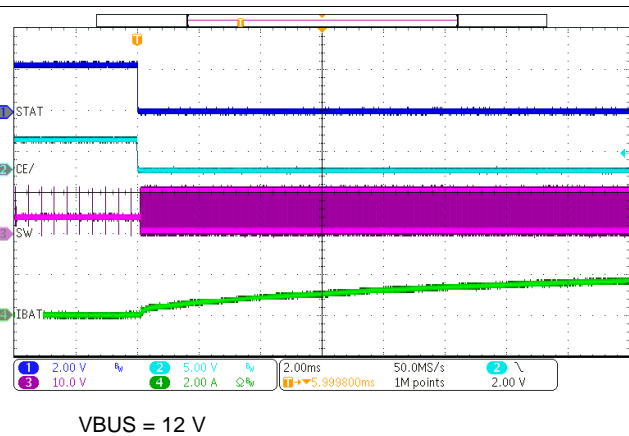
**Figure 53. Charge Disable**

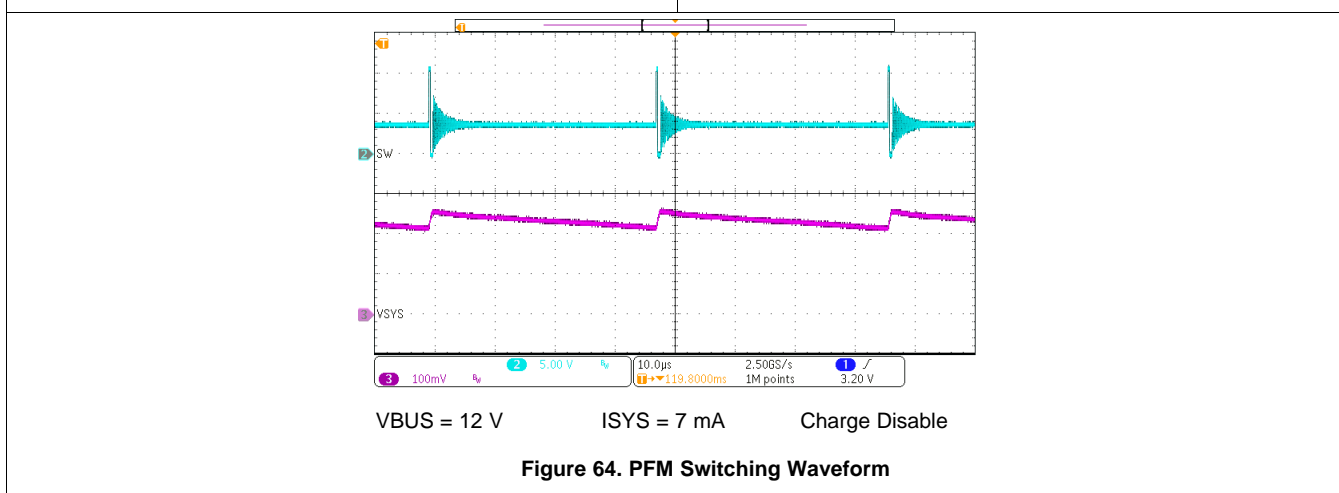
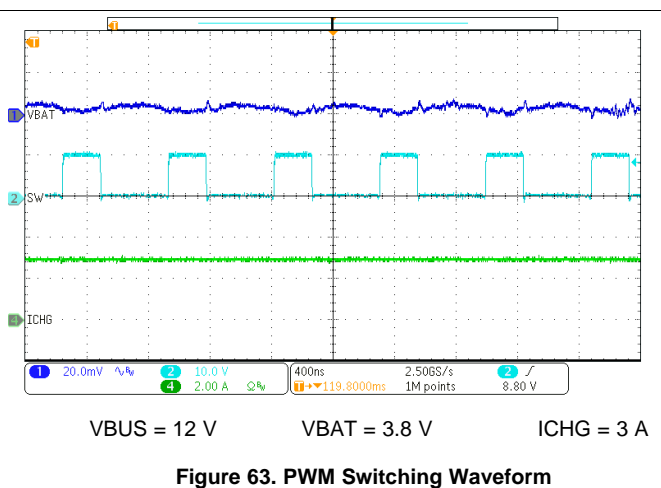
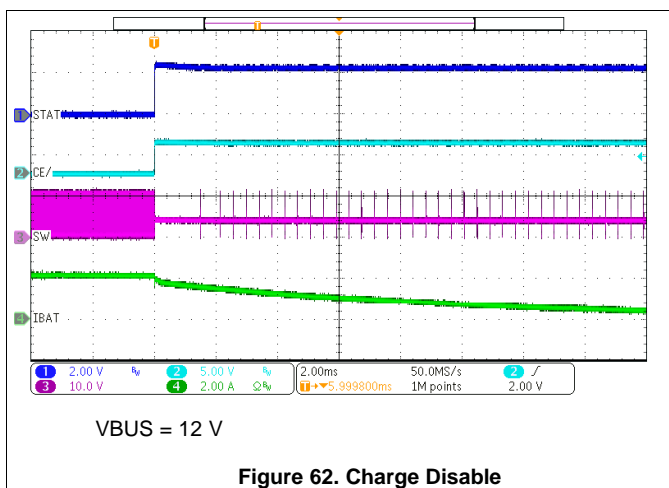


**Figure 54. Input Current DPM Response without Battery**

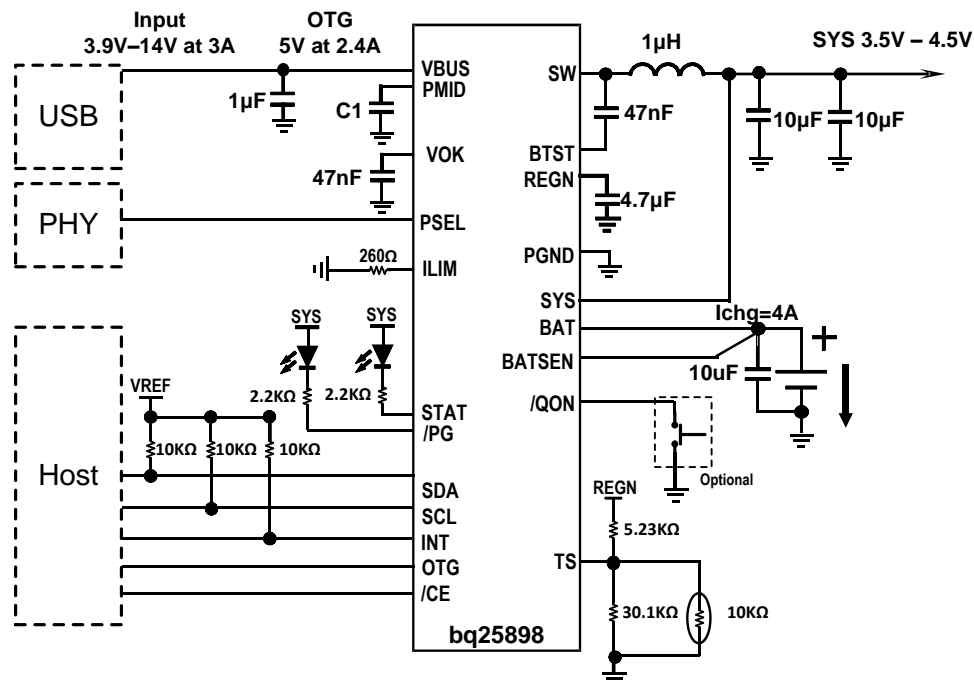


**Figure 55. Load Transient During Supplement Mode**


**Figure 56. PWM Switching Waveform**

**Figure 57. PFM Switching Waveform**

**Figure 58. Boost Mode Switching Waveform**

**Figure 59. Boost Mode Load Transient**

**Figure 60. Power Up with Charge Disabled**

**Figure 61. Charge Enable**



### 10.3 System Example



Copyright © 2016, Texas Instruments Incorporated

C1 = 8.2μF (OTG ≤ 1.8A) or 20μF (OTG ≤ 2.4A) is recommended

**Figure 65. bq25898 with PSEL Interface and USB On-The-Go (OTG)**



## 11 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9 V and 14 V input with at least 100-mA current rating connected to VBUS or a single-cell Li-Ion battery with voltage  $> V_{BATUVLO}$  connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

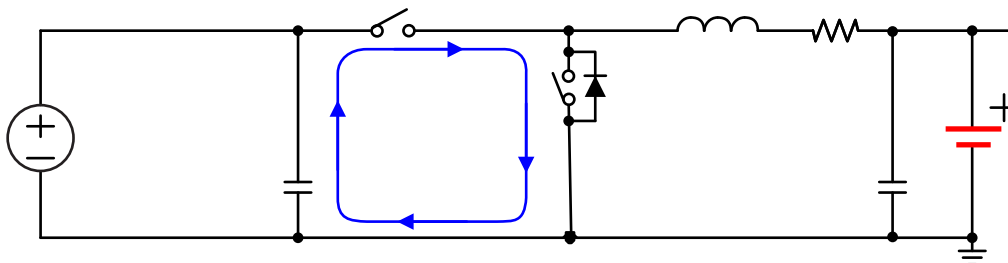
## 12 Layout

### 12.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see [Figure 66](#)) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Put output capacitor near to the inductor and the IC.
3. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
4. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
5. Connect all grounds together to reduce PCB size and improve thermal dissipation.
6. Avoid ground planes in parallel with high frequency traces in other layers.

### 12.2 Layout Example



**Figure 66. High Frequency Current Path**

## 13 Device and Documentation Support

### 13.1 Device Support

#### 13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 31. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq25898	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
bq25898D	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 Trademarks

MaxCharge, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.7 Glossary

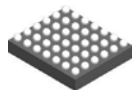
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

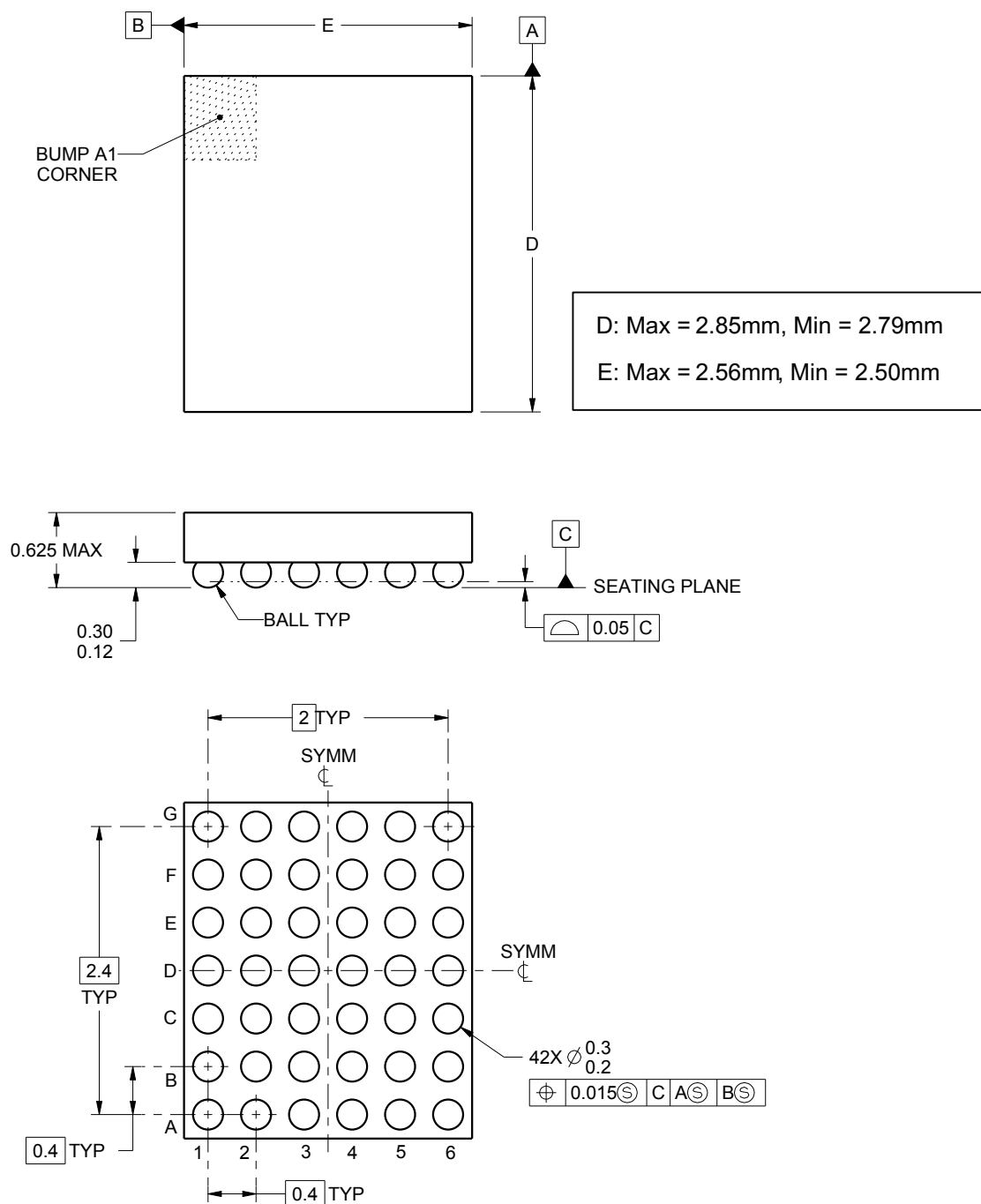
YFF0042



# PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4222067/A 05/2015

## NOTES:

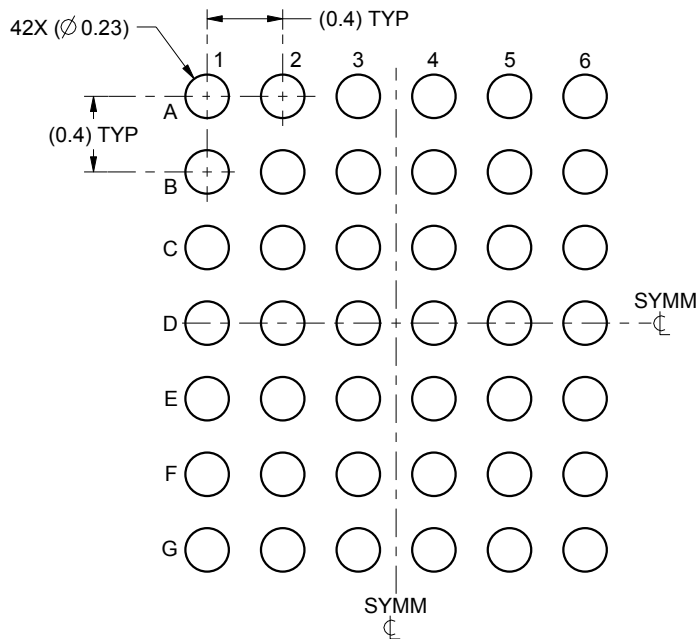
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

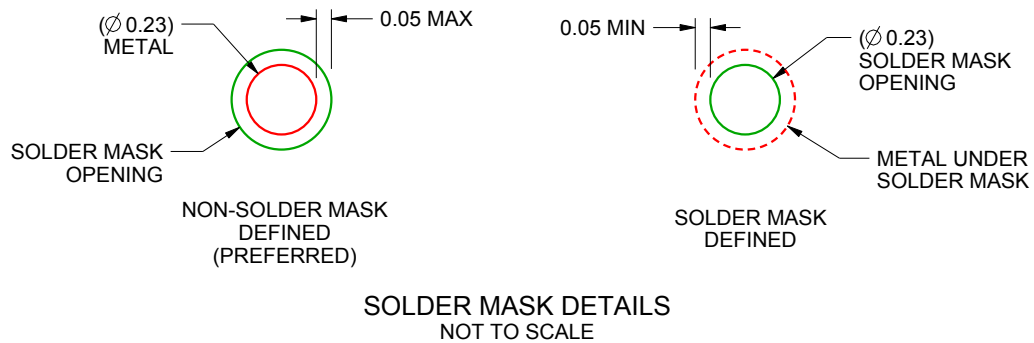
YFF0042

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:25X



4222067/A 05/2015

NOTES: (continued)

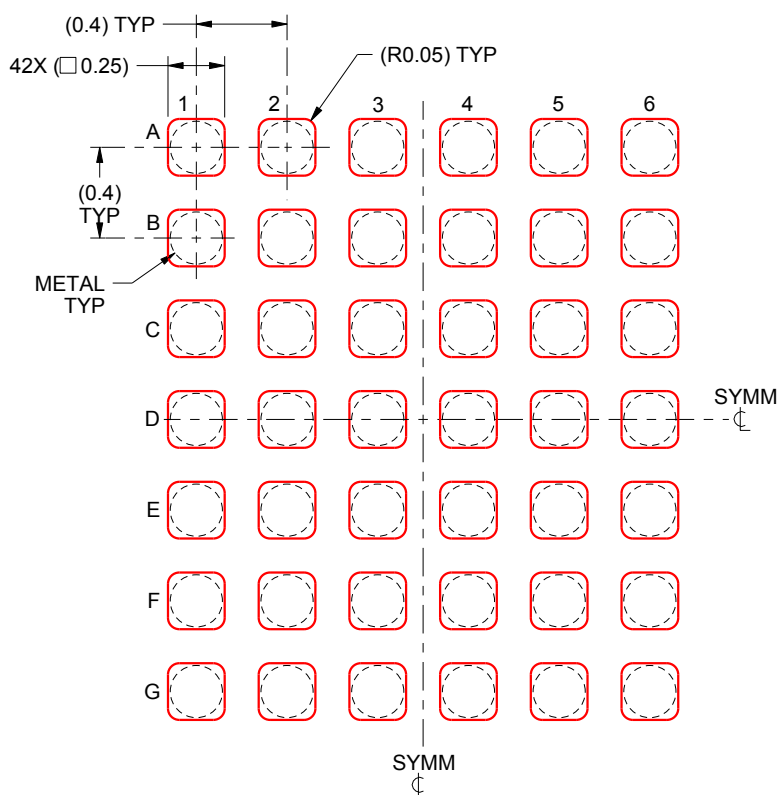
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YFF0042

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4222067/A 05/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">BQ25898DYFFR</a>	Active	Production	DSBGA (YFF)   42	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ25898D
BQ25898DYFFR.A	Active	Production	DSBGA (YFF)   42	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ25898D
<a href="#">BQ25898DYFFT</a>	Active	Production	DSBGA (YFF)   42	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ25898D
BQ25898DYFFT.A	Active	Production	DSBGA (YFF)   42	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ25898D
<a href="#">BQ25898YFFR</a>	Active	Production	DSBGA (YFF)   42	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ25898
BQ25898YFFR.A	Active	Production	DSBGA (YFF)   42	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ25898
<a href="#">BQ25898YFFT</a>	Active	Production	DSBGA (YFF)   42	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ25898
BQ25898YFFT.A	Active	Production	DSBGA (YFF)   42	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ25898

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25898DYFFR	DSBGA	YFF	42	3000	180.0	8.4	2.66	2.95	0.81	4.0	8.0	Q1
BQ25898DYFFT	DSBGA	YFF	42	250	180.0	8.4	2.66	2.95	0.81	4.0	8.0	Q1
BQ25898YFFR	DSBGA	YFF	42	3000	180.0	8.4	2.66	2.95	0.81	4.0	8.0	Q1
BQ25898YFFR	DSBGA	YFF	42	3000	180.0	8.4	2.66	2.95	0.81	4.0	8.0	Q1
BQ25898YFFT	DSBGA	YFF	42	250	180.0	8.4	2.66	2.95	0.81	4.0	8.0	Q1



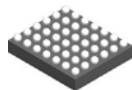
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25898DYFFR	DSBGA	YFF	42	3000	182.0	182.0	20.0
BQ25898DYFFT	DSBGA	YFF	42	250	182.0	182.0	20.0
BQ25898YFFR	DSBGA	YFF	42	3000	182.0	182.0	20.0
BQ25898YFFR	DSBGA	YFF	42	3000	182.0	182.0	20.0
BQ25898YFFT	DSBGA	YFF	42	250	182.0	182.0	20.0

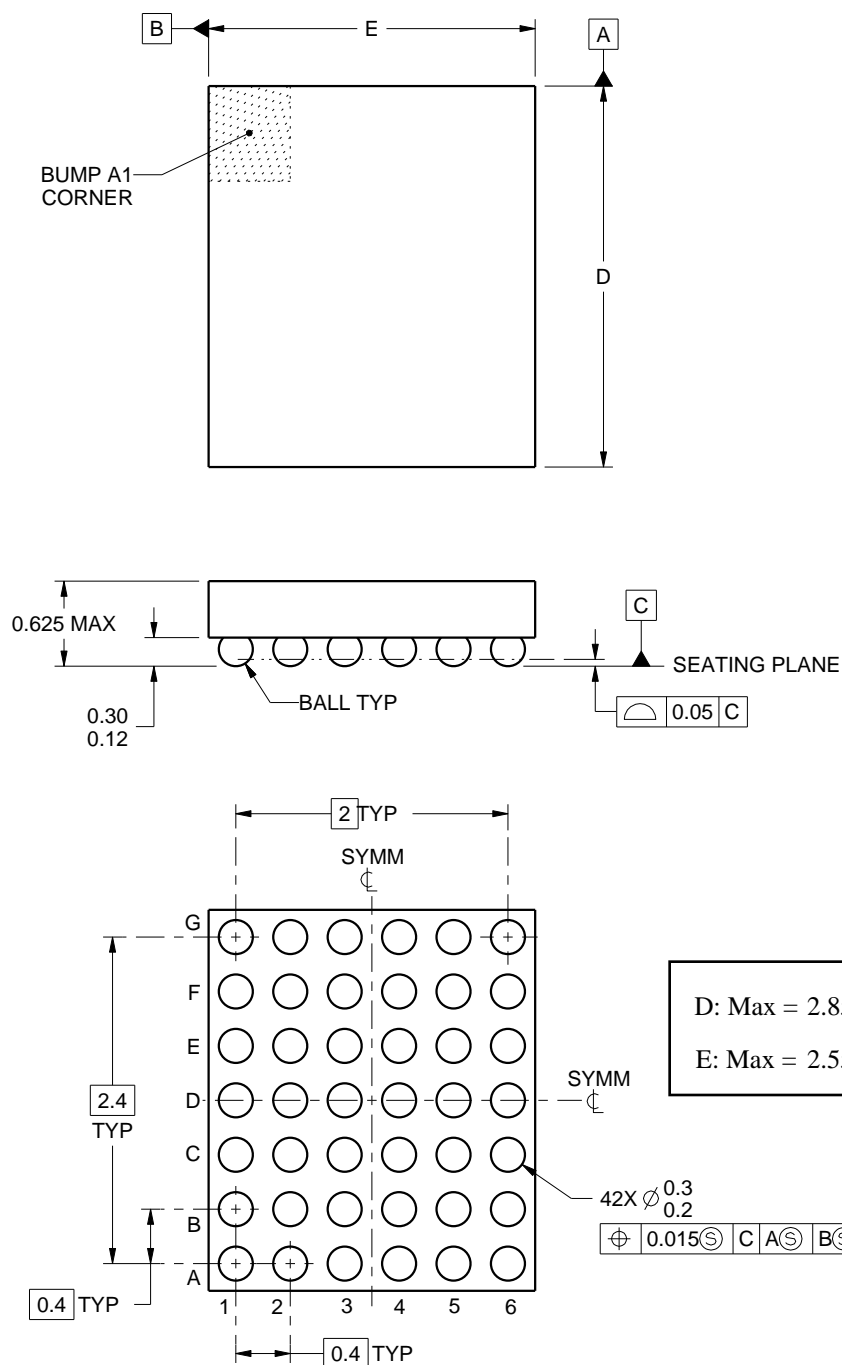
YFF0042



# PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4222067/A 05/2015

## NOTES:

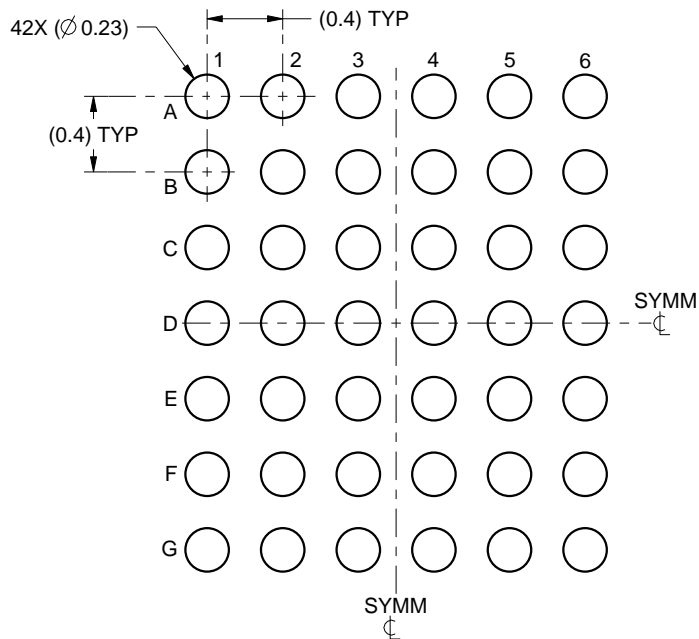
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

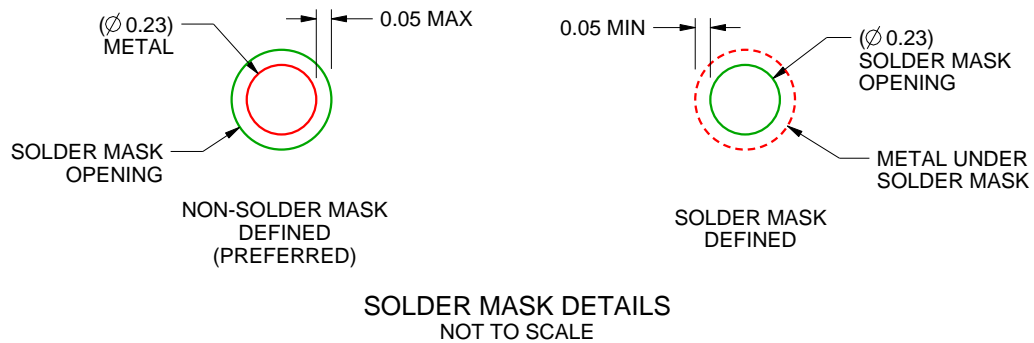
YFF0042

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:25X



4222067/A 05/2015

NOTES: (continued)

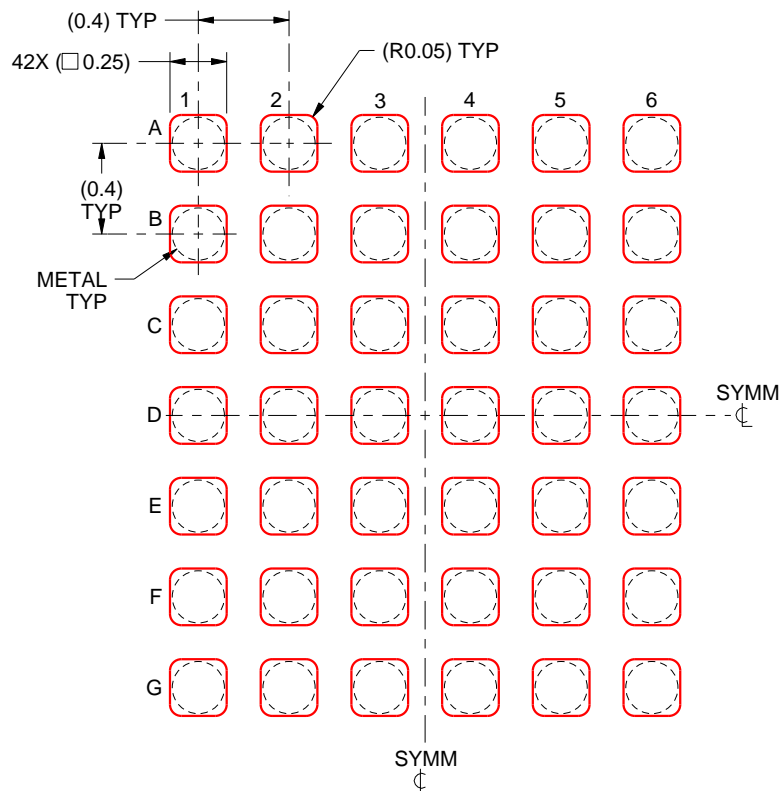
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YFF0042

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4222067/A 05/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated