

# BQ25792 I<sup>2</sup>C Controlled, 1-4 Cell, 5-A Buck-Boost Battery Charger with Dual-Input Selector and USB PD 3.0 OTG Output

## 1 Features

- High power density, high integration buck-boost charger for 1-4 cell batteries supporting any USB PD 3.0 profile
  - Integrates four switching MOSFETs, BATFET
  - Integrates input and charging current sensing
- Highly efficient
  - 750-kHz or 1.5-MHz switching frequencies
  - 5-A charging current with 10-mA resolution
    - 96.5% efficient: 16-V battery at 3A from 20V
- Supports a wide range of input sources
  - 3.6-V to 24-V wide input operating voltage range with 30-V absolute maximum rating
  - Maximum power tracking with input voltage dynamic power management (VINDPM) up to 22 V and input current dynamic power management (IINDPM) up to 3.3 A
  - Detects USB BC1.2, SDP, CDP, DCP, HVDCP and non-standard adapters
- Dual-input power mux controller (optional) for source selection
- Narrow voltage DC (NVDC) power path management
- Powers USB port from battery (USB OTG)
  - 2.8-V to 22-V OTG output voltage with 10-mV resolution to support USB-PD PPS
  - OTG output current regulation up to 3.32 A with 40-mA resolution
- Flexible autonomous and I<sup>2</sup>C mode for optimal system performance
- Integrated 16-bit ADC for voltage, current, and temperature monitoring
- Low battery quiescent current
  - 21  $\mu$ A for battery only operation
  - 600 nA in Charger Shutdown Mode
- High accuracy
  - +0.65% to -0.85% charge voltage regulation for 2S-4S batteries
  - $\pm$ 5% charge current regulation
  - $\pm$ 5% input current regulation
- Safety
  - Thermal regulation and thermal shutdown
  - Input/battery OVP and OCP
  - Converter MOSFETs OCP
  - Charging safety timer
- Package
  - 29-Pin 4 mm  $\times$  4 mm QFN

## 2 Applications

- [Video doorbell](#), [Smart home control](#)
- [Data concentrators](#), [Robotic lawn mower](#), [Vacuum robot](#)
- [Asset tracking](#), [Mobile POS](#)
- [Multiparameter patient monitor](#), [Electrocardiogram \(ECG\)](#), [Ultrasound smart probe](#)

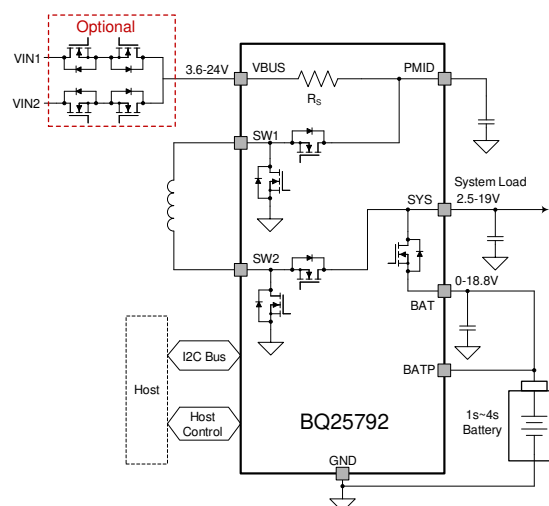
## 3 Description

The BQ25792 is a fully integrated switch-mode buck-boost charger for 1-4 cell Li-ion batteries and Li-polymer batteries. The integration includes 4 switching MOSFETs ( $Q_1$ ,  $Q_2$ ,  $Q_3$ ,  $Q_4$ ), input and charging current sensing circuits, the battery FET ( $Q_{BAT}$ ) and all the loop compensation of the buck-boost converter. It uses NVDC power path management, regulating the system slightly above the battery voltage without dropping below a configurable minimum system voltage. When system power exceeds the input source rating, battery supplement mode supports the system without overloading the input source. BQ25792 supports the full input and output (OTG) voltage ranges for USB Type-C™ and USB power delivery (USB-PD) applications.

### Device Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM) |
|-------------|------------------------|-----------------|
| BQ25792     | QFN (29)               | 4.0 mm x 4.0 mm |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision B (March 2021) to Revision C (August 2022)</b>   | <b>Page</b> |
|---|-------------|
| • Updated <a href="#">Section 5</a> device comparison table.....  | <b>3</b>    |
| • Removed reference to /PG pin and IBAT pin throughout the datasheet.....   | <b>4</b>    |
| • Corrected common drain to common source in ACDRVx pin function in <a href="#">Section 7</a> .....               | <b>5</b>    |
| • Added how to set max input current limit with ILIM_HIZ pin in <a href="#">Section 7</a> .....                   | <b>5</b>    |
| • Added SDRV connected to BAT when shipFET disabled as an option in <a href="#">Section 7</a> .....               | <b>5</b>    |
| • Clarified /QON pull up voltage in <a href="#">Section 7</a> .....   | <b>5</b>    |
| • Updated : System voltage regulation accuracy (when $V_{BAT} < V_{SYSMIN}$ ).....                                | <b>9</b>    |
| • Updated: OTG mode voltage regulation accuracy.....  | <b>9</b>    |
| • Added input sensing resistor to <a href="#">Section 9.2</a> .....   | <b>25</b>   |
| • Clarified buck-boost switching operation in <a href="#">Section 9.3.6</a> .....                                 | <b>34</b>   |
| • Added explanation of no battery operation in <a href="#">Section 9.3.6</a> .....                                | <b>34</b>   |
| • Clarified PFM peak inductor current in <a href="#">Section 9.3.6.3</a> .....                                    | <b>35</b>   |
| • Clarified SYSMIN charge current clamp and settings in <a href="#">Section 9.3.9.2</a> .....                     | <b>39</b>   |
| • Clarified trickle to precharge regulation in <a href="#">Section 9.3.9.2</a> .....                              | <b>39</b>   |
| • Added SDRV typical output voltage and current to <a href="#">Section 9.3.12</a> .....                           | <b>46</b>   |
| • Updated I2C terminology in text and figures in <a href="#">Section 9.3.14</a> .....                             | <b>49</b>   |
| • Clarified REG0x14 and REG0x33 regarding reporting IBAT discharge current in <a href="#">Section 9.5.1</a> ..... | <b>53</b>   |
| • Changed REG0x2E to no longer recommend 12-bit ADC setting in <a href="#">Section 9.5.1</a> .....                | <b>53</b>   |
| • Corrected part number and device revision in REG0x48 in <a href="#">Section 9.5.1</a> .....                     | <b>53</b>   |
| • Corrected voltage ADC readings as not being 2's complement in <a href="#">Section 9.5.1</a> .....               | <b>53</b>   |
| • Added optional input snubber/TVS to apps diagram in <a href="#">Section 10.2</a> .....                          | <b>126</b>  |

| <b>Changes from Revision A (November 2020) to Revision B (March 2021)</b>                                 | <b>Page</b> |
|---|-------------|
| • Consolidated voltage and current protections into list format in <a href="#">Section 9.3.13.1</a> ..... | <b>48</b>   |

| <b>Changes from Revision * (June 2020) to Revision A (November 2020)</b> | <b>Page</b> |
|--|-------------|
| • Changed from Advance Information to Production Data.....               | <b>1</b>    |

## 5 Device Comparison

| PART NUMBER        | BQ25790                 | BQ25792             | BQ25798             |
|--------------------|-------------------------|---------------------|---------------------|
| ACOV Default Value | 7V                      | 26V                 | 26V                 |
| ACOV Options       | 7V, 12V, 18V or 26V     | 7V, 12V, 22V or 26V | 7V, 12V, 22V or 26V |
| /PG pin            | Yes                     | No                  | No                  |
| IBAT pin           | Yes                     | No                  | No                  |
| BATN pin           | Yes                     | No                  | No                  |
| MPPT               | No                      | No                  | Yes                 |
| Backup Mode        | No                      | No                  | Yes                 |
| Package            | DSBGA 56, 2.9mm x 3.3mm | QFN 29, 4mm x 4mm   | QFN 29, 4mm x 4mm   |

## 6 Description (continued)

The charger supports the narrow VDC power path management, in which the system is regulated at a voltage slightly higher than the battery voltage without being allowed to drop below the minimum system voltage. The minimum system voltage allows the system to operate even when the battery is completely discharged or removed. When system power exceeds the input source rating, battery supplement mode supports the system power requirement without overloading the input source.

The device charges a battery from a wide range of the input sources including legacy USB adapter to high voltage USB PD adapter and traditional barrel adapter. The charger automatically sets converter to be buck, boost or buck-boost configurations based on input voltage and battery voltage without the host control. The dual input source selector manages the power flowing from two different input sources. The inputs selection is controlled by the host through I<sup>2</sup>C with default source #1 (VAC1) as the primary input and the source #2 (VAC2) as the secondary input.

To support fast charging using adjustable high voltage adapter, the device provides D+/D- handshake. The device is compliant with USB 2.0 and USB 3.0 power delivery specification with input current and voltage regulation. In addition, the Input Current Optimizer (ICO) allows the detection of maximum power point of an unknown input source.

Besides the I<sup>2</sup>C host controlled charging mode, this charger also supports autonomous charging mode. After power up, the charging is enabled with default register settings. The device can complete a charging cycle without any software engagements. It detects battery voltage and charges the battery in different phases: trickle charging, pre-charging, constant current (CC) charging and constant voltage (CV) charging. At the end of the charging cycle, the charger automatically terminates when the charge current is below a pre-set limit (termination current) in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

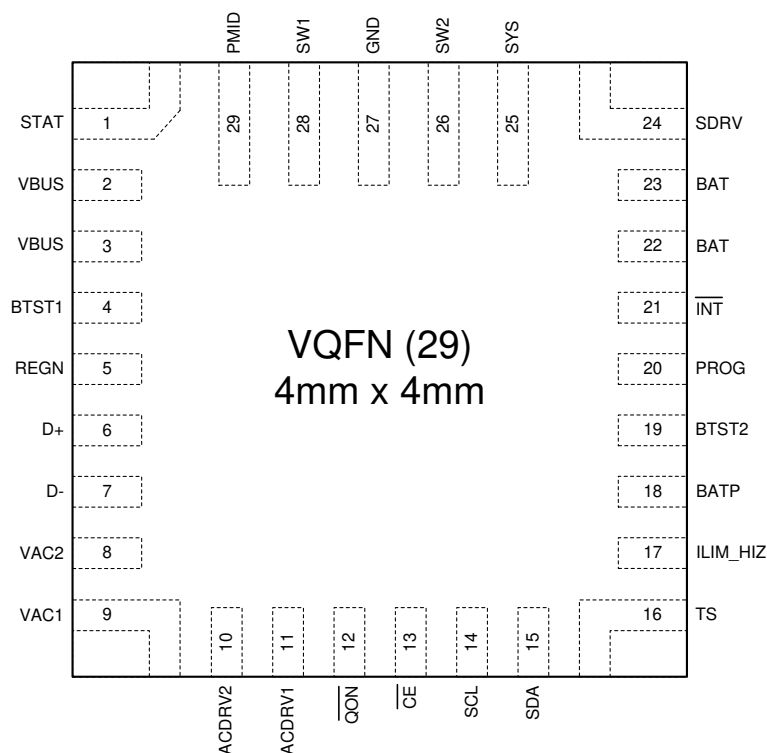
In the absence of input sources, this device supports USB On-the-Go (OTG) function, discharging battery to generate an adjustable 2.8-V to 22-V voltage on VBUS with 10-mV step size, which is compliant to the USB PD 3.0 specification defined programmable power supply (PPS) feature.

The charger provides various safety features for battery charging and system operations, including battery temperature negative thermistor monitoring, trickle charge, pre-charge and fast charge timers and over-voltage/overcurrent protections on battery and input. The thermal regulation reduces charge current when the junction temperature exceeds a programmable threshold. The STAT output of the device reports the charging status and any fault conditions. The INT pin immediately notifies host when fault occurs.

The device also provides a 16-bit analog-to-digital converter (ADC) for monitoring charge current and input/battery/system (VAC, VBUS, BAT, SYS, TS) voltages.

It is available in a 29-pin 4mm × 4mm QFN package.

## 7 Pin Configuration and Functions



**Figure 7-1. RQM Package 29-Pin VQFN Top View**

**Table 7-1. Pin Functions**

| PIN   |     | I/O | DESCRIPTION  |
|-------|-----|-----|--|
| NAME  | NO. |     |  |
| STAT  | 1   | DO  | <b>Open Drain Charge Status Output</b> – It indicates various charger operations. Connect to the pull up rail via a 10kΩ resistor. LOW indicates charging in progress. HIGH indicates charging completed or charging disabled. When any fault condition occurs, STAT pin blinks at 1Hz. The STAT pin function can be disabled when DIS_STAT bit is set to 1. |
| VBUS  | 2-3 | P   | <b>Charger Input Voltage</b> – The power input terminal of the charger. An input current sensing circuit is connected between VBUS and PMID. The recommended capacitors at VBUS are 2 pieces of 10μF and one piece of 0.1μF ceramic capacitors. Place the 0.1μF ceramic capacitor as close as possible to the charger IC.                                    |
| BTST1 | 4   | P   | <b>Input High Side Power MOSFET Gate Driver Power Supply</b> – Connect a 10V or higher rating, 47nF ceramic capacitor between SW1 and BTST1 as the bootstrap capacitor for driving high side switching MOSFET (Q1).  |
| REGN  | 5   | P   | <b>The Charger Internal Linear Regulator Output</b> – It is supplied from either VBUS or BAT dependent on which voltage is higher. Connect a 10V, 4.7μF ceramic capacitor from REGN to power ground. The REGN LDO output is used for the internal MOSFETs gate driving voltage and the voltage bias for TS pin resistor divider.                             |
| D+    | 6   | AIO | <b>Positive Line of the USB Data Line Pair</b> – D+/D- based USB host/charging port detection for VIN1 input. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and the adjustable high voltage adapter.  |
| D-    | 7   | AIO | <b>Negative Line of the USB Data Line Pair</b> – D+/D- based USB host/charging port detection for VIN1 input. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and the adjustable high voltage adapter.  |
| VAC2  | 8   | P   | <b>VAC2 Input Detection</b> – When a voltage between 3.6V and 24V is applied on VAC2, it represents a valid input being plugged into port #2. Connect to VBUS if the ACFET2 and RBFET2 are not installed.  |
| VAC1  | 9   | P   | <b>VAC1 Input Detection</b> – When a voltage between 3.6V and 24V is applied on VAC1, it represents a valid input being plugged into port #1. Connect to VBUS if the ACFET1 and RBFET1 are not installed.  |

**Table 7-1. Pin Functions (continued)**

| PIN                     |       | I/O | DESCRIPTION  |
|-------------------------|-------|-----|--|
| NAME                    | NO.   |     |  |
| ACDRV2                  | 10    | P   | <b>Input FETs Driver Pin 2</b> – The charge pump output to drive the port #2 input N-channel MOSFET (ACFET2) and the reverse blocking N-channel MOSFET (RBFET2). The charger turns on the back-to-back MOSFETs by increasing the ACDRV2 voltage 5V above the common source connection of the ACFET2 and RBFET2 when the turn-on condition is met. Tie ACDRV2 to GND if no ACFET2 and RBFET2 installed.   |
| ACDRV1                  | 11    | P   | <b>Input FETs Driver Pin 1</b> – The charge pump output to drive the port #1 input N-channel MOSFET (ACFET1) and the reverse blocking N-channel MOSFET (RBFET1). The charger turns on the back-to-back MOSFETs by increasing the ACDRV1 voltage 5V above the common source connection of the ACFET1 and RBFET1 when the turn-on condition is met. Tie ACDRV1 to GND if no ACFET1 and RBFET1 installed.   |
| $\overline{\text{QON}}$ | 12    | DI  | <b>Ship FET Enable or System Power Reset Control Input</b> – When the device is in ship mode or in the shutdown mode, the SDRV turns off the external ship FET to minimize the battery leakage current. A logic low on this pin with $t_{\text{SM\_EXIT}}$ duration turns on ship FET to force the device to exit the ship mode. A logic low on this pin with $t_{\text{RST}}$ duration resets system power by turning off the ship FET for $t_{\text{RST\_SFET}}$ (also setting the charger in HIZ mode when VBUS is high) and then turning on ship FET (also disabling the charger HIZ mode) to provide full system power reset. During $t_{\text{RST\_SFET}}$ when the ship FET is off, the charger applies a 30mA discharging current on SYS to discharge system voltage. The pin contains an internal pull-up through a $R_{\text{QON}}$ resistor. The typical output voltage is 3.6 V-3.8 V with VBUS and VBAT > 5V. |
| $\overline{\text{CE}}$  | 13    | DI  | <b>Active Low Charge Enable Pin</b> – Battery charging is enabled when EN_CHG bit is 1 and $\overline{\text{CE}}$ pin is LOW. $\overline{\text{CE}}$ pin must be pulled HIGH or LOW, do not leave floating.  |
| SCL                     | 14    | DI  | <b>I<sup>2</sup>C Interface Clock</b> – Connect SCL to the logic rail through a 10 k $\Omega$ resistor.  |
| SDA                     | 15    | DIO | <b>I<sup>2</sup>C Interface Data</b> – Connect SDA to the logic rail through a 10 k $\Omega$ resistor.   |
| TS                      | 16    | AI  | <b>Temperature Qualification Voltage Input</b> – Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin voltage is out of range. Recommend a 103AT-2 10k $\Omega$ thermistor.   |
| ILIM_HIZ                | 17    | AI  | <b>Input Current Limit Setting and HIZ Mode Control Pin</b> – Program ILIM_HIZ voltage by connecting a resistor divider from pull up rail to ILIM_HIZ pin to ground. The pin voltage is calculated as: $V_{\text{ILIM\_HIZ}} = 1\text{V} + 800\text{m}\Omega \times \text{IINDPM}$ , in which IINDPM is the target input current. The input current limit used by the charger is the lower setting of ILIM_HIZ pin and the IINDPM register. When the pin voltage is below 0.75V, the buck-boost converter enters non-switching mode, similar to HiZ mode using EN_HIZ bit, but with REGN on. When the pin voltage is above 1V, the converter resumes switching. Connect ILIM_HIZ to REGN to set the maximum input current limit.   |
| BATP                    | 18    | P   | <b>Positive Input for Battery Voltage Sensing</b> – Connect to the positive terminal of battery pack. Place 100 $\Omega$ series resistance between this pin and the battery positive terminal.   |
| BTST2                   | 19    | P   | <b>Output High Side Power MOSFET Gate Driver Power Supply</b> – Connect a 10V or higher rating, 47nF ceramic capacitor between SW2 and BTST2 as the bootstrap capacitor for driving high side switching MOSFET (Q4).   |
| PROG                    | 20    | AI  | <b>Charger POR Default Settings Program</b> – At power up, the charger detects the resistance tied to PROG pin to determine the default switching frequency and the default battery charging profile. The surface mount resistor with $\pm 1\%$ or $\pm 2\%$ tolerance is recommended. Please refer to more details in the section of PROG Pin Configuration.  |
| $\overline{\text{INT}}$ | 21    | DO  | <b>Open Drain Interrupt Output.</b> – Connect the $\overline{\text{INT}}$ pin to a logic rail via a 10k $\Omega$ resistor. The $\overline{\text{INT}}$ pin sends an active low, 256 $\mu\text{s}$ pulse to the host to report the charger device status and faults.  |
| BAT                     | 22-23 | P   | <b>The Battery Charging Power Connection</b> – Connect to the positive terminal of the battery pack. The internal charging current sensing circuit is connected between SYS and BAT. The recommended capacitors at BAT are 2 pieces of 10 $\mu\text{F}$ ceramic capacitors.  |
| SDRV                    | 24    | P   | <b>External N-channel Ship FET (SFET) Gate Driver Output</b> – The driver pin of the external ship FET. The ship FET is always turned on when the ship mode is disabled, and it keeps off when the charger is in ship mode or shutdown mode. Connect a 1nF, 50V rated, 0402 package, ceramic capacitor from SDRV to GND or SDRV to BAT when the ship FET is not used.  |
| SYS                     | 25    | P   | <b>The Charger Output Voltage to System</b> – The internal N-channel high side MOSFET (Q4) is connected between SYS and SW2 with drain on SYS and source on SW2. The recommended capacitors at SYS are 5 pieces of 10 $\mu\text{F}$ and one piece of 0.1 $\mu\text{F}$ ceramic capacitors. Place the 0.1 $\mu\text{F}$ ceramic capacitor as close as possible to the charger IC.   |
| SW2                     | 26    | P   | <b>Boost Side Half Bridge Switching Node</b> Inductor connection to mid point of Q3 and Q4 switches.   |
| GND                     | 27    | P   | <b>Ground Return</b>   |

**Table 7-1. Pin Functions (continued)**

| PIN  |     | I/O | DESCRIPTION  |
|------|-----|-----|--|
| NAME | NO. |     |  |
| SW1  | 28  | P   | <b>Buck Side Half Bridge Switching Node</b> Inductor connection to mid point of Q1 and Q2 switches.  |
| PMID | 29  | P   | <b>Q1 MOSFET Drain Connection</b> – An internal N-channel high side MOSFET (Q1) is connected between PMID and SW1 with drain on PMID and source on SW1. The recommended capacitors at PMID are 3 pieces of 10 $\mu$ F and one piece of 0.1 $\mu$ F ceramic capacitors. Place the 0.1 $\mu$ F ceramic capacitor as close as possible to the charger IC. |

## 8 Specifications

### 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                     |  | MIN       | MAX | UNIT |
|-------------------------------------|--|-----------|-----|------|
| Voltage range (with respect to GND) | VAC1, VAC2   | -2        | 30  | V    |
|                                     | VBUS (converter not switching)                                 | -2        | 30  | V    |
|                                     | PMID (converter not switching)                                 | -0.3      | 30  | V    |
|                                     | ACDRV1, ACDRV2, BTST1  | -0.3      | 32  | V    |
|                                     | SYS (converter not switching)                                  | -0.3      | 23  | V    |
|                                     | BATP, BAT  | -0.3      | 20  | V    |
|                                     | BTST2  | -0.3      | 29  | V    |
|                                     | SDRV   | -0.3      | 26  | V    |
|                                     | SW1  | -2 (50ns) | 30  | V    |
|                                     | SW2  | -2 (50ns) | 23  | V    |
|                                     | QON, D+, D-, CE, STAT, SCL, SDA, INT, ILIM_HIZ, PROG, TS, REGN | -0.3      | 6   | V    |
| Output Sink Current                 | INT, STAT  |           | 6   | mA   |
| Differential Voltage                | BTST1-SW1, BTST2-SW2   | -0.3      | 6   | V    |
|                                     | PMID-VBUS  | -0.3      | 6   | V    |
|                                     | SYS-BAT  | -0.3      | 16  | V    |
|                                     | SDRV-BAT   | -0.3      | 6   | V    |
| T <sub>J</sub>                      | Junction temperature   | -40       | 150 | °C   |
| T <sub>stg</sub>                    | Storage temperature  | -55       | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 8.2 ESD Ratings

|                    |                         |  | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±250  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                   |                                      | MIN | NOM | MAX  | UNIT |
|-------------------|--------------------------------------|-----|-----|------|------|
| V <sub>VBUS</sub> | Input voltage                        | 3.6 |     | 24   | V    |
| V <sub>BAT</sub>  | Battery voltage                      |     |     | 18.8 | V    |
| I <sub>VBUS</sub> | Input current                        |     |     | 3.3  | A    |
| I <sub>SW</sub>   | Output current (SW)                  |     |     | 5    | A    |
| I <sub>BAT</sub>  | Fast charging current                |     |     | 5    | A    |
|                   | RMS discharge current (continuously) |     |     | 6    | A    |
|                   | Peak discharge current (upto 1 sec)  |     |     | 10   | A    |
| T <sub>A</sub>    | Ambient temperature                  | -40 |     | 85   | °C   |



### 8.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

|                   |                            | MIN | NOM | MAX | UNIT |
|-------------------|----------------------------|-----|-----|-----|------|
| T <sub>J</sub>    | Junction temperature       | -40 |     | 125 | °C   |
| C <sub>VBUS</sub> | Effective VBUS capacitance |     | 2   |     | μF   |
| C <sub>PMID</sub> | Effective PMID capacitance |     | 4   |     | μF   |
| C <sub>SYS</sub>  | Effective SYS capacitance  |     | 6   |     | μF   |
| C <sub>BAT</sub>  | Effective BAT capacitance  |     | 3   |     | μF   |

### 8.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | BQ25792   | UNIT |
|-------------------------------|--|-----------|------|
|                               |  | RQM (QFN) |      |
|                               |  | 29-PIN    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 44.2      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 20.9      | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 9.7       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.5       | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 9.7       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 8.5 Electrical Characteristics

V<sub>VBUS\_UVLOZ</sub> < V<sub>VBUS</sub> < V<sub>VBUS\_OVP</sub>, T<sub>J</sub> = -40°C to +125°C, and T<sub>J</sub> = 25°C for typical values (unless otherwise noted)

| PARAMETER                 |  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|---------------------------|--|--|-----|-----|-----|------|
| <b>QUIESCENT CURRENTS</b> |  |  |     |     |     |      |
| I <sub>Q_BAT_ON</sub>     | Quiescent battery current (BATP, BAT, SYS) when the charger is in the battery only mode, battery FET is enabled, ADC is disabled | VBAT = 8V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, not in ship mode or shut down mode, system is powered by battery. T <sub>J</sub> < 85 °C |     | 17  | 24  | μA   |
| I <sub>Q_BAT_OFF</sub>    | Quiescent battery current (BATP) for when the charger is in ship mode.   | VBAT = 8V, No VBUS, I2C enabled, ADC disabled, in ship mode, T <sub>J</sub> < 85 °C  |     | 11  | 16  | μA   |
| I <sub>SD_BAT</sub>       | Shutdown battery current (BATP) when charger is in shut down mode.   | VBAT = 8V, No VBUS, I2C disabled, ADC disabled, in shut down mode, T <sub>J</sub> < 85 °C  |     | 0.5 | 0.7 | μA   |
| I <sub>Q_BAT_ON</sub>     | Quiescent battery current (BATP, BAT, SYS) when the charger is in the battery only mode, battery FET is enabled, ADC is enabled  | VBAT = 8V, No VBUS, I2C enabled, ADC enabled, not in ship mode or shut down mode, T <sub>J</sub> < 85 °C   |     | 540 |     | μA   |
| I <sub>Q_VBUS</sub>       | Quiescent input current (VBUS)   | VBUS = 15V, VBAT = 8V, charge disabled, converter switching, ISYS = 0A, OOA disabled   |     | 3   |     | mA   |
|                           |  | VBUS = 15V, VBAT = 8V, charge disabled, converter switching, ISYS = 0A, OOA enabled  |     | 5   |     | mA   |
| I <sub>SD_VBUS</sub>      | Shutdown input current (VBUS) in HIZ   | VBUS = 15V, HIZ mode, no battery, ADC disabled, ACDRV disabled   |     | 386 |     | μA   |
|                           |  | VBUS = 15V, HIZ mode, no battery, ADC disabled, ACDRV enabled  |     | 590 |     | μA   |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER                  |   | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNIT |
|----------------------------|---|---|------|------|------|------|
| I <sub>Q_OTG</sub>         | Quiescent battery current (BATP, BAT, SYS) in OTG         | VBAT = 8V, VBUS = 5V, OTG mode enabled, converter switching, I <sub>VBUS</sub> = 0A, OOA disabled |      | 3    |      | mA   |
|                            |   | VBAT = 8V, VBUS = 5V, OTG mode enabled, converter switching, I <sub>VBUS</sub> = 0A, OOA enabled  |      | 5    |      | mA   |
| VBUS / VBAT SUPPLY         |   |   |      |      |      |      |
| V <sub>VAC_PRESENT</sub>   | VAC present rising threshold to turn on the ACFET-RBFET   | For both VAC1 and VAC2  |      | 3.4  | 3.5  | V    |
|                            | VAC present falling threshold to turn off the ACFET-RBFET | For both VAC1 and VAC2  | 3.1  | 3.2  |      | V    |
| V <sub>VAC_OVP</sub>       | VAC overvoltage rising threshold, when VAC_OVP[1:0]=00    | For both VAC1 and VAC2  | 25.2 | 26   | 26.8 | V    |
|                            | VAC overvoltage falling threshold, when VAC_OVP[1:0]=00   | For both VAC1 and VAC2  | 24.4 | 25.2 | 26.0 | V    |
|                            | VAC overvoltage rising threshold, when VAC_OVP[1:0]=01    | For both VAC1 and VAC2  | 17.4 | 18.0 | 18.6 | V    |
|                            | VAC overvoltage falling threshold, when VAC_OVP[1:0]=01   | For both VAC1 and VAC2  | 16.9 | 17.5 | 18.1 | V    |
|                            | VAC overvoltage rising threshold, when VAC_OVP[1:0]=10    | For both VAC1 and VAC2  | 11.6 | 12   | 12.4 | V    |
|                            | VAC overvoltage falling threshold, when VAC_OVP[1:0]=10   | For both VAC1 and VAC2  | 11.2 | 11.6 | 12.0 | V    |
|                            | VAC overvoltage rising threshold, when VAC_OVP[1:0]=11    | For both VAC1 and VAC2  | 6.7  | 7    | 7.3  | V    |
|                            | VAC overvoltage falling threshold, when VAC_OVP[1:0]=11   | For both VAC1 and VAC2  | 6.5  | 6.8  | 7.1  | V    |
|                            | V <sub>VBUS_OP</sub>                                      | VBUS operating range  |      | 3.6  |      | 24   |
| V <sub>VBUS_UVLOZ</sub>    | VBUS rising for active I2C, no battery                    | VBUS rising   | 3.25 | 3.4  | 3.55 | V    |
| V <sub>VBUS_UVLO</sub>     | VBUS falling to turn off I2C, no battery                  | VBUS falling  | 3.05 | 3.2  | 3.35 | V    |
| V <sub>VBUS_PRESENT</sub>  | VBUS to start switching                                   | VBUS rising   | 3.3  | 3.4  | 3.5  | V    |
| V <sub>VBUS_PRESENTZ</sub> | VBUS to stop switching                                    | VBUS falling  | 3.1  | 3.2  | 3.3  | V    |
| V <sub>VBUS_OVP</sub>      | VBUS overvoltage rising threshold                         | VBUS rising   | 25.2 | 25.7 | 26.2 | V    |
| V <sub>VBUS_OVPZ</sub>     | VBUS overvoltage falling threshold                        | VBUS falling  | 24.0 | 24.4 | 24.8 | V    |
| I <sub>BUS_OCP</sub>       | IBUS over-current rising threshold                        |   | 7.0  | 8.0  | 9.0  | A    |
| I <sub>BUS_OCPZ</sub>      | IBUS over-current falling threshold                       |   | 6.5  | 7.5  | 8.5  | A    |
| V <sub>BAT_UVLOZ</sub>     | BAT voltage for active I2C, no VBUS, no VAC               | VBAT rising, when the charger is in ship mode   | 3.25 | 3.40 | 3.55 | V    |
|                            |   | VBAT rising, when the charger is in normal mode   | 2.50 | 2.60 | 2.71 | V    |

## 8.5 Electrical Characteristics (continued)

 $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER                    |  | TEST CONDITIONS   | MIN   | TYP   | MAX   | UNIT       |
|------------------------------|--|---|-------|-------|-------|------------|
| $V_{BAT\_UVLO}$              | BAT voltage to turn off I2C, no VBUS, no VAC   | VBAT falling, when the charger is in ship mode                                | 3.05  | 3.20  | 3.31  | V          |
|                              |  | VBAT falling, when the charger is in normal mode                              | 2.30  | 2.40  | 2.50  | V          |
| $V_{BAT\_OTG}$               | BAT voltage rising threshold to enable OTG mode  | VBAT rising   | 2.7   | 2.8   | 2.9   | V          |
| $V_{BAT\_OTGZ}$              | BAT voltage falling threshold to disable OTG mode  | VBAT falling  | 2.4   | 2.5   | 2.6   | V          |
| $V_{POORSRC}$                | Bad adapter detection threshold  | VBUS falling  | 3.3   | 3.4   | 3.5   | V          |
| $V_{POORSRC}$                | Bad adapter detection threshold hysteresis   | VBUS rising above $V_{POORSRC}$   | 150   | 200   | 250   | mV         |
| $I_{POORSRC}$                | Bad adapter detection current source   |   |       | 30    |       | mA         |
| $R_{VBUS\_PD}$               | VBUS pull down resistance  |   |       | 6     |       | k $\Omega$ |
| $R_{VAC\_PD}$                | VAC pull down resistance   | For both VAC1 and VAC2  |       | 60    |       | $\Omega$   |
| <b>POWER-PATH MANAGEMENT</b> |  |   |       |       |       |            |
| $V_{SYSMAX\_REG\_RNG}$       | System voltage regulation range, measured on SYS   |   | 3.2   |       | 19    | V          |
| $V_{SYSMAX\_REG\_ACC}$       | System voltage regulation accuracy (when $V_{BAT} > V_{SYSMIN}$ , charging disabled, PFM disabled) | $V_{BAT} = 16.8\text{V}$ (4s default)   | 16.82 | 17.00 | 17.25 | V          |
|                              |  | $V_{BAT} = 12.6\text{V}$ (3s default)   | 12.62 | 12.80 | 13.04 | V          |
|                              |  | $V_{BAT} = 8.4\text{V}$ (2s default)  | 8.44  | 8.60  | 8.77  | V          |
|                              |  | $V_{BAT} = 4.2\text{V}$ (1s default)  | 4.268 | 4.40  | 4.550 | V          |
| $V_{SYSMIN\_REG\_RNG}$       | $V_{SYSMIN}$ regulation range, measured on SYS   |   | 2.5   |       | 16    | V          |
| $V_{SYSMIN\_REG\_STEP}$      | $V_{SYSMIN}$ regulation step size  |   |       | 250   |       | mV         |
| $V_{SYSMIN\_REG\_ACC}$       |  | 4s battery  | 11.9  | 12.2  | 12.75 | V          |
|                              |  | 3s battery  | 9.0   | 9.2   | 9.55  | V          |
|                              |  | 2s battery  | 7.12  | 7.2   | 7.52  | V          |
|                              |  | 1s battery  | 3.5   | 3.7   | 4.1   | V          |
| $V_{SYS\_OVP}$               | VSYS overvoltage rising threshold  | As a percentage of the system regulation voltage, to turnoff the converter.   | 105.5 | 110.0 | 112.3 | %          |
|                              | VSYS overvoltage rising threshold  | $V_{SYS\_REG} = 17\text{V}$   | 18.36 | 18.70 | 19.04 | V          |
|                              | VSYS overvoltage rising threshold  | $V_{SYS\_REG} = 8.6\text{V}$  | 9.18  | 9.46  | 9.67  | V          |
|                              | VSYS overvoltage falling threshold   | As a percentage of the system regulation voltage, to re-enable the converter. | 95.5  | 100   | 102   | %          |
|                              | VSYS overvoltage falling threshold   | $V_{SYS\_REG} = 17\text{V}$   | 16.66 | 17    | 17.34 | V          |
|                              | VSYS overvoltage falling threshold   | $V_{SYS\_REG} = 8.6\text{V}$  | 8.31  | 8.6   | 8.78  | V          |
| $V_{SYS\_SHORT}$             | VSYS short voltage falling threshold   |   | 2.1   | 2.2   | 2.3   | V          |
| <b>BATTERY CHARGER</b>       |  |   |       |       |       |            |
| $V_{REG\_RANGE}$             | Typical charge voltage regulation range  |   | 3     |       | 18.8  | V          |
| $V_{REG\_STEP}$              | Typical charge voltage step  |   |       | 10    |       | mV         |
| $V_{REG\_ACC}$               | Charge voltage accuracy, $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$                          | $V_{REG} = 16.8\text{V}$  | -0.65 |       | 0.55  | %          |
|                              |  | $V_{REG} = 12.6\text{V}$  | -0.85 |       | 0.65  | %          |
|                              |  | $V_{REG} = 8.4\text{V}$   | -0.25 |       | 0.65  | %          |
|                              |  | $V_{REG} = 4.2\text{V}$   | -0.45 |       | 0.95  | %          |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER             |  | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNIT |
|-----------------------|--|---|------|------|------|------|
| $I_{CHG\_RANGE}$      | Typical charge current regulation range  |   | 0.05 |      | 5    | A    |
| $I_{CHG\_STEP}$       | Typical charge current regulation step   |   |      | 10   |      | mA   |
| $I_{CHG\_ACC}$        | Typical boost mode PWM charge current accuracy, $V_{BUS} < V_{BAT}$ , $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$                               | $I_{CHG} = 2.5\text{A}$ ; $V_{BAT}=8\text{V}$                           | -3   |      | 7    | %    |
|                       |  | $I_{CHG} = 2\text{A}$ ; $V_{BAT}=8\text{V}$                             | -2   |      | 8    | %    |
|                       |  | $I_{CHG} = 1.5\text{A}$ ; $V_{BAT}=8\text{V}$                           | 0    |      | 10   | %    |
|                       |  | $I_{CHG} = 1\text{A}$ ; $V_{BAT}=8\text{V}$                             | -2   |      | 8    | %    |
|                       |  | $I_{CHG} = 0.5\text{A}$ ; $V_{BAT}=8\text{V}$                           | -7.5 |      | 7.5  | %    |
| $I_{CHG\_ACC}$        | Typical buck mode PWM charge current accuracy, $V_{BUS} > V_{BAT}$ , $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$                                | $I_{CHG} = 4\text{A}$ ; $V_{BAT}=8\text{V}$                             | -5.5 |      | 2.5  | %    |
|                       |  | $I_{CHG} = 2\text{A}$ ; $V_{BAT}=8\text{V}$                             | -6.5 |      | 3.5  | %    |
|                       |  | $I_{CHG} = 1\text{A}$ ; $V_{BAT}=8\text{V}$                             | -5   |      | 5    | %    |
|                       |  | $I_{CHG} = 0.5\text{A}$ ; $V_{BAT}=8\text{V}$                           | -7.5 |      | 7.5  | %    |
| $I_{PRECHG\_RANGE}$   | Typical pre-charge current range   |   | 40   |      | 2000 | mA   |
| $I_{PRECHG\_STEP}$    | Typical pre-charge current step  |   |      | 40   |      | mA   |
| $I_{PRECHG\_ACC}$     | Typical LDO mode charge current accuracy when $V_{BATP}$ below $V_{SYSMIN}$ , $V_{BUS} < V_{BAT}$ , $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$ | $I_{PRECHG} = 480\text{mA}$ , $V_{BAT} = 6.5\text{V}$                   | -8   |      | 8    | %    |
|                       |  | $I_{PRECHG} = 200\text{mA}$ , $V_{BAT} = 6.5\text{V}$                   | -20  |      | 20   | %    |
|                       |  | $I_{PRECHG} = 120\text{mA}$ , $V_{BAT} = 6.5\text{V}$                   | -35  |      | 35   | %    |
| $I_{PRECHG\_ACC}$     | Typical LDO mode charge current accuracy when $V_{BATP}$ below $V_{SYSMIN}$ , $V_{BUS} > V_{BAT}$ , $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$ | $I_{PRECHG} = 1000\text{mA}$ , $V_{BAT} = 6.5\text{V}$                  | -4.5 |      | 3.5  | %    |
|                       |  | $I_{PRECHG} = 480\text{mA}$ , $V_{BAT} = 6.5\text{V}$                   | -8   |      | 8    | %    |
|                       |  | $I_{PRECHG} = 200\text{mA}$ , $V_{BAT} = 6.5\text{V}$                   | -20  |      | 20   | %    |
|                       |  | $I_{PRECHG} = 120\text{mA}$ , $V_{BAT} = 6.5\text{V}$                   | -30  |      | 30   | %    |
| $I_{TERM\_RANGE}$     | Typical termination current range  |   | 40   |      | 1000 | mA   |
| $I_{TERM\_STEP}$      | Typical termination current step   |   |      | 40   |      | mA   |
| $I_{TERM\_ACC}$       | Termination current accuracy, $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$   | $I_{TERM} = 120\text{mA}$ , $I_{CHG} < 1000\text{mA}$                   | -20  |      | 20   | %    |
|                       |  | $I_{TERM} = 480\text{mA}$ , $I_{CHG} > 1000\text{mA}$                   | -14  |      | 14   | %    |
| $V_{BAT\_SHORTZ}$     | Battery short voltage rising threshold to start pre-charge   | $V_{BAT}$ rising  |      | 2.25 |      | V    |
| $V_{BAT\_SHORT}$      | Battery short voltage falling threshold to stop pre-charge   | $V_{BAT}$ falling   |      | 2.06 |      | V    |
| $I_{BAT\_SHORT}$      | Battery short trickle charging current   | $V_{BAT} < V_{BAT\_SHORTZ}$   |      | 100  |      | mA   |
| $V_{BAT\_LOWV\_RISE}$ | Battery voltage rising threshold to start fast-charge, as percentage of $V_{REG}$  | $V_{BAT\_LOWV\_1:0}=00$   | 13   | 15   | 17   | %    |
|                       |  | $V_{BAT\_LOWV\_1:0}=01$   | 61.5 | 63.0 | 64.5 | %    |
|                       |  | $V_{BAT\_LOWV\_1:0}=10$   | 67.0 | 68.0 | 69.0 | %    |
|                       |  | $V_{BAT\_LOWV\_1:0}=11$   | 71.0 | 72.5 | 74.0 | %    |
| $V_{BAT\_LOWV\_HYS}$  | Battery voltage threshold hysteresis to stop fast-charge on falling edge   | $V_{BAT}$ falling, as percentage of $V_{REG}$ , $V_{BAT\_LOWV\_1:0}=11$ |      | 1.4  |      | %    |
| $V_{RECHG}$           | Battery recharge threshold   | $V_{BAT}$ falling, $V_{RECHG}=0011$ , $V_{REG}=8.4\text{V}$             |      | 200  |      | mV   |
|                       |  | $V_{BAT}$ falling, $V_{RECHG}=0111$ , $V_{REG}=16.8\text{V}$            |      | 400  |      | mV   |
| $I_{BAT\_LOAD}$       | Battery discharge load current   |   |      | 30   |      | mA   |
| $I_{SYS\_LOAD}$       | System discharge load current  |   |      | 30   |      | mA   |
| $R_{BATP}$            | BATP Input Resistance  |   |      | 2.5  |      | MΩ   |
| <b>BATFET</b>         |  |   |      |      |      |      |

## 8.5 Electrical Characteristics (continued)

 $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER                                 |  | TEST CONDITIONS  | MIN   | TYP   | MAX   | UNIT |
|---|--|--|-------|-------|-------|------|
| $V_{BATFET\_FWD}$                         | BATFET forward voltage in supplement mode                  | BAT discharging current 10mA   |       | 30    |       | mV   |
| $R_{BATFET}$                              | MOSFET on resistance from SYS to BAT                       |  |       | 8     |       | mΩ   |
| <b>BATTERY PROTECTIONS</b>                |  |  |       |       |       |      |
| $V_{BAT\_OVP}$                            | Battery overvoltage threshold                              | VBAT rising, as percentage of VREG                                       | 103   | 104   | 105   | %    |
|   |  | VBAT rising, VREG = 16.8V  | 17.30 | 17.47 | 17.64 | V    |
|   |  | VBAT rising, VREG = 8.4V   | 8.65  | 8.74  | 8.82  | V    |
|   |  | VBAT falling, as percentage of VREG                                      | 101   | 102   | 103   | %    |
|   |  | VBAT falling, VREG = 16.8V   | 16.97 | 17.14 | 17.30 | V    |
|   |  | VBAT falling, VREG = 8.4V  | 8.48  | 8.57  | 8.65  | V    |
| $V_{BAT\_SHORT}$                          | Battery short voltage                                      | VBAT falling, to clamp the charging current as trickle charging current. |       | 2.06  |       | V    |
|   |  | VBAT rising, to release the trickle charging current clamp               |       | 2.25  |       | V    |
| $I_{BAT\_OCP}$                            | Battery discharging over-current rising threshold          |  | 9.3   |       |       | A    |
| <b>INPUT VOLTAGE / CURRENT REGULATION</b> |  |  |       |       |       |      |
| $V_{INDPM\_RANGE}$                        | Typical input voltage regulation range                     |  | 3.6   |       | 22    | V    |
| $V_{INDPM\_STEP}$                         | Typical input voltage regulation step                      |  |       | 100   |       | mV   |
| $V_{INDPM\_ACC}$                          | Input voltage regulation accuracy                          | VINDPM=18.6V   | -2    |       | 2     | %    |
|   |  | VINDPM=10.6V   | -3    |       | 3     | %    |
|   |  | VINDPM=4.3V  | -5    |       | 5     | %    |
| $I_{INDPM\_RANGE}$                        | Typical input current regulation range                     |  | 0.1   |       | 3.3   | A    |
| $I_{INDPM\_STEP}$                         | Typical input current regulation step                      |  |       | 10    |       | mA   |
| $I_{INDPM\_ACC}$                          | Input current regulation accuracy                          | IINDPM = 500mA, VBUS=9V  | 415   | 460   | 500   | mA   |
|   |  | IINDPM = 1000mA, VBUS=9V   | 880   | 940   | 1000  | mA   |
|   |  | IINDPM = 2000mA, VBUS=9V   | 1800  | 1880  | 1960  | mA   |
|   |  | IINDPM = 3000mA, VBUS=9V   | 2720  | 2820  | 2920  | mA   |
| $V_{ILIM\_REG\_RNG}$                      | Voltage range for input current regulation at ILIM_HIZ pin |  | 1     |       | 4     | V    |
| $I_{LEAK\_ILIM}$                          | ILIM_HIZ pin leakage current                               | $V_{ILIM\_HIZ} = 4V$   | -1.5  |       | 1.5   | μA   |
| <b>D+ / D- DETECTION</b>                  |  |  |       |       |       |      |
| $V_{D+\_600MVSRC}$                        | D+ voltage source (600 mV)                                 |  | 500   | 600   | 700   | mV   |
| $I_{D+\_10UASRC}$                         | D+ current source (10 μA)                                  | $V_{D+} = 200\text{ mV}$ ,   | 7     | 10    | 14    | μA   |
| $I_{D+\_100UASNK}$                        | D+ current sink (100 μA)                                   | $V_{D+} = 500\text{ mV}$ ,   | 50    | 90    | 150   | μA   |
| $V_{D+\_0P325}$                           | D+ comparator threshold for Secondary Detection            | D+ pin rising, DPDM_NSCOMP2  | 250   |       | 400   | mV   |
| $V_{D+\_0P8}$                             | D+ comparator threshold for Data Contact Detection         | D+ pin rising, DPDM_NSCOMP2  | 775   | 850   | 925   | mV   |
| $I_{D+\_LKG}$                             | Leakage current into D+                                    | HIZ mode   | -1    |       | 1     | μA   |
| $V_{D-\_600MVSRC}$                        | D- voltage source (600 mV)                                 |  | 500   | 600   | 700   | mV   |
| $I_{D-\_100UASNK}$                        | D- current sink (100 μA)                                   | $V_{D-} = 500\text{ mV}$ ,   | 50    | 90    | 150   | μA   |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER         |  | TEST CONDITIONS                                     | MIN   | TYP  | MAX  | UNIT          |
|-------------------|--|---|-------|------|------|---------------|
| $V_{D\_0P325}$    | D- comparator threshold for Primary Detection    | D- pin Rising, DPDM_NSCOMP2                         | 250   |      | 400  | mV            |
| $I_{D\_LKG}$      | Leakage current into D-                          | HIZ mode  | -1    |      | 1    | $\mu\text{A}$ |
| $R_{D\_19K}$      | D- resistor to ground (19 k $\Omega$ )           | $V_{D\_} = 500\text{mV}$                            | 14.25 |      | 24.8 | k $\Omega$    |
| $V_{D+\_2p8\_hi}$ | D+ high comparator threshold for 2.8V detection  | D+ pin rising, DPDM_NSCOMP2                         | 2.85  | 3    | 3.1  | V             |
| $V_{D+\_2p8\_lo}$ | D+ low comparator threshold for 2.8V detection   | D+ pin rising, NSCMP1Z                              | 2.35  | 2.45 | 2.55 | V             |
| $V_{D+\_2p8}$     | D+ comparator threshold for non-standard adapter | (combined $V_{D+\_2p8\_hi}$ and $V_{D+\_2p8\_lo}$ ) | 2.55  |      | 2.85 | V             |
| $V_{D-\_2p8\_hi}$ | D- high comparator threshold for 2.8V detection  | D- pin rising, DPDM_NSCOMP2                         | 2.85  | 3    | 3.1  | V             |
| $V_{D-\_2p8\_lo}$ | D- low comparator threshold for 2.8V detection   | D- pin rising, NSCMP1Z                              | 2.35  | 2.45 | 2.55 | V             |
| $V_{D-\_2p8}$     | D- comparator threshold for non-standard adapter | (combined $V_{D-\_2p8\_hi}$ and $V_{D-\_2p8\_lo}$ ) | 2.55  |      | 2.85 | V             |
| $V_{D+\_2p0\_hi}$ | D+ high comparator threshold for 2.0V detection  | D+ pin rising, DPDM_NSCOMP2                         | 2.15  | 2.25 | 2.35 | V             |
| $V_{D+\_2p0\_lo}$ | D+ low comparator threshold for 2.0V detection   | D+ pin rising, NSCMP1Z                              | 1.6   | 1.7  | 1.85 | V             |
| $V_{D+\_2p0}$     | D+ comparator threshold for non-standard adapter | (combined $V_{D+\_2p0\_hi}$ and $V_{D+\_2p0\_lo}$ ) | 1.85  |      | 2.15 | V             |
| $V_{D-\_2p0\_hi}$ | D- high comparator threshold for 2.0V detection  | D- pin rising, DPDM_NSCOMP2                         | 2.15  | 2.25 | 2.35 | V             |
| $V_{D-\_2p0\_lo}$ | D- low comparator threshold for 2.0V detection   | D- pin rising, NSCMP1Z                              | 1.6   | 1.7  | 1.85 | V             |
| $V_{D-\_2p0}$     | D- comparator threshold for non-standard adapter | (combined $V_{D-\_2p0\_hi}$ and $V_{D-\_2p0\_lo}$ ) | 1.85  |      | 2.15 | V             |
| $V_{D+\_1p2\_hi}$ | D+ high comparator threshold for 1.2V detection  | D+ pin rising, DPDM_NSCOMP2                         | 1.35  | 1.5  | 1.6  | V             |
| $V_{D+\_1p2\_lo}$ | D+ low comparator threshold for 1.2V detection   | D+ pin rising, NSCPM1Z                              | 0.85  | 0.95 | 1.05 | V             |
| $V_{D+\_1p2}$     | D+ comparator threshold for non-standard adapter | (combined $V_{D+\_1p2\_hi}$ and $V_{D+\_1p2\_lo}$ ) | 1.05  |      | 1.35 | V             |
| $V_{D-\_1p2\_hi}$ | D- high comparator threshold for 1.2V detection  | D- pin rising, DPDM_NSCOMP2                         | 1.35  | 1.5  | 1.6  | V             |
| $V_{D-\_1p2\_lo}$ | D- low comparator threshold for 1.2V detection   | D- pin rising, NSCMP1Z                              | 0.85  | 0.95 | 1.05 | V             |
| $V_{D-\_1p2}$     | D- comparator threshold for non-standard adapter | (combined $V_{D-\_1p2\_hi}$ and $V_{D-\_1p2\_lo}$ ) | 1.05  |      | 1.35 | V             |

### THERMAL REGULATION AND THERMAL SHUTDOWN

|            |  |  |     |     |     |    |
|------------|--|--|-----|-----|-----|----|
| $T_{REG}$  | Junction temperature regulation accuracy | TREG = 120°C                           |     | 120 |     | °C |
|            |  | TREG = 100°C                           |     | 100 |     | °C |
|            |  | TREG = 80°C                            |     | 80  |     | °C |
|            |  | TREG = 60°C                            |     | 60  |     | °C |
| $T_{SHUT}$ | Thermal shutdown rising threshold        | Temperature increasing (TSHUT[1:0]=00) | 130 | 150 | 170 | °C |
|            |  | Temperature increasing (TSHUT[1:0]=01) | 110 | 130 | 150 | °C |
|            |  | Temperature increasing (TSHUT[1:0]=10) | 100 | 120 | 140 | °C |
|            |  | Temperature increasing (TSHUT[1:0]=11) | 65  | 85  | 105 | °C |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS  | MIN  | TYP  | MAX  | UNIT               |
|--|---|--|------|------|------|--------------------|
| $T_{SHUT\_HYS}$                                  | Thermal shutdown falling hysteresis                                       | Temperature decreasing by $T_{SHUT\_HYS}$                      |      | 30   |      | $^{\circ}\text{C}$ |
| <b>JEITA THERMISTOR COMPARATOR (CHARGE MODE)</b> |   |  |      |      |      |                    |
| $V_{T1\_RISE}$                                   | T1 comparator rising threshold. Charge is suspended above this voltage.   | As Percentage to REGN ( $0^{\circ}\text{C}$ w/ 103AT)          | 72.4 | 73.3 | 74.2 | %                  |
| $V_{T1\_FALL}$                                   | T1 comparator falling threshold. Charge is re-enabled below this voltage. | As Percentage to REGN ( $3^{\circ}\text{C}$ w/ 103AT)          | 71.5 | 72   | 72.5 | %                  |
| $V_{T2\_RISE}$                                   | T2 comparator rising threshold.   | As Percentage of REGN, JEITA_T2= $5^{\circ}\text{C}$ w/ 103AT  | 70.6 | 71.1 | 71.6 | %                  |
|  |   | As Percentage of REGN, JEITA_T2= $10^{\circ}\text{C}$ w/ 103AT | 67.9 | 68.4 | 68.9 | %                  |
|  |   | As Percentage of REGN, JEITA_T2= $15^{\circ}\text{C}$ w/ 103AT | 65.0 | 65.5 | 66.0 | %                  |
|  |   | As Percentage of REGN, JEITA_T2= $20^{\circ}\text{C}$ w/ 103AT | 61.9 | 62.4 | 62.9 | %                  |
| $V_{T2\_FALL}$                                   | T2 comparator falling threshold.  | As Percentage of REGN, JEITA_T2= $5^{\circ}\text{C}$ w/ 103AT  | 69.3 | 69.8 | 70.3 | %                  |
|  |   | As Percentage of REGN, JEITA_T2= $10^{\circ}\text{C}$ w/ 103AT | 66.6 | 67.1 | 67.6 | %                  |
|  |   | As Percentage of REGN, JEITA_T2= $15^{\circ}\text{C}$ w/ 103AT | 63.7 | 64.2 | 64.7 | %                  |
|  |   | As Percentage of REGN, JEITA_T2= $20^{\circ}\text{C}$ w/ 103AT | 60.6 | 61.1 | 61.6 | %                  |
| $V_{T3\_RISE}$                                   | T3 comparator rising threshold.   | As Percentage of REGN, JEITA_T3= $40^{\circ}\text{C}$ w/ 103AT | 49.2 | 49.7 | 50.2 | %                  |
|  |   | As Percentage of REGN, JEITA_T3= $45^{\circ}\text{C}$ w/ 103AT | 45.6 | 46.1 | 46.6 | %                  |
|  |   | As Percentage of REGN, JEITA_T3= $50^{\circ}\text{C}$ w/ 103AT | 42.0 | 42.5 | 43.0 | %                  |
|  |   | As Percentage of REGN, JEITA_T3= $55^{\circ}\text{C}$ w/ 103AT | 38.5 | 39   | 39.5 | %                  |
| $V_{T3\_FALL}$                                   | T3 comparator falling threshold.  | As Percentage of REGN, JEITA_T3= $40^{\circ}\text{C}$ w/ 103AT | 47.9 | 48.4 | 48.9 | %                  |
|  |   | As Percentage of REGN, JEITA_T3= $45^{\circ}\text{C}$ w/ 103AT | 44.3 | 44.8 | 45.3 | %                  |
|  |   | As Percentage of REGN, JEITA_T3= $50^{\circ}\text{C}$ w/ 103AT | 40.7 | 41.2 | 41.7 | %                  |
|  |   | As Percentage of REGN, JEITA_T3= $55^{\circ}\text{C}$ w/ 103AT | 37.2 | 37.7 | 38.2 | %                  |
| $V_{T5\_FALL}$                                   | T5 comparator falling threshold. Charge is suspended below this voltage.  | As Percentage of REGN ( $60^{\circ}\text{C}$ w/ 103AT)         | 33.7 | 34.2 | 34.7 | %                  |
| $V_{T5\_RISE}$                                   | T5 comparator rising threshold. Charge is re-enabled above this voltage.  | As Percentage of REGN ( $58^{\circ}\text{C}$ w/ 103AT)         | 35   | 35.5 | 36   | %                  |



## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER                                   |  | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNIT |
|---|--|---|------|------|------|------|
| COLD / HOT THERMISTOR COMPARATOR (OTG MODE) |  |   |      |      |      |      |
| V <sub>BCOLD_RISE</sub>                     | TCOLD comparator rising threshold.                                     | As Percentage of REGN (–20°C w/ 103AT)                    | 79.5 | 80.0 | 80.5 | %    |
|   |  | As Percentage of REGN (–10°C w/ 103AT)                    | 76.6 | 77.1 | 77.6 | %    |
| V <sub>BCOLD_FALL</sub>                     | TCOLD comparator falling threshold.                                    | As Percentage of REGN (–20°C w/ 103AT)                    | 78.2 | 78.7 | 79.2 | %    |
|   |  | As Percentage of REGN (–10°C w/ 103AT)                    | 75.3 | 75.8 | 76.3 | %    |
| V <sub>BHOT_FALL</sub>                      | THOT comparator falling threshold.                                     | As Percentage of REGN, (55°C w/ 103AT)                    | 37.2 | 37.7 | 38.2 | %    |
|   |  | As Percentage of REGN, (60°C w/ 103AT)                    | 33.9 | 34.4 | 34.9 | %    |
|   |  | As Percentage of REGN, (65°C w/ 103AT)                    | 30.8 | 31.3 | 31.8 | %    |
| V <sub>BHOT_RISE</sub>                      | THOT comparator rising threshold.                                      | As Percentage of REGN, (55°C w/ 103AT)                    | 38.8 | 39.3 | 39.8 | %    |
|   |  | As Percentage of REGN, (60°C w/ 103AT)                    | 35.2 | 35.7 | 36.2 | %    |
|   |  | As Percentage of REGN, (65°C w/ 103AT)                    | 32.0 | 32.5 | 33.0 | %    |
| SWITCHING CONVERTER                         |  |   |      |      |      |      |
| F <sub>SW</sub>                             | PWM switching frequency  | Oscillator frequency                                      | 1.5  |      | MHz  |      |
|   |  |   | 750  |      | kHz  |      |
| I <sub>IN_SS</sub>                          | Input current limit during converter start up                          | VSYS below 2.2V, IINDPM above 500mA                       | 500  |      | mA   |      |
| V <sub>BTST_REFRESH</sub>                   | Bootstrap refresh comparator threshold                                 | VBST1-VSW1 when Q2 refresh pulse is requested, VBUS = 15V | 2.5  | 3.0  | 3.6  | V    |
|   |  | VBST2-VSW2 when Q3 refresh pulse is requested, VBUS = 15V | 2.5  | 3.0  | 3.6  | V    |
| V <sub>F_D</sub>                            | Integrated BTST diode forward bias voltage                             | IF=20mA at 25 °C  | 0.8  |      | V    |      |
|   |  |   | 0.8  |      | V    |      |
| V <sub>R_D</sub>                            | Integrated BTST diode reverse breakdown voltage                        | IR=2μA at 25 °C   | 20   |      | V    |      |
|   |  |   | 20   |      | V    |      |
| SENSE RESISTANCE and MOSFET Rdson           |  |   |      |      |      |      |
| R <sub>SNS</sub>                            | VBUS to PMID input sensing resistance                                  | T <sub>J</sub> = -40°C-85°C (typical value is under 25°C) | 6    |      | mΩ   |      |
| R <sub>Q1_ON</sub>                          | Buck high-side switching MOSFET turnon resistance between PMID and SW1 | T <sub>J</sub> = -40°C-85°C (typical value is under 25°C) | 24   |      | mΩ   |      |
| R <sub>Q2_ON</sub>                          | Buck low-side switching MOSFET turnon resistance between SW1 and PGND  | T <sub>J</sub> = -40°C-85°C (typical value is under 25°C) | 35   |      | mΩ   |      |
| R <sub>Q3_ON</sub>                          | Boost low-side switching MOSFET turnon resistance between SW2 and PGND | T <sub>J</sub> = -40°C-85°C (typical value is under 25°C) | 28   |      | mΩ   |      |
| R <sub>Q4_ON</sub>                          | Boost high-side switching MOSFET turnon resistance between SW2 and SYS | T <sub>J</sub> = -40°C-85°C (typical value is under 25°C) | 17   |      | mΩ   |      |
| MOSFET CYCLE-BY-CYCLE CURRENT LIMIT         |  |   |      |      |      |      |
| I <sub>Q1_CBC</sub>                         | Q1 cycle by cycle current limit  |   | 7.5  |      | A    |      |



## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER   |   | TEST CONDITIONS  | MIN  | TYP | MAX  | UNIT |
|---|---|--|------|-----|------|------|
| I <sub>Q2_CBC</sub>   | Q2 cycle by cycle current limit             |  | 10   |     |      | A    |
| I <sub>Q3_CBC</sub>   | Q3 cycle by cycle current limit             |  | 10   |     |      | A    |
| I <sub>Q4_CBC</sub>   | Q4 cycle by cycle current limit             |  | 7.5  |     |      | A    |
| OTG MODE CONVERTER  |   |  |      |     |      |      |
| V <sub>OTG_RANGE</sub>  | Typical OTG mode voltage regulation range   |  | 2.8  |     | 22   | V    |
| V <sub>OTG_STEP</sub>   | Typical OTG mode voltage regulation step    |  |      | 10  |      | mV   |
| V <sub>OTG_ACC</sub>  |   | IVBUS = 0A, VOTG = 20V                                   | -3.5 |     | 3    | %    |
|   |   | IVBUS = 0A, VOTG = 12V                                   | -3.5 |     | 3    | %    |
|   |   | IVBUS = 0A, VOTG = 5V                                    | -3.5 |     | 3    | %    |
| I <sub>OTG_RANGE</sub>  | Typical OTG mode current regulation range   |  | 0.12 |     | 3.32 | A    |
| I <sub>OTG_STEP</sub>   | Typical OTG mode current regulation step    |  |      | 40  |      | mA   |
| I <sub>OTG_ACC</sub>  | OTG mode current regulation accuracy        | IOTG = 3.0A  | -2.2 |     | 2.2  | %    |
|   |   | IOTG = 1.52A   | -5   |     | 3    | %    |
|   |   | IOTG = 0.52A   | -15  |     | 8    | %    |
| V <sub>OTG_UVP</sub>  | OTG mode under voltage falling threshold    |  | 2.1  | 2.2 | 2.3  | V    |
| V <sub>OTG_OVP</sub>  | OTG mode overvoltage rising threshold       | As percentage of VOTG regulation, OTG mode OOA disabled. | 104  | 113 | 120  | %    |
|   | OTG mode overvoltage falling threshold      | As percentage of VOTG regulation                         | 90   | 98  | 104  | %    |
| I <sub>OTG_BAT</sub>  | Battery current regulation in OTG mode      | IBAT_REG_1:0 = 00, VBAT=8V, VOTG=9V                      | 2.8  | 3   | 3.2  | A    |
|   |   | IBAT_REG_1:0 = 01, VBAT=8V, VOTG=9V                      | 3.8  | 4   | 4.2  | A    |
|   |   | IBAT_REG_1:0 = 10, VBAT=8V, VOTG=9V                      | 4.8  | 5   | 5.3  | A    |
| REGN LDO  |   |  |      |     |      |      |
| V <sub>REGN</sub>   | REGN LDO output voltage                     | V <sub>VBUS</sub> = 5V, I <sub>REGN</sub> = 20mA         | 4.6  | 4.8 | 5    | V    |
|   |   | V <sub>VBUS</sub> = 15V, I <sub>REGN</sub> = 20mA        | 4.8  | 5   | 5.2  | V    |
| I <sub>REGN</sub>   | REGN LDO current limit                      | V <sub>VBUS</sub> = 5V, V <sub>REGN</sub> = 4.5V         | 30   |     |      | mA   |
| I2C INTERFACE (SCL, SDA)  |   |  |      |     |      |      |
| V <sub>IH_SDA</sub>   | Input high threshold level, SDA             | Pull up rail 1.8V  | 1.3  |     |      | V    |
| V <sub>IL_SDA</sub>   | Input low threshold level                   | Pull up rail 1.8V  |      |     | 0.4  | V    |
| V <sub>OL_SDA</sub>   | Output low threshold level                  | Sink current = 5mA                                       |      |     | 0.4  | V    |
| I <sub>BIAS_SDA</sub>   | High-level leakage current                  | Pull up rail 1.8V  |      |     | 1    | μA   |
| V <sub>IH_SCL</sub>   | Input high threshold level, SDA             | Pull up rail 1.8V  | 1.3  |     |      | V    |
| V <sub>IL_SCL</sub>   | Input low threshold level                   | Pull up rail 1.8V  |      |     | 0.4  | V    |
| V <sub>OL_SCL</sub>   | Output low threshold level                  | Sink current = 5mA                                       |      |     | 0.4  | V    |
| I <sub>BIAS_SCL</sub>   | High-level leakage current                  | Pull up rail 1.8V  |      |     | 1    | μA   |
| LOGIC I PIN ( $\overline{CE}$ , I <sub>LIM_HIZ</sub> , $\overline{QON}$ ) |   |  |      |     |      |      |
| V <sub>IH_CE</sub>  | Input high threshold level, $\overline{CE}$ |  | 1.3  |     |      | V    |
| V <sub>IL_CE</sub>  | Input low threshold level, $\overline{CE}$  |  |      |     | 0.4  | V    |
| I <sub>IN_BIAS_CE</sub>   | High-level leakage current, $\overline{CE}$ | Pull up rail 1.8V  |      |     | 1    | μA   |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

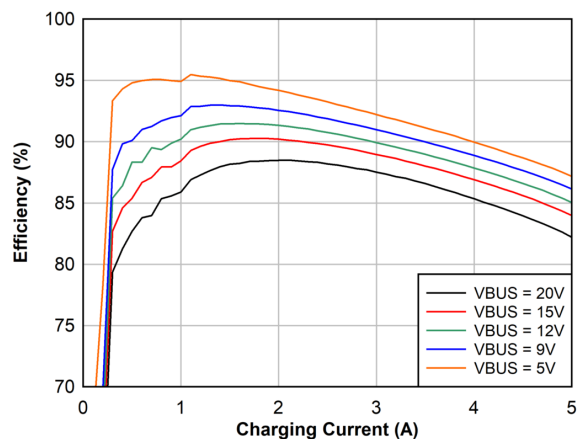
| PARAMETER                                |  | TEST CONDITIONS                          | MIN | TYP   | MAX  | UNIT |
|--|--|--|-----|-------|------|------|
| V <sub>IH_QON</sub>                      | Input high threshold level, $\overline{QON}$     |  | 1.3 |       |      | V    |
| V <sub>IL_QON</sub>                      | Input low threshold level, $\overline{QON}$      |  |     |       | 0.4  | V    |
| V <sub>QON</sub>                         | Internal $\overline{QON}$ pull up                | $\overline{QON}$ is pulled up internally |     | 3.2   |      | V    |
| R <sub>QON</sub>                         | Internal $\overline{QON}$ pull up resistance     |  |     | 200   |      | kΩ   |
| V <sub>IH_ILIM_HIZ</sub>                 | Input high threshold level, ILIM_HIZ             |  | 1   |       |      | V    |
| V <sub>IL_ILIM_HIZ</sub>                 | Input low threshold level, ILIM_HIZ              |  |     |       | 0.75 | V    |
| LOGIC O PIN ( $\overline{INT}$ , STAT)   |  |  |     |       |      |      |
| V <sub>OL_INT</sub>                      | Output low threshold level, $\overline{INT}$     | Sink current = 5mA                       |     |       | 0.4  | V    |
| I <sub>OUT_BIAS_INT</sub>                | High-level leakage current, $\overline{INT}$     | Pull up rail 1.8V                        |     |       | 1    | μA   |
| V <sub>OL_STAT</sub>                     | Output low threshold level, STAT                 | Sink current = 5mA                       |     |       | 0.4  | V    |
| I <sub>OUT_BIAS_STAT</sub>               | High-level leakage current, STAT                 | Pull up rail 1.8V                        |     |       | 1    | μA   |
| ADC MEASUREMENT ACCURACY AND PERFORMANCE |  |  |     |       |      |      |
| t <sub>ADC_CONV</sub>                    | Conversion time, each measurement                | ADC_SAMPLE[1:0] = 00                     |     | 24    |      | ms   |
|  |  | ADC_SAMPLE[1:0] = 01                     |     | 12    |      | ms   |
|  |  | ADC_SAMPLE[1:0] = 10                     |     | 6     |      | ms   |
|  |  | ADC_SAMPLE[1:0] = 11 (Not Recommended)   |     | 3     |      | ms   |
| ADC <sub>RES</sub>                       | Effective resolution                             | ADC_SAMPLE[1:0] = 00                     | 14  | 15    |      | bits |
|  |  | ADC_SAMPLE[1:0] = 01                     | 13  | 14    |      | bits |
|  |  | ADC_SAMPLE[1:0] = 10                     | 12  | 13    |      | bits |
|  |  | ADC_SAMPLE[1:0] = 11 (Not Recommended)   | 10  | 11    |      | bits |
| ADC MEASUREMENT RANGE AND LSB            |  |  |     |       |      |      |
| ADC <sub>IBUS_RANGE</sub>                | ADC VBUS current reading range (forward and OTG) | Range                                    | 0   |       | 5    | A    |
| ADC <sub>IBUS_STEP</sub>                 | ADC VBUS current reading step (forward and OTG)  | LSB                                      |     | 1     |      | mA   |
| ADC <sub>VBUS_RANGE</sub>                | ADC VBUS voltage reading range                   | Range                                    | 0   |       | 30   | V    |
| ADC <sub>VBUS_STEP</sub>                 | ADC VBUS voltage reading step                    | LSB                                      |     | 1     |      | mV   |
| ADC <sub>VAC_RANGE</sub>                 | ADC VAC voltage reading range                    | Range                                    | 0   |       | 30   | V    |
| ADC <sub>VAC_STEP</sub>                  | ADC VAC voltage reading step                     | LSB                                      |     | 1     |      | mV   |
| ADC <sub>VBAT_RANGE</sub>                | ADC BAT voltage reading range                    | Range                                    | 0   |       | 20   | V    |
| ADC <sub>VBAT_STEP</sub>                 | ADC BAT voltage reading step                     | LSB                                      |     | 1     |      | mV   |
| ADC <sub>VSYS_RANGE</sub>                | ADC SYS voltage reading range                    | Range                                    | 0   |       | 24   | V    |
| ADC <sub>VSYS_STEP</sub>                 | ADC SYS voltage reading step                     | LSB                                      |     | 1     |      | mV   |
| ADC <sub>IBAT_RANGE</sub>                | ADC BAT current reading range                    | Range                                    | 0   |       | 8    | A    |
| ADC <sub>IBAT_STEP</sub>                 | ADC BAT current reading step                     | LSB                                      |     | 1     |      | mA   |
| ADC <sub>TS_RANGE</sub>                  | ADC TS voltage reading range                     | Range                                    | 0   |       | 99.9 | %    |
| ADC <sub>TS_STEP</sub>                   | ADC TS voltage reading step                      | LSB                                      |     | 0.098 |      | %    |
| ADC <sub>TDIE_RANGE</sub>                | ADC die temperature reading range                | Range                                    | -40 |       | 150  | °C   |
| ADC <sub>TDIE_STEP</sub>                 | ADC die temperature reading step                 | LSB                                      |     | 0.5   |      | °C   |

## 8.6 Timing Requirements

| PARAMETER                  |                                       | TEST CONDITIONS             | MIN  | NOM | MAX  | UNIT |
|----------------------------|---------------------------------------|-----------------------------|------|-----|------|------|
| BATTERY CHARGER            |                                       |                             |      |     |      |      |
| t <sub>TOP_OFF</sub>       | Top-off timer accuracy                |                             | 12   | 15  | 18   | min  |
|                            |                                       |                             | 24   | 30  | 36   | min  |
|                            |                                       |                             | 36   | 45  | 54   | min  |
| t <sub>SAFETY_TRKCHG</sub> | Charge safety timer in trickle charge |                             | 0.9  | 1   | 1.1  | hr   |
| t <sub>SAFETY_PRECHG</sub> | Charge safety timer in pre-charge     | PRECHG_TMR = 0              | 1.8  | 2   | 2.2  | hr   |
| t <sub>SAFETY</sub>        | Charge safety timer accuracy          | CHG_TMR[1:0] = 00           | 4.5  | 5   | 5.5  | hr   |
|                            |                                       | CHG_TMR[1:0] = 01           | 7.2  | 8   | 8.8  | hr   |
|                            |                                       | CHG_TMR[1:0] = 10           | 10.8 | 12  | 13.2 | hr   |
|                            |                                       | CHG_TMR[1:0] = 11           | 21.6 | 24  | 26.4 | hr   |
| I2C INTERFACE              |                                       |                             |      |     |      |      |
| f <sub>SCL</sub>           | SCL clock frequency                   |                             | 1000 |     |      | KHZ  |
| WATCHDOG TIMER             |                                       |                             |      |     |      |      |
| t <sub>LP_WDT</sub>        | Watchdog reset time                   | EN_HIZ = 1, WATCHDOG = 160s | 100  | 160 | s    |      |
| t <sub>WDT</sub>           | Watchdog reset time                   | EN_HIZ = 0, WATCHDOG = 160s | 136  | 160 | s    |      |

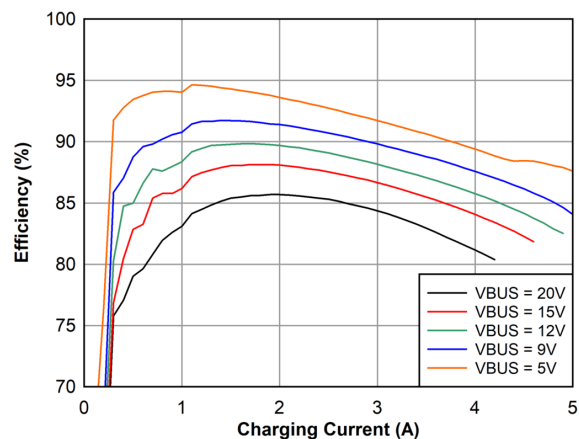
## 8.7 Typical Characteristics

$C_{VBUS} = 2 \times 10 \mu\text{F}$ ,  $C_{PMID} = 3 \times 10 \mu\text{F}$ ,  $C_{SYS} = 5 \times 10 \mu\text{F}$ ,  $C_{BAT} = 2 \times 10 \mu\text{F}$ ,  $L1 = 1 \mu\text{H}$  (SPM6530T-1R0M120) and  $L2 = 2.2 \mu\text{H}$  (WE-LHMI-74437346022)



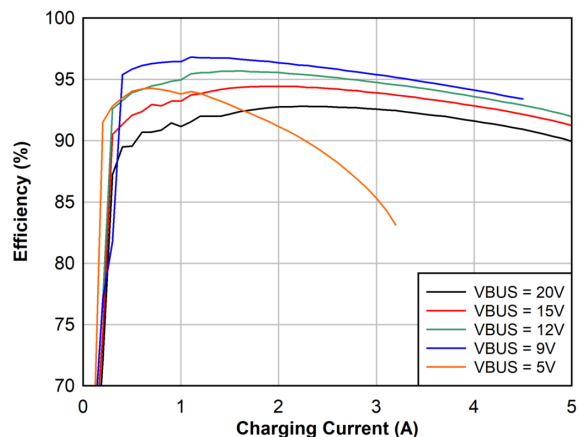
VBAT = 4V, Fsw = 750 kHz with L2 = 2.2  $\mu\text{H}$ , PFM disabled

**Figure 8-1. 1s Battery Charge Efficiency, 750 kHz**



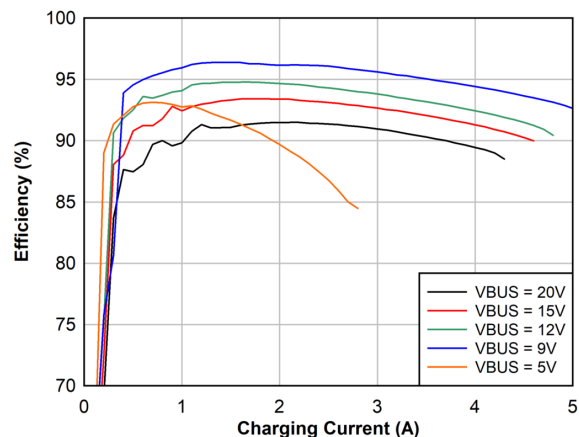
VBAT = 4V, Fsw = 1.5 MHz with L1 = 1.0  $\mu\text{H}$ , PFM disabled

**Figure 8-2. 1s Battery Charge Efficiency, 1.5 MHz**



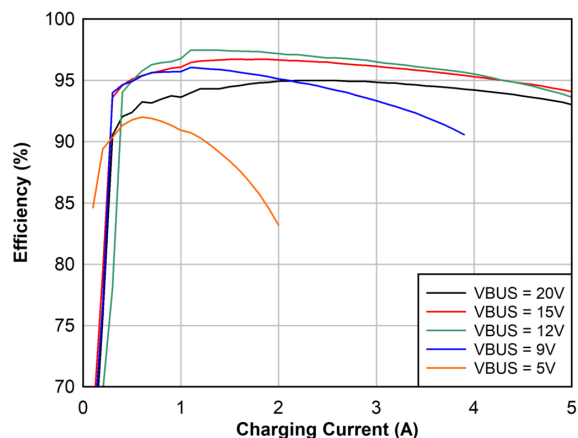
VBAT = 8V, Fsw = 750 kHz with L2 = 2.2  $\mu\text{H}$ , PFM disabled

**Figure 8-3. 2s Battery Charge Efficiency, 750 kHz**



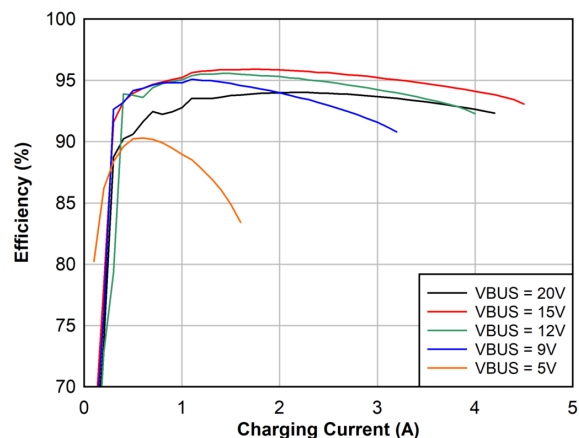
VBAT = 8V, Fsw = 1.5 MHz with L1 = 1  $\mu\text{H}$ , PFM disabled

**Figure 8-4. 2s Battery Charge Efficiency, 1.5 MHz**



VBAT = 12V, Fsw = 750 kHz with L2 = 2.2  $\mu\text{H}$ , PFM disabled

**Figure 8-5. 3s Battery Charge Efficiency, 750 kHz**

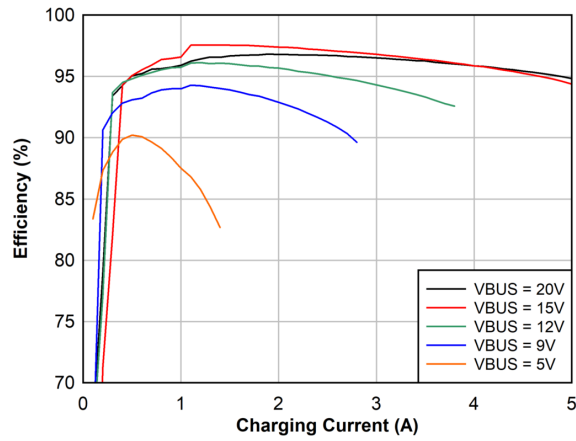


VBAT = 12V, Fsw = 1.5 MHz with L1 = 1  $\mu\text{H}$ , PFM disabled

**Figure 8-6. 3s Battery Charge Efficiency, 1.5 MHz**

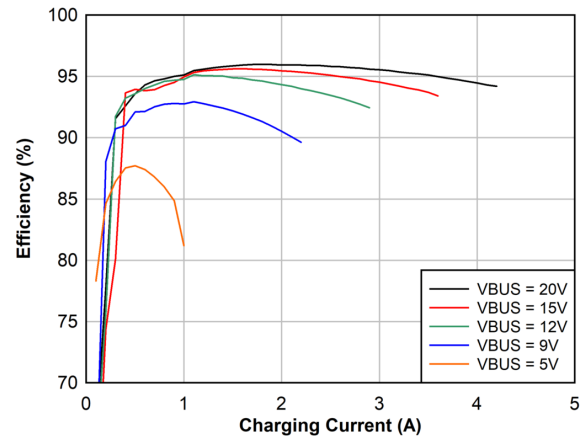
## 8.7 Typical Characteristics (continued)

$C_{VBUS} = 2 \times 10 \mu\text{F}$ ,  $C_{PMID} = 3 \times 10 \mu\text{F}$ ,  $C_{SYS} = 5 \times 10 \mu\text{F}$ ,  $C_{BAT} = 2 \times 10 \mu\text{F}$ ,  $L1 = 1 \mu\text{H}$  (SPM6530T-1R0M120) and  $L2 = 2.2 \mu\text{H}$  (WE-LHMI-74437346022)



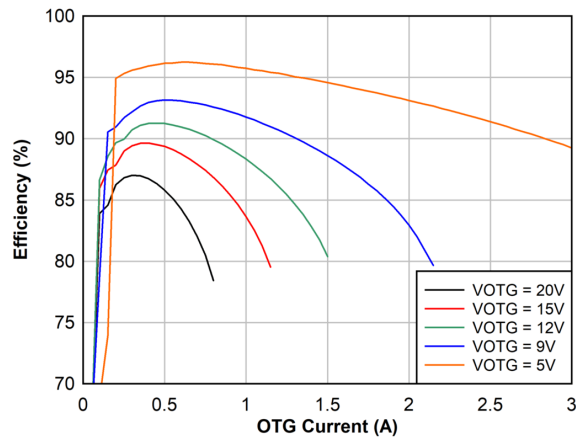
$V_{BAT} = 16\text{V}$ ,  $F_{sw} = 750 \text{ kHz}$  with  $L2 = 2.2 \mu\text{H}$ , PFM disabled

**Figure 8-7. 4s Battery Charge Efficiency, 750 kHz**



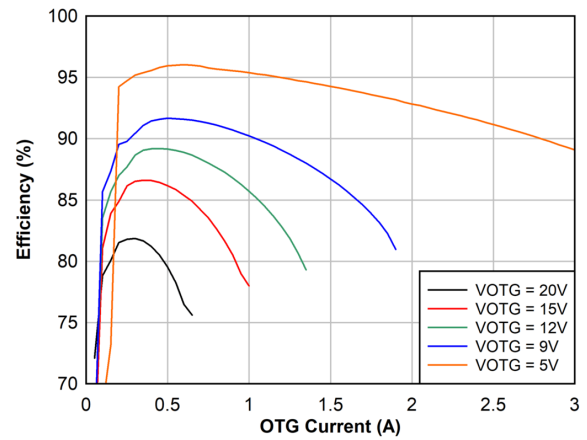
$V_{BAT} = 16\text{V}$ ,  $F_{sw} = 1.5 \text{ MHz}$  with  $L1 = 1 \mu\text{H}$ , PFM disabled

**Figure 8-8. 4s Battery Charge Efficiency, 1.5 MHz**



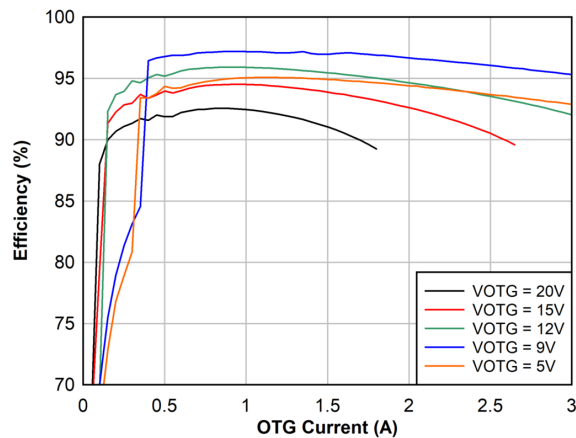
$V_{BAT} = 4.2\text{V}$ ,  $F_{sw} = 750 \text{ kHz}$  with  $L2 = 2.2 \mu\text{H}$ , PFM disabled

**Figure 8-9. 1s Battery OTG Efficiency, 750 kHz**



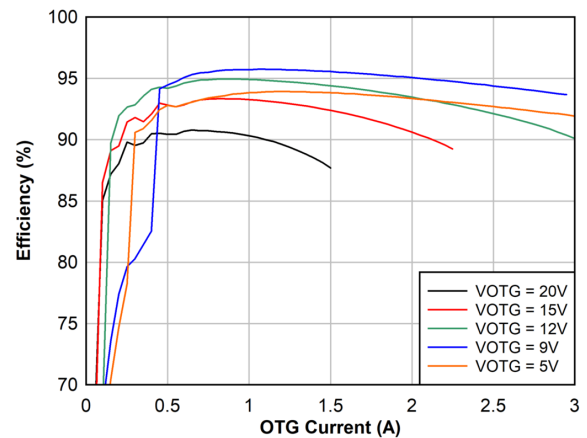
$V_{BAT} = 4.2\text{V}$ ,  $F_{sw} = 1.5 \text{ MHz}$  with  $L1 = 1 \mu\text{H}$ , PFM disabled

**Figure 8-10. 1s Battery OTG Efficiency, 1.5 MHz**



$V_{BAT} = 8.4\text{V}$ ,  $F_{sw} = 750 \text{ kHz}$  with  $L2 = 2.2 \mu\text{H}$ , PFM disabled

**Figure 8-11. 2s Battery OTG Efficiency, 750 kHz**

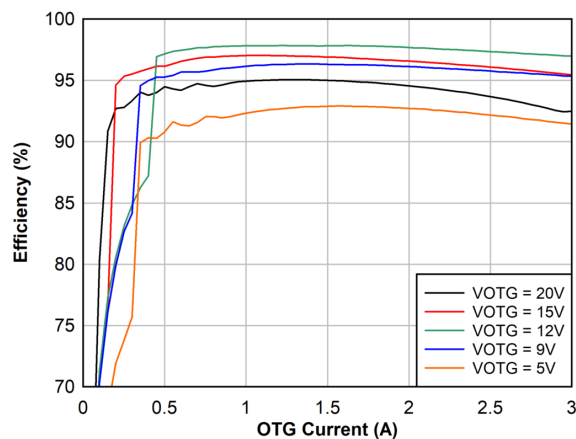


$V_{BAT} = 8.4\text{V}$ ,  $F_{sw} = 1.5 \text{ MHz}$  with  $L1 = 1 \mu\text{H}$ , PFM disabled

**Figure 8-12. 2s Battery OTG Efficiency, 1.5 MHz**

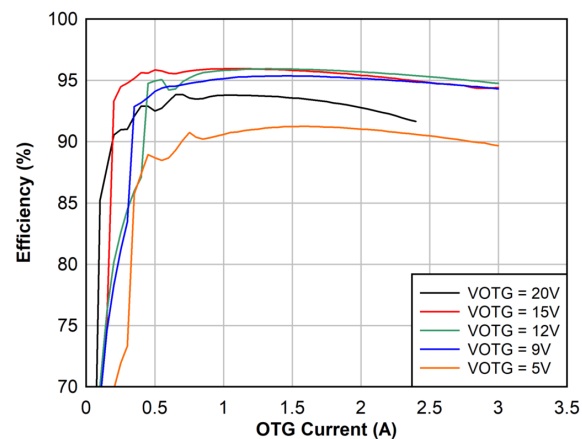
## 8.7 Typical Characteristics (continued)

$C_{VBUS} = 2 \times 10 \mu\text{F}$ ,  $C_{PMID} = 3 \times 10 \mu\text{F}$ ,  $C_{SYS} = 5 \times 10 \mu\text{F}$ ,  $C_{BAT} = 2 \times 10 \mu\text{F}$ ,  $L1 = 1 \mu\text{H}$  (SPM6530T-1R0M120) and  $L2 = 2.2 \mu\text{H}$  (WE-LHMI-74437346022)



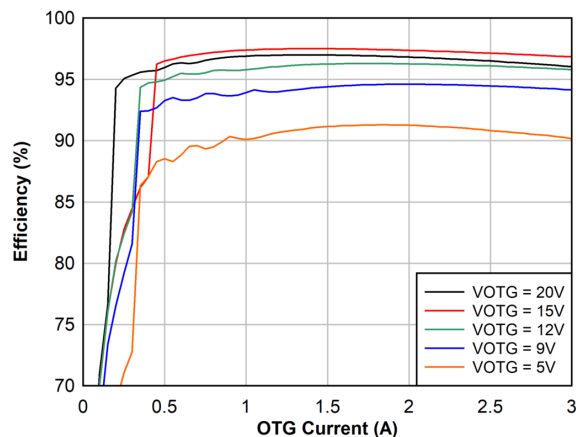
VBAT = 12.6V, Fsw = 750 kHz with L2 = 2.2  $\mu\text{H}$ , PFM disabled

**Figure 8-13. 3s Battery OTG Efficiency, 750 kHz**



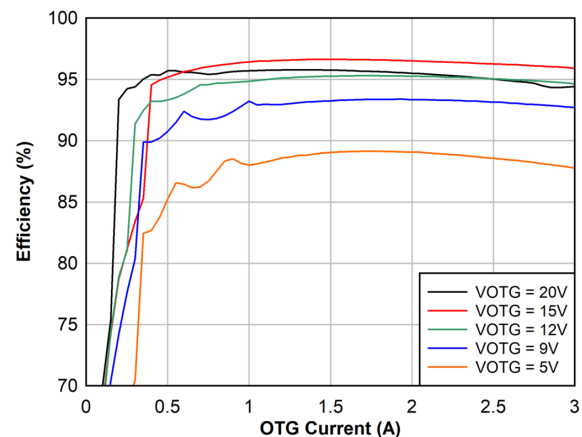
VBAT = 12.6V, Fsw = 1.5 MHz with L1 = 1  $\mu\text{H}$ , PFM disabled

**Figure 8-14. 3s Battery OTG Efficiency, 1.5 MHz**



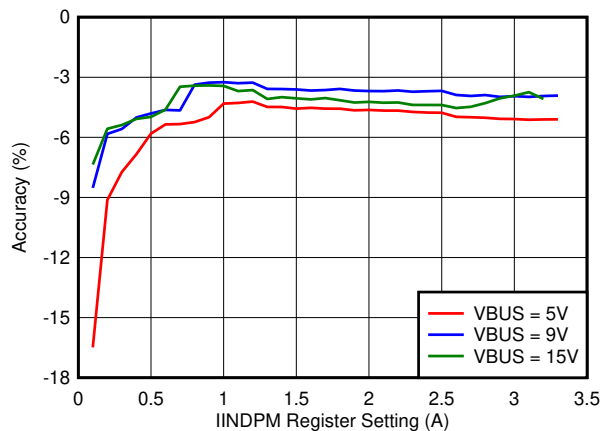
VBAT = 16.8V, Fsw = 750 kHz with L2 = 2.2  $\mu\text{H}$ , PFM disabled

**Figure 8-15. 4s Battery OTG Efficiency, 750 kHz**



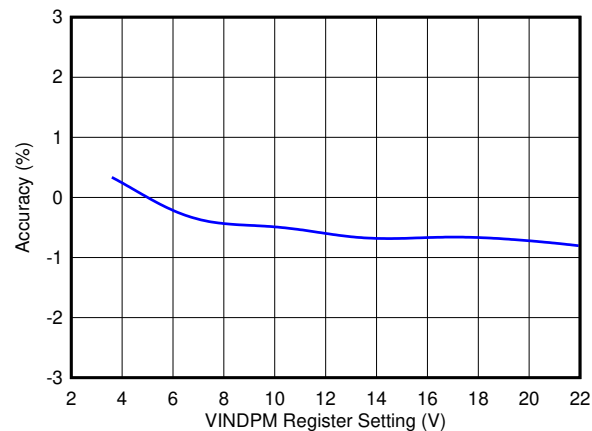
VBAT = 16.8V, Fsw = 1.5 MHz with L1 = 1  $\mu\text{H}$ , PFM disabled

**Figure 8-16. 4s Battery OTG Efficiency, 1.5 MHz**



VBAT = 8V, Fsw = 1.5MHz with L1 = 1  $\mu\text{H}$

**Figure 8-17. Input Current Regulation (IINDPM) Accuracy**

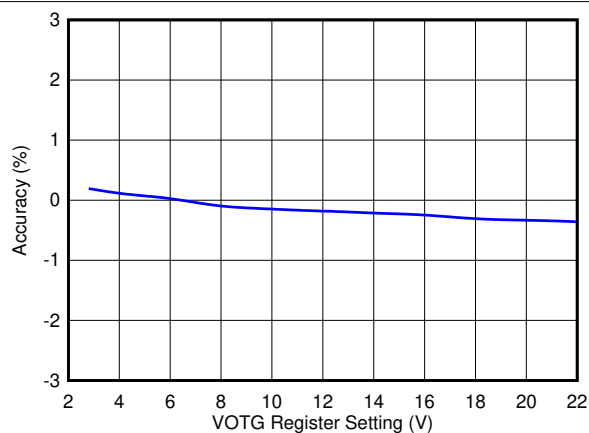


VBAT = 8V, Fsw = 1.5MHz with L1 = 1  $\mu\text{H}$

**Figure 8-18. Input Voltage Regulation (VINDPM) Accuracy**

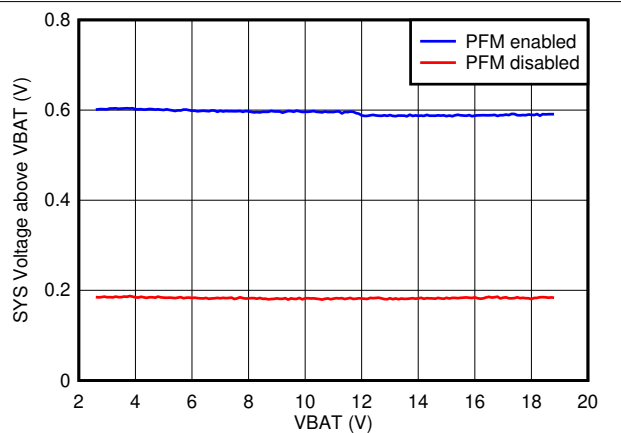
## 8.7 Typical Characteristics (continued)

$C_{VBUS} = 2 \times 10 \mu\text{F}$ ,  $C_{PMID} = 3 \times 10 \mu\text{F}$ ,  $C_{SYS} = 5 \times 10 \mu\text{F}$ ,  $C_{BAT} = 2 \times 10 \mu\text{F}$ ,  $L1 = 1 \mu\text{H}$  (SPM6530T-1R0M120) and  $L2 = 2.2 \mu\text{H}$  (WE-LHMI-74437346022)



$VBAT = 8.4\text{V}$ ,  $F_{sw} = 1.5\text{MHz}$  with  $L1 = 1 \mu\text{H}$

**Figure 8-19. OTG Voltage Regulation (VOTG) Accuracy**



$VBUS = 9\text{V}$ ,  $F_{sw} = 1.5\text{MHz}$  with  $L1 = 1 \mu\text{H}$ ,  $I_{SYS} = 0\text{A}$ , Charge Disabled

**Figure 8-20. Offset Voltage of SYS Regulation above VBAT**

## 9 Detailed Description

### 9.1 Overview

The BQ25792 is a fully integrated, switch-mode buck-boost charger for a 1 cell ~ 4 cell Li-ion battery and Li-polymer battery. For compact design and minimum component count, the charger integrates the 4 switching MOSFETs (Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub>, Q<sub>4</sub>), input and charging current sensing circuits, the battery FET (BATFET) and all the loop compensation of the buck-boost converter. It provides high power density and design flexibility to charge batteries across the full input voltage range for USB Type-C™ and USB-PD applications such as digital cameras, drones and mobile printers.

The charger supports narrow VDC (NVDC) power path management, in which the system is regulated at a voltage slightly higher than the battery voltage, without dropping below a configurable minimum system voltage. The system keeps operating even when the battery is completely discharged or removed. When load power exceeds the input source rating, the battery gets into supplement mode and prevents the input source from being overloaded and the system from crashing.

The device charges a battery from a wide range of input sources including legacy USB adapter to high voltage USB-PD adapter and traditional barrel adapter. The charger seamlessly transitions between buck, boost and buck-boost modes based on input voltage and battery voltage without host control. The optional dual-input source selector manages the power flowing from two different input sources, prioritizing the first available input source. The host may manually transition between input sources using I<sup>2</sup>C.

To support fast charging using adjustable high voltage adapter (HVDCP), the device provides D+/D- handshake. The device is compliant with USB 2.0 and USB 3.0 power delivery specification with input current and voltage regulation. In addition, the Input Current Optimizer (ICO) allows the detection of maximum power point of an unknown input source.

In addition to the I<sup>2</sup>C host controlled charging mode, BQ25792 also supports autonomous charging mode. After power up, the charging is defaulted enabled with all the registers default settings. The device can complete a charging cycle without any software engagements. It detects battery voltage and charges the battery in different phases: trickle charging, pre-charging, constant current (CC) charging and constant voltage (CV) charging. At the end of the charging cycle, the charger automatically terminates when the charge current is below a pre-set limit (termination current) in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

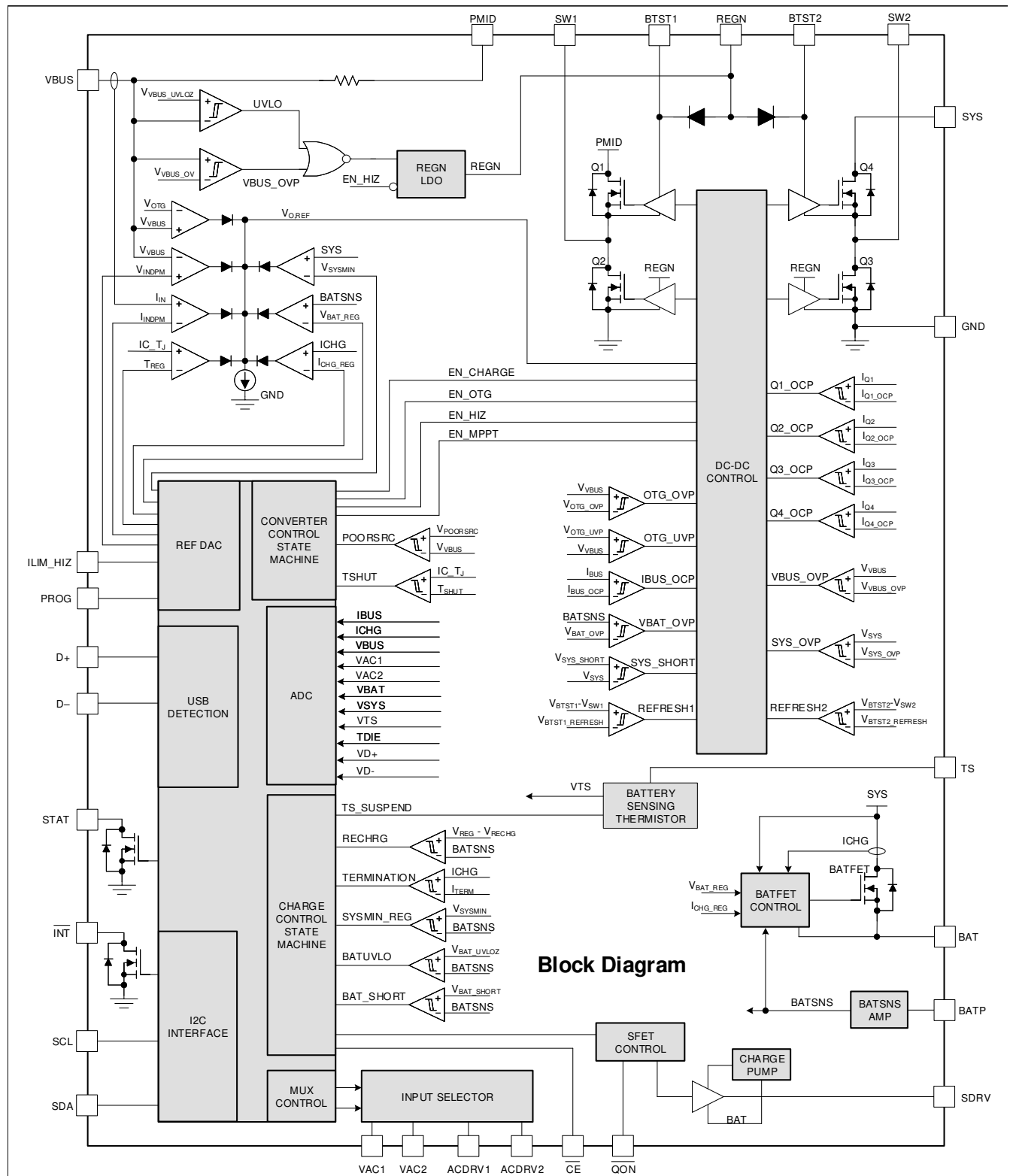
In the absence of input sources, BQ25792 supports USB On-the-Go (OTG) function, discharging the battery to generate an adjustable 2.8V~22V voltage on VBUS with 10mV step size. This is compliant with the USB PD 3.0 specification defined PPS feature.

The charger provides various safety features for battery charging and system operations, including battery temperature negative thermistor (NTC) monitoring, trickle charge, pre-charge and fast charge timers and over-voltage/over-current protections on the battery and the charger power input pin. The thermal regulation reduces charge current when the die temperature exceeds a programmable threshold. The STAT output of the device reports the charging status and any fault conditions. The  $\overline{\text{INT}}$  pin immediately notifies the host when a fault occurs.

The device also provides a 16-bit analog-to-digital converter (ADC) for monitoring charge current and input/battery/system voltages, the TS pin voltage and the die temperature. It is available in a 29-pin 4.0 mm x 4.0 mm QFN package.



## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Device Power-On-Reset

The internal bias circuits of the BQ25792 are powered from the higher of either  $V_{VBUS}$  or  $V_{BAT}$  through an integrated power selector. The valid voltage to power up the device has to be greater than  $V_{VBUS\_UVLOZ}$  when powering from VBUS or  $V_{BAT\_UVLOZ}$  when powering from BAT. When  $V_{VBUS} < V_{VBUS\_UVLOZ}$ ,  $V_{BAT} < V_{BAT\_UVLOZ}$  and a voltage higher than  $V_{AC\_PRESENT}$  is present at either VAC1 or VAC2, the device will be powered from  $V_{AC1}$  or  $V_{AC2}$ , depending on which comes first.

### 9.3.2 PROG Pin Configuration

At POR, the charger detects the PROG pin pull down resistance, then sets the charger default POR switching frequency and the battery cell count. Please follow the resistance list in [Table 9-1](#) to set the desired POR switching frequency and battery cell count. The surface mount resistor with  $\pm 1\%$  or  $\pm 2\%$  tolerance is recommended.

**Table 9-1. PROG Pin Resistance to Set Default Switching Frequency and Battery Cell Count**

| SWITCHING FREQUENCY | CELL COUNT | TYPICAL RESISTANCE AT PROG PIN |
|---------------------|------------|--------------------------------|
| 1.5 MHz             | 1s         | 3.0 k $\Omega$                 |
| 750 kHz             | 1s         | 4.7 k $\Omega$                 |
| 1.5 MHz             | 2s         | 6.04 k $\Omega$                |
| 750 kHz             | 2s         | 8.2 k $\Omega$                 |
| 1.5 MHz             | 3s         | 10.5 k $\Omega$                |
| 750 kHz             | 3s         | 13.7 k $\Omega$                |
| 1.5 MHz             | 4s         | 17.4 k $\Omega$                |
| 750 kHz             | 4s         | 27.0 k $\Omega$                |

Some of the charging parameters default values are determined by the battery cell count identified by PROG pin configuration, which are summarized in the table below.

**Table 9-2. Charging Parameters Dependent on Battery Cell Count**

| CELL (REG0x0A[7:6])    | 1s           | 2s           | 3s             | 4s            |
|------------------------|--------------|--------------|----------------|---------------|
| ICHG (REG0x03/04)      | 2 A          | 2 A          | 1 A            | 1 A           |
| VSYSMIN (REG0x00[5:0]) | 3.5 V        | 7 V          | 9 V            | 12 V          |
| VREG (REG0x01/02)      | 4.2 V        | 8.4 V        | 12.6 V         | 16.8 V        |
| VREG Range             | 3 V - 4.99 V | 5 V - 9.99 V | 10 V - 13.99 V | 14 V - 18.8 V |

After POR, the host can program the ICHG and VSYSMIN registers to any values within the ranges defined in the register tables. However, when programming the battery charging voltage (VREG), the host must ensure the VREG value is in the allowed range associated with the CELL register (REG0x0A[7:6]) setting defined in the table above. When the CELL register is changed, the ICHG, VSYSMIN and VREG registers are reset to the POR default values associated with the CELL setting.

For example, if the PROG pin resistance is a 2s battery configuration, the default POR CELL, ICHG, VSYSMIN and VREG settings will be 2s, 2 A, 7 V and 8.4 V respectively. After POR, the host can change ICHG and VSYSMIN to any values, and can change VREG to any value between 5V and 9.99V. Assuming that the CELL bits remain at the 2s battery configuration, then when the REG\_RST bit is set or the watchdog timer expires, the registers are reset to default values with ICHG, VSYSMIN and VREG automatically returning to 2 A, 7V and 8.4V respectively.

When the CELL register is 2s battery configuration, any write out of the range of VREG (5 V - 9.99 V) is ignored by the charger. If VREG needs to be programmed out of the 5 V - 9.9 V range, such as 11 V, the CELL bits have to be changed to the 3s setting. Setting the CELL bits will also cause the ICHG, VSYSMIN and VREG registers to reset to their 3s POR default values of 1 A, 9 V and 12.6 V. Then the host can program VREG in the range of

10 V - 13.99 V. If, after changing the CELL bits to 3S, the REG\_RST bit is set or the watchdog timer expires, the ICHG, VSYSMIN and VREG will then be reset to 1 A, 9 V and 12.6 V, regardless of the state of the PROG pin.

### 9.3.3 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above UVLO threshold ( $V_{BAT\_UVLOZ}$ ), the BATFET turns on and connects the battery to the system. The REGN LDO stays off to minimize the quiescent current. The low  $R_{DS(ON)}$  of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The POR sequence when the charger is powered from  $V_{BAT}$  is described as below:

1. 5 ms (typical) after  $V_{BAT} > V_{BAT\_UVLOZ}$ , the charger starts ACFET-RBFET detection, reads the resistance at the PROG pin, and then configures the charger POR register set accordingly.
2. 20 ms (typical) after  $V_{BAT} > V_{BAT\_UVLOZ}$ , the I<sup>2</sup>C registers become accessible to the host..
3. The charger turns the battery FET on to allow the battery to power the system.

### 9.3.4 Device Power Up from Input Source

When an input source is present at VBUS, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck-boost converter is started. The power up sequence from input source is as listed below:

1. The device begins the POR sequence when  $V_{VBUS} > V_{VBUS\_UVLOZ}$  if there is a direct path from input to VBUS, or otherwise when  $V_{AC1}$  or  $V_{AC2} > V_{AC\_PRESENT}$ .
2. 5 ms (typical) after a valid voltage is first present at either VBUS or VAC1/VAC2 pins, the charger starts the ACFET-RBFET detection, reads the resistance at PROG pin, and then configures the charger power on reset (POR) default register settings accordingly.
3. If ACFET-RBFET are detected on the input source pathway, the corresponding ACDRV turns on the pair.
4. 20 ms (typical) after valid voltage voltage presence, the I<sup>2</sup>C registers become accessible to the host.
5. As soon as  $V_{VBUS} > V_{VBUS\_UVLOZ}$  (in step 1 or after step 3),  $V_{BUS\_PRESENT\_STAT}$  is set to 1. 150 ms (typical) later, REGN is turned on.
6. Once REGN is on, the charger starts the poor source detection. After a good input source is detected (typically 30 ms if there is no retry),  $PG\_STAT$  is set to 1, then the ADC reads the ILIM\_HIZ pin voltage and VBUS voltage and updates the IINDPM and VINDPM registers accordingly.
7. When the poor source detection completes, the charger performs D+/D- detection and updates the  $V_{BUS\_STAT}$  and IINDPM registers accordingly.
8. 30 ms (typical) after the D+/D- detection completes, the converter starts switching to power SYS and charge the battery.

#### 9.3.4.1 Power Up REGN LDO

When the device is powered up from VBUS, the LDO is turned on when  $V_{VBUS\_PRESENT} < V_{BUS} < V_{VBUS\_OVP}$ . When the device is powered up from battery only condition, the LDO is turned on at either one of the following conditions:

- The charger is operated in the OTG mode
- VBAT is higher than 3.2V, and ADC TS channel is on ( $ADC\_EN = 1$  and  $TS\_ADC\_DIS = 0$ )

The REGN LDO supplies internal bias circuits and the MOSFETs gate drivers. The pull-up rails of ILIM\_HIZ, TS, and STAT can be connected to REGN. The INT pin pull-up rail is recommended to be an external 1.8V or 3.3V voltage source, rather than REGN, because at battery only condition, the REGN might not be available. Except the charger related pull up rails, the REGN is not recommended to source any other external circuit. The REGN has to power the internal MOSFETs gate drivers, which is very critical for the charger normal operation.

#### 9.3.4.2 Poor Source Qualification

After the REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to move forward to the next power on steps.

1. VBUS voltage below  $V_{VBUS\_OVP}$
2. VBUS voltage above  $V_{POORSRC}$  when pulling  $I_{POORSRC}$  (typical 30 mA)

Once the conditions are met, the status register bit PG\_STAT is set high and the  $\overline{\text{INT}}$  pin is pulsed to signal the host.

If VBUS\_OVP is detected (failing condition 1 above), the device automatically retries detection once the over-voltage fault goes away. If a poor source is detected (when pulling  $\text{I}_{\text{POORSRC}}$ , the VBUS voltage drops below  $\text{V}_{\text{POORSRC}}$ ), the device repeats poor source qualification routine every 2 seconds. After 7 consecutive failures, the device sets EN\_HIZ = 1 and goes to HIZ mode. The device will remain in HIZ until either the adapter is re-plugged or the EN\_HIZ bit is toggled, which will restart poor source detection with another 7 attempts. The EN\_HIZ bit is cleared automatically when the adapter is plugged in. If either condition 1 or condition 2 is not met, it means the input source is not qualified; the PG\_STAT bit remains low, and an  $\overline{\text{INT}}$  pulse will be asserted and PG\_FLAG will be set to 1, if PG\_MASK = 0.

#### 9.3.4.3 ILIM\_HIZ Pin

At POR, before the charger converter starts switching, the charger ADC reads the ILIM\_HIZ pin voltage, and calculates the input current limit (ILIM) set by this ILIM\_HIZ pin, according to:

$$\text{V}_{\text{ILIM\_HIZ}} = 1\text{V} + 800\text{ m}\Omega \times \text{ILIM} \quad (1)$$

The ILIM\_HIZ pin sets a high clamp for the IINDPM register. If the IINDPM setting from the D+/D- detection or the POR default 3A IINDPM setting is higher than the ILIM clamp, the IINDPM register stays at this ILIM clamp. In addition, the host cannot program the IINDPM register to any values higher than this ILIM clamp after POR, unless the register bit EN\_EXTILIM is set to 0.

The ILIM\_HIZ pin can be biased from a resistor voltage divider tied to either REGN or another external voltage source. For both the forward charging mode and the OTG mode, when the ILIM\_HIZ pin is pulled lower than 0.75V, the charger stops switching and REGN stays on. The charger resumes switching if the ILIM\_HIZ pin voltage becomes higher than 1V.

If the ADC reads the ILIM\_HIZ pin voltage is lower than 1.08V ( $1\text{V} + 800\text{ m}\Omega \times 100\text{ mA}$ ), the charger considers the ILIM clamp to be 100mA, which is the minimal setting of the IINDPM register.

#### 9.3.4.4 Default VINDPM Setting

In the POR sequence, right after the D+/D- detection, the charger initiates an ADC reading on the VBUS pin voltage without any load current (VBUS at no load condition,  $\text{VBUS}_0$ ) before the converter starts switching. The default VINDPM threshold is set to be  $\text{VBUS}_0 - 1.4\text{ V}$  ( $\text{VBUS}_0 \geq 7\text{ V}$ ) or  $\text{VBUS}_0 - 0.7\text{V}$  ( $\text{VBUS}_0 < 7\text{ V}$ ).

The  $\text{VBUS}_0$  can be remeasured at any time by setting the register bit FORCE\_VINDPM\_DET=1. The converter stops switching, the ADC measures the VBUS voltage, the VINDPM register field is updated, and then the FORCE\_VINDPM\_DET bit returns to 0. The force VINDPM detection only can be done when VSYS\_STAT = 0 ( $\text{VBAT} > \text{VSYS}_{\text{MIN}}$ ), otherwise stopping the converter would cause VSYS to drop below  $\text{VSYS}_{\text{MIN}}$ . If VSYS\_STAT = 1 ( $\text{VBAT} < \text{VSYS}_{\text{MIN}}$ ),  $\text{VBUS}_0$  measurement does not start, the FORCE\_VINDPM\_DET bit resets to 0 and the VINDPM register retains its current value. The host must ensure there is a battery present prior to setting FORCE\_VINDPM\_DET = 1, or to allow system to be supported by the battery during detection.

When the measured  $\text{VBUS}_0$  is out of the VINDPM register range, the charger sets the VINDPM register to the minimum value (3.6V) or maximum (22V) value as appropriate.

#### 9.3.4.5 Input Source Type Detection

After the input source is qualified, the charger runs Input Source Type Detection if AUTO\_INDET\_EN bit is set (default enabled).

The charger follows the USB Battery Charging Specification 1.2 (BC1.2) to detect SDP/CDP/DCP/HVDC input sources and the non-standard adapters through the USB D+/D- lines. After BC1.2 detection is completed, the BC1.2\_DONE\_STAT bit is set to 1, and an  $\overline{\text{INT}}$  pulse and BC1.2\_DONE\_FLAG are asserted if BC1.2\_DONE\_MASK = 0. In addition, when USB DCP is detected, the charger initiates adjustable high voltage adapter handshake on D+/D- if HVDCCP detection is enabled by the host. The input type might be changed after HVDCCP detection is completed.

After input source type detection, the following registers are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. VBUS\_STAT bits change to reflect the detected source

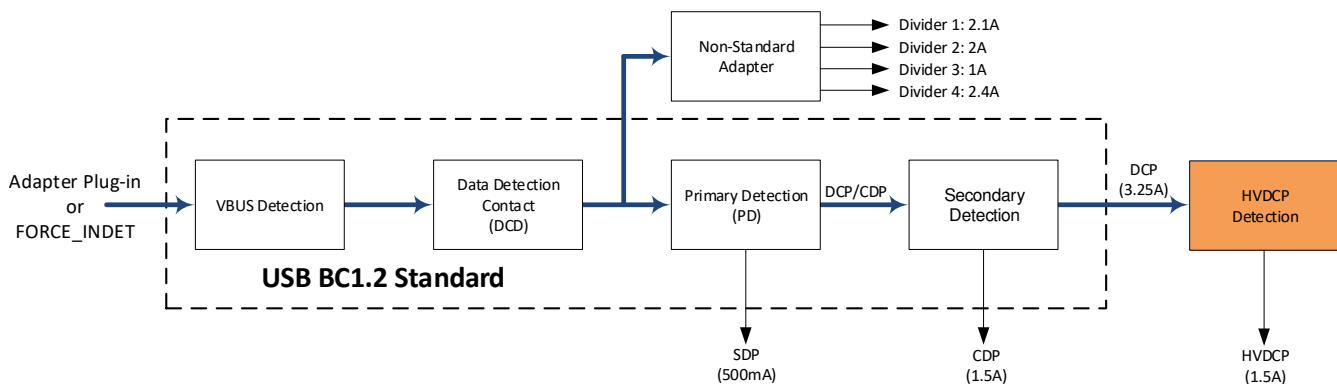
After detection is completed, the host can over-write IINDPM registers to change the input current limit if necessary. The charger input current is limited by the lower of IINDPM register or ILIM\_HIZ pin (when EN\_EXTILIM = 1) regardless of Input Current Optimizer (ICO) setting. When AUTO\_INDET\_EN is disabled, the Input Source Type Detection is bypassed, and the Input Current Limit (IINDPM) register remains unchanged from its previous value.

#### 9.3.4.5.1 D+/D– Detection Sets Input Current Limit

The device contains a D+/D– based input source detection to set the input current limit. The D+/D– detection has four major steps: Data Contact Detect (DCD), Primary Detection, Secondary Detection and High Voltage DCP (HVDCCP) detection.

The D+/D– Primary Detection includes standard USB BC1.2 and non-standard adapters. When an input source is plugged in, the device starts standard USB BC1.2 detection first. The USB BC1.2 is capable of identifying Standard Downstream Port (SDP), Charging Downstream Port (CDP) and Dedicated Charging Port (DCP). The non-standard detection is used to distinguish vendor specific adapters based on the unique dividers they apply to the D+/D– pins. The secondary detection is used to distinguish two types of charging ports, CDP and DCP.

A CDP usually requires the attached device to send back an enumeration within 2.5 seconds of CDP plug-in. Otherwise, the port will power cycle back to SDP even the D+/D– detection indicates CDP. This enumeration must be handled externally to the charger.



**Figure 9-1. D+/D– Detection Flow**

**Table 9-3. Non-Standard Adapter Detection**

| NON-STANDARD ADAPTER | D+ THRESHOLD                   | D– THRESHOLD                   | INPUT CURRENT LIMIT |
|----------------------|--------------------------------|--------------------------------|---------------------|
| Divider 1            | $V_{D+}$ within $V_{2P8\_VTH}$ | $V_{D-}$ within $V_{2P0\_VTH}$ | 2.1 A               |
| Divider 2            | $V_{D+}$ within $V_{1P2\_VTH}$ | $V_{D+}$ within $V_{1P2\_VTH}$ | 2A                  |
| Divider 3            | $V_{D+}$ within $V_{2P0\_VTH}$ | $V_{D-}$ within $V_{2P8\_VTH}$ | 1 A                 |
| Divider 4            | $V_{D+}$ within $V_{2P8\_VTH}$ | $V_{D-}$ within $V_{2P8\_VTH}$ | 2.4 A               |

When a Dedicated Charging Port (DCP) is detected, the charger initiates two high voltage adapter (HVDCCP) handshakes to enable the corresponding adapter to output a higher voltage for fast charging. The HVDCCP detection can be enabled by setting EN\_HVDCCP=1 and then setting either EN\_9V=1 to increase the input voltage to 9V or EN\_12V=1 to increase the input voltage to 12V. When EN\_12V and EN\_9V are both set to 1, the charger starts 12V first.

After the input source type detection is done, the DPDM\_STAT bit is set to 0, an  $\overline{INT}$  pulse and DPDM\_DONE\_FLAG are asserted if DPDM\_DONE\_MASK = 0. In addition, REG06\_Input\_Current\_Limit and VBUS\_STAT are updated as shown in [Table 9-4](#).

**Table 9-4. Input Current Limit Setting from D+/D- Detection**

| D+/D- DETECTION                     | INPUT CURRENT LIMIT (IINDPM) | VBUS_STAT_3:0 |
|-------------------------------------|------------------------------|---------------|
| USB SDP                             | 500 mA                       | 0001          |
| USB CDP                             | 1.5 A                        | 0010          |
| USB DCP                             | 3.25 A                       | 0011          |
| Adjustable High Voltage DCP (HVDCP) | 1.5A                         | 0100          |
| Unknown Adapter                     | 3 A                          | 0101          |
| Non-Standard Adapter, Divider 1     | 2.1 A                        | 0110          |
| Non-Standard Adapter, Divider 2     | 2 A                          | 0110          |
| Non-Standard Adapter, Divider 3     | 1 A                          | 0110          |
| Non-Standard Adapter, Divider 4     | 2.4 A                        | 0110          |

#### 9.3.4.5.2 HVDCP Detection Procedure

Figure 9-1 shows that an HVDCP source is first qualified as a DCP source in the USB BC1.2 standard detection stage, then qualified in the following HVDCP detection stage as an HVDCP source. When the HVDCP is first qualified as a DCP, the charger sets an IINDPM limit of 3.25A. The IINDPM is then updated to the HVDCP limit of 1.5A after the HVDCP handshake completes. In some cases the higher IINDPM limit of 3.25A may interfere with the source's ability to transition to 9V or 12V if the transition is attempted before the IINDPM is updated to 1.5A.

The recommended procedure for enabling detection of HVDCP sources is completed in the following steps:

- Before adapter insertion, the charger is configured with AUTO\_INDET\_EN = 1 and HVDCP\_EN = 0. EN\_12V and EN\_9V are set as desired for the system.
- When an adapter is inserted, it will be detected as SDP, CDP, DCP or a Non-Standard adapter and an I<sup>2</sup>C interrupt is sent to the host. If any detection other than DCP is made, the host proceeds as usual.
- If the adapter is detected as DCP (VBUS\_STAT[3:0] = 0011), the host first changes the Input Current Limit register to 1.5A and then changes HVDCP\_EN = 1.
- After HVDCP detection is complete, the host sets HVDCP\_EN = 0 to disable HVDCP support in preparation for the next input source detection sequence.

#### 9.3.4.5.3 Connector Fault Detection

The host can apply different status on D+ pin including HIZ, 0V, 0.6V, 1.2V, 2.0V, 2.7V, 3.3V or "short to D-", and different status on D- pin including HIZ, 0.6V, 1.2V, 2.0V, 2.7V or 3.3V. The device also provides ADC readings of the D+ and D- pin voltages. The host can use the information to determine if connector is normal or in any faults. The voltage values are set using the DPLUS\_DAC and DMINUS\_DAC register. The D+/D- pins are only applied at the VAC1 input source. If the DPLUS\_DAC or DMINUS\_DAC are programmed when the adapter is plugged in and the D+/D- detection is in process, the device will ignore the register programming.

### 9.3.5 Dual-Input Power Mux

The BQ25792 has two ACDRV drivers to control two optional sets of back-to-back power N-FETs, selecting and managing the power from two different input sources. In the POR sequence, the charger detects whether the ACFETs-RBFETs are present, then updates the ACRB1\_STAT or ACRB2\_STAT status bits accordingly. The ACFET1-RBFET1 or ACFET2-RBFET2 can be controlled by setting the register bit EN\_ACDRV1 or EN\_ACDRV2. If the external ACFET-RBFET is not present, then tie VAC1 / VAC2 to VBUS and connect ACDRV1 / ACDRV2 to GND. The power MUX drivers support three different application cases, which are elaborated below.

#### 9.3.5.1 ACDRV Turn On Condition

The ACDRV1 and ACDRV2 control the input power MUX. In order to turn on either ACDRV1 or ACDRV2, all of the following conditions must be valid:

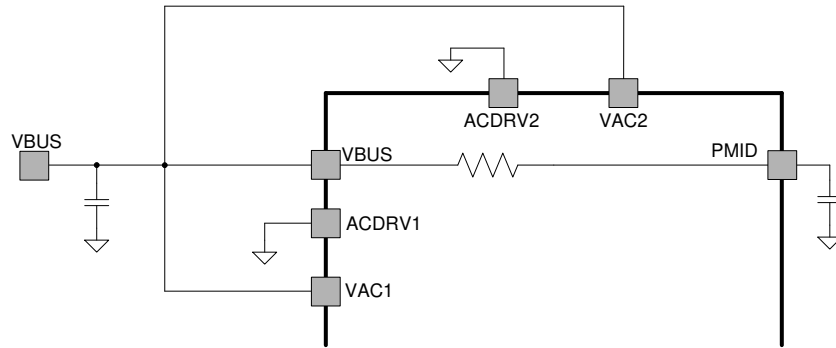
1. The corresponding ACFET-RBFET was detected at power on: ACDRV is not short to ground.
2. VAC is above  $V_{VAC_{present}}$  threshold
3. VAC is below  $V_{AC_{OVP}}$  threshold
4. DIS\_ACDRV\_BOTH is not set to '1'



5. EN\_HIZ is not set to '1'
6. VBUS is below  $V_{VBUS_{present}}$  threshold

### 9.3.5.2 VBUS Input Only

In this configuration, only a single input is connected to VBUS, so that no power MOSFETs are required. VAC1 and VAC2 are shorted to VBUS, and ACDRV1 and ACDRV2 are pulled down to GND, as shown in Figure 9-2. At POR, the charger detects that no ACFETs or RBFETs are present by sensing that the ACDRV1 and ACDRV2 pins are both shorted to GND and configures power mux register fields as shown in Table 9-5.



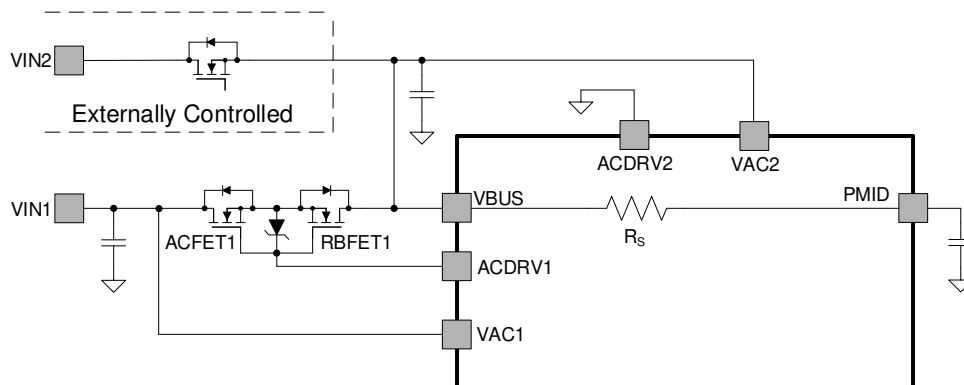
**Figure 9-2. Single Input Connected to VBUS Directly Without ACFET-RBFET**

**Table 9-5. Single Input Configuration Summary**

| PIN OR REGISTER FIELD | STATE                          |
|-----------------------|--------------------------------|
| External MOSFETs      | No external power mux MOSFETs. |
| VAC1 pin              | Shorted to VBUS                |
| VAC2 pin              | Shorted to VBUS                |
| ACDRV1 pin            | Shorted to GND                 |
| ACDRV2 pin            | Shorted to GND                 |
| ACRB1_STAT            | 0 (Read Only)                  |
| ACRB2_STAT            | 0 (Read Only)                  |
| DIS_ACDRV             | 1                              |
| EN_ACDRV1             | Locked at 0                    |
| EN_ACDRV2             | Locked at 0                    |

### 9.3.5.3 One ACFET-RBFET

In this configuration, only ACFET1-RBFET1 is present, ACFET2-RBFET2 is not. VAC1 is tied to the drain of ACFET1, ACDRV1 is connected to the gates of ACFET1 and RBFET1. VAC2 is shorted to VBUS, ACDRV2 is pulled down to GND. This structure is illustrated in Figure 9-3, which is able to support either single input (one from VAC1 to VBUS through ACFET1-RBFET1) or dual-input (one from VAC1 to VBUS through ACFET1-RBFET1, the other one connected directly to VBUS) applications. At POR, the charger detects only ACFET1-RBFET1 present and configures the power mux register fields as shown in Table 9-6.



**Figure 9-3. One ACFET-RBFET Structure Supporting One Input at VAC1 and/or One Input at VBUS**

**Table 9-6. Single Input Configuration Summary**

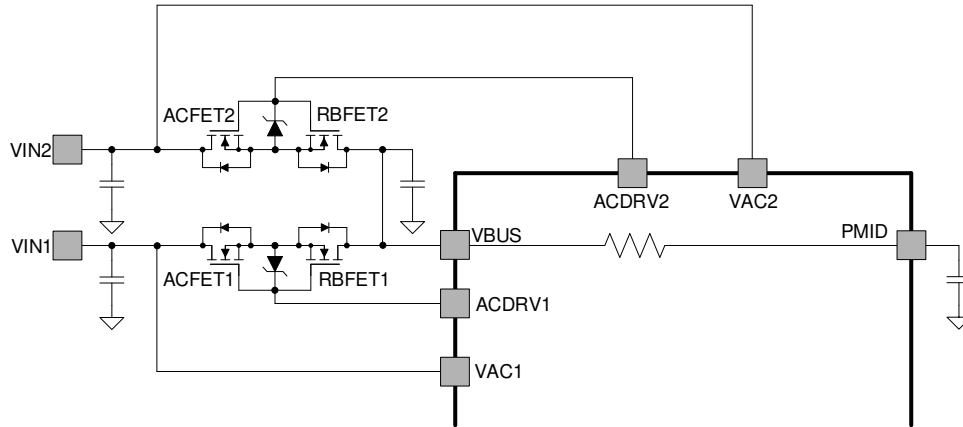
| PIN OR REGISTER FIELD | STATE   |
|-----------------------|---|
| External MOSFETs      | ACFET1 and RBFET1 only  |
| VAC1                  | Connected to input source 1   |
| VAC2                  | Shorted to VBUS   |
| ACDRV1                | Connected to ACFET1/RBFET1 gate terminals                                       |
| ACDRV2                | Shorted to GND  |
| ACRB1_STAT            | 0: ACFET1/RBFET1 Open (Path Disabled)<br>1: ACFET1/RBFET1 Closed (Path Enabled) |
| ACRB2_STAT            | 0 (Read Only)   |
| DIS_ACDRV             | 0: Allow ACDRV1 On if all requirements met<br>1: Force ACDRV1 Off               |
| EN_ACDRV1             | 0: Force ACDRV1 Off<br>1: Turn ACDRV1 On if all requirements met                |
| EN_ACDRV2             | Locked at 0   |

When a valid input is presented at VAC1, the charger will set EN\_ACDRV1 = 1 and turn ACFET1-RBFET1 on. To swap from the input at VAC1 to the input at VBUS, the host has to turn off the ACFET1-RBFET1 first by setting DIS\_ACDRV=1 (forcing EN\_ACDRV1 = 0), then enable the other input source which is connected directly to VBUS. To swap from the input at VBUS to the input at VAC1, the host has to disable the input source connected to VBUS, wait for VBUS to fall below  $V_{BUS\_PRESENT}$ , then turn on the ACFET1-RBFET1 by setting DIS\_ACDRV = 0.

#### 9.3.5.4 Two ACFETs-RBFETs

In this scenario, both ACFET1-RBFET1 and ACFET2-RBFET2 are present. VAC1 / VAC2 is tied to the drain of ACFET1 / ACFET2, ACDRV1 / ACDRV2 is connected to the gate of ACFET1 / ACFET2. This structure is developed to support dual-input connected at VAC1 and VAC2. At POR, the charger detects both ACFET1-RBFET1 and ACFET2-RBFET2 present, then updates ACRB1\_STAT and ACRB2\_STAT to 1.





**Figure 9-4. Two ACFETs-RBFETs Structure Supporting One Input at VAC1 and One Input at VAC2**

**Table 9-7. Dual Input Configuration Summary**

| PIN OR REGISTER FIELD | STATE  |
|-----------------------|--|
| External MOSFETs      | ACFET1, RBFET1, ACFET2, RBFET2   |
| VAC1 pin              | Connected to input source 1  |
| VAC2 pin              | Connected to input source 2  |
| ACDRV1 pin            | Connected to ACFET1/RBFET1 gate terminals  |
| ACDRV2 pin            | Connected to ACFET2/RBFET2 gate terminals  |
| ACRB1_STAT            | 0: ACFET1/RBFET1 Open (Path Disabled)<br>1: ACFET1/RBFET1 Closed (Path Enabled)        |
| ACRB2_STAT            | 0: ACFET2/RBFET2 Open (Path Disabled)<br>1: ACFET2/RBFET2 Closed (Path Enabled)        |
| DIS_ACDRV             | 0: Allow ACDRV1 or ACDRV2 on if all requirements met<br>1: Force ACDRV1 and ACDRV2 off |
| EN_ACDRV1             | 0: Force ACDRV1 Off<br>1: Turn ACDRV1 On if all requirements met                       |
| EN_ACDRV2             | 0: Force ACDRV2 Off<br>1: Turn ACDRV2 On if all requirements met                       |

In dual input mode, the ACDRV automatically turns on the ACFET-RBFET of the path where a valid input is first presented, without host intervention. If a valid input is presented on the second path while the first path is already on with a valid input, the ACFET-RBFET of the second path remains off. If desired, the host may manually perform a switch between power paths by switching the values of EN\_ACDRV1 and EN\_ACDRV2. Both EN\_ACDRV bits may be updated in a single I<sup>2</sup>C write operation to minimize the transition time. Note that programming EN\_ACDRV1 = 1, EN\_ACDRV2 = 1 at the same time to turn on both ACFET1-RBFET1 and ACFET2-RBFET2 is not allowed, and will be ignored by the charger.

To transition from one input to the other, the device first turns off the initially active ACFET-RBFET pair, waits until the VBUS voltage drops lower than  $V_{BUS\_PRESENT}$ , and then enables the new ACFET-RBFET pair. During this change over, the converter stops switching for a short period of time. When no battery is present or the battery is depleted, the system output will fall. The user has to be aware of this and avoid the input source swap when the battery voltage is too low.

If two valid voltages are present at VAC1 and VAC2 and the source on the connected path becomes invalid because of VAC\_UVLO, VAC\_OV or IBUS\_OC, the charger automatically swaps the input without any host engagement. Any time that the converter autonomously swaps the source paths, it will also update the EN\_ACDRV1 and EN\_ACDRV2 bits accordingly in order to indicate the active power path.

With only one valid input presented at either VAC1 or VAC2, the ACFET1-RBFET1 and ACFET2-RBFET2 can not be both turned off by setting REG0x13[7:6] = 00. Instead, the host should set DIS\_ACDRV = 1 to force both ACFET-RBFET pairs off. With input sources present at both VAC1 and VAC2, the host can turn off the two ACFET-RBFET pairs by setting either REG0x13[7:6] = 00 or DIS\_ACDRV = 1.

### 9.3.6 Buck-Boost Converter Operation

The charger employs a synchronous buck-boost converter that allows charging the 1s to 4s battery from a legacy 5V USB input source, HVDCP and USB-PD power sources. The converter operates uninterruptedly and continuously in buck, boost or buck-boost mode depending on the input to system output voltage difference. When the input voltage is close to the system output voltage, the converter operates in a proprietary buck-boost mode.

With a battery attached at BAT and input power at VBUS, the charger can provide at least the MINSYS voltage at SYS and charge current for the battery at BAT. Once the battery voltage reaches the MINSYS voltage, the SYS voltage follows the BAT voltage up. With no battery attached to BAT and input power at VBUS, the voltages at SYS and BAT vary depending on the whether or not charge is enabled as explained below.

1. No battery or battery removed and charge disabled by CE pin or EN\_CHG register or thermistor removed from TS pin - The charger keeps the BAT pin voltage at low-level, steady-state voltage and regulates SYS pin to MINSYS. The host can monitor the ADC BAT pin voltage and TS fault register to determine when a valid battery is attached.
2. No battery or battery removed while charge enabled and TS pin function is disabled - The charger continuously tries to charge the BAT capacitance, typically resulting in the BAT voltage alternating between a low level and BATOVF fault. The SYS voltage follows the battery voltage up, potentially reaching SYSOVP fault. In order to determine if a battery is attached, the host must periodically disable charge, force IBAT discharge current and then read the ADC BAT pin voltage. Alternatively, the host can monitor the INT pin for rapid interrupts and then read the charge status bits for fast (<1 s for typical BAT pin capacitance) toggling between charging, taper and termination.

#### 9.3.6.1 Force Input Current Limit Detection

In host mode, the host can force the device to run Input Current Limit Detection by setting FORCE\_INDET bit to 1. After the detection is completed, FORCE\_INDET bit automatically returns to 0. After the detection is completed, the input REG06\_Input\_Current\_Limit (IINDPM), and the VBUS\_STAT bits may be changed by the device according to the detection result.

#### 9.3.6.2 Input Current Optimizer (ICO)

The device provides Input Current Optimizer (ICO) to identify maximum power point in order to avoid overloading the input source. The algorithm automatically identifies maximum input current limit of an unknown power source and sets the charger IINDPM register properly, in order to prevent from entering the charger input voltage (VINDPM) regulation. This feature is disabled by default at POR (EN\_ICO = 0) and only activates when EN\_ICO bit is set to 1.

After DCP type input source is detected based on the procedures described in [Section 9.3.4.5](#), the algorithm runs automatically if EN\_ICO bit is set. The algorithm can also be forced to execute by setting FORCE\_ICO bit regardless of input source type detected. Please note that EN\_ICO = 1 is required for FORCE\_ICO to work.

The actual input current limit used by the Dynamic Power Management is reported in the ICO\_ILIM register whether set by ICO if enabled or IINDPM register if not. In addition, the current limit is clamped by the ILIM\_HIZ pin unless EN\_EXT\_ILIM bit is 0 to disable the ILIM\_HIZ pin function.

When V(BAT) > VMINSYS, the ICO algorithm starts with the maximum allowed input current as reported in ICO\_ILIM register as 500 mA then continually increases this limit until the optimal limit is found. When VBAT < VSYSTEMIN, the battery voltage can be too low to supplement a large system load if the charger buck converter

is limited to 500 mA and then ramped up by the ICO algorithm. Therefore, when a  $V_{BAT} < V_{SYS_{MIN}}$ , the ICO algorithm starts with the maximum allowed input current as reported in ICO\_ILIM register to the input current-limit register value in REG0x06 and then continually decreases this limit until the optimal limit is found.

Once the optimal input current is identified, the ICO\_STAT[1:0] and ICO\_FLAG bits are set. The actual input current is reported in the ICO\_ILIM register and does not change unless the algorithm is triggered again by the following events :

1. A new input source is plugged-in, or EN\_HIZ bit is toggled
2. IINDPM register is changed
3. VINDPM register is changed
4. FORCE\_ICO bit is set to 1
5. VBUS\_OVP event

These events also reset the ICO\_STAT[1:0] bits to 01

### 9.3.6.3 Pulse Frequency Modulation (PFM)

In order to improve converter light-load efficiency, the device switches to PFM control at light load condition. The effective switching frequency decreases accordingly as load current decreases. The PFM operation can be disabled by setting PFM\_FWD\_DIS = 1. With PFM disabled, the converter stays at the PWM mode switching frequency and transitions into DCM operation at light load condition. The minimum effective switching frequency in PFM can be limited to 25 kHz to eliminate the audible noise concern if the out of audio (OOA) feature is enabled by setting DIS\_FWD\_OOA = 0. The host can disable the OOA by setting DIS\_FWD\_OOA = 1, which may result in the converter effective switching frequency dropping below 25 kHz at extremely light load. The PFM operation of OTG mode can be independently controlled using the PFM\_OTG\_DIS and DIS\_OTG\_OOA bits. In PFM mode, the converter limits peak inductor current to 2 A, when OOA is enabled, and 3.3 A if OOA is disabled or if the load has increased close to the point of exiting PFM.

### 9.3.6.4 Device HIZ State

The charger enters HIZ mode when EN\_HIZ bit is set to 1. The HIZ mode refers to a charger state, in which the REGN LDO is off, and the converter stops switching even if the adapter is present. Similar to the battery only condition, the charger is in a low quiescent current mode, turns off the ADC and turns on the BATFET to support the system load. The ADC can be re-enabled during HIZ by setting EN\_ADC = 1.

Some of the faults, such as VBUS\_OVP, VSYS\_OVP, VBAT\_OVP and OTG\_OVP, force the converter to stop switching but keep the REGN and other internal circuits powered on. Alternatively, some of the faults, like VSYS\_SHORT and IBUS\_OCP, force the charger into HIZ mode by setting EN\_HIZ=1. More details could be found in the [Section 9.3.13](#).

## 9.3.7 USB On-The-Go (OTG)

### 9.3.7.1 OTG Mode to Power External Devices

The device supports the OTG operation to deliver power from the battery to other external devices through the USB ports. The OTG voltage regulation is set in VOTG[10:0] register bits. The OTG current regulation is set in IOTG[6:0] register bits. To enable the OTG operation, the following conditions have to be valid:

- The battery voltage is higher than  $V_{BAT\_OTG}$  rising threshold, and not trigger the VBAT\_OVP protection.
- The VBUS is below  $V_{VBUS\_UVLO}$ .
- The voltage at TS pin is within the range configured by BHOT and BCOLD register bits

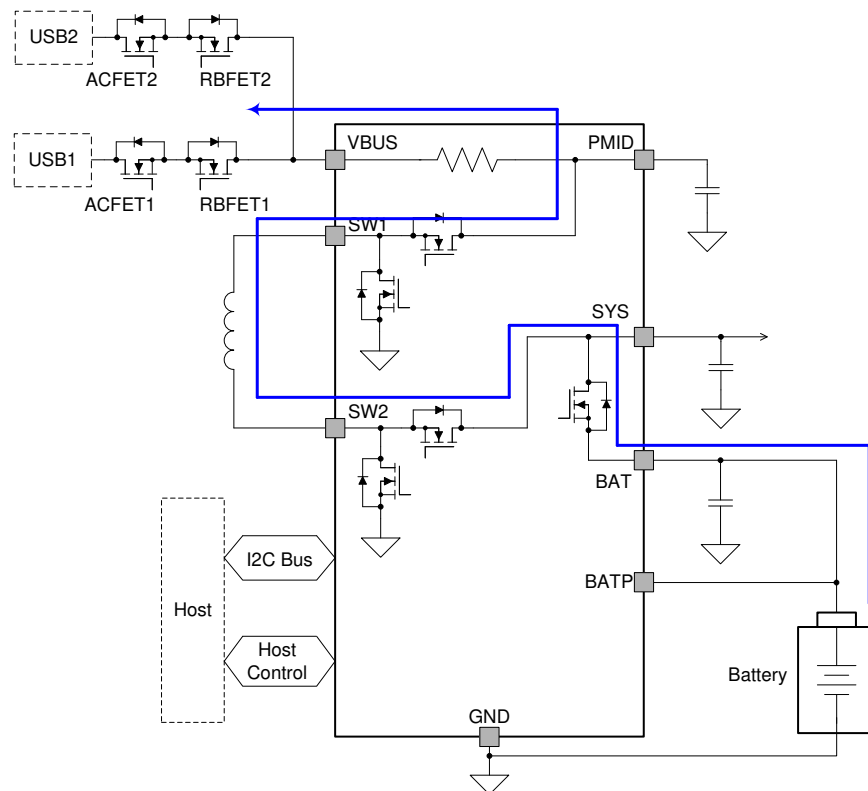
The population of ACFET1-RBFET1 and ACFET2-RBFET2 as detected at POR affects the operation of the converter in OTG mode as summarized in [Table 9-8](#).

**Table 9-8. OTG Behavior by Input Mux State**

| ACRB1_STAT | ACRB2_STAT | DIS_ACDRV | OTG BEHAVIOR  |
|------------|------------|-----------|---|
| 0          | 0          | 0         | Converter starts 5 ms after EN_OTG = 1  |
| 0          | 1          | 0         | EN_OTG = 1 does not start converter until EN_ACDRV2 = 1                         |
| 1          | 0          | 0         | EN_OTG = 1 does not start converter until EN_ACDRV1 = 1                         |
| 1          | 1          | 0         | EN_OTG = 1 does not start converter until either EN_ACDRV1 = 1 or EN_ACDRV2 = 1 |
| X          | X          | 1         | Converter starts 5 ms after EN_OTG = 1  |

For swapping the OTG output from port 1 to port 2, assuming EN\_ACDRV2 is already 0, the host has to set EN\_ACDRV1 = 0 to turn off ACFET1-RBFET1 first, which causes the converter to stop switching and VBUS to drop below  $V_{BUS\_PRESENT}$ . The host then sets EN\_ACDRV2 = 1, and the converter starts switching again and ACDRV2 turns on ACFET2-RBFET2, which allows VBUS to ramp up. The similar procedure can be applied to the case of swapping the OTG output from port 2 to port 1.

In OTG mode, the converter PFM operation can be disabled by setting PFM\_OTG\_DIS = 1 and the OOA can be disabled by setting DIS\_OTG\_OOA = 1.

**Figure 9-5. The Simplified Application Diagram for the OTG Mode Operation**

The simplified application diagram for the OTG mode operation is shown in [Figure 9-5](#), in which the power flow is illustrated by the blue arrows.

The charger regulates the battery discharging current in OTG mode. When IBAT rises higher than the IBAT\_REG[1:0] register setting, the charger reduces the OTG output current and prioritizes the system load current if there is any. The IBAT\_REG\_STAT bit is set to 1 and an  $\overline{INT}$  pulse is asserted, and if IBAT\_REG\_MASK = 0, the IBAT\_REG\_FLAG is set to 1. If the OTG output current is decreased to zero and the system load pulls even more current, the charger can no longer limit the battery discharging current.

When IBAT\_REG[1:0] is set to 00, 01 or 10 (3A, 4A or 5A), there is a soft-start applied to the OTG output current. When IBAT\_REG[1:0] is set to 11 (Disabled) no soft-start is applied.

### 9.3.8 Power Path Management

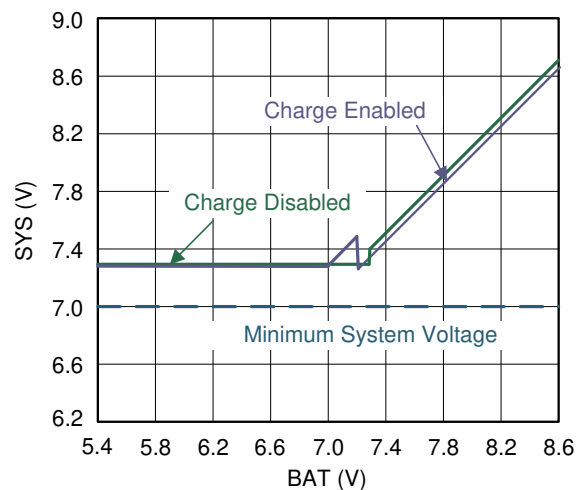
The device accommodates a wide range of input voltage range from 3.6V to 24V covering the legacy 5V USB input, HVDCP, USB-PD input and the wall adapter. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT) or both.

#### 9.3.8.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by VSYSMIN bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage. The default minimum system voltage at POR is determined according to the PROG pin configuration resistor.

The NVDC architecture also provides charging termination when the battery is fully charged. By turning off the BATFET, the adapter power is prioritized to support the system, which avoids having the battery continuously charged and discharged by the system load even if the adapter is present. This is important for extending the battery life time.

When the battery voltage is below the minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated at around 200 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the  $R_{DS(ON)}$  of the BATFET multiplied by the charging current. When battery charging is disabled and VBAT is above the minimum system voltage setting or charging is terminated, the system is always regulated at 200mV (typical, PWM switching) or 600mV (typical, PFM switching) above battery voltage. The status register VSYS\_STAT bit goes high when the system is in minimum system voltage regulation.



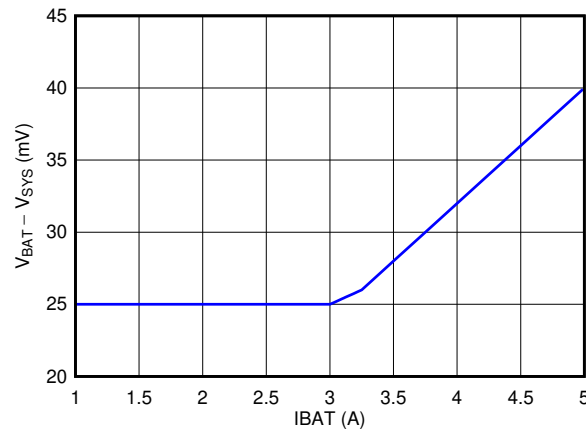
**Figure 9-6. Typical System Voltage vs Battery Voltage for a 2S Battery Configuration**

#### 9.3.8.2 Dynamic Power Management

To use the maximum available current from the input power source without over loading the adapter, the BQ25792 features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When the input power at the VBUS pin is too low to support the load from SYS pin and the battery charge current from BAT pin, the charger engages either IINDPM to limit its current or VINDPM to prevent further reduction in VBUS pin voltage.

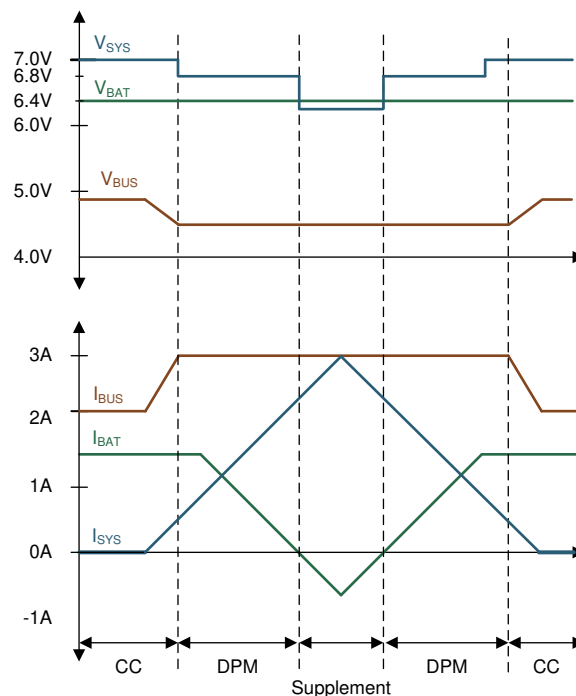
When the system voltage is regulated at VSYSMIN and SYS voltage temporarily drops lower than VSYSMIN, the VSYSMIN loop reduces charging current so that the SYS voltage remains at the VSYSMIN level. If the charge current falls to zero, but the input source is still overloaded, the SYS voltage will drop. Once the SYS voltage falls below the battery voltage, the device automatically enters supplement mode in which the BATFET

turns on. The battery starts discharging so that the system is supported from both the input source and battery. The battery FET operates in ideal diode mode, driving the battery FET gate voltage to regulate the BATFET  $V_{DS}$  at 25 mV for low current. This prevents SYS voltage oscillations from entering and exiting the supplement mode. As the discharge current increases, the ideal diode loop drives the BATFET gate to a higher voltage, in order to reduce the battery FET  $R_{DS(ON)}$  until the BATFET is fully turned on. Once the BATFET is fully on, the  $V_{DS}$  linearly increases with the discharge current. Figure 9-7 shows the V-I curve of the BATFET ideal diode operation. The BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.



**Figure 9-7. BATFET I-V Curve**

During DPM mode, the status register bits VINDPM\_STAT (VINDPM) and/or IINDPM\_STAT (IINDPM) go high. Figure 9-8 shows the DPM response with 5V/3A adapter, 6.4V battery, 1.5A charge current and 6.8V minimum system voltage setting.



**Figure 9-8. DPM Response**

### 9.3.9 Battery Charging Management

BQ25792 charges 1S~4S Li-Ion batteries with up to 5A charge current for high capacity cells. The battery charging in different stages is controlled by the integrated BATFET. The low  $R_{DS(ON)}$  BATFET improves charging efficiency and minimizes the voltage drop during discharging.

### 9.3.9.1 Autonomous Charging Cycle

When battery charging is enabled (EN\_CHG bit =1 and  $\overline{CE}$  pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in [Table 9-9](#). The host can always control the charging operation and optimize the charging parameters by writing to the corresponding registers through I<sup>2</sup>C.

**Table 9-9. Charging Parameter Default Settings**

| DEFAULT MODE   | BQ25792  |
|--|--|
| Charging voltage (REG01_Charge_Voltage_Limit)                  | 4.2 V (1S), 8.4 V (2S), 12.6 V (3S), 16.8 V (4S) |
| Recharging voltage threshold (VRECHG)                          | 200 mV   |
| Fast charge current (REG03_Charge_Current_Limit)               | 2 A (1S and 2S), 1 A (3S and 4S)                 |
| Pre-charge current (IPRECHG)                                   | 120 mA   |
| Trickle charge current (fixed value)                           | 100 mA   |
| Termination current (ITERM)                                    | 200 mA   |
| Temperature profile (REG17_NTC_Control_0, REG18_NTC_Control_1) | JEITA  |
| Fast charge safety timer (CHG_TMR)                             | 12 hours   |
| Pre-charge safety Timer (PRECHG_TMR)                           | 2 hours  |
| Trickle charge safety Timer (fixed value)                      | 1 hour   |

A new charge cycle starts when the following conditions are valid:

- $V_{BUS} > V_{V_{BUS\_PRESENT}}$
- $V_{BAT} < V_{RECHG}$  for TRECHG deglitch time
- Battery charging is enabled by setting register bit EN\_CHG = 1 and keeping  $\overline{CE}$  pin LOW
- No thermistor fault on TS pin
- No safety timer fault

The charger automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and the device is not in DPM mode or thermal regulation. When a fully charged battery voltage is discharged below recharge threshold (threshold selectable via VRECHG[1:0] bits), the device automatically starts a new charging cycle. After the charging terminates, toggling either  $\overline{CE}$  pin or EN\_CHG bit initiates a new charging cycle.

The STAT output indicates the charging status of: charging (LOW), charging complete or charging disabled (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting DIS\_STAT = 1. In addition, the status register (CHG\_STAT) indicates the different charging phases as:

- 000 – Not Charging
- 001 – Trickle Charge ( $V_{BAT} < V_{BAT\_SHORTZ}$ )
- 010 – Pre-charge ( $V_{BAT\_SHORTZ} < V_{BAT} < V_{BAT\_LOWV}$ )
- 011 – Fast Charge (CC mode)
- 100 – Taper Charge (CV mode)
- 101 – Reserved
- 110 – Top-off Timer Active Charging
- 111 – Charge Termination Done

When the charger transitions to any of these states, including when the charge cycle completes, an  $\overline{INT}$  is asserted to notify the host.

### 9.3.9.2 Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage, and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current/voltage accordingly.



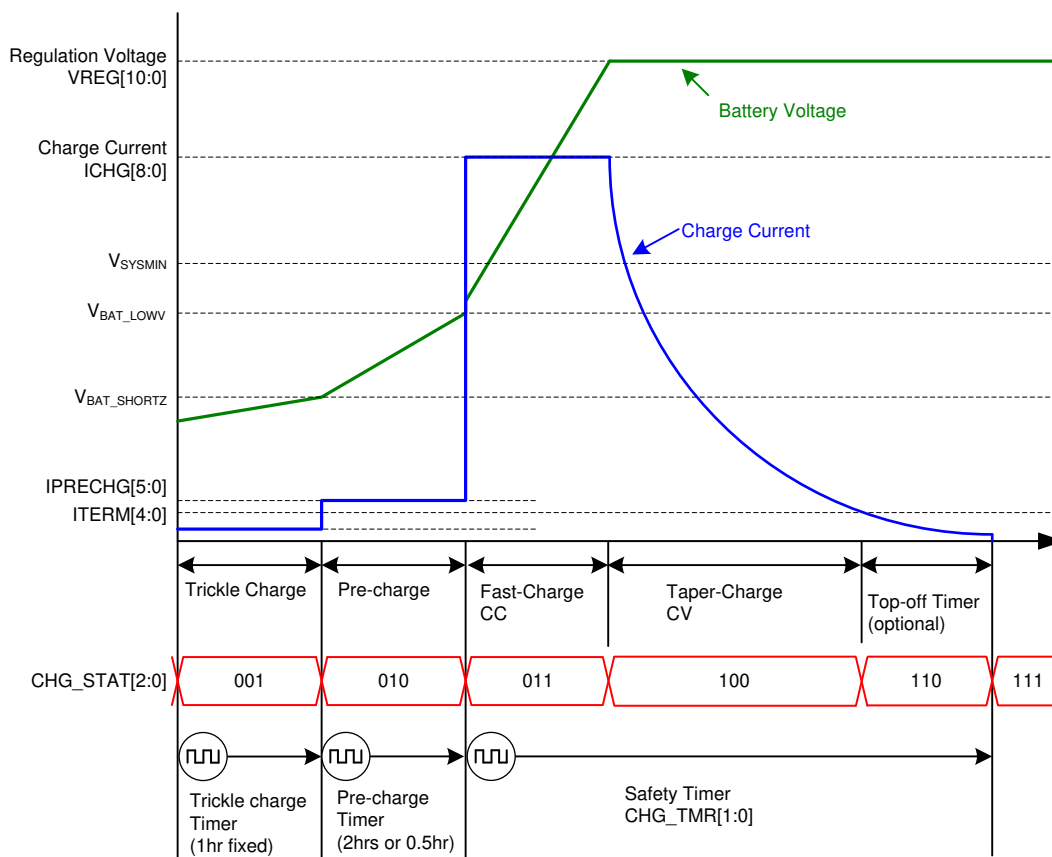
**Table 9-10. Default Charging Current Setting**

| VBAT                                 | CHARGING CURRENT | REGISTER DEFAULT SETTING           | CHRG_STAT |
|--------------------------------------|------------------|------------------------------------|-----------|
| $< V_{BAT\_SHORT}$                   | $I_{BAT\_SHORT}$ | 100 mA (fixed value)               | 001       |
| $V_{BAT\_SHORTZ}$ to $V_{BAT\_LOWV}$ | $I_{PRECHG}$     | 120 mA                             | 010       |
| $> V_{BAT\_LOWV}$                    | $I_{CHG}$        | 2 A (1S and 2S)<br>1 A (3S and 4S) | 011       |

If the charger is in DPM regulation or thermal regulation during charging, the actual charging current is less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as explained in [Section 9.3.9.4](#).

During SYSMIN regulation with BATFET LDO operation, the charge current is limited to 2 A, regardless of the charge current register setting, in order to protect the BATFET. It is not recommended to set the battery regulation voltage lower than the SYSMIN regulation voltage. The BATFET LDO operation can be disabled by setting  $DIS\_LDO = 1$ . In this state, charge current is regulated according to [Table 9-10](#) and SYS voltage is  $V(BAT)$  plus the IR drop through the BATFET, regardless of battery voltage. No  $VSYSMIN$  is maintained. Note that, when in trickle charge, setting  $DIS\_LDO = 1$  does not affect  $I_{BAT\_SHORT}$ .

$V_{BAT\_SHORTZ}$  is the battery voltage threshold for transition from trickle charge to precharge, which is fixed at 2.25V typical. During the trickle charge to precharge transition, the charger regulates the battery voltage to 2.5V/cell typical for  $t_{BAT\_SHORTZ}$  duration.  $V_{BAT\_LOWV}$  is the battery voltage threshold for the transition from pre-charge to fast charge. It is defined as a ratio of battery voltage regulation limit ( $VREG$ ).

**Figure 9-9. Battery Charging Profile**



### 9.3.9.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above the recharge threshold, the converter is operated in the battery constant voltage regulation loop and the current is below the termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system and the BATFET can turn on again if the supplement mode is triggered.

When termination is done, the status register CHG\_STAT is set to 111 and an  $\overline{\text{INT}}$  pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current (IINDPM), input voltage (VINDPM) or thermal (TREG) regulation. Termination can be permanently disabled by writing 0 to EN\_TERM bit prior to charging termination. Writing 0 to EN\_TERM when the termination has already occurred or in the top-off charging stage does not disable termination, until the next charging cycle has been restarted. If termination is enabled by setting EN\_TERM = 1 during an active charging cycle, the change is applied immediately.

At low termination currents (from 40mA to 160mA), due to the comparator offset, the actual termination current may be up to 20%~40% higher than the termination target. In order to compensate for the comparator offset, a programmable top-off timer (default disabled) can be activated after termination. While the top-off timer is running, the device continues to charge the battery in constant voltage mode (BATFET stays on) until the top-off time expires. The top-off timer follows safety timer constraints, such that if the safety timer is suspended, so is the top-off timer, and if the safety timer is doubled, so is the top-off timer. CHG\_STAT reports whether the top off timer is active via the 110 code. Once the top-off timer expires, charging terminates, the CHG\_STAT register is set to 111 and an  $\overline{\text{INT}}$  pulse is asserted to the host.

The top-off timer gets reset (set to 0 and counting resumes when appropriate) for any of the following conditions:

1. Charge disable to enable
2. Termination status low to high
3. REG\_RST register bit is set (disables top-off timer)

Once the charger detects termination, the charger reads the top-off timer (TOPOFF\_TMR) settings. Programming the top-off timer value after termination has no effect unless a recharge cycle is initiated. The top-off timer only starts to count when the charger's termination criteria are met. If EN\_TERM = 0, the charger never terminates charging, so the top-off timer does not start counting, even if it is enabled. An  $\overline{\text{INT}}$  is asserted to the host when the top-off timer starts counting as well as when the top-off timer expires. All charge cycle related  $\overline{\text{INT}}$  pulses (including top-off timer  $\overline{\text{INT}}$  pulse) can be masked by CHG\_MASK bit.

### 9.3.9.4 Charging Safety Timer

The device has a built-in safety timer to prevent an extended charging cycle due to abnormal battery conditions. The user can program the fast charge safety timer through I<sup>2</sup>C (CHG\_TMR bits). When the fast charge safety timer expires, the fault register CHG\_TMR\_STAT bit is set to 1, and an  $\overline{\text{INT}}$  pulse is asserted to the host. The trickle charge timer is fixed 1 hour. The pre-charge safety timer is adjustable 2 hours (POR default) or 0.5 hour. The fast charging timer POR default setting is 12 hours.

The trickle charge, pre-charge and fast charge safety timers can be disabled by setting EN\_TRICHG\_TMR, EN\_PRECHG\_TMR or EN\_CHG\_TMR bit to 0. Each charging safety timer can be enabled anytime regardless of the current charging state. Each timer restarts counting when it is enabled. As soon as each charging stage is initiated, the associated safety timer starts to count, which is illustrated in the battery charging profile chart shown in [Section 9.3.9.2](#).

During input voltage, current or thermal regulation, the safety timer counts at half-clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM\_STAT = 1) throughout the whole charging cycle, and the safety timer is set to 5 hours, then the timer will expire in 10 hours. This half-clock rate feature can be disabled by setting TMR2X\_EN = 0. If the host disables the half-clock rate while the charger is already running at half-clock rate, the charger keeps running at the half-clock rate and the half-clock rate is not disabled until the charger exit the voltage, current or thermal regulation.

During faults which disable charging or supplement mode, the timer is suspended. Since the timer is not counting in this state, the TMR2X\_EN bit has no effect. Once the fault goes away, the safety timer resumes. The

pre-charge safety timer and the trickle charge safety timer follow the same rules as the fast charge safety timer in terms of getting suspended, reset and counting at half-rate when TMR2X\_EN is set.

The fast charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle  $\overline{CE}$  pin, EN\_CHG bit, or charged battery falls below recharge threshold after termination)
2. BAT voltage changes from pre-charge to fast-charge or vice versa (in host-mode or default mode)
3. A change of the value of CHG\_TMR[1:0] register bits

The pre-charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle  $\overline{CE}$  pin, EN\_CHG bit, or charged battery falls below recharge threshold)
2. BAT voltage changes from trickle charge to pre-charge or vice versa, pre-charge to fast charge or vice versa (in host-mode or default mode)
3. A change of the value of PRECHG\_TMR register bit.

The trickle charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle  $\overline{CE}$  pin, EN\_CHG bit, or charged battery falls below recharge threshold)
2. BAT voltage changes from trickle charge to pre-charge or vice versa (in host-mode or default mode)

### 9.3.9.5 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitoring.

#### 9.3.9.5.1 JEITA Guideline Compliance in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the VT1-VT5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature T1-T2, JEITA recommends to reduce the charge current to be lower than half of the charge current at normal temperature T2-T3. The device provides the programmability of the charge current at T1-T2, to be 20%, 40% or 100% of the charge current at T2-T3 or charge suspend, which is controlled by the register bits JEITA\_ISETC.

The device provides the programmability of the charge voltage at T3-T5, to be with a voltage offset (0mV, 100mV or 200mV) less than charge voltage at T2-T3 or charge suspend, which is controlled by the register bits JEITA\_VSET.

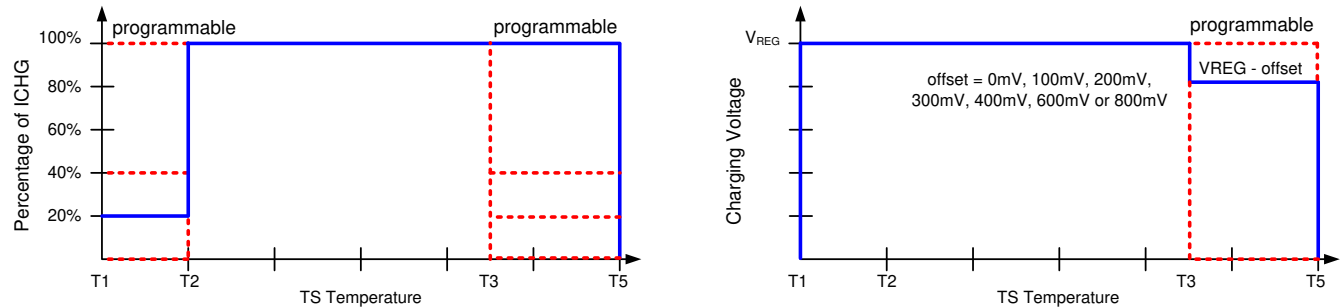
The charger also provides flexible voltage/current settings beyond the JEITA requirements. The charge current setting at warm temperature T3-T5 can be configured to be 20%, 40% or 100% of the charge current at T2-T3 or charge suspend, which is programmed by the register bits JEITA\_ISETH.

The charge termination is still enabled (when EN\_TERM=1) at cool temperature T1-T2 and warm temperature T3-T5. The termination current will be kept as the same in all different temperature ranges. In the normal operation, the charge will be terminated based on the charge current is lower than the termination current, the battery voltage is higher than the battery recharge voltage and the charger is in the battery voltage regulation loop. When the temperature enters T1-T2 or T3-T5, the charge current might drop to 20% or 40% of that at T2-T3, which might be lower than the termination current setting. If at this moment, the battery voltage is already higher than the battery recharge voltage and the charger is in the battery voltage regulation loop, the charge will be terminated.

At warm temperature T3-T5, the battery charge voltage will becomes lower. If the battery voltage is already very close to the battery charge voltage at T2-T3, to reduce the charge voltage by an offset might trigger the VBAT\_OVP. The charger should response as the normal VBAT\_OVP protection under this scenario.

At cool temperature T1-T2 or warm temperature T3-T5, the charge current will become different from that at the normal temperature range T2-T3, the safety timer should be adjusted accordingly. The safety timer will be suspended when the charge is suspended, and will run at half of the clock rate when the charge current is reduced to 20% or 40%, and will keep the same when the charge current is unchanged.

JEITA charging values are shown in Figure 9-10, in which the blue real line is the default setting and the red dash line is the programmable options.

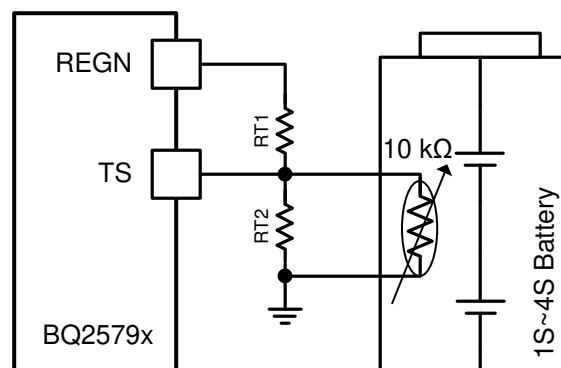


**Figure 9-10. TS Charging Values**

The NTC monitoring on the battery temperature can be ignored by the charger if TS\_IGNORE = 1. When the TS pin feedback is ignored, the charger considers the TS is always good for charging and OTG modes. The TS\_STAT including TS\_COLD\_STAT, TS\_COOL\_STAT, TS\_WARM\_STAT and TS\_HOT\_STAT, always report 000 with TS\_IGNORE = 1.

When TS\_IGNORE = 0, the charger adjusts the charging profile based on the TS pin feedback information. When the battery temperature crosses from one temperature range to the other one, the associated TS status bits are updated accordingly. The TS flag bits are set for the temperature range for which the TS voltage is reporting, and an  $\overline{\text{INT}}$  pulse is asserted to alert the host if TS\_MASK is low. The FLAG and  $\overline{\text{INT}}$  pulse can be individually masked by properly setting the associated mask bit, to prevent the  $\overline{\text{INT}}$  pulse from alerting the host of battery temperature range changes.

The typical TS resistor network is illustrated in Figure 9-11.



**Figure 9-11. TS Resistor Network**

Assuming a 103AT NTC thermistor on the battery pack, the value of TSR1 and TSR2 can be determined by:

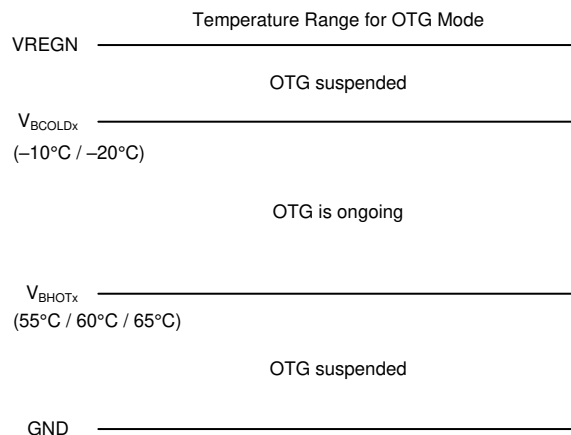
$$RT2 = \frac{RTH_{COLD} \times RTH_{HOT} \times \left( \frac{1}{VT1} - \frac{1}{VT5} \right)}{RTH_{HOT} \times \left( \frac{1}{VT5} - 1 \right) - RTH_{COLD} \times \left( \frac{1}{VT1} - 1 \right)} \quad (2)$$

$$RT1 = \frac{\frac{1}{\frac{1}{VT1} - 1}}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (3)$$

where VT# are the percentages of V(REGN) per the electrical spec table. The BQ25792 provides comparators with fixed thresholds for VT1 x V(REGN) and VT5 x V(REGN), and comparators with programmable thresholds for VT2 x V(REGN) and VT3 x V(REGN). The thresholds for VT2 x V(REGN) and VT3 x V(REGN) are controlled by TS\_COOL and TS\_WARM. This programmability gives more flexibility for the configuration of the JEITA profile. Select T1=0°C and T5=60°C for Li-ion or Li-polymer battery, the RT1 and RT2 are calculated to be 5.24KΩ and 30.31KΩ respectively.

### 9.3.9.5.2 Cold/Hot Temperature Window in OTG Mode

For battery protection during OTG mode, the device monitors the battery temperature to be within the VBCOLD to VBHOT thresholds. When RT1 is 5.24 KΩ and RT2 is 31.31 KΩ, TBCOLD default is -10°C and TBHOT default is 60°C. When the temperature is outside of this range, OTG mode is suspended, the converter stops switching. The charger waits in OTG mode (EN\_OTG = 1). In addition, the VBUS\_STAT bits are set to 000 and the corresponding TS\_COLD\_STAT or TS\_HOT\_STAT is reported. Once temperature returns to the normal temperature range, OTG mode is recovered and TS\_FAULT bit is cleared. During TS fault, REGN remains on.



**Figure 9-12. TS Pin Thermistor Sense Threshold in OTG Mode**

### 9.3.10 Integrated 16-Bit ADC for Monitoring

The device has an integrated 16-bit ADC to provide the user with critical system information for optimizing the behavior of the charger. The ADC is controlled through the ADC Control register. The ADC\_EN bit provides the ability to disable the ADC in order to conserve power dissipation. The ADC\_RATE bit allows continuous conversion or one-shot behavior. After a 1-shot conversion finishes, the ADC\_EN bit is cleared, and must be re-asserted to start a new conversion. The ADC\_AVG bit enables or disables (default) averaging. ADC\_AVG\_INIT starts average using the existing (default) or using a new ADC value.

To enable the ADC, the ADC\_EN bit must be set to 1. The ADC is allowed to operate if either VBUS > 3.4 V or VBAT > 2.9 V is valid. If ADC\_EN is set to 1 before VBUS or VBAT reaches its valid threshold, then the ADC conversion is postponed until one of the power supplies reaches the threshold. If the charger is in HIZ mode, the ADC still can be enabled by setting ADC\_EN = 1. At battery only condition, if the TS\_ADC channel is enabled, the ADC only works when battery voltage is higher than 3.2V, otherwise, the ADC works when the battery voltage is higher than 2.9V.

The ADC\_SAMPLE bits control the ADC sample speed, with conversion times of  $t_{ADC\_CONV}$ . If the host changes the sample speed in the middle of an ADC conversion, the ADC conversion stops the channel being converted, and that channel is reconverted at the new rate. At that point, some of the ADC register values might have been converted with one sample rate and others with a different sample rate.

By default, all ADC channels are enabled with 1-shot or continuous conversion mode unless the channel is disabled in the ADC\_Function\_Disable\_0 or ADC\_Function\_Disable\_1 register. If an ADC channel is disabled by setting the corresponding register bit, then the value in that register is from the last valid ADC conversion or the default POR value (all zeros.) If an ADC channel is disabled in the middle of an ADC measurement cycle, the device finishes the conversion of that channel. Even though no conversion takes place when all ADC channels are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in the ADC\_Function\_Disable\_0 or ADC\_Function\_Disable\_1 register is set to 0. In order to achieve the lowest quiescent current when disabling all ADC channels, set EN\_ADC to 0 instead of disabling with ADC\_Function\_Disable\_0 and ADC\_Function\_Disable\_1.

The ADC\_DONE\_STAT and ADC\_DONE\_FLAG bits are set when a conversion is complete in 1-shot mode only. This event produces an  $\overline{\text{INT}}$  pulse, which can be masked with ADC\_DONE\_MASK. During continuous conversion mode, the ADC\_DONE\_STAT and ADC\_DONE\_FLAG bits have no meaning and remain 0.

ADC conversion operates independently of the faults present in the device. ADC conversion continues even after a fault has occurred. ADC readings are only valid for DC states and not for transients.

If the host wants to exit the ADC more gracefully, it is recommended to write ADC\_RATE to one-shot in order to force the ADC to stop at the end of a complete cycle of conversions.

ADC Measurement Channels:

- IBUS (positive in forward converter mode)
- IBAT (positive for charging)
- VBUS
- VPMID
- VBAT
- VSYS
- TS
- TDIE

### 9.3.11 Status Outputs ( STAT, and $\overline{\text{INT}}$ )

#### 9.3.11.1 Charging Status Indicator (STAT Pin)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive an LED. The STAT pin function can be disabled via the DIS\_STAT bit.

**Table 9-11. STAT Pin State**

| CHARGING STATE  | STAT INDICATOR   |
|---|------------------|
| Charging in progress (including recharge and charging in top-off timer) | LOW              |
| Charging complete   | HIGH             |
| HIZ mode, charge disable  | HIGH             |
| Battery only mode and OTG mode  | HIGH             |
| Charge suspend (A fault condition which disable charging)               | Blinking at 1 Hz |

#### 9.3.11.2 Interrupt to Host ( $\overline{\text{INT}}$ )

In some applications, the host does not always monitor charger operation. The  $\overline{\text{INT}}$  pin notifies the system host on the device operation. By default, the following events generate an active-low, 256 $\mu$ s  $\overline{\text{INT}}$  pulse.

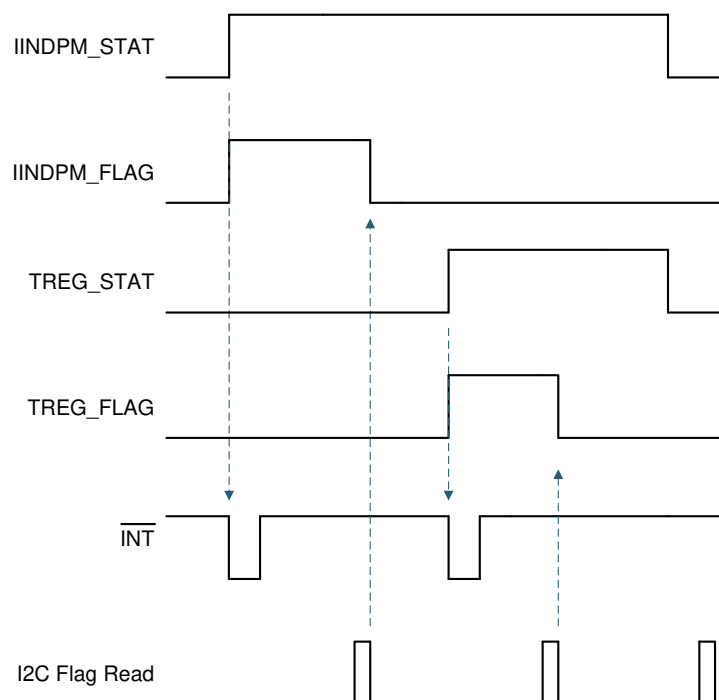
1. Good input source detected
  - $V_{\text{VBUS}} < V_{\text{VBUS\_OVP}}$  threshold
  - $V_{\text{VBUS}} > V_{\text{POORSRC}}$  (typical 3.4 V) when  $I_{\text{POORSRC}}$  (typical 30 mA) current is applied (not a poor source)
2. VBUS\_STAT changes state (VBUS\_STAT any bit change)
3. Good input source removed
4. Entering IINDPM regulation
5. Entering VINDPM regulation
6. Entering IC junction temperature regulation (TREG)

7. I<sup>2</sup>C Watchdog timer expired
  - At initial power up, this  $\overline{\text{INT}}$  gets asserted to signal I<sup>2</sup>C is ready for communication
8. Charger status changes state (CHRG\_STAT value change), including Charge Complete
9. TS\_STAT changes state (TS\_STAT any bit change)
10. VBUS over-voltage detected (VBUS\_OVP)
11. VAC over-voltage detected (VAC\_OVP for VAC1 or VAC2)
12. Junction temperature shutdown (TSHUT)
13. Battery over-voltage detected (BATOVP)
14. System over-voltage detected (VSYS\_OVP)
15. IBUS over-current detected (IBUS\_OCP)
16. IBAT over-current detected (IBAT\_OCP)
17. Charge safety timer expired, including trickle charge and pre-charge and fast charge safety timer expired
18. A rising edge on any of the other \*\_STAT bits

Each one of these  $\overline{\text{INT}}$  sources can be masked off to prevent  $\overline{\text{INT}}$  pulses from being sent out when they occur. Three bits exist for each one of these events:

- The STAT bit holds the *current status* of each  $\overline{\text{INT}}$  source
- The FLAG bit holds information on which source produced an  $\overline{\text{INT}}$ , regardless of the *current status*
- The MASK bit is used to prevent the device from sending out  $\overline{\text{INT}}$  for each particular event

When one of the above conditions occurs (a rising edge on any of the \*\_STAT bits), the device sends out an  $\overline{\text{INT}}$  pulse and keeps track of which source generated the  $\overline{\text{INT}}$  via the FLAG registers. The FLAG register bits are automatically reset to zero after the host reads them, and a new edge on STAT bit is required to re-assert the FLAG. This sequence is illustrated in Figure 9-13.



**Figure 9-13.  $\overline{\text{INT}}$  Generation Behavior Example**

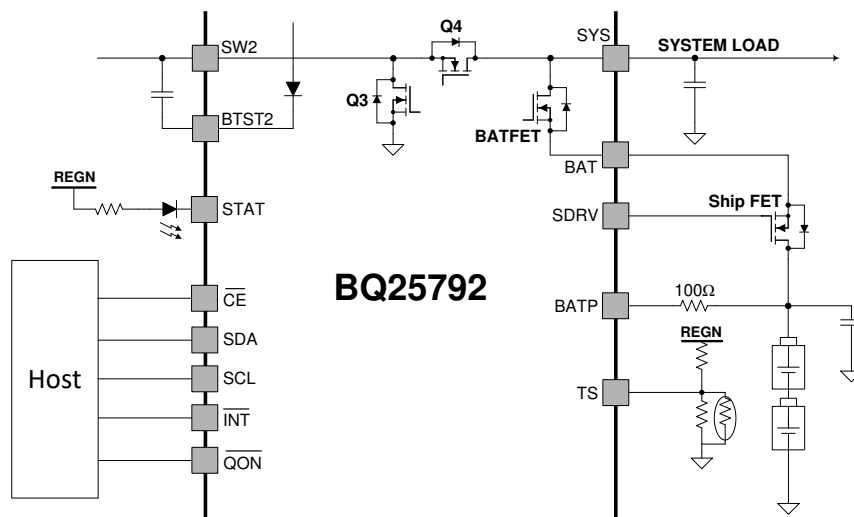
### 9.3.12 Ship FET Control

The charger provides an N-FET driving pin (SDRV) to control an external ship FET. The SDRV pin is the output of a charge pump that provides 100 nA typical drive current to drive the ship FET gate to typically 5-V above the battery voltage. When this ship FET is off, it removes leakage current from the battery to the system. The ship FET is controlled by the SDRV\_CTRL[1:0] register bits, to support the shutdown mode, ship mode and the system power reset.



- **IDLE Mode** when SDRV\_CTRL[1:0] = 00, POR default. The external ship FET is fully on, I<sup>2</sup>C is enabled. The internal BATFET status is determined by the charging status. This mode is valid with adapter present, during forward charging, in OTG mode or in the battery only condition.
- **Shutdown Mode** when SDRV\_CTRL[1:0] = 01. The ship FET turns and the internal BATFET are both off. The I<sup>2</sup>C is disabled. The charger is totally shutdown and can only be woken up by an adapter plug-in. This mode can only be entered when no adapter is present. If SDRV\_CTRL[1:0] is written to 01 with an adapter present, the write is ignored.
- **Ship Mode** when SDRV\_CTRL[1:0] = 10. The ship FET turns off. The I<sup>2</sup>C is still enabled. The charger can be woken up by setting SDRV\_CTRL[1:0] back to 00, or pulling the QON pin low, or an adapter plug-in. This mode can only be entered when no adapter is present. If SDRV\_CTRL[1:0] is written to 01 with an adapter present, the write is ignored.
- **System Power Reset** when SDRV\_CTRL[1:0] = 11. The ship FET is turned off for typical 350ms to reset the system power (converter goes to HIZ mode if VBUS is high), then the ship FET is fully turned on again. The BATFET keeps the status unchanged during the system power reset. After the reset is done, SDRV\_CTRL[1:0] goes back to 00.

When the host changes SDRV\_CTRL[1:0] from 00 to the other values, the charger turns off the ship FET immediately or delays by  $t_{SM\_DLY}$  as configured by SDRV\_DLY bit. The application diagram when the battery is connected to the charger through an external ship FET is illustrated in the figure below.



**Figure 9-14. The Application Diagram for the External Ship FET**

#### 9.3.12.1 Shutdown Mode

To further reduce battery leakage current, the host can shut down the charger by setting the register bits SDRV\_CTRL[1:0] to 01. In this mode, the I<sup>2</sup>C is disabled and the charger is totally shut down. The device can only be woken up by plugging in an adapter.

After the SDRV\_CTRL[1:0] is set to 01, the external ship FET turns off either immediately or after waiting for 10s as configured by SDRV\_DLY register bit. When VBUS is high because of an adapter being present or the OTG mode being enable, SDRV\_CTRL[1:0] will be reset to 00 if the host writes it to 01.

When the device exits shutdown mode, the SDRV\_CTRL bits are reset to the POR default values (00).

#### 9.3.12.2 Ship Mode

To extend battery life and minimize the system power loss when system is powered off during idle, shipping or storage, the device can turn off BATFET and external ship FET to minimize the battery leakage current. The ship mode is enabled when the host sets SDRV\_CTRL[1:0] to 10. The I<sup>2</sup>C is still enabled, but the charger system clock slows down to minimize the device quiescent current.

After the SDRV\_CTRL[1:0] is set to 10, the external ship FET is turned off either immediately or after waiting 10 seconds as configured by SDRV\_DLY register bit. When VBUS is high because of an adapter being present or OTG mode being enabled, SDRV\_CTRL[1:0] automatically resets to 00 if the host writes it to 10.

The following events will cause an exit from ship mode:

- Plug in an adapter
- Set SDRV\_CTRL[1:0] = 00
- Set REG\_RST = 1, to reset all the registers including SDRV\_CTRL bits back to default (00)
- A logic low of t<sub>SM\_EXIT</sub> (typical 1s or 15ms programmed by WKUP\_DLY bit) duration on QON pin

The charger exits ship mode by turning on the ship FET and internal BATFET to reconnect the battery to the system and resetting SDRV\_CTRL bits to their POR default value (00).

### 9.3.12.3 System Power Reset

The host can reset the system power by:

- Set the register bits SDRV\_CTRL[1:0] to 11
- A logic low of t<sub>RST</sub> (typical 10s) duration on QON pin

When the system power reset is enabled, the device turns off the ship FET for t<sub>RST\_SFET</sub> (typical 350ms) and also sets the charger in HIZ mode if VBUS is high. After the t<sub>RST\_SFET</sub> completes, the device then turns on the ship FET and disables the charger HIZ mode. While the SFET is off, the charger applies a 30mA (typical) sink current on SYS to discharge system voltage.

Regardless of whether the charger is at battery only condition or in the forward charging mode with adapter present, the charger resets the system power when the SDRV\_CTRL[1:0] bits are set to 11 or the QON pin is pulled low for t<sub>RST</sub> duration.

### 9.3.13 Protections

#### 9.3.13.1 Voltage and Current Monitoring

The device closely monitors the input, system and battery voltage and current, as well as internal FET currents for safe converter operation. It provides the following protection faults :

- VAC Over-voltage Protection (VAC\_OVP)
- VBUS Over-voltage Protection (VBUS\_OVP)
- VBUS Under-voltage Protection (POORSRC)
- System Over-voltage Protection (VSYS\_OVP)
- System Short Protection (VSYS\_SHORT)
- Battery Over-voltage Protection (VBAT\_OVP)
- Battery Over-current Protection (IBAT\_OCP)
- Input Over-current Protection (IBUS\_OCP)
- OTG Over-voltage Protection (OTG\_OVP)
- OTG Under-voltage Protection (OTG\_UVP)

#### 9.3.13.2 Thermal Regulation and Thermal Shutdown

The device monitors its internal junction temperature (T<sub>j</sub>) to avoid overheating and to limit the IC surface temperature. When the internal junction temperature exceeds the preset thermal regulation limit (TREG bits), the device reduces the charge current or OTG output current to maintain the junction temperature at the thermal regulation limit. A wide thermal regulation range from 60°C to 120°C allows optimization of the system thermal performance. During thermal regulation, the actual charging current is usually below the programmed value in the ICHG registers. Therefore, termination is disabled, the fast charging safety timer runs at half the clock rate, the status register TREG\_STAT bit goes high, TREG\_FLAG bit is set to 1, and an INT is asserted to alert host unless TREG\_MASK is set to 1.

Additionally, the device has thermal shutdown to turn off the converter when the IC junction temperature exceeds the TSHUT threshold. The fault register bits TSHUT\_STAT and TSHUT\_FLAG are set and an INT pulse is asserted to the host, unless TSHUT\_MASK is set to 1. The BATFET and the converter resumes normal operation when the IC die temperature decreases lower than TSHUT threshold by T<sub>SHUT\_HYS</sub>.



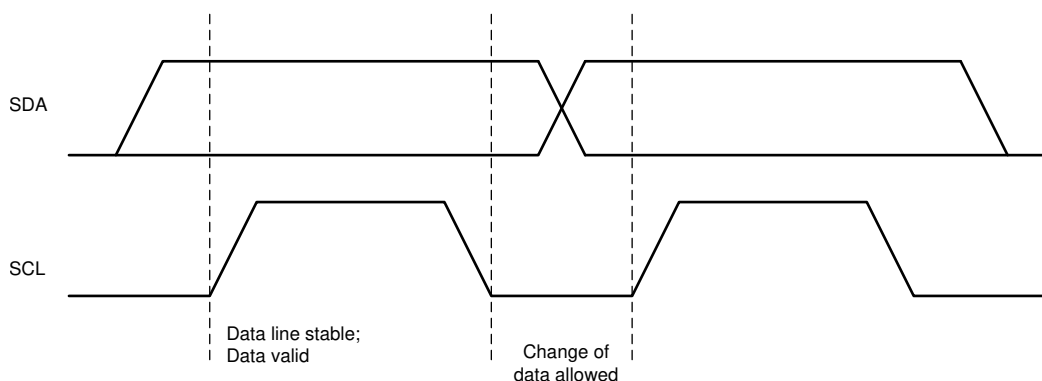
### 9.3.14 Serial Interface

The device uses I<sup>2</sup>C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I<sup>2</sup>C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL). Devices can be considered as controllers or targets when performing data transfers. A controller is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The device operates as a target device with 7-bit address 0x6B, receiving control inputs from the controller device like micro-controller or digital signal processor through REG00 – REG25. Register read beyond REG25 (0x25), returns 0xFF. The I<sup>2</sup>C interface supports both standard mode (up to 100 kbits/s), and fast mode (up to 400 kbits/s). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

#### 9.3.14.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on SCL line is LOW. One clock pulse is generated for each data bit transferred.

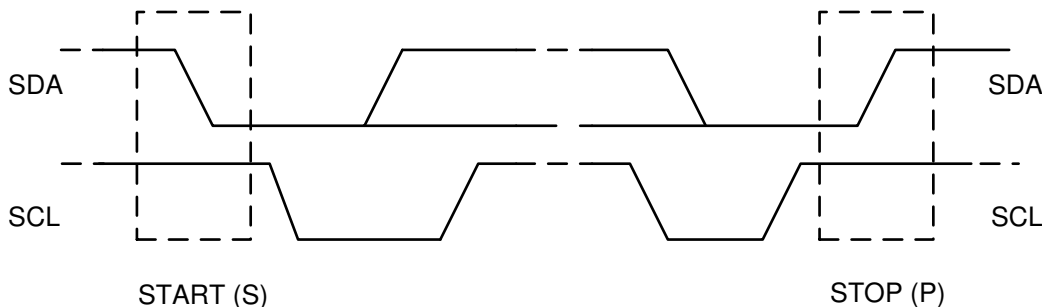


**Figure 9-15. Bit Transfers on the I<sup>2</sup>C Bus**

#### 9.3.14.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition, and free after the STOP condition.

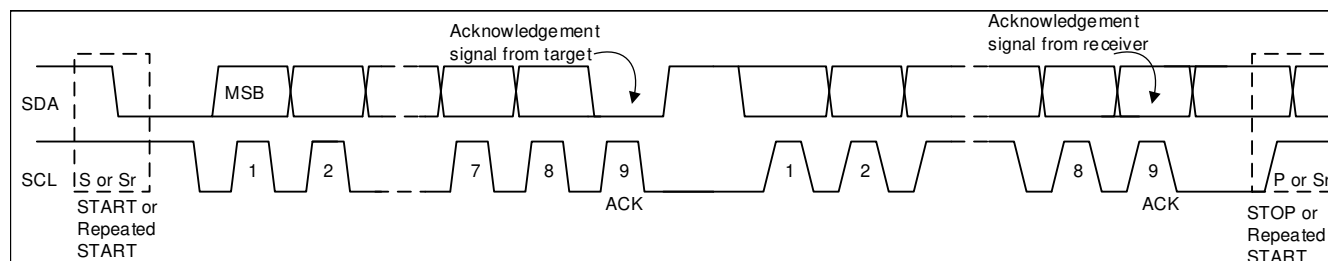


**Figure 9-16. START and STOP Conditions on the I<sup>2</sup>C Bus**

#### 9.3.14.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the

Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the controller into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.



**Figure 9-17. Data Transfer on the I²C Bus**

#### 9.3.14.4 Acknowledge (ACK) and Not Acknowledge (NACK)

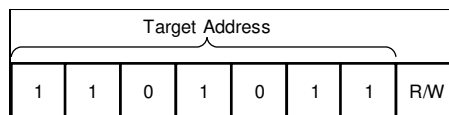
The ACK signaling takes place after each transmitted byte. The ACK bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9<sup>th</sup> clock pulse, are generated by the controller.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9<sup>th</sup> clock pulse.

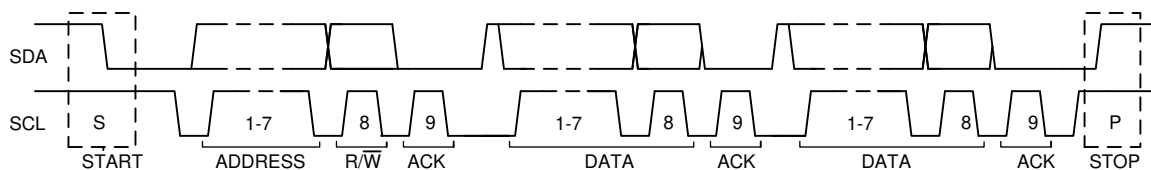
A NACK is signaled when the SDA line remains HIGH during the 9<sup>th</sup> clock pulse. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

#### 9.3.14.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/  $\bar{W}$ ). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The BQ25792 7-bit address is defined as 1101 011' (0x6B). The address bit arrangement is shown below.

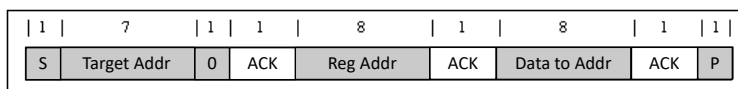


**Figure 9-18. 7-Bit Addressing (0x6B)**

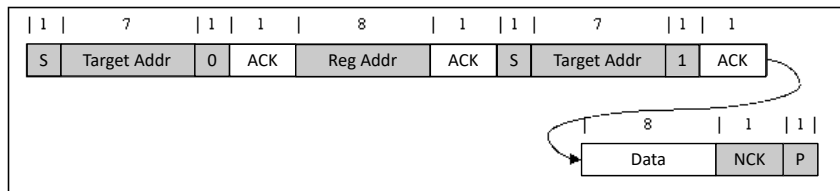


**Figure 9-19. Complete Data Transfer on the I²C Bus**

#### 9.3.14.6 Single Write and Read



**Figure 9-20. Single Write**

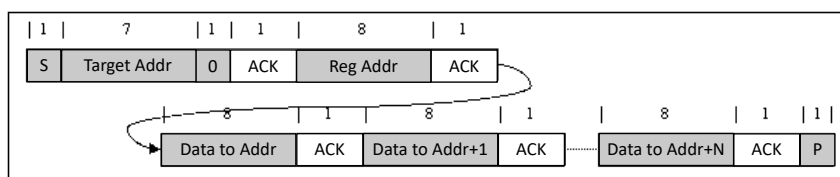


**Figure 9-21. Single Read**

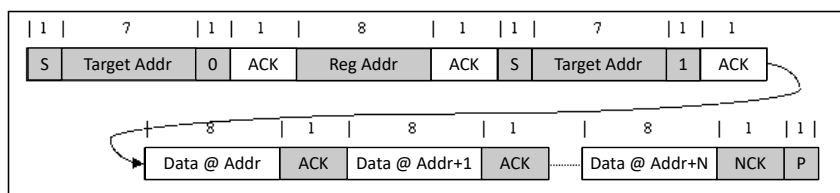
If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

#### 9.3.14.7 Multi-Write and Multi-Read

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire register map may be read in a single operation with a 49-byte read that starts at register address 0x0.



**Figure 9-22. Multi-Write**



**Figure 9-23. Multi-Read**

## 9.4 Device Functional Modes

### 9.4.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD\_STAT bit becomes HIGH, WD\_FLAG is set to 1, and an  $\overline{\text{INT}}$  is asserted low to alert the host (unless masked by WD\_MASK). The WD\_FLAG bit would read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD\_STAT bit is LOW.

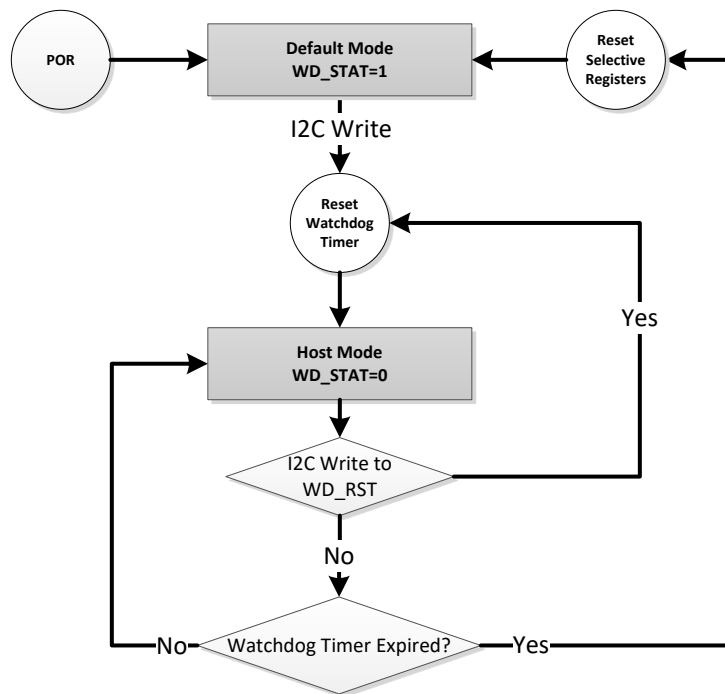
After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. At the end of the 1-hour or 2-hour or 12-hour timer expired, the charging is stopped and the buck-boost converter continues to operate to supply system load.

A write to any I<sup>2</sup>C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD\_RST bit before the watchdog timer expires (WD\_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer is expired, the device returns to default mode and all registers are reset to default values except the ones described in [Section 9.5](#). The watchdog timer will be reset on any write if the watchdog

timer has expired. When watchdog timer expires, WD\_STAT and WD\_FLAG is set to 1, and an  $\overline{\text{INT}}$  is asserted low to alert the host (unless masked by WD\_MASK).



**Figure 9-24. Watchdog Timer Flow Chart**

### 9.4.2 Register Bit Reset

Beside the register reset by the watchdog timer in the default mode, the register and the timer could be reset to the default value by writing the REG\_RST bit to 1. The register bits, which can be reset by the REG\_RST bit, are noted in the Register Map section. After the register reset, the REG\_RST bit will go back from 1 to 0 automatically.

The register reset by the REG\_RST bit will not initiate the ACFET-RBFET detection, which is only done at the charger first time POR. It will not repeat the open-circuit adapter measurements for the default VINDPM setting, which is only done when an adapter is plugged in. In addition, if the charger is in the process of forced ICO, the forced open-circuit adapter measurements or the forced D+/D- detection, set the REG\_RST to 1 will terminate all of these processes, because reset the register to default values will set FORCE\_ICO, FORCE\_INDET and FORCE\_VINDPM\_DET bits to 0.

## 9.5 Register Map

### 9.5.1 I2C Registers

Table 9-12 lists the I2C registers. All register offset addresses not listed in Table 9-12 should be considered as reserved locations and the register contents should not be modified.

**Table 9-12. I2C Registers**

| Offset | Acronym                      | Register Name          | Section                          |
|--------|------------------------------|------------------------|----------------------------------|
| 0h     | REG00_Minimal_System_Voltage | Minimal System Voltage | <a href="#">Section 9.5.1.1</a>  |
| 1h     | REG01_Charge_Voltage_Limit   | Charge Voltage Limit   | <a href="#">Section 9.5.1.2</a>  |
| 3h     | REG03_Charge_Current_Limit   | Charge Current Limit   | <a href="#">Section 9.5.1.3</a>  |
| 5h     | REG05_Input_Voltage_Limit    | Input Voltage Limit    | <a href="#">Section 9.5.1.4</a>  |
| 6h     | REG06_Input_Current_Limit    | Input Current Limit    | <a href="#">Section 9.5.1.5</a>  |
| 8h     | REG08_Precharge_Control      | Precharge Control      | <a href="#">Section 9.5.1.6</a>  |
| 9h     | REG09_Termination_Control    | Termination Control    | <a href="#">Section 9.5.1.7</a>  |
| Ah     | REG0A_Re-charge_Control      | Re-charge Control      | <a href="#">Section 9.5.1.8</a>  |
| Bh     | REG0B_VOTG_regulation        | VOTG regulation        | <a href="#">Section 9.5.1.9</a>  |
| Dh     | REG0D_IOTG_regulation        | IOTG regulation        | <a href="#">Section 9.5.1.10</a> |
| Eh     | REG0E_Timer_Control          | Timer Control          | <a href="#">Section 9.5.1.11</a> |
| Fh     | REG0F_Charger_Control_0      | Charger Control 0      | <a href="#">Section 9.5.1.12</a> |
| 10h    | REG10_Charger_Control_1      | Charger Control 1      | <a href="#">Section 9.5.1.13</a> |
| 11h    | REG11_Charger_Control_2      | Charger Control 2      | <a href="#">Section 9.5.1.14</a> |
| 12h    | REG12_Charger_Control_3      | Charger Control 3      | <a href="#">Section 9.5.1.15</a> |
| 13h    | REG13_Charger_Control_4      | Charger Control 4      | <a href="#">Section 9.5.1.16</a> |
| 14h    | REG14_Charger_Control_5      | Charger Control 5      | <a href="#">Section 9.5.1.17</a> |
| 15h    | REG15_Reserved               | Reserved               | <a href="#">Section 9.5.1.18</a> |
| 16h    | REG16_Temperature_Control    | Temperature Control    | <a href="#">Section 9.5.1.19</a> |
| 17h    | REG17_NTC_Control_0          | NTC Control 0          | <a href="#">Section 9.5.1.20</a> |
| 18h    | REG18_NTC_Control_1          | NTC Control 1          | <a href="#">Section 9.5.1.21</a> |
| 19h    | REG19_ICO_Current_Limit      | ICO Current Limit      | <a href="#">Section 9.5.1.22</a> |
| 1Bh    | REG1B_Charger_Status_0       | Charger Status 0       | <a href="#">Section 9.5.1.23</a> |
| 1Ch    | REG1C_Charger_Status_1       | Charger Status 1       | <a href="#">Section 9.5.1.24</a> |
| 1Dh    | REG1D_Charger_Status_2       | Charger Status 2       | <a href="#">Section 9.5.1.25</a> |
| 1Eh    | REG1E_Charger_Status_3       | Charger Status 3       | <a href="#">Section 9.5.1.26</a> |
| 1Fh    | REG1F_Charger_Status_4       | Charger Status 4       | <a href="#">Section 9.5.1.27</a> |
| 20h    | REG20_FAULT_Status_0         | FAULT Status 0         | <a href="#">Section 9.5.1.28</a> |
| 21h    | REG21_FAULT_Status_1         | FAULT Status 1         | <a href="#">Section 9.5.1.29</a> |
| 22h    | REG22_Charger_Flag_0         | Charger Flag 0         | <a href="#">Section 9.5.1.30</a> |
| 23h    | REG23_Charger_Flag_1         | Charger Flag 1         | <a href="#">Section 9.5.1.31</a> |
| 24h    | REG24_Charger_Flag_2         | Charger Flag 2         | <a href="#">Section 9.5.1.32</a> |
| 25h    | REG25_Charger_Flag_3         | Charger Flag 3         | <a href="#">Section 9.5.1.33</a> |
| 26h    | REG26_FAULT_Flag_0           | FAULT Flag 0           | <a href="#">Section 9.5.1.34</a> |
| 27h    | REG27_FAULT_Flag_1           | FAULT Flag 1           | <a href="#">Section 9.5.1.35</a> |
| 28h    | REG28_Charger_Mask_0         | Charger Mask 0         | <a href="#">Section 9.5.1.36</a> |
| 29h    | REG29_Charger_Mask_1         | Charger Mask 1         | <a href="#">Section 9.5.1.37</a> |
| 2Ah    | REG2A_Charger_Mask_2         | Charger Mask 2         | <a href="#">Section 9.5.1.38</a> |
| 2Bh    | REG2B_Charger_Mask_3         | Charger Mask 3         | <a href="#">Section 9.5.1.39</a> |
| 2Ch    | REG2C_FAULT_Mask_0           | FAULT Mask 0           | <a href="#">Section 9.5.1.40</a> |
| 2Dh    | REG2D_FAULT_Mask_1           | FAULT Mask 1           | <a href="#">Section 9.5.1.41</a> |

**Table 9-12. I2C Registers (continued)**

| Offset | Acronym                      | Register Name          | Section                          |
|--------|------------------------------|------------------------|----------------------------------|
| 2Eh    | REG2E_ADC_Control            | ADC Control            | <a href="#">Section 9.5.1.42</a> |
| 2Fh    | REG2F_ADC_Function_Disable_0 | ADC Function Disable 0 | <a href="#">Section 9.5.1.43</a> |
| 30h    | REG30_ADC_Function_Disable_1 | ADC Function Disable 1 | <a href="#">Section 9.5.1.44</a> |
| 31h    | REG31_IBUS_ADC               | IBUS ADC               | <a href="#">Section 9.5.1.45</a> |
| 33h    | REG33_IBAT_ADC               | IBAT ADC               | <a href="#">Section 9.5.1.46</a> |
| 35h    | REG35_VBUS_ADC               | VBUS ADC               | <a href="#">Section 9.5.1.47</a> |
| 37h    | REG37_VAC1_ADC               | VAC1 ADC               | <a href="#">Section 9.5.1.48</a> |
| 39h    | REG39_VAC2_ADC               | VAC2 ADC               | <a href="#">Section 9.5.1.49</a> |
| 3Bh    | REG3B_VBAT_ADC               | VBAT ADC               | <a href="#">Section 9.5.1.50</a> |
| 3Dh    | REG3D_VSYS_ADC               | VSYS ADC               | <a href="#">Section 9.5.1.51</a> |
| 3Fh    | REG3F_TS_ADC                 | TS ADC                 | <a href="#">Section 9.5.1.52</a> |
| 41h    | REG41_TDIE_ADC               | TDIE_ADC               | <a href="#">Section 9.5.1.53</a> |
| 43h    | REG43_D+_ADC                 | D+ ADC                 | <a href="#">Section 9.5.1.54</a> |
| 45h    | REG45_D-_ADC                 | D- ADC                 | <a href="#">Section 9.5.1.55</a> |
| 47h    | REG47_DPDM_Driver            | DPDM Driver            | <a href="#">Section 9.5.1.56</a> |
| 48h    | REG48_Part_Information       | Part Information       | <a href="#">Section 9.5.1.57</a> |

Complex bit access types are encoded to fit into small table cells. The following table shows the codes that are used for access types in this section.

**Table 9-13. I2C Access Type Codes**

| Access Type  | Code | Description  |
|--------------|------|--|
| Read Type    |      |  |
| R            | R    | Read   |
| Write Type   |      |  |
| W            | W    | Write  |
| Others       |      |  |
| Range        |      | The register bits are only valid in this defined range.  |
| Clamped Low  |      | Any write on the register lower than the minimal value of the valid range, will be ignored by the charger  |
| Clamped High |      | Any write on the register higher than the maximum value of the valid range, will be ignored by the charger |

### 9.5.1.1 REG00\_Minimal\_System\_Voltage Register (Offset = 0h) [reset = X]

REG00\_Minimal\_System\_Voltage is shown in [Figure 9-25](#) and described in [Table 9-14](#).

Return to the [Table 9-12](#).

Minimal System Voltage

**Figure 9-25. REG00\_Minimal\_System\_Voltage Register**

|          |   |             |   |   |   |   |   |
|----------|---|-------------|---|---|---|---|---|
| 7        | 6 | 5           | 4 | 3 | 2 | 1 | 0 |
| RESERVED |   | VSYSMIN_5:0 |   |   |   |   |   |
| R/W-0h   |   | R/W-X       |   |   |   |   |   |

**Table 9-14. REG00\_Minimal\_System\_Voltage Register Field Descriptions**

| Bit | Field       | Type | Reset | Notes                | Description   |
|-----|-------------|------|-------|----------------------|---|
| 7-6 | RESERVED    | R/W  | 0h    |                      | RESERVED  |
| 5-0 | VSYSMIN_5:0 | R/W  | X     | Reset by:<br>REG_RST | Minimal System Voltage:<br>During POR, the device reads the resistance tie to<br>PROG pin, to identify the default battery cell count and<br>determine the default power on VSYSMIN list below:<br>1s: 3.5V<br>2s: 7V<br>3s: 9V<br>4s: 12V<br>Type : RW<br>Range : 2500mV-16000mV<br>Fixed Offset : 2500mV<br>Bit Step Size : 250mV<br>Clamped High |



### 9.5.1.2 REG01\_Charge\_Voltage\_Limit Register (Offset = 1h) [reset = X]

REG01\_Charge\_Voltage\_Limit is shown in [Figure 9-26](#) and described in [Table 9-15](#).

Return to the [Table 9-12](#).

Charge Voltage Limit

**Figure 9-26. REG01\_Charge\_Voltage\_Limit Register**

|           |    |    |    |    |           |   |   |
|-----------|----|----|----|----|-----------|---|---|
| 15        | 14 | 13 | 12 | 11 | 10        | 9 | 8 |
| RESERVED  |    |    |    |    | VREG_10:0 |   |   |
| R-0h      |    |    |    |    | R/W-X     |   |   |
| 7         | 6  | 5  | 4  | 3  | 2         | 1 | 0 |
| VREG_10:0 |    |    |    |    |           |   |   |
| R/W-X     |    |    |    |    |           |   |   |

**Table 9-15. REG01\_Charge\_Voltage\_Limit Register Field Descriptions**

| Bit   | Field     | Type | Reset | Notes                | Description  |
|-------|-----------|------|-------|----------------------|--|
| 15-11 | RESERVED  | R    | 0h    |                      | RESERVED   |
| 10-0  | VREG_10:0 | R/W  | X     | Reset by:<br>REG_RST | Battery Voltage Limit:<br>During POR, the device reads the resistance tie to PROG pin, to identify the default battery cell count and determine the default power-on battery voltage regulation limit:<br>1s: 4.2V<br>2s: 8.4V<br>3s: 12.6V<br>4s: 16.8V<br>Type : RW<br>Range : 3000mV-18800mV<br>Fixed Offset : 0mV<br>Bit Step Size : 10mV<br>Clamped Low |

### 9.5.1.3 REG03\_Charge\_Current\_Limit Register (Offset = 3h) [reset = X]

REG03\_Charge\_Current\_Limit is shown in [Figure 9-27](#) and described in [Table 9-16](#).

Return to the [Table 9-12](#).

Charge Current Limit

**Figure 9-27. REG03\_Charge\_Current\_Limit Register**

|          |    |    |    |    |    |   |          |
|----------|----|----|----|----|----|---|----------|
| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8        |
| RESERVED |    |    |    |    |    |   | ICHG_8:0 |
| R-0h     |    |    |    |    |    |   | R/W-X    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1 | 0        |
| ICHG_8:0 |    |    |    |    |    |   |          |
| R/W-X    |    |    |    |    |    |   |          |

**Table 9-16. REG03\_Charge\_Current\_Limit Register Field Descriptions**

| Bit  | Field    | Type | Reset | Notes                            | Description  |
|------|----------|------|-------|----------------------------------|--|
| 15-9 | RESERVED | R    | 0h    |                                  | RESERVED   |
| 8-0  | ICHG_8:0 | R/W  | X     | Reset by:<br>WATCHDOG<br>REG_RST | Charge Current Limit<br>During POR, the device reads the resistance tie to PROG pin, to identify the default battery cell count and determine the default power-on battery charging current:<br>1s and 2s:<br>3s and 4s: 1A<br>Type : RW<br>Range : 50mA-5000mA<br>Fixed Offset : 0mA<br>Bit Step Size : 10mA<br>Clamped Low |

#### 9.5.1.4 REG05\_Input\_Voltage\_Limit Register (Offset = 5h) [reset = 24h]

REG05\_Input\_Voltage\_Limit is shown in [Figure 9-28](#) and described in [Table 9-17](#).

Return to the [Table 9-12](#).

Input Voltage Limit

**Figure 9-28. REG05\_Input\_Voltage\_Limit Register**

| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|---|---|---|---|
| VINDPM_7:0 |   |   |   |   |   |   |   |
| R/W-24h    |   |   |   |   |   |   |   |

**Table 9-17. REG05\_Input\_Voltage\_Limit Register Field Descriptions**

| Bit | Field      | Type | Reset | Description   |
|-----|------------|------|-------|---|
| 7-0 | VINDPM_7:0 | R/W  | 24h   | <p>Absolute VINDPM Threshold</p> <p>VINDPM register is reset to 3600mV upon adapter unplugged and it is set to the value based on the VBUS measurement when the adapter plugs in. It is not reset by the REG_RST and the WATCHDOG</p> <p>Type : RW</p> <p>POR: 3600mV (24h)</p> <p>Range : 3600mV-22000mV</p> <p>Fixed Offset : 0mV</p> <p>Bit Step Size : 100mV</p> <p>Clamped Low</p> |

### 9.5.1.5 REG06\_Input\_Current\_Limit Register (Offset = 6h) [reset = 12Ch]

REG06\_Input\_Current\_Limit is shown in [Figure 9-29](#) and described in [Table 9-18](#).

Return to the [Table 9-12](#).

Input Current Limit

**Figure 9-29. REG06\_Input\_Current\_Limit Register**

|            |    |    |    |    |    |   |            |
|------------|----|----|----|----|----|---|------------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| RESERVED   |    |    |    |    |    |   | IINDPM_8:0 |
| R-0h       |    |    |    |    |    |   | R/W-12Ch   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0          |
| IINDPM_8:0 |    |    |    |    |    |   |            |
| R/W-12Ch   |    |    |    |    |    |   |            |

**Table 9-18. REG06\_Input\_Current\_Limit Register Field Descriptions**

| Bit  | Field      | Type | Reset | Notes                | Description   |
|------|------------|------|-------|----------------------|---|
| 15-9 | RESERVED   | R    | 0h    |                      | RESERVED  |
| 8-0  | IINDPM_8:0 | R/W  | 12Ch  | Reset by:<br>REG_RST | Based on D+/D- detection results:<br>USB SDP = 500mA<br>USB CDP = 1.5A<br>USB DCP = 3.25A<br>Adjustable High Voltage DCP = 1.5A<br>Unknown Adapter = 3A<br>Non-Standard Adapter = 1A/2A/2.1A/2.4A<br>Type : RW<br>POR: 3000mA (12Ch)<br>Range : 100mA-3300mA<br>Fixed Offset : 0mA<br>Bit Step Size : 10mA<br>Clamped Low |

### 9.5.1.6 REG08\_Precharge\_Control Register (Offset = 8h) [reset = C3h]

REG08\_Precharge\_Control is shown in [Figure 9-30](#) and described in [Table 9-19](#).

Return to the [Table 9-12](#).

Precharge Control

**Figure 9-30. REG08\_Precharge\_Control Register**

| 7             | 6 | 5 | 4           | 3 | 2 | 1 | 0 |
|---------------|---|---|-------------|---|---|---|---|
| VBAT_LOWV_1:0 |   |   | IPRECHG_5:0 |   |   |   |   |
| R/W-3h        |   |   | R/W-3h      |   |   |   |   |

**Table 9-19. REG08\_Precharge\_Control Register Field Descriptions**

| Bit | Field         | Type | Reset | Notes                            | Description  |
|-----|---------------|------|-------|----------------------------------|--|
| 7-6 | VBAT_LOWV_1:0 | R/W  | 3h    | Reset by:<br>REG_RST             | Battery voltage thresholds for the transition from precharge to fast charge, which is defined as a ratio of battery regulation limit (VREG)<br>Type : RW<br>POR: 11b<br>0h = 15%*VREG<br>1h = 62.2%*VREG<br>2h = 66.7%*VREG<br>3h = 71.4%*VREG |
| 5-0 | IPRECHG_5:0   | R/W  | 3h    | Reset by:<br>WATCHDOG<br>REG_RST | Precharge current limit<br>Type : RW<br>POR: 120mA (3h)<br>Range : 40mA-2000mA<br>Fixed Offset : 0mA<br>Bit Step Size : 40mA<br>Clamped Low  |

### 9.5.1.7 REG09\_Termination\_Control Register (Offset = 9h) [reset = 5h]

REG09\_Termination\_Control is shown in [Figure 9-31](#) and described in [Table 9-20](#).

Return to the [Table 9-12](#).

Termination Control

**Figure 9-31. REG09\_Termination\_Control Register**

| 7        | 6       | 5        | 4         | 3 | 2 | 1 | 0 |
|----------|---------|----------|-----------|---|---|---|---|
| RESERVED | REG_RST | RESERVED | ITERM_4:0 |   |   |   |   |
| R-0h     | R/W-0h  | R/W-0h   | R/W-5h    |   |   |   |   |

**Table 9-20. REG09\_Termination\_Control Register Field Descriptions**

| Bit | Field     | Type | Reset | Notes                            | Description   |
|-----|-----------|------|-------|----------------------------------|---|
| 7   | RESERVED  | R    | 0h    |                                  | RESERVED  |
| 6   | REG_RST   | R/W  | 0h    |                                  | Reset registers to default values and reset timer<br>Type : RW<br>POR: 0b<br>0h = Not reset<br>1h = Reset                               |
| 5   | RESERVED  | R/W  | 0h    |                                  | RESERVED  |
| 4-0 | ITERM_4:0 | R/W  | 5h    | Reset by:<br>WATCHDOG<br>REG_RST | Termination current<br>Type : RW<br>POR: 200mA (5h)<br>Range : 40mA-1000mA<br>Fixed Offset : 0mA<br>Bit Step Size : 40mA<br>Clamped Low |

### 9.5.1.8 REG0A\_Re-charge\_Control Register (Offset = Ah) [reset = X]

REG0A\_Re-charge\_Control is shown in [Figure 9-32](#) and described in [Table 9-21](#).

Return to the [Table 9-12](#).

Re-charge Control

**Figure 9-32. REG0A\_Re-charge\_Control Register**

| 7        | 6 | 5          | 4 | 3          | 2 | 1 | 0 |
|----------|---|------------|---|------------|---|---|---|
| CELL_1:0 |   | TRECHG_1:0 |   | VRECHG_3:0 |   |   |   |
| R/W-X    |   | R/W-2h     |   | R/W-3h     |   |   |   |

**Table 9-21. REG0A\_Re-charge\_Control Register Field Descriptions**

| Bit | Field      | Type | Reset | Notes                            | Description   |
|-----|------------|------|-------|----------------------------------|---|
| 7-6 | CELL_1:0   | R/W  | X     |                                  | At POR, the charger reads the PROG pin resistance to determine the battery cell count and update this CELL bits accordingly.<br>Type : RW<br>0h = 1s<br>1h = 2s<br>2h = 3s<br>3h = 4s |
| 5-4 | TRECHG_1:0 | R/W  | 2h    | Reset by:<br>WATCHDOG<br>REG_RST | Battery recharge deglich time<br>Type : RW<br>POR: 10b<br>0h = 64ms<br>1h = 256ms<br>2h = 1024ms (default)<br>3h = 2048ms   |
| 3-0 | VRECHG_3:0 | R/W  | 3h    | Reset by:<br>WATCHDOG<br>REG_RST | Battery Recharge Threshold Offset (Below VREG)<br>Type : RW<br>POR: 200mV (3h)<br>Range : 50mV-800mV<br>Fixed Offset : 50mV<br>Bit Step Size : 50mV                                   |



### 9.5.1.9 REG0B\_VOTG\_regulation Register (Offset = Bh) [reset = DCh]

REG0B\_VOTG\_regulation is shown in [Figure 9-33](#) and described in [Table 9-22](#).

Return to the [Table 9-12](#).

VOTG regulation

**Figure 9-33. REG0B\_VOTG\_regulation Register**

|           |    |    |    |    |    |           |   |
|-----------|----|----|----|----|----|-----------|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9         | 8 |
| RESERVED  |    |    |    |    |    | VOTG_10:0 |   |
| R-0h      |    |    |    |    |    | R/W-DCh   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1         | 0 |
| VOTG_10:0 |    |    |    |    |    |           |   |
| R/W-DCh   |    |    |    |    |    |           |   |

**Table 9-22. REG0B\_VOTG\_regulation Register Field Descriptions**

| Bit   | Field     | Type | Reset | Notes                            | Description  |
|-------|-----------|------|-------|----------------------------------|--|
| 15-11 | RESERVED  | R    | 0h    |                                  | RESERVED   |
| 10-0  | VOTG_10:0 | R/W  | DCh   | Reset by:<br>WATCHDOG<br>REG_RST | OTG mode regulation voltage<br>Type : RW<br>POR: 5000mV (DCh)<br>Range : 2800mV-22000mV<br>Fixed Offset : 2800mV<br>Bit Step Size : 10mV<br>Clamped High |

### 9.5.1.10 REG0D\_IOTG\_regulation Register (Offset = Dh) [reset = 4Bh]

REG0D\_IOTG\_regulation is shown in [Figure 9-34](#) and described in [Table 9-23](#).

Return to the [Table 9-12](#).

IOTG regulation

**Figure 9-34. REG0D\_IOTG\_regulation Register**

| 7          | 6 | 5        | 4 | 3 | 2 | 1 | 0 |
|------------|---|----------|---|---|---|---|---|
| PRECHG_TMR |   | IOTG_6:0 |   |   |   |   |   |
| R/W-0h     |   | R/W-4Bh  |   |   |   |   |   |

**Table 9-23. REG0D\_IOTG\_regulation Register Field Descriptions**

| Bit | Field      | Type | Reset | Notes                            | Description  |
|-----|------------|------|-------|----------------------------------|--|
| 7   | PRECHG_TMR | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Pre-charge safety timer setting<br>Type : RW<br>POR: 0b<br>0h = 2 hrs (default)<br>1h = 0.5 hrs  |
| 6-0 | IOTG_6:0   | R/W  | 4Bh   | Reset by:<br>WATCHDOG<br>REG_RST | OTG current limit<br>Type : RW<br>POR: 3000mA (4Bh)<br>Range : 120mA-3320mA<br>Fixed Offset : 0mA<br>Bit Step Size : 40mA<br>Clamped Low |

### 9.5.1.11 REG0E\_Timer\_Control Register (Offset = Eh) [reset = 3Dh]

REG0E\_Timer\_Control is shown in [Figure 9-35](#) and described in [Table 9-24](#).

Return to the [Table 9-12](#).

Timer Control

**Figure 9-35. REG0E\_Timer\_Control Register**

| 7              | 6 | 5             | 4             | 3          | 2           | 1 | 0        |
|----------------|---|---------------|---------------|------------|-------------|---|----------|
| TOPOFF_TMR_1:0 |   | EN_TRICHG_TMR | EN_PRECHG_TMR | EN_CHG_TMR | CHG_TMR_1:0 |   | TMR2X_EN |
| R/W-0h         |   | R/W-1h        | R/W-1h        | R/W-1h     | R/W-2h      |   | R/W-1h   |

**Table 9-24. REG0E\_Timer\_Control Register Field Descriptions**

| Bit | Field          | Type | Reset | Notes                            | Description   |
|-----|----------------|------|-------|----------------------------------|---|
| 7-6 | TOPOFF_TMR_1:0 | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Top-off timer control<br>Type : RW<br>POR: 00b<br>0h = Disabled (default)<br>1h = 15 mins<br>2h = 30 mins<br>3h = 45 mins   |
| 5   | EN_TRICHG_TMR  | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable trickle charge timer (fixed as 1hr)<br>Type : RW<br>POR: 1b<br>0h = Disabled<br>1h = Enabled (default)   |
| 4   | EN_PRECHG_TMR  | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable pre-charge timer<br>Type : RW<br>POR: 1b<br>0h = Disabled<br>1h = Enabled (default)  |
| 3   | EN_CHG_TMR     | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable fast charge timer<br>Type : RW<br>POR: 1b<br>0h = Disabled<br>1h = Enabled (default)   |
| 2-1 | CHG_TMR_1:0    | R/W  | 2h    | Reset by:<br>WATCHDOG<br>REG_RST | Fast charge timer setting<br>Type : RW<br>POR: 10b<br>0h = 5 hrs<br>1h = 8 hrs<br>2h = 12 hrs (default)<br>3h = 24 hrs  |
| 0   | TMR2X_EN       | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | TMR2X_EN<br>Type : RW<br>POR: 1b<br>0h = Trickle charge, pre-charge and fast charge timer NOT slowed by 2X during input DPM or thermal regulation.<br>1h = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default) |

### 9.5.1.12 REG0F\_Charger\_Control\_0 Register (Offset = Fh) [reset = A2h]

REG0F\_Charger\_Control\_0 is shown in [Figure 9-36](#) and described in [Table 9-25](#).

Return to the [Table 9-12](#).

Charger Control 0

**Figure 9-36. REG0F\_Charger\_Control\_0 Register**

| 7               | 6             | 5      | 4      | 3         | 2      | 1       | 0        |
|-----------------|---------------|--------|--------|-----------|--------|---------|----------|
| EN_AUTO_IBATDIS | FORCE_IBATDIS | EN_CHG | EN_ICO | FORCE_ICO | EN_HIZ | EN_TERM | RESERVED |
| R/W-1h          | R/W-0h        | R/W-1h | R/W-0h | R/W-0h    | R/W-0h | R/W-1h  | R-0h     |

**Table 9-25. REG0F\_Charger\_Control\_0 Register Field Descriptions**

| Bit | Field           | Type | Reset | Notes                            | Description  |
|-----|-----------------|------|-------|----------------------------------|--|
| 7   | EN_AUTO_IBATDIS | R/W  | 1h    | Reset by:<br>REG_RST             | Enable the auto battery discharging during the battery OVP fault<br>Type : RW<br>POR: 1b<br>0h = The charger will NOT apply a discharging current on BAT during battery OVP<br>1h = The charger will apply a discharging current on BAT during battery OVP |
| 6   | FORCE_IBATDIS   | R/W  | 0h    | Reset by:<br>REG_RST             | Force a battery discharging current<br>Type : RW<br>POR: 0b<br>0h = IDLE (default)<br>1h = Force the charger to apply a discharging current on BAT regardless the battery OVP status   |
| 5   | EN_CHG          | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Charger Enable Configuration<br>Type : RW<br>POR: 1b<br>0h = Charge Disable<br>1h = Charge Enable (default)  |
| 4   | EN_ICO          | R/W  | 0h    | Reset by:<br>REG_RST             | Input Current Optimizer (ICO) Enable<br>Type : RW<br>POR: 0b<br>0h = Disable ICO (default)<br>1h = Enable ICO  |
| 3   | FORCE_ICO       | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Force start input current optimizer (ICO)<br>Note: This bit can only be set and returns 0 after ICO starts. This bit only valid when EN_ICO = 1<br>Type : RW<br>POR: 0b<br>0h = Do NOT force ICO (Default)<br>1h = Force ICO start                         |
| 2   | EN_HIZ          | R/W  | 0h    | Reset by:<br>REG_RST             | Enable HIZ mode.<br>This bit will be also reset to 0, when the adapter is plugged in at VBUS.<br>Type : RW<br>POR: 0b<br>0h = Disable (default)<br>1h = Enable   |
| 1   | EN_TERM         | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable termination<br>Type : RW<br>POR: 1b<br>0h = Disable<br>1h = Enable (default)  |

**Table 9-25. REG0F\_Charger\_Control\_0 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Notes | Description |
|-----|----------|------|-------|-------|-------------|
| 0   | RESERVED | R    | 0h    |       | Reserved    |

### 9.5.1.13 REG10\_Charger\_Control\_1 Register (Offset = 10h) [reset = 85h]

REG10\_Charger\_Control\_1 is shown in [Figure 9-37](#) and described in [Table 9-26](#).

Return to the [Table 9-12](#).

Charger Control 1

**Figure 9-37. REG10\_Charger\_Control\_1 Register**

| 7        | 6 | 5           | 4 | 3      | 2            | 1 | 0 |
|----------|---|-------------|---|--------|--------------|---|---|
| RESERVED |   | VAC_OVP_1:0 |   | WD_RST | WATCHDOG_2:0 |   |   |
| R-0h     |   | R/W-3h      |   | R/W-0h | R/W-5h       |   |   |

**Table 9-26. REG10\_Charger\_Control\_1 Register Field Descriptions**

| Bit | Field        | Type | Reset | Notes                            | Description   |
|-----|--------------|------|-------|----------------------------------|---|
| 7-6 | RESERVED     | R    | 0h    |                                  | Reserved  |
| 5-4 | VAC_OVP_1:0  | R/W  | 0h    | Reset by:<br>REG_RST             | VAC_OVP thresholds<br>Type : RW<br>POR: 00b<br>0h = 26V (default)<br>1h = 18V<br>2h = 12V<br>3h = 7V  |
| 3   | WD_RST       | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | I2C watch dog timer reset<br>Type : RW<br>POR: 0b<br>0h = Normal (default)<br>1h = Reset (this bit goes back to 0 after timer resets)                           |
| 2-0 | WATCHDOG_2:0 | R/W  | 5h    | Reset by:<br>REG_RST             | Watchdog timer settings<br>Type : RW<br>POR: 101b<br>0h = Disable<br>1h = 0.5s<br>2h = 1s<br>3h = 2s<br>4h = 20s<br>5h = 40s (default)<br>6h = 80s<br>7h = 160s |

### 9.5.1.14 REG11\_Charger\_Control\_2 Register (Offset = 11h) [reset = 40h]

REG11\_Charger\_Control\_2 is shown in [Figure 9-38](#) and described in [Table 9-27](#).

Return to the [Table 9-12](#).

Charger Control 2

**Figure 9-38. REG11\_Charger\_Control\_2 Register**

| 7           | 6             | 5      | 4      | 3        | 2             | 1 | 0        |
|-------------|---------------|--------|--------|----------|---------------|---|----------|
| FORCE_INDET | AUTO_INDET_EN | EN_12V | EN_9V  | HVDCP_EN | SDRV_CTRL_1:0 |   | SDRV_DLY |
| R/W-0h      | R/W-1h        | R/W-0h | R/W-0h | R/W-0h   | R/W-0h        |   | R/W-0h   |

**Table 9-27. REG11\_Charger\_Control\_2 Register Field Descriptions**

| Bit | Field         | Type | Reset | Notes                            | Description   |
|-----|---------------|------|-------|----------------------------------|---|
| 7   | FORCE_INDET   | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Force D+/D- detection<br>Type : RW<br>POR: 0b<br>0h = Do NOT force D+/D- detection (default)<br>1h = Force D+/D- algorithm, when D+/D- detection is done, this bit will be reset to 0                             |
| 6   | AUTO_INDET_EN | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Automatic D+/D- Detection Enable<br>Type : RW<br>POR: 1b<br>0h = Disable D+/D- detection when VBUS is plugged-in<br>1h = Enable D+/D- detection when VBUS is plugged-in (default)                                 |
| 5   | EN_12V        | R/W  | 0h    | Reset by:<br>REG_RST             | EN_12V HVDC<br>Type : RW<br>POR: 0b<br>0h = Disable 12V mode in HVDCP (default)<br>1h = Enable 12V mode in HVDCP  |
| 4   | EN_9V         | R/W  | 0h    | Reset by:<br>REG_RST             | EN_9V HVDC<br>Type : RW<br>POR: 0b<br>0h = Disable 9V mode in HVDCP (default)<br>1h = Enable 9V mode in HVDCP   |
| 3   | HVDCP_EN      | R/W  | 0h    | Reset by:<br>REG_RST             | High voltage DCP enable.<br>Type : RW<br>POR: 0b<br>0h = Disable HVDCP handshake (default)<br>1h = Enable HVDCP handshake   |
| 2-1 | SDRV_CTRL_1:0 | R/W  | 0h    | Reset by:<br>REG_RST             | SFET control<br>The external ship FET control logic to force the device enter different modes.<br>Type : RW<br>POR: 00b<br>0h = IDLE (default)<br>1h = Shutdown Mode<br>2h = Ship Mode<br>3h = System Power Reset |



**Table 9-27. REG11\_Charger\_Control\_2 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Notes                | Description   |
|-----|----------|------|-------|----------------------|---|
| 0   | SDRV_DLY | R/W  | 0h    | Reset by:<br>REG_RST | Delay time added to the taking action in bit [2:1] of the SFET control<br>Type : RW<br>POR: 0b<br>0h = Add 10s delay time (default)<br>1h = Do NOT add 10s delay time |

### 9.5.1.15 REG12\_Charger\_Control\_3 Register (Offset = 12h) [reset = 0h]

REG12\_Charger\_Control\_3 is shown in [Figure 9-39](#) and described in [Table 9-28](#).

Return to the [Table 9-12](#).

Charger Control 3

**Figure 9-39. REG12\_Charger\_Control\_3 Register**

| 7         | 6      | 5           | 4           | 3        | 2       | 1           | 0           |
|-----------|--------|-------------|-------------|----------|---------|-------------|-------------|
| DIS_ACDRV | EN_OTG | PFM_OTG_DIS | PFM_FWD_DIS | WKUP_DLY | DIS_LDO | DIS_OTG_OOA | DIS_FWD_OOA |
| R/W-0h    | R/W-0h | R/W-0h      | R/W-0h      | R/W-0h   | R/W-0h  | R/W-0h      | R/W-0h      |

**Table 9-28. REG12\_Charger\_Control\_3 Register Field Descriptions**

| Bit | Field       | Type | Reset | Notes                            | Description   |
|-----|-------------|------|-------|----------------------------------|---|
| 7   | DIS_ACDRV   | R/W  | 0h    |                                  | When this bit is set, the charger will force both EN_ACDRV1=0 and EN_ACDRV2=0<br>Type : RW<br>POR: 0b   |
| 6   | EN_OTG      | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | OTG mode control<br>Type : RW<br>POR: 0b<br>0h = OTG Disable (default)<br>1h = OTG Enable   |
| 5   | PFM_OTG_DIS | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Disable PFM in OTG mode<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable  |
| 4   | PFM_FWD_DIS | R/W  | 0h    | Reset by:<br>REG_RST             | Disable PFM in forward mode<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable  |
| 3   | WKUP_DLY    | R/W  | 0h    | Reset by:<br>REG_RST             | When wake up the device from ship mode, how much time ( $t_{SM\_EXIT}$ ) is required to pull low the QON pin.<br>Type : RW<br>POR: 0b<br>0h = 1s (Default)<br>1h = 15ms |
| 2   | DIS_LDO     | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Disable BATFET LDO mode in pre-charge stage.<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |
| 1   | DIS_OTG_OOA | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Disable OOA in OTG mode<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable  |
| 0   | DIS_FWD_OOA | R/W  | 0h    | Reset by:<br>REG_RST             | Disable OOA in forward mode<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable  |

### 9.5.1.16 REG13\_Charger\_Control\_4 Register (Offset = 13h) [reset = X]

REG13\_Charger\_Control\_4 is shown in [Figure 9-40](#) and described in [Table 9-29](#).

Return to the [Table 9-12](#).

Charger Control 4

**Figure 9-40. REG13\_Charger\_Control\_4 Register**

| 7         | 6         | 5        | 4        | 3                  | 2                | 1                    | 0           |
|-----------|-----------|----------|----------|--------------------|------------------|----------------------|-------------|
| EN_ACDRV2 | EN_ACDRV1 | PWM_FREQ | DIS_STAT | DIS_VSYS_SH<br>ORT | DIS_VOTG_UV<br>P | FORCE_VINDP<br>M_DET | EN_IBUS_OCP |
| R/W-0h    | R/W-0h    | R/W-X    | R/W-0h   | R/W-0h             | R/W-0h           | R/W-0h               | R/W-1h      |

**Table 9-29. REG13\_Charger\_Control\_4 Register Field Descriptions**

| Bit | Field                | Type | Reset | Notes                            | Description  |
|-----|----------------------|------|-------|----------------------------------|--|
| 7   | EN_ACDRV2            | R/W  | 0h    |                                  | External ACFET2-RBFET2 gate driver control<br>At POR, if the charger detects that there is no ACFET2-RBFET2 populated, this bit will be locked at 0<br>Type : RW<br>POR: 0b<br>0h = turn off (default)<br>1h = turn on   |
| 6   | EN_ACDRV1            | R/W  | 0h    |                                  | External ACFET1-RBFET1 gate driver control<br>At POR, if the charger detects that there is no ACFET1-RBFET1 populated, this bit will be locked at 0<br>Type : RW<br>POR: 0b<br>0h = turn off (default)<br>1h = turn on   |
| 5   | PWM_FREQ             | R/W  | X     |                                  | Switching frequency selection, this bit POR default value is based on the PROG pin strapping.<br>Type : RW<br>0h = 1.5 MHz<br>1h = 750 kHz   |
| 4   | DIS_STAT             | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Disable the STAT pin output<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |
| 3   | DIS_VSYS_SHORT       | R/W  | 0h    | Reset by:<br>REG_RST             | Disable forward mode VSYS short hiccup protection.<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable  |
| 2   | DIS_VOTG_UVP         | R/W  | 0h    | Reset by:<br>REG_RST             | Disable OTG mode VOTG UVP hiccup protection.<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable  |
| 1   | FORCE_VINDPM_D<br>ET | R/W  | 0h    | Reset by:<br>REG_RST             | Force VINDPM detection<br>Note: only when VBAT>VSYSMIN, this bit can be set to 1. Once the VINDPM auto detection is done, this bits returns to 0.<br>Type : RW<br>POR: 0b<br>0h = Do NOT force VINDPM detection (default)<br>1h = Force the converter stop switching, and ADC measures the VBUS voltage without input current, then the charger updates the VINDPM register accordingly. |

**Table 9-29. REG13\_Charger\_Control\_4 Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Notes                | Description  |
|-----|-------------|------|-------|----------------------|--|
| 0   | EN_IBUS_OCP | R/W  | 1h    | Reset by:<br>REG_RST | Enable IBUS_OCP in forward mode<br>Type : RW<br>POR: 1b<br>0h = Disable<br>1h = Enable (default) |

### 9.5.1.17 REG14\_Charger\_Control\_5 Register (Offset = 14h) [reset = 16h]

REG14\_Charger\_Control\_5 is shown in [Figure 9-41](#) and described in [Table 9-30](#).

Return to the [Table 9-12](#).

Charger Control 5

**Figure 9-41. REG14\_Charger\_Control\_5 Register**

| 7            | 6        | 5       | 4            | 3 | 2         | 1          | 0        |
|--------------|----------|---------|--------------|---|-----------|------------|----------|
| SFET_PRESENT | RESERVED | EN_IBAT | IBAT_REG_1:0 |   | EN_IINDPM | EN_EXTILIM | EN_BATOC |
| R/W-0h       | R-0h     | R/W-0h  | R/W-2h       |   | R/W-1h    | R/W-1h     | R/W-0h   |

**Table 9-30. REG14\_Charger\_Control\_5 Register Field Descriptions**

| Bit | Field        | Type | Reset | Notes                            | Description  |
|-----|--------------|------|-------|----------------------------------|--|
| 7   | SFET_PRESENT | R/W  | 0h    |                                  | The user has to set this bit based on whether a ship FET is populated or not. The POR default value is 0, which means the charger does not support all the features associated with the ship FET. The register bits list below all are locked at 0.<br>EN_BATOC=0<br>FORCE_SFET_OFF=0<br>SDRV_CTRL=00<br>When this bit is set to 1, the register bits list above become programmable, and the charger can support the features associated with the ship FET<br>Type : RW<br>POR: 0b<br>0h = No ship FET populated<br>1h = Ship FET populated |
| 6   | RESERVED     | R    | 0h    |                                  | Reserved   |
| 5   | EN_IBAT      | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | IBAT discharge current sensing enable for ADC<br>Type : RW<br>POR: 0b<br>0h = Disable IBAT discharge current sensing for ADC (default)<br>1h = Enable the IBAT discharge current sensing for ADC   |
| 4-3 | IBAT_REG_1:0 | R/W  | 2h    | Reset by:<br>WATCHDOG<br>REG_RST | Battery discharging current regulation in OTG mode<br>Type : RW<br>POR: 10b<br>0h = 3A<br>1h = 4A<br>2h = 5A (default)<br>3h = Disable   |
| 2   | EN_IINDPM    | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable the internal IINDPM register input current regulation<br>Type : RW<br>POR: 1b<br>0h = Disable<br>1h = Enable (default)  |
| 1   | EN_EXTILIM   | R/W  | 1h    | Reset by:<br>REG_RST             | Enable the external ILIM_HIZ pin input current regulation<br>Type : RW<br>POR: 1b<br>0h = Disable<br>1h = Enable (default)   |

**Table 9-30. REG14\_Charger\_Control\_5 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Notes                            | Description   |
|-----|----------|------|-------|----------------------------------|---|
| 0   | EN_BATOC | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable the battery discharging current OCP<br>Type : RW<br>POR: 0b<br>0h = Disable (default)<br>1h = Enable |

### 9.5.1.18 REG15\_Reserved Register (Offset = 15h) [reset = 00h]

REG15\_Reserved is shown in [Figure 9-42](#) and described in [Table 9-31](#).

Return to the [Table 9-12](#).

Reserved Register

**Figure 9-42. REG15\_Reserved Register**

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |   |   |   |   |   |   |   |
| R-0h     |   |   |   |   |   |   |   |

**Table 9-31. REG15\_Reserved Register Field Descriptions**

| Bit | Field    | Type | Reset | Notes | Description |
|-----|----------|------|-------|-------|-------------|
| 7-0 | RESERVED | R    | 0h    |       | Reserved    |

### 9.5.1.19 REG16\_Temperature\_Control Register (Offset = 16h) [reset = C0h]

REG16\_Temperature\_Control is shown in [Figure 9-43](#) and described in [Table 9-32](#).

Return to the [Table 9-12](#).

Temperature Control

**Figure 9-43. REG16\_Temperature\_Control Register**

| 7        | 6         | 5 | 4          | 3          | 2          | 1        | 0 |
|----------|-----------|---|------------|------------|------------|----------|---|
| TREG_1:0 | TSHUT_1:0 |   | VBUS_PD_EN | VAC1_PD_EN | VAC2_PD_EN | RESERVED |   |
| R/W-3h   | R/W-0h    |   | R/W-0h     | R/W-0h     | R/W-0h     | R-0h     |   |

**Table 9-32. REG16\_Temperature\_Control Register Field Descriptions**

| Bit | Field      | Type | Reset | Notes                            | Description   |
|-----|------------|------|-------|----------------------------------|---|
| 7-6 | TREG_1:0   | R/W  | 3h    | Reset by:<br>WATCHDOG<br>REG_RST | Thermal regulation thresholds.<br>Type : RW<br>POR: 11b<br>0h = 60°C<br>1h = 80°C<br>2h = 100°C<br>3h = 120°C (default) |
| 5-4 | TSHUT_1:0  | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Thermal shutdown thresholds.<br>Type : RW<br>POR: 00b<br>0h = 150°C (default)<br>1h = 130°C<br>2h = 120°C<br>3h = 85°C  |
| 3   | VBUS_PD_EN | R/W  | 0h    | Reset by:<br>REG_RST             | Enable VBUS pull down resistor (6k Ohm)<br>Type : RW<br>POR: 0b<br>0h = Disable (default)<br>1h = Enable                |
| 2   | VAC1_PD_EN | R/W  | 0h    | Reset by:<br>REG_RST             | Enable VAC1 pull down resistor<br>Type : RW<br>POR: 0b<br>0h = Disable (default)<br>1h = Enable                         |
| 1   | VAC2_PD_EN | R/W  | 0h    | Reset by:<br>REG_RST             | Enable VAC2 pull down resistor<br>Type : RW<br>POR: 0b<br>0h = Disable (default)<br>1h = Enable                         |
| 0   | RESERVED   | R    | 0h    |                                  | Reserved  |



### 9.5.1.20 REG17\_NTC\_Control\_0 Register (Offset = 17h) [reset = 7Ah]

REG17\_NTC\_Control\_0 is shown in [Figure 9-44](#) and described in [Table 9-33](#).

Return to the [Table 9-12](#).

NTC Control 0

**Figure 9-44. REG17\_NTC\_Control\_0 Register**

| 7              | 6 | 5 | 4               | 3 | 2               | 1 | 0        |
|----------------|---|---|-----------------|---|-----------------|---|----------|
| JEITA_VSET_2:0 |   |   | JEITA_ISETH_1:0 |   | JEITA_ISETC_1:0 |   | RESERVED |
| R/W-3h         |   |   | R/W-3h          |   | R/W-1h          |   | R-0h     |

**Table 9-33. REG17\_NTC\_Control\_0 Register Field Descriptions**

| Bit | Field           | Type | Reset | Notes                            | Description   |
|-----|-----------------|------|-------|----------------------------------|---|
| 7-5 | JEITA_VSET_2:0  | R/W  | 3h    | Reset by:<br>WATCHDOG<br>REG_RST | JEITA high temperature range (TWARN – THOT)<br>charge voltage setting<br>Type : RW<br>POR: 011b<br>0h = Charge Suspend<br>1h = Set VREG to VREG-800mV<br>2h = Set VREG to VREG-600mV<br>3h = Set VREG to VREG-400mV (default)<br>4h = Set VREG to VREG-300mV<br>5h = Set VREG to VREG-200mV<br>6h = Set VREG to VREG-100mV<br>7h = VREG unchanged |
| 4-3 | JEITA_ISETH_1:0 | R/W  | 3h    | Reset by:<br>WATCHDOG<br>REG_RST | JEITA high temperature range (TWARN – THOT)<br>charge current setting<br>Type : RW<br>POR: 11b<br>0h = Charge Suspend<br>1h = Set ICHG to 20%* ICHG<br>2h = Set ICHG to 40%* ICHG<br>3h = ICHG unchanged (default)  |
| 2-1 | JEITA_ISETC_1:0 | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | JEITA low temperature range (TCOLD – TCOOL)<br>charge current setting<br>Type : RW<br>POR: 01b<br>0h = Charge Suspend<br>1h = Set ICHG to 20%* ICHG (default)<br>2h = Set ICHG to 40%* ICHG<br>3h = ICHG unchanged  |
| 0   | RESERVED        | R    | 0h    |                                  | Reserved  |

### 9.5.1.21 REG18\_NTC\_Control\_1 Register (Offset = 18h) [reset = 54h]

REG18\_NTC\_Control\_1 is shown in [Figure 9-45](#) and described in [Table 9-34](#).

Return to the [Table 9-12](#).

NTC Control 1

**Figure 9-45. REG18\_NTC\_Control\_1 Register**

| 7           | 6 | 5           | 4 | 3        | 2 | 1      | 0         |
|-------------|---|-------------|---|----------|---|--------|-----------|
| TS_COOL_1:0 |   | TS_WARM_1:0 |   | BHOT_1:0 |   | BCOLD  | TS_IGNORE |
| R/W-1h      |   | R/W-1h      |   | R/W-1h   |   | R/W-0h | R/W-0h    |

**Table 9-34. REG18\_NTC\_Control\_1 Register Field Descriptions**

| Bit | Field       | Type | Reset | Notes                            | Description  |
|-----|-------------|------|-------|----------------------------------|--|
| 7-6 | TS_COOL_1:0 | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | JEITA VT2 comparator voltage rising thresholds as a percentage of REGN. The corresponding temperature in the brackets is achieved when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ.<br>Type : RW<br>POR: 01b<br>0h = 71.1% (5°C)<br>1h = 68.4% (default) (10°C)<br>2h = 65.5% (15°C)<br>3h = 62.4% (20°C)   |
| 5-4 | TS_WARM_1:0 | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | JEITA VT3 comparator voltage falling thresholds as a percentage of REGN. The corresponding temperature in the brackets is achieved when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ.<br>Type : RW<br>POR: 01b<br>0h = 48.4% (40°C)<br>1h = 44.8% (default) (45°C)<br>2h = 41.2% (50°C)<br>3h = 37.7% (55°C) |
| 3-2 | BHOT_1:0    | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | OTG mode TS HOT temperature threshold<br>Type : RW<br>POR: 01b<br>0h = 55°C<br>1h = 60°C (default)<br>2h = 65°C<br>3h = Disable  |
| 1   | BCOLD       | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | OTG mode TS COLD temperature threshold<br>Type : RW<br>POR: 0b<br>0h = -10°C (default)<br>1h = -20°C   |
| 0   | TS_IGNORE   | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Ignore the TS feedback, the charger considers the TS is always good to allow the charging and OTG modes, all the four TS status bits always stay at 0000 to report the normal condition.<br>Type : RW<br>POR: 0b<br>0h = NOT ignore (Default)<br>1h = Ignore   |

### 9.5.1.22 REG19\_ICO\_Current\_Limit Register (Offset = 19h) [reset = 0h]

REG19\_ICO\_Current\_Limit is shown in [Figure 9-46](#) and described in [Table 9-35](#).

Return to the [Table 9-12](#).

ICO Current Limit

**Figure 9-46. REG19\_ICO\_Current\_Limit Register**

|              |    |    |    |    |    |   |              |
|--------------|----|----|----|----|----|---|--------------|
| 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8            |
| RESERVED     |    |    |    |    |    |   | ICO_ILIM_8:0 |
| R-0h         |    |    |    |    |    |   | R-0h         |
| 7            | 6  | 5  | 4  | 3  | 2  | 1 | 0            |
| ICO_ILIM_8:0 |    |    |    |    |    |   |              |
| R-0h         |    |    |    |    |    |   |              |

**Table 9-35. REG19\_ICO\_Current\_Limit Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description   |
|------|--------------|------|-------|---|
| 15-9 | RESERVED     | R    | 0h    | RESERVED  |
| 8-0  | ICO_ILIM_8:0 | R    | 0h    | Input Current Limit obtained from ICO or ILIM_HIZ pin setting<br>Type : R<br>POR: 0mA (0h)<br>Range : 100mA-3300mA<br>Fixed Offset : 0mA<br>Bit Step Size : 10mA<br>Clamped Low |

### 9.5.1.23 REG1B\_Charger\_Status\_0 Register (Offset = 1Bh) [reset = 0h]

REG1B\_Charger\_Status\_0 is shown in [Figure 9-47](#) and described in [Table 9-36](#).

Return to the [Table 9-12](#).

Charger Status 0

**Figure 9-47. REG1B\_Charger\_Status\_0 Register**

| 7           | 6           | 5       | 4            | 3       | 2                | 1                | 0                 |
|-------------|-------------|---------|--------------|---------|------------------|------------------|-------------------|
| IINDPM_STAT | VINDPM_STAT | WD_STAT | POORSRC_STAT | PG_STAT | AC2_PRESENT_STAT | AC1_PRESENT_STAT | VBUS_PRESENT_STAT |
| R-0h        | R-0h        | R-0h    | R-0h         | R-0h    | R-0h             | R-0h             | R-0h              |

**Table 9-36. REG1B\_Charger\_Status\_0 Register Field Descriptions**

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 7   | IINDPM_STAT      | R    | 0h    | IINDPM status (forward mode) or IOTG status (OTG mode)<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = In IINDPM regulation or IOTG regulation |
| 6   | VINDPM_STAT      | R    | 0h    | VINDPM status (forward mode) or VOTG status (OTG mode)<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = In VINDPM regulation or VOTG regulation |
| 5   | WD_STAT          | R    | 0h    | I2C watch dog timer status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = WD timer expired  |
| 4   | POORSRC_STAT     | R    | 0h    | Poor source detection status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Weak adaptor detected   |
| 3   | PG_STAT          | R    | 0h    | Power Good Status<br>Type : R<br>POR: 0b<br><br>0h = NOT in power good status<br>1h = Power good   |
| 2   | AC2_PRESENT_STAT | R    | 0h    | VAC2 insert status<br>Type : R<br>POR: 0b<br><br>0h = VAC2 NOT present<br>1h = VAC2 present (above present threshold)                            |

**Table 9-36. REG1B\_Charger\_Status\_0 Register Field Descriptions (continued)**

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 1   | AC1_PRESENT_STAT  | R    | 0h    | VAC1 insert status<br>Type : R<br>POR: 0b<br><br>0h = VAC1 NOT present<br>1h = VAC1 present (above present threshold)  |
| 0   | VBUS_PRESENT_STAT | R    | 0h    | VBUS present status<br>Type : R<br>POR: 0b<br><br>0h = VBUS NOT present<br>1h = VBUS present (above present threshold) |

### 9.5.1.24 REG1C\_Charger\_Status\_1 Register (Offset = 1Ch) [reset = 0h]

REG1C\_Charger\_Status\_1 is shown in [Figure 9-48](#) and described in [Table 9-37](#).

Return to the [Table 9-12](#).

Charger Status 1

**Figure 9-48. REG1C\_Charger\_Status\_1 Register**

| 7            | 6 | 5 | 4             | 3 | 2 | 1               | 0 |
|--------------|---|---|---------------|---|---|-----------------|---|
| CHG_STAT_2:0 |   |   | VBUS_STAT_3:0 |   |   | BC1.2_DONE_STAT |   |
| R-0h         |   |   | R-0h          |   |   | R-0h            |   |

**Table 9-37. REG1C\_Charger\_Status\_1 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description   |
|-----|---------------|------|-------|---|
| 7-5 | CHG_STAT_2:0  | R    | 0h    | Charge Status bits<br>Type : R<br>POR: 000b<br><br>0h = Not Charging<br>1h = Trickle Charge<br>2h = Pre-charge<br>3h = Fast charge (CC mode)<br>4h = Taper Charge (CV mode)<br>5h = Reserved<br>6h = Top-off Timer Active Charging<br>7h = Charge Termination Done  |
| 4-1 | VBUS_STAT_3:0 | R    | 0h    | VBUS status bits<br>0h: No Input or BHOT or BCOLD in OTG mode<br>1h: USB SDP (500mA)<br>2h: USB CDP (1.5A)<br>3h: USB DCP (3.25A)<br>4h: Adjustable High Voltage DCP (HVDCP) (1.5A)<br>5h: Unknown adaptor (3A)<br>6h: Non-Standard Adapter (1A/2A/2.1A/2.4A)<br>7h: In OTG mode<br>8h: Not qualified adaptor<br>9h: Reserved<br>Ah: Reserved<br>Bh: Device directly powered from VBUS<br>Ch: Reserved<br>Dh: Reserved<br>Eh: Reserved<br>Fh: Reserved<br>Type : R<br>POR: 0h |

**Table 9-37. REG1C\_Charger\_Status\_1 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 0   | BC1.2_DONE_STAT | R    | 0h    | BC1.2 status bit<br>Type : R<br>POR: 0b<br>0h = BC1.2 or non-standard detection NOT complete<br>1h = BC1.2 or non-standard detection complete |

### 9.5.1.25 REG1D\_Charger\_Status\_2 Register (Offset = 1Dh) [reset = 0h]

REG1D\_Charger\_Status\_2 is shown in [Figure 9-49](#) and described in [Table 9-38](#).

Return to the [Table 9-12](#).

Charger Status 2

**Figure 9-49. REG1D\_Charger\_Status\_2 Register**

| 7            | 6 | 5        | 4 | 3 | 2         | 1         | 0                     |
|--------------|---|----------|---|---|-----------|-----------|-----------------------|
| ICO_STAT_1:0 |   | RESERVED |   |   | TREG_STAT | DPDM_STAT | VBAT_PRESEN<br>T_STAT |
| R-0h         |   | R-0h     |   |   | R-0h      | R-0h      | R-0h                  |

**Table 9-38. REG1D\_Charger\_Status\_2 Register Field Descriptions**

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 7-6 | ICO_STAT_1:0      | R    | 0h    | Input Current Optimizer (ICO) status<br>Type : R<br>POR: 00b<br><br>0h = ICO disabled<br>1h = ICO optimization in progress<br>2h = Maximum input current detected<br>3h = Reserved |
| 5-3 | RESERVED          | R    | 0h    | RESERVED   |
| 2   | TREG_STAT         | R    | 0h    | IC thermal regulation status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in thermal regulation  |
| 1   | DPDM_STAT         | R    | 0h    | D+/D- detection status bits<br>Type : R<br>POR: 0b<br><br>0h = The D+/D- detection is NOT started yet, or the detection is done<br>1h = The D+/D- detection is ongoing             |
| 0   | VBAT_PRESENT_STAT | R    | 0h    | Battery present status ( $V_{BAT} > V_{BAT\_UVLOZ}$ )<br>Type : R<br>POR: 0b<br><br>0h = $V_{BAT}$ NOT present<br>1h = $V_{BAT}$ present   |



### 9.5.1.26 REG1E\_Charger\_Status\_3 Register (Offset = 1Eh) [reset = 0h]

REG1E\_Charger\_Status\_3 is shown in [Figure 9-50](#) and described in [Table 9-39](#).

Return to the [Table 9-12](#).

Charger Status 3

**Figure 9-50. REG1E\_Charger\_Status\_3 Register**

| 7          | 6          | 5             | 4         | 3            | 2               | 1               | 0        |
|------------|------------|---------------|-----------|--------------|-----------------|-----------------|----------|
| ACRB2_STAT | ACRB1_STAT | ADC_DONE_STAT | VSYS_STAT | CHG_TMR_STAT | TRICHG_TMR_STAT | PRECHG_TMR_STAT | RESERVED |
| R-0h       | R-0h       | R-0h          | R-0h      | R-0h         | R-0h            | R-0h            | R-0h     |

**Table 9-39. REG1E\_Charger\_Status\_3 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7   | ACRB2_STAT      | R    | 0h    | The ACFET2-RBFET2 status<br>Type : R<br>POR: 0b<br><br>0h = ACFET2-RBFET2 is NOT placed<br>1h = ACFET2-RBFET2 is placed  |
| 6   | ACRB1_STAT      | R    | 0h    | The ACFET1-RBFET1 status<br>Type : R<br>POR: 0b<br><br>0h = ACFET1-RBFET1 is NOT placed<br>1h = ACFET1-RBFET1 is placed  |
| 5   | ADC_DONE_STAT   | R    | 0h    | ADC Conversion Status (in one-shot mode only)<br>Type : R<br>POR: 0b<br><br>0h = Conversion NOT complete<br>1h = Conversion complete   |
| 4   | VSYS_STAT       | R    | 0h    | VSYS Regulation Status (forward mode)<br>Type : R<br>POR: 0b<br><br>0h = Not in VSYSMIN regulation ( $V_{BAT} > V_{SYSMIN}$ )<br>1h = In VSYSMIN regulation ( $V_{BAT} < V_{SYSMIN}$ ) |
| 3   | CHG_TMR_STAT    | R    | 0h    | Fast charge timer status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Safety timer expired  |
| 2   | TRICHG_TMR_STAT | R    | 0h    | Trickle charge timer status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Safety timer expired   |

**Table 9-39. REG1E\_Charger\_Status\_3 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 1   | PRECHG_TMR_STAT | R    | 0h    | Pre-charge timer status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Safety timer expired |
| 0   | RESERVED        | R    | 0h    | RESERVED   |

### 9.5.1.27 REG1F\_Charger\_Status\_4 Register (Offset = 1Fh) [reset = 0h]

REG1F\_Charger\_Status\_4 is shown in [Figure 9-51](#) and described in [Table 9-40](#).

Return to the [Table 9-12](#).

Charger Status 4

**Figure 9-51. REG1F\_Charger\_Status\_4 Register**

| 7        | 6 | 5 | 4                    | 3                | 2                | 1                | 0           |
|----------|---|---|----------------------|------------------|------------------|------------------|-------------|
| RESERVED |   |   | VBATOTG_LO<br>W_STAT | TS_COLD_STA<br>T | TS_COOL_STA<br>T | TS_WARM_STA<br>T | TS_HOT_STAT |
| R-0h     |   |   | R-0h                 | R-0h             | R-0h             | R-0h             | R-0h        |

**Table 9-40. REG1F\_Charger\_Status\_4 Register Field Descriptions**

| Bit | Field            | Type | Reset | Description   |
|-----|------------------|------|-------|---|
| 7-5 | RESERVED         | R    | 0h    | RESERVED  |
| 4   | VBATOTG_LOW_STAT | R    | 0h    | The battery voltage is too low to enable OTG mode.<br>Type : R<br>POR: 0b<br><br>0h = The battery voltage is high enough to enable the OTG operation<br>1h = The battery voltage is too low to enable the OTG operation |
| 3   | TS_COLD_STAT     | R    | 0h    | The TS temperature is in the cold range, lower than T1.<br>Type : R<br>POR: 0b<br><br>0h = TS status is NOT in cold range<br>1h = TS status is in cold range  |
| 2   | TS_COOL_STAT     | R    | 0h    | The TS temperature is in the cool range, between T1 and T2.<br>Type : R<br>POR: 0b<br><br>0h = TS status is NOT in cool range<br>1h = TS status is in cool range  |
| 1   | TS_WARM_STAT     | R    | 0h    | The TS temperature is in the warm range, between T3 and T5.<br>Type : R<br>POR: 0b<br><br>0h = TS status is NOT in warm range<br>1h = TS status is in warm range  |
| 0   | TS_HOT_STAT      | R    | 0h    | The TS temperature is in the hot range, higher than T5.<br>Type : R<br>POR: 0b<br><br>0h = TS status is NOT in hot range<br>1h = TS status is in hot range  |

### 9.5.1.28 REG20\_FAULT\_Status\_0 Register (Offset = 20h) [reset = 0h]

REG20\_FAULT\_Status\_0 is shown in [Figure 9-52](#) and described in [Table 9-41](#).

Return to the [Table 9-12](#).

FAULT Status 0

**Figure 9-52. REG20\_FAULT\_Status\_0 Register**

| 7             | 6             | 5             | 4             | 3             | 2             | 1             | 0             |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| IBAT_REG_STAT | VBUS_OVP_STAT | VBAT_OVP_STAT | IBUS_OCP_STAT | IBAT_OCP_STAT | CONV_OCP_STAT | VAC2_OVP_STAT | VAC1_OVP_STAT |
| R-0h          | R-0h          | R-0h          | R-0h          | R-0h          | R-0h          | R-0h          | R-0h          |

**Table 9-41. REG20\_FAULT\_Status\_0 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description   |
|-----|---------------|------|-------|---|
| 7   | IBAT_REG_STAT | R    | 0h    | IBAT regulation status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in battery discharging current regulation |
| 6   | VBUS_OVP_STAT | R    | 0h    | VBUS over-voltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in over voltage protection              |
| 5   | VBAT_OVP_STAT | R    | 0h    | VBAT over-voltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in over voltage protection              |
| 4   | IBUS_OCP_STAT | R    | 0h    | IBUS over-current status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in over current protection              |
| 3   | IBAT_OCP_STAT | R    | 0h    | IBAT over-current status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in over current protection              |
| 2   | CONV_OCP_STAT | R    | 0h    | Converter over current status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Converter in over current protection      |

**Table 9-41. REG20\_FAULT\_Status\_0 Register Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 1   | VAC2_OVP_STAT | R    | 0h    | VAC2 over-voltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in over voltage protection |
| 0   | VAC1_OVP_STAT | R    | 0h    | VAC1 over-voltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in over voltage protection |

### 9.5.1.29 REG21\_FAULT\_Status\_1 Register (Offset = 21h) [reset = 0h]

REG21\_FAULT\_Status\_1 is shown in [Figure 9-53](#) and described in [Table 9-42](#).

Return to the [Table 9-12](#).

FAULT Status 1

**Figure 9-53. REG21\_FAULT\_Status\_1 Register**

| 7               | 6             | 5            | 4            | 3        | 2          | 1        | 0 |
|-----------------|---------------|--------------|--------------|----------|------------|----------|---|
| VSYS_SHORT_STAT | VSYS_OVP_STAT | OTG_OVP_STAT | OTG_UVP_STAT | RESERVED | TSHUT_STAT | RESERVED |   |
| R-0h            | R-0h          | R-0h         | R-0h         | R-0h     | R-0h       | R-0h     |   |

**Table 9-42. REG21\_FAULT\_Status\_1 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7   | VSYS_SHORT_STAT | R    | 0h    | VSYS short circuit status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in SYS short circuit protection     |
| 6   | VSYS_OVP_STAT   | R    | 0h    | VSYS over-voltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in SYS over-voltage protection       |
| 5   | OTG_OVP_STAT    | R    | 0h    | OTG over voltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in OTG over-voltage                   |
| 4   | OTG_UVP_STAT    | R    | 0h    | OTG under voltage status.<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in OTG under voltage                |
| 3   | RESERVED        | R    | 0h    | RESERVED   |
| 2   | TSHUT_STAT      | R    | 0h    | IC temperature shutdown status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in thermal shutdown protection |
| 1-0 | RESERVED        | R    | 0h    | RESERVED   |

### 9.5.1.30 REG22\_Charger\_Flag\_0 Register (Offset = 22h) [reset = 0h]

REG22\_Charger\_Flag\_0 is shown in [Figure 9-54](#) and described in [Table 9-43](#).

Return to the [Table 9-12](#).

Charger Flag 0

**Figure 9-54. REG22\_Charger\_Flag\_0 Register**

| 7           | 6           | 5       | 4                | 3       | 2                    | 1                    | 0                     |
|-------------|-------------|---------|------------------|---------|----------------------|----------------------|-----------------------|
| IINDPM_FLAG | VINDPM_FLAG | WD_FLAG | POORSRC_FL<br>AG | PG_FLAG | AC2_PRESENT<br>_FLAG | AC1_PRESENT<br>_FLAG | VBUS_PRESE<br>NT_FLAG |
| R-0h        | R-0h        | R-0h    | R-0h             | R-0h    | R-0h                 | R-0h                 | R-0h                  |

**Table 9-43. REG22\_Charger\_Flag\_0 Register Field Descriptions**

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 7   | IINDPM_FLAG      | R    | 0h    | IINDPM / IOTG flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = IINDPM / IOTG signal rising edge detected                                       |
| 6   | VINDPM_FLAG      | R    | 0h    | VINDPM / VOTG Flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VINDPM / VOTG regulation signal rising edge detected                            |
| 5   | WD_FLAG          | R    | 0h    | I2C watchdog timer flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = WD timer signal rising edge detected                                       |
| 4   | POORSRC_FLAG     | R    | 0h    | Poor source detection flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Poor source status rising edge detected                                 |
| 3   | PG_FLAG          | R    | 0h    | Power good flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Any change in PG_STAT even (adapter good qualification or adapter good going away) |
| 2   | AC2_PRESENT_FLAG | R    | 0h    | VAC2 present flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VAC2 present status changed  |

**Table 9-43. REG22\_Charger\_Flag\_0 Register Field Descriptions (continued)**

| Bit | Field             | Type | Reset | Description   |
|-----|-------------------|------|-------|---|
| 1   | AC1_PRESENT_FLAG  | R    | 0h    | VAC1 present flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VAC1 present status changed |
| 0   | VBUS_PRESENT_FLAG | R    | 0h    | VBUS present flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VBUS present status changed |



### 9.5.1.31 REG23\_Charger\_Flag\_1 Register (Offset = 23h) [reset = 0h]

REG23\_Charger\_Flag\_1 is shown in [Figure 9-55](#) and described in [Table 9-44](#).

Return to the [Table 9-12](#).

Charger Flag 1

**Figure 9-55. REG23\_Charger\_Flag\_1 Register**

| 7        | 6        | 5        | 4         | 3        | 2         | 1                     | 0                   |
|----------|----------|----------|-----------|----------|-----------|-----------------------|---------------------|
| CHG_FLAG | ICO_FLAG | RESERVED | VBUS_FLAG | RESERVED | TREG_FLAG | VBAT_PRESEN<br>T_FLAG | BC1.2_DONE_<br>FLAG |
| R-0h     | R-0h     | R-0h     | R-0h      | R-0h     | R-0h      | R-0h                  | R-0h                |

**Table 9-44. REG23\_Charger\_Flag\_1 Register Field Descriptions**

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 7   | CHG_FLAG          | R    | 0h    | Charge status flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Charge status changed                         |
| 6   | ICO_FLAG          | R    | 0h    | ICO status flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = ICO status changed                               |
| 5   | RESERVED          | R    | 0h    | RESERVED   |
| 4   | VBUS_FLAG         | R    | 0h    | VBUS status flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VBUS status changed                             |
| 3   | RESERVED          | R    | 0h    | RESERVED   |
| 2   | TREG_FLAG         | R    | 0h    | IC thermal regulation flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TREG signal rising threshold detected |
| 1   | VBAT_PRESENT_FLAG | R    | 0h    | VBAT present flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VBAT present status changed                    |

**Table 9-44. REG23\_Charger\_Flag\_1 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 0   | BC1.2_DONE_FLAG | R    | 0h    | BC1.2 status Flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = BC1.2 detection status changed |

### 9.5.1.32 REG24\_Charger\_Flag\_2 Register (Offset = 24h) [reset = 0h]

REG24\_Charger\_Flag\_2 is shown in [Figure 9-56](#) and described in [Table 9-45](#).

Return to the [Table 9-12](#).

Charger Flag 2

**Figure 9-56. REG24\_Charger\_Flag\_2 Register**

| 7        | 6              | 5             | 4         | 3            | 2               | 1               | 0               |
|----------|----------------|---------------|-----------|--------------|-----------------|-----------------|-----------------|
| RESERVED | DPDM_DONE_FLAG | ADC_DONE_FLAG | VSYS_FLAG | CHG_TMR_FLAG | TRICHG_TMR_FLAG | PRECHG_TMR_FLAG | TOPOFF_TMR_FLAG |
| R-0h     | R-0h           | R-0h          | R-0h      | R-0h         | R-0h            | R-0h            | R-0h            |

**Table 9-45. REG24\_Charger\_Flag\_2 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 7   | RESERVED        | R    | 0h    | RESERVED  |
| 6   | DPDM_DONE_FLAG  | R    | 0h    | D+/D- detection is done flag.<br>Type : R<br>POR: 0b<br><br>0h = D+/D- detection is NOT started or still ongoing<br>1h = D+/D- detection is completed |
| 5   | ADC_DONE_FLAG   | R    | 0h    | ADC conversion flag (only in one-shot mode)<br>Type : R<br>POR: 0b<br><br>0h = Conversion NOT completed<br>1h = Conversion completed                  |
| 4   | VSYS_FLAG       | R    | 0h    | VSYSMIN regulation flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Entered or existed VSYSMIN regulation                                       |
| 3   | CHG_TMR_FLAG    | R    | 0h    | Fast charge timer flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Fast charge timer expired rising edge detected                               |
| 2   | TRICHG_TMR_FLAG | R    | 0h    | Trickle charge timer flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Trickle charger timer expired rising edge detected                        |
| 1   | PRECHG_TMR_FLAG | R    | 0h    | Pre-charge timer flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Pre-charge timer expired rising edge detected                                 |

**Table 9-45. REG24\_Charger\_Flag\_2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 0   | TOPOFF_TMR_FLAG | R    | 0h    | Top off timer flag<br>Type : R<br>POR: 0b<br>0h = Normal<br>1h = Top off timer expired rising edge detected |

### 9.5.1.33 REG25\_Charger\_Flag\_3 Register (Offset = 25h) [reset = 0h]

REG25\_Charger\_Flag\_3 is shown in [Figure 9-57](#) and described in [Table 9-46](#).

Return to the [Table 9-12](#).

Charger Flag 3

**Figure 9-57. REG25\_Charger\_Flag\_3 Register**

| 7        | 6 | 5 | 4                    | 3                 | 2                 | 1                 | 0           |
|----------|---|---|----------------------|-------------------|-------------------|-------------------|-------------|
| RESERVED |   |   | VBATOTG_LO<br>W_FLAG | TS_COLD_FL<br>A_G | TS_COOL_FL<br>A_G | TS_WARM_FL<br>A_G | TS_HOT_FLAG |
| R-0h     |   |   | R-0h                 | R-0h              | R-0h              | R-0h              | R-0h        |

**Table 9-46. REG25\_Charger\_Flag\_3 Register Field Descriptions**

| Bit | Field            | Type | Reset | Description   |
|-----|------------------|------|-------|---|
| 7-5 | RESERVED         | R    | 0h    | RESERVED  |
| 4   | VBATOTG_LOW_FLAG | R    | 0h    | VBAT too low to enable OTG flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VBAT falls below the threshold to enable the OTG mode |
| 3   | TS_COLD_FLAG     | R    | 0h    | TS cold temperature flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TS across cold temperature (T1) is detected                  |
| 2   | TS_COOL_FLAG     | R    | 0h    | TS cool temperature flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TS across cool temperature (T2) is detected                  |
| 1   | TS_WARM_FLAG     | R    | 0h    | TS warm temperature flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TS across warm temperature (T3) is detected                  |
| 0   | TS_HOT_FLAG      | R    | 0h    | TS hot temperature flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TS across hot temperature (T5) is detected                    |

### 9.5.1.34 REG26\_FAULT\_Flag\_0 Register (Offset = 26h) [reset = 0h]

REG26\_FAULT\_Flag\_0 is shown in [Figure 9-58](#) and described in [Table 9-47](#).

Return to the [Table 9-12](#).

FAULT Flag 0

**Figure 9-58. REG26\_FAULT\_Flag\_0 Register**

| 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| IBAT_REG_FL<br>AG | VBUS_OVP_FL<br>AG | VBAT_OVP_FL<br>AG | IBUS_OCP_FL<br>AG | IBAT_OCP_FL<br>AG | CONV_OCP_F<br>LAG | VAC2_OVP_FL<br>AG | VAC1_OVP_FL<br>AG |
| R-0h              | R-0h              | R-0h              | R-0h              | R-0h              | R-0h              | R-0h              | R-0h              |

**Table 9-47. REG26\_FAULT\_Flag\_0 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7   | IBAT_REG_FLAG | R    | 0h    | IBAT regulation flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter or exit IBAT regulation |
| 6   | VBUS_OVP_FLAG | R    | 0h    | VBUS over-voltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter VBUS OVP              |
| 5   | VBAT_OVP_FLAG | R    | 0h    | VBAT over-voltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter VBAT OVP              |
| 4   | IBUS_OCP_FLAG | R    | 0h    | IBUS over-current flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter IBUS OCP              |
| 3   | IBAT_OCP_FLAG | R    | 0h    | IBAT over-current flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter discharged OCP        |
| 2   | CONV_OCP_FLAG | R    | 0h    | Converter over-current flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter converter OCP    |

**Table 9-47. REG26\_FAULT\_Flag\_0 Register Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description   |
|-----|---------------|------|-------|---|
| 1   | VAC2_OVP_FLAG | R    | 0h    | VAC2 over-voltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter VAC2 OVP |
| 0   | VAC1_OVP_FLAG | R    | 0h    | VAC1 over-voltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter VAC1 OVP |

### 9.5.1.35 REG27\_FAULT\_Flag\_1 Register (Offset = 27h) [reset = 0h]

REG27\_FAULT\_Flag\_1 is shown in [Figure 9-59](#) and described in [Table 9-48](#).

Return to the [Table 9-12](#).

FAULT Flag 1

**Figure 9-59. REG27\_FAULT\_Flag\_1 Register**

| 7               | 6             | 5            | 4            | 3        | 2          | 1        | 0 |
|-----------------|---------------|--------------|--------------|----------|------------|----------|---|
| VSYS_SHORT_FLAG | VSYS_OVP_FLAG | OTG_OVP_FLAG | OTG_UVP_FLAG | RESERVED | TSHUT_FLAG | RESERVED |   |
| R-0h            | R-0h          | R-0h         | R-0h         | R-0h     | R-0h       | R-0h     |   |

**Table 9-48. REG27\_FAULT\_Flag\_1 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 7   | VSYS_SHORT_FLAG | R    | 0h    | VSYS short circuit flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Stop switching due to system short            |
| 6   | VSYS_OVP_FLAG   | R    | 0h    | VSYS over-voltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Stop switching due to system over-voltage      |
| 5   | OTG_OVP_FLAG    | R    | 0h    | OTG over-voltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Stop OTG due to VBUS over voltage               |
| 4   | OTG_UVP_FLAG    | R    | 0h    | OTG under-voltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Stop OTG due to VBUS under-voltage             |
| 3   | RESERVED        | R    | 0h    | RESERVED  |
| 2   | TSHUT_FLAG      | R    | 0h    | IC thermal shutdown flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TS shutdown signal rising threshold detected |
| 1-0 | RESERVED        | R    | 0h    | RESERVED  |



### 9.5.1.36 REG28\_Charger\_Mask\_0 Register (Offset = 28h) [reset = 0h]

REG28\_Charger\_Mask\_0 is shown in [Figure 9-60](#) and described in [Table 9-49](#).

Return to the [Table 9-12](#).

Charger Mask 0

**Figure 9-60. REG28\_Charger\_Mask\_0 Register**

| 7           | 6           | 5       | 4            | 3       | 2                | 1                | 0                 |
|-------------|-------------|---------|--------------|---------|------------------|------------------|-------------------|
| IINDPM_MASK | VINDPM_MASK | WD_MASK | POORSRC_MASK | PG_MASK | AC2_PRESENT_MASK | AC1_PRESENT_MASK | VBUS_PRESENT_MASK |
| R/W-0h      | R/W-0h      | R/W-0h  | R/W-0h       | R/W-0h  | R/W-0h           | R/W-0h           | R/W-0h            |

**Table 9-49. REG28\_Charger\_Mask\_0 Register Field Descriptions**

| Bit | Field            | Type | Reset | Notes                | Description   |
|-----|------------------|------|-------|----------------------|---|
| 7   | IINDPM_MASK      | R/W  | 0h    | Reset by:<br>REG_RST | IINDPM / IOTG mask flag<br>Type : RW<br>POR: 0b<br>0h = Enter IINDPM / IOTG does produce INT pulse<br>1h = Enter IINDPM / IOTG does NOT produce INT pulse                       |
| 6   | VINDPM_MASK      | R/W  | 0h    | Reset by:<br>REG_RST | VINDPM / VOTG mask flag<br>Type : RW<br>POR: 0b<br>0h = Enter VINDPM / VOTG does produce INT pulse<br>1h = Enter VINDPM / VOTG does NOT produce INT pulse                       |
| 5   | WD_MASK          | R/W  | 0h    | Reset by:<br>REG_RST | I2C watch dog timer mask flag<br>Type : RW<br>POR: 0b<br>0h = I2C watch dog timer expired does produce INT pulse<br>1h = I2C watch dog timer expired does NOT produce INT pulse |
| 4   | POORSRC_MASK     | R/W  | 0h    | Reset by:<br>REG_RST | Poor source detection mask flag<br>Type : RW<br>POR: 0b<br>0h = Poor source detected does produce INT<br>1h = Poor source detected does NOT produce INT                         |
| 3   | PG_MASK          | R/W  | 0h    | Reset by:<br>REG_RST | Power Good mask flag<br>Type : RW<br>POR: 0b<br>0h = PG toggle does produce INT<br>1h = PG toggle does NOT produce INT  |
| 2   | AC2_PRESENT_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VAC2 present mask flag<br>Type : RW<br>POR: 0b<br>0h = VAC2 present status change does produce INT<br>1h = VAC2 present status change does NOT produce INT                      |
| 1   | AC1_PRESENT_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VAC1 present mask flag<br>Type : RW<br>POR: 0b<br>0h = VAC1 present status change does produce INT<br>1h = VAC1 present status change does NOT produce INT                      |

**Table 9-49. REG28\_Charger\_Mask\_0 Register Field Descriptions (continued)**

| Bit | Field             | Type | Reset | Notes                | Description  |
|-----|-------------------|------|-------|----------------------|--|
| 0   | VBUS_PRESENT_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VBUS present mask flag<br>Type : RW<br>POR: 0b<br>0h = VBUS present status change does produce INT<br>1h = VBUS present status change does NOT produce INT |

### 9.5.1.37 REG29\_Charger\_Mask\_1 Register (Offset = 29h) [reset = 0h]

REG29\_Charger\_Mask\_1 is shown in [Figure 9-61](#) and described in [Table 9-50](#).

Return to the [Table 9-12](#).

Charger Mask 1

**Figure 9-61. REG29\_Charger\_Mask\_1 Register**

| 7        | 6        | 5        | 4         | 3        | 2         | 1                 | 0               |
|----------|----------|----------|-----------|----------|-----------|-------------------|-----------------|
| CHG_MASK | ICO_MASK | RESERVED | VBUS_MASK | RESERVED | TREG_MASK | VBAT_PRESENT_MASK | BC1.2_DONE_MASK |
| R/W-0h   | R/W-0h   | R-0h     | R/W-0h    | R-0h     | R/W-0h    | R/W-0h            | R/W-0h          |

**Table 9-50. REG29\_Charger\_Mask\_1 Register Field Descriptions**

| Bit | Field             | Type | Reset | Notes                | Description  |
|-----|-------------------|------|-------|----------------------|--|
| 7   | CHG_MASK          | R/W  | 0h    | Reset by:<br>REG_RST | Charge status mask flag<br>Type : RW<br>POR: 0b<br>0h = Charging status change does produce INT<br>1h = Charging status change does NOT produce INT        |
| 6   | ICO_MASK          | R/W  | 0h    | Reset by:<br>REG_RST | ICO status mask flag<br>Type : RW<br>POR: 0b<br>0h = ICO status change does produce INT<br>1h = ICO status change does NOT produce INT                     |
| 5   | RESERVED          | R    | 0h    |                      | RESERVED   |
| 4   | VBUS_MASK         | R/W  | 0h    | Reset by:<br>REG_RST | VBUS status mask flag<br>Type : RW<br>POR: 0b<br>0h = VBUS status change does produce INT<br>1h = VBUS status change does NOT produce INT                  |
| 3   | RESERVED          | R    | 0h    |                      | RESERVED   |
| 2   | TREG_MASK         | R/W  | 0h    | Reset by:<br>REG_RST | IC thermal regulation mask flag<br>Type : RW<br>POR: 0b<br>0h = entering TREG does produce INT<br>1h = entering TREG does NOT produce INT                  |
| 1   | VBAT_PRESENT_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VBAT present mask flag<br>Type : RW<br>POR: 0b<br>0h = VBAT present status change does produce INT<br>1h = VBAT present status change does NOT produce INT |
| 0   | BC1.2_DONE_MASK   | R/W  | 0h    | Reset by:<br>REG_RST | BC1.2 status mask flag<br>Type : RW<br>POR: 0b<br>0h = BC1.2 status change does produce INT<br>1h = BC1.2 status change does NOT produce INT               |

### 9.5.1.38 REG2A\_Charger\_Mask\_2 Register (Offset = 2Ah) [reset = 0h]

REG2A\_Charger\_Mask\_2 is shown in [Figure 9-62](#) and described in [Table 9-51](#).

Return to the [Table 9-12](#).

Charger Mask 2

**Figure 9-62. REG2A\_Charger\_Mask\_2 Register**

| 7        | 6              | 5             | 4         | 3            | 2               | 1               | 0               |
|----------|----------------|---------------|-----------|--------------|-----------------|-----------------|-----------------|
| RESERVED | DPDM_DONE_MASK | ADC_DONE_MASK | VSYS_MASK | CHG_TMR_MASK | TRICHG_TMR_MASK | PRECHG_TMR_MASK | TOPOFF_TMR_MASK |
| R-0h     | R/W-0h         | R/W-0h        | R/W-0h    | R/W-0h       | R/W-0h          | R/W-0h          | R/W-0h          |

**Table 9-51. REG2A\_Charger\_Mask\_2 Register Field Descriptions**

| Bit | Field           | Type | Reset | Notes                | Description   |
|-----|-----------------|------|-------|----------------------|---|
| 7   | RESERVED        | R    | 0h    |                      | RESERVED  |
| 6   | DPDM_DONE_MASK  | R/W  | 0h    | Reset by:<br>REG_RST | D+/D- detection is done mask flag<br>Type : RW<br>POR: 0b<br>0h = D+/D- detection done does produce INT pulse<br>1h = D+/D- detection done does NOT produce INT pulse                     |
| 5   | ADC_DONE_MASK   | R/W  | 0h    | Reset by:<br>REG_RST | ADC conversion mask flag (only in one-shot mode)<br>Type : RW<br>POR: 0b<br>0h = ADC conversion done does produce INT pulse<br>1h = ADC conversion done does NOT produce INT pulse        |
| 4   | VSYS_MASK       | R/W  | 0h    | Reset by:<br>REG_RST | VSYS min regulation mask flag<br>Type : RW<br>POR: 0b<br>0h = enter or exit VSYSMIN regulation does produce INT pulse<br>1h = enter or exit VSYSMIN regulation does NOT produce INT pulse |
| 3   | CHG_TMR_MASK    | R/W  | 0h    | Reset by:<br>REG_RST | Fast charge timer mask flag<br>Type : RW<br>POR: 0b<br>0h = Fast charge timer expire does produce INT<br>1h = Fast charge timer expire does NOT produce INT                               |
| 2   | TRICHG_TMR_MASK | R/W  | 0h    | Reset by:<br>REG_RST | Trickle charge timer mask flag<br>Type : RW<br>POR: 0b<br>0h = Trickle charge timer expire does produce INT<br>1h = Trickle charge timer expire does NOT produce INT                      |
| 1   | PRECHG_TMR_MASK | R/W  | 0h    | Reset by:<br>REG_RST | Pre-charge timer mask flag<br>Type : RW<br>POR: 0b<br>0h = Pre-charge timer expire does produce INT<br>1h = Pre-charge timer expire does NOT produce INT                                  |
| 0   | TOPOFF_TMR_MASK | R/W  | 0h    | Reset by:<br>REG_RST | Top off timer mask flag<br>Type : RW<br>POR: 0b<br>0h = Top off timer expire does produce INT<br>1h = Top off timer expire does NOT produce INT   |

### 9.5.1.39 REG2B\_Charger\_Mask\_3 Register (Offset = 2Bh) [reset = 0h]

REG2B\_Charger\_Mask\_3 is shown in [Figure 9-63](#) and described in [Table 9-52](#).

Return to the [Table 9-12](#).

Charger Mask 3

**Figure 9-63. REG2B\_Charger\_Mask\_3 Register**

| 7        | 6 | 5 | 4                    | 3                | 2                | 1                | 0               |
|----------|---|---|----------------------|------------------|------------------|------------------|-----------------|
| RESERVED |   |   | VBATOTG_LO<br>W_MASK | TS_COLD_MA<br>SK | TS_COOL_MA<br>SK | TS_WARM_MA<br>SK | TS_HOT_MAS<br>K |
| R-0h     |   |   | R/W-0h               | R/W-0h           | R/W-0h           | R/W-0h           | R/W-0h          |

**Table 9-52. REG2B\_Charger\_Mask\_3 Register Field Descriptions**

| Bit | Field                | Type | Reset | Notes                            | Description   |
|-----|----------------------|------|-------|----------------------------------|---|
| 7-5 | RESERVED             | R    | 0h    |                                  | RESERVED  |
| 4   | VBATOTG_LOW_M<br>ASK | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | VBAT too low to enable OTG mask<br>Type : RW<br>POR: 0b<br>0h = VBAT falling below the threshold to enable the<br>OTG mode, does produce INT<br>1h = VBAT falling below the threshold to enable the<br>OTG mode, does NOT produce INT |
| 3   | TS_COLD_MASK         | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | TS cold temperature interrupt mask<br>Type : RW<br>POR: 0b<br>0h = TS across cold temperature (T1) does produce<br>INT<br>1h = TS across cold temperature (T1) does NOT<br>produce INT  |
| 2   | TS_COOL_MASK         | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | TS cool temperature interrupt mask<br>Type : RW<br>POR: 0b<br>0h = TS across cool temperature (T2) does produce<br>INT<br>1h = TS across cool temperature (T2) does NOT<br>produce INT  |
| 1   | TS_WARM_MASK         | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | TS warm temperature interrupt mask<br>Type : RW<br>POR: 0b<br>0h = TS across warm temperature (T3) does produce<br>INT<br>1h = TS across warm temperature (T3) does NOT<br>produce INT  |
| 0   | TS_HOT_MASK          | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | TS hot temperature interrupt mask<br>Type : RW<br>POR: 0b<br>0h = TS across hot temperature (T5) does produce<br>INT<br>1h = TS across hot temperature (T5) does NOT<br>produce INT   |

### 9.5.1.40 REG2C\_FAULT\_Mask\_0 Register (Offset = 2Ch) [reset = 0h]

REG2C\_FAULT\_Mask\_0 is shown in [Figure 9-64](#) and described in [Table 9-53](#).

Return to the [Table 9-12](#).

FAULT Mask 0

**Figure 9-64. REG2C\_FAULT\_Mask\_0 Register**

| 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| IBAT_REG_MA<br>SK | VBUS_OVP_M<br>ASK | VBAT_OVP_M<br>ASK | IBUS_OCP_MA<br>SK | IBAT_OCP_MA<br>SK | CONV_OCP_M<br>ASK | VAC2_OVP_M<br>ASK | VAC1_OVP_M<br>ASK |
| R/W-0h            | R/W-0h            | R/W-0h            | R/W-0h            | R/W-0h            | R/W-0h            | R/W-0h            | R/W-0h            |

**Table 9-53. REG2C\_FAULT\_Mask\_0 Register Field Descriptions**

| Bit | Field         | Type | Reset | Notes                | Description   |
|-----|---------------|------|-------|----------------------|---|
| 7   | IBAT_REG_MASK | R/W  | 0h    | Reset by:<br>REG_RST | IBAT regulation mask flag<br>Type : RW<br>POR: 0b<br>0h = enter or exit IBAT regulation does produce INT<br>1h = enter or exit IBAT regulation does NOT produce INT |
| 6   | VBUS_OVP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VBUS over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = entering VBUS OVP does produce INT<br>1h = entering VBUS OVP does NOT produce INT                       |
| 5   | VBAT_OVP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VBAT over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = entering VBAT OVP does produce INT<br>1h = entering VBAT OVP does NOT produce INT                       |
| 4   | IBUS_OCP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | IBUS over-current mask flag<br>Type : RW<br>POR: 0b<br>0h = IBUS OCP fault does produce INT<br>1h = IBUS OCP fault does NOT produce INT                             |
| 3   | IBAT_OCP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | IBAT over-current mask flag<br>Type : RW<br>POR: 0b<br>0h = IBAT OCP fault does produce INT<br>1h = IBAT OCP fault does NOT produce INT                             |
| 2   | CONV_OCP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | Converter over-current mask flag<br>Type : RW<br>POR: 0b<br>0h = Converter OCP fault does produce INT<br>1h = Converter OCP fault does NOT produce INT              |
| 1   | VAC2_OVP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VAC2 over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = entering VAC2 OVP does produce INT<br>1h = entering VAC2 OVP does NOT produce INT                       |
| 0   | VAC1_OVP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VAC1 over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = entering VAC1 OVP does produce INT<br>1h = entering VAC1 OVP does NOT produce INT                       |

### 9.5.1.41 REG2D\_FAULT\_Mask\_1 Register (Offset = 2Dh) [reset = 0h]

REG2D\_FAULT\_Mask\_1 is shown in [Figure 9-65](#) and described in [Table 9-54](#).

Return to the [Table 9-12](#).

FAULT Mask 1

**Figure 9-65. REG2D\_FAULT\_Mask\_1 Register**

| 7               | 6             | 5            | 4            | 3        | 2          | 1        | 0 |
|-----------------|---------------|--------------|--------------|----------|------------|----------|---|
| VSYS_SHORT_MASK | VSYS_OVP_MASK | OTG_OVP_MASK | OTG_UVP_MASK | RESERVED | TSHUT_MASK | RESERVED |   |
| R/W-0h          | R/W-0h        | R/W-0h       | R/W-0h       | R/W-0h   | R/W-0h     | R-0h     |   |

**Table 9-54. REG2D\_FAULT\_Mask\_1 Register Field Descriptions**

| Bit | Field           | Type | Reset | Notes                | Description   |
|-----|-----------------|------|-------|----------------------|---|
| 7   | VSYS_SHORT_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VSYS short circuit mask flag<br>Type : RW<br>POR: 0b<br>0h = System short fault does produce INT<br>1h = System short fault does NOT produce INT                    |
| 6   | VSYS_OVP_MASK   | R/W  | 0h    | Reset by:<br>REG_RST | VSYS over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = System over-voltage fault does produce INT<br>1h = System over-voltage fault does NOT produce INT       |
| 5   | OTG_OVP_MASK    | R/W  | 0h    | Reset by:<br>REG_RST | OTG over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = OTG VBUS over-voltage fault does produce INT<br>1h = OTG VBUS over-voltage fault does NOT produce INT    |
| 4   | OTG_UVP_MASK    | R/W  | 0h    | Reset by:<br>REG_RST | OTG under-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = OTG VBUS under voltage fault does produce INT<br>1h = OTG VBUS under voltage fault does NOT produce INT |
| 3   | RESERVED        | R/W  | 0h    |                      | RESERVED  |
| 2   | TSHUT_MASK      | R/W  | 0h    | Reset by:<br>REG_RST | IC thermal shutdown mask flag<br>Type : RW<br>POR: 0b<br>0h = TSHUT does produce INT<br>1h = TSHUT does NOT produce INT   |
| 1-0 | RESERVED        | R    | 0h    |                      | RESERVED  |

### 9.5.1.42 REG2E\_ADC\_Control Register (Offset = 2Eh) [reset = 30h]

REG2E\_ADC\_Control is shown in [Figure 9-66](#) and described in [Table 9-55](#).

Return to the [Table 9-12](#).

ADC Control

**Figure 9-66. REG2E\_ADC\_Control Register**

| 7      | 6        | 5              | 4       | 3            | 2        | 1 | 0 |
|--------|----------|----------------|---------|--------------|----------|---|---|
| ADC_EN | ADC_RATE | ADC_SAMPLE_1:0 | ADC_AVG | ADC_AVG_INIT | RESERVED |   |   |
| R/W-0h | R/W-0h   | R/W-3h         | R/W-0h  | R/W-0h       | R/W-0h   |   |   |

**Table 9-55. REG2E\_ADC\_Control Register Field Descriptions**

| Bit | Field          | Type | Reset | Notes                            | Description   |
|-----|----------------|------|-------|----------------------------------|---|
| 7   | ADC_EN         | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | ADC Control<br>Type : RW<br>POR: 0b<br>0h = Disable<br>1h = Enable  |
| 6   | ADC_RATE       | R/W  | 0h    | Reset by:<br>REG_RST             | ADC conversion rate control<br>Type : RW<br>POR: 0b<br>0h = Continuous conversion<br>1h = One shot conversion   |
| 5-4 | ADC_SAMPLE_1:0 | R/W  | 3h    | Reset by:<br>REG_RST             | ADC sample speed<br>Type : RW<br>POR: 11b<br>0h = 15 bit effective resolution<br>1h = 14 bit effective resolution<br>2h = 13 bit effective resolution<br>3h = 12 bit effective resolution (default - not recommended) |
| 3   | ADC_AVG        | R/W  | 0h    | Reset by:<br>REG_RST             | ADC average control<br>Type : RW<br>POR: 0b<br>0h = Single value<br>1h = Running average  |
| 2   | ADC_AVG_INIT   | R/W  | 0h    | Reset by:<br>REG_RST             | ADC average initial value control<br>Type : RW<br>POR: 0b<br>0h = Start average using the existing register value<br>1h = Start average using a new ADC conversion  |
| 1-0 | RESERVED       | R/W  | 0h    |                                  | RESERVED  |



### 9.5.1.43 REG2F\_ADC\_Function\_Disable\_0 Register (Offset = 2Fh) [reset = 0h]

REG2F\_ADC\_Function\_Disable\_0 is shown in [Figure 9-67](#) and described in [Table 9-56](#).

Return to the [Table 9-12](#).

ADC Function Disable 0

**Figure 9-67. REG2F\_ADC\_Function\_Disable\_0 Register**

| 7            | 6            | 5            | 4            | 3            | 2          | 1            | 0        |
|--------------|--------------|--------------|--------------|--------------|------------|--------------|----------|
| IBUS_ADC_DIS | IBAT_ADC_DIS | VBUS_ADC_DIS | VBAT_ADC_DIS | VSYS_ADC_DIS | TS_ADC_DIS | TDIE_ADC_DIS | RESERVED |
| R/W-0h       | R/W-0h       | R/W-0h       | R/W-0h       | R/W-0h       | R/W-0h     | R/W-0h       | R-0h     |

**Table 9-56. REG2F\_ADC\_Function\_Disable\_0 Register Field Descriptions**

| Bit | Field        | Type | Reset | Notes                | Description   |
|-----|--------------|------|-------|----------------------|---|
| 7   | IBUS_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | IBUS ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 6   | IBAT_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | IBAT ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 5   | VBUS_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | VBUS ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 4   | VBAT_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | VBAT ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 3   | VSYS_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | VSYS ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 2   | TS_ADC_DIS   | R/W  | 0h    | Reset by:<br>REG_RST | TS ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |
| 1   | TDIE_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | TDIE ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 0   | RESERVED     | R    | 0h    |                      | RESERVED  |

#### 9.5.1.44 REG30\_ADC\_Function\_Disable\_1 Register (Offset = 30h) [reset = 0h]

REG30\_ADC\_Function\_Disable\_1 is shown in [Figure 9-68](#) and described in [Table 9-57](#).

Return to the [Table 9-12](#).

ADC Function Disable 1

**Figure 9-68. REG30\_ADC\_Function\_Disable\_1 Register**

| 7          | 6          | 5            | 4            | 3        | 2 | 1 | 0 |
|------------|------------|--------------|--------------|----------|---|---|---|
| DP_ADC_DIS | DM_ADC_DIS | VAC2_ADC_DIS | VAC1_ADC_DIS | RESERVED |   |   |   |
| R/W-0h     | R/W-0h     | R/W-0h       | R/W-0h       | R-0h     |   |   |   |

**Table 9-57. REG30\_ADC\_Function\_Disable\_1 Register Field Descriptions**

| Bit | Field        | Type | Reset | Notes                | Description   |
|-----|--------------|------|-------|----------------------|---|
| 7   | DP_ADC_DIS   | R/W  | 0h    | Reset by:<br>REG_RST | D+ ADC Control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |
| 6   | DM_ADC_DIS   | R/W  | 0h    | Reset by:<br>REG_RST | D- ADC Control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |
| 5   | VAC2_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | VAC2 ADC Control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 4   | VAC1_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | VAC1 ADC Control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 3-0 | RESERVED     | R    | 0h    |                      | RESERVED  |

### 9.5.1.45 REG31\_IBUS\_ADC Register (Offset = 31h) [reset = 0h]

REG31\_IBUS\_ADC is shown in [Figure 9-69](#) and described in [Table 9-58](#).

Return to the [Table 9-12](#).

IBUS ADC

**Figure 9-69. REG31\_IBUS\_ADC Register**

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IBUS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| IBUS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

**Table 9-58. REG31\_IBUS\_ADC Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 15-0 | IBUS_ADC_15:0 | R    | 0h    | IBUS ADC reading<br>Reported in 2's Complement.<br>When the current is flowing from VBUS to PMID, IBUS ADC reports positive value, and when the current is flowing from PMID to VBUS, IBUS ADC reports negative value.<br>Type : R<br>POR: 0mA (0h)<br>Range : 0mA-5000mA<br>Fixed Offset : 0mA<br>Bit Step Size : 1mA |

### 9.5.1.46 REG33\_IBAT\_ADC Register (Offset = 33h) [reset = 0h]

REG33\_IBAT\_ADC is shown in [Figure 9-70](#) and described in [Table 9-59](#).

Return to the [Table 9-12](#).

IBAT ADC

**Figure 9-70. REG33\_IBAT\_ADC Register**

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IBAT_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| IBAT_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

**Table 9-59. REG33\_IBAT\_ADC Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 15-0 | IBAT_ADC_15:0 | R    | 0h    | <p>IBAT ADC reading<br/>Reported in 2's Complement.<br/>The IBAT ADC reports positive value for the battery charging current, and negative value for the battery discharging current if EN_IBAT in REG0x14[5] = 1.</p> <p>Type : R<br/>POR: 0mA (0h)<br/>Range : 0mA-8000mA<br/>Fixed Offset : 0mA<br/>Bit Step Size : 1mA</p> |

### 9.5.1.47 REG35\_VBUS\_ADC Register (Offset = 35h) [reset = 0h]

REG35\_VBUS\_ADC is shown in [Figure 9-71](#) and described in [Table 9-60](#).

Return to the [Table 9-12](#).

VBUS ADC

**Figure 9-71. REG35\_VBUS\_ADC Register**

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VBUS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VBUS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

**Table 9-60. REG35\_VBUS\_ADC Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description   |
|------|---------------|------|-------|---|
| 15-0 | VBUS_ADC_15:0 | R    | 0h    | VBUS ADC reading<br>Type : R<br>POR: 0mV (0h)<br>Range : 0mV-30000mV<br>Fixed Offset : 0mV<br>Bit Step Size : 1mV |

### 9.5.1.48 REG37\_VAC1\_ADC Register (Offset = 37h) [reset = 0h]

REG37\_VAC1\_ADC is shown in [Figure 9-72](#) and described in [Table 9-61](#).

Return to the [Table 9-12](#).

VAC1 ADC

**Figure 9-72. REG37\_VAC1\_ADC Register**

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VAC1_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VAC1_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

**Table 9-61. REG37\_VAC1\_ADC Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 15-0 | VAC1_ADC_15:0 | R    | 0h    | VAC1 ADC reading.<br>Type : R<br>POR: 0mV (0h)<br>Range : 0mV-30000mV<br>Fixed Offset : 0mV<br>Bit Step Size : 1mV |

### 9.5.1.49 REG39\_VAC2\_ADC Register (Offset = 39h) [reset = 0h]

REG39\_VAC2\_ADC is shown in [Figure 9-73](#) and described in [Table 9-62](#).

Return to the [Table 9-12](#).

VAC2 ADC

**Figure 9-73. REG39\_VAC2\_ADC Register**

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VAC2_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VAC2_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

**Table 9-62. REG39\_VAC2\_ADC Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 15-0 | VAC2_ADC_15:0 | R    | 0h    | VAC2 ADC reading.<br>Type : R<br>POR: 0mV (0h)<br>Range : 0mV-30000mV<br>Fixed Offset : 0mV<br>Bit Step Size : 1mV |

### 9.5.1.50 REG3B\_VBAT\_ADC Register (Offset = 3Bh) [reset = 0h]

REG3B\_VBAT\_ADC is shown in [Figure 9-74](#) and described in [Table 9-63](#).

Return to the [Table 9-12](#).

VBAT ADC

**Figure 9-74. REG3B\_VBAT\_ADC Register**

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VBAT_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VBAT_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

**Table 9-63. REG3B\_VBAT\_ADC Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description   |
|------|---------------|------|-------|---|
| 15-0 | VBAT_ADC_15:0 | R    | 0h    | The battery remote sensing voltage (VBATP-GND) ADC reading<br>Type : R<br>POR: 0mV (0h)<br>Range : 0mV-20000mV<br>Fixed Offset : 0mV<br>Bit Step Size : 1mV |



### 9.5.1.51 REG3D\_VSYS\_ADC Register (Offset = 3Dh) [reset = 0h]

REG3D\_VSYS\_ADC is shown in [Figure 9-75](#) and described in [Table 9-64](#).

Return to the [Table 9-12](#).

VSYS ADC

**Figure 9-75. REG3D\_VSYS\_ADC Register**

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VSYS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VSYS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

**Table 9-64. REG3D\_VSYS\_ADC Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description   |
|------|---------------|------|-------|---|
| 15-0 | VSYS_ADC_15:0 | R    | 0h    | VSYS ADC reading<br>Type : R<br>POR: 0mV (0h)<br>Range : 0mV-24000mV<br>Fixed Offset : 0mV<br>Bit Step Size : 1mV |

### 9.5.1.52 REG3F\_TS\_ADC Register (Offset = 3Fh) [reset = 0h]

REG3F\_TS\_ADC is shown in [Figure 9-76](#) and described in [Table 9-65](#).

Return to the [Table 9-12](#).

TS ADC

**Figure 9-76. REG3F\_TS\_ADC Register**

|             |    |    |    |    |    |   |   |
|-------------|----|----|----|----|----|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h        |    |    |    |    |    |   |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| TS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h        |    |    |    |    |    |   |   |

**Table 9-65. REG3F\_TS\_ADC Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description  |
|------|-------------|------|-------|--|
| 15-0 | TS_ADC_15:0 | R    | 0h    | TS ADC reading<br>Type : R<br>POR: 0% (0h)<br>Range : 0%-99.9023%<br>Fixed Offset : 0%<br>Bit Step Size : 0.0976563% |

### 9.5.1.53 REG41\_TDIE\_ADC Register (Offset = 41h) [reset = 0h]

REG41\_TDIE\_ADC is shown in [Figure 9-77](#) and described in [Table 9-66](#).

Return to the [Table 9-12](#).

TDIE\_ADC

**Figure 9-77. REG41\_TDIE\_ADC Register**

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TDIE_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| TDIE_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

**Table 9-66. REG41\_TDIE\_ADC Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description   |
|------|---------------|------|-------|---|
| 15-0 | TDIE_ADC_15:0 | R    | 0h    | TDIE ADC reading<br>Reported in 2 's Complement.<br>Type : R<br>POR: 0°C (0h)<br>Range : -40°C-150°C<br>Fixed Offset : 0°C<br>Bit Step Size : 0.5°C |

#### 9.5.1.54 REG43\_D+\_ADC Register (Offset = 43h) [reset = 0h]

REG43\_D+\_ADC is shown in [Figure 9-78](#) and described in [Table 9-67](#).

Return to the [Table 9-12](#).

D+ ADC

**Figure 9-78. REG43\_D+\_ADC Register**

|             |    |    |    |    |    |   |   |
|-------------|----|----|----|----|----|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| D+_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h        |    |    |    |    |    |   |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| D+_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h        |    |    |    |    |    |   |   |

**Table 9-67. REG43\_D+\_ADC Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description  |
|------|-------------|------|-------|--|
| 15-0 | D+_ADC_15:0 | R    | 0h    | D+ ADC reading<br>Type : R<br>POR: 0mV (0h)<br>Range : 0mV-3600mV<br>Fixed Offset : 0mV<br>Bit Step Size : 1mV |

### 9.5.1.55 REG45\_D- \_ADC Register (Offset = 45h) [reset = 0h]

REG45\_D- \_ADC is shown in [Figure 9-79](#) and described in [Table 9-68](#).

Return to the [Table 9-12](#).

D- ADC

**Figure 9-79. REG45\_D- \_ADC Register**

|              |    |    |    |    |    |   |   |
|--------------|----|----|----|----|----|---|---|
| 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| D- _ADC_15:0 |    |    |    |    |    |   |   |
| R-0h         |    |    |    |    |    |   |   |
| 7            | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| D- _ADC_15:0 |    |    |    |    |    |   |   |
| R-0h         |    |    |    |    |    |   |   |

**Table 9-68. REG45\_D- \_ADC Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description  |
|------|--------------|------|-------|--|
| 15-0 | D- _ADC_15:0 | R    | 0h    | D- ADC reading<br>Type : R<br>POR: 0mV (0h)<br>Range : 0mV-3600mV<br>Fixed Offset : 0mV<br>Bit Step Size : 1mV |

### 9.5.1.56 REG47\_DPDM\_Driver Register (Offset = 47h) [reset = 0h]

REG47\_DPDM\_Driver is shown in [Figure 9-80](#) and described in [Table 9-69](#).

Return to the [Table 9-12](#).

DPDM Driver

**Figure 9-80. REG47\_DPDM\_Driver Register**

| 7             | 6 | 5 | 4              | 3 | 2 | 1        | 0 |
|---------------|---|---|----------------|---|---|----------|---|
| DPLUS_DAC_2:0 |   |   | DMINUS_DAC_2:0 |   |   | RESERVED |   |
| R/W-0h        |   |   | R/W-0h         |   |   | R/W-0h   |   |

**Table 9-69. REG47\_DPDM\_Driver Register Field Descriptions**

| Bit | Field          | Type | Reset | Description   |
|-----|----------------|------|-------|---|
| 7-5 | DPLUS_DAC_2:0  | R/W  | 0h    | D+ Output Driver<br>Type : RW<br>POR: 000b<br><br>0h = HIZ<br>1h = 0<br>2h = 0.6V<br>3h = 1.2V<br>4h = 2.0V<br>5h = 2.7V<br>6h = 3.3V<br>7h = D+/D- Short |
| 4-2 | DMINUS_DAC_2:0 | R/W  | 0h    | D- Output Driver<br>Type : RW<br>POR: 000b<br><br>0h = HIZ<br>1h = 0<br>2h = 0.6V<br>3h = 1.2V<br>4h = 2.0V<br>5h = 2.7V<br>6h = 3.3V<br>7h = reserved    |
| 1-0 | RESERVED       | R/W  | 0h    | RESERVED  |

### 9.5.1.57 REG48\_Part\_Information Register (Offset = 48h) [reset = 0h]

REG48\_Part\_Information is shown in [Figure 9-81](#) and described in [Table 9-70](#).

Return to the [Table 9-12](#).

Part Information

**Figure 9-81. REG48\_Part\_Information Register**

| 7        | 6 | 5      | 4 | 3 | 2           | 1 | 0 |
|----------|---|--------|---|---|-------------|---|---|
| RESERVED |   | PN_2:0 |   |   | DEV_REV_2:0 |   |   |
| R-0h     |   | R-0h   |   |   | R-0h        |   |   |

**Table 9-70. REG48\_Part\_Information Register Field Descriptions**

| Bit | Field       | Type | Reset | Description   |
|-----|-------------|------|-------|---|
| 7-6 | RESERVED    | R    | 0h    | RESERVED  |
| 5-3 | PN_2:0      | R    | 1h    | Device Part number<br>POR: 001b = BQ25792<br>All the other options are reserved<br>Type : R |
| 2-0 | DEV_REV_2:0 | R    | 0h    | Device Revision<br>POR: 000b = BQ25792<br>Type : R  |

## 10 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

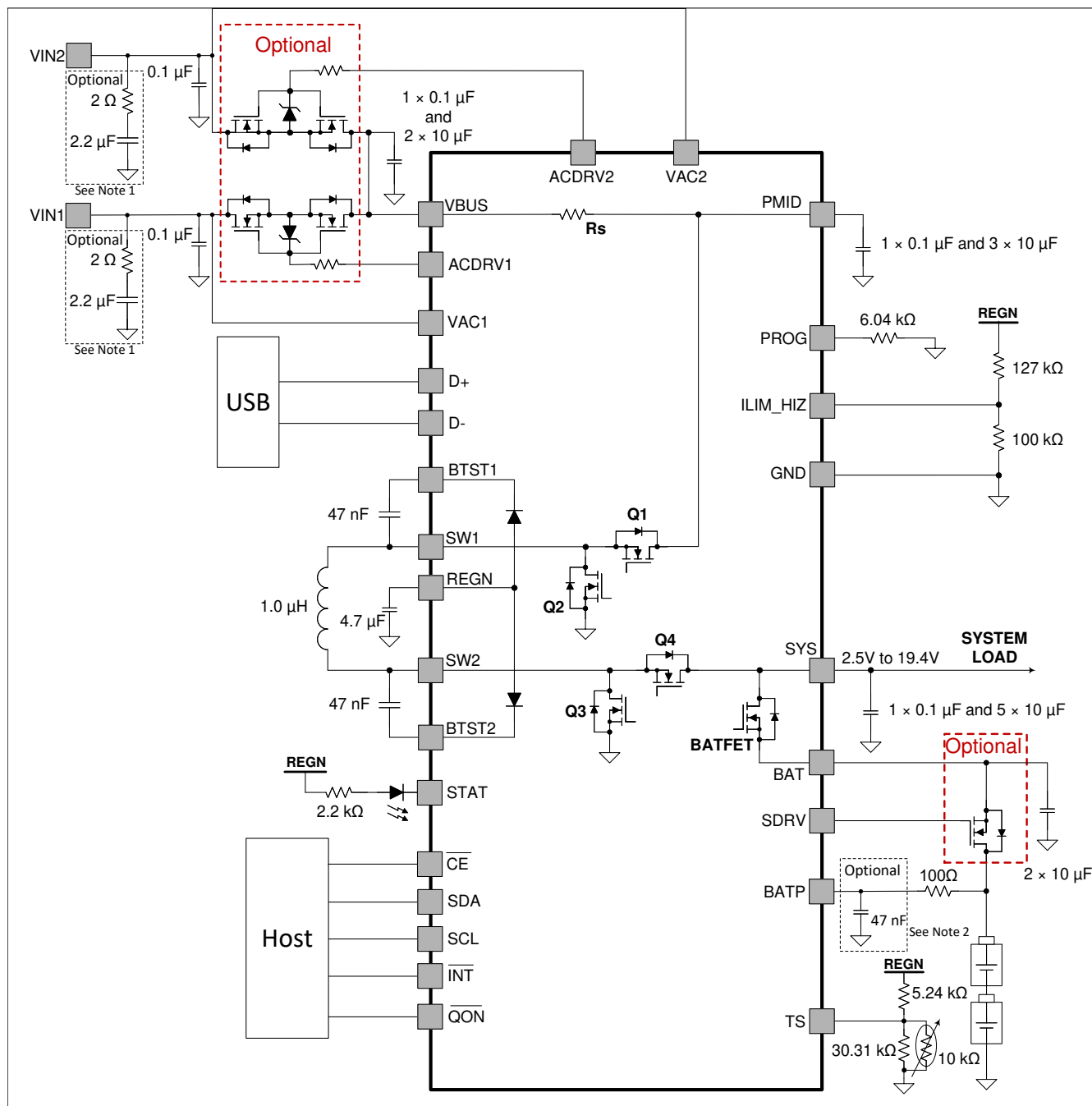
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### 10.1 Application Information

A typical application consists of the device configured as an I<sup>2</sup>C controlled power path management device and a multi-cell battery charger for Li-Ion and Li-polymer batteries. It integrates the four switching MOSFETs (Q<sub>1</sub> to Q<sub>4</sub>) for the buck-boost converter, and the battery FET (BATFET) between system and battery. The device also integrates the input current sensing and charging current sensing circuitries, the bootstrap diode for the high-side gate driving and the dual-input power mux for the power sources selection.

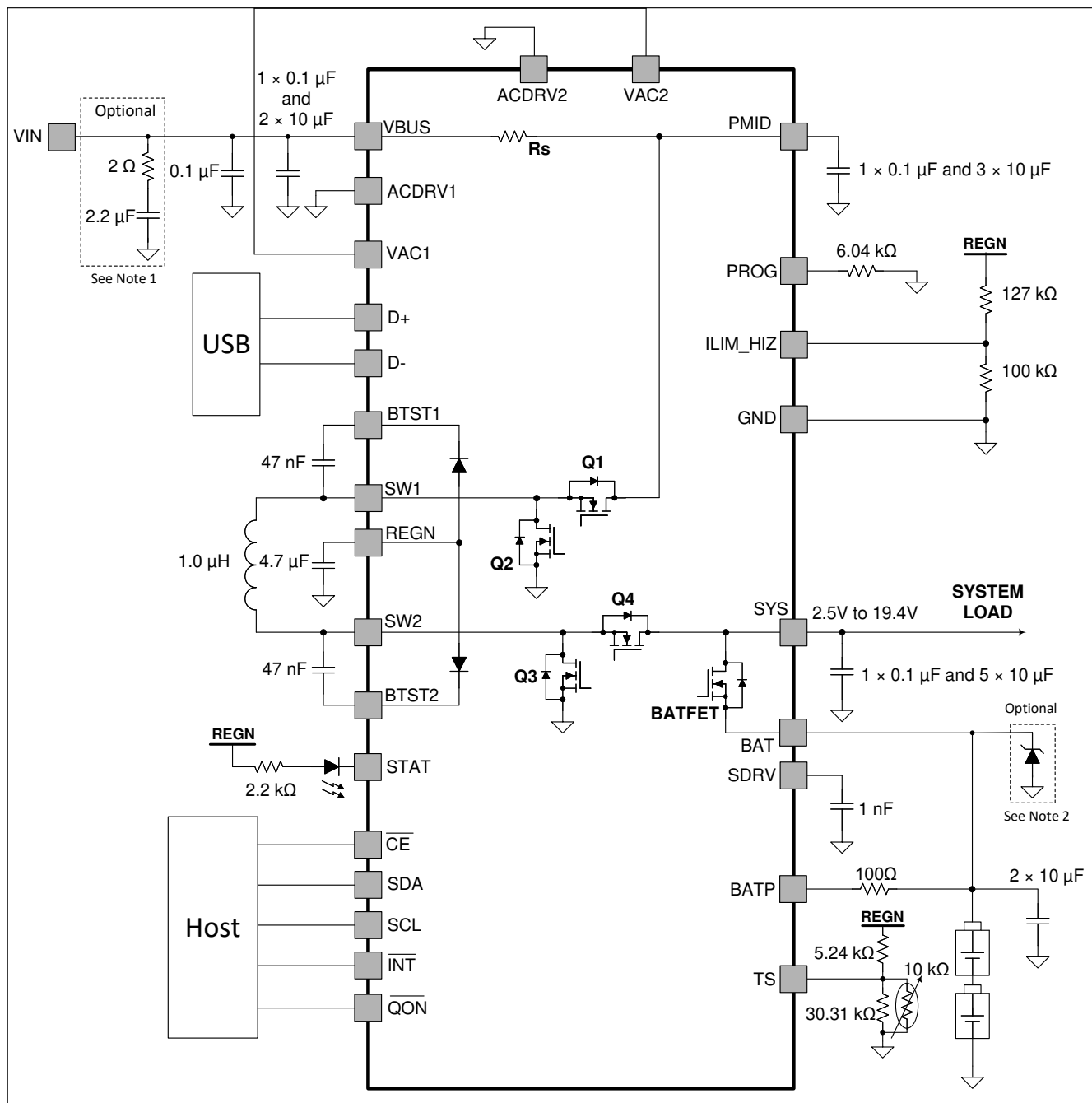


## 10.2 Typical Application



**Figure 10-1. BQ25792 Application Diagram with Two Input Sources and Ship FET**

1. Recommended if hot plugging adapters > 15 V.
2. Recommended if hot plugging 4S battery packs with long leads or PCB traces.



**Figure 10-2. BQ25792 Application Diagram with Single Input Source and No Ship FET**

1. Recommended if hot plugging adapters > 15 V.
2. Recommended if hot plugging 4S battery packs with long leads or PCB traces.

### 10.2.1 Design Requirements

For this design example, use the parameters shown in the table below.

**Table 10-1. Design Parameters**

| PARAMETER  | VALUE       |
|--|-------------|
| V <sub>BUS</sub> voltage range                       | 5 V to 20 V |
| Input current limit (I <sub>INDPM</sub> [8:0])       | 3.0 A       |
| Fast charge current limit (I <sub>CHG</sub> [8:0])   | 3.0 A       |
| Battery regulation voltage (V <sub>REG</sub> [10:0]) | 8.4 V       |

### 10.2.2 Detailed Design Procedure

#### 10.2.2.1 Inductor Selection

The device has 1.5 MHz switching frequency to allow the use of small inductor (1μH) and capacitor values. It also provide the 750kHz switching frequency to achieve higher efficiency for the applications which have enough design space to accommodate the larger inductor (2.2 μH) and capacitors. Please note that the 1.5 MHz switching frequency only works with the 1μH inductor and the 750 kHz switching frequency only works with the 2.2μH inductor.

Because the converter might be either operated in the buck mode or the boost mode, so the inductor current is equal to either the charging current or the input current. The inductor saturation current should be higher than the larger value of the input current (I<sub>IN</sub>) or the charging current (I<sub>CHG</sub>) plus half the ripple current (I<sub>RIPPLE</sub>):

$$I_{SAT} \geq \max \left[ \left( I_{IN} + \frac{I_{RIPPLE}}{2} \right), \left( I_{CHG} + \frac{I_{RIPPLE}}{2} \right) \right] \quad (4)$$

The inductor ripple current (I<sub>RIPPLE</sub>) depends on the input voltage (V<sub>BUS</sub>), the output voltage (V<sub>SYS</sub>), the switching frequency (F<sub>SW</sub>) and the inductance (L). The inductor current ripples for buck mode and boost mode are calculated with equations (4) and (5), respectively:

$$I_{RIPPLE\_BUCK} = \frac{V_{SYS} \times (V_{BUS} - V_{SYS})}{V_{BUS} \times F_{SW} \times L} \quad (5)$$

$$I_{RIPPLE\_BOOST} = \frac{V_{BUS} \times (V_{SYS} - V_{BUS})}{V_{SYS} \times F_{SW} \times L} \quad (6)$$

The inductor current ripple in the buck mode is usually larger than that in the boost mode, since the voltage-second applied on the inductor is larger. The maximum inductor current ripple in the buck mode happens in the vicinity of  $D = V_{SYS} / V_{BUS} = 0.5$ . The SYS voltage is approximately 8V for the 2s battery configuration, so the worst case for the inductor ripples is with the 15V or 20V input voltage.

#### 10.2.2.2 Input (V<sub>BUS</sub> / P<sub>MD</sub>) Capacitor

In the buck mode operation, the input current is discontinuous, which dominates the input RMS ripple current and input voltage ripple. The input capacitors should have enough ripple current rating to absorb the input AC current and have large enough capacitance to maintain the small input voltage ripple. For the buck mode operation, the input RMS ripple current is calculated by the equation (6) and the input voltage ripple is calculated by the equation (7), where  $D = V_{SYS} / V_{BUS}$ .

$$I_{CIN\_BUCK} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (7)$$

$$\Delta V_{IN\_BUCK} = \frac{D \times (1 - D) \times I_{CHG}}{C_{IN} \times F_{SW}} \quad (8)$$

The worst case input RMS ripple current and input voltage ripple both occur at 0.5 duty cycle condition. The SYS voltage is approximately 8V for the 2s battery configuration, so the worst case is when 15V to 20V VBUS condition. Low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed close to the PMID and GND pins of the IC. The voltage rating of the capacitor must be higher than the normal input voltage level. The capacitor with 25V or higher voltage rating is preferred for up to 20V input voltage. 1\*0.1 µF + 3\*10 µF ceramic capacitors are suggested for up to 3.3-A input current limit to support the converter in forward mode.

#### 10.2.2.3 Output (V<sub>SY</sub>) Capacitor

In the boost mode operation, the output current is discontinuous, which dominates the output RMS ripple current and output voltage ripple. The output capacitors should have enough ripple current rating to absorb the output AC current and have large enough capacitance to maintain the small output voltage ripple. For the boost mode operation, the output RMS ripple current is calculated by the equation (8) and the output voltage ripple is calculated by the equation (9), where  $D = (1 - V_{BUS} / V_{SYS})$ .

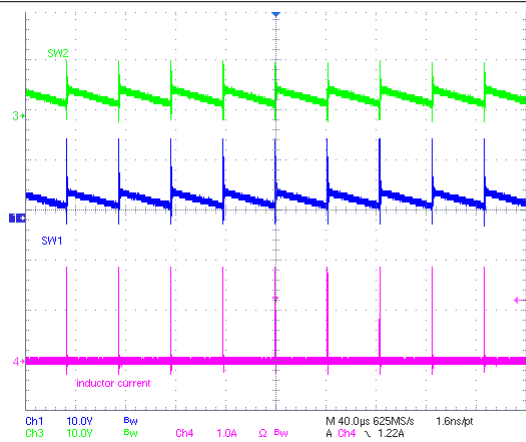
$$I_{COUT\_BOOST} = I_{CHG} \times \sqrt{\frac{D}{(1-D)}} \quad (9)$$

$$\Delta V_{OUT\_BOOST} = \frac{I_{CHG} \times D}{C_{OUT} \times F_{SW}} \quad (10)$$

The worst case output RMS ripple current and output voltage ripple both occur at the lowest VBUS input voltage. The SYS voltage is approximately 8V for the 2s battery configuration, so the worst case is 5V VBUS condition. Low ESR ceramic capacitor such as X7R or X5R is preferred for the output decoupling capacitor and should be placed close to the SYS and GND pins of the IC. The voltage rating of the capacitor must be higher than the normal input voltage level. The capacitor with 16V or higher voltage rating is preferred for the 2s battery configuration. 1\*0.1 µF + 5\*10 µF capacitors are suggested for up to 5A charging current.

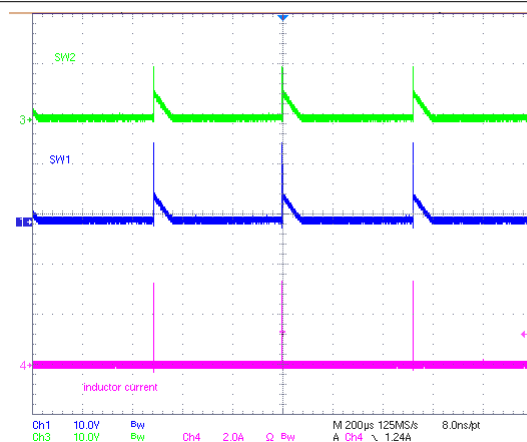
### 10.2.3 Application Curves

$C_{VBUS} = 2 \times 10 \mu\text{F}$ ,  $C_{PMID} = 3 \times 10 \mu\text{F}$ ,  $C_{SYS} = 5 \times 10 \mu\text{F}$ ,  $C_{BAT} = 2 \times 10 \mu\text{F}$ ,  $L1 = 1 \mu\text{H}$  (SPM6530T-1R0M120),  $F_{sw} = 1.5\text{MHz}$ .



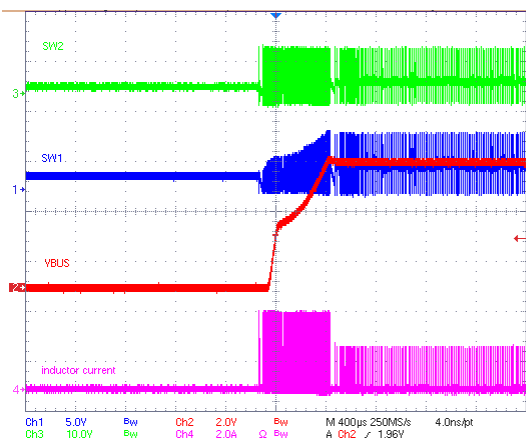
VBUS = 15V VBAT = 8V ICHG = 0A

**Figure 10-3. Buck Mode PFM with OOA**



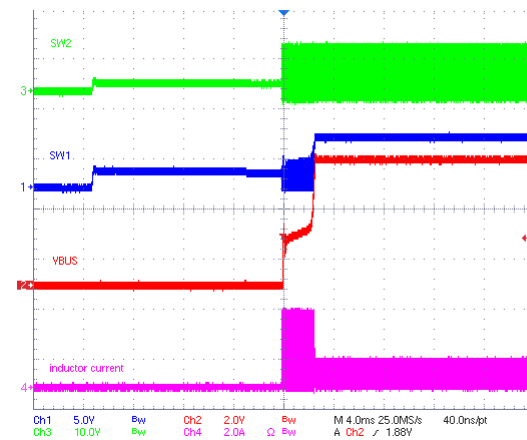
VBUS = 15V VBAT = 8V ICHG = 0A

**Figure 10-4. Buck Mode PFM without OOA**



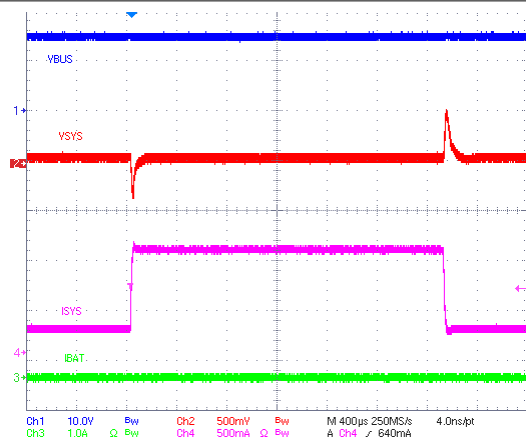
VBAT = 8V VOTG = 5V IBUS = 0A

**Figure 10-5. OTG Startup at No Load**



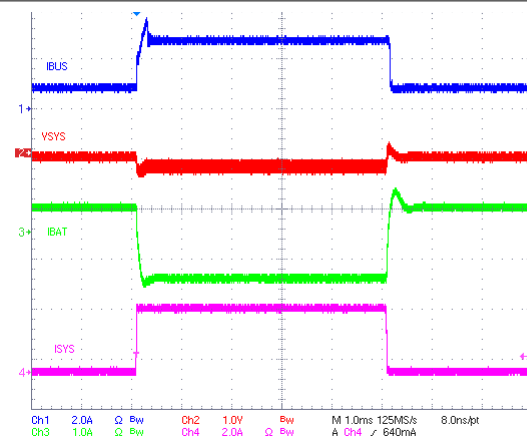
VBAT = 8V VOTG = 5V IBUS = 500mA

**Figure 10-6. OTG Startup at 500-mA Load**



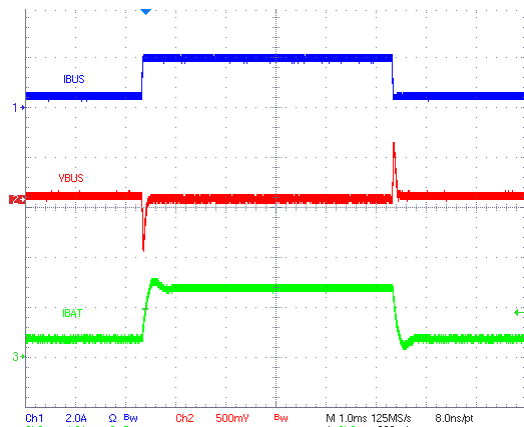
VBUS = 15V VBAT = 8V Charge disabled

**Figure 10-7. VSYS Load Transient Response**



VBUS = 5V VBAT = 8V Charge enabled

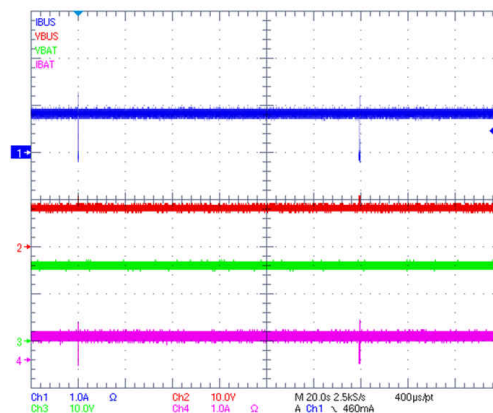
**Figure 10-8. IINDPM Transient Response**



VBAT = 8V

VOTG = 5V

**Figure 10-9. VOTG Load Transient Response**

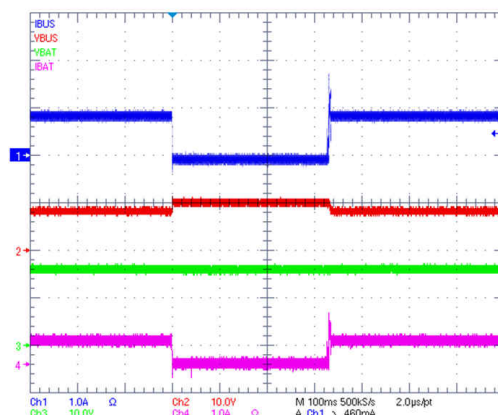


VOC = 10V

VMPP = 8.1V

VBAT = 8V

**Figure 10-10. MPPT Operation**



VOC = 10V

VMPP = 8.1V

VBAT = 8V

**Figure 10-11. MPPT Operation Zoom**

## 11 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.6 V and 24 V input with recommended >500mA current rating connected to VBUS or a 1s to 4s Li-Ion battery with voltage higher than  $V_{BAT\_UVLO}$  connected to BAT. The source current rating needs to be at least 3A for the buck-boost converter of the charger to provide maximum output power to SYS.

The charger does not support the testing condition when the battery connection is floating. The BAT pin has to be connected to a real battery or some devices which can emulate the battery, like the battery emulator or bulk capacitors. When the BAT pin is floating, please disable charge by setting EN\_CHG to 0 or pulling low the  $\overline{CE}$  pin. Otherwise, the voltage overshoot at SYS might trigger the SYSOVP protection periodically.

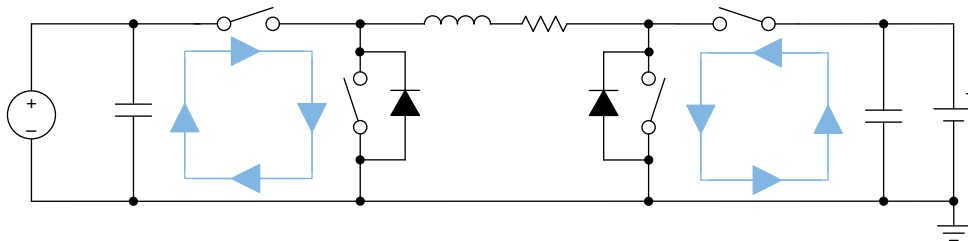
## 12 Layout

### 12.1 Layout Guidelines

The switching nodes rising and falling times should be minimized for minimum switching loss. Proper layout of the components to minimize the high frequency current path loops (shown in the figure below) is important to prevent the electrical and magnetic field radiation and the high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place the SYS output capacitors as close to SYS and GND as possible. Place a 0.1  $\mu\text{F}$  small size (such as 0402 or 0201) capacitor closer than the other 10  $\mu\text{F}$  capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
2. Place the PMID input capacitors as close to PMID and GND as possible. Place a 0.1  $\mu\text{F}$  small size (such as 0402 or 0201) capacitor closer than the other 10  $\mu\text{F}$  capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
3. Place the VBUS input capacitors as close to VBUS and GND as possible. Place a 0.1  $\mu\text{F}$  small size (such as 0402 or 0201) capacitor closer than the other 10  $\mu\text{F}$  capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. The connection from SYS/PMID/VBUS to the 0.1  $\mu\text{F}$  has to be routed on the top layer of the PCB, the returning back to GND also has to be in the top layer. Keep the whole routing loop as small as possible.
5. Place the inductor input terminal to SW1 and the inductor output terminal to SW2 as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the inductor current. Minimize parasitic capacitance from this area to any other trace or plane.
6. Place the BAT capacitors close to BAT and GND, place the VBUS capacitors close to VBUS and GND.
7. The REGN decoupling capacitor and the bootstrap capacitors should be placed next to the IC and make trace connection as short as possible.
8. Ensure that there are sufficient thermal vias directly under the power MOSFETs, connecting to copper on other layers.
9. Via size and number should be enough for a given current path.
10. Route BATP away from switching nodes such as SW1 and SW2.

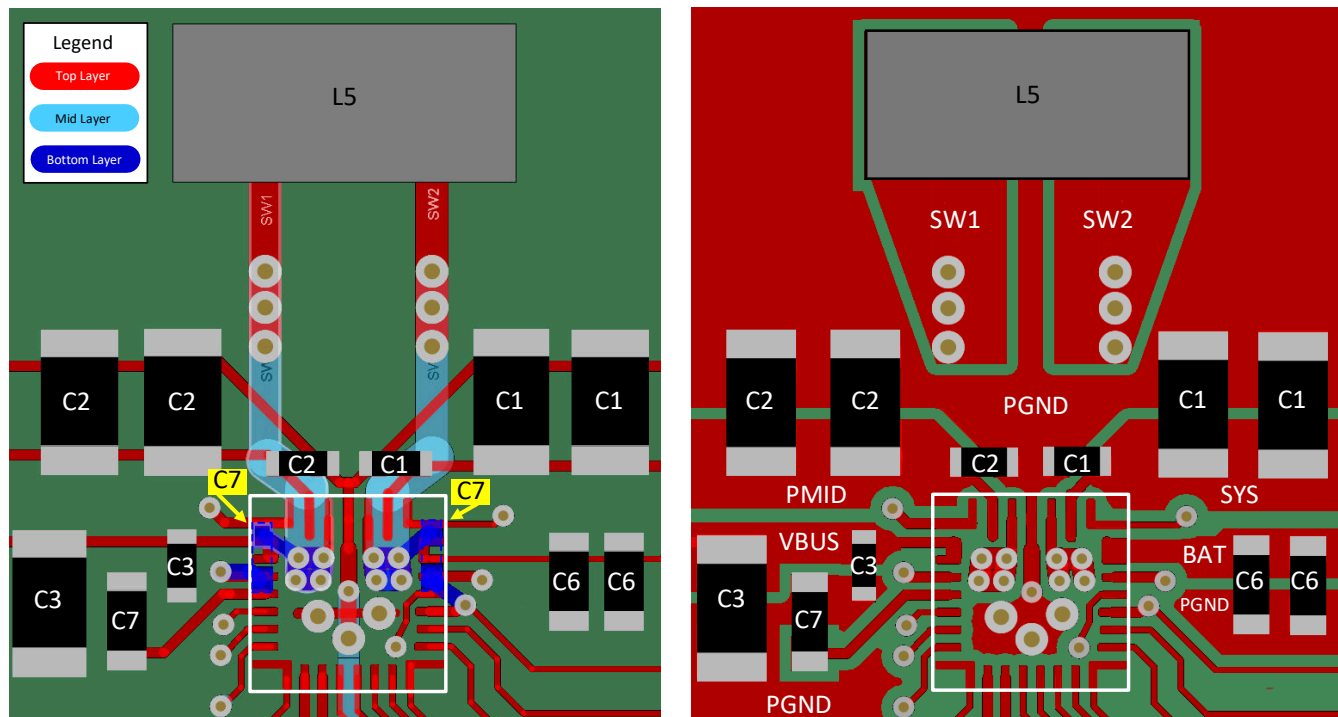
Refer to the EVM design and more information in the [BQ25792EVM](#), [BQ25798EVM](#), and [BQ25798BKUPEVM \(BMS034\) Evaluation Module](#) for the recommended component placement with trace and via locations.



**Figure 12-1. Buck-Boost Converter High Frequency Current Path**



## 12.2 Layout Example



**Figure 12-2. PCB Layout Example (Top Layer Copper Pours Removed on Left, Shown on Right)**

Figure 12-2 shows the recommended placement and routing of external components. The components are labelled with "R," "C" or "L" to indicate resistor, capacitor or inductor and a number that corresponds to the numbered list in Section 12.1. Since the layout guidelines are listed in priority order, this number also provides a priority for component placement.

The placement of C1 and C2 0.1 μF PMID and SYS capacitors is critical for noise filtering. They should be placed on the same layer as the BQ25792, as close to the IC as possible. This will generally require that the traces to connect SW1 and SW2 to the inductor are routed on a different layer.

The SW1 and SW2 pins are routed to vias placed under the IC and then back out on an inner PCB layer. This supports the tightest placement of C1 and C2 capacitors as described above. These vias are also used to route to the C7 BTST1 and BTST2 capacitors on the bottom layer as shown.

## 13 Device and Documentation Support

### 13.1 Device Support

#### 13.1.1 Third-Party Products Disclaimer

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### 13.2 Documentation Support

#### 13.2.1 Related Documentation

For related documentation see the following:

- [BQ25792EVM](#), [BQ25798EVM](#), and [BQ25798BKUPEVM \(BMS034\) Evaluation Module](#)

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins     | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|--------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">BQ25792RQMR</a> | Active        | Production           | VQFN-HR (RQM)   29 | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | BQ25792             |
| BQ25792RQMR.A               | Active        | Production           | VQFN-HR (RQM)   29 | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | BQ25792             |
| BQ25792RQMR.B               | Active        | Production           | VQFN-HR (RQM)   29 | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | BQ25792             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

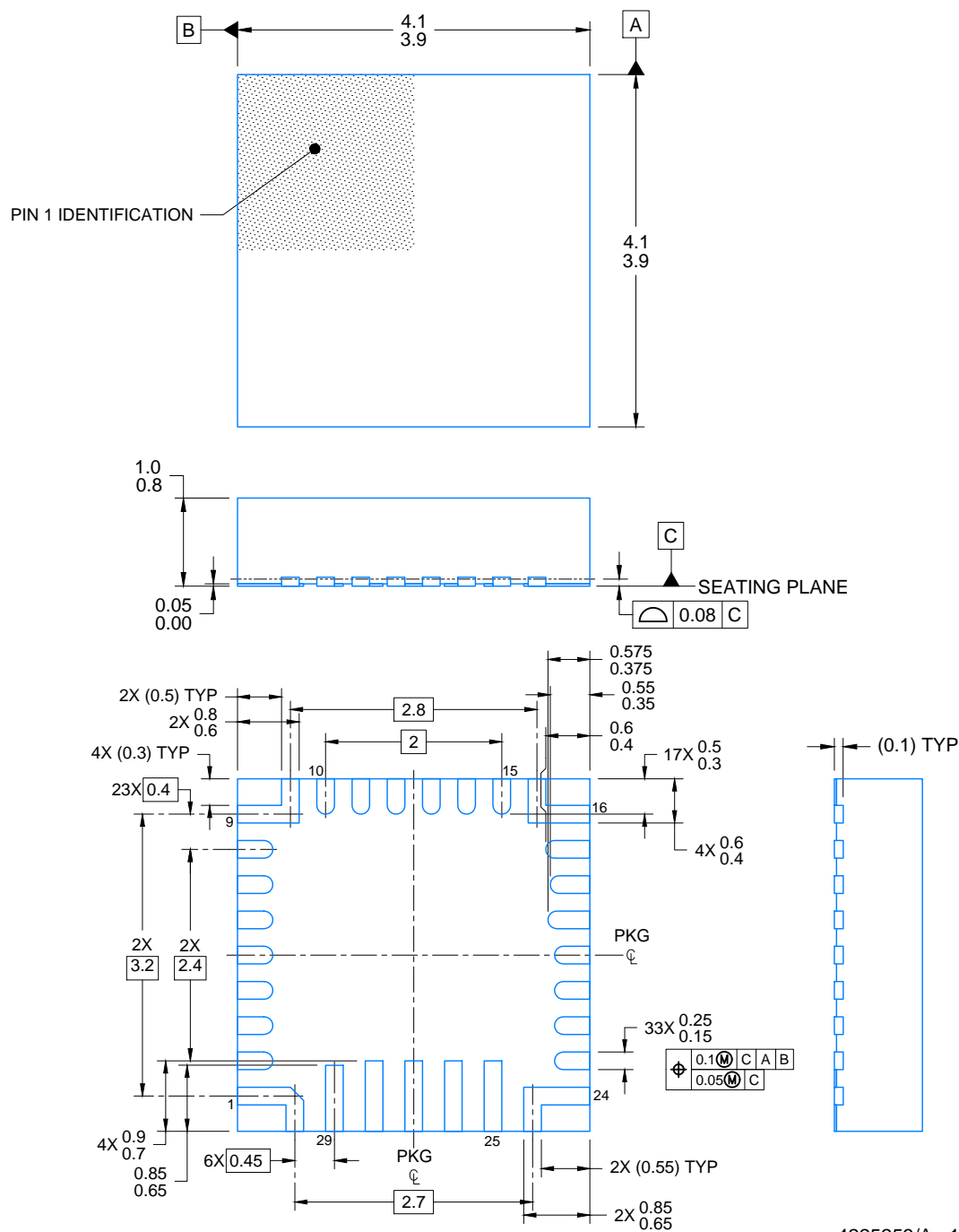
| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ25792RQMR | VQFN-HR      | RQM             | 29   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

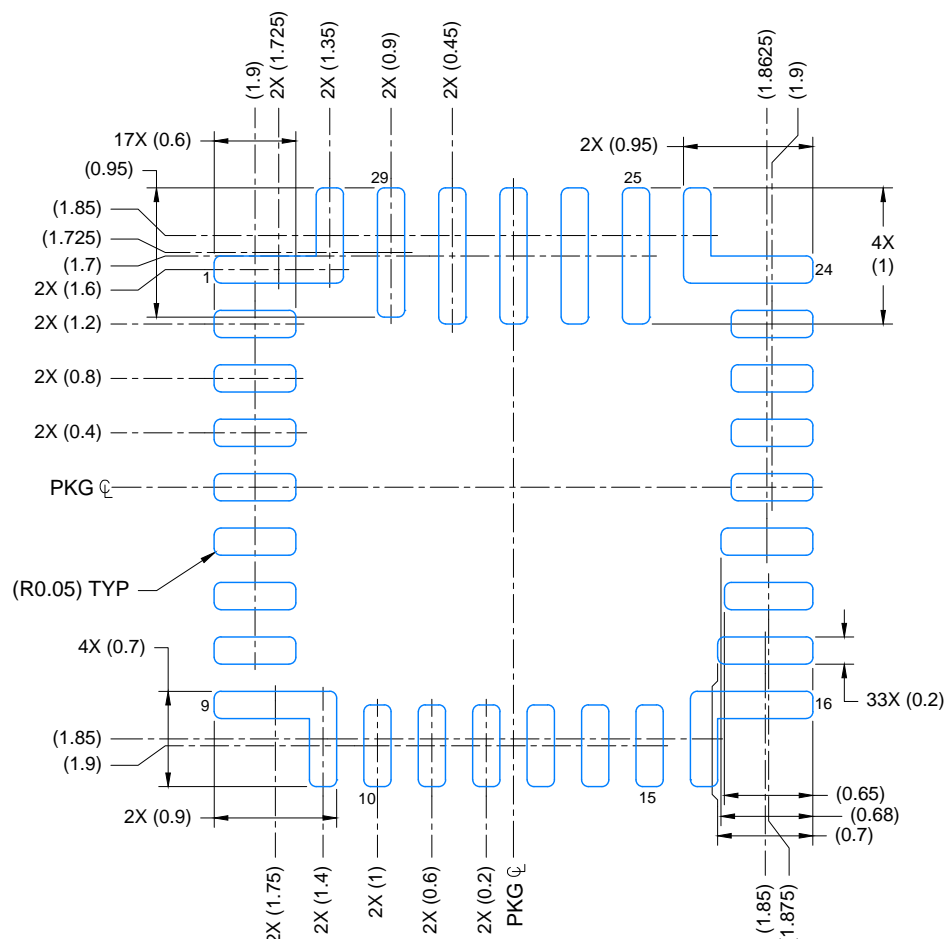
| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ25792RQMR | VQFN-HR      | RQM             | 29   | 3000 | 367.0       | 367.0      | 35.0        |



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NOTES:

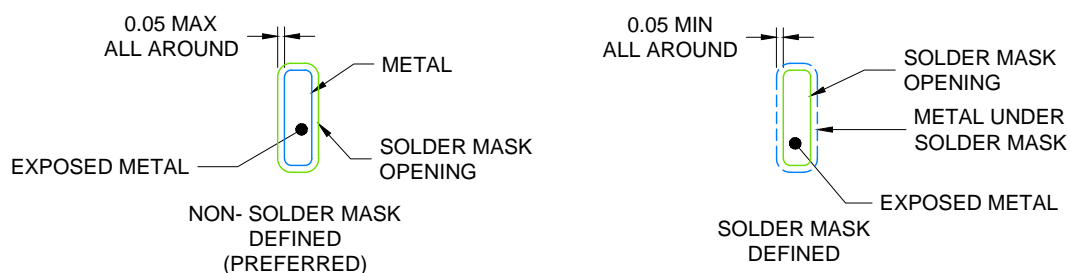
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 18X



## SOLDER MASK DETAILS

NOT TO SCALE

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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



### VQFN-HR - 1 mm max height

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NOTES: (continued)

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