











bq24770, bq24773

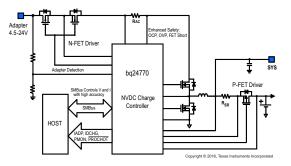
SLUSC03C - AUGUST 2014 - REVISED DECEMBER 2016

bg2477x NVDC Battery Charge Controller With System Power Monitor and Processor Hot Indicator

Features

- Host-controlled NVDC-1 1S-4S Battery Charge Controller with 4.5-24 V Input Range
 - Support SMBus (bg24770) and I2C (bg24773)
 - System Instant-on Operation with no Battery or **Deeply Discharged Battery**
 - Supplement Mode with Synchronous BATFET Control when Adaptor is fully loaded
- Ultra Fast Input Current DPM at 100 µs
- Ultra Low Quiescent Current of 600 µA and High PFM Light Load Efficiency >80% at 20 mA Load to Meet Energy Star and ErP Lot6.
- High Accuracy Power / Current Monitor for CPU Throttling
 - Comprehensive PROCHOT Profile
 - Input and Battery Current Monitor (IADP/IBAT)
 - System Power Monitor (PMON)
- Programmable Input Current Limit, Charge Voltage, Charge Current and Minimum System Voltage Regulation
 - ±0.5% Charge Voltage (16 mV/step)
 - ±2% Input/charge Current (64 mA/step)
 - ±2% 40x Input / 16x Discharge / 20x Charge **Current Monitor**
- Support Battery LEARN Function
- High Integration
 - NMOS ACFET and RBFET Driver
 - PMOS battery FET Gate Driver
 - Internal Loop Compensation
 - Independent Comparator
 - Automatic Trickle Charge to Wake up Gas Gauge
- 600kHz to 1.2MHz Programmable Switching Frequency

Simplified Schematic



2 Applications

- Ultrabook, Notebook, Detachable, and Tablet PC
- Handheld Terminal
- Industrial, Medical, Portable Equipment

3 Description

The bg2477x is high-efficiency, synchronous, NVDC-1 battery charge controllers, offering low component count for space-constraint, multi-chemistry battery charging applications.

The power path management allows the system to be regulated at battery voltage but does not drop below system minimum voltage (programmable). With this feature, the system keeps operating even when the battery is completely discharged or removed. The power path management allows the battery to provide supplement current to the system to keep the input supply from being overloaded.

The bq2477x provides drivers and power path management for N-channel ACFET and reverse blocking FET. The devices provides driver to control NVDC operation of external P-channel battery FET. It also drives high-side and low-side MOSFETs of the switching regulator.

The bq2477x monitors adapter current (IADP), battery charge/discharge current (IBAT) and system power (PMON). The flexibly programmed PROCHOT output goes directly to CPU for throttle back when needed.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24770	WOEN (20 Din)	4.00mm x 4.00mm ²
bq24773	WQFN (28-Pin)	4.00mm x 4.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Light Load Efficiency (V_{IN} = 19.5 V)

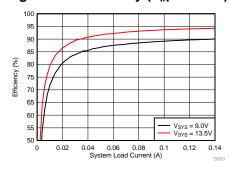




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С	hanges from Revision B (October 2014) to Revision C	Page
•	First public release of the full data sheet	1
С	hanges from Revision A (October 2014) to Revision B	Page
•	Changed text in the Simplified Schematic From; "Hybrid Power Boost Charge" To NVDC Charge"	1
•	Changed Equation 1 From: "V = K _(PMON) " To:" I = K _(PMON) "	17
•	Changed 0x2011H to 0x0211H in the POS STATE column of Table 4	26
•	Changed 0x4854H to 0x4B54H in the POS STATE column of Table 4	26
•	Changed Table 7, column "SMBus 0x3CH" To: "SMBus 0x38H"	29
С	hanges from Original (August 2014) to Revision A	Page
•	Changed the equation in the description of pin 21 From: $V_{(ILIM)} = 20 \times IDPM \times (V_{(ACP)} - V_{(ACN)})$ To: $V_{(ILIM)} = 20 \times IDPM \times R_{AC}$	4

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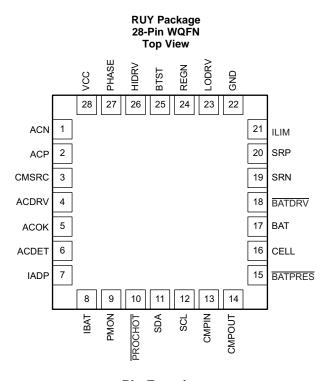
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Device Comparison Table

	bq24770	bq24773
Communication Interface	SMBus	I2C
Communication Address	0x12H (0x00010010)	D4H (0x11010100)
Default Switching Frequency	800kHz	1.2MHz
Default Input Current Limit	3200mA	2944mA
Device ID	0x0114H	0x41H

6 Pin Configuration and Functions



Pin Functions

PIN	NAME	DESCRIPTION
1	ACN	Input current sense resistor negative input. Place an optional 0.1-µF ceramic capacitor from ACN to GND for common-mode filtering. Place a 0.1-µF ceramic capacitor from ACN to ACP to provide differential mode filtering.
2	ACP	Input current sense resistor positive input. Place a 1-µF and 0.1-µF ceramic capacitor from ACP to GND for common-mode filtering. Place a 0.1-µF ceramic capacitor from ACN to ACP to provide differential-mode filtering.
3	CMSRC	ACDRV charge pump source input. Place a $4 \text{ k}\Omega$ resistor from CMSRC to the common source of ACFET (Q1) and RBFET (Q2) limits the in-rush current on CMSRC pin. When CMSRC is grounded, ACDRV pin becomes logic output internally puled up to REGN. ACDRV HIGH indicates to external driver that ACFET/RBFET can be turned on. It directly drives CMOS logic.
4	Charge pump output to drive both adapter input n-channel MOSFET (ACFET) and reverse blocking n-MOSFET (RBFET). ACDRV voltage is 6 V above CMSRC to turn on ACFET/RBFET when ACOK goe Place a 4 kΩ resistor from ACDRV to the gate of ACFET and RBFET limits the in-rush current on ACI When CMSRC is grounded, ACDRV pin becomes logic output internally pulled up to REGN. ACDRV indicates that ACFET/RBFET can be turned on. It directly drives CMOS logic.	
5	АСОК	Active HIGH AC adapter detection open drain output. It is pulled HIGH to external pull-up supply rail by external pull-up resistor when a valid adapter is present (ACDET above 2.4 V, VCC above UVLO but below ACOV and VCC above BAT). If any of the above conditions is not valid, ACOK is pulled LOW by internal MOSFET. Connect a 10- $k\Omega$ pull up resistor from ACOK to the pull-up supply rail.

Product Folder Links: bq24770 bq24773



Pin Functions (continued)

ACDET pin to GND pin. When ACDET pin is above 0.6 V and VCC is above UVLO, RESN LDO is present, ACOK comparator, and i current monitor buffer (IADP) are all active. Independent comparator, IBAT buffer, PMON buffer and PROCF can be enabled with SMBus/IZC. When ACDET pin is above 2.4 V, and VCC is above BAT, but below ACOV, ACOK goes HIGH. ACFET/RBI furms on. Buffered adapter current output. V _[ADDP] = 40 or 80 × (V _{ACDP}) = V _{ACND}) The ratio of 40x and 80x is selectable with SMBus/IZC. Discent 100pF or less ceramic decoupling capacitor for IADP pin to GND. This pin can be floating if it is not in use. IADP output voltage is clamped below 3.3 v. Buffered battery current selected by SMBus/IZC. V _{Chang} = 20 × (V _{Span} - V _{Span}) for charge current, or V _{span} for charge below 3.3 v. Buffered battery current selected by SMBus/IZC. White is a clamped below 3.3 v. Current mode system power monitor. The output voltage is proportional to the total power from the adapter below 3.3 v. Current mode system power monitor. The output voltage is proportional to the total power from the adapter below 3.3 v. The maximum cap on PMON is 100 pF. Active low open drain output of "processor hor" indicator. It monitors adapter input current, battery discharge current, and system voltage. After any event in the PROCHOT profile is triggered, a minimum 10-ms pulse is asserted. SDA SMBus/IZC open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10 pull-up resistor according to SMBus/IZC specifications. Input of independent comparator, Internal reference, output polarity and deglitch time is selectable by SMBus/IZC specifications. Input of independent comparator, Internal reference, output polarity and deglitch time is selectable by SMBus/IZC when BATFERS is HIGH. BATFERS bit of several propers from LOW to HIGH, the device exists LEARN mode, and disable charge. REG 0x16) goes back to default. Hore to ace anable DIPM and charge through SMBus/IZC when BATFERS is HIGH. BATFERS bit on a	PIN	NAME	DESCRIPTION
Men ACDET pin is above 0.6 v and VCC is above UVLO. REON LDO is present. ACOK comparator, and an ACDET pin is above 2.6 v. and VCC is above UVLO. REON LDO is present. ACOK comparator, and and PROCF can be enabled with SMBus/I2C. When ACDET pin is above 2.4 v. and VCC is above BAT, but below ACOV, ACOK goes HiGH. ACFET/RBI furns on. Buffered adapter current output. V _(MDP) = 40 or 80 × (V _(ACP) – V _(ACN)) The ratio of 40x and 80x is selectable with SMBus/I2C. Place 100pF or less ceramic decoupling capacitor for IADP pin to GND. This pin can be floating if it is not in use. IADP output voltage is clamped below 3.3 v. Buffered battery current selected by SMBus/I2C. V _(BAP) = 20 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current, or V _(BAP) = 16 × (V _(SRP) – V _(SRP)) for charge current and continued to the continued current and continued to the continued current and current and current and current and current and selectable many selectable			Adapter detection input. Program adapter valid input threshold by connecting a resistor divider from adapter input to
turns on. Buffered adapter current output. V _(MDP) = 40 or 80 × (V _(ACP) – V _(ACN)) The ratio of 40x and 80x is selectable with SMBus/I2C. Place 100pF or less ceramic decoupling capacitor for ADP pin to 6ND. This pin can be floating if it is not in use. IADP output voltage is clamped below 3.7. Buffered battery current selected by SMBus/I2C. V _{Place} = 20 x (V _{SRP)} – V _(SRP) of refer battery current selected by SMBus/I2C. Place 100pF or less or decoupling capacitor from IBAT pin to 6ND. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V. Current mode system power monitor. The output voltage is proportional to the total power from the adapter battery. The gain is selectable through SMBus/I2C. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V. The maximum cap on PMON is 100 pF. Active low open drain output of "processor hor" indicator. It monitors adapter input current, battery discharge current, and system voltage. After any event in the PROCHOT profile is triggered, a minimum 10-ms pulse it asserted. SCL SMBus/I2C open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10 pill-up resistor according to SMBus/I2C specifications. Input of independent comparator. Internal reference, output polarity and deglitch time is selectable by SMBus/I2C profile in the profile in t	6	ACDET	When ACDET pin is above 0.6 V and VCC is above UVLO, REGN LDO is present, ACOK comparator, and input current monitor buffer (IADP) are all active. Independent comparator, IBAT buffer, PMON buffer and PROCHOT can be enabled with SMBus/I2C.
IADP			
BAT	7	IADP	The ratio of 40x and 80x is selectable with SMBus/I2C. Place 100pF or less ceramic decoupling capacitor from
battery. The gain is selectable through SMBus/I2C. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V. The maximum cap on PMON is 100 pF. Active low open drain output of "processor hot" indicator. It monitors adapter input current, battery discharge current, and system voltage. After any event in the PROCHOT profile is triggered, a minimum 10-ms pulse is asserted. SDA SMBus/I2C open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10 pull-up resistor according to SMBus/I2C specifications. SCL SMBus/I2C obeck input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pull-resistor according to SMBus/I2C specifications. SCL SMBus/I2C dock input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pull-resistor according to SMBus/I2C. Specifications. SCL SMBus/I2C dock input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pull-resistor according to SMBus/I2C. CMPIN United independent comparator. Internal reference, output polarity and deglitch time is selectable by SMBus/I2C. CMPIN United independent comparator. Internal reference, output polarity and deglitch time are selectable by SMBus/I2C. Active low battery present input signal. LOW indicates battery present, HIGH indicates battery absent. When BATPRES pin goes from LOW to HIGH, the device exits LEARN mode, and disable charge. REG 0x15() val goes back to default. Host can enable IDPM and charge through SMBus/I2C. CELL pin also sets SYSOVP threshold. GND for 5-cell, and HIGH for 3- or 4-cell. CELL pin is biased from 18 BAT pin to accurately sense the battery pack voltage. Place a 0.1-μF capacitor from BAT to GND close to the filter high-frequency noise. P-channel battery FET (BATFET) gate driver output. It is shorted to SRN to turn off the BATFET. It goes bell SRN to turn on BATFET. BATFET is in linear mode to regulate SYS at minimum system voltage when batter depleted. BATFET is fully on	8	IBAT	Buffered battery current selected by SMBus/I2C. $V_{(IBAT)} = 20 \times (V_{(SRP)} - V_{(SRN)})$ for charge current, or $V_{(IBAT)} = 8$ or $16 \times (V_{(SRN)} - V_{(SRN)})$ for discharge current, with ratio selectable through SMBus/I2C. Place 100pF or less ceramic decoupling capacitor from IBAT pin to GND. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V.
turrent, and system voltage. After any event in the PROCHOT profile is triggered, a minimum 10-ms pulse is asserted. SDA SMBus/I2C open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10 pull-up resistor according to SMBus/I2C specifications. SCL SMBus/I2C scie, input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pull-up resistor according to SMBus/I2C specifications. Input of independent comparator. Internal reference, output polarity and deglitch time is selectable by SMBus/I2C specifications. Input of independent comparator. Internal reference, output polarity and deglitch time is selectable by SMBus/I2C (specifications). Input of independent comparator. Internal reference, output polarity and deglitch time is selectable by SMBus/I2C (specifications). Input of independent comparator. Place 10kΩ pull-up resistor from CMPOUT to program hysteresis. With LOW (0x38)(e)=0), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN ground. CMPOUT Depr-drain output of independent comparator. Place 10kΩ pull-up resistor from CMPOUT to pull-up supply internal reference, output polarity and deglitch time are selectable by SMBus/I2C. Active low battery present input signal. LOW indicates battery present, HIGH indicates battery absent. When BATPRES in goes back to default. Host can enable IDPM and charge through SMBus/I2C when BATPRES is HIGH. BATPRES BATPRES by goes from LOW to HIGH, the device exist LEARN mode, and disable charge. REG 0x15() values before host writes to MaxChargeVoltage(), MaxChargeVoltage() follows the CELL pin setting. CELL pin also sets SYSOVP brreshold. GND for 1-cell, Float for 2-cell, and HIGH for 18.5 V. When REG 0x15() above 15V, SYSOVP is disabled. Battery-voltage remote sense. Directly connect a Kelvin sense trace from the battery-pack positive terminal the BATPET is an BATPET is in linear mode to regulate SYS at minimum system voltage when batter depleted. BATFET is patte	9	PMON	Current mode system power monitor. The output voltage is proportional to the total power from the adapter and battery. The gain is selectable through SMBus/I2C. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V. The maximum cap on PMON is 100 pF.
pull-up resistor according to SMBus/I2C specifications. SMBus/I2C clock input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pull-resistor according to SMBus/I2C specifications. Input of independent comparator. Internal reference, output polarity and deglitch time is selectable by SMBus/I2C Mow (0x3B[6]=1), place a resistor between CMPIN and CMPOUT to program hysteresis. With LOW (0x3B[6]=0), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN ground. CMPOUT Open-drain output of independent comparator. Place 10kΩ pull-up resistor from CMPOUT to pull-up supply internal reference, output polarity and deglitch time are selectable by SMBus/I2C. Active low battery present input signal. LOW indicates battery present, HIGH indicates battery absent. When BATPRES pin goes from LOW to HIGH, the device exist LEARN mode, and disable charge. REG 0x15(1) val goes back to default. Host can enable IDPM and charge through SMBus/I2C when BATPRES is HIGH. Battery cell selection pin. GND for 1-cell, Float for 2-cell, and HIGH for 3- or 4-cell. CELL pin is biased from IDB before host writes to MaxChargeVoltage(), MaxChargeVotage() follows the CELL pin setting. CELL pin also sets SYSOVP threshold. GND for 5 V. Float for 12 V and HIGH for 18.5 V. When REG 0x15() above 15V, SYSOVP is disabled. Battery-voltage remote sense. Directly connect a Kelvin sense trace from the battery-pack positive terminal tender by the pack positive present of the pack voltage. Place a 0.1-μF capacitor from BAT to GND close to the filter high-frequency noise. P-channel battery FET (BATFET) gate driver output. It is shorted to SRN to turn off the BATFET. It goes bels SRN to turn on BATFET is in linear mode to regulate SYS at minimum system voltage when battery back positive node BAT pin. Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN p a 0.1 μF ceramic capacitor to GND for common-mode filtering. Charge current sense r	10	PROCHOT	Active low open drain output of "processor hot" indicator. It monitors adapter input current, battery discharge current, and system voltage. After any event in the PROCHOT profile is triggered, a minimum 10-ms pulse is asserted.
resistor according to SMBus/I2C specifications. Input of independent comparator. Internal reference, output polarity and deglitich time is selectable by SMBus With polarity HIGH (0x3B[6]=1), place a resistor between CMPIN and CMPOUT to program hysteresis. With LOW (0x3B[6]=0), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN ground. CMPOUT Open-drain output of independent comparator. Place 10kΩ pull-up resistor from CMPOUT to pull-up supply related internal reference, output polarity and deglitch time are selectable by SMBus/I2C. Active low battery present input signal. LOW indicates battery present, HIGH indicates battery absent. When BATPRES pin goes from LOW to HIGH, the device exits LEARN mode, and disable charge. REG 0x15() val goes back to default. Host can enable IDPM and charge through SMBus/I2C when BATPRES is HIGH. Battery cell selection pin. GND for 1-cell, Float for 2-cell, and HIGH for 3- or 4-cell. CELL pin is biased from I Before host writes to MaxChargeVoltage(), MaxChargeVotage() follows the CELL pin setting. CELL pin also sets SYSOVP threshold. GND for 5 V, Float for 12 V and HIGH for 18.5 V. When REG 0x15() above 15V, SYSOVP is disabled. Battery-voltage remote sense. Directly connect a Kelvin sense trace from the battery-pack positive terminal the BAT pin to accurately sense the battery pack voltage. Place a 0.1-µF capacitor from BAT to GND close to the filter high-frequency noise. P-channel battery FET (BATFET) gate driver output. It is shorted to SRN to turn off the BATFET. It goes bels SRN to turn on BATFET is fully on during fast charge and supplement mode. Connect the source of the BATFET to charge current sensing node SRN pin, and the drain of the BATFET to charge current sensing node SRN pin, and the drain of the BATFET to charge current sensing node SRN pin, and the drain of the BATFET to charge current sensing resistor divider from supply rail to ILIM pin to pin. The ILIM voltage is calculated as: V _(ILIM) = 20 × IDPM × R _{AC} , in whic	11	SDA	SMBus/I2C open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10-k Ω pull-up resistor according to SMBus/I2C specifications.
CMPIN With polarity HIGH (0x3B[6]=1), place a resistor between CMPIN and CMPOUT to program hysteresis. With LOW (0x3B[6]=0), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN ground. CMPOUT Open-drain output of independent comparator. Place 10kΩ pull-up resistor from CMPOUT to pull-up supply internal reference, output polarity and deglitch time are selectable by SMBus/I2C. Active low battery present input signal. LOW indicates battery present, HIGH indicates battery absent. When BATPRES pin goes from LOW to HIGH, the device exits LEARN mode, and disable charge. REG 0x150 val goes back to default. Host can enable IDPM and charge through SMBus/I2C when BATPRES is HIGH. Battery cell selection pin. GND for 1-cell, Float for 2-cell, and HIGH for 3- or 4-cell. CELL pin sib biased from 1 Before host writes to MaxChargeVotlage(), MaxChargeVotage() follows the CELL pin setting. CELL pin also sets SYSOVP threshold. GND for 5 V, Float for 12 V and HIGH for 18.5 V. When REG 0x15() above 15V, SYSOVP is disabled. Battery-voltage remote sense. Directly connect a Kelvin sense trace from the battery-pack positive terminal to BAT pin to accurately sense the battery pack voltage. Place a 0.1-μF capacitor from BAT to GND close to the filter high-frequency noise. P-channel battery FET (BATFET) gate driver output. It is shorted to SRN to turn off the BATFET. It goes bell SRN to turn on BATFET. BATFET is in linear mode to regulate SYS at minimum system voltage when batter depleted. BATFET is fully on during fast charge and supplement mode. Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN p a 0.1μF ceramic capacitor for GND for common-mode filtering. Charge current sense resistor positive input. Connect a 0.1-μF ceramic capacitor from SRF SRN to provide differential mode filtering. Charge current sense resistor positive input. Connecting a resistor divider from supply rail to ILIM pin to pin. The ILIM voltage	12	SCL	SMBus/I2C clock input. Connect to clock line from the host controller or smart battery. Connect a 10-k Ω pull-up resistor according to SMBus/I2C specifications.
Internal reference, output polarity and deglitch time are selectable by SMBus/I2C. Active low battery present input signal. LOW indicates battery present, HIGH indicates battery absent. When BATPRES pin goes from LOW to HIGH, the device exits LEARN mode, and disable charge. REG 0x15() val goes back to default. Host can enable IDPM and charge through SMBus/I2C when BATPRES is HIGH. Battery cell selection pin. GND for 1-cell, Float for 2-cell, and HIGH for 3- or 4-cell. CELL pin is biased from Before host writes to MaxChargeVoltage(), MaxChargeVotage() follows the CELL pin setting. CELL pin also sets SYSOVP threshold. GND for 5 V, Float for 12 V and HIGH for 18.5 V. When REG 0x15() above 15V, SYSOVP is disabled. BAT BAT BAT pin to accurately sense the battery pack voltage. Place a 0.1-μF capacitor from BAT to GND close to th filter high-frequency noise. P-channel battery FET (BATFET) gate driver output. It is shorted to SRN to turn off the BATFET. It goes bels SRN to turn on BATFET. BATFET is in linear mode to regulate SYS at minimum system voltage when batter depleted. BATFET is fully on during fast charge and supplement mode. Connect the source of the BATFET to charge current sensing node SRN pin, and the drain of the BATFET to battery pack positive node BAT pin. Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN p a 0.1μF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-μF ceramic capacitor from SRF SRN to provide differential mode filtering. Input current limit input. Program ILIM voltage by connecting a resistor divider from supply rail to ILIM pin to pin. The ILIM voltage and DAC limit voltage sets input current regulation limit. Host can ignore the IDPM from ILIM pin by setting 0x38[7]=0. IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through power pad underneath IC.	13	CMPIN	Input of independent comparator. Internal reference, output polarity and deglitch time is selectable by SMBus/I2C. With polarity HIGH (0x3B[6]=1), place a resistor between CMPIN and CMPOUT to program hysteresis. With polarity LOW (0x3B[6]=0), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN to ground.
BATPRES pin goes from LOW to HIGH, the device exits LEARN mode, and disable charge. REG 0x15() val goes back to default. Host can enable IDPM and charge through SMBus/I2C when BATPRES is HIGH. Battery cell selection pin. GND for 1-cell, Float for 2-cell, and HIGH for 3- or 4-cell. CELL pin is biased from I Before host writes to MaxChargeVoltage(), MaxChargeVotage() follows the CELL pin setting. CELL pin also sets SYSOVP threshold. GND for 5 V, Float for 12 V and HIGH for 18.5 V. When REG 0x15() above 15V, SYSOVP is disabled. Battery-voltage remote sense. Directly connect a Kelvin sense trace from the battery-pack positive terminal t BAT pin to accurately sense the battery pack voltage. Place a 0.1-μF capacitor from BAT to GND close to th filter high-frequency noise. P-channel battery FET (BATFET) gate driver output. It is shorted to SRN to turn off the BATFET. It goes bell SRN to turn on BATFET. BATFET is in linear mode to regulate SYS at minimum system voltage when batter depleted. BATFET is fully on during fast charge and supplement mode. Connect the source of the BATFET to charge current sensing node SRN pin, and the drain of the BATFET to battery pack positive node BAT pin. Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN p a 0.1μF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-μF ceramic capacitor from SRF SRN to provide differential mode filtering. Input current limit input. Program ILIM voltage by connecting a resistor divider from supply rail to ILIM pin to pin. The ILIM voltage is calculated as: V _(ILIM) = 20 × IDPM × R _{AC} , in which IDPM is the target regulation curr The lower of ILIM voltage and DAC limit voltage sets input current regulation limit. Host can ignore the IDPM from ILIM pin by setting 0x38[7]=0. IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through power pad underneath IC.	14	CMPOUT	Open-drain output of independent comparator. Place $10k\Omega$ pull-up resistor from CMPOUT to pull-up supply rail. Internal reference, output polarity and deglitch time are selectable by SMBus/I2C.
Before host writes to MaxChargeVoltage(), MaxChargeVotage() follows the CELL pin setting. CELL pin also sets SYSOVP threshold. GND for 5 V, Float for 12 V and HIGH for 18.5 V. When REG 0x15() above 15V, SYSOVP is disabled. Battery-voltage remote sense. Directly connect a Kelvin sense trace from the battery-pack positive terminal to BAT pin to accurately sense the battery pack voltage. Place a 0.1-μF capacitor from BAT to GND close to th filter high-frequency noise. P-channel battery FET (BATFET) gate driver output. It is shorted to SRN to turn off the BATFET. It goes beles SRN to turn on BATFET. BATFET is in linear mode to regulate SYS at minimum system voltage when batter depleted. BATFET is fully on during fast charge and supplement mode. Connect the source of the BATFET to charge current sensing node SRN pin, and the drain of the BATFET to battery pack positive node BAT pin. Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN p a 0.1μF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-μF ceramic capacitor from SRF SRN to provide differential mode filtering. Charge current sense resistor positive input. Connect a 0.1-μF ceramic capacitor from SRF officerential mode filtering. Input current limit input. Program ILIM voltage by connecting a resistor divider from supply rail to ILIM pin to pin. The ILIM voltage is calculated as: V _(ILIM) = 20 × IDPM × R _{AC} , in which IDPM is the target regulation current lenower of ILIM voltage and DAC limit voltage sets input current regulation limit. Host can ignore the IDPM from ILIM pin by setting 0x38[7]=0. CRND IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through power pad underneath IC.	15	BATPRES	Active low battery present input signal. LOW indicates battery present, HIGH indicates battery absent. When BATPRES pin goes from LOW to HIGH, the device exits LEARN mode, and disable charge. REG 0x15() value goes back to default. Host can enable IDPM and charge through SMBus/I2C when BATPRES is HIGH.
BAT pin to accurately sense the battery pack voltage. Place a 0.1-μF capacitor from BAT to GND close to th filter high-frequency noise. P-channel battery FET (BATFET) gate driver output. It is shorted to SRN to turn off the BATFET. It goes belt SRN to turn on BATFET. BATFET is in linear mode to regulate SYS at minimum system voltage when batter depleted. BATFET is fully on during fast charge and supplement mode. Connect the source of the BATFET to charge current sensing node SRN pin, and the drain of the BATFET to battery pack positive node BAT pin. Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN p a 0.1μF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-μF ceramic capacitor from SRF SRN to provide differential mode filtering. Charge current sense resistor positive input. Connect a 0.1-μF ceramic capacitor from SRP to SRN to provide differential mode filtering. Input current limit input. Program ILIM voltage by connecting a resistor divider from supply rail to ILIM pin to pin. The ILIM voltage is calculated as: V _(ILIM) = 20 × IDPM × R _{AC} , in which IDPM is the target regulation current regulation limit. Host can ignore the IDPM from ILIM pin by setting 0x38[7]=0. IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through power pad underneath IC.	16	CELL	CELL pin also sets SYSOVP threshold. GND for 5 V, Float for 12 V and HIGH for 18.5 V. When REG 0x15() is
SRN to turn on BATFET. BATFET is in linear mode to regulate SYS at minimum system voltage when batter depleted. BATFET is fully on during fast charge and supplement mode. Connect the source of the BATFET to charge current sensing node SRN pin, and the drain of the BATFET to battery pack positive node BAT pin. Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN p a 0.1μF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-μF ceramic capacitor from SRF SRN to provide differential mode filtering. Charge current sense resistor positive input. Connect a 0.1-μF ceramic capacitor from SRP to SRN to provide differential mode filtering. Input current limit input. Program ILIM voltage by connecting a resistor divider from supply rail to ILIM pin to pin. The ILIM voltage is calculated as: V _(ILIM) = 20 × IDPM × R _{AC} , in which IDPM is the target regulation current limit input. Program ILIM voltage sets input current regulation limit. Host can ignore the IDPM from ILIM pin by setting 0x38[7]=0. IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through power pad underneath IC.	17	BAT	Battery-voltage remote sense. Directly connect a Kelvin sense trace from the battery-pack positive terminal to the BAT pin to accurately sense the battery pack voltage. Place a 0.1 - μ F capacitor from BAT to GND close to the IC to filter high-frequency noise.
19 SRN a 0.1μF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-μF ceramic capacitor from SRF SRN to provide differential mode filtering. 20 SRP Charge current sense resistor positive input. Connect a 0.1-μF ceramic capacitor from SRP to SRN to provide differential mode filtering. 21 ILIM ILIM Voltage Input current limit input. Program ILIM voltage by connecting a resistor divider from supply rail to ILIM pin to pin. The ILIM voltage is calculated as: V _(ILIM) = 20 × IDPM × R _{AC} , in which IDPM is the target regulation current The lower of ILIM voltage and DAC limit voltage sets input current regulation limit. Host can ignore the IDPM from ILIM pin by setting 0x38[7]=0. 22 GND IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through power pad underneath IC.	18	BATDRV	Connect the source of the BATFET to charge current sensing node SRN pin, and the drain of the BATFET to the
differential mode filtering. Input current limit input. Program ILIM voltage by connecting a resistor divider from supply rail to ILIM pin to pin. The ILIM voltage is calculated as: V _(ILIM) = 20 × IDPM × R _{AC} , in which IDPM is the target regulation curr The lower of ILIM voltage and DAC limit voltage sets input current regulation limit. Host can ignore the IDPM from ILIM pin by setting 0x38[7]=0. IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through power pad underneath IC.	19	SRN	Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN pin with a 0.1µF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-µF ceramic capacitor from SRP to SRN to provide differential mode filtering.
ILIM pin. The ILIM voltage is calculated as: V _(ILIM) = 20 x IDPM x R _{AC} , in which IDPM is the target regulation curr. The lower of ILIM voltage and DAC limit voltage sets input current regulation limit. Host can ignore the IDPM from ILIM pin by setting 0x38[7]=0. IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through power pad underneath IC.	20	SRP	Charge current sense resistor positive input. Connect a 0.1-µF ceramic capacitor from SRP to SRN to provide differential mode filtering.
power pad underneath IC.	21	ILIM	Input current limit input. Program ILIM voltage by connecting a resistor divider from supply rail to ILIM pin to GND pin. The ILIM voltage is calculated as: $V_{(ILIM)} = 20 \times IDPM \times R_{AC}$, in which IDPM is the target regulation current. The lower of ILIM voltage and DAC limit voltage sets input current regulation limit. Host can ignore the IDPM setting from ILIM pin by setting $0x38[7]=0$.
23 LODRV Low side power MOSFET driver output. Connect to low side n-channel MOSFET gate	22	GND	IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through the power pad underneath IC.
	23	LODRV	Low side power MOSFET driver output. Connect to low side n-channel MOSFET gate.
24 REGN 5.4V linear regulator output supplied from VCC. The LDO is active when ACDET above 0.6V, VCC above U'Connect a 1µF ceramic capacitor from REGN to power ground.	24	REGN	5.4V linear regulator output supplied from VCC. The LDO is active when ACDET above 0.6V, VCC above UVLO. Connect a 1µF ceramic capacitor from REGN to power ground.

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Pin Functions (continued)

PIN	NAME	DESCRIPTION
25	BTST	High side power MOSFET driver power supply. Connect a 0.047-µF capacitor from BTST to PHASE. The bootstrap diode between REGN and BTST is integrated.
26	HIDRV	High side power MOSFET driver output. Connect to the high side n-channel MOSFET gate.
27	PHASE	High side power MOSFET driver source. Connect to the source of the high side n-channel MOSFET.
28	Input supply from adapter or battery. Place Schottky diode-OR from adapter/battery. After the Schottky diode, 10-Ω resistor and 1-μF capacitor to ground as low pass filter to limit inrush current.	
	Thermal Pad	Exposed pad beneath the IC. Analog ground and power ground star-connected only at the thermal pad plane. Always solder thermal pad to the board, and have vias on the thermal pad plane connecting to analog ground and power ground planes. It also serves as a thermal pad to dissipate the heat.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
	SRN, SRP, ACN, ACP, CMSRC, VCC, BAT, BATDRV	-0.3	30	V
	PHASE	-2.0	30	V
	BTST, HIDRV, ACDRV	-0.3	36	V
	LODRV (2% duty cycle)	-4.0	7	V
Voltage range	HIDRV (2% duty cycle)	-4.0	36	V
	PHASE (2% duty cycle)	-4.0	30	V
	ACDET, SDA, SCL, LODRV, REGN, IADP, IBAT, PMON, BATPRES, ACOK, CELL, CMPIN, CMPOUT, ILIM	-0.3	7	V
	PROCHOT	-0.3	5.5	V
Differential valters	BTST-PHASE, HIDRV-PHASE	-0.3	7	V
Differential voltage	SRP-SRN, ACP-ACN	-0.5	0.5	V
Junction temperature	range, T _J	–40 155 °C		°C
Storage temperature	range, T _{stg}	– 55	155	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			MIN	MAX	UNIT
V _(ESD) Electrostatic discharge	Floatroototio	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	500	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

⁽²⁾ All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	ACN, ACP, CMSRC, VCC	0	24	V
	BATDRV, BAT, SRN, SRP	0	19.2	V
	PHASE	-2	24	V
Voltage range	BTST, HIDRV, ACDRV	0	30	V
	ACDET, SDA, SCL, LODRV, REGN, IADP, IBAT, PMON, BATPRES, ACOK, CELL, CMPIN, CMPOUT, ILIM	0	6.5	V
	PROCHOT	-0.3	5.3	V
Differential colleges	BTST-PHASE, HIDRV-PHASE	0	6.5	V
Differential voltage	SRP-SRN, ACP-ACN	-0.35	0.35	V
Junction temperature	range, T _J	-20	125	°C
Operating free-air ter	nperature range, T _A	-40	-20 125	

7.4 Thermal Information

		bq2477x	
	THERMAL METRIC ⁽¹⁾	RUY (WQFN)	UNIT
		28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.5	°C/W
ΨЈΤ	Junction-to-top characterization parameter	0.3	°C/W
ΨЈВ	Junction-to-board characterization parameter	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

 $4.5\text{V} \le \text{V}_{(\text{VCC})} \le 24\text{V}, -20^{\circ}\text{C} \le \text{T}_{\text{J}} \le 125^{\circ}\text{C}, \text{ typical values are at T}_{\text{A}} = 25^{\circ}\text{C}, \text{ with respect to GND (unless otherwise noted)}$

	PARAMETER	TEST CONDITION	MIN TY	P MAX	UNIT
OPERATING CON	DITIONS				
V _(IN_OP)	Input voltage operating range		4.5	24	V
MINIMUM SYSTEM	VI VOLTAGE REGULATION (0x3E REGIS	TER)			
V _(SYSMIN_RNG)	System voltage regulation range		1.024	19.2	V
		Minovotom)/oltogo/\ 0\cdot240011	9.21	6	V
		MinsystemVoltage()=0x2400H	-2%	2%	
\ <u>\</u>	Minimum system voltage regulation	Minovetory/altore/ 0v490011	6.14	4	V
V _(MINSYS_REG_ACC)	accuracy	MinsystemVoltage()=0x1800H	-3%	3%	
		MinsystemVoltage()=0x0E00H	3.58	4	V
			-3%	3%	
MAXIMUM SYSTE	M VOLTAGE REGULATION (0x15 REGIS	STER, CHARGE DISABLE)	·		
V _(SYSMAX_RNG)	System voltage regulation range		1.024	19.2	V
		Marrich and Vallage (V. Organou I.	13.50	4	V
		MaxChargVoltage() = 0x34C0H	-2%	2%	
.,	Maximum system voltage regulation	MaxChargVoltage() = 0x2330H	9.00	8	V
V _(MAXSYS_REG_ACC)	accuracy		-3%	3%	
		MaxChargVoltage() = 0x1130H	4	4	V
			-3%	3%	

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 $4.5\text{V} \le \text{V}_{(VCC)} \le 24\text{V}, -20^{\circ}\text{C} \le \text{T}_{J} \le 125^{\circ}\text{C}, \text{ typical values are at T}_{A} = 25^{\circ}\text{C}, \text{ with respect to GND (unless otherwise noted)}$

	PARAMETER	lues are at T _A = 25°C, with respect to GNI	MIN	TYP	MAX	UNIT
CHARGE VOLTAG	E REGULATION (0x15 REGISTER, CHARG				III OC	01111
		L LNADLL)	1.024		19.2	V
V _(BAT_RGN)	Battery voltage range		1.024	40.0	19.2	V
		ChargeVoltage() = 0x41A0H	0.50/	16.8	0.50/	V
			-0.5%	40.500	0.5%	
		ChargeVoltage() = 0x3130H		12.592		V
V _(BAT REG ACC)	Battery voltage regulation accuranc (0°C -		-0.5%		0.5%	
(BNI_NEO_NOO)	85°C)	ChargeVoltage() = 0x20D0H		8.4		V
		3 1 3 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	-0.6%		0.6%	
		ChargeVoltage() = 0x1070H		4.208		V
		Charge voltage() = exterent	-1%		1%	
CHARGE CURREN	IT REGULATION					
V _(IREG_CHG_RNG)	Charge current regulation differential	$V_{\text{(IREG CHG)}} = V_{\text{(SRP)}} - V_{\text{(SRN)}}$	0		81.28	mV
(IREG_CHG_RNG)	voltage range	V(IREG_CHG) - V(SRP) V(SRN)	0		01.20	
		ChargeCurrent() = 0x1000H		4096		mA
			-2%		2%	
		ChargeCurrent() = 0x0800H		2048		mA
	Charge current regulation accuracy 10 Ω	Charge current() = 0x000011	-4%		3%	
(CHRG_REG_ACC)	current sensing resistor, V _{BAT} > V _(SYSMIN) (0°C - 85°C)	Character (National Inc.)		1024		mA
	,	ChargeCurrent() = 0x0400H	-6%		5%	
				512		mA
		ChargeCurrent() = 0x0200H	-12%		10%	
		CELL = Float or High, BAT below 0x3E(), in LDO	,,			
	Pre-charge current clamp (2s-4s)	mode		384		mA
(== /	Pre-charge current clamp (1s only)	CELL = LOW, BAT below BATLOWV threshold		384		mA
	Fact charge ourrent clamp (1a only)	CELL = LOW, BAT above BATLOWV threshold,		2		۸
	Fast charge current clamp (1s only)	but below 0x3E()		2		Α
PRECHARGE CUR	RENT REGULATION IN LDO MODE					
		ChargeCurrent() = 0v0190H		384		mA
		ChargeCurrent() = 0x0180H	-15%		15%	
		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		256		mA
	Precharge current regulation accuracy,	ChargeCurrent() = 0x0100H	-20%		20%	
(PRECHRG_REG_ACC)	$V_{BAT} > V_{(SYSMIN)}$ (0°C - 85°C)			192		mA
		ChargeCurrent() = 0x00C0H	-25%		25%	
				128		mA
		ChargeCurrent() = 0x0080H	-30%		30%	
	SRP, SRN leakage current mismatch		-21		21	μA
LEAK_SRP_SRN)	ST CHARGE COMPARATOR		-21		21	μΑ
DO MODE TO FA						
(BAT_SYSMIN)	LDO mode to fast charge mode threshold, V _{BAT} rising	as percentage of 0x3E()	94%	96%	99%	
	Fast charge mode to LDO mode threshold	4				
V(BAT_SYSMIN_HYST)	hysteresis	as percentage of 0x3E()		4%		
NPUT CURRENT I	REGULATION					
/upso ps	Input current regulation differential voltage	$V_{\text{(IREG DPM)}} = V_{\text{(ACP)}} - V_{\text{(ACN)}}$	0		81.28	mV
(IREG_DPM_RNG)	range	· (IREG_DPM) - · (ACP) · (ACN)	3		01.20	
		ChargeCurrent() = 0x1000H		4096		mA
			-2		2%	
		ChargeCurrent() = 0v0800H		2048		mA
	Input ourrent regulation accuracy	ChargeCurrent() = 0x0800H	-3		3%	
(DPM_REG_ACC)	Input current regulation accuracy	0 0 0 0000		1024		mA
		ChargeCurrent() = 0x0400H	-5		5%	
				512		mA
		ChargeCurrent() = 0x0200H			10%	
			-10		10 /0	



 $4.5V \le V_{(VCC)} \le 24V$, $-20^{\circ}C \le T_{J} \le 125^{\circ}C$, typical values are at $T_{A} = 25^{\circ}C$, with respect to GND (unless otherwise noted)

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I _(LEAK_ACP_ ACN)	ACP, ACN leakage current mismatch		—11		20	μA
	SENSE AMPLIFIER	1				
V _(ACP/N_OP)	Input common mode range	Voltage on ACP/ACN	4.5		24	V
V _(IADP_CLAMP)	IADP output clamp voltage		3.1	3.2	3.3	V
I _(IADP)	IADP output current				1	mA
(IADF)		V _(IADP) /V _(ACP-ACN) , ChargeOption0[4]=0, (770/773)		40		
$A_{(IADP)}$	Input current sense gain	V _(IADP) /V _(ACP-ACN) , ChargeOption0[4]=1, (770/773)		80		V/V
		V _(ACP-ACN) = 40.96 mV	-2%		2%	
		V _(ACP-ACN) = 40.00 mV V _(ACP-ACN) = 20.48 mV	-3%		4%	
$V_{(IADP_ACC)}$	Input current monitor accuracy	V _(ACP-ACN) = 20.46 mV	-6%		7%	
		V _(ACP-ACN) = 10.24 mV V _(ACP-ACN) = 5.12 mV	-10%		18%	
<u> </u>	Maximum output load canasitance	V(ACP-ACN) = 3.12 IIIV	-1076			n.E
CHARGE CURRE	Maximum output load capacitance	ADI IEIED			100	pF
	NT AND DISCHARGE CURRENT SENSE AN				40	
V _(SRP/N_OP)	Battery common mode range	Voltage on SRP/SRN	2.8		18	V
V _(IBAT_CLAMP)	IBAT output clamp voltage		3.1	3.2	3.3	V
I _(IBAT)	IBAT output current)			1	mA
A _(IBAT_DCHG)	Discharge current sensing gain on IBAT pin	V _(IBAT) /V _(SRN-SRP) , ChargeOption0[3]=0		8		V/V
	piii	V _(IBAT) /V _(SRN-SRP) , ChargeOption0[3]=1		16		
		$V_{(SRN-SRP)} = 40.96 \text{ mV}$	-2%		2%	
I(IBAT_DCHG_ACC)	Discharge current monitor accuracy on	$V_{(SRN-SRP)} = 20.48 \text{ mV}$	-3%		3%	
(IBAT_DCTIG_ACC)	IBAT pin	V _(SRN-SRP) = 10.24 mV	-5%		5%	
		$V_{(SRN-SRP)} = 5.12 \text{ mV}$	-10%		10%	
A _(IBAT_CHG)	Charge current sensing gain on IBAT pin	$V_{(IBAT)}/V_{(SRN-SRP)}$		20		V/V
		V _(SRN-SRP) = 40.96 mV	-2%		2%	
	Charge current monitor accuracy on IBAT	V _(SRN-SRP) = 20.48 mV	-3%		4%	
(IBAT_CHG_ACC)	pin (0°C - 85°C)	V _(SRN-SRP) = 10.24 mV	-5%		7%	
		V _(SRN-SRP) = 5.12 mV	-10%		15%	
$C_{(IBAT_MAX)}$	Maximum output load capacitance				100	pF
SYSTEM POWER	SENSE AMPLIFIER					
V _(ACP/N_OP)	Input common mode range	Voltage on ACP/ACN	4.5		24	V
V _(SRP/N_OP)	Battery common mode range	Voltage on SRP/SRN	2.8		18	٧
V _(PMON)	Power buffer output voltage				3.3	V
V _(PMON_CLAMP)	Power buffer clamp voltage		3	3.2	3.3	V
I _(PMON)	Power buffer output current				105	μA
	System power sense gain,	ChargeOption1[9]=0		0.25		μA/V
A _(PMON)	$V_{(PMON)}/(V_{(ACP-ACN)} \times V_{(ACN)} + V_{(SRN-SRP)} \times V_{(ACN)}$	ChargeOption1[9]=1		1		μΑ/V
	V _(SRP))	0 1 11	-5%	•	5%	μ. σ.
V _(PMON_ACC)	PMON output accuracy	Input 19.5 V, 65W, 1 μΑ/W				
DEON DEOUL AT	O.D.	Battery 11 V, 44W, 1 µA/W	-6%		6%	
REGN REGULATO		V 40 V V 0 20 V (2 -2 -1 -1 -1				.,
V _(REGN_REG)	REGN Regulator voltage (0 mA - 40 mA)	V _(VCC) > 10 V, V _(ACDET) > 0.6 V (0 - 50 mA load)	5	5.5	6	V
V _(DROPOUT)	REGN Voltage in drop out mode	$V_{\text{(VCC)}} = 5 \text{ V}, I_{\text{(LOAD)}} = 20 \text{ mA}$	4.4	4.6	4.7	V
(REGN_LIM)	REGN Current Limit when converter is disabled or in T _(SHUT) (no charging)	V _(REGN) = 4 V, V _(ACP) > V _(UVLO) , 0.6 V < ACDET < 2.4 V	6.5			mA
(CON_ENVI)	REGN Current Limit when converter is enabled (charging)	$V_{(REGN)} = 4 \text{ V}, V_{(ACP)} > V_{(UVLO)}$	50	65		mA
C _(REGN)	REGN Output Capacitor Required for Stability	I _{LOAD} = 100 μA to 50 mA		1		μF
QUIESCENT CUR	RENT			-		
I _(BAT_BATFET_OFF)	Standby mode. System powered by battery. BATFET off (0°C - 85°C). I(SRN) + I(SRN) + I(SRP)+ I(PHASE) + I(BTST) + I(ACP) + I(ACN) + I(BAT) + I(CMSRC) + I(VCC)	V _{BAT} = 16.8 V V _(VCC) < V _(UVLO) , ACDET < 0.6 V		20	27	μΑ

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 $4.5V \le V_{(VCC)} \le 24V$, $-20^{\circ}C \le T_{J} \le 125^{\circ}C$, typical values are at $T_{A} = 25^{\circ}C$, with respect to GND (unless otherwise noted)

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
		$\begin{array}{l} V_{BAT} = 16.8 \text{ V} \\ V_{(VCC)} > V_{(UVLO)}, \text{ ACDET} < 0.6 \text{ V}, 0x12[15]{=}1, \\ low power mode enabled \end{array}$		22	30	μΑ
I _(BAT_BATFET_ON)	Standby mode. System powered by battery. BATFET on (0°C - 85°C). I(SRN) + I(SRP) + I(PHASE) + I(BTST) + I(ACP) + I(ACN) + IBAT + I(CMSRC) + I(VCC)	$ \begin{aligned} & V_{BAT} = 16.8 \text{ V} \\ & V_{(VCC)} > V_{(UVLO)}, \text{ ACDET} < 0.6 \text{ V}, 0x12[15] = 0, \\ & 0x3B[2] = 0, \\ & I_{BAT} \text{ Enabled, REGN} = 0 \end{aligned} $		114	150	μΑ
	(AUN) · BAT · (UMSRC) · (VCC)	$ \begin{aligned} & V_{BAT} = 16.8 \text{ V} \\ & V_{(VCC)} > V_{(UVLO)}, \text{ ACDET} < 0.6 \text{ V}, 0x12[15] = 0, \\ & 0x3B[2] = 0, \\ & I_{BAT} \text{ enabled, REGN} = 5.5 \text{V} \end{aligned} $		650	775	μΑ
I _(STANDBY)	Adapter standby quiescent current, $I_{(VCC)} + I_{(ACP)} + I_{(ACN)} + I_{(CMSRC)} + I_{(SRP)} + I_{(SRN)} + I_{(PHASE)} + I_{(BTST)}$	$\begin{aligned} &\text{ACN} = \text{ACP} = \text{CMSRC} = \text{VCC} = 20 \text{ V}, \\ &\text{V}_{\text{BAT}} = 12.6\text{V}, \text{V}_{(\text{ACDET})} > 2.4\text{V}, \\ &\text{CELL pul up, T}_{\text{J}} = 0^{\circ}\text{C} - 85^{\circ}\text{C} \end{aligned}$		650	815	μΑ
	Adapter current,	I _(STANDBY) plus supply current in PFM, 200mW output; Reg0x12[10]=0;MOSFET Qg=4 nF;		1.5	2	mA
I _(AC_SWLIGHT)	$I_{(VCC)} + I_{(ACP)} + I_{(ACN)} + I_{(CMSRC)} + I_{(SRP)} + I_{(SRN)} + I_{(PHASE)} + I_{(BTST)}$	I _(STANDBY) plus supply current in PFM, 200mW output, Reg0x12[10]=1; limit 40kHz, MOSFET Qg=4 nF;		3	5	mA
I _(AC_SW)	$ \begin{aligned} & \text{Adapter current,} \\ & I_{(VCC)} + I_{(ACP)} + I_{(ACN)} + I_{(CMSRC)} + I_{(SRP)} + \\ & I_{(SRN)} + I_{(PHASE)} + I_{(BTST)} \end{aligned} $	$ \begin{aligned} & V_{(\text{ULVO})} < V_{(\text{VCC})} < V_{(\text{ACOVP})}, V_{\text{BAT}} = 16.8 \text{V}, \\ & V_{(\text{ACDET})} > 2.4 \text{V}, \\ & \text{charge enabled, 800k Hz switching,} \\ & \text{MOSFET Qg=4 nF} \end{aligned} $		8		mA
ACOK COMPARA	TOR				'	
V _(ACOK_RISE)	ACOK rising threshold	V _(VCC) > V _(UVLO) , ACDET rising	2.37	2.4	2.43	V
V _(ACOK_FALL)	ACOK falling threshold	$V_{(VCC)} > V_{(UVLO)}$	2.32	2.35	2.38	V
V _(ACOK_RISE_DEG)	ACOK rising deglitch to turn on ACFET	V _(VCC) > V _(UVLO)		2		ms
V _(ACOK_FALL_DEG)	ACOK falling deglitch to turn off ACFET	$V_{(VCC)} > V_{(UVLO)}$		2		μs
V _(WAKEUP_RISE)	WAKEUP detect rising threshold	ACDET rising		0.56	0.8	V
V _(WAKEUP_FALL)	WAKEUP detect falling threshold		0.3	0.5		V
UNDER VOLTAGI	E LOCKOUT COMPARATOR (UVLO)					
V _(UVLOZ)	V _{CC} undervoltage rising threshold	V _{CC} rising	2.5	2.7	2.9	V
V _(UVLO)	V _{CC} undervoltage falling threshold	V _{CC} falling	2.3	2.5	2.7	V
SLEEP COMPARA	ATOR (VCC_BAT)					
V _(VCC-BAT_FALL)	VCC-BAT falling threshold	Input connected to VCC via schottler diada	-25	55	135	mV
$V_{(VCC-BAT_RISE)}$	VCC-BAT rising threshold	Input connected to VCC via schottky diode	174	275	370	mV
t _{VCC_BAT_RDEG}	V _{CC} to BAT rising deglitch	V _{CC} rising above SRN deglitch to turn on ACDRV		4		ms
t _{VCC_SRN_FDEG}	V _{CC} to BATfalling deglitch	V _{CC} falls below SRN deglitch to turn off ACDRV		100		μs
INPUT OVERVOL	TAGE COMPARATOR (ACOVP)					
$V_{(ACOV_RISE)}$	V _{CC} overvoltage rising threshold	V _{CC} rising	24	26	28	V
$V_{(ACOV_FALL)}$	V _{CC} overvoltage falling threshold	V _{CC} falling	22	24.5	27.5	V
V _(ACOV_RISE_DEG)	V _{CC} overvoltage rising deglitch	V _{CC} rising to turn off ACDRV		100		μs
$V_{(ACOV_FALL_DEG)}$	V _{CC} overvoltage falling deglitch	V _{CC} falling falling to turn on ACDRV		3		ms
INPUT OVERCUR	RENT COMPARATOR (ACOC)		T		т	
V _(ACOC)	ACP to ACN rising threshold, respect to inputcurrent(), peak	Voltage across input sense resistor rising, Reg0x12[7]=1	270%	300%	330%	
V _(ACOC_FLOOR)	Measure between ACP and ACN	Set IDPM to min	44	50	55	mV
V _(ACOC_CEILING)	Measure between ACP and ACN	Set IDPM to max	174	180	185	mV
t _{RELAX}	Falling deglitch time	Relax Time, No Latchoff		300		ms
SYSTEM OVERVO	OLTAGE COMPARATOR (SYS_OVP)		T			
	System Overvoltage riging threshold to turn	CELL = Low	4.9	5	5.2	V
$V_{(SYSOVP_RISE)}$	System Overvoltage rising threshold to turn off ACFET	CELL = Float	11.9	12	12.3	V
		CELL = High	18.4	18.5	19	V



 $4.5\text{V} \le \text{V}_{(\text{VCC})} \le 24\text{V}, -20^{\circ}\text{C} \le \text{T}_{\text{J}} \le 125^{\circ}\text{C}, \text{ typical values are at T}_{\text{A}} = 25^{\circ}\text{C}, \text{ with respect to GND (unless otherwise noted)}$

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
		CELL = Low	4.6	4.7	4.9	V
V _(SYSOVP FALL)	System Overvoltage falling threshold	CELL = Float	10.9	11.1	11.3	V
(=====,		CELL = High	17.4	17.7	17.9	V
OVP	Discharge current when the OVP stop switching was triggered	On SRP and SRN		19		mA
SYSOVP	Deglitch time to latch off ACFET			25		μs
BAT OVERVOLTA	GE COMPARATOR (BAT_OVP)					
V _(OVP_RISE)	Overvoltage rising threshold as percentage of V _(BAT_REG)	BAT rising	101%	102%	103%	
V _(OVP_FALL)	Overvoltage falling threshold as percentage of V _(BAT_REG)	BAT falling	100%	101%	102%	
l _{OVP}	Discharge current during OVP	On SRP and SRN		19		mA
t _{OVP_RISE}	Overvoltage rising deglitch to turn off BATDRV to disable charge			20		ms
CONVERTER CYC	LE-BY-CYCLE COMPARATOR (ILIM_HI)		,			
	0	Reg0x12 [6]=1	249	290	333	mV
V _(OCP_limit)	Converter over current limit (PH-GND)	Reg0x12 [6]=0	142	170	202	mV
$V_{(OCP_limit_SYSSHORT)}$	0 . 0 . 00	Reg0x12 [6]=1	41	66	87	mV
(OCF_IIIIIL_5155HURI	System Short or SRN < 2.5 V	Reg0x12 [6]=0	7	31	53	mV
CONVERTER CYC	LE-BY-CYCLE UNDER-CURRENT COMPA	ATOR (UCP)				
V _(UCP FALL)	Charge Undercurrent falling threshold	PH voltage when LSFET is on	-2.8		0.4	mV
BATTERY LOWV (COMPARATOR					
		CELL = Low	2.64	2.85	3.06	V
$V_{(BATLV_FALL)}$	BATLOWV falling threshold	CELL = Float or High	5.71	5.92	6.12	V
		CELL = Low	2.89	3.10	3.31	V
V _(BATLV_RHYST)	BATLOWV rising threshold	CELL = Float or High	5.96	6.17	6.37	V
LIGHT LOAD COM	PARATOR (LIGHT_LOAD)	,				
V _{LL(FALL)}	Light load falling threshold detected on ACP-ACN		0	0.5	1.1	mV
V _{LL(RISE)}	Light load rising threshold detected on ACP-ACN		0.7	1.4	2.1	mV
THERMAL SHUTD	OWN COMPARATOR					
T _(SHUT)	Thermal shutdown rising temperature	Temperature increasing		155		°C
T _(SHUT_HYS)	Thermal shutdown hysteresis, falling			20		°C
SHUT RDEG	Thermal shutdown rising deglitch			100		μs
tshut_fhys	Thermal shutdown falling deglitch			10		ms
VSYS PROCHOT C	COMPARATOR		l .			
		Reg0x3C [7:6]=00		5.75		V
		Reg0x3C [7:6]=01	5.9	6	6.15	V
$V_{(SYS_PRO)}$	V _(SYS) threshold falling threshold	Reg0x3C [7:6]=10		6.25	-	V
		Reg0x3C [7:6]=11		6.5		V
tsys_pro_rise_deg	V _(SYS) Rising Deglitch for throttling	· · ·		20		μs
CRIT PROCHOT C	()		1			
V _(ICRIT_PRO)	IADP rising threshold for throttling above IDPM	Reg0x3C [15:11]=01001	145%	150%	155%	
INOM PROCHOT C						
V _(INOM_PRO)	INOM rising threshold as percentage of IDPM		106%	110%	114%	
		<u> </u>				
DCHG PROCHOT						
IDCHG PROCHOT	IDCHG threshold for throttling for IDSCHG			6144		mA

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 $4.5\text{V} \le \text{V}_{(\text{VCC})} \le 24\text{V}, -20^{\circ}\text{C} \le \text{T}_{\text{J}} \le 125^{\circ}\text{C}, \text{ typical values are at T}_{\text{A}} = 25^{\circ}\text{C}, \text{ with respect to GND (unless otherwise noted)}$

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
INDEPENDENT C	COMPARATOR					
	Independent comparator threshold	Reg0x3B [7]=1, CMPIN rising	1.17	1.2	1.23	V
$V_{(INDEP_CMP)}$	independent comparator threshold	Reg0x3B [7]=0, CMPIN rising	2.27	2.3	2.33	V
V _(INDEP_CMP_HYS)	Independent comparator hysteresis	Reg0x3B [6]=0, CMPIN falling		100		mV
PWM OSCILLATO	OR					
		Reg0x12 [9:8]=00	510	600	690	
_	DWM Switching fraguency	Reg0x12 [9:8]=01	680	800	920	kHz
F _{SW}	PWM Switching frequency	Reg0x12 [9:8]=10	850	1000	1150	KIIZ
		Reg0x12 [9:8]=11	1020	1200	1380	
BATFET GATE D	RIVER (BATDRV)					
V _(BATDRV_ON)	Gate Drive Voltage on BATFET	V _(SRN) - V _(BATDRV) when BAT = 16 V	8.5	9.5	10.5	V
R _(BATDRV_ON)	Measured by sourcing 10 μA current to BATDRV		3	3.5	4	kΩ
R _(BATDRV_OFF)	Measured by sinking 100 μA current from BATDRV		1.5	2	2.5	kΩ
ACFET GATE DR	RIVER (ACDRV)		•			
I _(ACFET)	ACDRV charge pump current limit	V _(ACDRV) - V _(CMSRC) = 5 V	40	60		μΑ
V _(ACDRV_ON)	Gate drive voltage on ACFET	$V_{(ACDRV)} - V_{(CMSRC)}$ when $V_{(VCC)} > V_{(UVLO)}$	5.5	6.2		V
R _(ACDRV_OFF)	ACDRV turn-off resistance	Ι = 30μΑ	5	6.2	7.4	kΩ
R _(ACDRV_LOAD)	Minimum load between gate and source		500			kΩ
PWM HIGH SIDE	DRIVER (HIDRV)					
R _{DS(HI ON)}	High side driver(HSD) turn-on resistance	$V_{(BTST)} - V_{(PH)} = 5 \text{ V}$		4		Ω
R _{DS(HI_OFF)}	High side driver turn-off resistance	V _(BTST) – V _(PH) = 5 V		0.65	1.3	Ω
V _(BTST_REFRESH)	Bootstrap refresh comparator falling threshold voltage	V _(BTST) – V _(PH) when low side refresh pulse is requested	3.5	3.8	4.1	V
PWM LOW SIDE	DRIVER (LODRV)					
R _{DS(LO ON)}	Low side driver (LSD) turn-on resistance	$V_{(BTST)} - V_{(PH)} = .55 \text{ V}$		5.5		Ω
R _{DS(LO OFF)}	Low side driver turn-off resistance	V _(BTST) - V _(PH) = 5.5 V		1	1.45	Ω
INTERNAL SOFT	START	(-151)				
	Soft start step size			64		mA
I _(CHG_DAC)	Soft start step time			30		μs
INTEGRATED BT	ST DIODE					•
V _F	Forward bias voltage	I _F = 20 mA at 25°C		0.8		V
V _R	Reverse breakdown voltage	I _R = 2 μA at 25°C			20	V
PWM DRIVERS T		I			-	
t _{DEADTIME} RISE	Driver dead time from low side to high side			20		ns
t _{DEADTIME_FALL}	Driver dead time from high side to low side			20		ns
LOGIC INPUT (SI		1				
		I2C (bg24773)			0.4	V
$V_{(IN_LO)}$	Input low threshold	SMBus (bg24770)			0.8	V
		I2C (bq24773)	1.3		0	V
$V_{(IN_HI)}$	Input high threshold	SMBus (bq24770)	2.1			
LOGIC OUTPUT	OPEN DRAIN (ACOK, SDA,CMPOUT)					•
V _(OUT_LO)	Output saturation voltage	5 mA drain current			0.4	V
V _(OUT_ LEAK)	Leakage current (ACOK, SDA, SCL)	V = 7 V	-1		1	μA
	OPEN DRAIN (PROCHOT)	1				•
V _(OUT_LO)	Output saturation voltage	50 Ω pull up to 1.05 V/ 5mA load			300	mV
V _(OUT_ LEAK)	Leakage current	V = 5.5 V	-1		1	μA
ANALOG INPUT		1			•	r *
V _(CELL_HIGH)	3S/4S	REGN = 5.4 V	1.9			V
V _(CELL_FLOAT)	28	REGN = 5.4 V	1.2		1.8	V
·(CELL_FLOAT)		0 = 0.1 V	1.2		1.0	٧



 $4.5\text{V} \le \text{V}_{(VCC)} \le 24\text{V}, -20^{\circ}\text{C} \le \text{T}_{J} \le 125^{\circ}\text{C}$, typical values are at $\text{T}_{A} = 25^{\circ}\text{C}$, with respect to GND (unless otherwise noted)

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{(CELL_LOW)}$	18	REGN = 5.4 V			1.1	V
R _(CELL_UP)	Internal resistor between CELL and REGN			405		kΩ
R _(CELL_DN)	Internal resistor between CELL and GND			141		kΩ
ANALOG INPUT (/	BATPRES)					
V _(BATPRES_RISE)	BATPRES pin rising threshold	BATPRES rising	2.1	2.2	2.3	V
V _(BATPRES_FALL)	BATPRES pin falling threshold	BATPRES falling	2	2.05	2.1	V

7.6 Timing Requirements

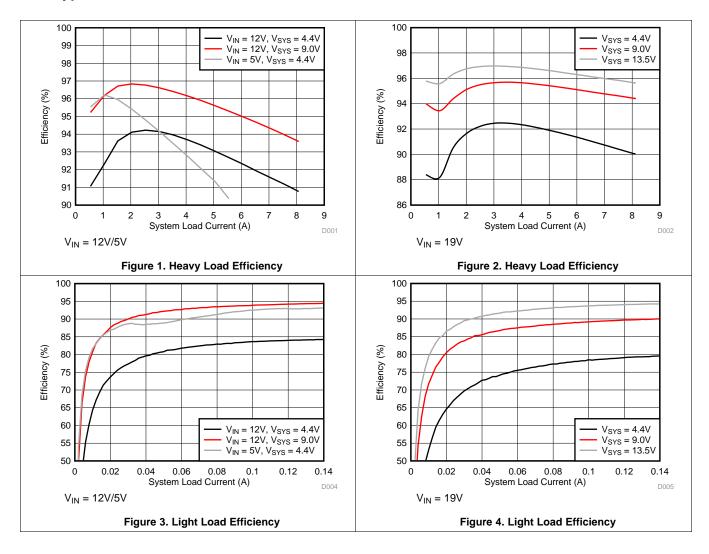
	- 5	MIN	TYP	MAX	UNIT
SMBus TIN	NING CHARACTERISTICS	<u>'</u>			
t _r	SCLK/SDATA rise time			1	μs
t _f	SCLK/SDATA fall time			300	ns
t _{W(H)}	SCLK pulse width high	4		50	μs
$t_{W(L)}$	SCLK Pulse Width Low	4.7			μs
t _{SU(STA)}	Setup time for START condition	4.7			μs
t _{H(STA)}	START condition hold time after which first clock pulse is generated	4			μs
t _{SU(DAT)}	Data setup time	250			μs
t _{H(DTA)}	Data hold time	300			μs
t _{SU(STOP)}	Setup time for STOP condition	4			μs
t _(BUF)	Bus free time between START and STOP condition	4.7			μs
F _{S(CL)}	Clock Frequency	10		100	KHz
HOST COM	MUNICATION FAILURE	·			
t _{timeout}	SMBus bus release timeout ⁽¹⁾	25		35	ms
t _{BOOT}	Deglitch for watchdog reset signal	10			ms
	Watchdog timeout period, ChargeOption() bit [14:13] = 01 ⁽²⁾	35	44	53	s
t_{WDI}	Watchdog timeout period, ChargeOption() bit [14:13] = 10 ⁽²⁾	70	88	105	s
	Watchdog timeout period, ChargeOption() bit [14:13] = 11 ⁽²⁾ (default)	140	175	210	s

⁽¹⁾ Devices participating in a transfer will timeout when any clock low exceeds the 25ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35 ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified as it incorporates the cumulative stretch limit for both a master (10 ms) and a slave (25 ms).

(2) User can adjust threshold via SMBus ChargeOption() REG0x12.



7.7 Typical Characteristics





8 Detailed Description

8.1 Overview

The bq2477x is a 1-4 cell battery charge controller with power selection for space-constrained, multi-chemistry portable applications such as notebook and detachable ultrabook. It supports wide input range of input sources from 4.5V to 24V, and 1-4 cell battery for a versatile solution.

The bq2477x supports automatic system power source selection with separate drivers for n-channel MOSFETs on the adapter side, and p-channel MOSFETs on the battery side.

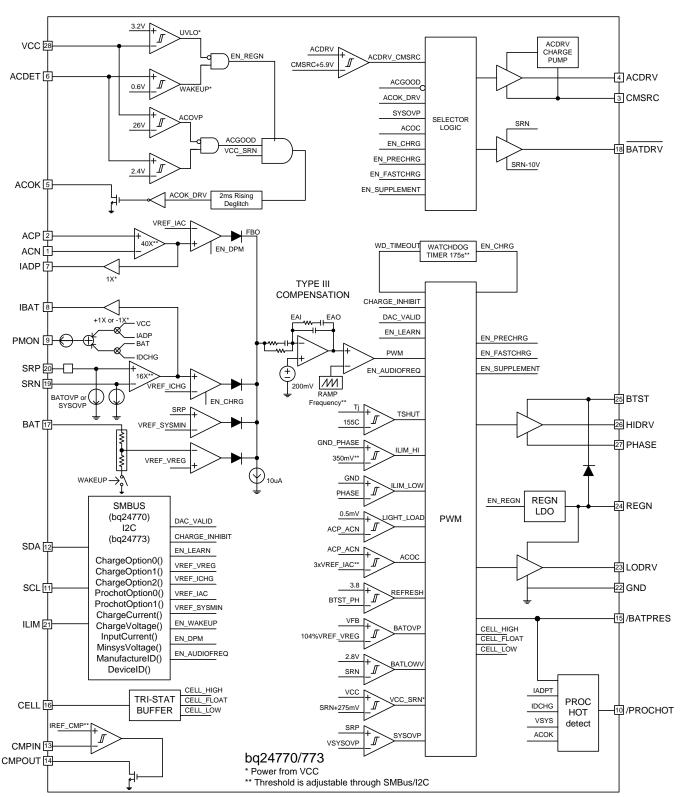
The bq2477x features Dynamic Power Management (DPM) to limit the input power and avoid AC adapter overloading. During battery charging, as the system power increases, the charging current will reduce to maintain total input current below adapter rating. If system power demand is temporarily exceeds adapter rating, the bq2477x supports NVDC architecture to allow battery discharge energy to supplement system power. For details, refer to the *System Voltage Regulation with Narrow VDC Architecture* section.

The bq2477x closely monitors system power (PMON), input current (IADP) and battery current (IBAT) with highly accurate current sense amplifiers. If current is too high, adapter or battery is removed, a PROCHOT signal is asserted to CPU so that the CPU optimizes its performance to the power available to the system.

The SMBus/I2C controls input current, charge current and charge voltage registers with high resolution, high accuracy regulation limits. It also sets the PROCHOT timing and threshold profile to meet system requirements.



8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Battery Only

Battery is connected to VCC via diode. When VCC voltage is above UVLO, bq2477x powers up to turn on BATFET and starts SMBus/I2C communication. By default, bq2477x stays in low power mode (0x12[15] = 1) with lowest quiescent current.

When 0x12[15] is set to 0, the device enters performance mode. The user can enable IBAT buffer through SMBus/I2C. In order to enable PMON, PROCHOT or independent comparator, the bq2477x enables REGN LDO for accurate reference.

8.3.2 Adapter Detect and ACOK Output

An external resistor divider attenuates the adapter voltage before it goes to ACDET. The adapter detect threshold should typically be programmed to a value greater than the maximum battery voltage, but lower than the maximum allowed adapter voltage. When ACDET is above 0.6V, REGN LDO and bias circuits are enabled.

The open drain ACOK output can be pulled to external rail under the following conditions:

- $V_{(UVLO)} < V_{(VCC)} < V_{(ACOVP)}$
- V_(ACDET) > 2.4 V
- $V_{(VCC)} V_{(SRN)} > V_{(VCC SRN RISE)}$

8.3.2.1 Adapter Overvoltage (ACOVP)

When the VCC pin voltage is higher than 26 V, it is considered adapter over voltage. ACOK is pulled low, and charge is disabled. ACFET/RBFET are turned off to disconnect the high voltage adapter to system during ACOVP. BATFET is turned on if turn-on conditions are valid. When VCC voltage falls below 22 V, it is considered as adapter voltage returns back to normal voltage. ACOK is pulled high by an external pullup resistor. BATFET is turned off and ACFET and RBFET is turned on to power the system from the adapter.

8.3.3 System Power Selection

The bq2477x device automatically switches adapter or battery power to system.

The ACDRV drives a pair of common-source (CMSRC) N-channel power MOSFETs (ACFET and RBFET) between adapter and ACP (see Figure 21 for details). The ACFET separates adapter from system and battery, and provides a limited di/dt when plugging in adapter by controlling the ACFET turn-on time. The RBFET provides negative input voltage protection and battery discharge protection when adapter is shorted to ground, and minimizes system power dissipation with its low R_{DS(on)} compared to a Schottky diode.

When the adapter is not present, ACDRV is pulled to CMSRC to keep ACFET and RBFET off, disconnecting the adapter from the system. BATDRV stays as low as VSRN – 10 V to connect battery to system if all of the following conditions are valid:

- $V_{(VCC)} > V_{(UVLO)}$
- $V_{(SRN)} V_{(SRP)} > 2.56 \text{ mV}$

After the adapter plugs in, the system power source switches from battery to adapter if ACOK is HIGH. The gate drive voltage on ACFET and RBFET is $V_{(CMSRC)}$ + 6 V. If ACDRV-CMSRC voltage drops at least 100 mV from its normal voltage, the converter stops.

To limit the adapter inrush current during ACFET turn-on, the Cgs and Cgd external capacitor of ACFET must be carefully selected following the guidelines below:

- Minimize total capacitance on system
- Cgs should be 40x or higher than Cgd to avoid ACFET false turn on during adapter hot plug-in
- Check with MOSFET vendor on peak current rating
- Place 4 $k\Omega$ resistor in series with ACDRV and CMSRC pins to limit MOSFET turn on/off time.



Feature Description (continued)

8.3.4 System Power Up

After the ACFET is turned on, the converter is enabled and the HSFET and LSFET start switching. Every time the buck converter is started, the IC automatically applies soft-start (no soft-start when exit LEARN) on buck output current to avoid any overshoot or stress on the output capacitors or the power converter. No external components are needed for this function.

When power up, the converter output voltage is a default value set by CELL pin configuration.

CELL PIN	DEFAULT BATTERY CONFIGURATION	DEFAULT MaxChargevoltage()	DEFAULT MinSystemVoltage()	SYSOVP THRESHOLD
Low	1s	4400mV	3568mV	5 V
Float	2s	9008mV	6144mV	12 V
High	3s/4s	13504mV	9008mV	18.5 V when MaxChargeVoltage() < 15 V

Table 1. Cell Pin Configuration

8.3.4.1 Dynamic Power Management (IDPM) and Supplement Mode

When the input current exceeds the input current setting, the bq2477x decreases the charge current to provide priority to system load. As the system current rises, the available charge current drops accordingly toward zero. If the system load keeps increasing after charge current drops down to zero, the system voltage starts to drop. As the system voltage drops below battery voltage, the device enters supplement mode, the battery starts discharge, and the total system power equals to input supply power and battery discharge power.

8.3.4.2 Minimum System Voltage Regulation and LDO Mode

The BATDRV drives a p-channel BATFET between converter output and battery to provide a charge and discharge path for battery. The system is always above the MinSystemVoltage() even with depleted battery or without battery.

When battery voltage is below the minimum system voltage setting, this BATFET works in linear mode (LDO mode) during battery charging. The precharge current is set by ChargeCurrent() and clamped below 384mA. If battery voltage reaches the minimum system voltage, BATFET fully turns on.

The minimum BATDRV voltage is 1.1 V. For 1s application, the BATFET has to fully turn on when the gate voltage is 1.1 V or higher. Otherwise, BATFET may not operate properly.

8.3.5 Current and Power Monitor

8.3.5.1 High Accuracy Current Sense Amplifier (IADP and IBAT)

As an industry standard, a high-accuracy current sense amplifier (CSA) is used to monitor the input current (IADP) and the charge/discharge current (IBAT). IADP voltage is 40X or 80X the differential voltage across ACP and ACN. IBAT voltage is 20X (during charging), or 8X/16X (during discharging) of the differential across SRP and SRN. After VCC is above $V_{(UVLO)}$ and ACDET is above 0.6 V, IADP output becomes valid. To lower the voltage on current monitoring, a resistor divider from CSA output to GND can be used and accuracy over temperature can still be achieved.

A maximum 100-pF capacitor is recommended to connect on the output for decoupling high-frequency noise. An additional RC filter is optional, if additional filtering is desired. Note that adding filtering also adds additional response delay. The CSA output voltage is clamped at 3.3 V.

8.3.5.2 High Accuracey Power Sense Amplifier (PMON)

The bq2477x device monitors total available power from adapter and battery together. The ratio of PMON current and total power $K_{(PMON)}$ can be programmed in ChargeOption1() bit[8] with default 1µA/W. The bq2477x device allows input sense resistor 2x of charge sense resistor by setting ChargeOption1() bit[12] to 1.

$$I = K_{(PMON)}(V_{IN} \times I_{IN} + V_{BAT} \times I_{BAT}) (I_{BAT} > 0 \text{ during battery discharging, } I_{BAT} < 0 \text{ during battery charging)})$$
 (1)



A maximum PMON output current is 100µA. The user picks output resistor based on peak system power rating. The PMON output voltage is clamped below 3.3V.

8.3.6 Processor Hot Indication for CPU Throttling

When CPU is running turbo mode, the peak power may exceed total available power from adapter and battery. The adapter current and battery discharge overshoot, or system voltage drop indicates the system power may be too high. When the adapter or battery is removed, the remaining power source may not support the peak power in turbo mode. The processor hot function in bq2477x monitors these events, and PROCHOT pulse is asserted.

The PROCHOT triggering events include:

- · ICRIT: adapter peak current
- INOM: adapter average current (110% of input current limit)
- IDCHG: battery discharge current
- VSYS: system voltage on SRN for 2s 4s battery
- ACOK: upon adapter removal (ACOK pin HIGH to LOW)
- BATPRES: upon battery removal (BATPRES pin LOW to HIGH)
- CMPOUT: Independent comparator output (CMPOUT pin HIGH to LOW)

The threshold of ICRIT, IDCHG or VSYS, and the deglitch time of ICRIT, INOM, IDCHG or CMPOUT are programmable through SMBus. Each triggering event can be individually enabled in REG0x3D[6:0].

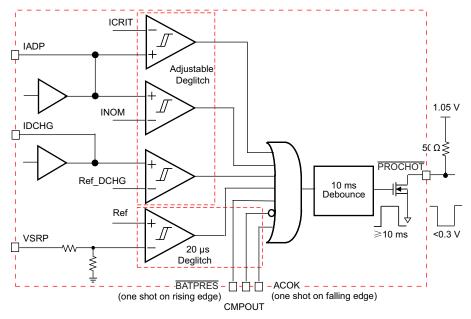


Figure 5. PROCHOT Profile

When any event in PROCHOT profile is triggered, PROCHOT is asserted low for minimum 10 ms (default 0x3C[4:3]). At the end of the 10 ms, if the PROCHOT event is still active, the pulse gets extended.

8.3.7 Converter Operation

The bq2477x typically use $2.2/3.3~\mu H$ inductor and $60~\mu F$ output capacitance to achieve all loops stable. This capacitance could be from system bus decoupling cap. But in order to achieve good output transient response, like mini output drop or min output spike, then it is better to have more output capacitance from the system bus, which could be the total input capacitance from the input of the down-stream DC-DC converters for CPU core, DDR and chip-set.



Ceramic capacitors show a DC-bias effect. This effect reduces the effective capacitance when a DC-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a DC bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value to get the required value at the operating point.

8.3.7.1 Continuous Conduction Mode (CCM)

With sufficient charge current, the inductor current does not cross 0, which is defined as CCM. The controller starts a new cycle with ramp coming up from 200 mV. As long as EAO voltage is above the ramp voltage, the high-side MOSFET (HSFET) stays on. When the ramp voltage exceeds EAO voltage, HSFET turns off and lowside MOSFET (LSFET) turns on. At the end of the cycle, ramp gets reset and LSFET turns off, ready for the next cycle. There is always break-before-make logic during transition to prevent cross-conduction and shoot-through. During the dead time when both MOSFETs are off, the body-diode of the low-side power MOSFET conducts the inductor current.

During CCM, the inductor current always flows and creates a fixed two-pole system. Having the LSFET turn-on keeps the power dissipation low and allows safe charging at high currents.

8.3.7.2 Discontinuous Conduction Mode (DCM)

During the HSFET off time when LSFET is on, the inductor current decreases. If the current goes to 0, the converter enters DCM. Every cycle, when the voltage across SRP and SRN falls below 0 mV, the undercurrent-protection comparator (UCP) turns off LSFET to avoid negative inductor current, which may boost the system through the body diode of HSFET.

During DCM the loop response automatically changes. It changes to a single-pole system and the pole is proportional to the load current.

8.3.7.3 PFM Mode

In order to improve converter light-load efficiency, the bq2477x switches to PFM control at light load with charge disable or charge in LDO mode. The effective switching frequency will decrease accordingly when system load decreases. The minimum frequency can be limit to 40kHz (ChargeOption0() bit[10]=1). To have higher light load efficiency, set "Audio Frequency Limit" bit low (Chargeoption0() bit[10]=0).

8.3.7.4 Switching Frequency Adjust

The charger switching frequency can be adjusted to solve EMI issue via SMBus/I2C command. ChargeOption0() bit [9:8] can be used to set switching frequency. If frequency is reduced, the current ripple is increased. Inductor value must be carefully selected so that it will not trigger cycle-by-cycle peak over current protection even for the worst condition such as higher input voltage, 50% duty cycle, lower inductance and lower switching frequency.

8.3.8 Learn Mode

LEARN mode is set up to calibrate gauge in the pack. When LEARN is enabled, the system first discharge the battery below depletion threshold, and complete another charging cycle for gauge calibration. During the discharging, BATFET turns on and converter stops.

A battery LEARN cycle can be activated via SMBus/I2C "LEARN Enable" command (ChargeOption0() bit[5]=1 enable Learn Mode). When LEARN is enabled with an adapter connected, the system power switch to battery by turning off converter and keep ACFET/BATFET on. Learn mode allows the battery to discharge in order to calibrate the battery gas gauge over a complete discharge/charge cycle. When LEARN is disabled, the system power switch to adapter by turning on converter in a few hundreds μ s.

bq2477x also supports hardware pin to exist LEARN mode by driving BATPRES to HIGH. When BATPRES pin is pulled to HIGH, bq2477x resets "LEARN Enable" (ChargeOption0() bit[5]) and IDPM_EN (ChargeOption() bit[1]), and reset MaxChargeVoltage() and ChargeCurrent().



8.3.9 Charger Timeout

The bq2477x includes a watchdog timer to terminate charging if the charger does not receive a write MaxChargeVoltage() or write ChargeCurrent() command within 175s (adjustable via ChargeOption() command). If a watchdog timeout occurs all register values keep unchanged but charge is suspended. Write ChargeVoltage() or write ChargeCurrent() commands must be re-sent to reset watchdog timer and resume charging. The watchdog timer can be disabled, or set to 44s, 88s or 175s via SMBus command (ChargeOption() bit[14:13]). If watchdog is in timeout, disabling watchdog timer by writing ChargeOption() bit[14:13] also resumes charging.

8.3.10 Device Protection Features

8.3.10.1 Input Overcurrent Protection (ACOC)

If the input current exceeds the 3X of input current DAC set point, the converter is disabled. After 300ms, the converter is turned on again.

The ACOC function threshold can be set to 3X of input DPM current (ChargeOption0 bit [7]=1) or function disable (ChargeOption0) bit [7]=0, default) via SMBus command The bg2477x has a cycle-to-cycle peak overcurrent protection. It monitors the voltage across R_{ds(on)} of the LSFET or the input current sense resistor, and prevents the converter from over current condition. The high-side gate drive turns off when the overcurrent is detected, and resumes automatically when the overcurrent condition is gone.

8.3.10.2 Converter Overcurrent Protection

When LODRV pulse is longer than 100ns, the LSFET OCP is active and the threshold is automatically set to 290mV (ChargeOption0() bit [6]=1, default) or 170mV (ChargeOption0() bit [6]=0) via SMBus/I2C command. The blanking time prevents noise when MOSFET just turn on.

When LODRV pulse is shorter than 100ns, bg2477x sets OCP limit proportional to PROCHOT ICRIT setting (ProchotOption0() bit[8]). The IDPM function is disabled (0x12[1]=0). Set InputCurrent() to a right value even IDPM is disabled.

8.3.10.3 Battery Overvoltage Protection (BATOVP)

The bg2477x immediately stops the converter when the voltage at BAT exceeds 104% (1s) or 102% (2s - 4s) of the regulation voltage set-point. This allows guick response to an overvoltage condition - such as occurs when the load is removed or the battery is disconnected. A 19 mA current sink from SRP/SRN to GND is on only during BATOVP and allows discharging the stored output inductor energy that is transferred to the output capacitors.

8.3.10.4 System Overvoltage Protection (SYSOVP)

When the converter starts up, the bq24770 reads CELL pin configuration and sets MaxChargeVoltage() and SYSOVP threshold (1s - 5 V, 2s - 12 V, 3s - 18.5 V). Before MaxChargeVoltage() is written by host, the battery configuration will change with CELL pin voltage.

When SYSOVP happens, the device latchs off ACFET/RBFET. Register ChargeOption0() bit[12] is set as 1.

The user can clear the latch off by either write of 0 to register bit or removal and plugin adapter again (ACDET below 0.6V and back up again). After the latch-off is cleared, ACFET/RBFET turn on and converter starts.

8.3.10.5 Thermal Shutdown Protection (TSHUT)

The WQFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As an added level of protection, the charger converter turns off for self-protection whenever the junction temperature exceeds the 155°C. The charger stays off until the junction temperature falls below 135°C. During thermal shutdown, the REGN LDO current limit is reduced to 14 mA.

Once the temperature falls below 135°C, charge can be resumed with soft start.



8.4 Device Functional Modes

8.4.1 Battery Charging

The bq2477x charges 1-4 cell battery in constant current (CC), and constant voltage (CV) mode. The host programs battery voltage to ChargeVoltage() (0x15()). According to battery voltage, the host programs appropriate charge current to ChargeCurrent() (0x14()). When battery is full or battery is not in good condition to charge, host terminates charge by setting 0x12[0] to 1, or setting ChargeCurrent() to zero.

See the Feature Description section for details on charge enable conditions and register programming.

8.4.2 System Voltage Regulation with Narrow VDC Architecture

The bq2477x deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by MinSystemVoltage(). Even with a deeply depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode). As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the VDS of BATFET.

See the Feature Description section for details on system voltage regulation and register programming.

8.5 Programming

8.5.1 SMBus Interface

The bq24770 device operates as a slave, receiving control inputs from the embedded controller host through the SMBus interface. The bq24770 device uses a simplified subset of the commands documented in *System Management Bus Specification V1.1*, which can be downloaded from www.smbus.org. The bq24770 device uses the SMBus read-word and write-word protocols (shown in Table 2 and Table 3) to communicate with the smart battery. The bq24770 device performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus. In addition, the bq24770 device has two identification registers, a 16-bit device ID register (0xFFH) and a 16-bit manufacturer ID register (0xFEH).

SMBus/I2C communication starts when VCC is above V_(UVLO).

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pullup resistors ($10~k\Omega$) for SDA and SCL to achieve rise times according to the SMBus specifications. Communication starts when the master signals a start condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a stop condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. Figure 6 and Figure 7 show the timing diagram for signals on the SMBus interface. The address byte, command byte, and data bytes are transmitted between the start and stop conditions. The SDA state changes only while SCL is low, except for the start and stop conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the bq2477x device because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock cycle. The bq2477x supports the charger commands listed in Table 2.

Product Folder Links: bq24770 bq24773



Programming (continued)

8.5.1.1 SMBus Write-Word and Read-Word Protocols

Table 2. Write-Word Format

S (1)(2)	SLAVE ADDRESS ⁽¹⁾	W (1)(3)	ACK (4)(5)	COMMAND BYTE ⁽¹⁾	ACK (4)(5)	LOW DATA BYTE ⁽¹⁾	ACK (4)(5)	HIGH DATA BYTE ⁽¹⁾	ACK (4)(5)	P (1)(6)
	7 bits	1b	1b	8 bits	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	

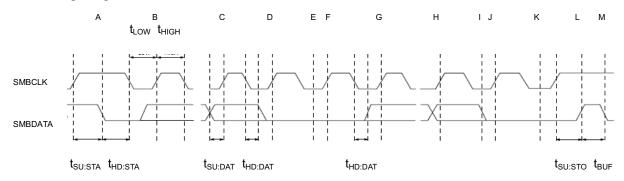
- Master to slave
- S = Start condition or repeated start condition
- W = Write bit (logic-low)
- Slave to master (shaded gray) ACK = Acknowledge (logic-low)
- P = Stop condition

Table 3. Read-Word Format

S ⁽¹⁾	SLAVE ADDRESS ⁽¹⁾	W (1)(3)	ACK (4)(5)	COMMAND BYTE ⁽¹⁾	ACK (4)(5)	S ⁽¹⁾	SLAVE ADDRESS ⁽¹⁾	R ⁽¹⁾ (6)	ACK (4)(5)	LOW DATA BYTE ⁽⁴⁾	ACK (1)(5)	HIGH DATA BYTE ⁽⁴⁾	NACK (1)(7)	P (1)(8)
	7 bits	1b	1b	8 bits	1b		7 bits	1b	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	

- Master to slave
- S = Start condition or repeated start condition (2)
- W = Write bit (logic-low)
- Slave to master (shaded gray)
- ACK = Acknowledge (logic-low)
- R = Read bit (logic-high)
 NACK = Not acknowledge (logic-high)
- P = Stop condition

8.5.1.2 Timing Diagrams



A = Start condition

B = MSB of address clocked into slave

C = LSB of address clocked into slave

D = R/W bit clocked into slave

E = Slave pulls SMBDATA line low

F = ACKNOWLEDGE bit clocked into master

G = MSB of data clocked into slave

H = LSB of data clocked into slave

I = Slave pulls SMBDATA line low

J = Acknowledge clocked into master

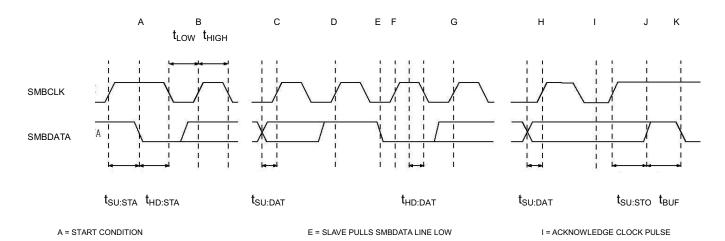
K = Acknowledge clock pulse

L = Stop condition, data executed by slave

M = New start condition

Figure 6. SMBus Write Timing





A = Start condition

B = MSB of address clocked into slave

C = LSB of address clocked into slave

D = R/W bit clocked into slave

E = Slave pulls SMBDATA line low

F = ACKNOWLEDGE bit clocked into master

G = MSB of data clocked into master

H = LSB of data clocked into master

I = Acknowledge clock pulse

J = Stop condition

K = New start condition

Figure 7. SMBus Read Timing

8.5.2 I²C Serial Interface

The bq24773 uses I2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address D4H, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG0F. The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits). connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

8.5.2.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

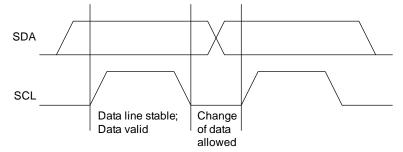


Figure 8. Bit Transfer on the I²C Bus

8.5.2.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCI is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

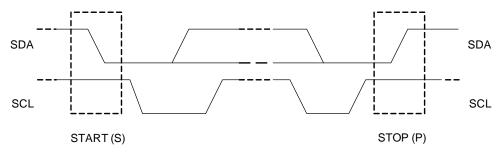


Figure 9. START and STOP Conditions

8.5.2.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

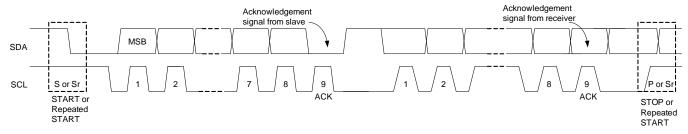


Figure 10. Data Transfer on the I²C Bus

8.5.2.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.



8.5.2.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).



Figure 11. Complete Data Transfer

8.5.2.6 Single Read and Write

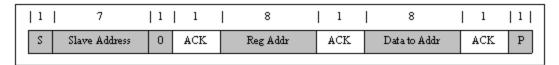


Figure 12. Single Write

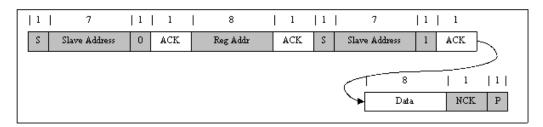


Figure 13. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

8.5.2.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write.

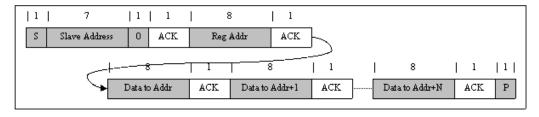


Figure 14. Multi Write

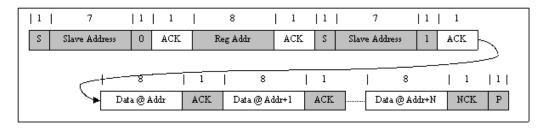


Figure 15. Multi Read



8.6 Register Maps

The bq2477x supports battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Table 4. The SMBUS address is 0x12H or 0001001_X, and I2C address is D4H or 1101010_X, where X is the read/write bit. ManufacturerID() and DeviceID() can be used to identify the bq2477x. The ManufacturerID() command always returns 0x0040H.

Table 4. Battery Charger Command Summary

REGISTER ADDRESS	REGISTER NAME	R/W	DESCRIPTION	POR STATE
SMBus: 0x12H I2C: 01H/00H	ChargeOption0()	R/W	Charger Option Control 0	0xE14EH
SMBus: 0x3B I2C: 03H/02H	ChargeOption1()	R/W	Charge Option Control 1	0x0211H
SMBus: 0x38H I2C: 11H/10H	ChargeOption2()	R/W	Charge Options Control 2	0x0080H
SMBus: 0x3CH I2C: 05H/04H	ProchotOption() R/W PROCH		PROCHOT Option 0	0x4B54H
SMBus: 0x3DH I2C: 07H/06H	ProchotOntion1()		PROCHOT Option 1	0x8120H
SMBus: 0x14H I2C: 0BH/0AH	ChargeCurrent()	R/W	7-Bit Charge Current Setting	0x0000H
SMBus: 0x15H I2C: 0DH/0CH	MaxChargeVoltage()	R/W	11-Bit Charge Voltage Setting	1S-4.4V, 2S-9.008V, 3S/4S-13.504V
SMBus: 0x3EH I2C: 0EH	MinSystemVoltage()	R/W	6-Bit Minimum System Voltage Setting	1S-3.584V, 2S-6.144V, 3S/4S-9.216V
SMBus: 0x3FH I2C: 0FH	InputCurrent()	R/W	7-Bit Input Current Setting	3200mA (770), 2944mA (773)
SMBus: 0xFEH	ManufacturerID()	Read Only	Manufacturer ID	0x0040H
SMBus: 0xFFH I2C: 09H	DeviceAddress()	Read Only	Device Address	0x0114H (770) 0x41H (773)



8.6.1 ChargeOption0 Register

Figure 16. ChargeOption0 Register (0x12H)

15	14	13	12	11	10	9	8
Low Power Mode Enable	WATCHDOG	Timer Adjust	IDPM AUTO DISABLE	SYSOVP Status& Clear	Audio Frequency Limit	Switching Fr	equency[1:0]
R/W	R/	W	R/W	R/W	R/W	R/	W
7	6	5	4	3	2	1	0
ACOC Setting	LSFET OCP Threshold	LEARN Enable	IADP Amplifier Ratio	IBAT Amplifier Ratio for Discharge Current	Reserved	IDPM Enable	Charge Inhibit
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. ChargeOption0 Register (0x12H)

12C 01H	12C 00H	SMBus 0x12H	BIT NAME	DESCRIPTION		
[7]		[15]	Low Power Mode Enable	IC in performance mode with battery only. The enable of PROCHOT, current monitor buffer, power monitor buffer and comparator follow register setting. IC in low power mode with battery only. IC is in the lowest quiescent current when this bit is enabled. /PROCHOT, discharge current monitor buffer, power monitor buffer and independent comparator are disabled.		
[6:5]		[14:13]	WATCHDOG Timer Adjust	set maximum delay between consecutive SMBus/I2C Write charge voltage or charge current command. If IC does not receive write on MaxChargeVoltage() or ChargeCurrent() within the watchdog time period, ChargeCurrent() is set to 0mA to stop charging. The converter keeps running to regulate the system voltage. After expiration, the timer will resume upon the write of MaxChargeVoltage() or ChargeCurrent(). 00: Disable Watchdog Timer 01: Enabled, 44 sec 10: Enabled, 88 sec 11: Enable Watchdog Timer (175s) < default at POR>		
[4]		[12]	IDPM AUTO DISABLE	When the BATPRES pin goes from LOW to HIGH, the charger IC automatically disables the IDPM function (IDPM Enable bit becomes 0). The host can enable IDPM function again by writing IDPM_EN bit 1. 0 - Disable this function <default at="" por=""> 1 - Enable this function</default>		
[3]		[11]	SYSOVP Status& Clear	When the SYSOVP occurs, the bit is HIGH. After the SYSOVP is removed, the user must write a 0 to this register or unplug the adapter to clear the OVP condition. 0: not in SYSOVP, write 0 to clear SYSOVP latch <default at="" por=""> 1: Device in SYSOVP, ACFET/RBFET latches off</default>		
[2]		[10]	Audio Frequency Limit	O: No limit of switching frequency <default at="" por=""> 1: Set minimum switching frequency to 40kHz to avoid audio noise</default>		
[1:0]		[9:8]	Switching Frequency[1:0]	Converter switching frequency. 00: 600 kHz 01: 800kHz <default at="" bq24770="" in="" por=""> 10: 1 MHz 11: 1.2MHz <default at="" bq24773="" in="" por=""></default></default>		
	[7]	[7]	ACOC Setting	Input over-current protection threshold by detecting ACP_ACN voltage. 0: disable ACOC <default at="" por=""> 1: ACOC limit 300% of IDPM</default>		
	[6]	[6]	LSFET OCP Threshold	Cycle-by-cycle over-current protection threshold by detecting GND-PHASE 0: 170mV 1: 290mV <default at="" por=""></default>		
	[5]	[5]	LEARN Enable	Battery LEARN mode enable. In LEARN mode, buck converter turns off while ACFET and RBFET stay on. The BATFET turns on to discharge. Set this bit 0 will stop LEARN mode and turn back on buck converter. 0: Disable LEARN Mode <default at="" por=""> 1: Enable LEARN Mode</default>		
	[4]	[4]	IADP Amplifier Ratio	0: 40x <default at="" por=""> 1: 80x</default>		
	[3]	[3]	IBAT Amplifier Ratio for Discharge Current	0: 8x 1: 16x <default at="" por=""></default>		
	[2]	[2]	Reserved	1- Reserved		
	[1]	[1]	IDPM Enable	Input regulation loop enable. 0 – IDPM disabled 1 – IDPM enabled <default at="" por=""></default>		
	[0]	[0]	Charge Inhibit	Change inhibit bit. To enable charge, first writes this bit to 0 and then write 0x14() non-zero value. 0: Enable charge <default at="" por=""> 1: Disable charge</default>		



8.6.2 ChargeOption1 Register

Figure 17. ChargeOption1 Register (0x3BH)

15	14	13	12	11	10	9	8
	Reserved		RSNS_RATIO	IBAT Enable	PMON Enable	PMON Gain	Reserved
	R		R/W	R/W	R/W	R/W	R
7	6	5	4	3	2	1	0
CMP_REF	CMP_POL	CMP_DEG [1:0]		FET Latch-off Enable	FORCE BATFET Off	Discharge BAT Enable	Auto Wakeup Enable
R/W	R/W R/		/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. ChargeOption1 Register (0x3BH)

12C 03H	12C 02H	SMBus 0x3BH	BIT NAME	DESCRIPTION			
[7:5]		[15:13]		0- Reserved			
[4]		[12]	RSNS_RATIO	Adjust ratio of input sense resistor (RAC) and charge sense resistor (RSR) for power calculation. 0: RAC and RSR 1:1 <default at="" por=""> 1: RAC and RSR 2:1</default>			
[3]		[11]	IBAT Enable	Enable the IBAT output buffer. 0: Turn off IBAT buffer to minimize Iq <default at="" por=""> 1: Turn on IBAT buffer</default>			
[2]		[10]	PMON Enable	Enable PMON sensing circuit and output buffer. 0: turn off PMON buffer to minimize Iq <default at="" por=""> 1: turn on PMON buffer</default>			
[1]		[9]	PMON Gain	PMON output current with respect to the total system power on 10mohm RAC and RSR. 0: 0.25 µA/W 1: 1µA/W <default at="" por=""></default>			
[0]		[8]	Reserved	0- Reserved			
	[7]	[7]	CMP_REF	Independent comparator internal reference. 0: 2.3 V <default at="" por=""> 1: 1.2 V</default>			
	[6]	[6]	CMP_POL	Independent comparator output polarity 0: When CMPIN is above internal threshold, CMPOUT is LOW <default at="" por=""> 1: When CMPIN is above internal threshold, CMPOUT is HIGH</default>			
	[5:4]	[5:4]	CMP_DEG [1:0]	Independent comparator deglitch time. 00: Independent comparator is disabled 01: Independent comparator is enabled with output deglitch time 2 µs <default at="" por=""> 10: Independent comparator is enabled with output deglitch time 2 ms 11: Independent comparator is enabled with output deglitch time 5 sec</default>			
	[3]	[3]	FET Latch-off Enable	When comparator is triggered, all the power path MOSFETs latch off. In order to clear power path latch off, both adapter and battery have to be removed. Therefore, at POR state, the latch off is cleared. 0: When comparator is triggered, no power path latch off <default at="" por=""> 1: When comparator is triggered, power path latches off</default>			
	[2]	[2]	FORCE BATFET Off	The host can force BATFET to turn off at any time. After BATFET is forced off, plugin adapter will set the bit back to 0. 0: Allow BATFET turn on <default at="" por=""> 1: Turn off BATFET</default>			
	[1]	[1]	Discharge BAT Enable	When this bit is 1, discharge BAT pin down below 3.8 V in 40 ms. When 40ms is over, this bit is reset to 0 0 : Disable discharge mode <default at="" por=""> 1: Enable discharge mode</default>			
	[0]	[0]	Auto Wakeup Enable	When this bit is HIGH, if the battery is below 3 V(1s) or 6 V(2s-4s), the IC will automatically enable 128 mA charging current to charge depleted battery for 30 mins. When the battery voltage exceeds 3 V (1S) or 6 V (2S-4S), the charge will stop after 1min deglitch time. After the 30 mins expires, the charging will stop, and this bit is set back to LOW. 0: Disable auto-wakeup 1: Enable auto-wakeup < default at POR>			

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8.6.3 ChargeOption2 Register

Figure 18. ChargeOption2 Register (0x38H)

15	14	13	12	11	10	9	8	
	Reserved							
	R							
7	6	5	4	3	2	1	0	
External ILIM Enable	IBAT Output Select	Reserved						
R/W	R/W	R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. ChargeOption2 Register (0x38H)

12C 10H	SMBus 0x38H	BIT NAME	DESCRIPTION
	[15:8]		0- Reserved
[7]	[7]	External ILIM Enable	0: Input current limit is set by REG0x3F. 1: Input current limit is set by the lower value of ILIM pin and REG0x3F. <default at="" por=""></default>
[6]	[6]	IBAT Output Select	0: IBAT pin as discharge current. <default at="" por=""> 1: IBAT pin as charge current.</default>
[5:0]	[5:0]	Reserved	0- Reserved

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8.6.4 ProchotOption0 Register

Figure 19. ProchotOption0 Register (0x3CH)

15	14	13	12	11	10	9	8
	ICRI ⁻	Γ Comparator Thres	ICRIT Comparator Deglitch Time		Input OCP Threshold		
		R/W			R	/W	R/W
7	6	5	4	3	2	1	0
VSYS compa	rator threshold	PROCHOT Pulse Extension Enable	PROCHOT	Pulse Width	PROCHOT Host Clear	INOM Comparator Deglitch Time	Reserved
	R/W	•	R/	W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. ProchotOption0 Register (0x3CH)

I2C 05H	12C 04H	SMBus 0x3CH	BIT NAME	DESCRIPTION			
[7:3]		[15:11]	ICRIT Comparator Threshold	5 bits, percentage of IDPM in 0x3FH. Measure current between ACP and ACN. Trigger when the current is above this threshold.			
				Step: 5%, Default 150% (01001) 00000:110% 00001:110% 00010:115% 00011:120% 10111:220% 11000:225% 11001:230% 11010:250% 11011:300% 11100:350% 11101:400% 11110:450% 11111:Out of Range			
				If IDPM setting exceeds 3.584A (0111000), ICRIT threshold is clamped at 230%.			
[2:1]		[10:9]	ICRIT Comparator Deglitch Time	00: 10 μs 01: 100 μs <default at="" por=""></default> 10: 400 μs 11: 800 μs			
[0]		[8]	Input OCP Threshold	Input over-current setting by detecting ACP-ACN. 0: 125% of ICRIT 1: 200% of ICRIT <default at="" por=""></default>			
	[7:6]	[7:6]	VSYS comparator threshold	Measure on SRP with fixed 20us deglitch time. Trigger when SRP voltage is below the threshold. 00: 5.75 V (2-4s) or 2.85 V (1s) 01: 6V (2-4s) or 3.1V (1s) <default at="" por=""> 10: 6.25 V (2-4s) or 3.3 5V (1s) 11: 6.5 V (2-4s) or 3.6 V (1s)</default>			
	[5]	[5]	PROCHOT Pulse Extension Enable	When pulse extension is enabled, keep PROCHOT pin voltage low until host writes 0x3C[2]=1. 0: Pulse width is set by REG0x3C[4:3] <default at="" por=""> 1: Pulse stays LOW till host sets REG0x3C[2] to 0.</default>			
	[4:3]	[4:3]	PROCHOT Pulse Width	Minimum PROCHOT pulse width when REG0x3C[5]=0 00: 100 μs 01: 1 ms 10: 12 ms <default at="" por=""> 11: 6 ms</default>			
	[2]	[2]	PROCHOT Host Clear	Clear PROCHOT pulse when REG0x3C[5]=1. 0: Clear PROCHOT pulse and drive /PROCHOT pin to HIGH. 1: Idle <default at="" por=""></default>			
	[1]	[1]	INOM Comparator Deglitch Time	INOM is always 10% above IDPM in 0x3FH. Measure current between ACP and ACN. Trigger when the current is above this threshold. 0: 1ms max <default at="" por=""> 1: 50 ms max</default>			
	[0]	[0]	Reserved	0- Reserved			

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8.6.5 ProchotOption1 Register

Figure 20. ProchotOption1 Register (0x3DH)

15	14	13	12	11	10	9	8
		IDCHG Compa	arator Deglitch me				
		R/	W				
7	6	5	4	3	2	1	0
Reserved		PROCHOT envelop selector					
R		R/W					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. ProchotOption1 Register (0x3DH)

12C 07H	12C 06H	SMBus 0x3DH	BIT NAME	DESCRIPTION	
[7:2]		[15:10]	IDCHG Comparator Threshold	6 bit, range, range 0A – 32256 mA, step 512 mA. Measure current between SRN and SRP. Trigger when the discharge current is above the threshold. Default: 16384 mA (100000)	
[1:0]		[9:8]	IDCHG Comparator Deglitch Time	00: 1.6 ms 01: 100 μs <default at="" por=""> 10: 6 ms 11: 12 ms</default>	
	[7]	[7]	Reserved	0- Reserved	
	[6:0]	[6:0]	PROCHOT envelop selector	When adapter is present, the /PROCHOT function is enabled by the below bits. When adapter is removed, ICRIT, INOM, BATPRES and ACOK functions are automatically disabled in the PROCHOT profile. Comparator, IBAT and VSYS function setting are preserved. When all the bits are 0, PROCHOT function is disabled. Bit6: Independent comparator, 0: disable <default at="" por="">; 1: enable Bit5: ICRIT, 0: disable; 1: enable <default at="" por=""> Bit4: INOM, 0: disable <default at="" por="">; 1: enable Bit3: IDCHG, 0: disable <default at="" por="">; 1: enable Bit2: VSYS, 0: disable; 1: enable <default at="" por=""> Bit1: BATPRES, 0: disable <default at="" por="">; 1: enable (one-shot rising edge triggered) Bit0: ACOK, 0: disable <default at="" por="">; 1: enable (one-shot falling edge triggered)</default></default></default></default></default></default></default>	

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8.6.6 Setting the Charge Current

To set the charge current, write a 16-bit ChargeCurrent() command. With $10m\Omega$ sense resistor, the bq2477x provides charge current range of 128mA to 8.128A, with 64mA step resolution. It is suggested to write battery voltage to MaxChargeVoltage() before programming ChargeCurrent(). When battery is absent, the host should write 0A to ChargeCurrent().

During pre-charge, the charge current is clamped at 384mA. Sending ChargeCurrent() 0mA will terminate charge. Upon POR, charge current setting is 0mA.

For 1s charging, the charge current is clamped at 384 mA when battery is below BATLOWV threshold. When battery is between BATLOWV and SYSMIN, the charging current is clamped at 2 A. When battery is above SYSMIN, the charging current follows register setting.

To program charge current in bq24773, the host has to write 2-byte command with REG0A first, followed by REG0B. No other command can be inserted in between. After the completion of REG0A and REG0B, charge current will be updated. If host writes REG0B first, the command will be ignored. If the time between write of REG0A and REG0B exceeds watchdog timer, the REG0A command will be ignored.

The SRP and SRN pins are used to sense voltage drop across R_{SR} with default value of $10m\Omega$. For a larger sense resistor, a larger sense voltage is given, and a higher regulation accuracy; but at the expense of higher conduction loss. A current sensing resistor value no more than $20m\Omega$ is suggested.

A $0.1\mu F$ capacitor between SRP and SRN for differential mode filtering is recommended; a $0.1\mu F$ capacitor between SRN and ground, and an optional $0.1\mu F$ capacitor between SRP and ground for common mode filtering. Meanwhile, the capacitance on SRP should not be higher than $0.1\mu F$ in order to properly sense voltage across SRP and SRN.

Table 10. Charge Current Register with $10m\Omega$ Sense Resistor

I2C 0BH	I2C 0AH	SMBus 0x14H	BIT NAME	DESCRIPTION
	0	0	_	Not used. Value ignored.
	1	1	_	Not used. Value ignored.
	2	2	_	Not used. Value ignored.
	3	3	_	Not used. Value ignored.
	4	4	_	Not used. Value ignored.
	5	5	_	Not used. Value ignored.
	6	6	Charge Current, DACICHG 0	0 = Adds 0mA of charger current. 1 = Adds 64mA of charger current.
	7	7	Charge Current, DACICHG 1	0 = Adds 0mA of charger current. 1 = Adds 128mA of charger current.
0		8	Charge Current, DACICHG 2	0 = Adds 0mA of charger current. 1 = Adds 256mA of charger current.
1		9	Charge Current, DACICHG 3	0 = Adds 0mA of charger current. 1 = Adds 512mA of charger current.
2		10	Charge Current, DACICHG 4	0 = Adds 0mA of charger current. 1 = Adds 1024mA of charger current.
3		11	Charge Current, DACICHG 5	0 = Adds 0mA of charger current. 1 = Adds 2048mA of charger current.
4		12	Charge Current, DACICHG 6	0 = Adds 0mA of charger current. 1 = Adds 4096mA of charger current.
5		13		Not used. 1 = invalid write.
6		14	-	Not used. 1 = invalid write.
7		15	_	Not used. 1 = invalid write.

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8.6.7 Setting the Maximum Charge Voltage

To set the output charge regulation voltage, write a 16-bit MaxChargeVoltage() command. The bq2477x provides charge voltage range from 1.024V to 19.200V, with 16mV step resolution. Upon POR or when charge is disabled, the system is regulated at MaxChargeVoltage().

If enable charge without writing any command to MaxChargeVoltage(), the MaxChargeVoltage() is automatically changed to 4.2V/cell. If disable charge without writing any command to MaxChargeVoltage(), the MaxChargeVoltage() automatically goes back to POR value. Once writing a valid value to MaxChargeVoltage(), the register doesn't automatically change between charge enable and disable.

The BAT pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery pack positive side as possible. A decoupling capacitor of 0.1µF is recommended as close to IC as possible to decouple high frequency noise.

To program charge voltage in bq24773, the host has to write 2-byte command with REG0C first, followed by REG0D. No other command can be inserted in between. After the completion of REG0C and REG0D, charge voltage will be updated. If host writes REG0D first, the command will be ignored. If the time between write of REG0C and REG0D exceeds watchdog timer, the REG0C command will be ignored.

Table 11. Max Charge Voltage Register

I2C 0DH	I2C 0CH	SMBus REG 0x15H	BIT NAME	DESCRIPTION
	0	0	ı	Not used. Value ignored.
	1	1	-	Not used. Value ignored.
	2	2	-	Not used. Value ignored.
	3	3	_	Not used. Value ignored.
	4	4	Charge Voltage, DACV 0	0 = Adds 0mV of charger voltage. 1 = Adds 16mV of charger voltage.
	5	5	Charge Voltage, DACV 1	0 = Adds 0mV of charger voltage. 1 = Adds 32mV of charger voltage.
	6	6	Charge Voltage, DACV 2	0 = Adds 0mV of charger voltage. 1 = Adds 64mV of charger voltage.
	7	7	Charge Voltage, DACV 3	0 = Adds 0mV of charger voltage. 1 = Adds 128mV of charger voltage.
0		8	Charge Voltage, DACV 4	0 = Adds 0mV of charger voltage. 1 = Adds 256mV of charger voltage.
1		9	Charge Voltage, DACV 5	0 = Adds 0mV of charger voltage. 1 = Adds 512mV of charger voltage.
2		10	Charge Voltage, DACV 6	0 = Adds 0mV of charger voltage. 1 = Adds 1024mV of charger voltage.
3		11	Charge Voltage, DACV 7	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
4		12	Charge Voltage, DACV 8	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
5		13	Charge Voltage, DACV 9	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
6		14	Charge Voltage, DACV 10	0 = Adds 0mV of charger voltage. 1 = Adds 16384mV of charger voltage.
7		15	-	Not used. 1 = invalid write.



8.6.8 Setting the Minimum Charge Voltage

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. When charge is enabled, and the battery is below MinSystemVoltage(), the system is regulated at the minimum system voltage setting. When charge is disabled, the system is regulated at MaxChargeVoltage().

To set the minimum system voltage, write a 16-bit MinSystemVoltage() command. The bq2477x provides minimum system voltage range from 1.024V to 19.200V, with 256mV step resolution.

Table 12. Minimum System Voltage Register

I2C 0EH	SMBus 0x3EH	BIT NAME	DESCRIPTION
	0	-	Not used. Value ignored.
	1	-	Not used. Value ignored.
	2	-	Not used. Value ignored.
	3	-	Not used. Value ignored.
	4	-	Not used. Value ignored.
	5	-	Not used. Value ignored.
	6	-	Not used. Value ignored.
	7	-	Not used. Value ignored.
0	8	Minimum System Voltage, DACMINSV 0	0 = Adds 0mV of system Voltage. 1 = Adds 256mV of system Voltage.
1	9	Minimum System Voltage, DACMINSV 1	0 = Adds 0mV of system Voltage. 1 = Adds 512mV of system Voltage.
2	10	Minimum System Voltage, DACMINSV 2	0 = Adds 0mV of system Voltage. 1 = Adds 1024mV of system Voltage.
3	11	Minimum System Voltage, DACMINSV 3	0 = Adds 0mV of system Voltage. 1 = Adds 2048mV of system Voltage.
4	12	Minimum System Voltage, DACMINSV 4	0 = Adds 0mV of system Voltage. 1 = Adds 4096mV of system Voltage.
5	13	Minimum System Voltage, DACMINSV 5	0 = Adds 0mV of system Voltage. 1 = Adds 8192mV of system Voltage.
6	14	-	Not used. 1 = invalid write.
7	15	-	Not used. 1 = invalid write.

Table 13. Default MaxChargeVoltage and System Voltage

NUMBER of CELLs	MaxChargeVoltage()		Min System Voltage()
	Charge Enable	Charge Disable	MinSystemVoltage()
1S (CELL=GND)	4.192V	4.400V	3.584V
2S (CELL=FLOAT)	8.400V	9.008V	6.144V
3S/4S (CELL=High)	12.592V	13.500V	9.216V



8.6.9 Setting Input Current

Normally, input power source powers system and charges battery. With AC wall adapter output current can be regulated to save system cost.

To set the input current limit, write a 16-bit InputCurrent() command. When using a $10m\Omega$ sense resistor, the bq2477x provides an input-current limit range of 128mA to 8.128A, with 64mA resolution. Upon POR, default input current limit is 3.2A (770) or 2.944A (773).

The ACP and ACN pins are used to sense $R_{(AC)}$ with default value of $10m\Omega$. However, resistors of other values can also be used. For a larger sense resistor, larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss.

Table 14. Input Current Register using $10m\Omega$ sense resistor

I2C 0FH	SMBus REG 0x3FH	BIT NAME	DESCRIPTION	
	0	-	Not used. Value ignored.	
	1	-	Not used. Value ignored.	
	2	-	Not used. Value ignored.	
	3	-	Not used. Value ignored.	
	4	-	Not used. Value ignored.	
	5	-	Not used. Value ignored.	
0	6	Input Current, DACIIN 0	0 = Adds 0mA of input current. 1 = Adds 64mA of input current.	
1	7	Input Current, DACIIN 1	0 = Adds 0mA of input current. 1 = Adds 128mA of input current.	
2	8	Input Current, DACIIN 2	0 = Adds 0mA of input current. 1 = Adds 256mA of input current.	
3	9	Input Current, DACIIN 3	0 = Adds 0mA of input current. 1 = Adds 512mA of input current.	
4	10	Input Current, DACIIN 4	0 = Adds 0mA of input current. 1 = Adds 1024mA of input current.	
5	11	Input Current, DACIIN 5	0 = Adds 0mA of input current. 1 = Adds 2048mA of input current.	
6	12	Input Current, DACIIN 6	0 = Adds 0mA of input current. 1 = Adds 4096mA of input current.	
7	13	-	Not used. 1 = invalid write.	
	14	-	Not used. 1 = invalid write.	
	15	-	Not used. 1 = invalid write.	



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq2477xEVM-540 evaluation module (EVM) is a complete charger module for evaluating the bq2477x. The application curves were taken using the bq24770EVM-540. Refer to the EVM user's guide (SLUUAO3) for EVM information.

9.2 Typical Application, bq24770

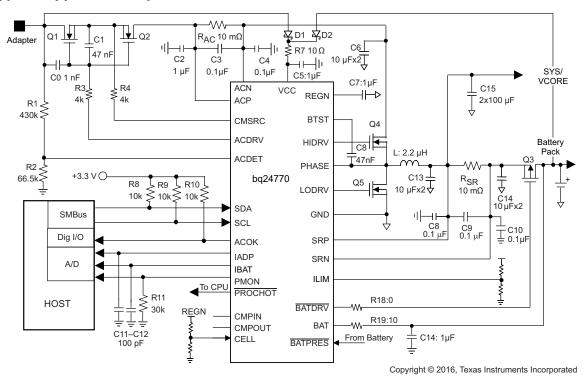


Figure 21. bq24770 Application Schematic

9.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE	
Input Voltage ⁽¹⁾	17.7V < Adapter Voltage < 24V	
Input Current Limit (1)	3.2A for 65W adapter	
Battery Charge Voltage (2)	8400mV for 2s battery	
Battery Charge Current (2)	4096mA for 3s battery	
Minimum System Voltage (2)	6144mA for 2s battery	

- (1) Refer to adapter specification for settings for Input Voltage and Input Current Limit.
- Refer to battery specification for settings.



9.2.2 Detailed Design Procedure

The parameters are configurable using the evaluation software.

The simplified application circuit (see Figure 21) shows the minimum capacitance requirements for each pin. Inductor, capacitor, and MOSFET selection are explained in the rest of this section. Refer to the EVM user's guide (SLUUAO3) for the full application schematic.

9.2.2.1 Reverse Input Voltage Protection

Q6, R12, and R13 in Figure 22 give system and IC protection from reversed adapter voltage. In normal operation, Q6 is turned off by negative Vgs. When adapter voltage is reversed, Q6 Vgs is positive. As a result, Q6 turns on to short gate and source of Q2 so that Q2 is off. Q2 body diode blocks negative voltage to system. However, CMSRC and ACDRV pins need R3 and R4 to limit the current due to the ESD diode of these pins when turned on. Q6 must has low Vgs threshold voltage and low Qgs gate charge so it turns on before Q2 turns on. R3 and R4 must have enough power rating for the power dissipation when the ESD diode is on. If Q1 is replaced by Schottky diode for reverse adapter voltage protection, no extra small MOSFET and resistors are needed.

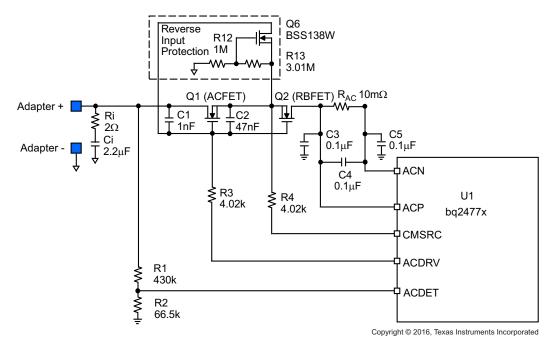


Figure 22. Reverse Input Voltage Protection Circuit

9.2.2.2 Inductor Selection

The bq2477x has three selectable fixed switching frequency. Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \ge I_{CHG} + (1/2)I_{RIPPLE}$$
 (2)

The inductor ripple current depends on input voltage (V_{IN}) , duty cycle $(D = V_{OUT}/V_{IN})$, switching frequency (f_S) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{f_{S} \times L}$$
(3)

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9V to 12.6V for 3-cell battery pack. For 20 V adapter voltage, 10 V battery voltage gives the maximum inductor ripple current. Another example is 4-cell battery, the battery voltage range is from 12 V to 16.8 V, and 12 V battery voltage gives the maximum inductor ripple current.

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Usually inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.2.3 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by Equation 4:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)}$$
(4)

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25 V rating or higher capacitor is preferred for 19-20 V input voltage. 10-20 μ F capacitance is suggested for typical of 3-4 A charging current.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's datasheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

9.2.2.4 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE}$$
 (5)

The bq2477x has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 10 kHz and 20 kHz. The preferred ceramic capacitor is 25V X7R or X5R for output capacitor. 10-20μF capacitance is suggested for a typical of 3-4A charging current. Place the capacitors after charging current sensing resistor to get the best charge current regulation accuracy.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

9.2.2.5 Power MOSFETs Selection

Two external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6V of gate drive voltage. 30 V or higher voltage rating MOSFETs are preferred for 19-20 V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For the top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD} . For the bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_{G} .

$$FOM_{top} = R_{DS(on)} \times Q_{GD}; FOM_{bottom} = R_{DS(on)} \times Q_{G}$$
(6)

The lower the FOM value, the lower the total power loss. Usually lower R_{DS(ON)} has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle $(D=V_{OUT}/V_{IN})$, charging current (I_{CHG}) , MOSFET's on-resistance $(R_{DS(ON)})$, input voltage (V_{IN}) , switching frequency (f_S) , turn on time (t_{on}) and turn off time (t_{off}) :

$$P_{\text{top}} = D \times I_{\text{CHG}}^2 \times R_{\text{DS(on)}} + \frac{1}{2} \times V_{\text{IN}} \times I_{\text{CHG}} \times (t_{\text{on}} + t_{\text{off}}) \times f_{\text{s}}$$
(7)

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The first item represents the conduction loss. Usually MOSFET $R_{DS(ON)}$ increases by 50% with 100°C junction temperature rise. The second term represents the switching loss. The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \quad t_{off} = \frac{Q_{SW}}{I_{off}}$$
(8)

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current and I_{off} is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}) :

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS}$$
 (9)

Gate driving current can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (R_{on}) and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}}$$
(10)

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous conduction mode:

$$P_{\text{bottom}} = (1 - D) \times I_{\text{CHG}}^2 \times R_{\text{DS(on)}}$$

$$(11)$$

When charger operates in non-synchronous mode, the bottom-side MOSFET is off. As a result all the freewheeling current goes through the body-diode of the bottom-side MOSFET. The body diode power loss depends on its forward voltage drop (V_F) , non-synchronous mode charging current $(I_{NONSYNC})$, and duty cycle (D).

$$P_D = V_F \times I_{NONSYNC} \times (1 - D)$$
 (12)

The maximum charging current in non-synchronous mode can be up to 0.25 A for a 10 m Ω charging current sensing resistor or 0.5 A if battery voltage is below 2.5 V. The minimum duty cycle happens at lowest battery voltage. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

9.2.2.6 Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second order system. The voltage spike at VCC pin maybe beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent over voltage event on VCC pin.

There are several methods to damping or limit the over voltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over voltage level to an IC safe level. However these two solutions may not have low cost or small size.

A cost effective and small size solution is shown in Figure 23. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result the over voltage spike is limited to a safe level. D1 is used for reverse voltage protection for VCC pin. C2 is VCC pin decoupling capacitor and it should be place to VCC pin as close as possible. C2 value should be less than C1 value so R1 can dominant the equivalent ESR value to get enough damping effect. R2 is used to limit inrush current of D1 to prevent D1 getting damage when adapter hot plug-in. R2 and C2 should have 10 µs time constant to limit the dv/dt on VCC pin to reduce inrush current when adapter hot plug in. R1 has high inrush current. R1 package must be sized enough to handle inrush current power loss according to resistor manufacturer's data sheet. The filter components value always need to be verified with real application and minor adjustments may need to fit in the real application circuit.

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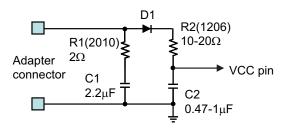
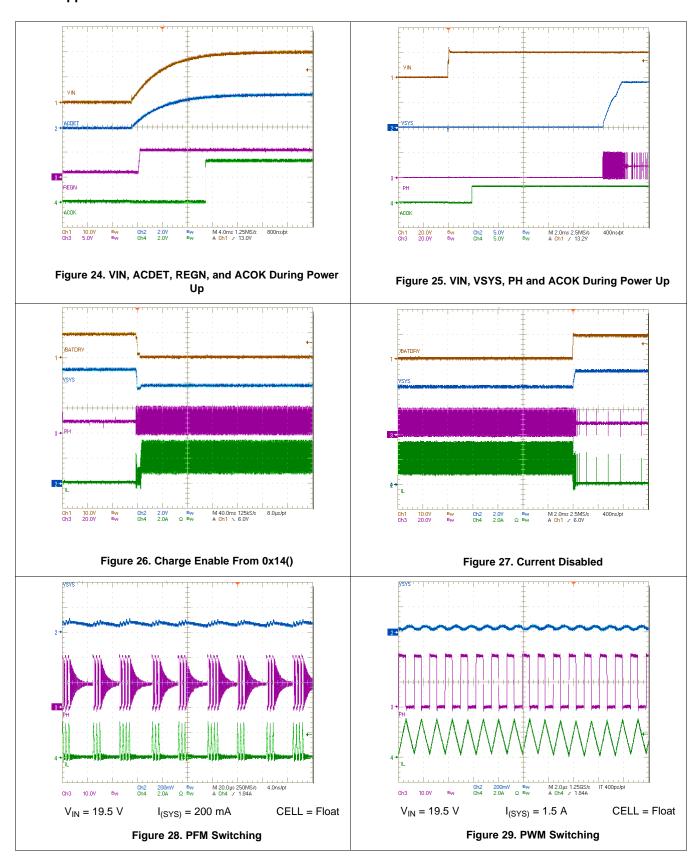


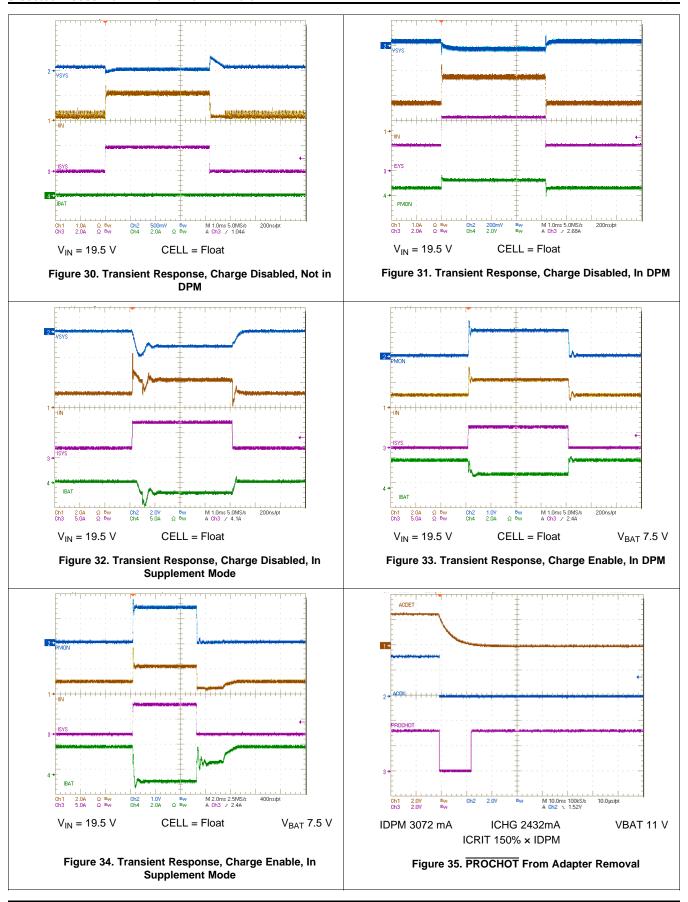
Figure 23. Input Filter



9.2.3 Application Curves









9.2.4 Typical Application, bq24773

The bq2477xEVM-540 evaluation module (EVM) is a complete charger module for evaluating the bq2477x. The application curves were taken using the bq24770EVM-540. Refer to the EVM user's guide (SLUUAO3) for EVM information.

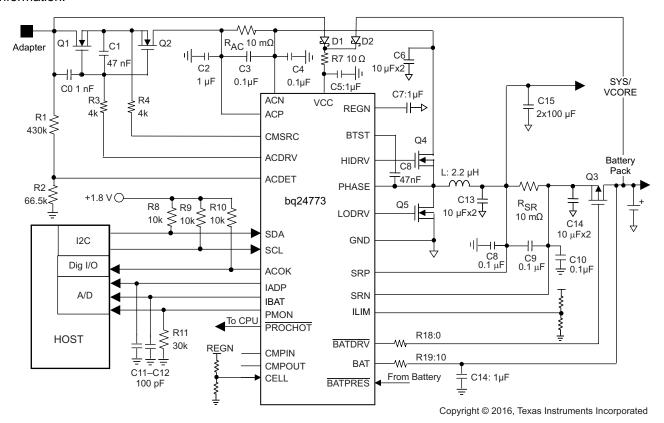


Figure 36. bq24773 Typical Schematic

9.2.4.1 Design Requirements

Refer to Typical Application, bq24770 for the Design Requirements.

9.2.4.2 Detailed Design Procedure

Refer to Typical Application, bq24770 for the Detailed Design Procedure.

9.2.4.3 Application Curves

Refer to Typical Application, bq24770 for the Application Curves.



10 Power Supply Recommendations

When adapter is attached, and ACOK goes HIGH, the system is connected to adapter through ACFET/RBFET. An external resistor voltage divider attenuates the adapter voltage before it goes to ACDET. The adapter detect threshold should typically be programmed to a value greater than the maximum battery voltage, but lower than the IC maximum allowed input voltage (ACOVP) and system maximum allowed voltage.

When adapter is removed, the system is connected to battery through BATFET. Typically the battery depletion threshold should be greater than the minimum system voltage so that the battery capacity can be fully utilized for maximum battery life.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 37) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Layout of the PCB according to this specific order is essential.

- Place input capacitor as close as possible to switching MOSFET's supply and ground connections and use shortest copper trace connection. These parts should be placed on the same layer of PCB instead of on different layers and using vias to make this connection.
- The IC should be placed close to the switching MOSFET's gate pins and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of switching MOSFETs.
- Place inductor input pin to switching MOSFET's output pin as close as possible. Minimize the copper area of
 this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging
 current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this
 area to any other trace or plane.
- The charging current sensing resistor should be placed right next to the inductor output. Route the sense
 leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop
 area) and do not route the sense leads through a high-current path (see Figure 38 for Kelvin connection for
 best current accuracy). Place decoupling capacitor on these traces next to the IC
- Place output capacitor next to the sensing resistor output and ground
- Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
- Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling
- Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground (power pad should tie to analog ground in this case if possible).
- Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible
- It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground.
 Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
- The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the WQFN information, See SCBA017 and SLUA271.

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11.2 Layout Example

11.2.1 Layout Consideration of Current Path

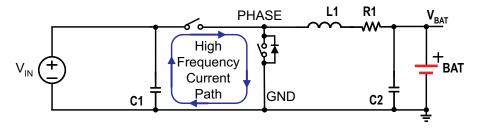


Figure 37. High Frequency Current Path

11.2.2 Layout Consideration of Short Circuit Protection

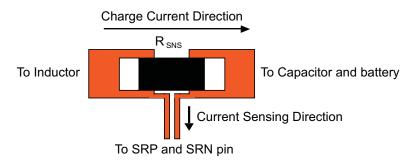


Figure 38. Sensing Resistor PCB Layout



12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 15. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
bq24770	Click here	Click here	Click here	Click here	Click here	
bq24773	Click here	Click here	Click here	Click here	Click here	

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: bq24770 bq24773

www.ti.com

14-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
BQ24770RUYR	Active	Production	WQFN (RUY) 28	3000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 85	BQ 24770
BQ24770RUYR.A	Active	Production	WQFN (RUY) 28	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24770
BQ24770RUYR.B	Active	Production	WQFN (RUY) 28	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24770
BQ24770RUYT	Active	Production	WQFN (RUY) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24770
BQ24770RUYT.A	Active	Production	WQFN (RUY) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24770
BQ24770RUYT.B	Active	Production	WQFN (RUY) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24770
BQ24773RUYR	Active	Production	WQFN (RUY) 28	3000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 85	BQ 24773
BQ24773RUYR.A	Active	Production	WQFN (RUY) 28	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24773
BQ24773RUYR.B	Active	Production	WQFN (RUY) 28	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24773
BQ24773RUYT	Active	Production	WQFN (RUY) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24773
BQ24773RUYT.A	Active	Production	WQFN (RUY) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24773
BQ24773RUYTG4	Active	Production	WQFN (RUY) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24773
BQ24773RUYTG4.A	Active	Production	WQFN (RUY) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24773

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



PACKAGE OPTION ADDENDUM

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- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS WHO WE PI WHO WE PI WHO WE BO WE Cavity AO WE Cavity AO WE Cavity

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24770RUYR	WQFN	RUY	28	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24770RUYT	WQFN	RUY	28	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24773RUYR	WQFN	RUY	28	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24773RUYT	WQFN	RUY	28	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24773RUYTG4	WQFN	RUY	28	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2



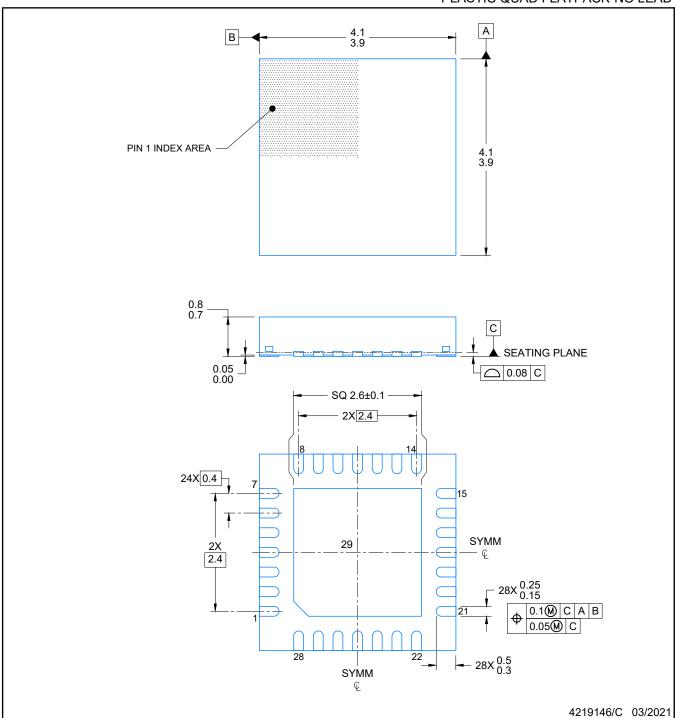
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*All dimensions are nominal

7 till dillitorioriorio di o mominidi							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24770RUYR	WQFN	RUY	28	3000	346.0	346.0	33.0
BQ24770RUYT	WQFN	RUY	28	250	210.0	185.0	35.0
BQ24773RUYR	WQFN	RUY	28	3000	346.0	346.0	33.0
BQ24773RUYT	WQFN	RUY	28	250	210.0	185.0	35.0
BQ24773RUYTG4	WQFN	RUY	28	250	210.0	185.0	35.0

PLASTIC QUAD FLATPACK-NO LEAD

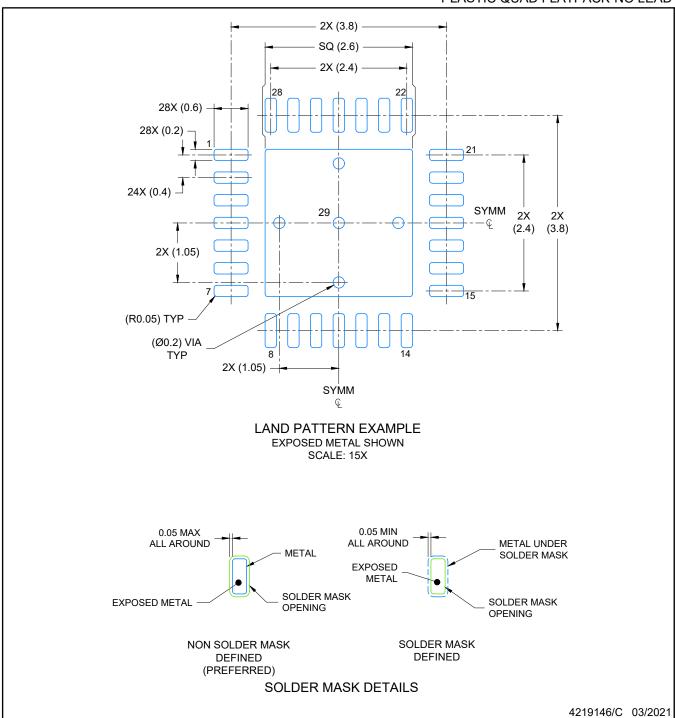


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLATPACK-NO LEAD

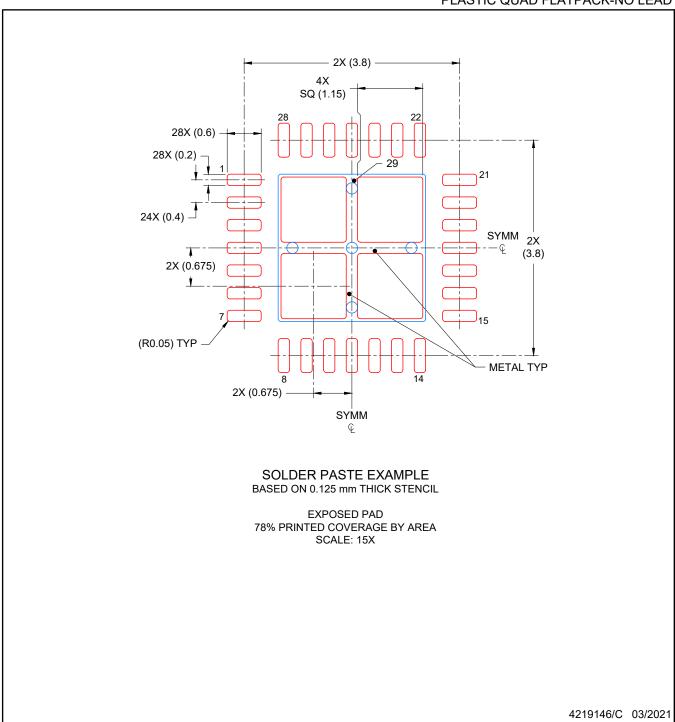


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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