

## NiCd/NiMH Fast-Charge Management ICs

### Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge status
- Fast-charge termination by rate of rise of temperature, maximum voltage, maximum temperature, and maximum time
- Internal band-gap voltage reference
- Optional top-off charge (bq2002T only)
- Selectable pulse-trickle charge rates (bq2002T only)
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

### General Description

The bq2002D/T Fast-Charge IC are low-cost CMOS battery-charge controllers able to provide reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002D/T to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002D/T integrates fast charge with optional top-off and pulsed-trickle control in a single IC for charging one or more NiCd or NiMH battery cells.

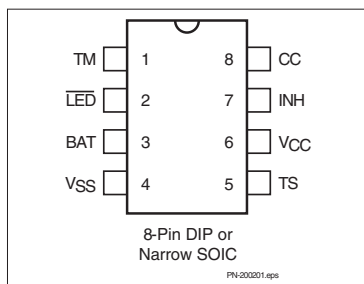
Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

Fast charge is terminated by any of the following:

- Rate of temperature rise
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, the bq2002T optionally tops-off and pulse-trickles the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002D/T may be placed in low-standby-power mode to reduce system power consumption.

### Pin Connections



### Pin Names

|                 |                         |                 |                         |
|-----------------|-------------------------|-----------------|-------------------------|
| TM              | Timer mode select input | TS              | Temperature sense input |
| LED             | Charging status output  | V <sub>CC</sub> | Supply voltage input    |
| BAT             | Battery voltage input   | INH             | Charge inhibit input    |
| V <sub>SS</sub> | System ground           | CC              | Charge control output   |

### bq2002D/T Selection Guide

| Part No. | TCO                     | HTF                    | LTF                   | Fast Charge | Time-Out | Top-Off | Maintenance |
|----------|-------------------------|------------------------|-----------------------|-------------|----------|---------|-------------|
| bq2002D  | 0.225 * V <sub>CC</sub> | 0.25 * V <sub>CC</sub> | None                  | C/4         | 440 min  | None    | None        |
|          |                         |                        |                       | 1C          | 110 min  | None    | None        |
|          |                         |                        |                       | 2C          | 55 min   | None    | None        |
| bq2002T  | 0.225 * V <sub>CC</sub> | 0.25 * V <sub>CC</sub> | 0.4 * V <sub>CC</sub> | C/4         | 320 min  | C/64    | C/256       |
|          |                         |                        |                       | 1C          | 80 min   | C/16    | C/256       |
|          |                         |                        |                       | 2C          | 40 min   | None    | C/128       |

# bq2002D/T

## Pin Descriptions

|            |  |
|------------|--|
| <b>TM</b>  | <b>Timer mode input</b>  |
|            | A three-level input that controls the settings for the fast charge safety timer, voltage termination mode, top-off, pulse-trickle, and voltage hold-off time.                        |
| <b>LED</b> | <b>Charging output status</b>  |
|            | Open-drain output that indicates the charging status.  |
| <b>BAT</b> | <b>Battery input voltage</b>   |
|            | The battery voltage sense input. The input to this pin is created by a high-impedance resistor divider network connected between the positive and negative terminals of the battery. |
| <b>Vss</b> | <b>System ground</b>   |
| <b>TS</b>  | <b>Temperature sense input</b>   |
|            | Input for an external battery temperature monitoring thermistor.   |
| <b>Vcc</b> | <b>Supply voltage input</b>  |
|            | 5.0V ±20% power input.   |
| <b>INH</b> | <b>Charge inhibit input</b>  |
|            | When high, INH suspends the fast charge in progress. When returned low, the IC re-   |

sumes operation at the point where initially suspended.

## CC Charge control output

An open-drain output used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide top-off, if enabled, and pulse trickle.

## Functional Description

Figures 2 and 3 show state diagrams of bq2002D/T and Figure 4 shows the block diagram of the bq2002D/T.

## Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of

$$\frac{RB1}{RB2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

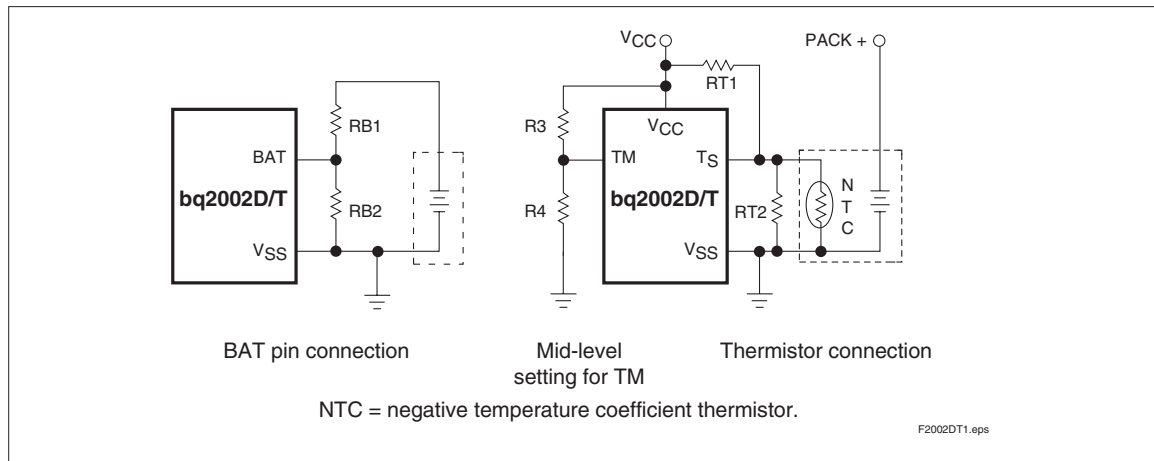


Figure 1. Voltage and Temperature Monitoring and TM Pin Configuration

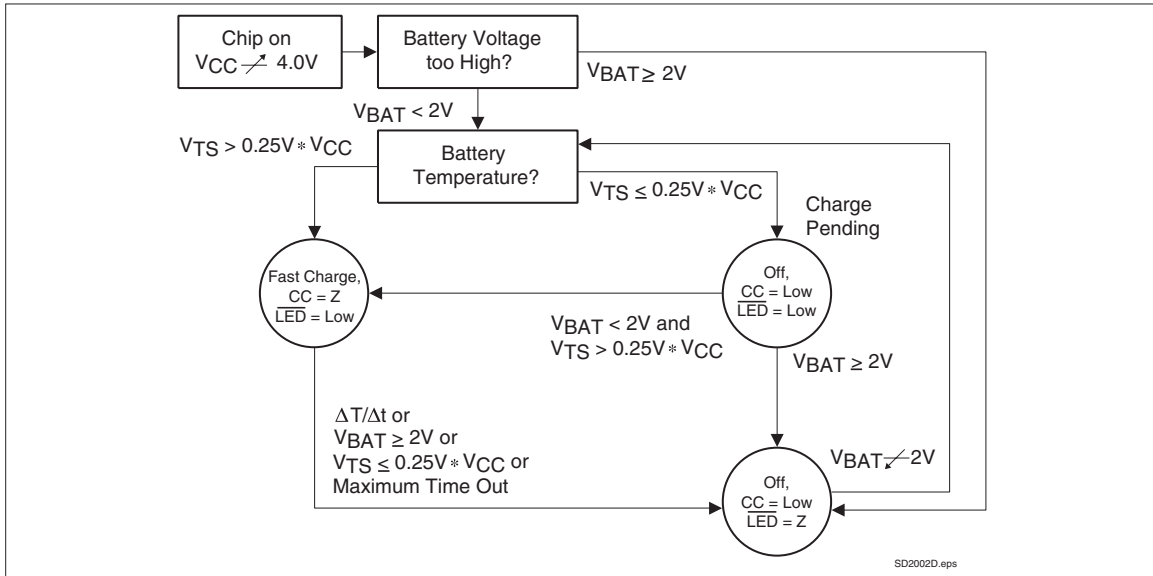


Figure 2. bq2002D State Diagram

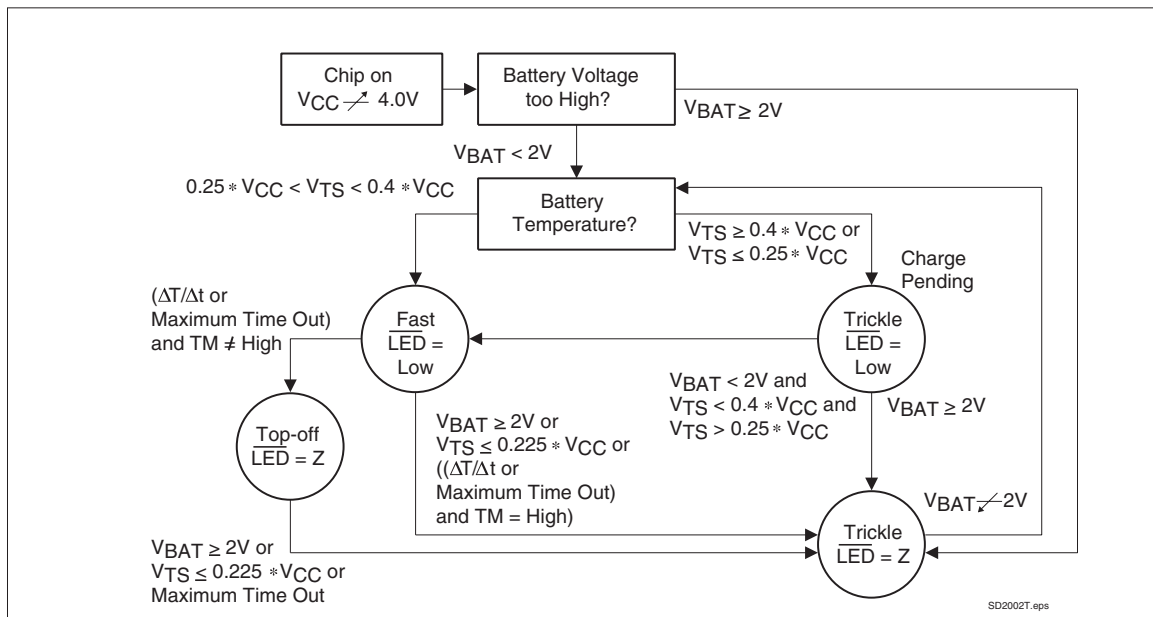


Figure 3. bq2002T State Diagram

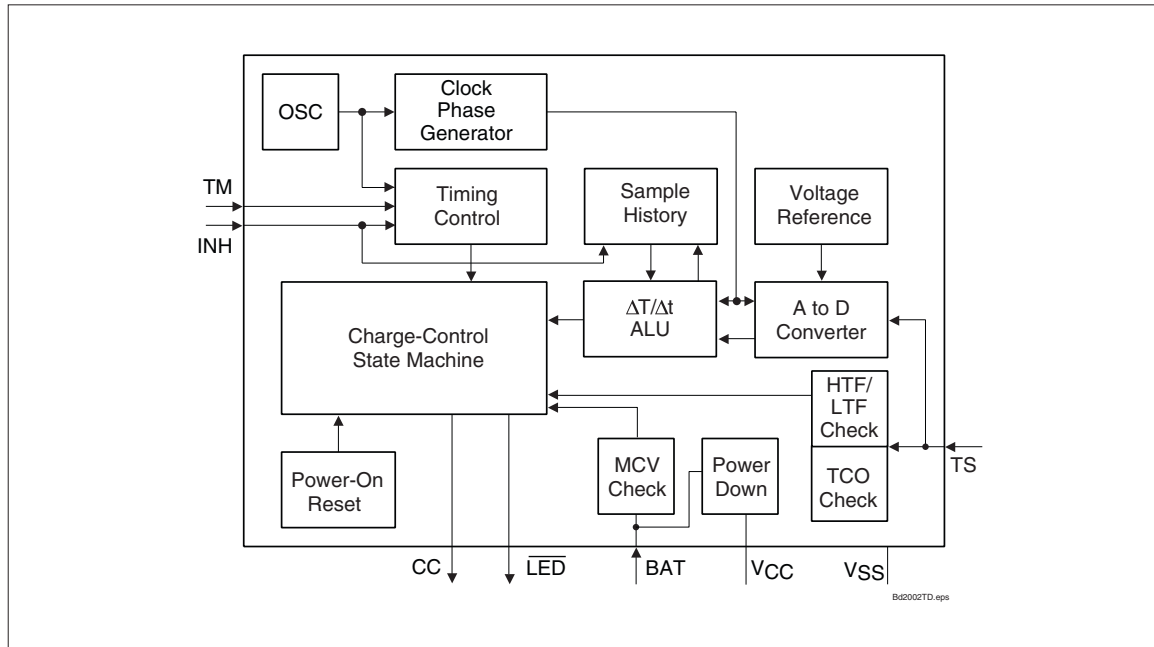


Figure 4. Block Diagram

**Note:** This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1 MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V<sub>CC</sub> and V<sub>SS</sub>. See Figure 1.

### Starting A Charge Cycle

Either of two events starts a charge cycle (see Figure 5):

1. Application of power to V<sub>CC</sub> or
2. Voltage at the BAT pin falling through the maximum cell voltage where

$$V_{MCV} = 2V \pm 5\%$$

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is  $V_{BAT} < V_{MCV}$ . The valid temperature range is  $V_{HTF} < V_{TS} < V_{LTF}$  for the bq2002T and  $V_{HTF} < V_{TS}$  for the bq2002D where

$$V_{LTF} = 0.4 * V_{CC} \pm 5\%$$

$$V_{HTF} = 0.25 * V_{CC} \pm 5\% \text{ (bq2002T only)}$$

If the battery voltage or temperature is outside of these limits, the IC pulse-trickle charges until the temperature falls within the allowed fast charge range or a new charge cycle is started.

Fast charge continues until termination by one or more of the four possible termination conditions:

- Rate of temperature rise
- Maximum voltage
- Maximum temperature
- Maximum time

### T/ t Termination

The bq2002D/T samples at the voltage at the TS pin every 19s and compares it to the value measured three samples earlier. If the voltage has fallen 25.6mV or more, fast charge is terminated. The  $\Delta T/\Delta t$  termination test is valid only when  $V_{TCO} < V_{TS} < V_{LTF}$  for the bq2002T and  $V_{TCO} < V_{TS}$  for the bq2002D.

### Temperature Sampling

A sample is taken by averaging together 16 measurements taken 570μs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This tech-

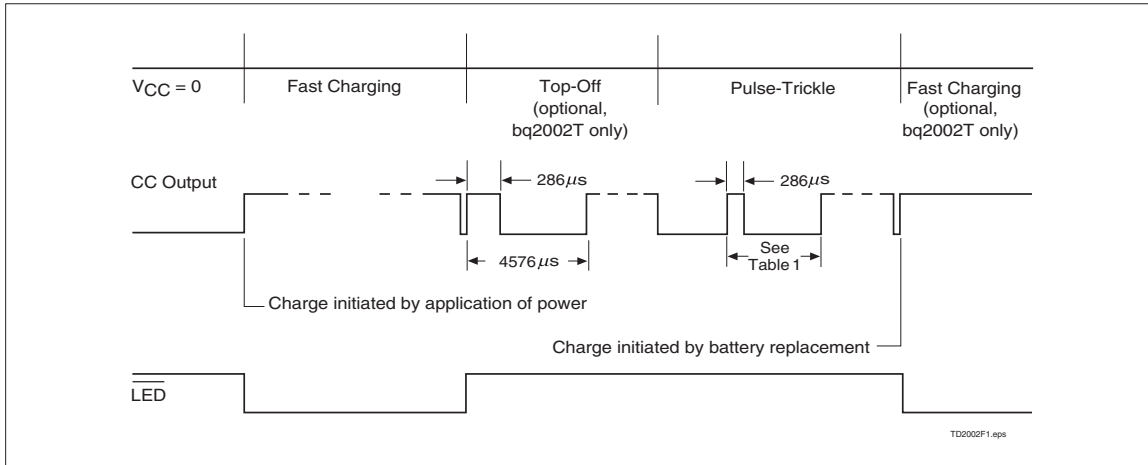


Figure 5. Charge Cycle Phases

nique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is  $\pm 20\%$ .

#### Maximum Voltage, Temperature, and Time

Any time the voltage on the BAT pin exceeds the maximum cell voltage,  $V_{MCV}$ , fast charge or optional top-off charge is terminated.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold  $V_{TCO}$  where

$$V_{TCO} = 0.225 * V_{CC} \pm 5\%$$

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and

Table 1. Fast-Charge Safety Time/Top-Off Table

| Part No. | Corresponding Fast-Charge Rate | TM   | Typical Fast-Charge and Top-Off Time Limits (minutes) | Top-Off Rate | Pulse-Trickle Rate | Pulse-Trickle Period (ms) |
|----------|--------------------------------|------|---|--------------|--------------------|---------------------------|
| bq2002D  | C/4                            | Mid  | 440   | None         | None               | None                      |
|          | 1C                             | Low  | 110   | None         | None               | None                      |
|          | 2C                             | High | 55  | None         | None               | None                      |
| bq2002T  | C/4                            | Mid  | 320   | C/64         | C/256              | 18.3                      |
|          | 1C                             | Low  | 80  | C/16         | C/256              | 73.1                      |
|          | 2C                             | High | 40  | None         | C/128              | 73.1                      |

**Notes:** Typical conditions =  $25^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V}$   
Mid =  $0.5 * V_{CC} \pm 0.5\text{V}$   
Tolerance on all timing is  $\pm 20\%$

## bq2002D/T

---

enforced again on the top-off phase, if selected (bq2002T only). There is no time limit on the trickle-charge phase.

### Top-off Charge—bq2002T Only

An optional top-off charge phase may be selected to follow fast charge termination for 1C and C/4 rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM pin. (See Table 1.) During top-off, the CC pin is modulated at a duty cycle of 286µs active for every 4290µs inactive. This modulation results in an average rate 1/16th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

### Pulse-Trickle Charge—bq2002T Only

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged by driving the CC pin active for a period of 286µs for every 72.9ms of inactivity for 1C and 2C selections, and 286µs for every 17.9ms of inactivity for C/4 selection. This results in a trickle rate of C/256 for the top-off enabled mode and C/128 otherwise.

### TM Pin

The TM pin is a three-level pin used to select the charge timer, top-off, voltage termination mode, trickle rate, and voltage hold-off period options. Table 1 describes the states selected by the TM pin. The mid-level selection input is developed by a resistor divider between V<sub>CC</sub> and ground that fixes the voltage on TM at V<sub>CC</sub>/2 ± 0.5V. See Figure 5.

### Charge Status Indication

In the fast charge and charge pending states, and whenever the inhibit pin is active, the  $\overline{\text{LED}}$  pin goes low. The  $\overline{\text{LED}}$  pin is driven to the high-Z state for all other conditions. Figure 3 outlines the state of the  $\overline{\text{LED}}$  pin during charge.

### Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin. When high, INH suspends all fast charge and top-off activity and the internal charge timer. INH freezes the current state of  $\overline{\text{LED}}$  until inhibit is removed. Temperature monitoring is not affected by the INH pin. During charge inhibit, the bq2002D/T continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH became active. The V<sub>TS</sub> sample history is cleared by INH.

### Low-Power Mode

The IC enters a low-power state when V<sub>BAT</sub> is driven above the power-down threshold (V<sub>PD</sub>) where

$$V_{PD} = V_{CC} - (1V \pm 0.5V)$$

Both the CC pin and the  $\overline{\text{LED}}$  pin are driven to the high-Z state. The operating current is reduced to less than 1µA in this mode. When V<sub>BAT</sub> returns to a value below V<sub>PD</sub>, the IC pulse-trickle charges until the next new charge cycle begins.

## Absolute Maximum Ratings

| Symbol              | Parameter   | Minimum | Maximum | Unit | Notes      |
|---------------------|---|---------|---------|------|------------|
| V <sub>CC</sub>     | V <sub>CC</sub> relative to V <sub>SS</sub>   | -0.3    | +7.0    | V    |            |
| V <sub>T</sub>      | DC voltage applied on any pin excluding V <sub>CC</sub> relative to V <sub>SS</sub> | -0.3    | +7.0    | V    |            |
| T <sub>OPR</sub>    | Operating ambient temperature   | 0       | +70     | °C   | Commercial |
| T <sub>STG</sub>    | Storage temperature   | -40     | +85     | °C   |            |
| T <sub>SOLDER</sub> | Soldering temperature   | -       | +260    | °C   | 10s max.   |
| T <sub>BIAS</sub>   | Temperature under bias  | -40     | +85     | °C   |            |

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## DC Thresholds (T<sub>A</sub> = 0 to 70°C; V<sub>CC</sub> ±20%)

| Symbol           | Parameter              | Rating                  | Tolerance | Unit | Notes  |
|------------------|------------------------|-------------------------|-----------|------|--|
| V <sub>TCO</sub> | Temperature cutoff     | 0.225 * V <sub>CC</sub> | ±5%       | V    | V <sub>TS</sub> ≤ V <sub>TCO</sub> terminates fast charge and top-off        |
| V <sub>HTF</sub> | High-temperature fault | 0.25 * V <sub>CC</sub>  | ±5%       | V    | V <sub>TS</sub> ≤ V <sub>HTF</sub> inhibits fast charge start                |
| V <sub>LTF</sub> | Low-temperature fault  | 0.4 * V <sub>CC</sub>   | ±5%       | V    | V <sub>TS</sub> ≥ V <sub>LTF</sub> inhibits fast charge start (bq2002T only) |
| V <sub>MCV</sub> | Maximum cell voltage   | 2                       | ±5%       | V    | V <sub>BAT</sub> ≥ V <sub>MCV</sub> inhibits/terminates fast charge          |

## bq2002D/T

### Recommended DC Operating Conditions (T<sub>A</sub> = 0 to 70°C)

| Symbol           | Condition                         | Minimum                  | Typical | Maximum                  | Unit | Notes   |
|------------------|-----------------------------------|--------------------------|---------|--------------------------|------|---|
| V <sub>CC</sub>  | Supply voltage                    | 4.0                      | 5.0     | 6.0                      | V    |   |
| V <sub>BAT</sub> | Battery input                     | 0                        | -       | V <sub>CC</sub>          | V    |   |
| V <sub>TS</sub>  | Thermistor input                  | 0.5                      | -       | V <sub>CC</sub>          | V    | V <sub>TS</sub> < 0.5V prohibited   |
| V <sub>IH</sub>  | Logic input high                  | 0.5                      | -       | -                        | V    | INH   |
|                  | Logic input high                  | V <sub>CC</sub> - 0.5    | -       | -                        | V    | TM  |
| V <sub>IM</sub>  | Logic input mid                   | $\frac{V_{CC}}{2} - 0.5$ | -       | $\frac{V_{CC}}{2} + 0.5$ | V    | TM  |
| V <sub>IL</sub>  | Logic input low                   | -                        | -       | 0.1                      | V    | INH   |
|                  | Logic input low                   | -                        | -       | 0.5                      | V    | TM  |
| V <sub>OL</sub>  | Logic output low                  | -                        | -       | 0.8                      | V    | $\overline{\text{LED}}$ , CC, I <sub>OL</sub> = 10mA  |
| V <sub>PD</sub>  | Power down                        | V <sub>CC</sub> - 1.5    | -       | V <sub>CC</sub> - 0.5    | V    | V <sub>BAT</sub> ≥ V <sub>PD</sub> max. powers down bq2002D/T;<br>V <sub>BAT</sub> < V <sub>PD</sub> min. = normal operation. |
| I <sub>CC</sub>  | Supply current                    | -                        | -       | 500                      | μA   | Outputs unloaded, V <sub>CC</sub> = 5.1V  |
| I <sub>SB</sub>  | Standby current                   | -                        | -       | 1                        | μA   | V <sub>CC</sub> = 5.1V, V <sub>BAT</sub> = V <sub>PD</sub>  |
| I <sub>OL</sub>  | $\overline{\text{LED}}$ , CC sink | 10                       | -       | -                        | mA   | @V <sub>OL</sub> = V <sub>SS</sub> + 0.8V   |
| I <sub>L</sub>   | Input leakage                     | -                        | -       | ±1                       | μA   | INH, CC, V = V <sub>SS</sub> to V <sub>CC</sub>   |
| I <sub>OZ</sub>  | Output leakage in high-Z state    | -5                       | -       | -                        | μA   | $\overline{\text{LED}}$ , CC  |

**Note:** All voltages relative to V<sub>SS</sub>.



## Impedance

| Symbol           | Parameter               | Minimum | Typical | Maximum | Unit |
|------------------|-------------------------|---------|---------|---------|------|
| R <sub>BAT</sub> | Battery input impedance | 50      | -       | -       | MΩ   |
| R <sub>TS</sub>  | TS input impedance      | 50      | -       | -       | MΩ   |

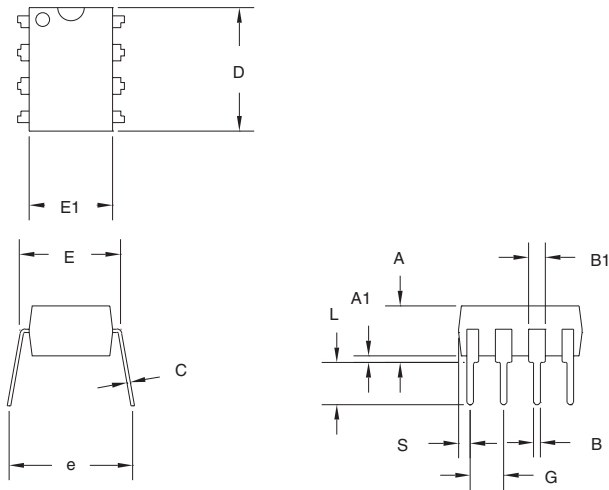
## Timing (T<sub>A</sub> = 0 to +70°C; V<sub>CC</sub> ±10%)

| Symbol           | Parameter           | Minimum | Typical | Maximum | Unit | Notes |
|------------------|---------------------|---------|---------|---------|------|-------|
| d <sub>FCV</sub> | Time-base variation | -20     | -       | 20      | %    |       |

**Note:** Typical is at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V.

## bq2002D/T

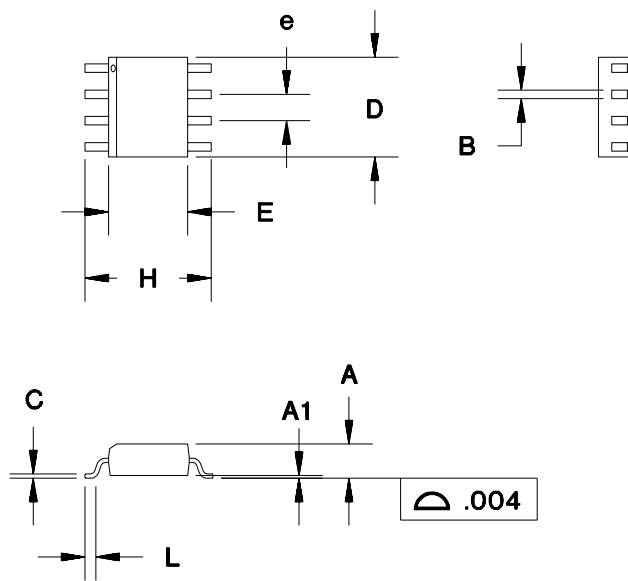
### 8-Pin DIP (PN)



#### 8-Pin PN (0.300" DIP)

| Dimension | Inches |       | Millimeters |      |
|-----------|--------|-------|-------------|------|
|           | Min.   | Max.  | Min.        | Max. |
| A         | 0.160  | 0.180 | 4.06        | 4.57 |
| A1        | 0.015  | 0.040 | 0.38        | 1.02 |
| B         | 0.015  | 0.022 | 0.38        | 0.56 |
| B1        | 0.055  | 0.065 | 1.40        | 1.65 |
| C         | 0.008  | 0.013 | 0.20        | 0.33 |
| D         | 0.350  | 0.380 | 8.89        | 9.65 |
| E         | 0.300  | 0.325 | 7.62        | 8.26 |
| E1        | 0.230  | 0.280 | 5.84        | 7.11 |
| e         | 0.300  | 0.370 | 7.62        | 9.40 |
| G         | 0.090  | 0.110 | 2.29        | 2.79 |
| L         | 0.115  | 0.150 | 2.92        | 3.81 |
| S         | 0.020  | 0.040 | 0.51        | 1.02 |

### 8-Pin SOIC Narrow (SN)

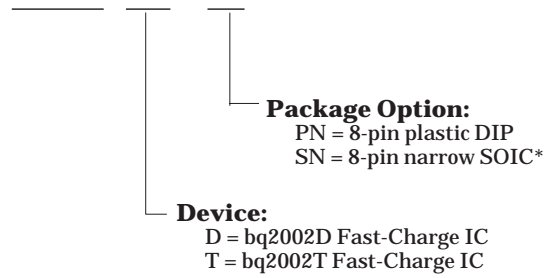


#### 8-Pin SN (0.150" SOIC)

| Dimension | Inches |       | Millimeters |      |
|-----------|--------|-------|-------------|------|
|           | Min.   | Max.  | Min.        | Max. |
| A         | 0.060  | 0.070 | 1.52        | 1.78 |
| A1        | 0.004  | 0.010 | 0.10        | 0.25 |
| B         | 0.013  | 0.020 | 0.33        | 0.51 |
| C         | 0.007  | 0.010 | 0.18        | 0.25 |
| D         | 0.185  | 0.200 | 4.70        | 5.08 |
| E         | 0.150  | 0.160 | 3.81        | 4.06 |
| e         | 0.045  | 0.055 | 1.14        | 1.40 |
| H         | 0.225  | 0.245 | 5.72        | 6.22 |
| L         | 0.015  | 0.035 | 0.38        | 0.89 |

---

## Ordering Information



\* bq2002D is only available in the 8-pin narrow SOIC package

**bq2002D/T****Data Sheet Revision History**

| Change No. | Page No. | Description   | Nature of Change         |
|------------|----------|---|--------------------------|
| 1          | 3        | Was: Table 1 gave the bq2002D/T Operational Summary.<br>Is: Figure 2 gives the bq2002D/T Operational Summary. | Changed table to figure. |
| 1          | 5        | Added top-off values.   | Added column and values. |
| 2          | All      | Revised and expanded this data sheet  |                          |
| 3          | All      | Revised and included bq2002D  | Addition of device       |
| 4          |          | Specified package information for the bq2002D   |                          |
| 5          | 1, 5     | Corrected transposed rows in Selection Guide Table and made Table 1 consistent with Selection Guide           |                          |
| 6          | 4        | Temperature Sampling — From 16 measurements taken 57us apart To: 16 measurements taken 570us apart.           |                          |

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">BQ2002DSN</a>   | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 2002D               |
| BQ2002DSN.B                 | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 2002D               |
| <a href="#">BQ2002DSNTR</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 2002D               |
| BQ2002DSNTR.B               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 2002D               |
| <a href="#">BQ2002TSN</a>   | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 2002T               |
| BQ2002TSN.B                 | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 2002T               |
| <a href="#">BQ2002TSNTR</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 2002T               |
| BQ2002TSNTR.B               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 2002T               |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ2002DSNTR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| BQ2002TSNTR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ2002DSNTR | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| BQ2002TSNTR | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |



## TUBE

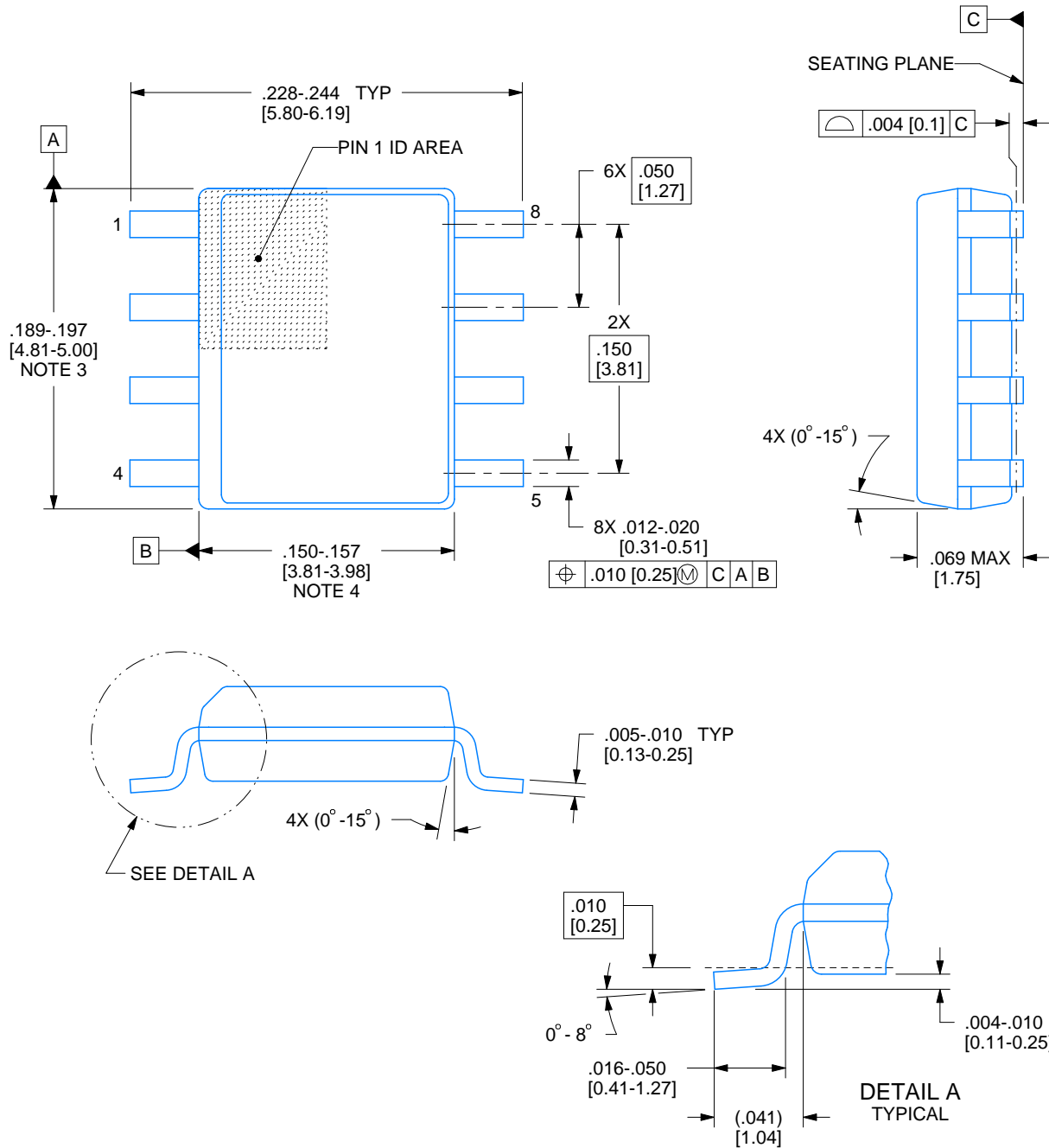


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| BQ2002DSN   | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| BQ2002DSN.B | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| BQ2002TSN   | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| BQ2002TSN.B | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |

**D0008A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

**NOTES:**

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated