









AWR1243 SWRS188D - MAY 2017 - REVISED DECEMBER 2021

# AWR1243 Single-Chip 77- and 79-GHz FMCW Transceiver

#### 1 Features

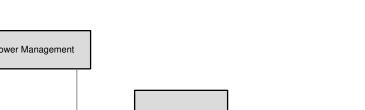
- **FMCW** transceiver
  - Integrated PLL, transmitter, receiver, Baseband, and ADC
  - 76- to 81-GHz coverage with 4 GHz available bandwidth
  - Four receive channels
  - Three transmit channels (two can be used simultaneously)
  - Ultra-accurate chirp engine based on fractional-N PLL
  - TX power: 12 dBm
  - RX noise figure:
    - 14 dB (76 to 77 GHz)
    - 15 dB (77 to 81 GHz)
  - Phase noise at 1 MHz:
    - –95 dBc/Hz (76 to 77 GHz)
    - –93 dBc/Hz (77 to 81 GHz)
- Built-in calibration and self-test
  - Built-in firmware (ROM)
  - Self-calibrating system across process and temperature
- Host interface
  - Control interface with external processor over
  - Data interface with external processor over MIPI D-PHY and CSI2 V1.1
  - Interrupts for fault reporting

- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 functional safety system design up to ASIL-D
  - Hardware integrity up to ASIL-B
  - Safety-related certification
    - ISO 26262 certified upto ASIL B by TUV SUD
- AEC-Q100 qualified
- Device advanced features
  - Embedded self-monitoring with no host processor involvement
  - Complex baseband architecture
  - Embedded interference detection capability
- Power management
  - Built-in LDO network for enhanced PSRR
  - I/Os support dual voltage 3.3 V/1.8 V
- Clock source
  - Supports externally driven clock (square/sine)
  - Supports 40 MHz crystal connection with load capacitors
- Easy hardware design
  - 0.65-mm pitch, 161-pin 10.4 mm × 10.4 mm flip chip BGA package for easy assembly and low-cost PCB design
  - Small solution size
- **Operating Conditions** 
  - Junction temp range: –40°C to 125°C



## 2 Applications

- Automotive Sensor for measuring range, velocity and angle
- Automated highway driving



Automatic emergency braking

Adaptive cruise control

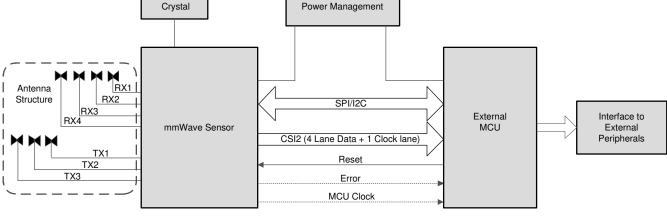


Figure 2-1. Autonomous Radar Sensor For Automotive Applications

## 3 Description

The AWR1243 device is an integrated single-chip FMCW transceiver capable of operation in the 76- to 81-GHz band. The device enables unprecedented levels of integration in an extremely small form factor. AWR1243 is an ideal solution for low power, self-monitored, ultra-accurate radar systems in the automotive space.

The AWR1243 device is a self-contained FMCW transceiver single-chip solution that simplifies the implementation of Automotive Radar sensors in the band of 76 to 81 GHz. It is built on TI's low-power 45-nm RFCMOS process, which enables a monolithic implementation of a 3TX, 4RX system with built-in PLL and ADC converters. Simple programming model changes can enable a wide variety of sensor implementation (Short, Mid, Long) with the possibility of dynamic reconfiguration for implementing a multimode sensor. Additionally, the device is provided as a complete platform solution including TI reference designs, software drivers, sample configurations, API guides, and user documentation.

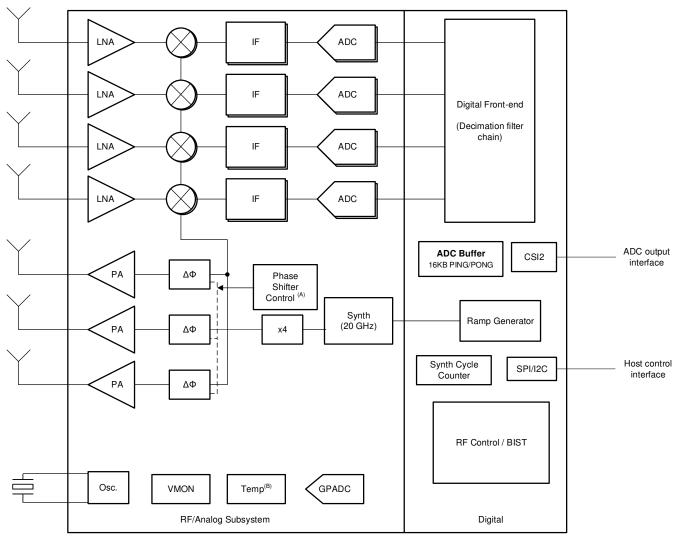
#### **Device Information**

PART NUMBER <sup>(2)</sup>	PACKAGE <sup>(1)</sup>	BODY SIZE	TRAY / TAPE AND REEL
AWR1243FBIGABLQ1	FCBGA (161)	10.4 mm × 10.4 mm	Tray
AWR1243FBIGABLRQ1	POBGA (101)	10.4 111111 ^ 10.4 111111	Tape and Reel

- For more information, see Section 13, Mechanical, Packaging, and Orderable Information.
- For more information, see Section 12.1, Device Nomenclature.

## **4 Functional Block Diagram**

Figure 4-1 shows the functional block diagram of the device.



- A. Phase Shift Control:
  - 0° / 180° BPM for AWR1243
- B. Internal temperature sensor accuracy is  $\pm$  7 °C.

Figure 4-1. Functional Block Diagram



## **Table of Contents**

1 Features	1	9.1 Overview	33
2 Applications	<mark>2</mark>	9.2 Functional Block Diagram	33
3 Description		9.3 Subsystems	
4 Functional Block Diagram	3	9.4 Other Subsystems	
5 Revision History		10 Monitoring and Diagnostics	
6 Device Comparison	6	10.1 Monitoring and Diagnostic Mechanisms	
6.1 Related Products		11 Applications, Implementation, and Layout	
7 Terminal Configuration and Functions	8	11.1 Application Information	
7.1 Pin Diagram		11.2 Short-, Medium-, and Long-Range Radar	42
7.2 Signal Descriptions		11.3 Reference Schematic	43
8 Specifications	16	12 Device and Documentation Support	44
8.1 Absolute Maximum Ratings	16	12.1 Device Nomenclature	
8.2 ESD Ratings	16	12.2 Tools and Software	45
8.3 Power-On Hours (POH)	17	12.3 Documentation Support	45
8.4 Recommended Operating Conditions	17	12.4 Support Resources	45
8.5 Power Supply Specifications	18	12.5 Trademarks	46
8.6 Power Consumption Summary	19	12.6 Electrostatic Discharge Caution	46
8.7 RF Specification	20	12.7 Glossary	46
8.8 Thermal Resistance Characteristics for FCBGA	A	13 Mechanical, Packaging, and Orderable	
Package [ABL0161]	<mark>21</mark>	Information	<mark>47</mark>
8.9 Timing and Switching Characteristics	21	13.1 Packaging Information	<mark>47</mark>
9 Detailed Description		13.2 Tray Information for	47



# **5 Revision History**

Changes from May 1, 2020 to December 8, 2021 (from Revision C (May 2020) to R	Revision D
(December 2021))	Page
• Global: Updated to reflect Functional Safety-Compliance and relevant certification of	
<ul> <li>Global: Replaced "A2D" with "ADC"; Changed Masters Subsystem and Masters R4</li> </ul>	F to Main Subsystem and
Main R4F; Shift to more inclusive langauge made in terms of Master/Slave terminol	ogy1
<ul> <li>(Features): Mentioned the specific operating temperature range for the mmWave S</li> </ul>	ensor1
(Applications) :Revised the figure and updated application links	
• (Device Information): Removed a pre-production orderable part number (XA1243FF	PBGABL) from the table
and its assosiated features.	2
<ul> <li>Updated/Changed Functional Block Diagram to remove XA1243FPBGABL OPN sp</li> </ul>	
<ul> <li>(Device Comparison): Removed a row on Functionaly-Safety compliance and inste</li> </ul>	
this and LVDS Interface; modified the existing table-note on simultaneous TX opera	
information on Device security added	
• (Device Comparison): Updated/Changed RF Specification Receiver from "Max real	
"Max real/complex 2x sampling rate (Msps)"; and "Max complex sampling rate (Msp	os)" to "Max complex 1x
sampling rate (Msps)"	6
<ul> <li>(Signal Descriptions): Removed XA1243FPBGABL OPN specific pin functions; update</li> </ul>	•
CLKP and CLKM pins for Reference Oscillator	
(Absolute Maximum Ratings): Added entries for externally supplied power on the RI	
a table-note for the signal level applied on TX	
(Power Supply Specifications): Updated/Changed footnote in Table 8-1	
<ul> <li>(Maximum Current Rating at Power Terminals): Updated footnotes section to add es</li> </ul>	· · · · · · · · · · · · · · · · · · ·
VIOIN rail	19
(Average Power Consumption at Power Terminals): Removed 3TX, 4RX power num	•
operational simultaneously in the device	
• (RF Specification): Updated/Changed RF Specification Receiver from "A2D sampling to the specification of the spe	
sampling rate (complex 1x)"; and "A2D sampling rate (real)" to "ADC sampling rate	
• (RF Specification): Updated/Changed the table to remove XA1243FPBGABL specification of the second	
• (Synchronized Frame Triggering): Updated the maximum pulse width to 4ns	
• (Clock Specifications): Updated/Changed Table 8-6 to reflect correct device operation (Table 5-6). Parising of frequency and the suppose are a frequency and	
• (Table. External Clock Mode Specifications): Revised frequency tolerance specs fro	
<ul> <li>(Switching Characteristics for Output Timing versus Load Capacitance): Updated/M</li> </ul>	
remove Slew Rate = 1 condition; removed a footnote	
• Figure 9-1: Updated the figure to remove XA1243FPBGABL OPN specific features.	
• (Monitoring and Diagnostic Mechanisms): Added a new section	
• (Reference Schematics): Added weblinks to AWR1243 EVM documentation collate	
(Device Nomenclature):Updated/changed Device Nomenclature	44



## **6 Device Comparison**

FUNCTION		AWR1243 <sup>(1)</sup>	AWR1443	AWR1642	AWR1843
Number of rec	eivers	4	4	4	4
Number of trar	nsmitters	3	3	2	3
On-chip memo	ory	_	576KB	1.5MB	2MB
Max I/F (Intern	nediate Frequency) (MHz)	15	5	5	10
Max real/comp	olex 2x sampling rate (Msps)	37.5	12.5	12.5	25
Max complex	1x sampling rate (Msps)	18.75	6.25	6.25	12.5
Device Securit	y <sup>(2)</sup>	_	_	Yes	Yes
Processor					
MCU (R4F)		_	Yes	Yes	Yes
DSP (C674x)		_	_	Yes	Yes
Peripherals					
Serial Peripher	ral Interface (SPI) ports	1	1	2	2
Quad Serial Pe	eripheral Interface (QSPI)	_	Yes	Yes	Yes
Inter-Integrated	d Circuit (I <sup>2</sup> C) interface	_	1	1	1
Controller Area	a Network (DCAN) interface	_	Yes	Yes	Yes
CAN-FD		_	_	Yes	Yes
Trace		_	_	Yes	Yes
PWM		_	_	Yes	Yes
Hardware In Lo	oop (HIL/DMM)	_	_	Yes	Yes
GPADC		_	Yes	Yes	Yes
LVDS/Debug <sup>(3</sup>	5)	Yes	Yes	Yes	Yes
CSI2		Yes	_	_	_
Hardware acce	elerator	_	Yes	_	Yes
1-V bypass mo	ode	Yes	Yes	Yes	Yes
Cascade (20-0	GHz sync)	_	_	_	_
JTAG		_	Yes	Yes	Yes
Number of Tx	that can be simultaneously used	2	2	2	3 <sup>(4)</sup>
Per chirp confi	gurable Tx phase shifter	_	_	_	Yes
Product status <sup>(5)</sup>	PRODUCT PREVIEW (PP), ADVANCE INFORMATION (AI), or PRODUCTION DATA (PD)	PD	PD	PD	PD

<sup>(1)</sup> Developed for Functional Safety applications, the device supports hardware integrity upto ASIL-B. Refer to the related documentation for more details.

<sup>(2)</sup> Device security features including Secure Boot and Customer Programmable Keys are available in select devices for only select part variants as indicated by the Device Type identifier in Section 3, Device Information table.

<sup>(3)</sup> The LVDS interface is not a production interface and is only used for debug.

<sup>(4) 3</sup> Tx Simultaneous operation is supported only in AWR1843 with 1V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin. Rest of the other devices only support simultaneous operation of 2 Transmitters.

<sup>(5)</sup> PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



#### **6.1 Related Products**

For information about other devices in this family of products or related products see the links that follow.

mmWave Sensors

TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for automotive applications.

**Sensors** 

Automotive mmWave TI's automotive mmWave sensor portfolio offers high-performance radar front end to ultra-high resolution, small and low-power single-chip radar solutions. TI's scalable sensor portfolio enables design and development of ADAS system solution for every performance, application and sensor configuration ranging from comfort functions to safety functions in all vehicles.

for AWR1243

Companion Products Review products that are frequently purchased or used in conjunction with this product.



## 7 Terminal Configuration and Functions

## 7.1 Pin Diagram

Figure 7-1 shows the pin locations for the 161-pin FCBGA package. Figure 7-2, Figure 7-3, Figure 7-4, and Figure 7-5 show the same pins, but split into four quadrants.

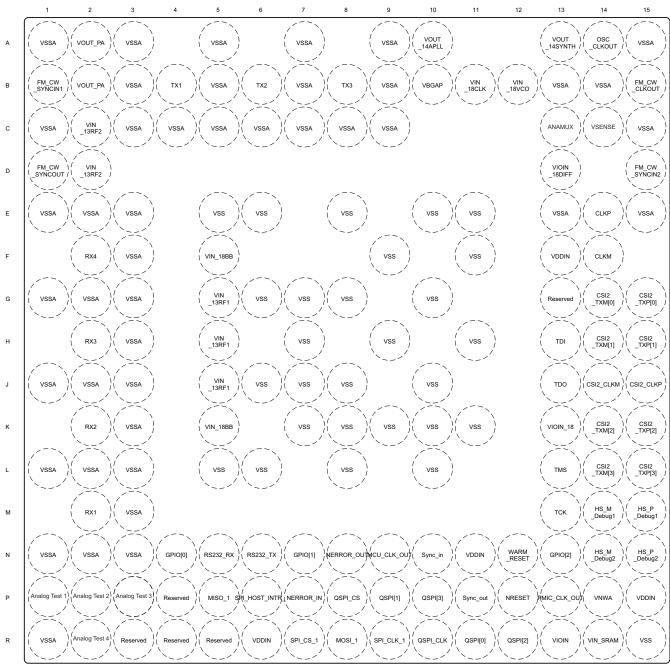


Figure 7-1. Pin Diagram

Not to scale

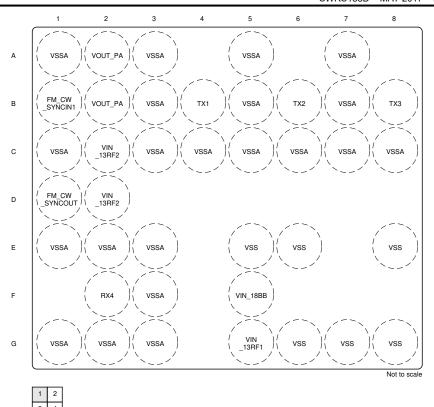


Figure 7-2. Top Left Quadrant

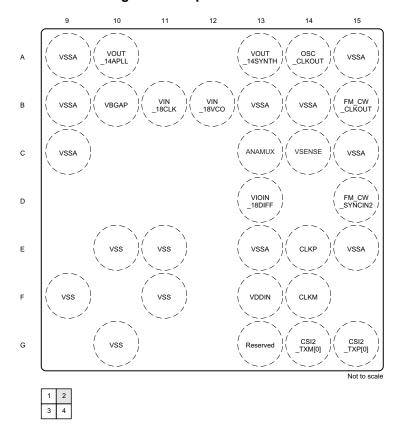


Figure 7-3. Top Right Quadrant



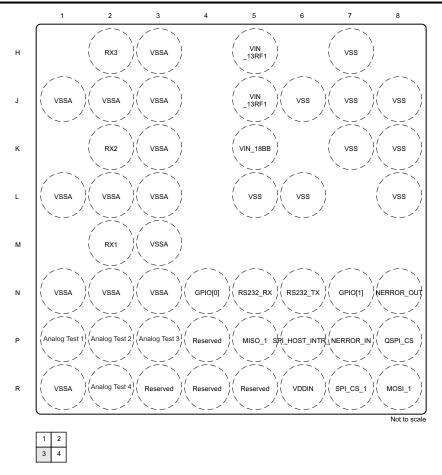


Figure 7-4. Bottom Left Quadrant

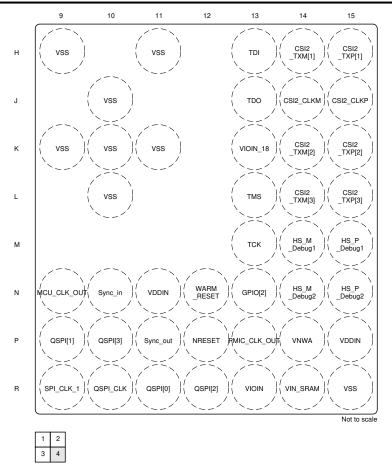


Figure 7-5. Bottom Right Quadrant



## 7.2 Signal Descriptions

Section 7.2.1 lists the pins by function and describes that function.

#### Note

All IO pins of the device (except NERROR IN, NERROR\_OUT, and WARM\_RESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

## 7.2.1 Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
	TX1	B4	0	_	Single-ended transmitter1 o/p
Transmitters	TX2	B6	0	_	Single-ended transmitter2 o/p
	TX3	B8	0	_	Single-ended transmitter3 o/p
	RX1	M2	I	<del>_</del>	Single-ended receiver1 i/p
Receivers	RX2	K2	I	_	Single-ended receiver2 i/p
Receivers	RX3	H2	I	_	Single-ended receiver3 i/p
	RX4	F2	I	_	Single-ended receiver4 i/p
	CSI2_TXP[0]	G15	0	_	Differential data Out – Lane 0 (for CSI and LVDS
CSI2_TXM[0]		G14	0	<del>_</del>	debug interface)
CSI2_CLKP		J15	0	_	Differential clock Out (for CSI and LVDS debug
	CSI2_CLKM	J14	0	_	interface)
	CSI2_TXP[1]	H15	0	_	Differential data Out – Lane 1 (for CSI and LVDS
	CSI2_TXM[1]	H14	0	_	debug interface)
CSI2 TX	CSI2_TXP[2]	K15	0	<del>_</del>	Differential data Out – Lane 2 (for CSI and LVDS
	CSI2_TXM[2]	K14	0	_	debug interface)
	CSI2_TXP[3]	L15	0	_	Differential data Out – Lane 3 (for CSI and LVDS
	CSI2_TXM[3]	L14	0	_	debug interface)
	HS_DEBUG1_P	M15	0	_	Differential debug port 1 (for LVDS debug interface)
	HS_DEBUG1_M	M14	0	_	— Differential debug port 1 (for EVDS debug interface)
	HS_DEBUG2_P	N15	0	_	Differential debug port 2 (for LVDS debug interface)
	HS_DEBUG2_M	N14	0	_	Differential debug port 2 (for EVDS debug interface)
	FM_CW_CLKOUT	B15	0		Reserved Signal. Not applicable in AWR1243.
Reserved	FM_CW_SYNCOUT	D1		_	Reserved Signal. Not applicable III AVVK 1245.
Space	FM_CW_SYNCIN1	B1			Reserved Signal. Not applicable in AWR1243.
	FM_CW_SYNCIN2	D15	'	_	reserved Signal. Not applicable III AVVI 1245.
Reference clock	OSC_CLKOUT	A14	0	_	Reference clock output from clocking subsystem after cleanup PLL. Can be used by peripheral chip in multichip cascading
System	SYNC_OUT	P11	0	Pull Down	Low-frequency frame synchronization signal output. Can be used by peripheral chip in multichip cascading
synchronization	SYNC_IN	N10	ı	Pull Down	Low-frequency frame synchronization signal input. This signal could also be used as a hardware trigger for frame start



www.ti.com

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
SPI control	SPI_CS_1	R7	ı	Pull Up	SPI chip select
interface from	SPI_CLK_1	R9	I	Pull Down	SPI clock
external MCU (default	MOSI_1	R8	I	Pull Up	SPI data input
peripheral	MISO_1	P5	0	Pull Up	SPI data output
mode)	SPI_HOST_INTR_1	P6	0	Pull Down	SPI interrupt to host
	RESERVED	R3, R4, R5, P4		_	
	NRESET	P12	I	_	Power on reset for chip. Active low
Reset	WARM_RESET <sup>(2)</sup>	N12	Ю	Open Drain	Open-drain fail-safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.
	SOP2	P13	I		The SOP pins are driven externally (weak drive)
Sense on Power	SOP1	P11	I	_	and the AWR device senses the state of these pins during bootup to decide the bootup mode. After boot
	SOP0	J13	ı		the same pins have other functionality.  [SOP2 SOP1 SOP0] = [0 0 1] → Functional SPI mode  [SOP2 SOP1 SOP0] = [1 0 1] → Flashing mode  [SOP2 SOP1 SOP0] = [0 1 1] → debug mode
	NERROR_OUT	N8	0	Open Drain	Open-drain fail-safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.
Safety	NERROR_IN	P7	I	Open Drain	Fail-safe input to the device. Error output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by firmware
	TMS	L13	I	Pull Up	
ITAC	TCK	M13	I	Pull Down	ITAC part for TI internal development
JTAG	TDI	H13	I	Pull Up	- JTAG port for TI internal development
	TDO	J13	0	_	
Reference	CLKP	E14	I	_	In XTAL mode: Input for the reference crystal In External clock mode: Single ended input reference clock port
oscillator	CLKM	F14	0	_	In XTAL mode: Feedback drive for the reference crystal In External clock mode: Connect this port to ground
Band-gap voltage	VBGAP	B10	0	_	



FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
	VDDIN	F13,N11,P15 ,R6	POW	_	1.2-V digital power supply
	VIN_SRAM	R14	POW	_	1.2-V power rail for internal SRAM
	VNWA	P14	POW	_	1.2-V power rail for SRAM array back bias
	VIOIN	R13	POW	_	I/O supply (3.3-V or 1.8-V): All CMOS I/Os would operate on this supply.
	VIOIN_18	K13	POW	_	1.8-V supply for CMOS IO
	VIN_18CLK	B11	POW	_	1.8-V supply for clock module
	VIOIN_18DIFF	D13	POW	_	1.8-V supply for CSI2 port
	Reserved	G13	POW	_	No connect
	VIN_13RF1	G5,J5,H5	POW	_	1.3-V Analog and RF supply,VIN_13RF1 and
	VIN_13RF2	C2,D2	POW	_	VIN_13RF2 could be shorted on the board
	VIN_18BB	K5,F5	POW	_	1.8-V Analog baseband power supply
	VIN_18VCO	B12	POW	_	1.8-V RF VCO supply
Power supply	vss	E5,E6,E8,E1 0,E11,F9,F1 1,G6,G7,G8, G10,H7,H9, H11,J6,J7,J8 ,J10,K7,K8,K 9,K10,K11,L 5,L6,L8,L10, R15	GND	_	Digital ground
	VSSA	A1,A3,A5,A7 ,A9,A15,B3, B5,B7,B9,B1 3,B14,C1,C3 ,C4,C5,C6,C 7,C8,C9,C15 ,E1,E2,E3,E 13,E15,F3,G 1,G2,G3,H3, J1,J2,J3,K3, L1,L2,L3, M3,N1,N2,N 3,R1	GND	_	Analog ground
	VOUT_14APLL	A10	0	_	
	VOUT_14SYNTH	A13	0	_	
Internal LDO output/inputs	VOUT_PA	A2,B2	Ю	_	When internal PA LDO is used this pin provides the output voltage of the LDO. When the internal PA LDO is bypassed and disabled 1V supply should be fed on this pin. This is mandatory in 3TX simultaneous use case.
F. 4	PMIC_CLK_OUT	P13	0	_	Dithered clock input to PMIC
External clock out	MCU_CLK_OUT	N9	0	_	Programmable clock given out to external MCU or the processor
	GPIO[0]	N4	Ю	Pull Down	General-purpose IO
General-	GPIO[1]	N7	Ю	Pull Down	General-purpose IO
purpose I/Os	GPIO[2]	N13	10	Pull Down	General-purpose IO



www.ti.com

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS <sup>(1)</sup>	DESCRIPTION
	QSPI_CS	P8	0	Pull Up	Chip-select output from the device. Device is a controller connected to serial flash peripheral.
QSPI for Serial	QSPI_CLK	R10	0	Pull Down	Clock output from the device. Device is a controller connected to serial flash peripheral.
Flash	QSPI[0]	R11	10	Pull Down	Data IN/OUT
	QSPI[1]	P9	10	Pull Down	Data IN/OUT
	QSPI[2]	R12	10	Pull Up	Data IN/OUT
	QSPI[3]	P10	Ю	Pull Up	Data IN/OUT
Flash	RS232_TX	N6	0	Pull Down	
programming and RS232 UART	RS232_RX	N5	I	Pull Up	UART pins for programming external flash
Test and Debug	Analog Test1	P1	10	_	Internal test signal
output for	Analog Test2	P2	10	_	Internal test signal
preproduction phase. Can be	Analog Test3	P3	10	_	Internal test signal
pinned out on	Analog Test4	R2	Ю	_	Internal test signal
production hardware for	ANAMUX	C13	10	_	Internal test signal
field debug	VSENSE	C14	Ю	_	Internal test signal

<sup>(1)</sup> Status of PULL structures associated with the IO after device POWER UP.

<sup>(2)</sup> For the AWR1243 WARM\_RESET can be used as an output only pin for status indication.



## 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

	PARAMETERS <sup>(1)</sup> (2)	MIN	MAX	UNIT	
VDDIN	1.2 V digital power supply	-0.5	1.4	V	
VIN_SRAM	1.2 V power rail for internal SRAM	-0.5	1.4	V	
VNWA	1.2 V power rail for SRAM array back bias	-0.5	1.4	V	
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	-0.5	3.8	V	
VIOIN_18	1.8 V supply for CMOS IO	-0.5	2	V	
VIN_18CLK	1.8 V supply for clock module	-0.5	2	V	
VIOIN_18DIFF	1.8 V supply for CSI2 port	-0.5	2	V	
VIN_13RF1	1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could	0.5	4.45		
VIN_13RF2	be shorted on the board.	-0.5	1.45	V	
VIN_13RF1	1-V Internal LDO bypass mode. Device supports mode				
VIN_13RF2	where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	-0.5	1.4	V	
VIN_18BB	1.8-V Analog baseband power supply	-0.5	2	V	
VIN_18VCO supply	1.8-V RF VCO supply	-0.5	2	V	
RX1-4	Externally applied power on RF inputs		10	dBm	
TX1-3	Externally applied power on RF outputs <sup>(3)</sup>		10	dBm	
	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	-0.3V	VIOIN + 0.3		
Input and output voltage range	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input		OIN + 20% up to of signal period	V	
CLKP, CLKM	Input ports for reference crystal	-0.5	2	V	
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	-20	20	mA	
T <sub>J</sub>	Operating junction temperature range	-40	125	°C	
T <sub>STG</sub>	Storage temperature range after soldered onto PC board	-55	150	°C	

<sup>(1)</sup> Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 8.2 ESD Ratings

				VALUE	UNIT
		Human-body model (HBM), per AEC Q100	-002 <sup>(1)</sup>	±2000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per AEC	All other pins	±500	V
		Q100-011	Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

<sup>(2)</sup> All voltage values are with respect to V<sub>SS</sub>, unless otherwise noted.

<sup>(3)</sup> This value is for an externally applied signal level on the TX. Additionally, a reflection coefficient up to Gamma = 1 can be applied on the TX output.

## 8.3 Power-On Hours (POH)

JUNCTION TEMPERATURE (T <sub>j</sub> )	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)
-40°C			600 (6%)
75°C	100% duty avala	1.2	2000 (20%)
95°C	100% duty cycle	1.2	6500 (65%)
125°C			900 (9%)

<sup>(1)</sup> This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

## **8.4 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIN	1.2 V digital power supply	1.14	1.2	1.32	V
VIN_SRAM	1.2 V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2 V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O supply (3.3 V or 1.8 V):	3.135	3.3	3.465	V
VIOIN	All CMOS I/Os would operate on this supply.	1.71	1.8	1.89	V
VIOIN_18	1.8 V supply for CMOS IO	1.71	1.8	1.9	V
VIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.9	V
VIOIN_18DIFF	1.8 V supply for CSI2 port	1.71	1.8	1.9	V
VIN_13RF1	1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2	1.23	1.3	1.36	V
VIN_13RF2	could be shorted on the board	1.23	1.3	1.30	V
VIN_13RF1 (1-V Internal LDO bypass mode)		0.95	1	1.05	V
VIN_13RF2 (1-V Internal LDO bypass mode)					
VIN18BB	1.8-V Analog baseband power supply	1.71	1.8	1.9	V
VIN_18VCO	1.8V RF VCO supply	1.71	1.8	1.9	V
	Voltage Input High (1.8 V mode)	1.17			V
VIH	Voltage Input High (3.3 V mode)	2.25			V
	Voltage Input Low (1.8 V mode)			0.3*VIOIN	V
VIL	Voltage Input Low (3.3 V mode)			0.62	V
V <sub>OH</sub>	High-level output threshold (I <sub>OH</sub> = 6 mA)	VIOIN – 450			mV
V <sub>OL</sub>	Low-level output threshold (I <sub>OL</sub> = 6 mA)			450	mV
	V <sub>IL</sub> (1.8V Mode)			0.2	
/IOIN_18 /IN_18CLK /IOIN_18DIFF /IN_13RF1 /IN_13RF2 /IN_13RF1 1-V Internal LDO pypass mode) /IN_13RF2 1-V Internal LDO pypass mode) /IN_13RF2 1-V Internal LDO pypass mode) /IN_18VCO /IN_18VCO /IN_18VCO /IN_IN_INTERNATION	V <sub>IH</sub> (1.8V Mode)	0.96			V
SOP[2:0]	V <sub>IL</sub> (3.3V Mode)			0.3	V
IOIN IOIN_18 IN_18CLK IOIN_18DIFF IN_13RF1 IN_13RF2 IN_13RF1 I-V Internal LDO ypass mode) IN_13RF2 IN_13RF2 IN_13RF2 IN_13RF2 IN_13RF2 IN_13RF2 IN_13RF2 IN_18VCO IN_18BB IN_18VCO IN_18BB IN_18VCO IH IL OH	V <sub>IH</sub> (3.3V Mode)	1.57			

<sup>(2)</sup> The specified POH are applicable with max Tx output power settings using the default firmware gain tables. The specified POH would not be applicable, if the Tx gain table is overwritten using an API.



## 8.5 Power Supply Specifications

Table 8-1 describes the four rails from an external power supply block of the AWR1243 device.

**Table 8-1. Power Supply Rails Characteristics** 

radio o mi onor ouppry ramo omanacionos							
SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOS IN THE DEVICE					
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, CSI2	Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL					
1.3 V (or 1 V in internal LDO bypass mode) <sup>(1)</sup>	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA					
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/Os	Input VIOIN					
1.2 V	Core Digital and SRAMs	Input: VDDIN, VIN_SRAM					

<sup>(1)</sup> The device only supports simultaneous operation of 2 transmitters. In the 1-V LDO bypass mode, 1V supply needs to be fed on the VOUT PA pin.

The 1.3-V (1.0 V) and 1.8-V power supply ripple specifications mentioned in Table 8-2 are defined to meet a target spur level of -105 dBc (RF Pin = -15 dBm) at the RX. The spur and ripple levels have a dB-to-dB relationship, for example, a 1-dB increase in supply ripple leads to a  $\sim$ 1 dB increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

Table 8-2. Ripple Specifications

Table 6 21 1 Tople 6 positions						
	RF RAIL		VCO/IF RAIL			
FREQUENCY (kHz)	1.0 V (INTERNAL LDO BYPASS) (μV <sub>RMS</sub> )	1.3 V (μV <sub>RMS</sub> )	1.8 V (μV <sub>RMS</sub> )			
137.5	7	648	83			
275	5	76	21			
550	3	22	11			
1100	2	4	6			
2200	11	82	13			
4400	13	93	19			
6600	22	117	29			



## **8.6 Power Consumption Summary**

Table 8-3 and Table 8-4 summarize the power consumption at the power terminals.

**Table 8-3. Maximum Current Ratings at Power Terminals** 

PARAMETER	SUPPLY NAME	DESCRIPTION	MIN	TYP MAX	UNIT
Current consumption <sup>(1)</sup>	VDDIN, VIN_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail		500	
	VIN_13RF1, VIN_13RF2	Total current drawn by all nodes driven by 1.3V (or 1V in LDO Bypass mode) rail		2000	- mA
	VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO	Total current drawn by all nodes driven by 1.8V rail		850	
	VIOIN	Total current drawn by all nodes driven by 3.3V rail <sup>(2)</sup>		50	

- (1) The specified current values are at typical supply voltage level.
- (2) The exact VIOIN current depends on the peripherals used and their frequency of operation.

**Table 8-4. Average Power Consumption at Power Terminals** 

			•				
PARAMETER	CONE	DITION	DESCRIPTION	MIN	TYP	MAX	UNIT
Average power consumption  LDO bypass mode  2TX, 4RX  1.3-V internal LDO enabled	1TX, 4RX	Complings 16 66 MCna compley		1.62			
	, ,,	2TX, 4RX	Sampling: 16.66 MSps complex Transceiver, 40-ms frame time, 512 chirps, 512 samples/chirp, 8.5-µs interchirp time (50% duty cycle)		1.79		W
	_	1TX, 4RX			1.80		VV
	OTV ADV	Data Port: MIPI-CSI-2		2.01			



#### 8.7 RF Specification

over recommended operating conditions and with run time calibrations enabled (unless otherwise noted)

	PARAMETER		MIN	TYP	MAX	UNIT
		76 to 77 GHz (VCO1)		14		
	Noise figure	77 to 81 GHz (VCO2)		15		dB
	1-dB compression point (Out Of Band) <sup>(1)</sup>			-8		dBm
Receiver	Maximum gain		48		dB	
	Gain range		24		dB	
	Gain step size		2		dB	
	Image Rejection Ratio (IMRR)			30		dB
	IF bandwidth <sup>(2)</sup>				15	MHz
	ADC sampling rate (real/complex 2x)				37.5	Msps
Receiver	ADC sampling rate (complex 1x)			18.75	Msps	
receiver	ADC resolution		12		Bits	
	Return loss (S11)		<-10		dB	
	Gain mismatch variation (over temperature)		±0.5		dB	
	Phase mismatch variation (over temperature		±3		0	
	In-band IIP2	RX gain = 30dB IF = 1.5, 2 MHz at -12 dBFS		16		dBm
	Out-of-band IIP2	RX gain = 24dB IF = 10 kHz at -10dBm, 1.9 MHz at -30 dBm		24		dBm
	Idle Channel Spurs			-90		dBFS
Transmitter	Output power			12		dBm
Transmitter	Amplitude noise		-145		dBc/Hz	
Clock	Frequency range	76		81	GHz	
	Ramp rate				100	MHz/µs
subsystem	Phase noise at 1-MHz offset	76 to 77 GHz (VCO1)		<b>-</b> 95		dBc/Hz
	i ilase iloise at i-ivii iz oliset	77 to 81 GHz (VCO2)		-93		ubc/i IZ

<sup>(1) 1-</sup>dB Compression Point (Out Of Band) is measured by feed a Continuous wave Tone (10 kHz) well below the lowest HPF cut-off frequency.

Available HPF Corner Frequencies (kHz)

HPF1 HPF2

175, 235, 350, 700 350, 700, 1400, 2800

The filtering performed by the digital baseband chain is targeted to provide:

- · Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

Figure 8-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

<sup>(2)</sup> The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

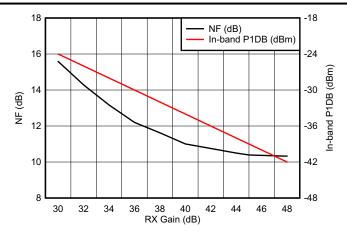


Figure 8-1. Noise Figure, In-band P1dB vs Receiver Gain

#### 8.8 Thermal Resistance Characteristics for FCBGA Package [ABL0161]

THERMAL ME	THERMAL METRICS <sup>(1)</sup>	
RΘ <sub>JC</sub>	Junction-to-case	5
RΘ <sub>JB</sub>	Junction-to-board	5.9
RΘ <sub>JA</sub>	Junction-to-free air	21.6
RΘ <sub>JMA</sub>	Junction-to-moving air	15.3 <sup>(4)</sup>
Psi <sub>JT</sub>	Junction-to-package top	0.69
Psi <sub>JB</sub>	Junction-to-board	5.8

- (1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.
- (2) °C/W = degrees Celsius per watt.
- (3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [RO<sub>JC</sub>] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
  - · JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions Natural Convection (Still Air)
  - · JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
  - JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
  - JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements
- (4) Air flow = 1 m/s

#### 8.9 Timing and Switching Characteristics

#### 8.9.1 Power Supply Sequencing and Reset Timing

The AWR1243 device expects all external voltage rails and SOP lines to be stable before reset is deasserted. Figure 8-2 describes the device wake-up sequence.



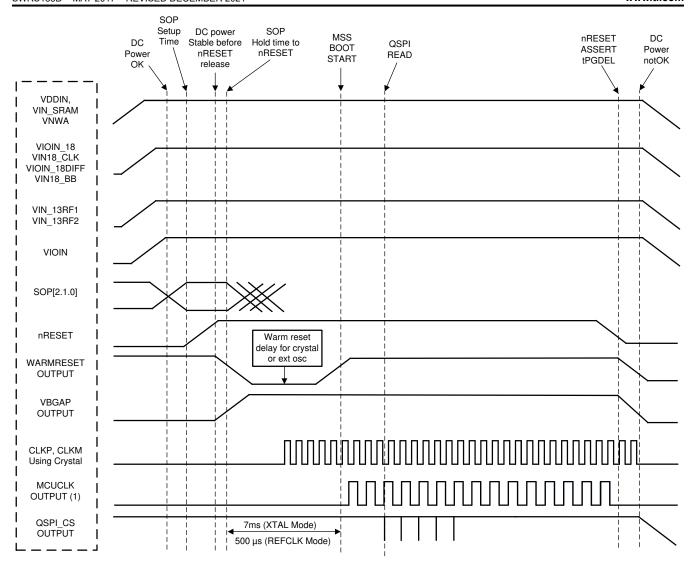


Figure 8-2. Device Wake-up Sequence

#### 8.9.2 Synchronized Frame Triggering

The AWR1243 device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC\_IN signal to start radar frames. The typical time difference between the rising edge of the external pulse and the frame transmission on air (Tlag) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time.

The periodicity of the external SYNC\_IN pulse should be always greater than the programmed frame periodic in the frame configurations in all instances.

www.ti.com

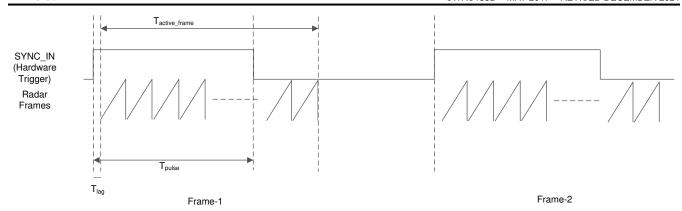


Figure 8-3. Sync In Hardware Trigger

**Table 8-5. Frame Trigger Timing** 

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T <sub>active_frame</sub>	Active frame duration	User defined		ne
T <sub>pulse</sub>		25	4000	ns



#### 8.9.3 Input Clocks and Oscillators

#### 8.9.3.1 Clock Specifications

An external crystal is connected to the device pins. Figure 8-4 shows the crystal implementation.

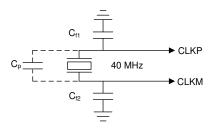


Figure 8-4. Crystal Implementation

#### Note

The load capacitors,  $C_{f1}$  and  $C_{f2}$  in Figure 8-4, should be chosen such that Equation 1 is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins. Note that Cf1 and Cf2 include the parasitic capacitances due to PCB routing.

$$C_{L} = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_{P}$$
(1)

Table 8-6 lists the electrical characteristics of the clock crystal.

Table 8-6. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f <sub>P</sub>	Parallel resonance crystal frequency		40		MHz
C <sub>L</sub>	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	-40		125	°C
Frequency tolerance	Crystal frequency tolerance <sup>(1)</sup> (2)	-200		200	ppm
Drive level			50	200	μW

- (1) The crystal manufacturer's specification must satisfy this requirement.
- (2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40-MHz clock is fed externally. Table 8-7 lists the electrical characteristics of the external clock signal.

**Table 8-7. External Clock Mode Specifications** 

DADAM	PARAMETER			SPECIFICATION			
PARAMETER		MIN	TYP	MAX	UNIT		
	Frequency		40		MHz		
	AC-Amplitude	700		1200	mV (pp)		
	DC-t <sub>rise/fall</sub>			10	ns		
Input Clock:	Phase Noise at 1 kHz			-132	dBc/Hz		
External AC-coupled sine wave or DC-coupled square wave	Phase Noise at 10 kHz			-143	dBc/Hz		
Phase Noise referred to 40 MHz	Phase Noise at 100 kHz			-152	dBc/Hz		
	Phase Noise at 1 MHz			-153	dBc/Hz		
	Duty Cycle	35		65	%		
	Freq Tolerance	-100		100	ppm		



## 8.9.4 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

#### 8.9.4.1 Peripheral Description

The SPI uses a MibSPI Protocol by TI.

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Section 8.9.4.1.2 and Section 8.9.4.1.3 assume the operating conditions stated in Section 8.9.4.1.1. Section 8.9.4.1.2, Section 8.9.4.1.3, and Figure 8-5 describe the timing and switching characteristics of the MibSPI.

#### 8.9.4.1.1 SPI Timing Conditions

		MIN	TYP MAX	UNIT		
Input Conditions						
t <sub>R</sub>	Input rise time	1	3	ns		
t <sub>F</sub>	Input fall time	1	3	ns		
Output Conditions						
C <sub>LOAD</sub>	Output load capacitance	2	15	pF		

# 8.9.4.1.2 SPI Peripheral Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	t <sub>c(SPC)S</sub>	Cycle time, SPICLK	25			ns
2	t <sub>w(SPCH)S</sub>	Pulse duration, SPICLK high	10			ns
3	t <sub>w(SPCL)S</sub>	Pulse duration, SPICLK low	10			ns
4	t <sub>d(SPCL-SOMI)S</sub>	Delay time, SPISOMI valid after SPICLK low			10	ns
5	t <sub>h(SPCL-SOMI)S</sub>	Hold time, SPISOMI data valid after SPICLK low	2			ns

# 8.9.4.1.3 SPI Peripheral Mode Timing Requirements (SPICLK = input, SPISIMO = input, and SPISOMI = output)

NO.		MIN	TYP	MAX	UNIT
6	t <sub>su(SIMO-SPCH)S</sub> Setup time, SPISIMO before SPICLK high	3			ns
7	t <sub>h(SPCH-SIMO)S</sub> Hold time, SPISIMO data valid after SPICLK high	1			ns

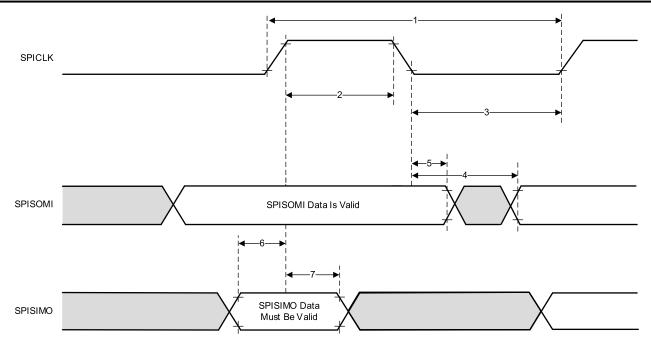


Figure 8-5. SPI Peripheral Mode External Timing



## 8.9.4.2 Typical Interface Protocol Diagram (Peripheral Mode)

- 1. Host should ensure that there is a delay of at least two SPI clocks between CS going low and start of SPI clock.
- 2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

Figure 8-6 shows the SPI communication timing of the typical interface protocol.

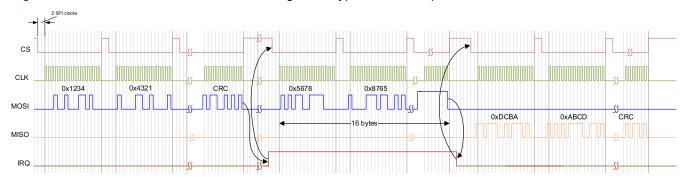


Figure 8-6. SPI Communication

## 8.9.5 LVDS Interface Configuration

The AWR1243 supports seven differential LVDS IOs/Lanes to support debug where raw ADC data could be extracted. The lane configuration supported is four Data lanes (LVDS\_TXP/M), one Bit Clock lane (LVDS\_CLKP/M) one Frame clock lane (LVDS\_FRCLKP/M). The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

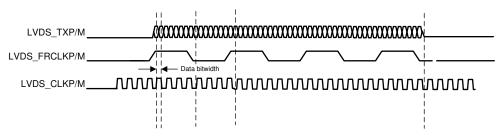


Figure 8-7. LVDS Interface Lane Configuration And Relative Timings

#### 8.9.5.1 LVDS Interface Timings

**Table 8-8. LVDS Electrical Characteristics** 

14510 0 01 1750 110011041 011414000110410								
TEST CONDITIONS	MIN	TYP	MAX	UNIT				
max 1 pF lumped capacitive load on LVDS lanes	48%		52%					
peak-to-peak single-ended with 100 $\Omega$ resistive load between differential pairs	250		450	mV				
	1125		1275	mV				
20%-80%, 900 Mbps		330		ps				
900 Mbps		80		ps				
	max 1 pF lumped capacitive load on LVDS lanes  peak-to-peak single-ended with 100 Ω resistive load between differential pairs  20%-80%, 900 Mbps	max 1 pF lumped capacitive load on LVDS lanes  peak-to-peak single-ended with 100 Ω resistive load between differential pairs  250  1125  20%-80%, 900 Mbps	max 1 pF lumped capacitive load on LVDS lanes  peak-to-peak single-ended with 100 Ω resistive load between differential pairs  250  1125  20%-80%, 900 Mbps  330	max 1 pF lumped capacitive load on LVDS lanes  peak-to-peak single-ended with 100 Ω resistive load between differential pairs  250 450 20%-80%, 900 Mbps 330				



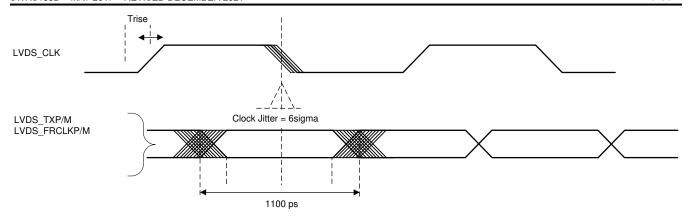


Figure 8-8. Timing Parameters

## 8.9.6 General-Purpose Input/Output

Section 8.9.6.1 lists the switching characteristics of output timing relative to load capacitance.

## 8.9.6.1 Switching Characteristics for Output Timing versus Load Capacitance (CL)

	PARAMETER <sup>(1)</sup>	TEST CONDITIONS	VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t <sub>r</sub>	Max rise time	C <sub>L</sub> = 20 pF	2.8	3.0	
		C <sub>L</sub> = 50 pF	6.4	6.9	ns
		C <sub>L</sub> = 75 pF	9.4	10.2	
t <sub>f</sub>		C <sub>L</sub> = 20 pF	2.8	2.8	
		C <sub>L</sub> = 50 pF	6.4	6.6	ns
		C <sub>L</sub> = 75 pF	9.4	9.8	

<sup>(1)</sup> The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

## 8.9.7 Camera Serial Interface (CSI)

The CSI is a MIPI D-PHY compliant interface for connecting this device to a camera receiver module. This interface is made of four differential lanes; each lane is configurable for carrying data or clock. The polarity of each wire of a lane is also configurable. Section 8.9.7.1, Figure 8-9, Figure 8-10, and Figure 8-11 describe the clock and data timing of the CSI. The clock is always ON once the CSI IP is enabled. Hence it remains in HS mode.

## 8.9.7.1 CSI Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER		MIN	TYP MAX	UNIT
HPTX					
HSTX <sub>DBR</sub>	Data bit rate	(1/2/4 data lane PHY)	150	600	Mbps
f <sub>CLK</sub>	DDR clock frequency	(1/2/4 data lane PHY)	75	300	MHz
$\Delta_{VCMTX(LF)}$	Common-level variation	mon-level variation –50 5		50	mV
t <sub>R</sub> and t <sub>F</sub>	20% to 80% rise time and fall time			0.3	UI
LPTX DRIVER					I
t <sub>EOT</sub>	Time from start of THS-TRAIL period to start of LP-11 state			105 + 12*UI	ns
DATA-CLOCK Timing Spec	ification				
UINOM	Nominal Unit Interval		1.67	13.33	ns
UIINST,MIN	Minimum instantaneous Unit Interval		1.131		ns
TSKEW[TX]	Data to clock skew measured at transm	-0.15	0.15	UIINST, MIN	
CSI2 TIMING SPECIFICAT	ION				
T <sub>CLK-PRE</sub>	Time that the HS clock shall be driven by the transmitter before any associated data lane beginning the transition from LP to HS mode.		8		ns
T <sub>CLK-PREPARE</sub>	Time that the transmitter drives the cloc state immediately before the HS-0 line stransmission.	38	95	ns	
T <sub>CLK-PREPARE</sub> + T <sub>CLK-ZERO</sub>	T <sub>CLK-PREPARE</sub> + time that the transmitter drives the HS-0 state before starting the clock.		300		ns
T <sub>EOT</sub>	Transmitted time interval from the start of T <sub>HS-TRAIL</sub> or T <sub>CLKTRAIL</sub> , to the start of the LP-11 state following a HS burst.			105 ns + 12*UI	ns
T <sub>HS-PREPARE</sub>	Time that the transmitter drives the data lane LP-00 line state immediately before the HS-0 line state starting the HS transmission		40 + 4*UI	85 + 6*UI	ns
T <sub>HS-PREPARE</sub> + T <sub>HS-ZERO</sub>	T <sub>HS-PREPARE</sub> + time that the transmitter to transmitting the Sync sequence.	drives the HS-0 state prior	145 ns + 10*UI		
T <sub>HS-EXIT</sub>	Time that the transmitter drives LP-11 for	ollowing a HS burst.	100		ns
T <sub>HS-TRAIL</sub>	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst		max(8*UI, 60 ns + 4*UI)		ns
T <sub>LPX</sub>	TXXXransmitted length of any low-power	er state period	50		ns

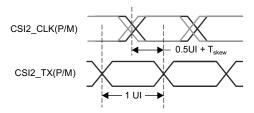


Figure 8-9. Clock and Data Timing in HS Transmission



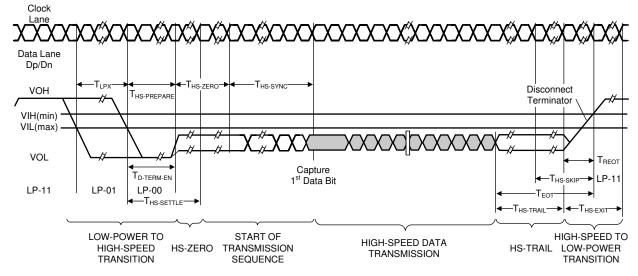
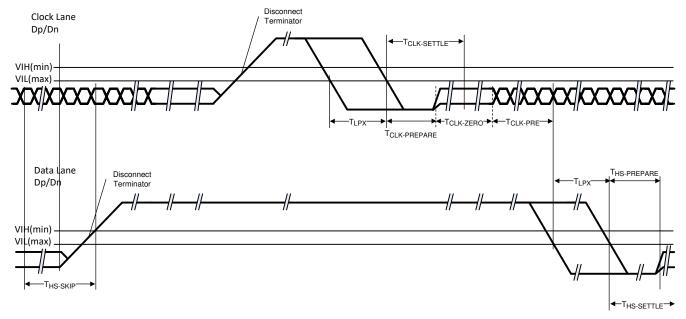


Figure 8-10. High-Speed Data Transmission Burst



A. The HS to LP transition of the CLK does not actually take place since the CLK is always ON in HS mode.

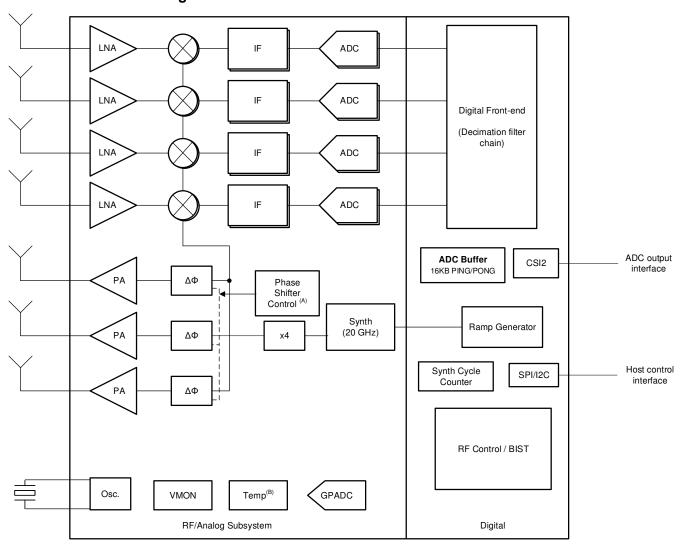
Figure 8-11. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

## 9 Detailed Description

## 9.1 Overview

The AWR1243 device is a single-chip highly integrated 77-GHz transceiver and front end that includes three transmit and four receive chains. The device can be used in long-range automotive radar applications such as automatic emergency braking and automatic adaptive cruise control. The AWR1243 has extremely small form factor and provides ultra-high resolution with very low power consumption. This device, when used with the TDA3X or TD2X, offers higher levels of performance and flexibility through a programmable digital signal processor (DSP); thus addressing the standard short-, mid-, and long-range automotive radar applications.

### 9.2 Functional Block Diagram



- A. Phase Shift Control:
  - 0° / 180° BPM for AWR1243
- B. Internal temperature sensor accuracy is ± 7 °C.

Figure 9-1. Functional Block Diagram



#### 9.3 Subsystems

## 9.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated simultaneously for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

Please note that AWR1243 device supports simultaneous operation of 2 transmitters only.

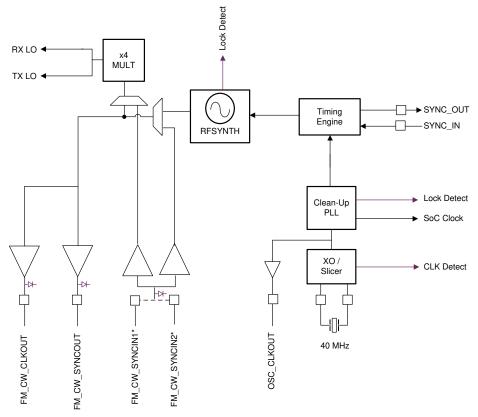
#### 9.3.1.1 Clock Subsystem

The AWR1243 clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The output of the RF synthesizer is available at the device pin boundary for multichip cascaded configuration. The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 9-2 describes the clock subsystem.



 $<sup>^{\</sup>star}$  These pins are 20GHz LO input pins. Connect LO to one pin while grounding the other pin.

Figure 9-2. Clock Subsystem



#### 9.3.1.2 Transmit Subsystem

The AWR1243 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. A maximum of two transmit chains can be operational at the same time, however all three chains can be operated together in a time-multiplexed fashion. The device supports binary phase modulation for MIMO radar and interference mitigation.

Each transmit chain can deliver a maximum of 12 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization.

Figure 9-3 describes the transmit subsystem.

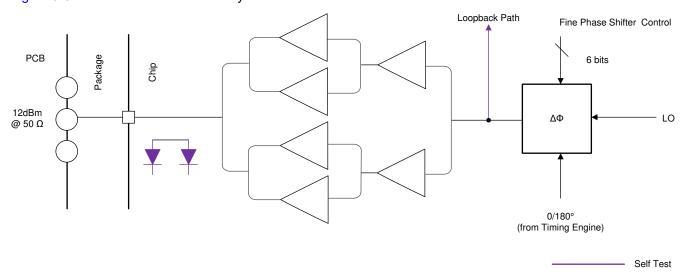


Figure 9-3. Transmit Subsystem (Per Channel)

#### 9.3.1.3 Receive Subsystem

The AWR1243 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, ADC conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the AWR1243 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The AWR1243 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 15 MHz.

Figure 9-4 describes the receive subsystem.

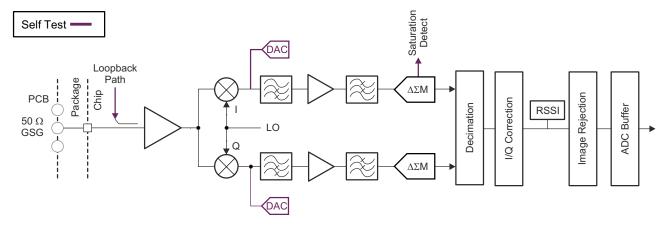


Figure 9-4. Receive Subsystem (Per Channel)

#### 9.3.2 Host Interface

The AWR1243 device communicates with the host radar processor over the following main interfaces:

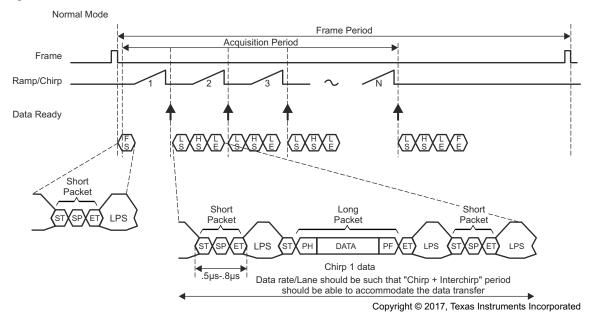
- Reference Clock Reference clock available for host processor after device wakeup
- Control 4-port standard SPI (peripheral) for host control along with HOST INTR pin for async events.. All
  radio control commands (and response) flow through this interface.
- Data High-speed serial port following the MIPI CSI2 format. Four data and one clock lane (all differential).
   Data from different receive channels can be multiplexed on a single data lane to optimize board routing. This is a unidirectional interface used for data transfer only.
- Reset Active-low reset for device wakeup from host
- Out-of-band interrupt
- · Error Used for notifying the host in case the radio controller detects a fault

## 9.4 Other Subsystems

#### 9.4.1 ADC Data Format Over CSI2 Interface

The AWR1243 device uses MIPI D-PHY / CSI2-based format to transfer the raw ADC samples to the external MCU. This is shown in Figure 9-5.

- · Supports four data lanes
- CSI-2 data rate scalable from 150 Mbps to 600 Mbps per lane
- · Virtual channel based
- · CRC generation



Frame Start - CSi2 VSYNC Start Short PacketLine Start - CSI2 HSYNC Start Short PacketLine End - CSI2 HSYNC End Short PacketFrame End - CSi2 VSYNC End Short Packet

Figure 9-5. CSI-2 Transmission Format



The data payload is constructed with the following three types of information:

- Chirp profile information
- · The actual chirp number
- ADC data corresponding to chirps of all four channels
  - Interleaved fashion
- Chirp quality data (configurable)

The payload is then split across the four physical data lanes and transmitted to the receiving D-PHY. The data packet packing format is shown in Figure 9-6

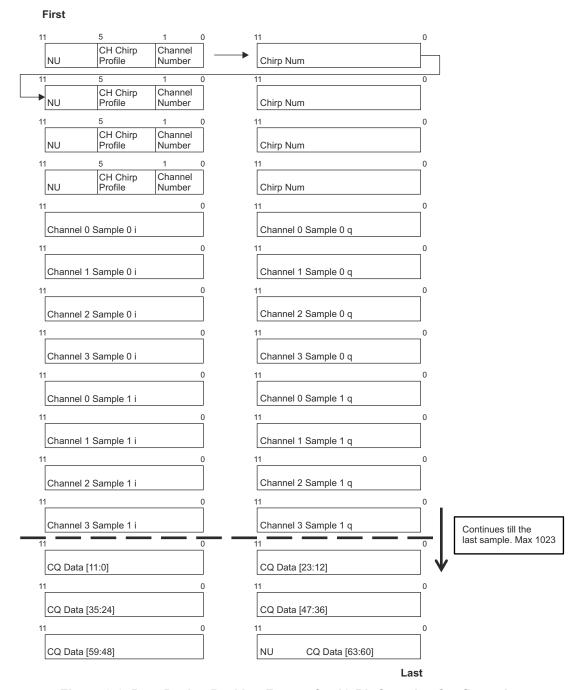


Figure 9-6. Data Packet Packing Format for 12-Bit Complex Configuration

# 10 Monitoring and Diagnostics

# 10.1 Monitoring and Diagnostic Mechanisms

Below is the list given for the main monitoring and diagnostic mechanisms available in the AWR1243.

MSS R4F is the processor used for running TI's Functional Firmware stored in the ROM that helps in the execution of the API calls issued by the host processor (It is not a customer programmable core).

Table 10-1. Monitoring and Diagnostic Mechanisms for AWR1243

S No	Feature	Description							
1	Boot time LBIST For MSS R4F Core and associated VIM	AWR1243 architecture supports hardware logic BIST (LBIST) engine self-test Controller (STC). This logic is used to provide a very high diagnostic coverage (>90%) on the MSS R4F CPU core and Vectored Interrupt Module (VIM) at a transistor level. LBIST for the CPU and VIM are triggered by the bootloader.							
2	Boot time PBIST for MSS R4F TCM Memories	MSS R4F has three Tightly coupled Memories (TCM) memories TCMA, TCMB0 and TCMB1. AWR1243 architecture supports a hardware programmable memory BIST (PBIST) engine. This logic is used to provide a very high diagnostic coverage (March-13n) on the implemented MSS R4F TCMs at a transistor level.  PBIST for TCM memories is triggered by Bootloader at the boot time . CPU stays there in while loop and does not proceed further if a fault is identified.							
3	End to End ECC for MSS R4F TCM Memories	TCMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. An 8-bit code word is used to store the ECC data as calculated over the 64-bit data bus. ECC evaluation is done by the ECC control logic inside the CPU. This scheme provides end-to-end diagnostics on the transmissions between CPU and TCM. CPU is configured to have predetermined response (Ignore or Abort generation) to single and double bit error conditions.							
4	MSS R4F TCM bit multiplexing	Logical TCM word and its associated ECC code is split and stored in two physical SRAM banks. This scheme provides an inherent diagnostic mechanism for address decode failures in the physical SRAM banks. Faults in the bank addressing are detected by the CPU as an ECC fault. Further, bit multiplexing scheme implemented such that the bits accessed to generate a logical (CPU) word are not physically adjacent. This scheme helps to reduce the probability of physical multi-bit faults resulting in logical multi-bit faults; rather they manifest as multiple single bit faults. As the SECDED TCM ECC can correct a single bit fault in a logical word, this scheme improves the usefulness of the TCM ECC diagnostic.							
5	Clock Monitor	AWR1243 architecture supports Three Digital Clock Comparators (DCCs) and an internal RCOSC. Dual functionality is provided by these modules – Clock detection and Clock Monitoring.  DCCint is used to check the availability/range of Reference clock at boot otherwise the device is moved into limp mode (Device still boots but on 10MHz RCOSC clock source. This provides debug capability). DCCint is only used by boot loader during boot time. It is disabled once the APLL is enabled and locked.  DCC1 is dedicated for APLL lock detection monitoring, comparing the APLL output divided version with the Reference input clock of the device. Initially (before configuring APLL), DCC1 is used by bootloader to identify the precise frequency of reference input clock against the internal RCOSC clock source. Failure detection for DCC1 would cause the device to go into limp mode.  Clock Compare module (CCC) module is used to compare the APLL divided down frequency with reference clock (XTAL). Failure detection is indicated by the nERROR OUT signal.							
6	RTI/WD for MSS R4F	Internal watchdog is enabled by the bootloader in a windowed watchdog (DWWD) mode  Watchdog expiry issues an internal warm reset and nERROR OUT signal to the host.							
7	MPU for MSS R4F	Cortex-R4F CPU includes an MPU. The MPU logic can be used to provide spatial separation of software tasks in the device memory. Cortex-R4F MPU supports 12 regions. It is expected that the operating system controls the MPU and changes the MPU settings based on the needs of each task. A violation of a configured memory protection policy results in a CPU abort.							
8	PBIST for Peripheral interface SRAMs - SPI, I2C	AWR1243 architecture supports a hardware programmable memory BIST (PBIST) engine for Peripheral SRAMs as well.  PBIST for peripheral SRAM memories is triggered by the bootloader. The PBIST tests are destructive to memory contents, and as such are typically run only at boot time  Any fault detected by the PBIST results in an error indicated in PBIST and boot status response message.							



### Table 10-1. Monitoring and Diagnostic Mechanisms for AWR1243 (continued)

S No	Feature	g and Diagnostic Mechanisms for AWR1243 (continued)  Description
9	ECC for Peripheral interface SRAMs – SPI, I2C	Peripheral interface SRAMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. When a single or double bit error is detected the error is indicated by nERROR (double bit error) or via SPI message (single bit error).
10	Cyclic Redundancy Check – Main SS	Cyclic Redundancy Check (CRC) module is available for the Main SS. The firmware uses this feature for data transfer checks in mailbox and SPI communication.
11	MPU for DMAs	AWR1243 architecture supports MPUs on Main SS DMAs. The firmware uses this for stack protection.
12	Boot time LBIST For BIST R4F Core and associated VIM	AWR1243 architecture supports hardware logic BIST (LBIST) even for BIST R4F core and associated VIM module. This logic provides very high diagnostic coverage (>90%) on the BIST R4F CPU core and VIM.  This is triggered by MSS R4F boot loader at boot time and it does not proceed further if the fault is detected.
13	Boot time PBIST for BIST R4F TCM Memories	AWR1243 architecture supports a hardware programmable memory BIST (PBIST) engine for BIST R4F TCMs which provide a very high diagnostic coverage (March-13n) on the BIST R4F TCMs. PBIST is triggered at the power up of the BIST R4F.
14	End to End ECC for BIST R4F TCM Memories	BIST R4F TCMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. Single bit error is communicated to the BIST R4FCPU while double bit error is communicated to MSS R4F as an interrupt which sends a async event to the host.
15	BIST R4F TCM bit multiplexing	Logical TCM word and its associated ECC code is split and stored in two physical SRAM banks. This scheme provides an inherent diagnostic mechanism for address decode failures in the physical SRAM banks and helps to reduce the probability of physical multi-bit faults resulting in logical multi-bit faults.
16	Temperature Sensors	AWR1243 architecture supports various temperature sensors all across the device (next to power hungry modules such as PAs, DSP etc) which is monitored during the inter-frame period. <sup>(1)</sup>
17	Tx Power Monitors	AWR1243 architecture supports power detectors at the Tx output. (2)
18	Error Signaling Error Output	When a diagnostic detects a fault, the error must be indicated. The AWR1243 architecture provides aggregation of fault indication from internal monitoring/diagnostic mechanisms using nERROR signaling or async event over SPI interface.
19	Synthesizer (Chirp) frequency monitor	Monitors Synthesizer's frequency ramp by counting (divided-down) clock cycles and comparing to ideal frequency ramp. Excess frequency errors above a certain threshold, if any, are detected and reported.
20	Ball break detection for TX ports (TX Ball break monitor)	AWR1243 architecture supports a ball break detection mechanism based on Impedance measurement at the TX output(s) to detect and report any large deviations that can indicate a ball break.  Monitoring is done by TIs code running on BIST R4F and failure is reported to the host. It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4F.
21	RX loopback test	Built-in TX to RX loopback to enable detection of failures in the RX path(s), including Gain, inter-RX balance, etc.
22	IF loopback test	Built-in IF (square wave) test tone input to monitor IF filter's frequency response and detect failure.
23	RX saturation detect	Provision to detect ADC saturation due to excessive incoming signal level and/or interference.

- (1) Monitoring is done by the Tl's code running on BIST R4F. There are two modes in which it could be configured to report the temperature sensed via API by customer application.
  - a. Report the temperature sensed after every N frames
  - b. Report the condition once the temperature crosses programmed threshold.

It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4Fvia Mailbox.

- (2) Monitoring is done by the TI's code running on BIST R4F.
  - There are two modes in which it could be configured to report the detected output power via API by customer application.
  - a. Report the power detected after every N frames
  - b. Report the condition once the output power degrades by more than configured threshold from the configured.

It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4F.



Note

Refer to the Device Safety Manual or other relevant collaterals for more details on applicability of all diagnostics mechanisms. For certification details, refer to the device product folder.

# 11 Applications, Implementation, and Layout

#### **Note**

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 11.1 Application Information

A typical application addresses the standard short-, mid-, long-range, and high-performance imaging radar applications with this radar front end and external programmable MCU. Figure 11-1 shows a short-, medium-, or long-range radar application.

## 11.2 Short-, Medium-, and Long-Range Radar

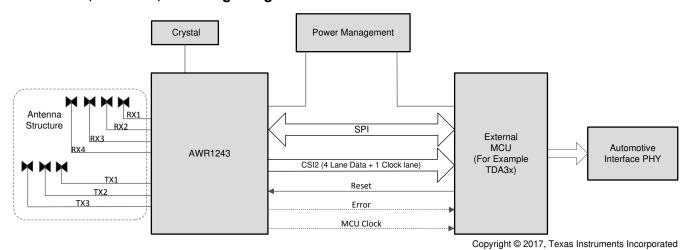


Figure 11-1. Short-, Medium-, and Long-Range Radar



## 11.3 Reference Schematic

The reference schematic and power supply information can be found in the AWR1243 EVM Documentation.

Listed for convenience are: Design Files, Schematics, Layouts, and Stack up for PCB.

- Altium AWR1243 EVM Design Files
- AWR1243 EVM Schematic Drawing, Assembly Drawing, and Bill of Materials

# 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

#### 12.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *AWR1243*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- **X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- **P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

**null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing. **TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. Tl's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL0161 ALB0161), the temperature range (for example, blank is the default commercial temperature range). Figure 12-1 provides a legend for reading the complete device name for any *AWR1243* device.

For orderable part numbers of *AWR1243* devices in the ABL0161 package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the AWR1243 Device Errata.

44

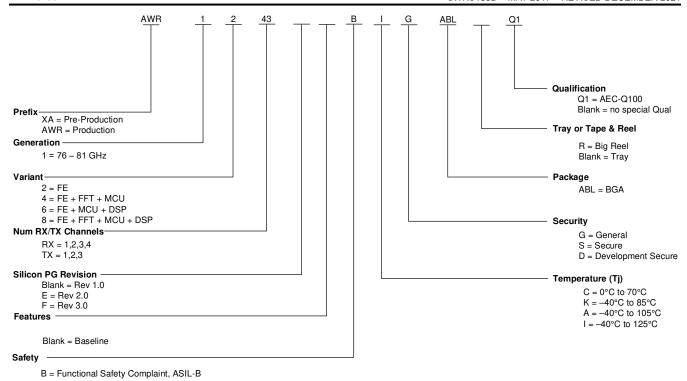


Figure 12-1. Device Nomenclature

#### 12.2 Tools and Software

#### **Development Tools**

AWR1243 cascade application note Describes TI's cascaded mmWave radar system.

#### Models

AWR1243 BSDL model	Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.
AWR1x43 IBIS model	IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.
AWR1243 checklist for schematic review, layout review, bringup/wakeup	A set of steps in spreadsheet form to select system functions and pinmux options. Specific EVM schematic and layout notes to apply to customer engineering. A bringup checklist is suggested for customers.

#### 12.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

#### **Errata**

AWR1243 device errata Describes known advisories, limitations, and cautions on silicon and provides workarounds.

#### 12.4 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 12.5 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

## 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.7 Glossary

TI Glossary

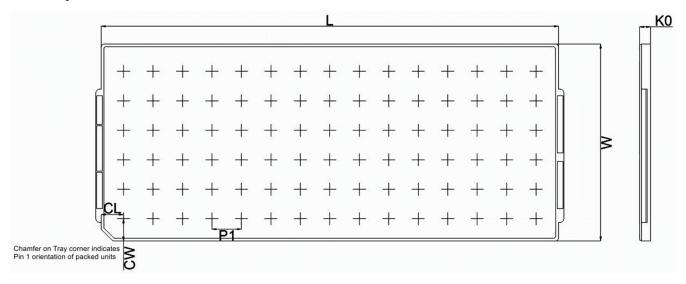
This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

## 13.1 Packaging Information

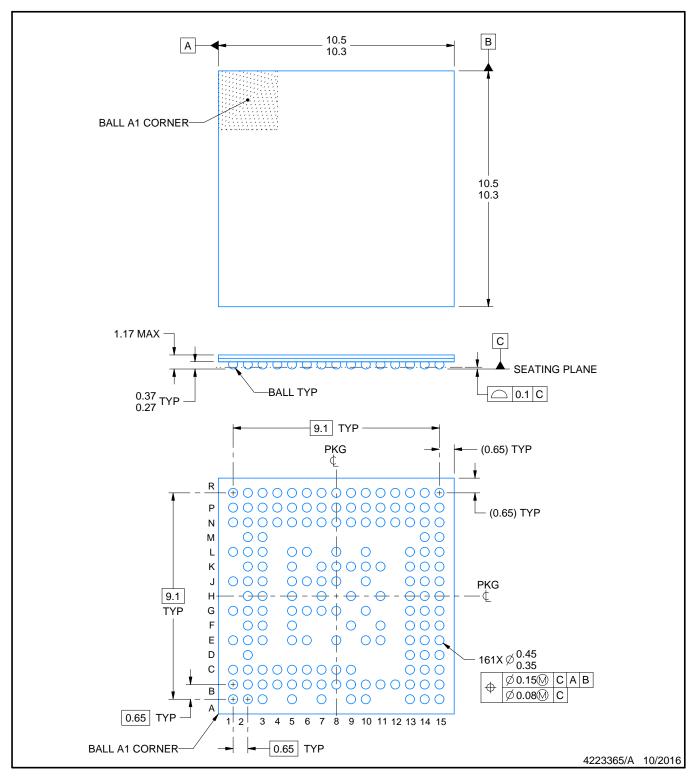
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 13.2 Tray Information for





PLASTIC BALL GRID ARRAY

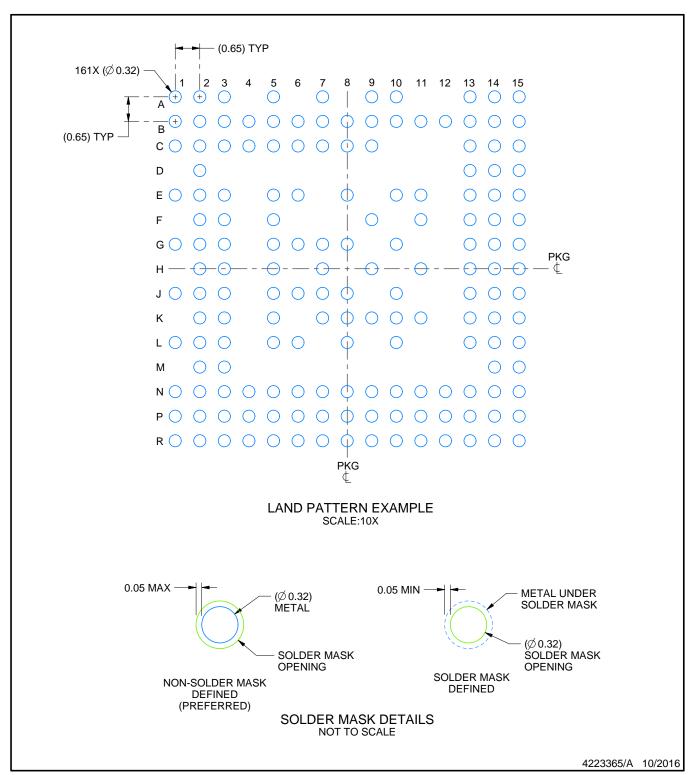


#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



PLASTIC BALL GRID ARRAY

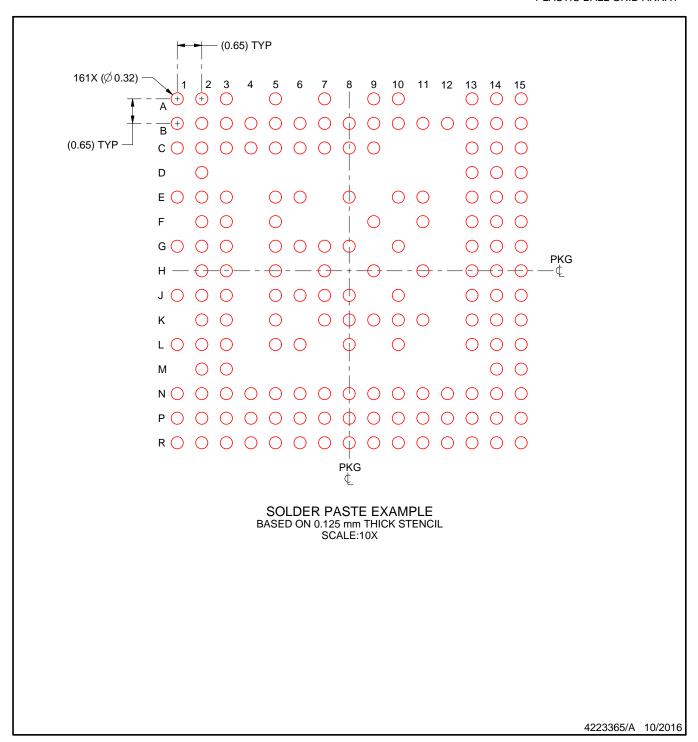


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



PLASTIC BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



www.ti.com 9-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	age   Pins Package qty   Carrier		Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)	
AWR1243FBIGABLQ1	Active	Production	FCCSP (ABL)   161	176   JEDEC TRAY (10+1)	-	Call TI	Level-3-260C-168 HR	-40 to 125	AWR1243 IG 964FC	
AWR1243FBIGABLQ1.B	Active	Production	FCCSP (ABL)   161	176   JEDEC TRAY (10+1)		Call TI	Level-3-260C-168 HR	-40 to 125	AWR1243 IG 964FC	
AWR1243FBIGABLRQ1	Active	Production	FCCSP (ABL)   161	1000   LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	AWR1243 IG 964FC ABL G1	
AWR1243FBIGABLRQ1.B	Active	Production	FCCSP (ABL)   161	1000   LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	AWR1243 IG 964FC ABL G1	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# PACKAGE OPTION ADDENDUM

www.ti.com 9-Nov-2025

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



www.ti.com 23-May-2025

#### **TRAY**



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

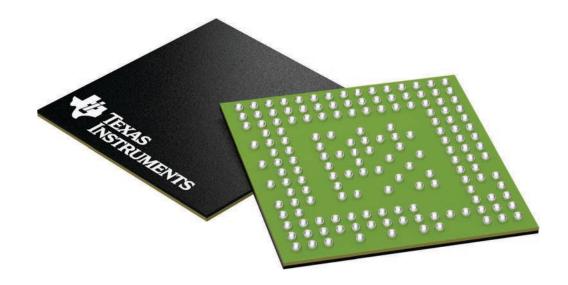
#### \*All dimensions are nominal

	Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	Κ0 (μm)	P1 (mm)	CL (mm)	CW (mm)
	AWR1243FBIGABLQ1	ABL	FCCSP	161	176	8 x 22	150	315	135.9	7620	13.4	16.8	17.2
	AWR1243FBIGABLQ1.B	ABL	FCCSP	161	176	8 x 22	150	315	135.9	7620	13.4	16.8	17.2

10.4 x 10.4, 0.65 mm pitch

PLASTIC BALL GRID ARRAY

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025