

# AMC23C15-Q1 Automotive, Dual, Fast Response, Reinforced Isolated Window Comparator With Adjustable Threshold

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
- Wide high-side supply range: 3V to 27V
- Low-side supply range: 2.7V to 5.5V
- Dual window comparator:
  - Window comparator 1:  $\pm 5\text{mV}$  to  $\pm 300\text{mV}$  adjustable threshold
  - Window comparator 2:  $\pm 60\text{mV}$  fixed threshold
- Supports positive-comparator mode:
  - Cmp0: 600mV to 2.7V adjustable threshold
  - Cmp2: 60mV fixed threshold
  - Cmp1 and Cmp3: Disabled
- Reference current for threshold adjustment:  $100\mu\text{A}$ ,  $\pm 1\%$
- Trip threshold error:  $\pm 1\%$  (max) at 250mV
- Open-drain outputs
- Propagation delay: 280ns (typ)
- High CMTI: 15V/ns (min)
- Safety-related certifications:
  - 7000V<sub>PK</sub> reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5000V<sub>RMS</sub> isolation for 1 minute per UL1577

## 2 Applications

- Overcurrent or overvoltage detection in:
  - [Solid-state relays \(SSR\)](#)
  - [Motor drives](#)
  - [Frequency inverters](#)
  - [Solar inverters](#)
  - [DC/DC converters](#)

## 3 Description

The AMC23C15-Q1 is a dual, isolated window comparator with a short response time. The open-drain outputs are separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5kV<sub>RMS</sub> according to VDE 0884-17 and UL1577, and supports a working voltage of up to 1kV<sub>RMS</sub>.

Both comparators have windows that are centered around 0V, meaning that the comparators trip if the input exceeds the thresholds in a positive or negative direction. One comparator has fixed thresholds of  $\pm 60\text{mV}$ . The second comparator has adjustable thresholds from  $\pm 5\text{mV}$  to  $\pm 300\text{mV}$  through a single external resistor.

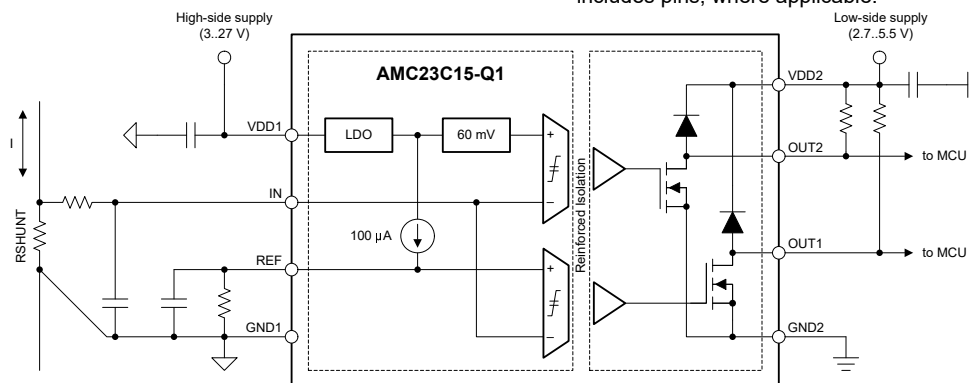
The AMC23C15-Q1 also supports a positive-comparator only mode. When the voltage on the REF pin is greater than 550mV, the negative comparators are disabled and only the positive comparators are functional. The reference voltage in this mode can be as high as 2.7V. This mode is particularly useful for monitoring positive voltage supplies.

The AMC23C15-Q1 is offered in a wide-body 8-pin SOIC package, is AEC-Q100 qualified for automotive applications, and supports the temperature range from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| AMC23C15-Q1 | DWV (SOIC, 8)          | 5.85mm × 11.5mm             |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



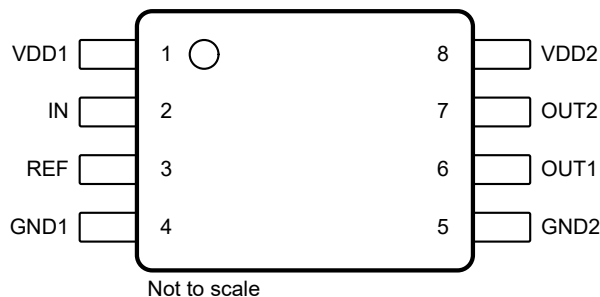
Typical Application



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## 4 Pin Configuration and Functions



**Figure 4-1. DWV Package, 8-Pin SOIC (Top View)**

**Table 4-1. Pin Functions**

| PIN |      | TYPE             | DESCRIPTION   |
|-----|------|------------------|---|
| NO. | NAME |                  |   |
| 1   | VDD1 | High-side power  | High-side power supply. <sup>(1)</sup>  |
| 2   | IN   | Analog input     | Common analog input pin for window comparator 1 and 2.  |
| 3   | REF  | Analog input     | Reference pin that defines the trip threshold for window comparator 1. The voltage on this pin also affects the hysteresis of comparator Cmp0, as explained in the <a href="#">Reference Input</a> section. This pin is internally connected to a 100-μA current source. Connect a resistor from REF to GND1 to define the trip threshold, and a capacitor from REF to GND1 to filter the reference voltage. For best transient noise immunity, place the capacitor as closely to the pin as possible. This pin can also be driven by an external voltage source. |
| 4   | GND1 | High-side ground | High-side ground.   |
| 5   | GND2 | Low-side ground  | Low-side ground.  |
| 6   | OUT1 | Digital output   | Open-drain output of window comparator 1. Connect to an external pullup resistor or leave unconnected (floating) when not used.   |
| 7   | OUT2 | Digital output   | Open-drain output of window comparator 2. Connect to an external pullup resistor or leave unconnected (floating) when not used.   |
| 8   | VDD2 | Low-side power   | Low-side power supply. <sup>(1)</sup>   |

(1) See the [Layout](#) section for power-supply decoupling recommendations.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

see<sup>(1)</sup>

|                        |  | MIN  | MAX        | UNIT |
|------------------------|--|------|------------|------|
| Power-supply voltage   | VDD1 to GND1                                 | −0.3 | 30         | V    |
|                        | VDD2 to GND2                                 | −0.3 | 6.5        |      |
| Analog input voltage   | REF to GND1                                  | −0.5 | 6.5        | V    |
|                        | IN to GND1                                   | −6   | 5.5        |      |
| Digital output voltage | OUT1, OUT2 to GND2                           | −0.5 | VDD2 + 0.5 | V    |
| Input current          | Continuous, any pin except power-supply pins | −10  | 10         | mA   |
| Temperature            | Junction, T <sub>J</sub>                     |      | 150        | °C   |
|                        | Storage, T <sub>stg</sub>                    | −65  | 150        |      |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings

|                    |                         |  | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> , HBM ESD classification Level 2 | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per AEC Q100-011, CDM ESD classification Level C6            | ±1000 |      |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

|                          |   |                                  |  | MIN               | NOM        | MAX                 | UNIT |
|--------------------------|---|----------------------------------|--|-------------------|------------|---------------------|------|
| <b>POWER SUPPLY</b>      |   |                                  |  |                   |            |                     |      |
| V <sub>VDD1</sub>        | High-side power-supply voltage              | VDD1 to GND1                     |  | 3.0               | 5          | 25                  | V    |
| V <sub>VDD2</sub>        | Low-side power supply voltage               | VDD2 to GND2                     |  | 2.7               | 3.3        | 5.5                 | V    |
| <b>ANALOG INPUT</b>      |   |                                  |  |                   |            |                     |      |
| V <sub>IN</sub>          | Input voltage                               | IN to GND1, VDD1 ≤ 4.3 V         |  | –0.4              | VDD1 – 0.3 |                     | V    |
|                          |   | IN to GND1, VDD1 > 4.3 V         |  | –0.4              | 4          |                     |      |
| V <sub>REF</sub>         | Reference voltage, window comparator mode   | REF to GND1                      |  | 20 <sup>(2)</sup> |            | 300                 | mV   |
|                          | Reference voltage, positive-comparator mode | Low hysteresis mode              |  | 20 <sup>(2)</sup> |            | 450                 |      |
|                          |   | High hysteresis mode (Cmp0 only) |  | 600               |            | 2700 <sup>(1)</sup> |      |
|                          | Reference voltage headroom                  | VDD1 – V <sub>REF</sub>          |  | 1.4               |            |                     | V    |
|                          | Filter capacitance on REF pin               |                                  |  | 20                | 100        |                     | nF   |
| <b>DIGITAL OUTPUTS</b>   |   |                                  |  |                   |            |                     |      |
|                          | Digital output voltage                      | OUT1, OUT2 to GND2               |  | GND2              |            | VDD2                | V    |
|                          | Sink current                                | OUT1, OUT2                       |  | 0                 |            | 4                   | mA   |
| <b>TEMPERATURE RANGE</b> |   |                                  |  |                   |            |                     |      |
| T <sub>A</sub>           | Specified ambient temperature               |                                  |  | –40               | 25         | 125                 | °C   |

- (1) Reference voltages (V<sub>REF</sub>) > 1.6V require V<sub>VDD1</sub> > V<sub>VDD1,MIN</sub> to maintain minimum headroom (V<sub>VDD1</sub> – V<sub>REF</sub>) of 1.4V.  
(2) The device has been tested with V<sub>REF</sub> as low as 5mV. The device remains functional but relative switching threshold accuracy can decrease because of offset errors.

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | DWV (SOIC) | UNIT |
|-------------------------------|--|------------|------|
|                               |  | 8 PINS     |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 102.8      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 45.1       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 63.0       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 14.3       | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 61.1       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | n/a        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Power Ratings

| PARAMETER       |  | TEST CONDITIONS           | VALUE | UNIT |
|-----------------|--|---------------------------|-------|------|
| P <sub>D</sub>  | Maximum power dissipation (both sides) | VDD1 = 25 V, VDD2 = 5.5 V | 110   | mW   |
|                 |  | VDD1 = VDD2 = 5.5 V       | 34    |      |
|                 |  | VDD1 = VDD2 = 3.6 V       | 22    |      |
| P <sub>D1</sub> | Maximum power dissipation (high-side)  | VDD1 = 25 V               | 98    | mW   |
|                 |  | VDD1 = 5.5 V              | 21    |      |
|                 |  | VDD1 = 3.6 V              | 14    |      |
| P <sub>D2</sub> | Maximum power dissipation (low-side)   | VDD2 = 5.5 V              | 12    | mW   |
|                 |  | VDD2 = 3.6 V              | 8     |      |

## 5.6 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS   | VALUE              | UNIT             |
|--|---|---|--------------------|------------------|
| GENERAL  |   |   |                    |                  |
| CLR  | External clearance <sup>(1)</sup>                     | Shortest pin-to-pin distance through air  | ≥ 8.5              | mm               |
| CPG  | External creepage <sup>(1)</sup>                      | Shortest pin-to-pin distance across the package surface   | ≥ 8.5              | mm               |
| DTI  | Distance through insulation                           | Minimum internal gap (internal clearance) of the double insulation  | ≥ 15.4             | μm               |
| CTI  | Comparative tracking index                            | DIN EN 60112 (VDE 0303-11); IEC 60112   | ≥ 600              | V                |
|  | Material group  | According to IEC 60664-1  | I                  |                  |
|  | Overvoltage category per IEC 60664-1                  | Rated mains voltage ≤ 600V <sub>RMS</sub>   | I-III              |                  |
|  |   | Rated mains voltage ≤ 1000V <sub>RMS</sub>  | I-II               |                  |
| DIN EN IEC 60747-17 (VDE 0884-17) <sup>(2)</sup> |   |   |                    |                  |
| V <sub>IORM</sub>                                | Maximum repetitive peak isolation voltage             | At AC voltage   | 1410               | V <sub>PK</sub>  |
| V <sub>IOWM</sub>                                | Maximum-rated isolation working voltage               | At AC voltage (sine wave)   | 1000               | V <sub>RMS</sub> |
|  |   | At DC voltage   | 1410               | V <sub>DC</sub>  |
| V <sub>IOTM</sub>                                | Maximum transient isolation voltage                   | V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60s (qualification test),<br>V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1s (100% production test)  | 7070               | V <sub>PK</sub>  |
| V <sub>IMP</sub>                                 | Maximum impulse voltage <sup>(3)</sup>                | Tested in air, 1.2/50μs waveform per IEC 62368-1  | 7700               | V <sub>PK</sub>  |
| V <sub>IOSM</sub>                                | Maximum surge isolation voltage <sup>(4)</sup>        | Tested in oil (qualification test),<br>1.2/50μs waveform per IEC 62368-1  | 10000              | V <sub>PK</sub>  |
| q <sub>pd</sub>                                  | Apparent charge <sup>(5)</sup>                        | Method a, after input/output safety test subgroups 2 and 3,<br>V <sub>pd(ini)</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60s, V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10s       | ≤ 5                | pC               |
|  |   | Method a, after environmental tests subgroup 1,<br>V <sub>pd(ini)</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60s, V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10s                   | ≤ 5                |                  |
|  |   | Method b1, at preconditioning (type test) and routine test,<br>V <sub>pd(ini)</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = 1s, V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> , t <sub>m</sub> = 1s | ≤ 5                |                  |
|  |   | Method b2, at routine test (100% production) <sup>(7)</sup><br>V <sub>pd(ini)</sub> = V <sub>pd(m)</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = t <sub>m</sub> = 1s                                 | ≤ 5                |                  |
| C <sub>IO</sub>                                  | Barrier capacitance, input to output <sup>(6)</sup>   | V <sub>IO</sub> = 0.5 V <sub>PP</sub> at 1MHz   | ≅ 1.5              | pF               |
| R <sub>IO</sub>                                  | Insulation resistance, input to output <sup>(6)</sup> | V <sub>IO</sub> = 500V at T <sub>A</sub> = 25°C   | > 10 <sup>12</sup> | Ω                |
|  |   | V <sub>IO</sub> = 500V at 100°C ≤ T <sub>A</sub> ≤ 125°C  | > 10 <sup>11</sup> |                  |
|  |   | V <sub>IO</sub> = 500V at T <sub>S</sub> = 150°C  | > 10 <sup>9</sup>  |                  |
|  | Pollution degree                                      |   | 2                  |                  |
|  | Climatic category                                     |   | 55/125/21          |                  |
| UL1577   |   |   |                    |                  |
| V <sub>ISO</sub>                                 | Withstand isolation voltage                           | V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60s (qualification test),<br>V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1s (100% production test)  | 5000               | V <sub>RMS</sub> |

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.
- (7) Either method b1 or b2 is used in production.

## 5.7 Safety-Related Certifications

| VDE   | UL  |
|---|---|
| DIN EN IEC 60747-17 (VDE 0884-17),<br>EN IEC 60747-17,<br>DIN EN IEC 62368-1 (VDE 0868-1),<br>EN IEC 62368-1,<br>IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9 | Recognized under 1577 component recognition and<br>CSA component acceptance NO 5 programs |
| Reinforced insulation   | Single protection   |
| Certificate number: 40040142  | File number: E181974  |

## 5.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER      |   | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT |
|----------------|---|--|-----|-----|------|------|
| I <sub>S</sub> | Safety input, output, or supply current | R <sub>θJA</sub> = 102.8°C/W,<br>VDD1 = VDD2 = 5.5 V,<br>T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C |     |     | 220  | mA   |
|                |   | R <sub>θJA</sub> = 102.8°C/W,<br>VDD1 = VDD2 = 3.6 V,<br>T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C |     |     | 340  |      |
| P <sub>S</sub> | Safety input, output, or total power    | R <sub>θJA</sub> = 102.8°C/W,<br>T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C                         |     |     | 1220 | mW   |
| T <sub>S</sub> | Maximum safety temperature              |  |     |     | 150  | °C   |

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P, where P is the power dissipated in the device.

T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum junction temperature.

P<sub>S</sub> = I<sub>S</sub> × AVDD<sub>max</sub> + I<sub>S</sub> × DVDD<sub>max</sub>, where AVDD<sub>max</sub> is the maximum high-side voltage and DVDD<sub>max</sub> is the maximum controller-side supply voltage.

## 5.9 Electrical Characteristics

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{DD1} = 3.0\text{ V}$  to  $25\text{ V}$ ,  $V_{DD2} = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $V_{REF} = 20\text{ mV}$  to  $2.7\text{ V}$ <sup>(1)</sup>, and  $V_{IN} = -400\text{ mV}$  to  $4\text{ V}$ <sup>(3)</sup>; typical specifications are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ , and  $V_{REF} = 250\text{ mV}$  (unless otherwise noted)

| PARAMETER   |   | TEST CONDITIONS  | MIN  | TYP                                  | MAX | UNIT |
|---|---|--|------|--------------------------------------|-----|------|
| ANALOG INPUT                                      |   |  |      |                                      |     |      |
| R <sub>IN</sub>                                   | Input resistance                        | IN pin, 0 ≤ V <sub>IN</sub> ≤ 4 V  |      | 1                                    |     | GΩ   |
| I <sub>BIAS</sub>                                 | Input bias current                      | IN pin, 0 ≤ V <sub>IN</sub> ≤ 4 V <sup>(4)</sup>   |      | 0.1                                  | 25  | nA   |
|   |   | IN pin, −400 mV ≤ V <sub>IN</sub> ≤ 0 V <sup>(5)</sup>   | −310 | −0.5                                 |     |      |
| C <sub>IN</sub>                                   | Input capacitance                       | IN pin   |      | 4                                    |     | pF   |
| REFERENCE PIN                                     |   |  |      |                                      |     |      |
| I <sub>REF</sub>                                  | Reference current                       | REF to GND1, 20 mV < V <sub>REF</sub> ≤ 2.7 V  | 99   | 100                                  | 101 | μA   |
| V <sub>MSEL</sub>                                 | Mode selection threshold <sup>(2)</sup> | V <sub>REF</sub> rising  | 500  | 550                                  | 600 | mV   |
|   |   | V <sub>REF</sub> falling   | 450  | 500                                  | 550 |      |
|   | Mode selection threshold hysteresis     |  |      | 50                                   |     | mV   |
| 60-mV FIXED-THRESHOLD COMPARATORS (CMP2 and CMP3) |   |  |      |                                      |     |      |
| V <sub>IT+</sub>                                  | Positive-going trip threshold           | Cmp2   |      | 64                                   |     | mV   |
| E <sub>IT+</sub>                                  | Positive-going trip threshold error     | Cmp2   | −3.5 |                                      | 3.5 | mV   |
| V <sub>IT−</sub>                                  | Negative-going trip threshold           | Cmp2   |      | 60                                   |     | mV   |
| E <sub>IT−</sub>                                  | Negative-going trip threshold error     | Cmp2   | −3.5 |                                      | 3.5 | mV   |
| V <sub>IT−</sub>                                  | Negative-going trip threshold           | Cmp3   |      | −64                                  |     | mV   |
| E <sub>IT−</sub>                                  | Negative-going trip threshold error     | Cmp3   | −4.5 |                                      | 4.5 | mV   |
| V <sub>IT+</sub>                                  | Positive-going trip threshold           | Cmp3   |      | −60                                  |     | mV   |
| E <sub>IT+</sub>                                  | Positive-going trip threshold error     | Cmp3   | −4.5 |                                      | 4.5 | mV   |
| V <sub>HYS</sub>                                  | Trip threshold hysteresis               | Cmp2 and Cmp3; (V <sub>IT+</sub> − V <sub>IT−</sub> )  |      | 4                                    |     | mV   |
| VARIABLE-THRESHOLD COMPARATORS (CMP0 AND CMP1)    |   |  |      |                                      |     |      |
| V <sub>IT+</sub>                                  | Positive-going trip threshold           | Cmp0   |      | V <sub>REF</sub> + V <sub>HYS</sub>  |     | mV   |
| E <sub>IT+</sub>                                  | Positive-going trip threshold error     | Cmp0, (V <sub>IT+</sub> − V <sub>REF</sub> − V <sub>HYS</sub> ),<br>V <sub>REF</sub> = 20 mV, V <sub>HYS</sub> = 4 mV  | −2   |                                      | 2   | mV   |
|   |   | Cmp0, (V <sub>IT+</sub> − V <sub>REF</sub> − V <sub>HYS</sub> ),<br>V <sub>REF</sub> = 250 mV, V <sub>HYS</sub> = 4 mV | −2   |                                      | 2   |      |
|   |   | Cmp0, (V <sub>IT+</sub> − V <sub>REF</sub> − V <sub>HYS</sub> ),<br>V <sub>REF</sub> = 2 V, V <sub>HYS</sub> = 25 mV   | −5   |                                      | 5   |      |
| V <sub>IT−</sub>                                  | Negative-going trip threshold           | Cmp0   |      | V <sub>REF</sub>                     |     | mV   |
| E <sub>IT−</sub>                                  | Negative-going trip threshold error     | Cmp0, (V <sub>IT−</sub> − V <sub>REF</sub> ), V <sub>REF</sub> = 20 mV   | −2.5 |                                      | 2.5 | mV   |
|   |   | Cmp0, (V <sub>IT−</sub> − V <sub>REF</sub> ), V <sub>REF</sub> = 250 mV  | −2.5 |                                      | 2.5 |      |
|   |   | Cmp0, (V <sub>IT−</sub> − V <sub>REF</sub> ), V <sub>REF</sub> = 2 V   | −5   |                                      | 5   |      |
| V <sub>IT−</sub>                                  | Negative-going trip threshold           | Cmp1   |      | −V <sub>REF</sub> − V <sub>HYS</sub> |     | mV   |
| E <sub>IT−</sub>                                  | Negative-going trip threshold error     | Cmp1, (V <sub>IT−</sub> + V <sub>REF</sub> + V <sub>HYS</sub> ),<br>V <sub>REF</sub> = 20 mV, V <sub>HYS</sub> = 4 mV  | −3   |                                      | 3   | mV   |
|   |   | Cmp1, (V <sub>IT−</sub> + V <sub>REF</sub> + V <sub>HYS</sub> ),<br>V <sub>REF</sub> = 250 mV, V <sub>HYS</sub> = 4 mV | −3   |                                      | 3   |      |
| V <sub>IT+</sub>                                  | Positive-going trip threshold           | Cmp1   |      | −V <sub>REF</sub>                    |     | mV   |
| E <sub>IT+</sub>                                  | Positive-going trip threshold error     | Cmp1, (V <sub>IT+</sub> + V <sub>REF</sub> ), V <sub>REF</sub> = 20 mV   | −3.5 |                                      | 3.5 | mV   |
|   |   | Cmp1, (V <sub>IT+</sub> + V <sub>REF</sub> ), V <sub>REF</sub> = 250 mV  | −3.5 |                                      | 3.5 |      |
| V <sub>HYS</sub>                                  | Trip threshold hysteresis               | Cmp0 and Cmp1, (V <sub>IT+</sub> − V <sub>IT−</sub> ), V <sub>REF</sub> ≤ 450 mV                                       |      | 4                                    |     | mV   |
|   |   | Cmp0 only, (V <sub>IT+</sub> − V <sub>IT−</sub> ), V <sub>REF</sub> ≥ 600 mV   |      | 25                                   |     |      |
| DIGITAL OUTPUTS                                   |   |  |      |                                      |     |      |
| V <sub>OL</sub>                                   | Low-level output voltage                | I <sub>SINK</sub> = 4 mA   |      | 80                                   | 250 | mV   |
| I <sub>LKG</sub>                                  | Open-drain output leakage current       | VDD2 = 5 V, V <sub>OUT</sub> = 5 V   |      | 5                                    | 100 | nA   |
| CMTI  | Common-mode transient immunity          | V <sub>IN</sub> − V <sub>REF</sub>   ≥ 4 mV, R <sub>PULLUP</sub> = 10 kΩ   | 15   | 40                                   |     | V/ns |



## 5.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{DD1} = 3.0\text{ V}$  to  $25\text{ V}$ ,  $V_{DD2} = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $V_{REF} = 20\text{ mV}$  to  $2.7\text{ V}$ <sup>(1)</sup>, and  $V_{IN} = -400\text{ mV}$  to  $4\text{ V}$ <sup>(3)</sup>; typical specifications are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ , and  $V_{REF} = 250\text{ mV}$  (unless otherwise noted)

| PARAMETER           |                                       | TEST CONDITIONS                               | MIN | TYP | MAX | UNIT |
|---------------------|---------------------------------------|---|-----|-----|-----|------|
| <b>POWER SUPPLY</b> |                                       |   |     |     |     |      |
| VDD1 <sub>UV</sub>  | VDD1 undervoltage detection threshold | VDD1 rising                                   |     |     | 3   | V    |
|                     |                                       | VDD1 falling                                  |     |     | 2.9 |      |
| VDD1 <sub>POR</sub> | VDD1 power-on reset threshold         | VDD1 falling                                  |     |     | 2.3 | V    |
| VDD2 <sub>UV</sub>  | VDD2 undervoltage detection threshold | VDD2 rising                                   |     |     | 2.7 | V    |
|                     |                                       | VDD2 falling                                  |     |     | 2.1 |      |
| I <sub>DD1</sub>    | High-side supply current              | $3.0\text{ V} \leq V_{DD1} \leq 3.4\text{ V}$ |     |     | 4.0 | mA   |
|                     |                                       | $3.4\text{ V} < V_{DD1} \leq 25\text{ V}$     |     | 3.2 | 4.3 |      |
| I <sub>DD2</sub>    | Low-side supply current               |   |     | 1.8 | 2.2 | mA   |

- (1) Reference voltages  $>1.6\text{ V}$  require  $V_{DD1} > V_{DD1\text{MIN}}$ . See the *Recommended Operation Conditions* table for details.
- (2) The voltage level  $V_{REF}$  determines if the device operates as window-comparator with positive and negative thresholds or as simple comparator with positive thresholds only. See the *Reference Input* section for more details.
- (3) But not exceeding the maximum input voltage specified in the *Recommended Operation Conditions* table.
- (4) The typical value is measured at  $V_{IN} = 0.4\text{ V}$ .
- (5) The typical value is measured at  $V_{IN} = -400\text{ mV}$ .

## 5.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

| PARAMETER           |   | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|---------------------|---|---|-----|-----|-----|------|
| OPEN-DRAIN OUTPUTS  |   |   |     |     |     |      |
| t <sub>pH</sub>     | Propagation delay time,  V <sub>IN</sub>   rising <sup>(1)</sup>  | VDD2 = 3.3 V, V <sub>REF</sub> = 250 mV, V <sub>OVERDRIVE</sub> = 10 mV, C <sub>L</sub> = 15 pF |     | 280 | 410 | ns   |
|                     |   | VDD2 = 3.3 V, V <sub>REF</sub> = 2 V, V <sub>OVERDRIVE</sub> = 50 mV, C <sub>L</sub> = 15 pF    |     | 240 | 370 |      |
| t <sub>pL</sub>     | Propagation delay time,  V <sub>IN</sub>   falling <sup>(1)</sup> | VDD2 = 3.3 V, V <sub>REF</sub> = 250 mV, V <sub>OVERDRIVE</sub> = 10 mV, C <sub>L</sub> = 15 pF |     | 280 | 410 | ns   |
|                     |   | VDD2 = 3.3 V, V <sub>REF</sub> = 2 V, V <sub>OVERDRIVE</sub> = 50 mV, C <sub>L</sub> = 15 pF    |     | 240 | 370 |      |
| t <sub>f</sub>      | Output signal fall time   | R <sub>PULLUP</sub> = 4.7 kΩ, C <sub>L</sub> = 15 pF  |     | 2   |     | ns   |
| MODE SELECTION      |   |   |     |     |     |      |
| t <sub>HSEL</sub>   | Comparator hysteresis selection deglitch time                     | Cmp0, V <sub>REF</sub> rising or falling  |     | 10  |     | μs   |
| t <sub>DIS13</sub>  | Comparator disable deglitch time                                  | Cmp1 and Cmp3, V <sub>REF</sub> rising  |     | 10  |     | μs   |
| t <sub>EN13</sub>   | Comparator enable deglitch time                                   | Cmp1 and Cmp3, V <sub>REF</sub> falling   |     | 100 |     | μs   |
| START-UP TIMING     |   |   |     |     |     |      |
| t <sub>LS,STA</sub> | Low-side start-up time  | VDD2 step to 2.7 V, VDD1 ≥ 3.0 V  |     | 40  |     | μs   |
| t <sub>HS,STA</sub> | High-side start-up time   | VDD1 step to 3.0 V, VDD2 ≥ 2.7 V  |     | 45  |     | μs   |
| t <sub>HS,BLK</sub> | High-side blanking time   |   |     | 200 |     | μs   |
| t <sub>HS,FLT</sub> | High-side-fault detection delay time                              |   |     | 100 |     | μs   |

(1) Valid for OUT1 and OUT2

## 5.11 Timing Diagrams

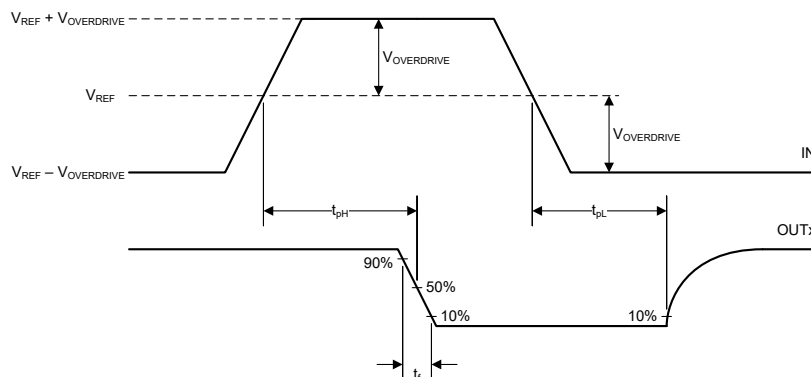


Figure 5-1. Rise, Fall, and Delay Time Definition

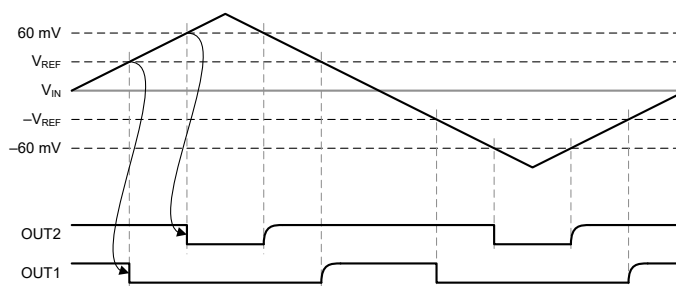
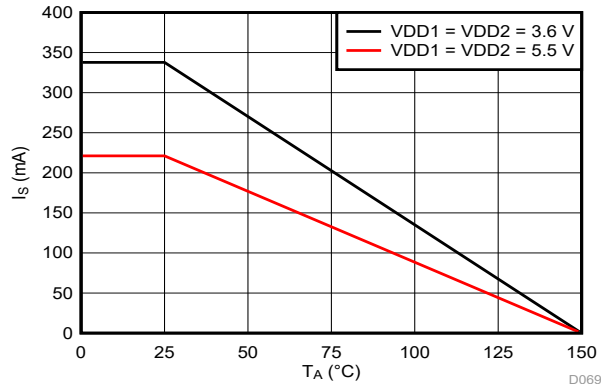
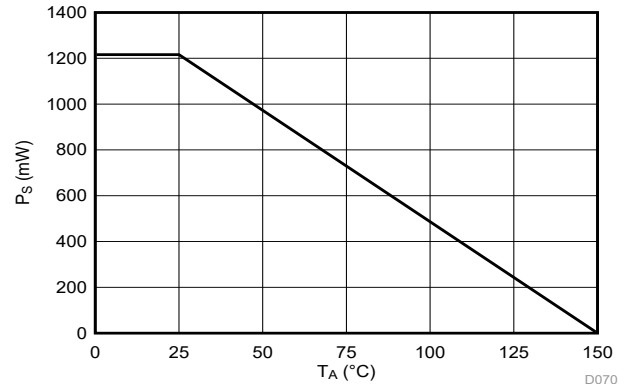


Figure 5-2. Functional Timing Diagram

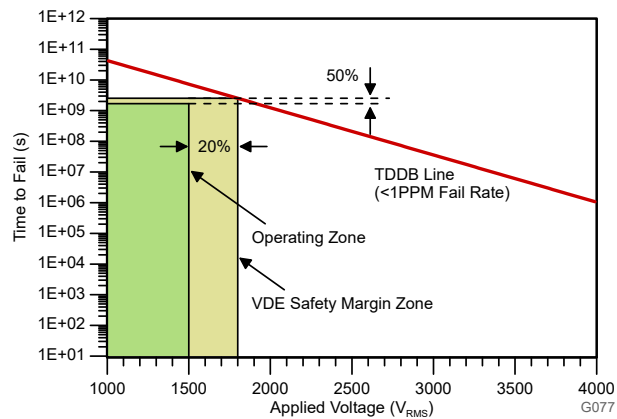
## 5.12 Insulation Characteristics Curves



**Figure 5-3. Thermal Derating Curve for Safety-Limiting Current per VDE**



**Figure 5-4. Thermal Derating Curve for Safety-Limiting Power per VDE**



$T_A$  up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1000V<sub>RMS</sub>, operating lifetime > 400 years

**Figure 5-5. Reinforced Isolation Capacitor Lifetime Projection**

## 5.13 Typical Characteristics

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

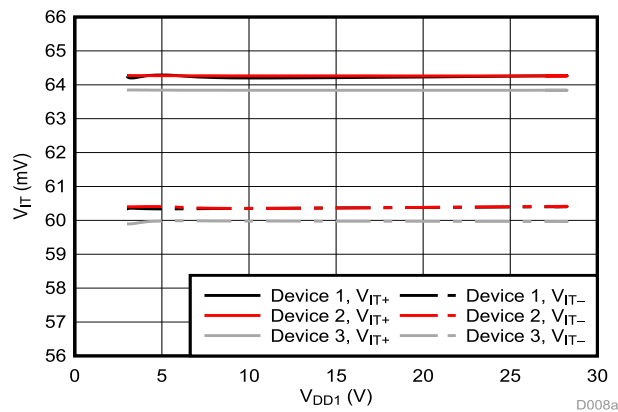


Figure 5-6. Cmp2 Trip Threshold vs Supply Voltage

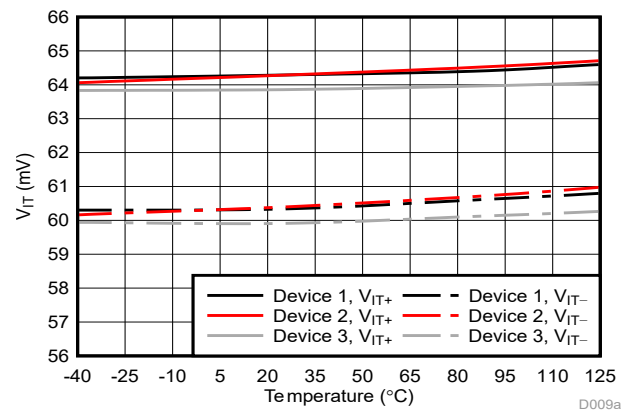


Figure 5-7. Cmp2 Trip Threshold vs Temperature

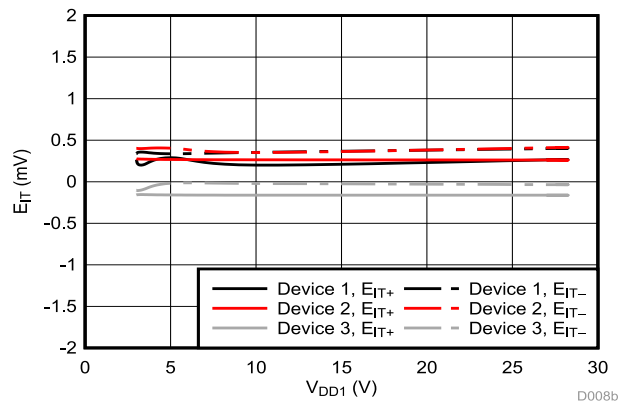


Figure 5-8. Cmp2 Trip Threshold Error vs Supply Voltage

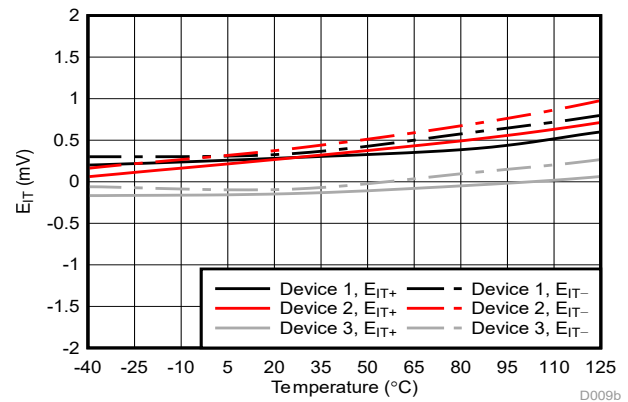


Figure 5-9. Cmp2 Trip Threshold Error vs Temperature

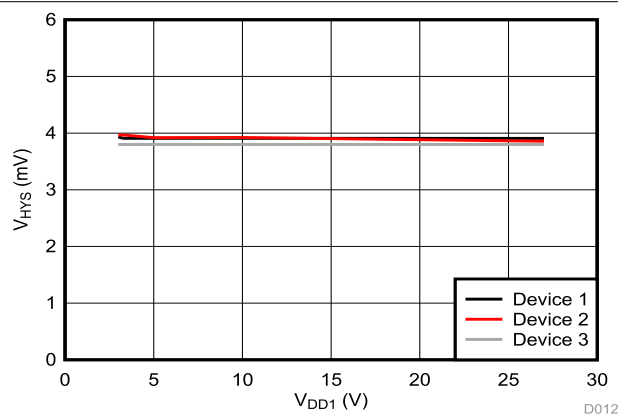


Figure 5-10. Cmp2 Trip Threshold Hysteresis vs Supply Voltage

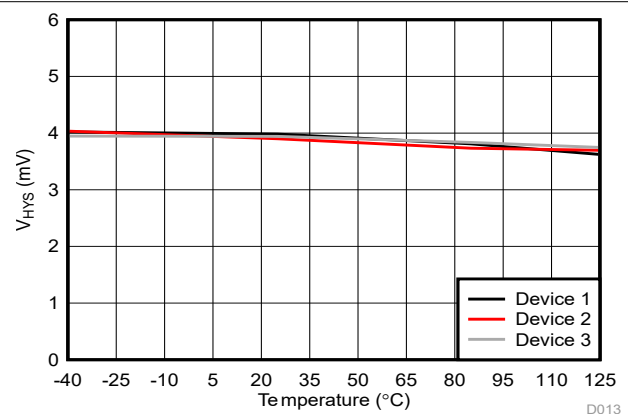


Figure 5-11. Cmp2 Trip Threshold Hysteresis vs Temperature

## 5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

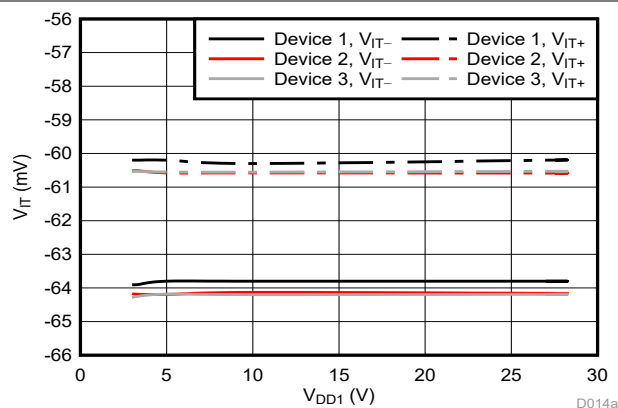


Figure 5-12. Cmp3 Trip Threshold vs Supply Voltage

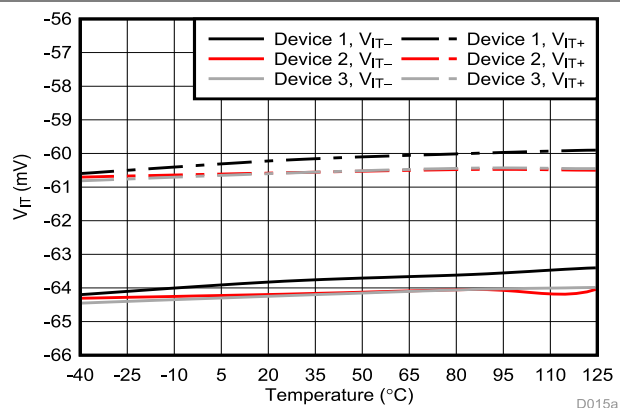


Figure 5-13. Cmp3 Trip Threshold vs Temperature

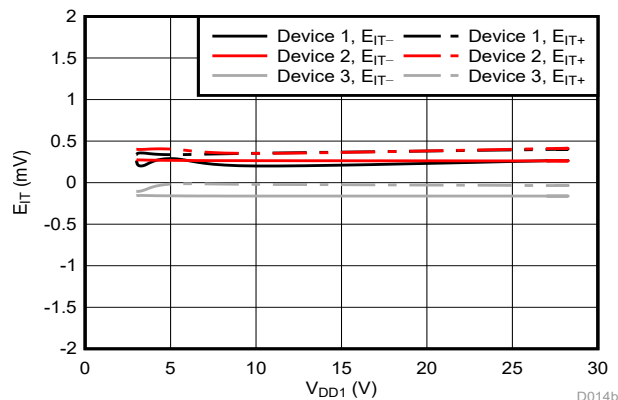


Figure 5-14. Cmp3 Trip Threshold Error vs Supply Voltage

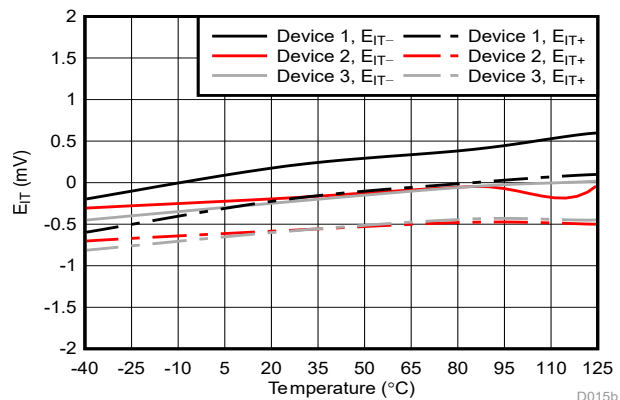


Figure 5-15. Cmp3 Trip Threshold Error vs Temperature

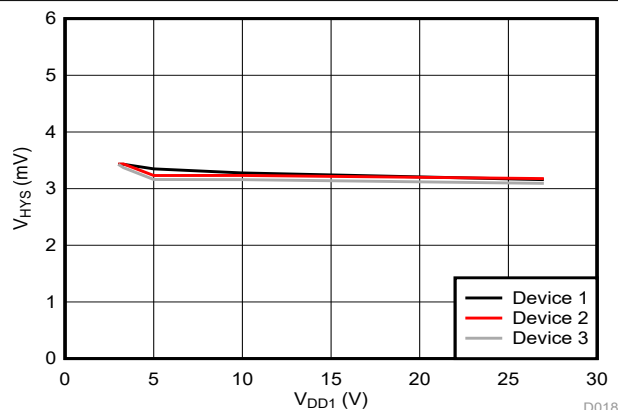


Figure 5-16. Cmp3 Trip Threshold Hysteresis vs Supply Voltage

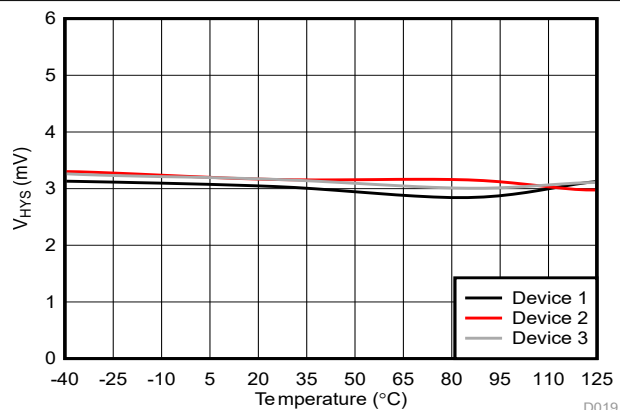


Figure 5-17. Cmp3 Trip Threshold Hysteresis vs Temperature

## 5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

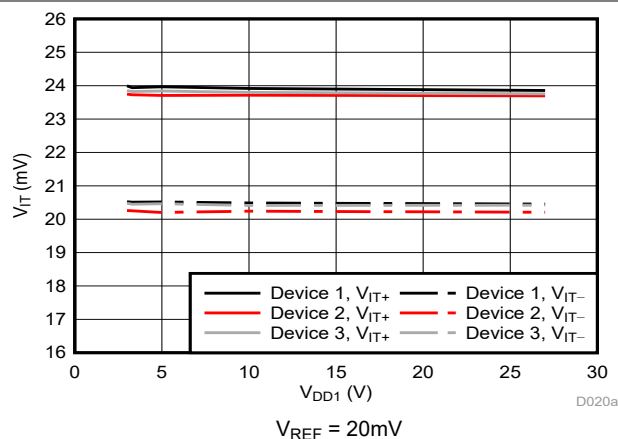


Figure 5-18. Cmp0 Trip Threshold vs Supply Voltage

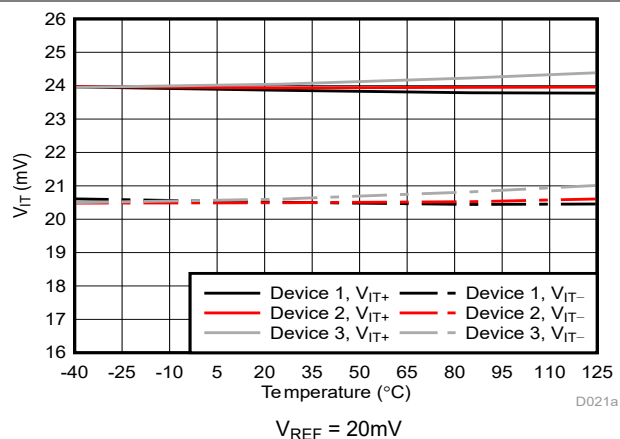


Figure 5-19. Cmp0 Trip Threshold vs Temperature

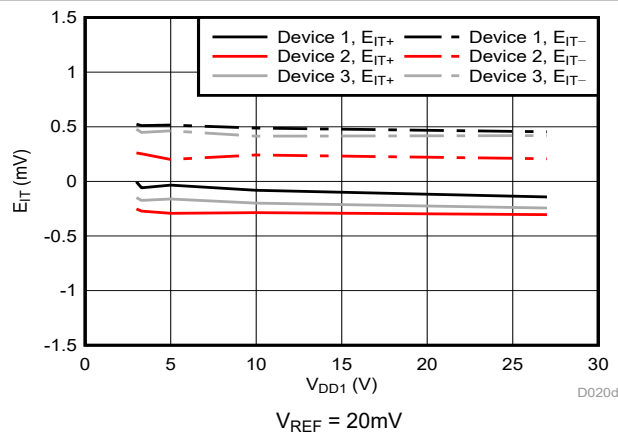


Figure 5-20. Cmp0 Trip Threshold Error vs Supply Voltage

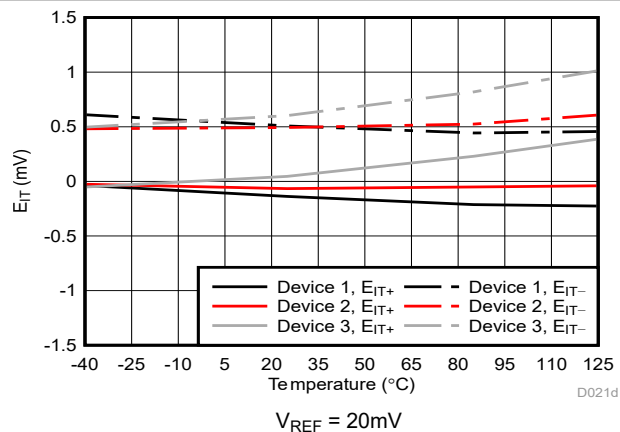


Figure 5-21. Cmp0 Trip Threshold Error vs Temperature

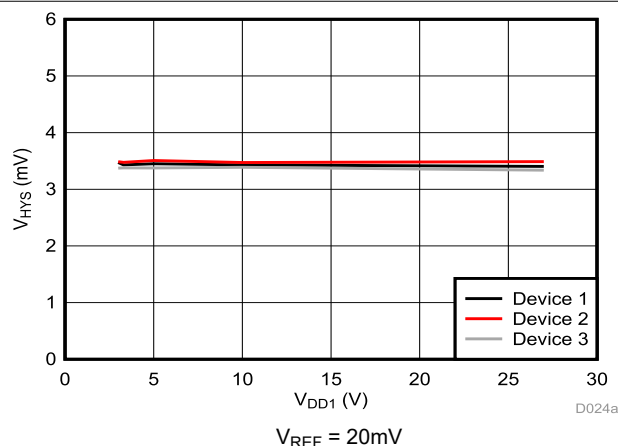


Figure 5-22. Cmp0 Trip Threshold Hysteresis vs Supply Voltage

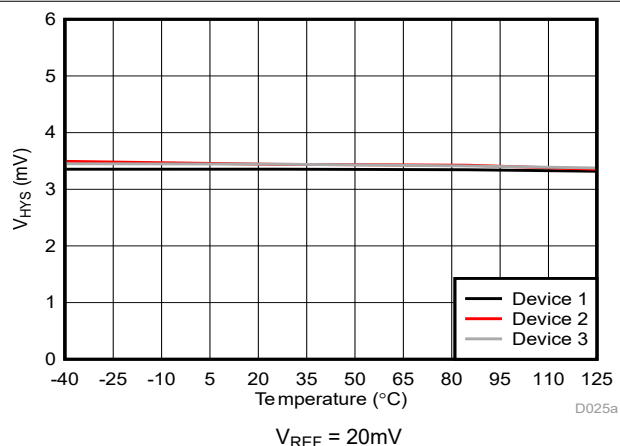


Figure 5-23. Cmp0 Trip Threshold Hysteresis vs Temperature

## 5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

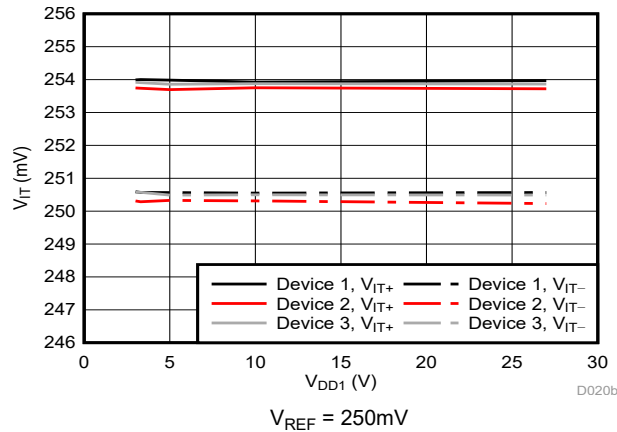


Figure 5-24. Cmp0 Trip Threshold vs Supply Voltage

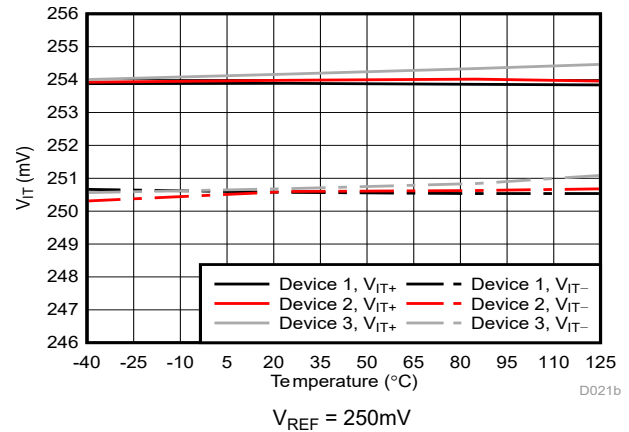


Figure 5-25. Cmp0 Trip Threshold vs Temperature

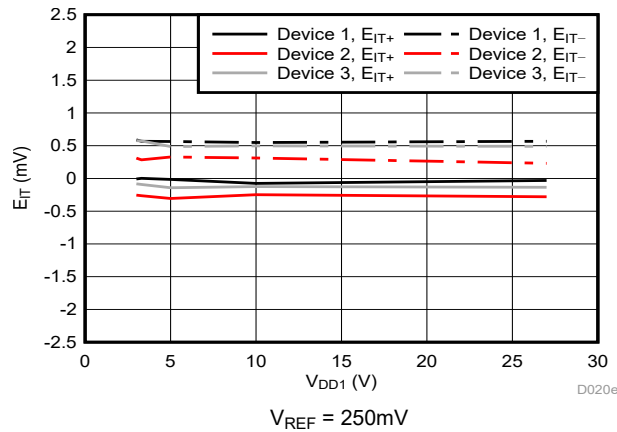


Figure 5-26. Cmp0 Trip Threshold Error vs Supply Voltage

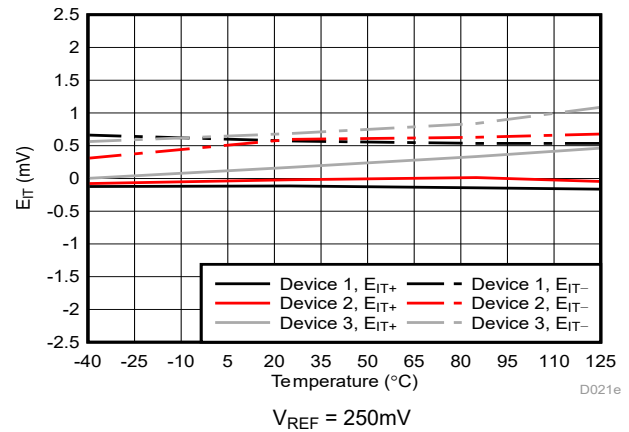


Figure 5-27. Cmp0 Trip Threshold Error vs Temperature

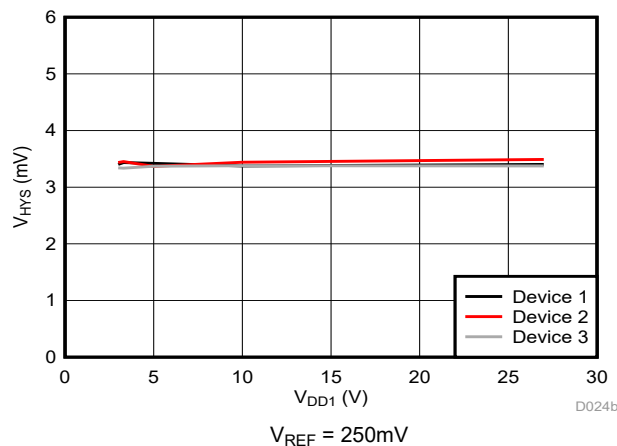


Figure 5-28. Cmp0 Trip Threshold Hysteresis vs Supply Voltage

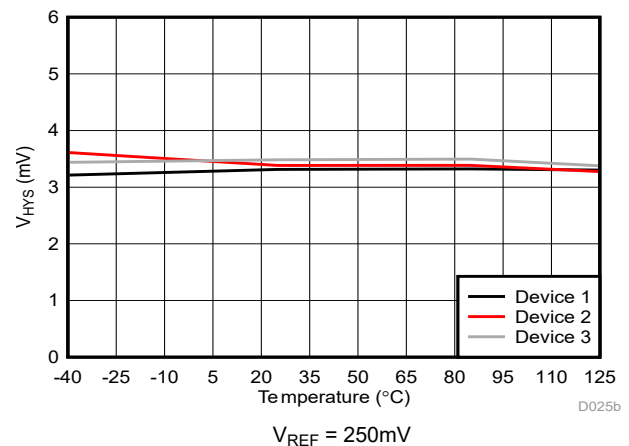


Figure 5-29. Cmp0 Trip Threshold Hysteresis vs Temperature

## 5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

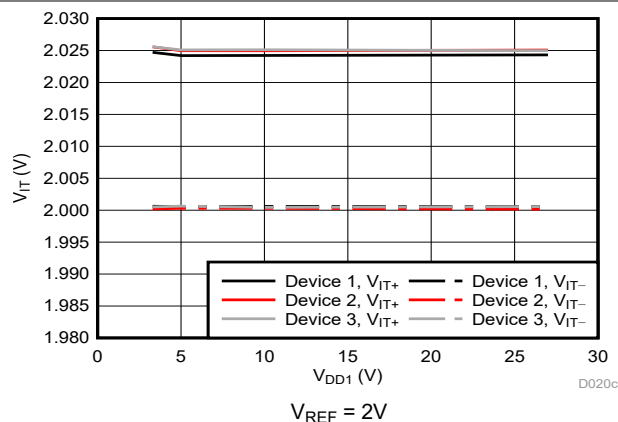


Figure 5-30. Cmp0 Trip Threshold vs Supply Voltage

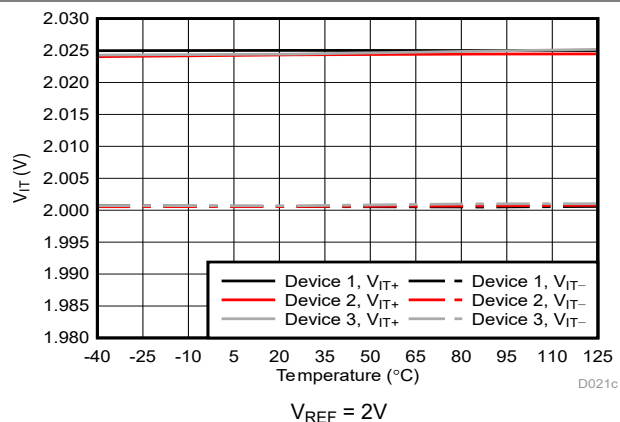


Figure 5-31. Cmp0 Trip Threshold vs Temperature

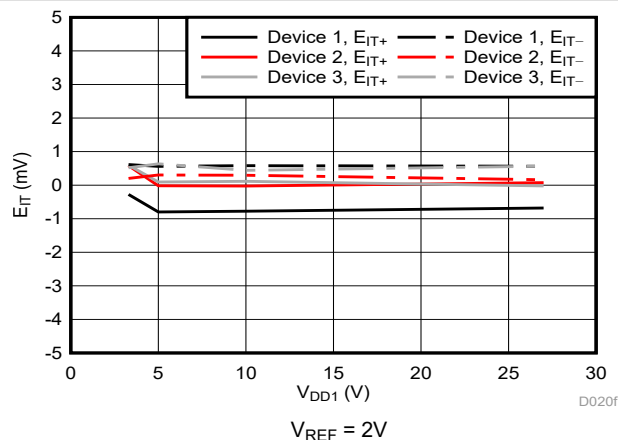


Figure 5-32. Cmp0 Trip Threshold Error vs Supply Voltage

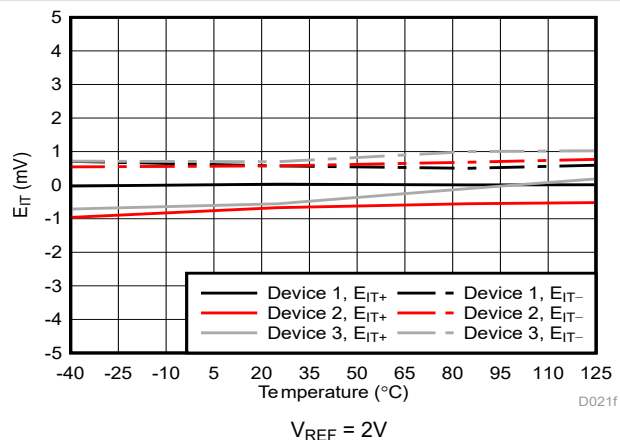


Figure 5-33. Cmp0 Trip Threshold Error vs Temperature

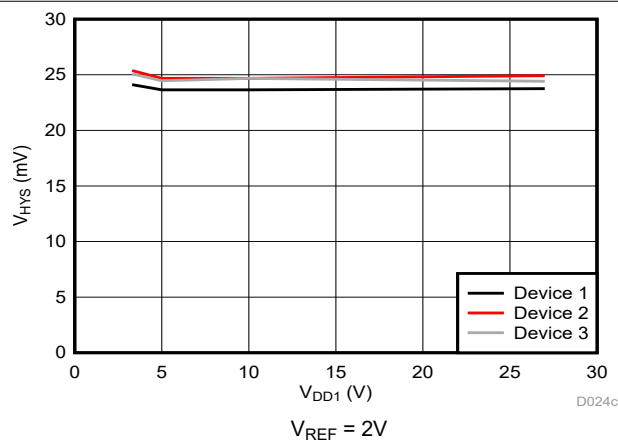


Figure 5-34. Cmp0 Trip Threshold Hysteresis vs Supply Voltage

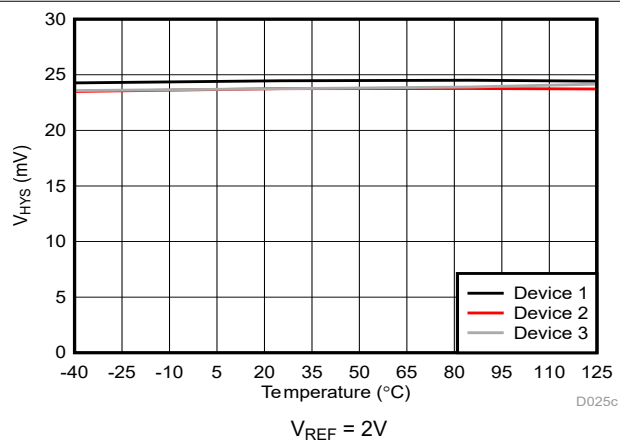


Figure 5-35. Cmp0 Trip Threshold Hysteresis vs Temperature



## 5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

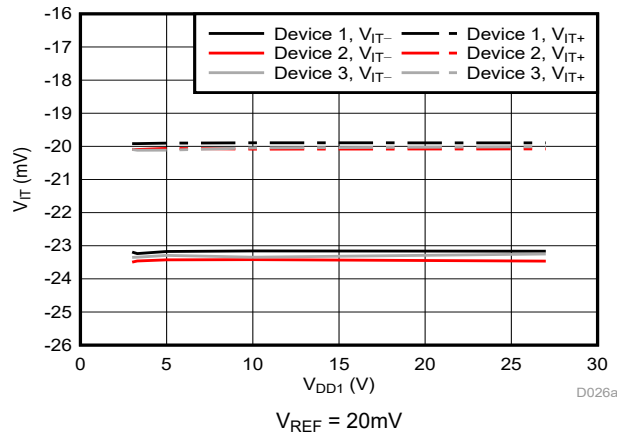


Figure 5-36. Cmp1 Trip Threshold vs Supply Voltage

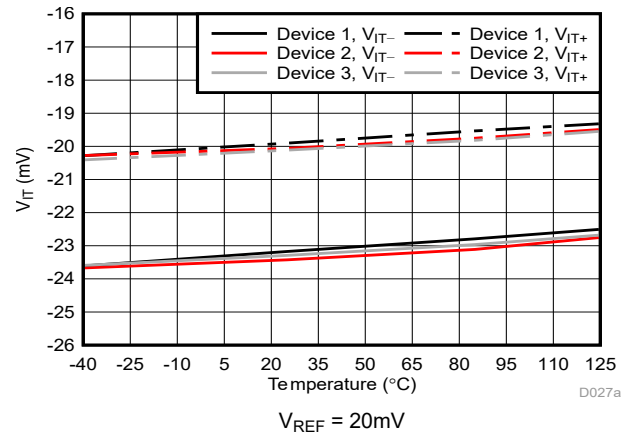


Figure 5-37. Cmp1 Trip Threshold vs Temperature

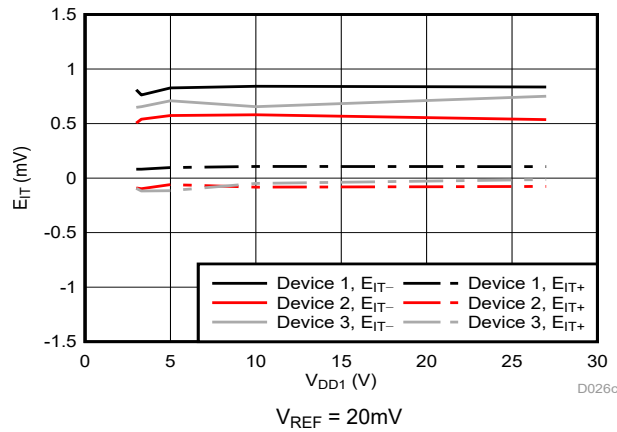


Figure 5-38. Cmp1 Trip Threshold Error vs Supply Voltage

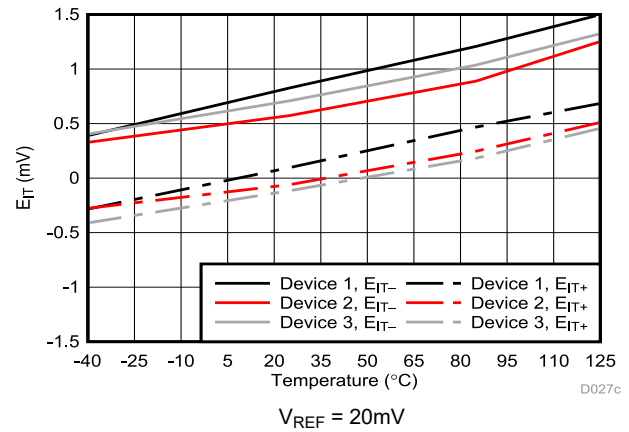


Figure 5-39. Cmp1 Trip Threshold Error vs Temperature

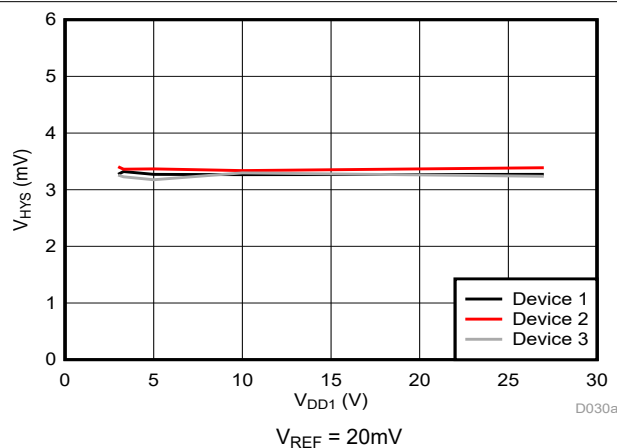


Figure 5-40. Cmp1 Trip Threshold Hysteresis vs Supply Voltage

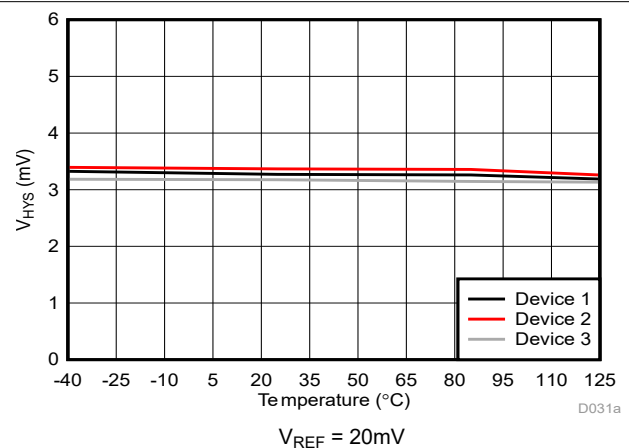


Figure 5-41. Cmp1 Trip Threshold Hysteresis vs Temperature

## 5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

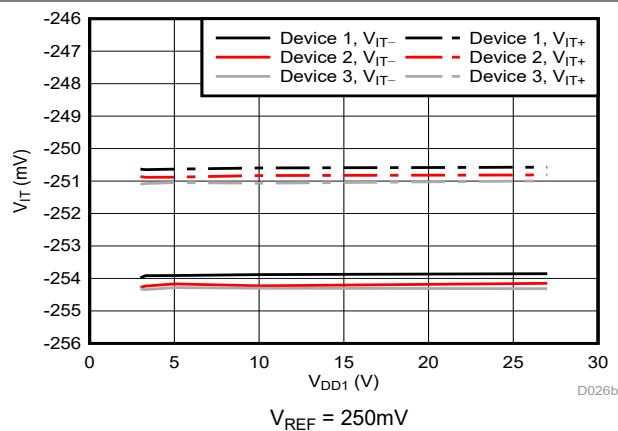


Figure 5-42. Cmp1 Trip Threshold vs Supply Voltage

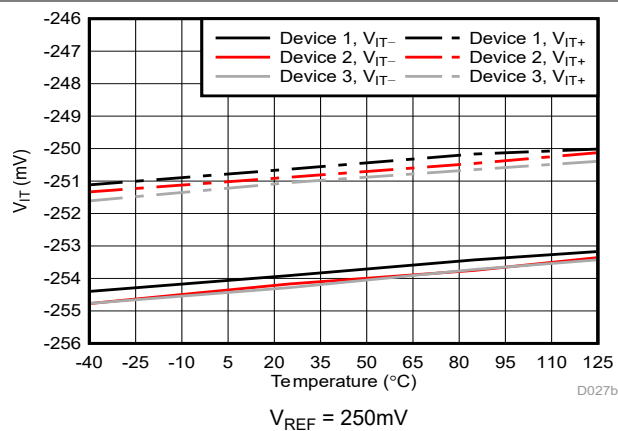


Figure 5-43. Cmp1 Trip Threshold vs Temperature

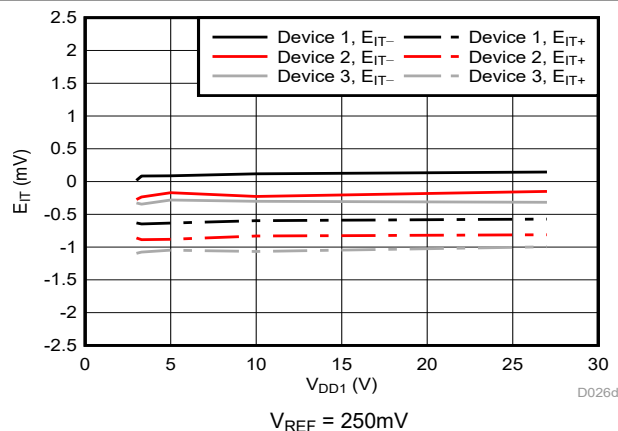


Figure 5-44. Cmp1 Trip Threshold Error vs Supply Voltage

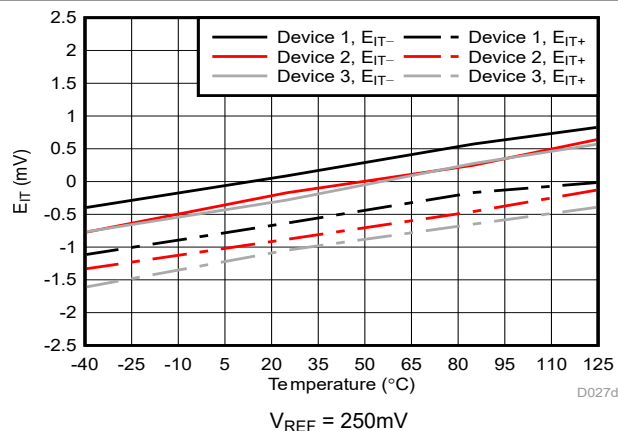


Figure 5-45. Cmp1 Trip Threshold Error vs Temperature

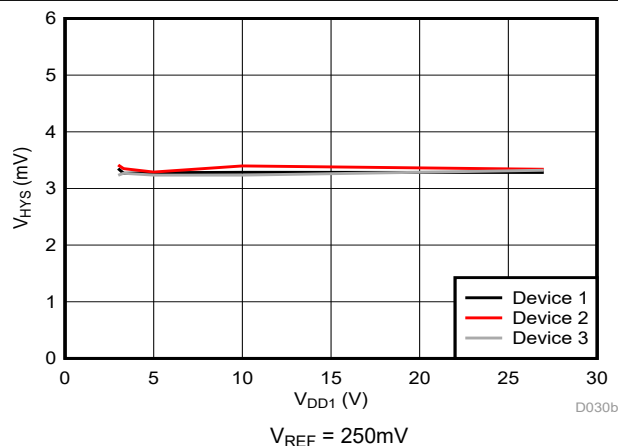


Figure 5-46. Cmp1 Trip Threshold Hysteresis vs Supply Voltage

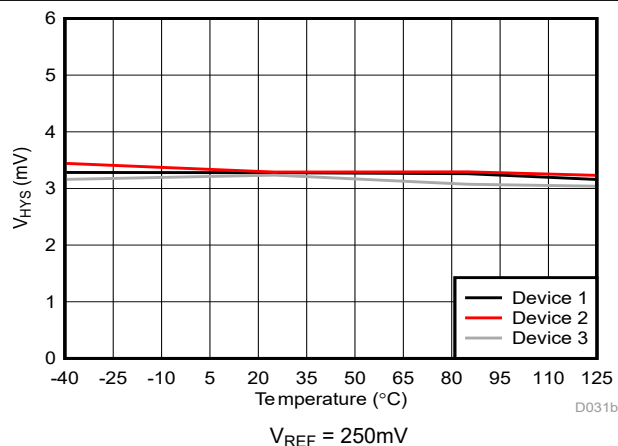


Figure 5-47. Cmp1 Trip Threshold Hysteresis vs Temperature

## 5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

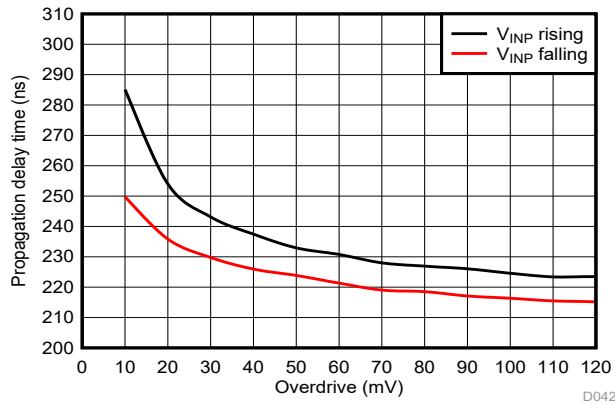


Figure 5-48. Cmp2 Propagation Delay vs Overdrive

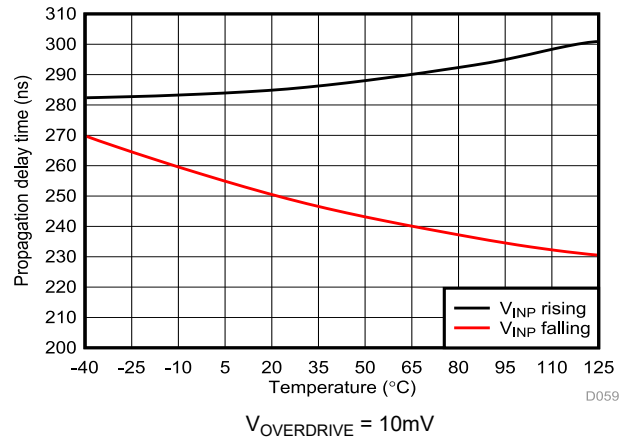


Figure 5-49. Cmp2 Propagation Delay vs Temperature

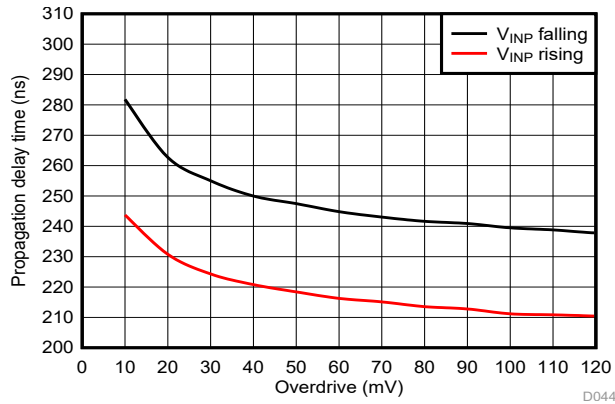


Figure 5-50. Cmp3 Propagation Delay vs Overdrive

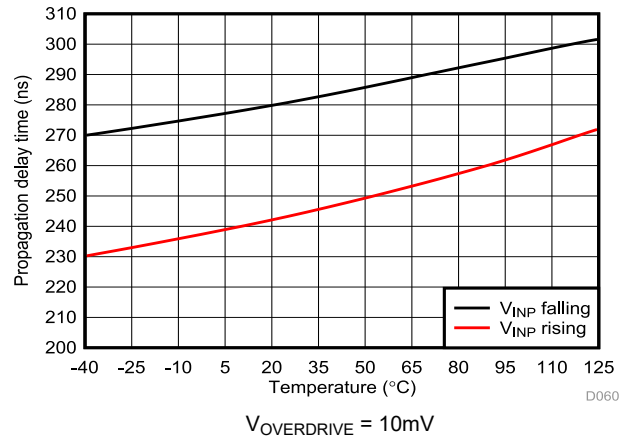


Figure 5-51. Cmp3 Propagation Delay vs Temperature

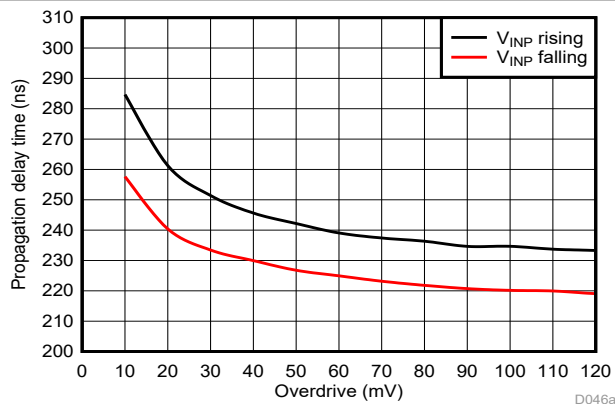


Figure 5-52. Cmp0 Propagation Delay vs Overdrive

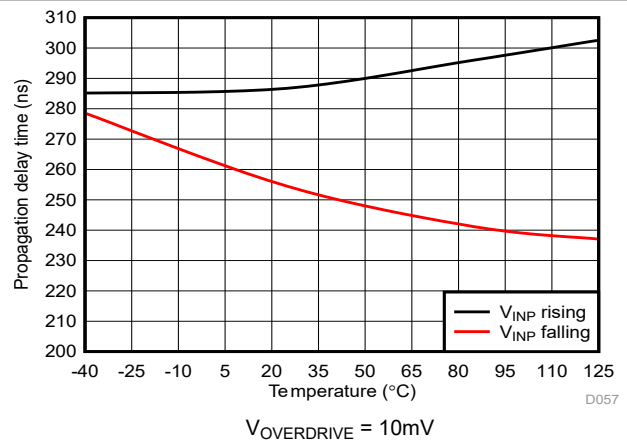


Figure 5-53. Cmp0 Propagation Delay vs Temperature

## 5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

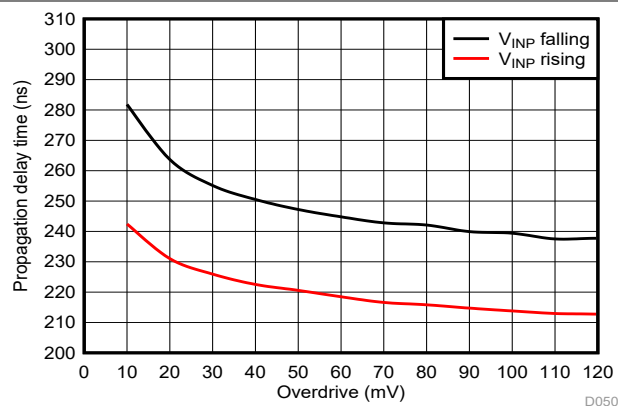


Figure 5-54. Cmp1 Propagation Delay vs Overdrive

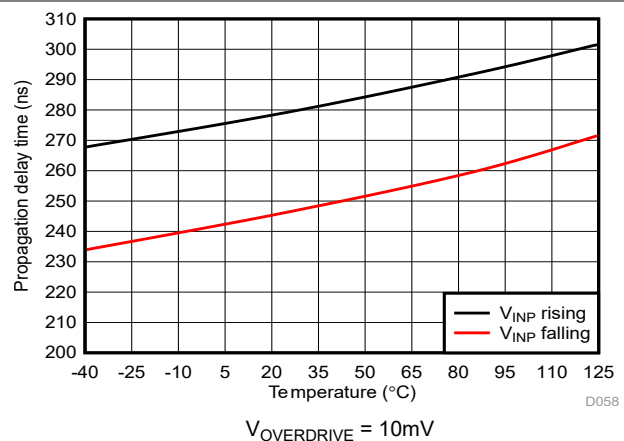


Figure 5-55. Cmp1 Propagation Delay vs Temperature

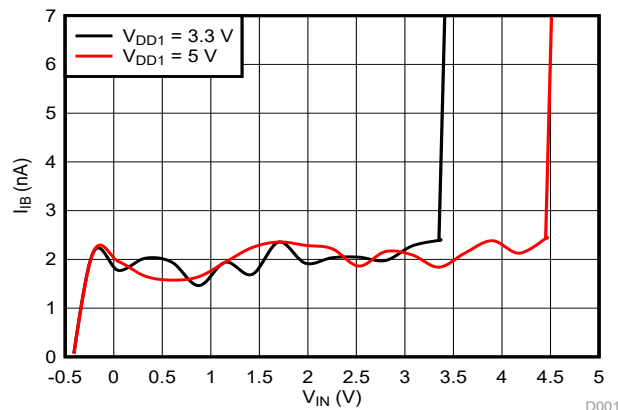


Figure 5-56. Input Bias Current vs Input Voltage

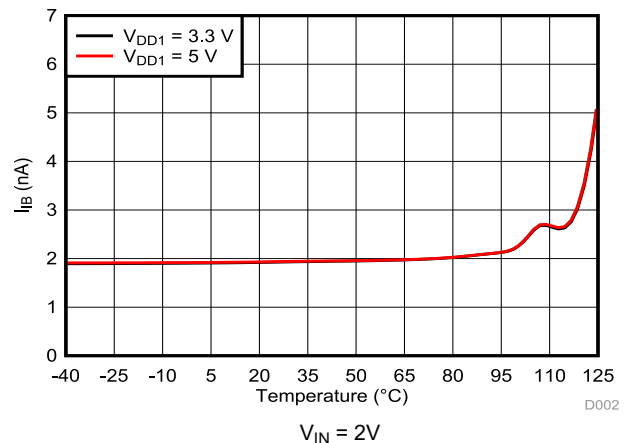


Figure 5-57. Input Bias Current vs Temperature

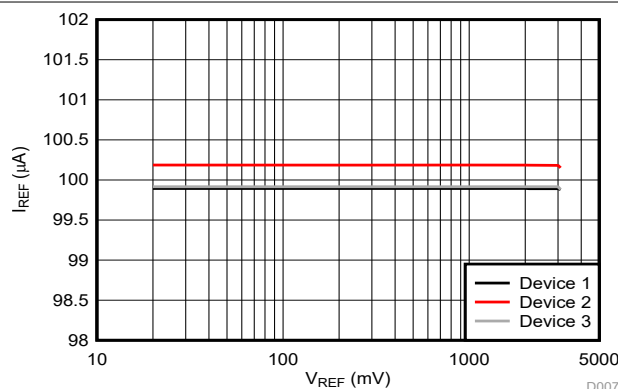


Figure 5-58. Reference Current vs Reference Voltage

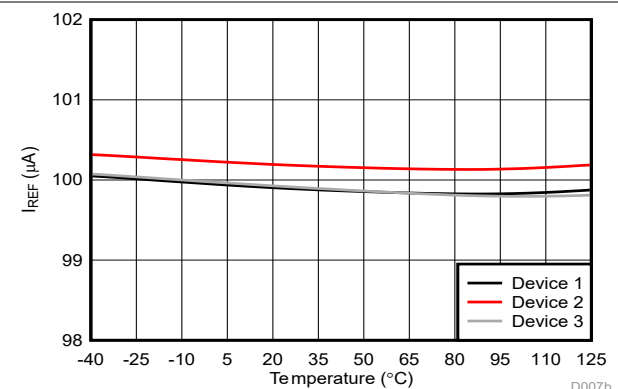


Figure 5-59. Reference Current vs Temperature

## 5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

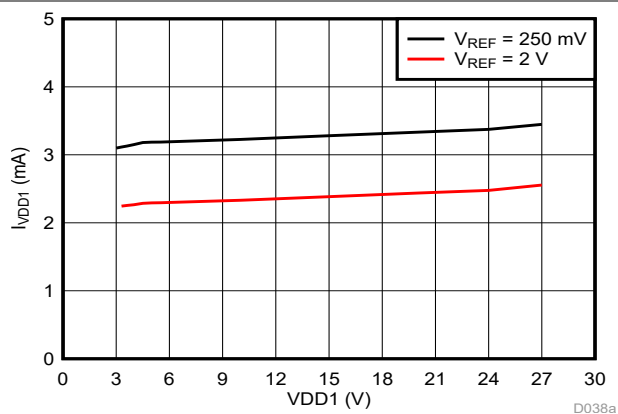


Figure 5-60. High-Side Supply Current vs Supply Voltage

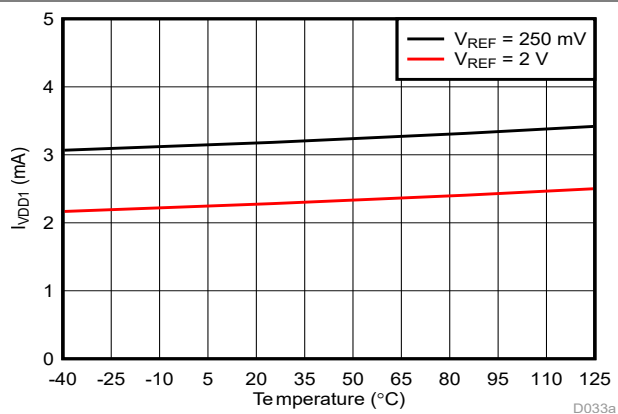


Figure 5-61. High-Side Supply Current vs Temperature

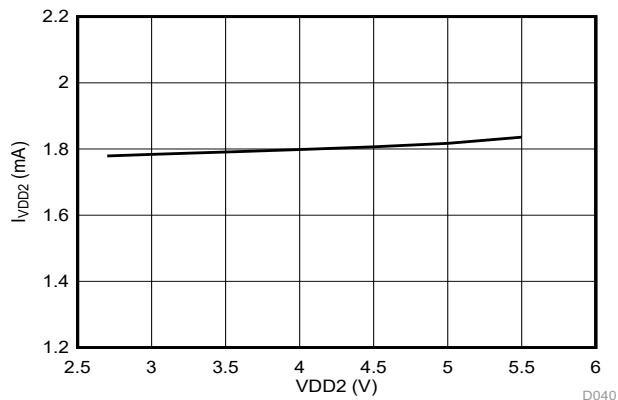


Figure 5-62. Low-Side Supply Current vs Supply Voltage

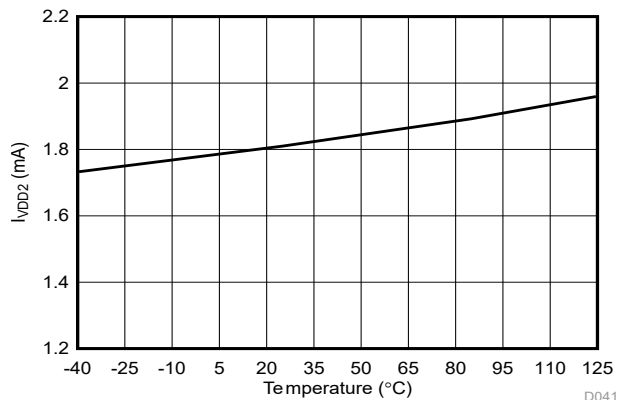


Figure 5-63. Low-Side Supply Current vs Temperature

## 6 Detailed Description

### 6.1 Overview

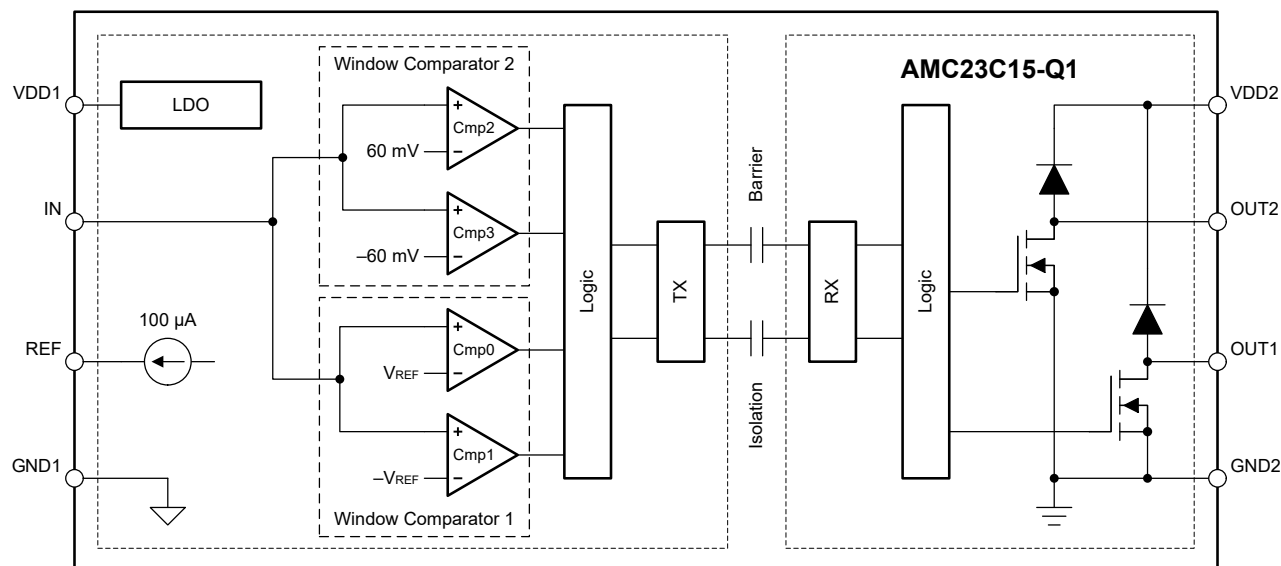
The AMC23C15-Q1 is a dual, isolated window comparator with open-drain outputs. Window comparator 1 is comprised of comparator Cmp0 and Cmp1 and window comparator 2 is comprised of Cmp2 and Cmp3. Cmp0 and Cmp2 compare the input voltage ( $V_{IN}$ ) against the respective positive thresholds ( $V_{IT+}$ ) and Cmp1 and Cmp3 compare the input voltage ( $V_{IN}$ ) against the respective negative thresholds ( $V_{IT-}$ ). The respective  $V_{IT+}$  and  $V_{IT-}$  thresholds are of equal magnitude but opposite signs, therefore both window comparators have windows that are centered around 0V. Window comparator 2 has fixed thresholds of  $\pm 60\text{mV}$ . Window comparator 1 has adjustable thresholds from  $\pm 5\text{mV}$  to  $\pm 300\text{mV}$  through an internally generated  $100\mu\text{A}$  reference current and a single external resistor.

The open-drain outputs are actively pulled low when the input voltage ( $V_{IN}$ ) is outside the respective comparison window, but are otherwise in a high-impedance state.

When the voltage on the REF pin is greater than  $V_{MSEL}$ , the device operates in positive-comparator mode. This mode is particularly useful for monitoring positive voltage supplies. Both negative comparators (Cmp1 and Cmp3) are disabled and only the positive comparators (Cmp0 and Cmp2) are functional. The reference voltage in this mode can be as high as 2.7V.

Galvanic isolation between the high- and low-voltage side of the device is achieved by transmitting the comparator states across a  $\text{SiO}_2$ -based, reinforced capacitive isolation barrier. This isolation barrier supports a high level of magnetic field immunity, as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application note](#). The digital modulation scheme used in the AMC23C15-Q1 to transmit data across the isolation barrier, and the isolation barrier characteristics, result in high reliability and common-mode transient immunity.

### 6.2 Functional Block Diagram



## 6.3 Feature Description

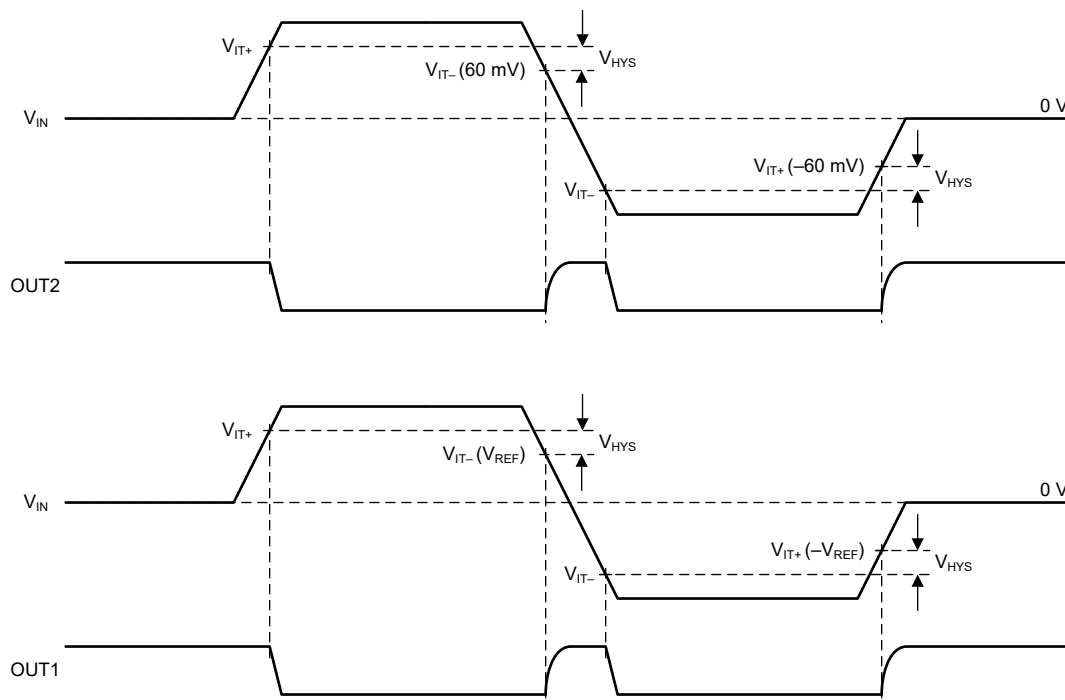
### 6.3.1 Analog Input

The AMC23C15-Q1 has a single input that drives both window comparators. Window comparator 1 has an adjustable threshold and window comparator 2 has a fixed threshold.

The positive comparators trip when the input voltage ( $V_{IN}$ ) rises above the respective  $V_{IT+}$  threshold that is defined as the reference value plus the internal hysteresis voltage (for example, 64mV for the fixed-threshold comparator). The positive comparators release when  $V_{IN}$  drops below the respective  $V_{IT-}$  threshold that equals the reference value (for example, 60mV for the fixed-threshold comparator). The negative comparators trip when  $V_{IN}$  drops below the respective  $V_{IT-}$  threshold that is defined as the negative reference value minus the internal hysteresis voltage (for example, -64mV for the fixed-threshold comparator). The negative comparators release when  $V_{IN}$  rises above the respective  $V_{IT+}$  threshold that equals the negative reference value (for example -60mV for the fixed-threshold comparator).

The difference between  $V_{IT+}$  and  $V_{IT-}$  is referred to as the *comparator hysteresis* and is 4mV for reference voltages below 450mV. The integrated hysteresis makes the AMC23C15-Q1 less sensitive to input noise and provides stable operation in noisy environments without having to add external positive feedback to create hysteresis. The hysteresis of Cmp0 increases to 25mV for reference values ( $V_{REF}$ ) greater than 600mV. See the [Reference Input](#) description for more details.

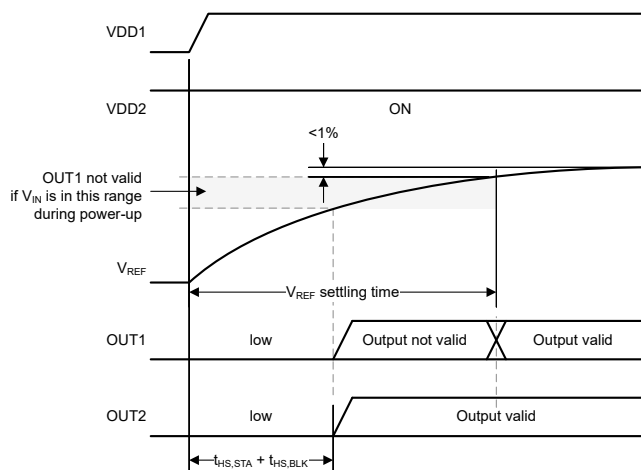
Figure 6-1 shows a timing diagram of the relationship between hysteresis and switching thresholds.



**Figure 6-1. Switching Thresholds and Hysteresis**

### 6.3.2 Reference Input

The voltage on the REF pin determines the trip threshold of window comparator 1. The internal precision current source forces a 100 $\mu$ A current through an external resistor connected from the REF pin to GND1. The resulting voltage across the resistor ( $V_{REF}$ ) equals the magnitude of the positive and negative trip thresholds, see [Figure 6-1](#). Place a 100nF capacitor parallel to the resistor to filter the reference voltage. This capacitor must be charged by the 100 $\mu$ A current source during power-up and the charging time can exceed the high-side blanking time ( $t_{HS,BLK}$ ). In this case, as shown in [Figure 6-2](#), window comparator 1 can output an incorrect state after the high-side blanking time has expired until  $V_{REF}$  reaches the final value. See the [Power-Up and Power-Down Behavior](#) section for more details on power-up behavior.

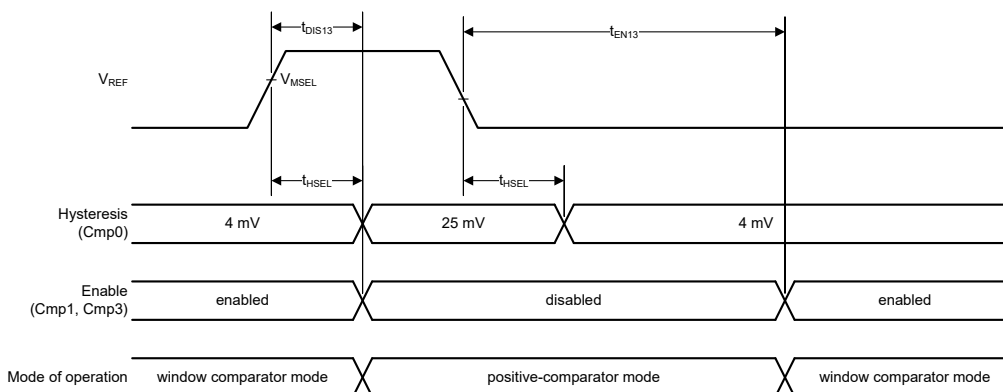


**Figure 6-2. Output Behavior for Long Settling Times of the Reference Voltage**

The voltage on the REF pin also determines the functionality of the negative comparators (Cmp1, Cmp3) and the hysteresis of the positive comparator (Cmp0) shown in the [Functional Block Diagram](#). If  $V_{REF}$  exceeds the  $V_{MSEL}$  threshold defined in the [Electrical Characteristics](#) table, both negative comparators (Cmp1 and Cmp3) are disabled and the hysteresis of Cmp0 is increased from 4mV (typical) to 25mV. Positive-comparator mode is intended for voltage-monitoring applications that require higher input voltages and higher noise immunity.

The reference pin can be driven by an external voltage source to change the comparator thresholds during operation. However, do not drive  $V_{REF}$  dynamically across the  $V_{MSEL}$  threshold during normal operation because doing so changes the hysteresis of the Cmp0 comparator and can lead to unintentional switching of the OUT1 output.

[Figure 6-3](#) shows a mode selection timing diagram.



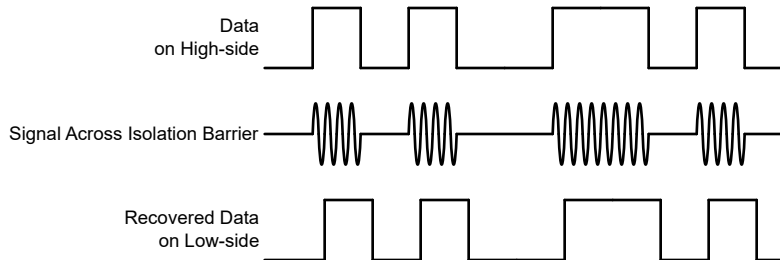
**Figure 6-3. Mode Selection**



### 6.3.3 Isolation Channel Signal Transmission

The AMC23C15-Q1 uses an on-off keying (OOK) modulation scheme, as shown in Figure 6-4, to transmit the comparator output states across the SiO<sub>2</sub>-based isolation barrier. The transmit driver (TX) shown in the [Functional Block Diagram](#) transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the data for the logic that drives the open-drain output buffers. The AMC23C15-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.



**Figure 6-4. OOK-Based Modulation Scheme**

### 6.3.4 Open-Drain Digital Outputs

The AMC23C15-Q1 has two open-drain outputs, one for each window comparator. As illustrated in Figure 6-1, OUT1 is actively pulled low when  $|V_{IN}|$  exceeds the threshold values defined by the voltage on the REF pin. OUT2 is actively pulled low when  $|V_{IN}|$  exceeds the threshold values defined by the internal 60mV reference.

The open-drain outputs are diode-connected to the VDD2 supply, see the [Functional Block Diagram](#), which means the outputs cannot be pulled more than 500mV above the VDD2 supply before significant current begins to flow into the OUTx pins. In particular, the open-drain outputs are clamped to one diode voltage above ground if VDD2 is at the GND2 level. This behavior is indicated by the gray shadings in Figure 6-5 through Figure 6-10.

On a system level, the CMTI performance of an open-drain signal line depends on the value of the pullup resistor. During a common-mode transient event with a high slew rate (high dV/dt), the open-drain signal line can be pulled low because of parasitic capacitive coupling between the high side and the low side of the printed circuit board (PCB). The effect of the parasitic coupling on the signal level is a function of the pullup strength and a lower value pullup resistor results in better CMTI performance. The AMC23C15-Q1 is characterized by a relatively weak pullup resistor value of 10kΩ to make sure that the specified CMTI performance is met in a typical application with a 4.7kΩ or lower pullup resistor.

### 6.3.5 Power-Up and Power-Down Behavior

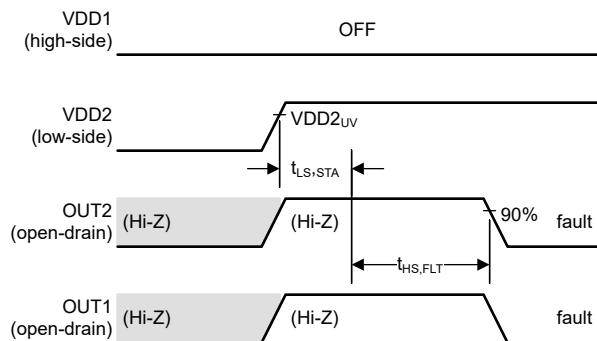
Both open-drain outputs power up in a high-impedance (Hi-Z) state when the low-side supply (VDD2) turns on. After power-up, if the high-side is not functional yet, both outputs are actively pulled low. As shown in [Figure 6-5](#), this condition happens after the low-side start-up time plus the high-side fault detection delay time ( $t_{LS,STA} + t_{HS,FLT}$ ). Similarly, if the high-side supply drops below the undervoltage threshold (VDD1<sub>UV</sub>), as described in [Figure 6-8](#), for more than the high-side fault detection delay time during normal operation, both outputs are pulled low. This delay allows the system to shut down reliably when the high-side supply is missing.

Communication start between the high-side and low-side of the comparator is delayed by the high-side blanking time ( $t_{HS,BLK}$ , a time constant implemented on the high-voltage side) to allow the internal 60-mV reference and the voltage on the REF pin to settle and to avoid unintentional switching of the comparator outputs during power-up.

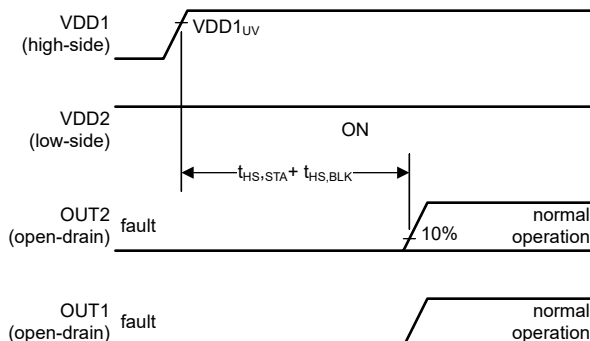
[Figure 6-5](#) through [Figure 6-10](#) depict typical power-up and power-down scenarios.

In [Figure 6-5](#), the low-side supply (VDD2) turns on but the high-side supply (VDD1) remains off. Both outputs power up in the default Hi-Z state. After  $t_{HS,FLT}$ , both outputs are pulled low indicating a no-power fault on the high side.

In [Figure 6-6](#), the high-side supply (VDD1) turns on long after the low-side supply (VDD2) turns on. Both outputs are initially in an active-low state, see [Figure 6-5](#). After the high-side supply is enabled, there is a duration of  $t_{HS,STA} + t_{HS,BLK}$  before the device assumes normal operation and both outputs reflect the current state of the window comparators.



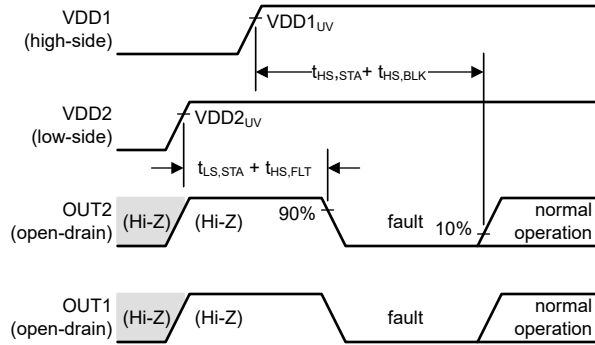
**Figure 6-5. VDD2 Turns On, VDD1 Stays Off**



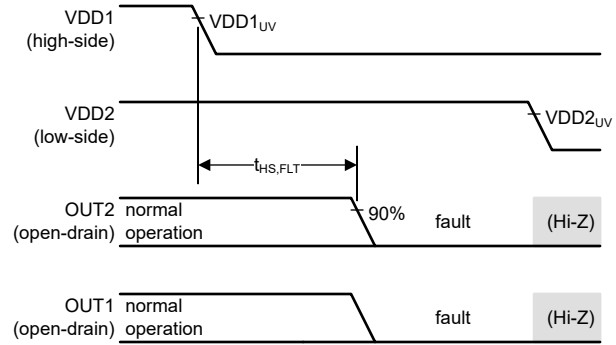
**Figure 6-6. VDD2 is On; VDD1 Turns On (Long Delay)**

In [Figure 6-7](#), the low-side supply (VDD2) turns on, followed by the high-side supply (VDD1) with only a short delay. Both outputs are initially in a Hi-Z state. The high-side fault detection delay ( $t_{HS,FLT}$ ) is shorter than the high-side blanking time ( $t_{HS,BLK}$ ), and therefore both outputs are pulled low after  $t_{HS,FLT}$ , indicating that the high-side is not operational yet. After the high-side blanking time ( $t_{HS,BLK}$ ) elapses, the device assumes normal operation and both outputs reflect the current state of the window comparators.

In [Figure 6-8](#), the high-side supply (VDD1) turns off, followed by the low-side supply (VDD2). After the high-side fault detection delay time ( $t_{HS,FLT}$ ), both outputs are actively pulled low. As soon as VDD2 drops below the VDD2<sub>UV</sub> threshold, both outputs enter a Hi-Z state.



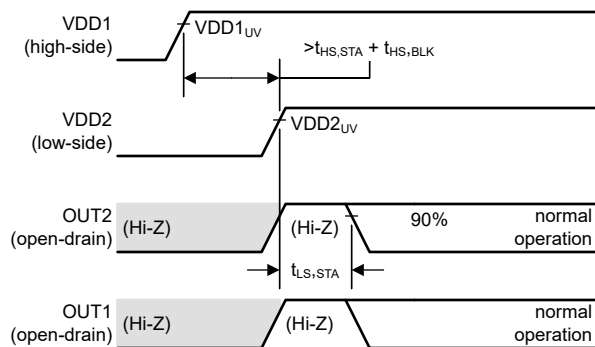
**Figure 6-7. VDD2 Turns On, Followed by VDD1 (Short Delay)**



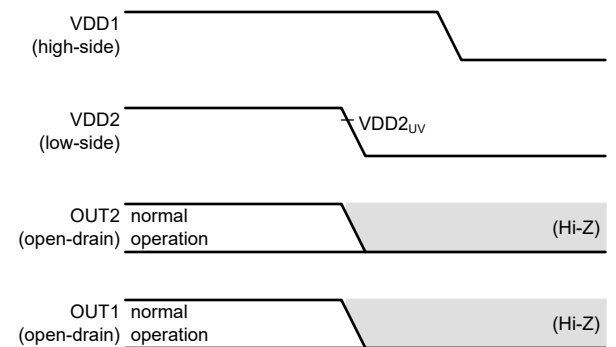
**Figure 6-8. VDD1 Turns Off, Followed by VDD2**

In [Figure 6-9](#), the low-side supply (VDD2) turns on after the high-side is fully powered up (the delay between VDD1 and VDD2 is greater than  $(t_{HS,STA} + t_{HS,BLK})$ ). Both outputs start in a Hi-Z state. After the low-side start-up time ( $t_{LS,STA}$ ), the device enters normal operation.

In [Figure 6-10](#), the low-side supply (VDD2) turns off, followed by the high-side supply (VDD1). As soon as VDD2 drops below the  $VDD2_{UV}$  threshold, both outputs enter a Hi-Z state.



**Figure 6-9. VDD1 Turns On, Followed by VDD2 (Long Delay)**



**Figure 6-10. VDD2 Turns Off, Followed by VDD1**

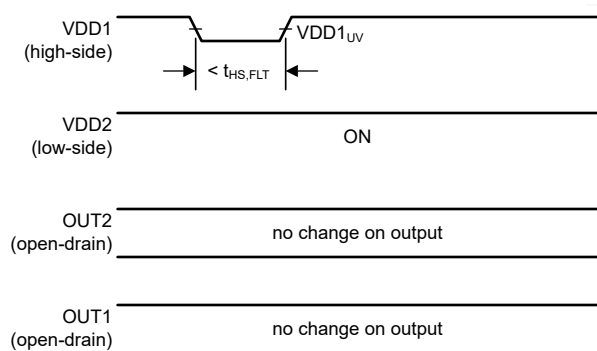
### 6.3.6 VDD1 Brownout and Power-Loss Behavior

Brownout is a condition where the VDD1 supply drops below the specified operating voltage range but the device remains functional. Power loss is a condition where the VDD1 supply drops below a level where the device stops being functional. Depending on the duration and the voltage level, a brownout condition can or can not be noticeable at the output of the device. A power-loss condition is always signaled on the output of the isolated comparator.

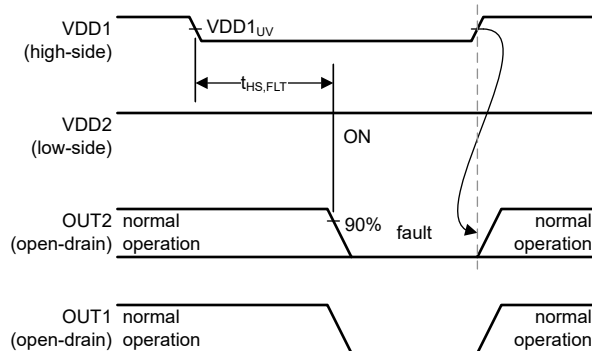
Figure 6-11 through Figure 6-13 show typical brownout and power-loss scenarios.

In Figure 6-11, VDD1 droops below the undervoltage detection threshold ( $VDD1_{UV}$ ) but recovers before the high-side-fault detection delay time ( $t_{HS,FLT}$ ) expires. The brownout event has no effect on the comparator outputs.

In Figure 6-12, VDD1 droops below the undervoltage detection threshold ( $VDD1_{UV}$ ) for more than the high-side-fault detection delay time ( $t_{HS,FLT}$ ). The brownout condition is detected as a fault and both outputs are pulled low after a delay equal to  $t_{HS,FLT}$ . The device resumes normal operation as soon as VDD1 recovers above the  $VDD1_{UV}$  threshold.

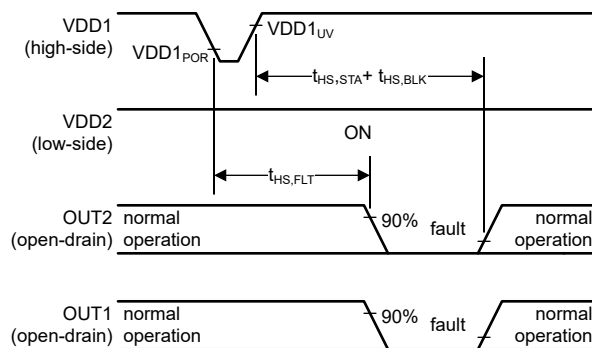


**Figure 6-11. Output Response to a Short Brownout Event on VDD1**



**Figure 6-12. Output Response to a Long Brownout Event on VDD1**

In Figure 6-13, VDD1 droops below the power-on-reset (POR) threshold ( $VDD1_{POR}$ ). The power-loss condition is detected as a fault and both outputs are pulled low after a delay equal to  $t_{HS,FLT}$ . The device resumes normal operation after a delay equal to  $t_{HS,STA} + t_{HS,BLK}$  after VDD1 recovers above the  $VDD1_{UV}$  threshold.



**Figure 6-13. Output Response to a Power-Loss Event on VDD1**

## 6.4 Device Functional Modes

The AMC23C15-Q1 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the [Recommended Operating Conditions](#) table.

The four comparators on the high-side (Cmp0 to Cmp3) function as two independent window comparators when the voltage on the REF pin is below the  $V_{MSEL}$  threshold. If the voltage on the REF pin exceeds the  $V_{MSEL}$  threshold, the negative comparators (Cmp1 and Cmp3) are disabled, and Cmp0 and Cmp2 function as two independent positive comparators, as described in the [Reference Input](#) section.

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

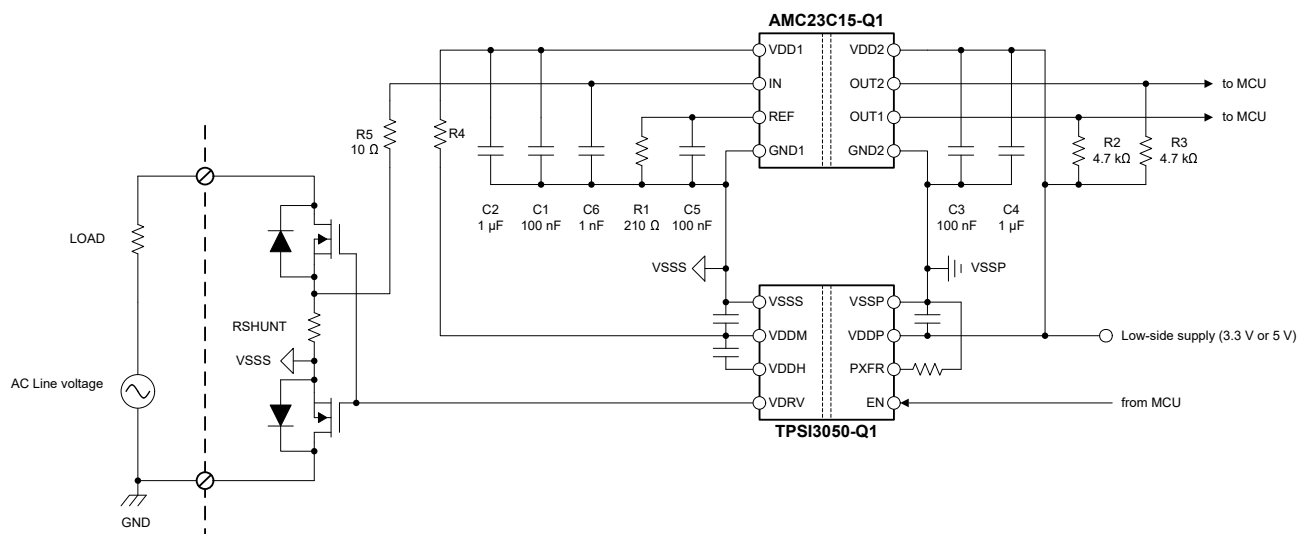
### 7.1 Application Information

With low response time, high common-mode transient immunity (CMTI), and a reinforced isolation barrier, the AMC23C15-Q1 is designed to provide fast and reliable overcurrent and overvoltage detection for high-voltage applications in harsh and noisy environments.

### 7.2 Typical Application

#### 7.2.1 Overcurrent and Short-Circuit Current Detection

Fast overcurrent and short-circuit current detection is a common requirement in circuit breakers and solid state relays (SSR), and can be implemented with a single AMC23C15-Q1 isolated window comparator as shown in [Figure 7-1](#).



**Figure 7-1. Using the AMC23C15-Q1 for Overcurrent and Short-Circuit Detection**

The load current flowing through a shunt resistor (RSHUNT) connected in series with two back-to-back NMOS power switches of an SSR, and produces a voltage drop that is sensed by the AMC23C15-Q1. This voltage is compared against an adjustable threshold for overcurrent detection and a fixed, 60-mV threshold for short-circuit detection, respectively. The sense voltage can be positive or negative in respect to VSSS, which is the ground reference for the isolated comparator, depending on the direction of current flow. The absolute value of the trip threshold for overcurrent detection is set by the external resistor R1. The trip threshold for short-circuit

detection is fixed by the internal 60-mV reference. Overcurrent conditions are signaled on OUT1, and short-circuit conditions are signaled on OUT2. For a detailed description and a reference design of a SSR, see the [Overcurrent and Overtemperature Protection for Solid-State Relays Reference Design design guide](#) available for download on [www.ti.com](http://www.ti.com).

As depicted in [Figure 7-1](#), the integrated LDO of the AMC23C15-Q1 allows direct connection of the high-side supply input (VDD1) to the VDDM supply that is generated by the isolated switch driver [TPSI3050-Q1](#). No additional isolated power supply or regulator is required to power the high-side of the isolated comparator, which makes the solution very space and cost efficient. The fast response time and high common-mode transient immunity (CMTI) of the AMC23C15-Q1 provide reliable and accurate operation even in high-noise environments.

### 7.2.1.1 Design Requirements

[Table 7-1](#) lists the parameters for the application example in [Figure 7-1](#).

**Table 7-1. Design Requirements**

| PARAMETER                                 | VALUE          |
|---|----------------|
| High-side supply voltage                  | 3 V to 25 V    |
| Low-side supply voltage                   | 2.7 V to 5.5 V |
| Shunt-resistor value                      | 1 mΩ           |
| Overcurrent detection threshold           | ±25 A          |
| Short-circuit current detection threshold | ±60 A          |

### 7.2.1.2 Detailed Design Procedure

The value of the shunt resistor in this example is 1 mΩ, determined by the internal 60-mV reference of the AMC23C15-Q1 and the desired 60-A short-circuit detection threshold.

At the desired 25-A overcurrent detection level, the voltage drop across the shunt resistor is  $1\text{ m}\Omega \times 25\text{ A} = 25\text{ mV}$ . The positive-going trip threshold of window comparator 1 is  $V_{\text{REF}} + V_{\text{HYS}}$ , where  $V_{\text{HYS}}$  is 4 mV as specified in the [Electrical Characteristics](#) table, and  $V_{\text{REF}}$  is the voltage across R1 that is connected between the REF and GND1 pins. R1 is calculated as  $(V_{\text{TRIP}} - V_{\text{HYS}}) / I_{\text{REF}} = (25\text{ mV} - 4\text{ mV}) / 100\text{ }\mu\text{A} = 210\text{ }\Omega$  and matches a value from the E96 series (1% accuracy).

A 10-Ω, 1-nF RC filter (R5, C6) is placed at the input of the comparator to filter the input signal and reduce noise sensitivity. This filter adds  $10\text{ }\Omega \times 1\text{ nF} = 10\text{ ns}$  of propagation delay that must be considered when calculating the overall response time of the protection circuit. Larger filter constants are preferable to increase noise immunity if the system can tolerate the additional delay.

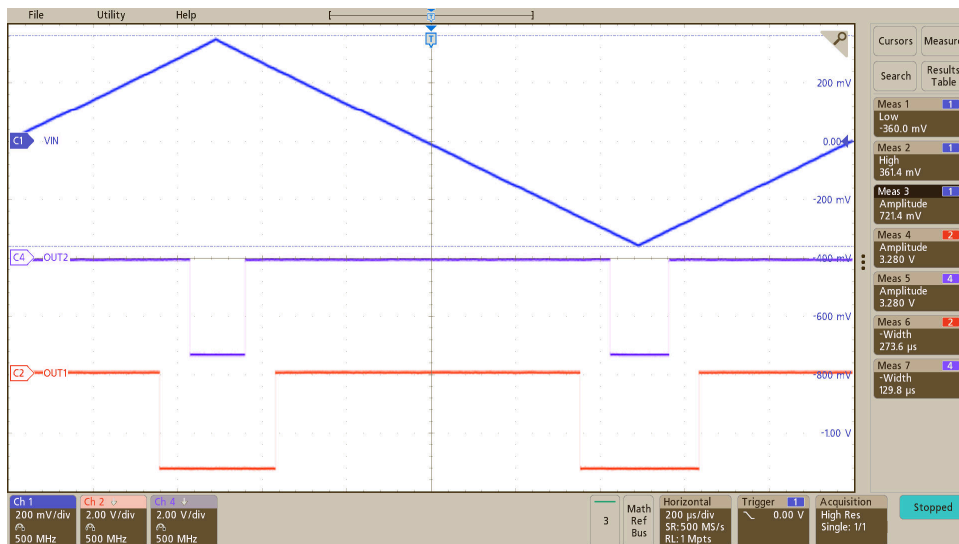
[Table 7-2](#) summarizes the key parameters of the design.

**Table 7-2. Overcurrent and Short-Circuit Detection Design Example**

| PARAMETER   | VALUE          |
|---|----------------|
| Reference resistor value (R1)                           | 210 Ω          |
| Reference capacitor value (C5)                          | 100 nF         |
| Reference voltage                                       | 21 mV          |
| Reference voltage settling time (to 90% of final value) | 50 μs          |
| Overcurrent trip threshold (rising)                     | 25 mV / 25.0 A |
| Overcurrent trip threshold (falling)                    | 21 mV / 21 A   |
| Short-circuit current trip threshold (rising)           | 64 mV / 64 A   |
| Short-circuit current trip threshold (falling)          | 60 mV / 60.0 A |

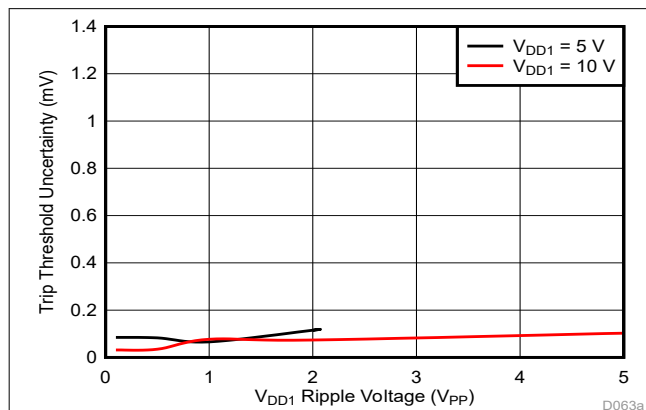
## 7.2.2 Application Curves

Figure 7-2 shows the typical response of the AMC23C15-Q1 to a bipolar, triangular input waveform with an amplitude of 140mV<sub>PP</sub>. OUT1 switches when VIN crosses the ±50mV level determined by the REF pin voltage that is biased to 50mV in this example. OUT2 switches when VIN crosses the ±60mV level determined by the fixed internal reference value.

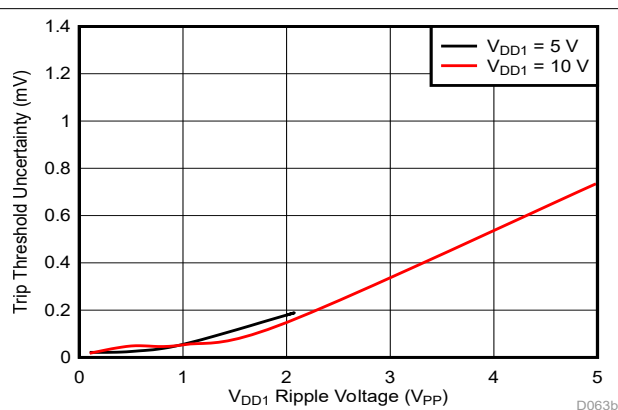


**Figure 7-2. Output Response of the AMC23C15-Q1 to a Triangular Input Waveform**

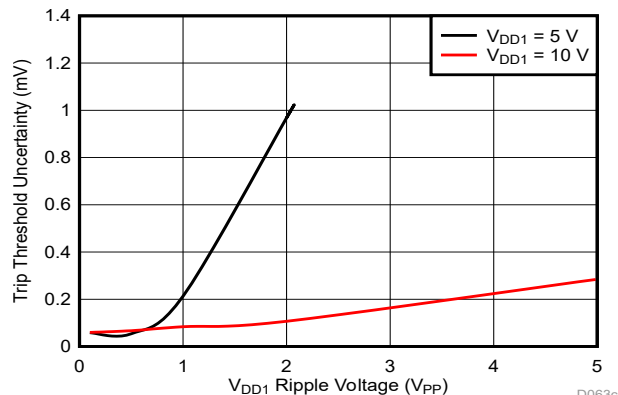
The integrated LDO of the AMC23C15-Q1 greatly relaxes the power-supply requirements on the high-voltage side and allows powering the device from non-regulated transformer, charge pump, and bootstrap supplies. As given by the following images, the internal LDO provides a stable operating voltage to the internal circuitry, allowing the trip thresholds to remain mostly undisturbed even at ripple voltages of 2V<sub>PP</sub> and higher.



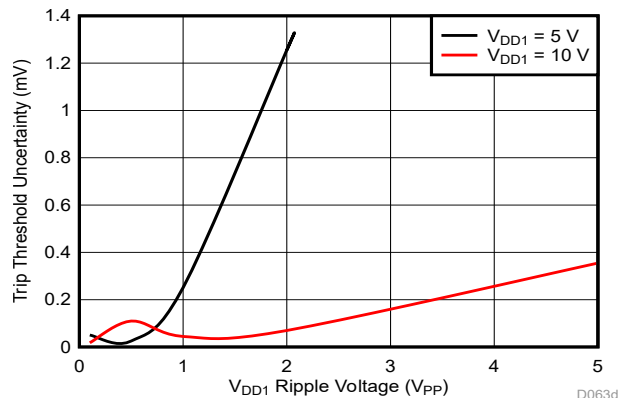
**Figure 7-3. Trip Threshold Sensitivity to VDD1 Ripple Voltage (Cmp0, f<sub>RIPPLE</sub> = 10kHz)**



**Figure 7-4. Trip Threshold Sensitivity to VDD1 Ripple Voltage (Cmp1, f<sub>RIPPLE</sub> = 10kHz)**



**Figure 7-5. Trip Threshold Sensitivity to VDD1 Ripple Voltage (Cmp2,  $f_{\text{RIPPLE}} = 10\text{kHz}$ )**



**Figure 7-6. Trip Threshold Sensitivity to VDD1 Ripple Voltage (Cmp3,  $f_{\text{RIPPLE}} = 10\text{kHz}$ )**

### 7.3 Best Design Practices

Keep the connection between the low-side of the sense resistor and the GND1 pin of the AMC23C15-Q1 short and low impedance. Any voltage drop in the ground line adds error to the voltage sensed at the input of the comparator and leads to inaccuracies in the trip thresholds.

For best common-mode transient immunity, place the filter capacitor C5 as closely to the REF pin as possible as illustrated in [Figure 7-8](#). Use a low-value pullup resistor ( $<10\text{k}\Omega$ ) on the open-drain output, as explained in the [Open-Drain Digital Outputs](#) section, to minimize the effect of capacitive coupling on the open-drain signal line during a common-mode transient event.

Do not exceed the  $300\text{mV}$   $V_{\text{REF}}$  limit specified in the [Recommended Operating Conditions](#) table for bidirectional current-sensing applications. Do not operate the device with the REF pin biased close to the  $V_{\text{MSEL}}$  threshold ( $450\text{mV}$  to the  $600\text{mV}$  range) to avoid dynamic switching of the Cmp0 hysteresis as explained in the [Reference Input](#) section.

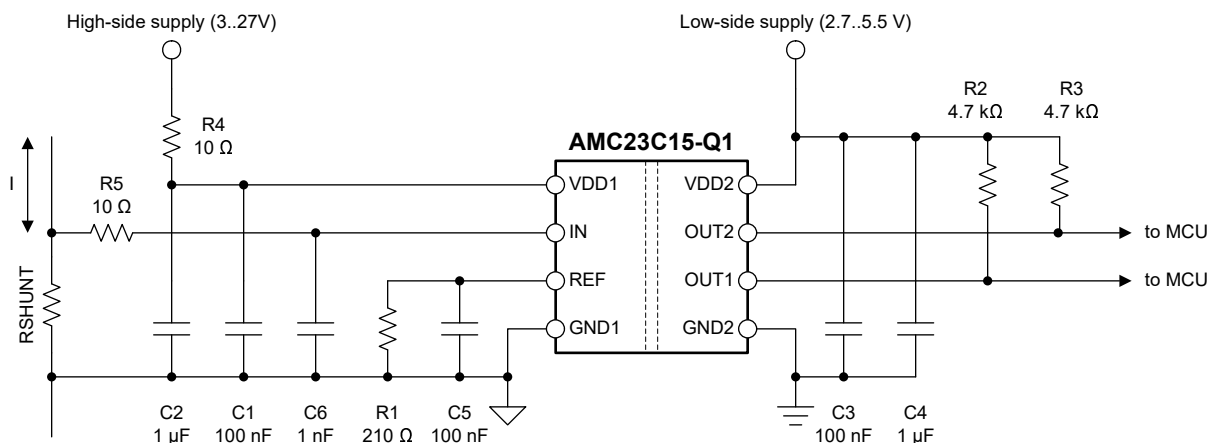
The AMC23C15-Q1 provides a limited  $200\mu\text{s}$  blanking time ( $t_{\text{HS,BLK}}$ ) to allow the reference voltage ( $V_{\text{REF}}$ ) to settle during start-up. For many applications, the reference voltage takes longer to settle than the  $200\mu\text{s}$  blanking time and the output of the comparator can possibly glitch during system start-up as described in [Figure 6-2](#). Consider the reference voltage settling time in the overall system start-up design.



## 7.4 Power Supply Recommendations

The AMC23C15-Q1 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1μF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1μF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 7-7 shows a decoupling schematic for the AMC23C15-Q1.

For high VDD1 supply voltages (>5.5V) place a 10Ω resistor (R4) in series with the VDD1 power supply for additional filtering.



**Figure 7-7. Decoupling of the AMC23C15-Q1**

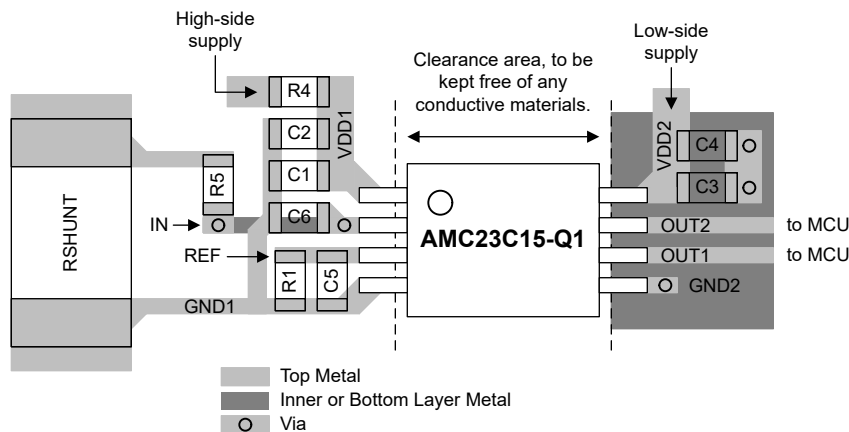
Capacitors must provide adequate effective capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of the nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

## 7.5 Layout

### 7.5.1 Layout Guidelines

Figure 7-8 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC23C15-Q1 supply pins) and placement of the other components required by the device.

### 7.5.2 Layout Example



**Figure 7-8. Recommended Layout of the AMC23C15-Q1**

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Isolation Glossary application note](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application note](#)
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity application note](#)
- Texas Instruments, [TPSI3050-Q1 Automotive Reinforced Isolated Switch Driver with Integrated 10V Gate Supply data sheet](#)
- Texas Instruments, [Isolated Amplifier Voltage Sensing Excel Calculator design tool](#)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.4 Trademarks

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### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from March 27, 2023 to September 30, 2024 (from Revision \* (March 2023) to Revision A (December 2024))

|   | Page |
|---|------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1    |
| • Changed $V_{IOWM}$ from 750V <sub>RMS</sub> to 1000V <sub>RMS</sub> .....                           | 6    |
| • Changed $V_{IOWM}$ from 1060V <sub>DC</sub> to 1410V <sub>DC</sub> .....                            | 6    |
| • Added Safety-Related Certificate number.....  | 7    |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">AMC23C15QDWVRQ1</a> | Active        | Production           | SOIC (DWV)   8 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | MC23C15Q            |
| AMC23C15QDWVRQ1.A               | Active        | Production           | SOIC (DWV)   8 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | MC23C15Q            |
| AMC23C15QDWVRQ1.B               | Active        | Production           | SOIC (DWV)   8 | 1000   LARGE T&R      | -           | Call TI                              | Call TI                           | -40 to 125   |                     |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF AMC23C15-Q1 :

- Catalog : [AMC23C15](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AMC23C15QDWVRQ1 | SOIC         | DWV             | 8    | 1000 | 330.0              | 16.4               | 12.05   | 6.15    | 3.3     | 16.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

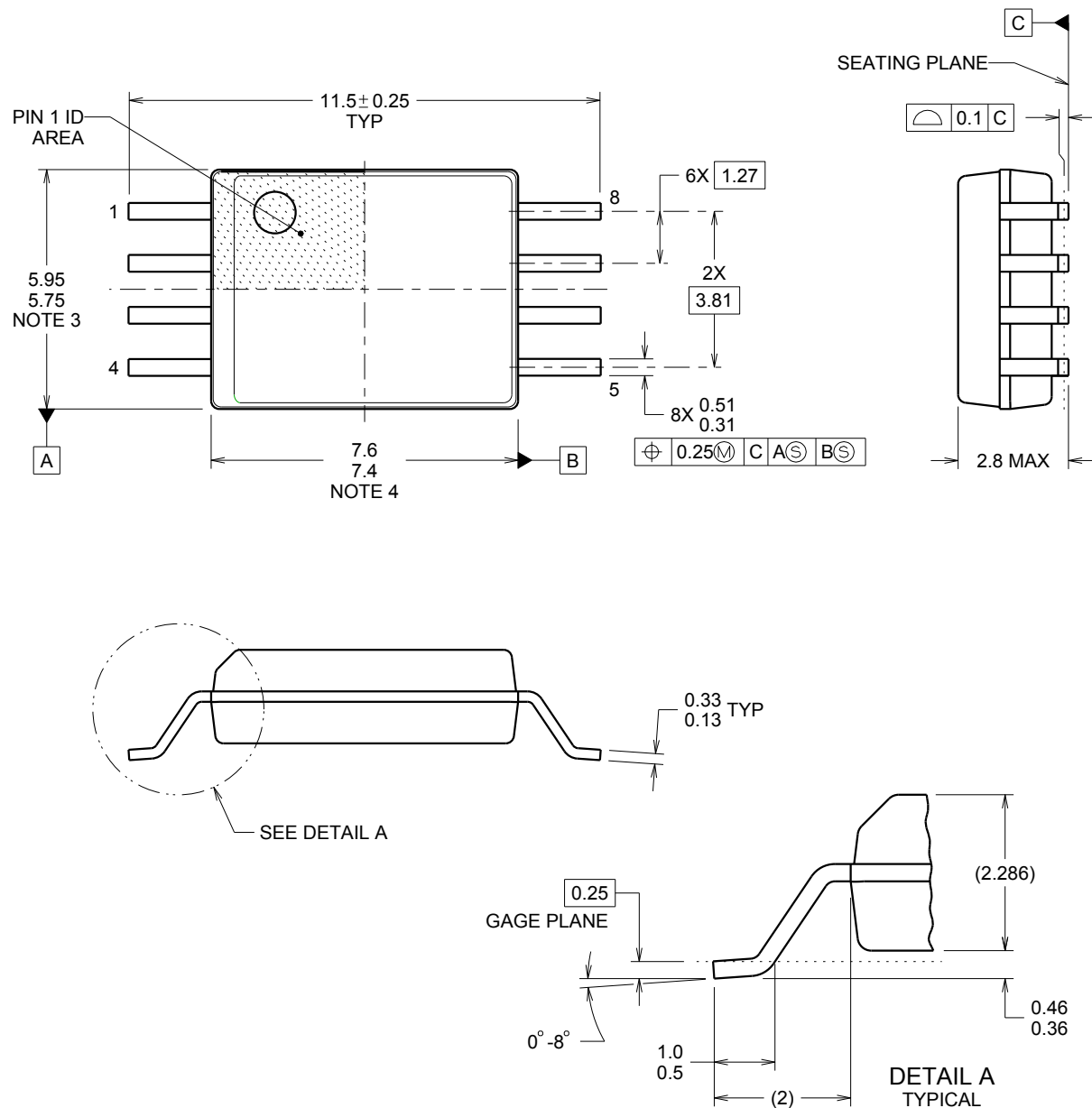
| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| AMC23C15QDWVRQ1 | SOIC         | DWV             | 8    | 1000 | 350.0       | 350.0      | 43.0        |

DWV0008A



SOIC - 2.8 mm max height

SOIC

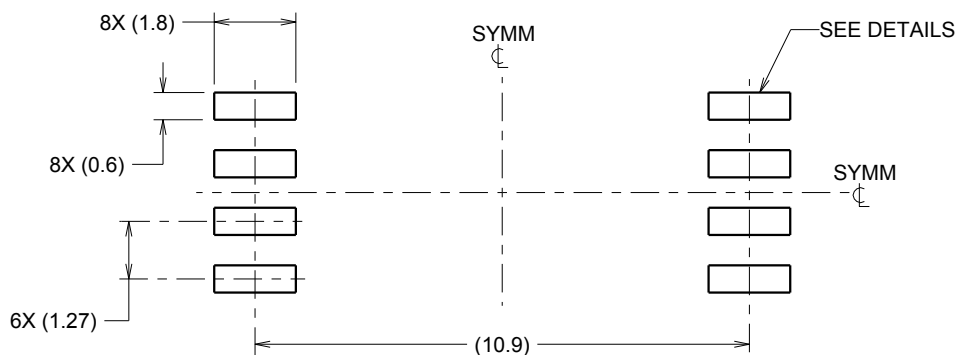


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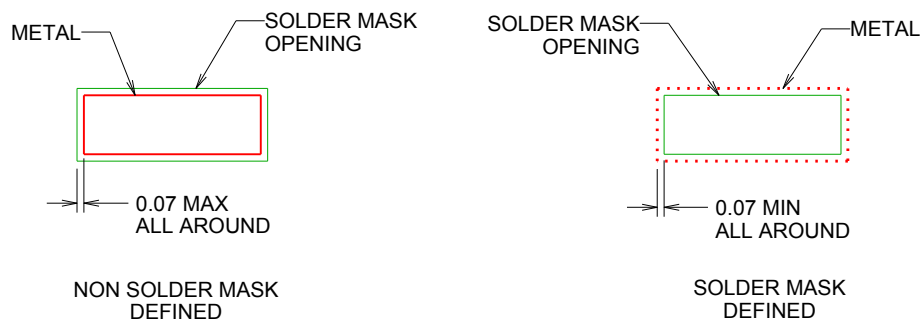
## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.





LAND PATTERN EXAMPLE  
9.1 mm NOMINAL CLEARANCE/CREEPAGE  
SCALE:6X

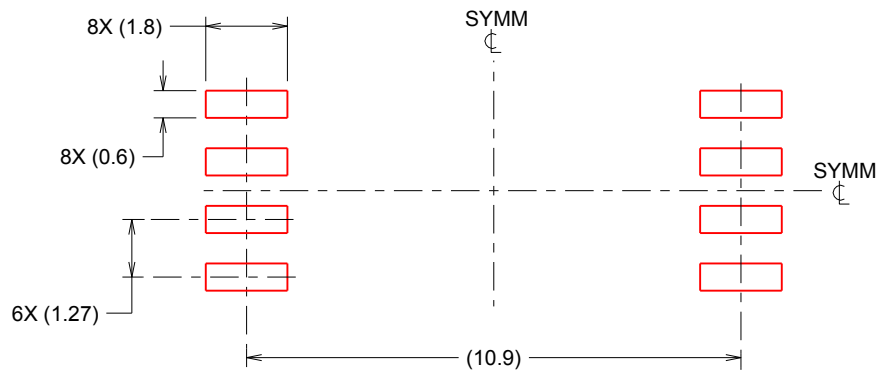


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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