AMC1302-Q1 Automotive, Precision, ±50-mV Input, Reinforced Isolated Amplifier

1 Features

- AEC-Q100 qualified for automotive applications:
  – Temperature grade 1: –40°C to 125°C, T_A
- Functional Safety-Capable
  – Documentation available to aid functional safety system design
- ±50-mV input voltage range optimized for current measurements using shunt resistors
- Fixed gain: 41
- Low DC errors:
  – Offset error: ±50 µV (max)
  – Offset drift: ±0.8 µV/°C (max)
  – Gain error: ±0.2% (max)
  – Gain drift: ±35 ppm/°C (max)
  – Nonlinearity: 0.03% (max)
- 3.3-V or 5-V operation on high-side and low-side
- Fail-safe output
- High CMTI: 100 kV/µs (min)
- Low EMI, meets CISPR-11 and CISPR-25 standards
- Safety-related certifications:
  – 7000-V_{PK} reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  – 5000-V_{RMS} isolation for 1 minute per UL1577

2 Applications

- Shunt-resistor-based current sensing in:
  – HEV/EV onboard chargers (OBC)
  – HEV/EV DC/DC converters
  – HEV/EV inverters and motor control
  – HEV/EV eTurbo/chargers

3 Description

The AMC1302-Q1 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to DIN EN IEC 60747-17 (VDE 0884-17), and supports a working voltage of up to 1.5 kV_{RMS}.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from hazardous voltages and damage.

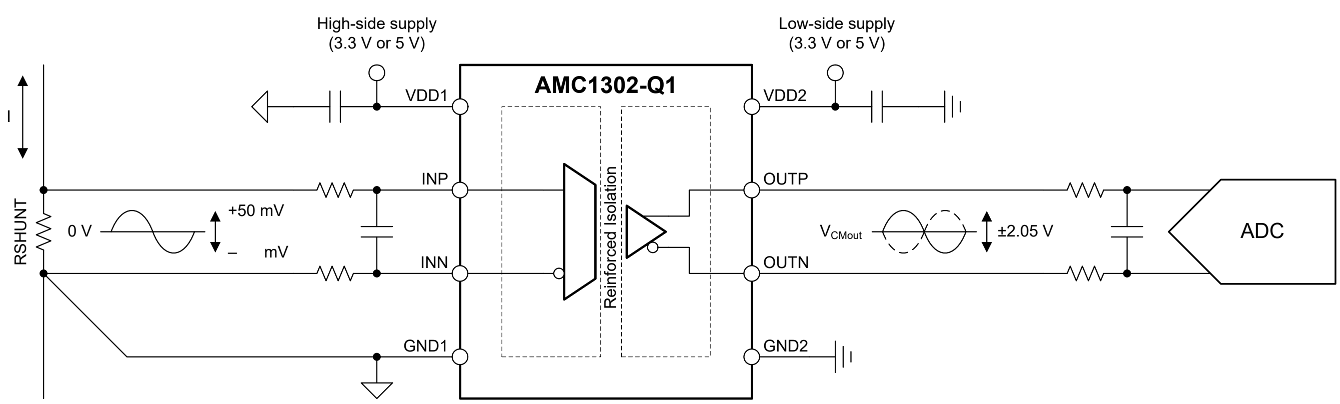
The input of the AMC1302-Q1 is optimized for direct connection to a low-impedance shunt resistor or other low-impedance voltage source with low signal levels. The excellent DC accuracy and low temperature drift supports accurate current control in PFC stages, DC/DC converters, traction inverters, and OBCs over the full automotive temperature range from –40°C to +125°C.

The integrated missing-shunt and missing high-side supply detection features simplify system-level design and diagnostics.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1302-Q1	SOIC (8)	5.85 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2021) to Revision B (June 2022) **Page**

- Added Functional Safety-Capable bullets to *Features* section.......1
- Changed isolation standard from DIN VDE V 0884-11 (VDE V 0884-11) to DIN EN IEC 60747-17 (VDE 0884-17) and updated the *Insulation Specifications* and *Safety-Related Certifications* tables accordingly.......1
- Changed reinforced isolation from *7071* V_{PK} to *7000* V_{PK}.......1
- Changed *Applications* section.......1

Changes from Revision * (October 2018) to Revision A (April 2021) **Page**

- *Updated the numbering format for tables, figures, and cross-references throughout the document*.......1
- Changed VDE certificate in *Safety-related certifications* Features bullet from DIN V VDE V 0884-11 (VDE V 0884-11) to *DIN VDE V 0884-11*.......1
- Changed *CMTI* specification from *140 kV/µs (typ), 70 kV/µs (min)* to *100 kV/µs (min)* in *Features* section.......1
- Changed V_{OS} from –100 µV / ±10 µV / 100 µV to –50 µV / ±2.5 µV / 50 µV (min / typ / max).......8
- Changed E_G from –0.3% / ±0.05% / 0.3% to –0.2% / ±0.04% / 0.2% (min / typ / max).......8
- Changed TCE_G from –50 ppm/°C / ±15 ppm/°C / 50 ppm/°C to –35 ppm/°C / ±3 ppm/°C / 35 ppm/°C (min / typ / max).......8
- Changed $V_{Failsafe}$ from –2.6 V / –2.5 V (typ / max) to –2.63 V / –2.57 V / –2.53 V (min / typ / max).......8
- Changed CMTI from 55 kV/µs / 80 kV/µs to 100 kV/µs, 150 kV/µs (min / typ).......8
- Changed $VDD1_{POR}$ from 1.75 V / 2.15 V / 2.7 V to 2.4 V / 2.6 V / 2.8 V (min / typ / max).......8
- Changed *Rise, Fall, and Delay Time Waveforms* image.......9
- Changed *Power-Supply Rejection Ratio vs Ripple Frequency* figure.......11

5 Pin Configuration and Functions

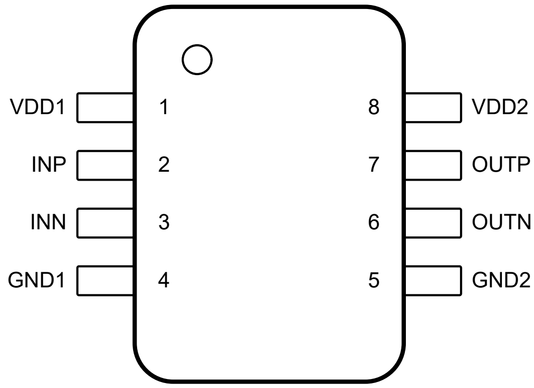


Figure 5-1. DWV Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply.(1)
2	INP	Analog input	Noninverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage.(2)
3	INN	Analog input	Inverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage.(2)
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply.(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2) See the *Layout* section for details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	V
Analog input voltage	INP, INN	GND1 – 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 [(1)], HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1	3	5	5.5	V
	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$		±64		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} – V_{INN}$	–50		50	mV
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN})$ / 2 to GND1	–0.032		VDD1 – 2.2	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–55		125	°C
	Specified ambient temperature		–40		125	

6.4 Thermal Information

THERMAL METRIC(1)		AMC1302-Q1 DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	99	mW
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 3.6 V	31	mW
		VDD1 = 5.5 V	54	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 3.6 V	26	mW
		VDD2 = 5.5 V	45	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8400	
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	9800	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5 V_{PP} at 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500 V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 6000 V_{RMS}, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 85.4°C/W, VDDx = 5.5 V, T_J = 150°C, T_A = 25°C			266	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 85.4°C/W, VDDx = 3.6 V, T_J = 150°C, T_A = 25°C			407	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 85.4°C/W, T_J = 150°C, T_A = 25°C			1464	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = – 40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = – 50 mV to + 50 mV, and INN = GND1; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{CMov}	Common-mode overvoltage detection level	$(V_{INP} + V_{INN})$ / 2 to GND1	VDD1 – 2			V
	Hysteresis of common-mode overvoltage detection level			60		mV
V_{OS}	Input offset voltage[(1) (2)]	T_A = 25°C, $V_{INP} = V_{INN}$ = GND1	–50	±2.5	50	µV
TCV_{OS}	Input offset drift[(1) (2) (3)]		–0.8	±0.15	0.8	µV/°C
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \le V_{CM} \le V_{VCM\ max}$		–100		dB
		f_{IN} = 10 kHz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–98		
C_{IN}	Single-ended input capacitance	INN = GND1, f_{IN} = 300 kHz		4		pF
C_{IND}	Differential input capacitance	f_{IN} = 300 kHz		2		
R_{IN}	Single-ended input resistance	INN = GND1		4.75		kΩ
R_{IND}	Differential input resistance			4.9		
I_{IB}	Input bias current	INP = INN = GND1; $I_{IB} = (I_{IBP} + I_{IBN})$ / 2	–48.5	–36	–28.5	uA
TCI_{IB}	Input bias current drift			±1.5		nA/°C
I_{IO}	Input offset current	$I_{IO} = I_{IBP} – I_{IBN}$		±10		nA
ANALOG OUTPUT						
	Nominal gain			41		
E_G	Gain error[(1)]	T_A = 25°C	–0.2%	±0.04%	0.2%	
TCE_G	Gain error drift[(1) (4)]		–35	±3	35	ppm/°C
	Nonlinearity[(1)]		–0.03%	±0.01%	0.03%	
	Nonlinearity drift			1		ppm/°C
THD	Total harmonic distortion	f_{IN} = 10 kHz		–85		dB
	Output noise	INP = INN = GND1, f_{IN} = 0 Hz, BW = 100 kHz brickwall filter		260		$µV_{RMS}$
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, BW = 10 kHz	80	84		dB
		f_{IN} = 10 kHz, BW = 100 kHz		70		
PSRR	Power-supply rejection ratio[(2)]	PSRR vs VDD1, at DC		–113		dB
		PSRR vs VDD1, 100-mV and 10-kHz ripple		–108		
		PSRR vs VDD2, at DC		–116		
		PSRR vs VDD2, 100-mV and 10-kHz ripple		–87		
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	$V_{OUT} = (V_{OUTP} – V_{OUTN})$; $\|V_{IN}\| = \|V_{INP} – V_{INN}\| > \|V_{Clipping}\|$	–2.52	±2.49	2.52	V
$V_{Failsafe}$	Failsafe differential output voltage	$V_{CM} \ge V_{CMov}$, or VDD1 missing	–2.63	–2.57	–2.53	V
BW	Output bandwidth		220	280		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		< 0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, INN = INP = GND1, outputs shorted to either GND2 or VDD2		±14		mA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1 kV	100	150		kV/µs

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = – 40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = – 50 mV to + 50 mV, and INN = GND1; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$VDD1_{POR}$	VDD1 power-on-reset threshold voltage	VDD1 falling	2.4	2.6	2.8	V
IDD1	High-side supply current	3.0 V ≤ VDD1 ≤ 3.6 V		6.2	8.5	mA
		4.5 V ≤ VDD1 ≤ 5.5 V		7.2	9.8	
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		5.3	7.2	
		4.5 V ≤ VDD2 ≤ 5.5 V		5.9	8.1	

(1) The typical value includes one standard deviation ("sigma") at nominal operating conditions.
(2) This parameter is input referred.
(3) Offset error temperature drift is calculated using the box method, as described by the following equation: $TCV_{OS} = (V_{OS,MAX} - V_{OS,MIN}) / TempRange$ where $V_{OS,MAX}$ and $V_{OS,MIN}$ refer to the maximum and minimum V_{OS} values measured within the temperature range (–40 to 125℃).
(4) Gain error temperature drift is calculated using the box method, as described by the following equation: $TCE_G\ (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125℃).

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.5		μs
t_f	Output signal fall time			1.5		μs
	V_{INx} to V_{OUTx} signal delay (50% – 10%)	unfiltered output		1	1.5	μs
	V_{INx} to V_{OUTx} signal delay (50% – 50%)	unfiltered output		1.6	2.1	μs
	V_{INx} to V_{OUTx} signal delay (50% – 90%)	unfiltered output		2.5	3	μs
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP and OUTN valid, 0.1% settling		500		μs

6.11 Timing Diagram

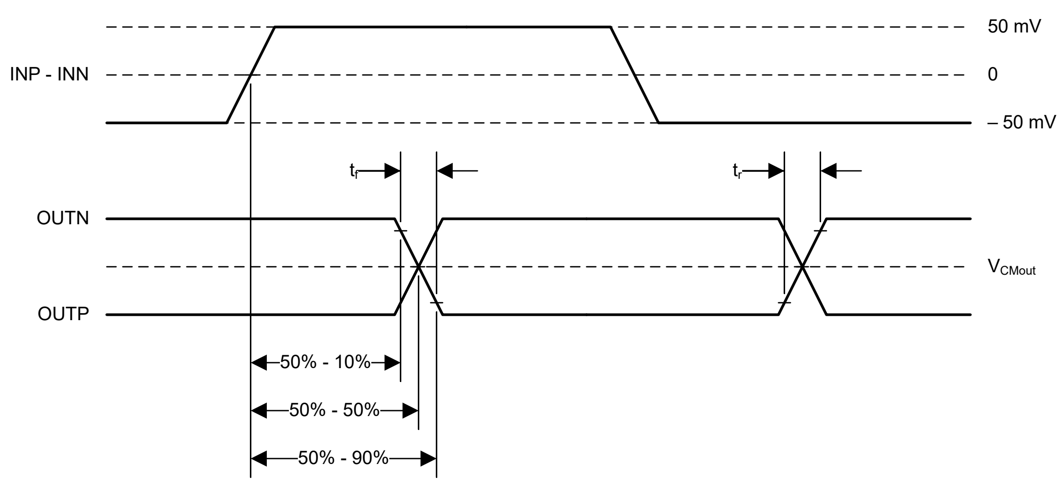


Figure 6-1. Rise, Fall, and Delay Time Waveforms

6.12 Insulation Characteristics Curves

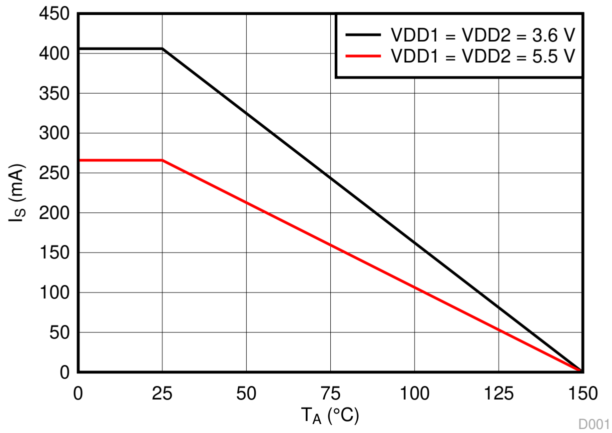


Figure 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

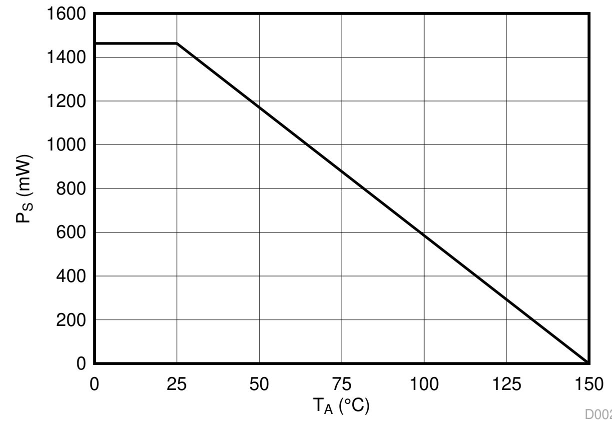
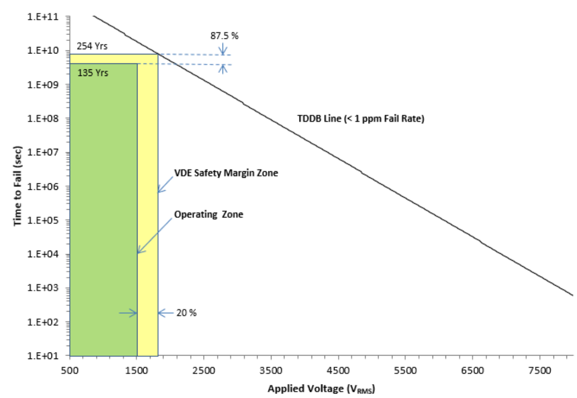


Figure 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

Figure 6-4. Reinforced Isolation Capacitor Lifetime Projection

6.13 Typical Characteristics

at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, INP = –50 mV to 50 mV, INN = GND1, and f_{IN} = 10 kHz (unless otherwise noted)

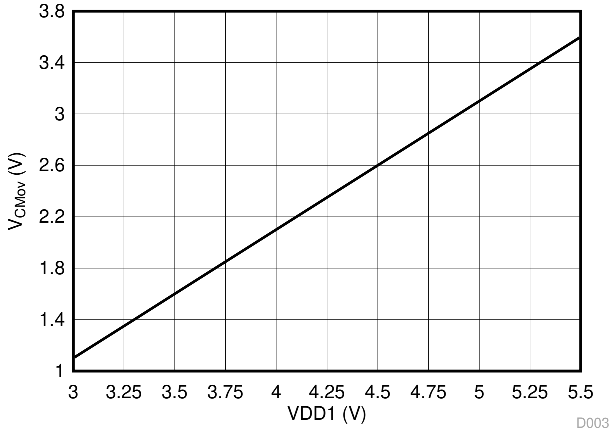


Figure 6-5. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage

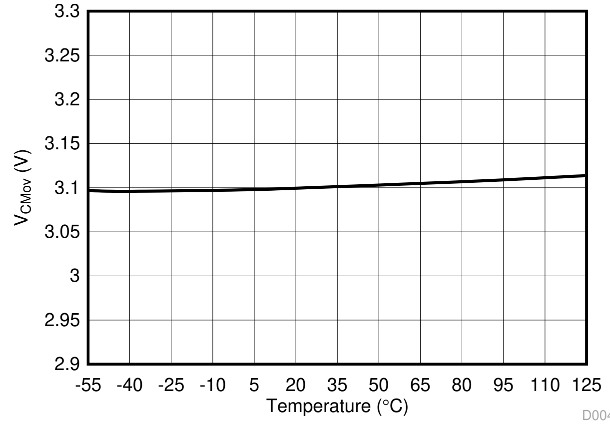


Figure 6-6. Common-Mode Overvoltage Detection Level vs Temperature

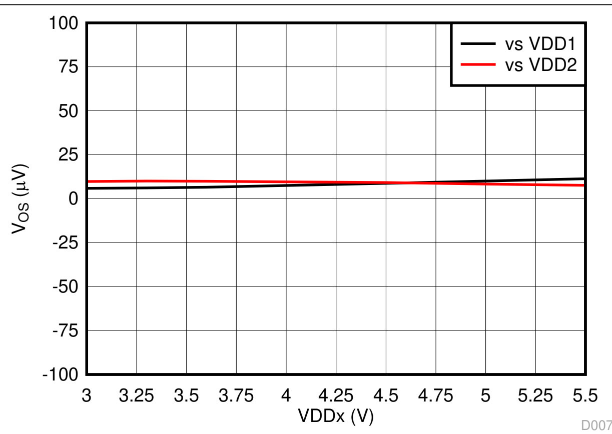


Figure 6-7. Input Offset Voltage vs Supply Voltage

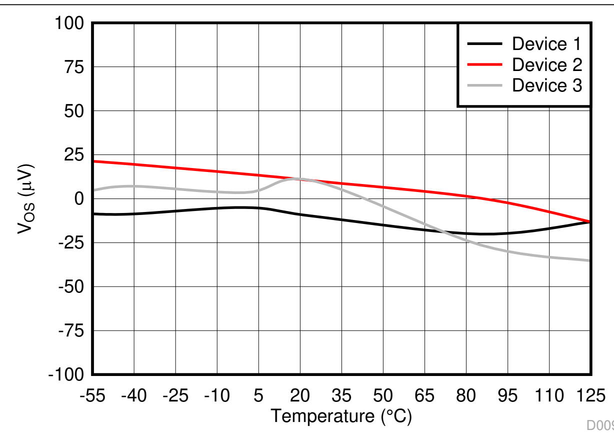


Figure 6-8. Input Offset Voltage vs Temperature

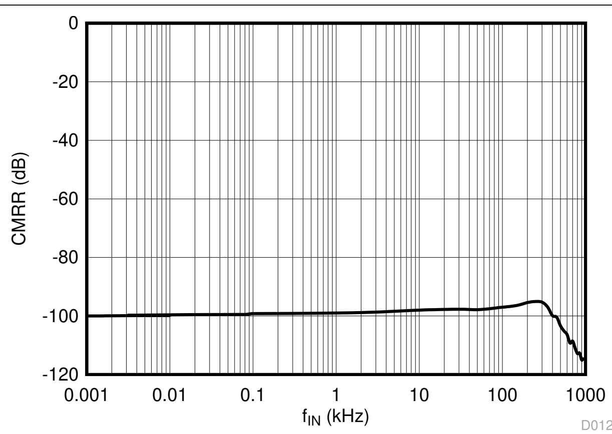


Figure 6-9. Common-Mode Rejection Ratio vs Input Frequency

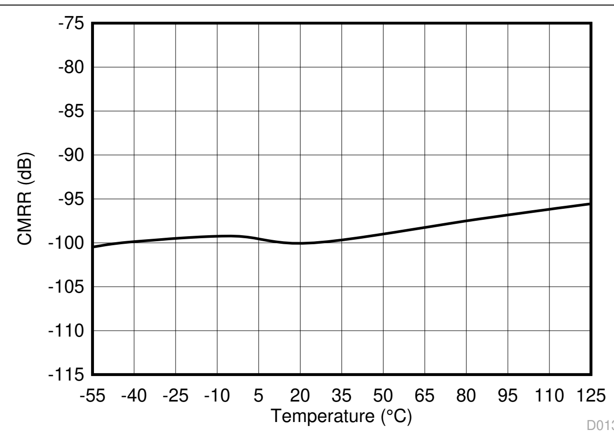


Figure 6-10. Common-Mode Rejection Ratio vs Temperature

6.13 Typical Characteristics (continued)

at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, INP = –50 mV to 50 mV, INN = GND1, and f_{IN} = 10 kHz (unless otherwise noted)

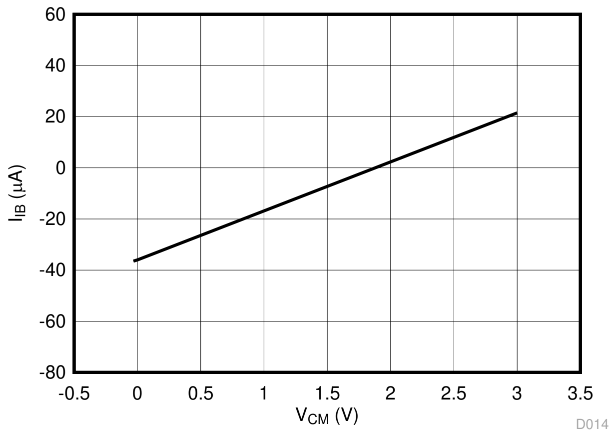


Figure 6-11. Input Bias Current vs Common-Mode Input Voltage

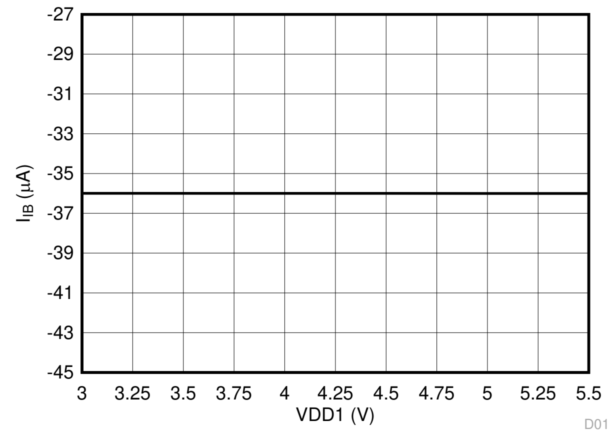


Figure 6-12. Input Bias Current vs High-Side Supply Voltage

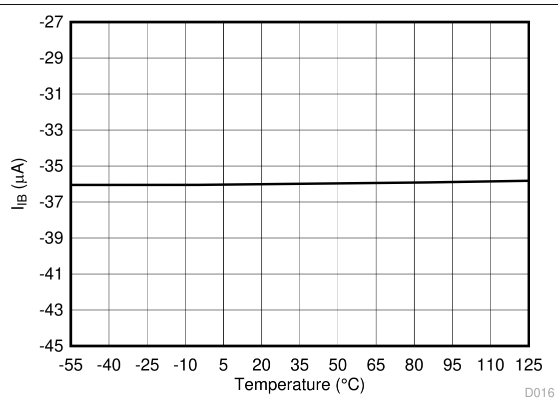


Figure 6-13. Input Bias Current vs Temperature

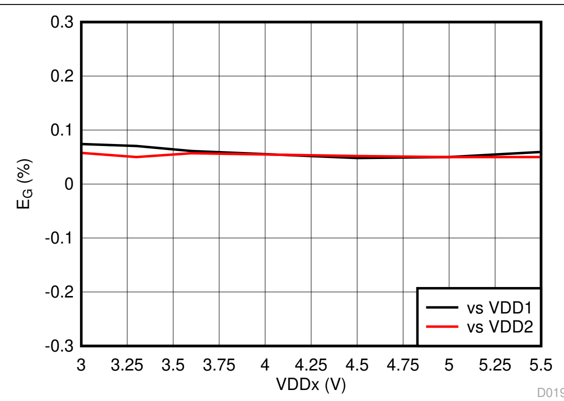


Figure 6-14. Gain Error vs Supply Voltage

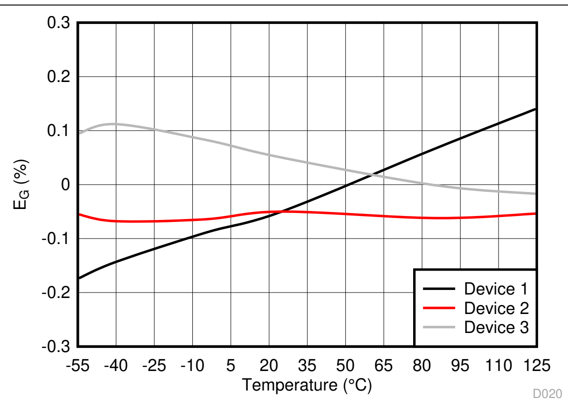


Figure 6-15. Gain Error vs Temperature

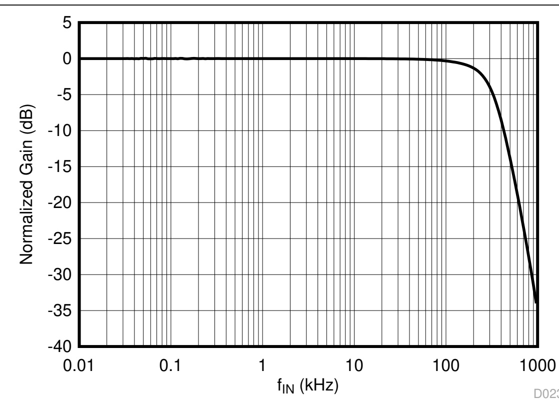


Figure 6-16. Normalized Gain vs Input Frequency

6.13 Typical Characteristics (continued)

at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, INP = –50 mV to 50 mV, INN = GND1, and f_{IN} = 10 kHz (unless otherwise noted)

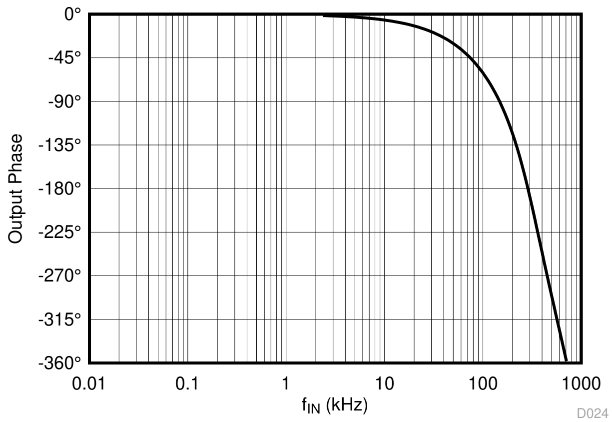


Figure 6-17. Output Phase vs Input Frequency

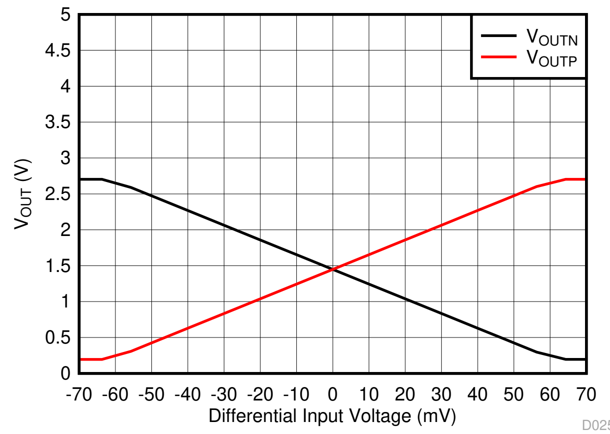


Figure 6-18. Output Voltage vs Input Voltage

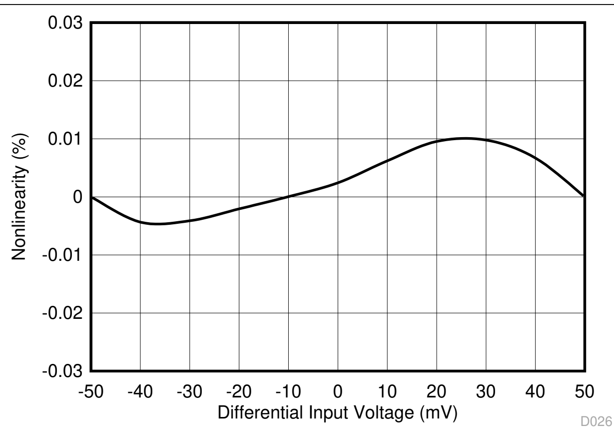


Figure 6-19. Nonlinearity vs Input Voltage

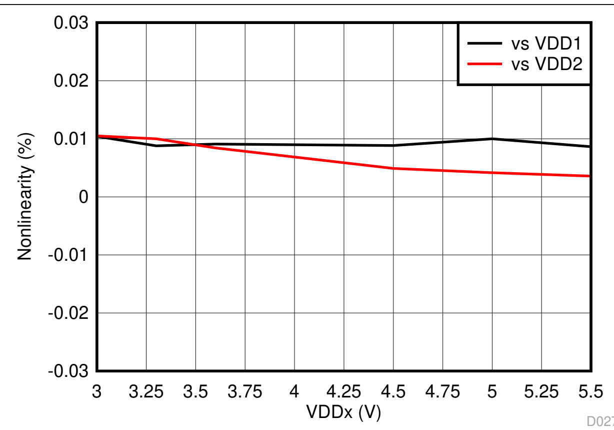


Figure 6-20. Nonlinearity vs Supply Voltage

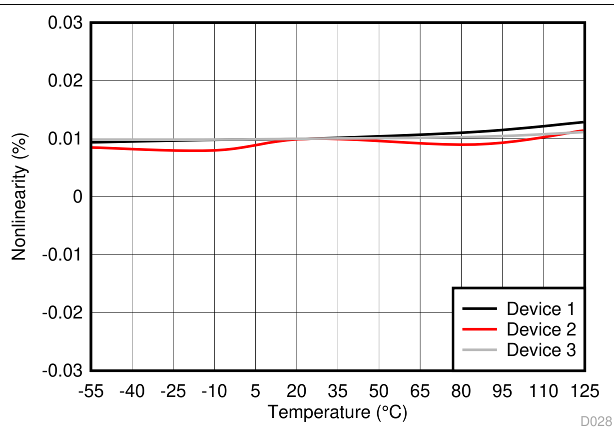


Figure 6-21. Nonlinearity vs Temperature

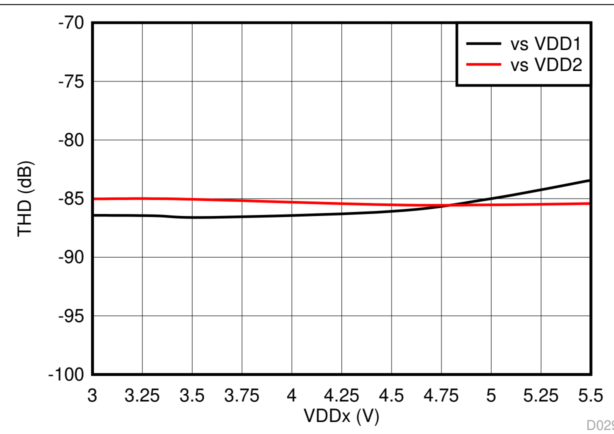


Figure 6-22. Total Harmonic Distortion vs Supply Voltage

6.13 Typical Characteristics (continued)

at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, INP = –50 mV to 50 mV, INN = GND1, and f_{IN} = 10 kHz (unless otherwise noted)

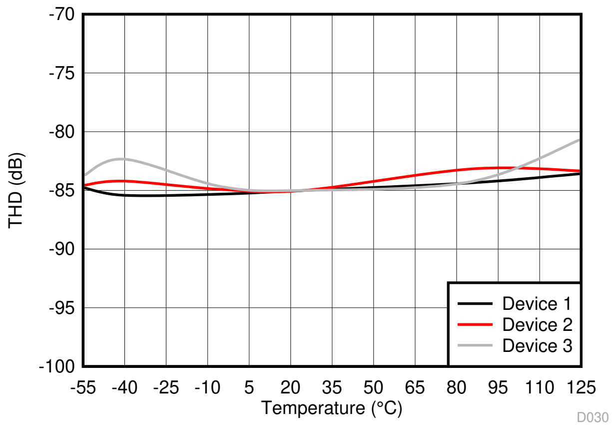


Figure 6-23. Total Harmonic Distortion vs Temperature

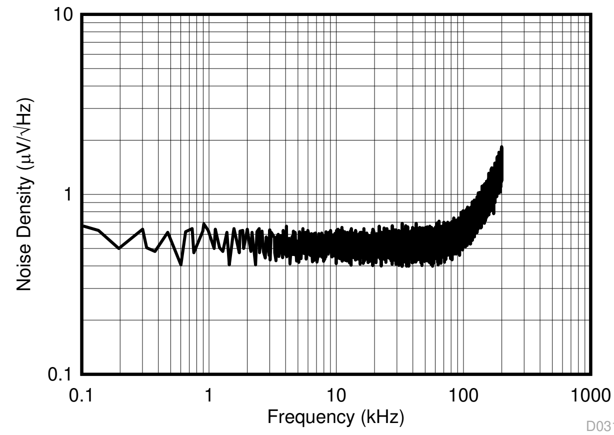


Figure 6-24. Output Noise Density vs Frequency

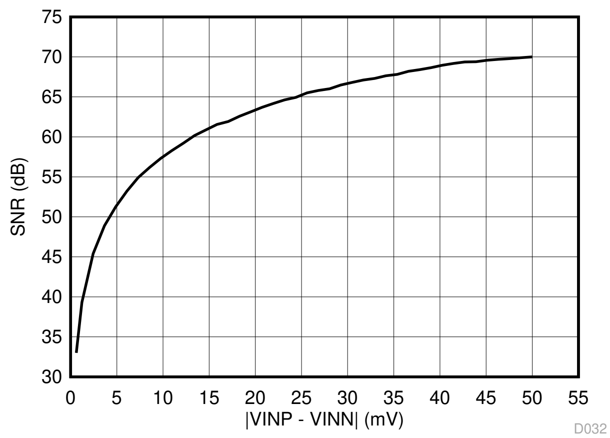


Figure 6-25. Signal-to-Noise Ratio vs Input Voltage

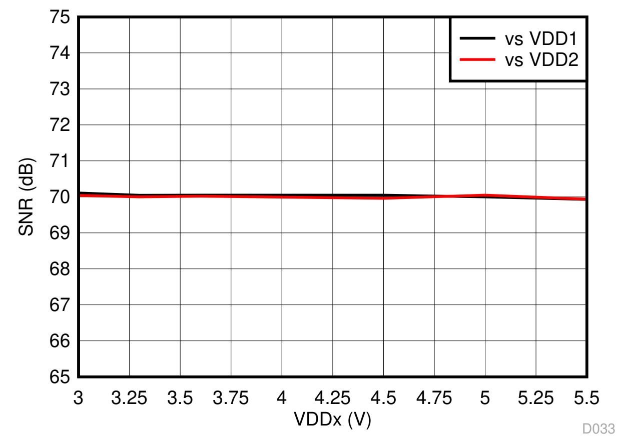


Figure 6-26. Signal-to-Noise Ratio vs Supply Voltage

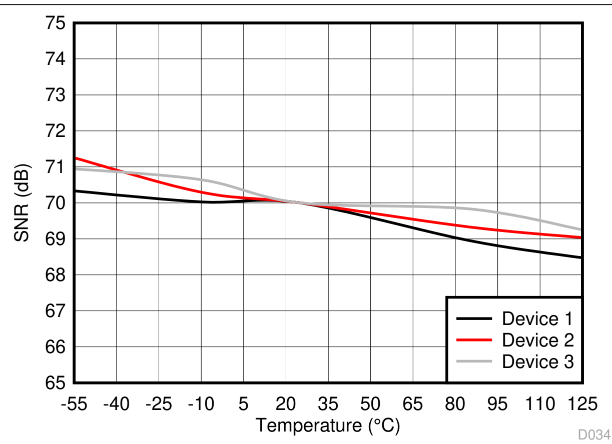


Figure 6-27. Signal-to-Noise Ratio vs Temperature

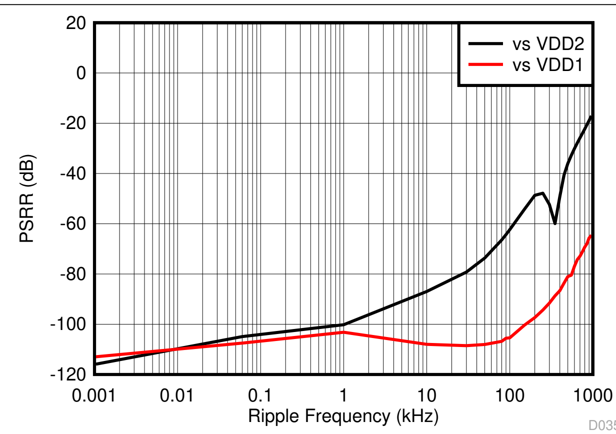


Figure 6-28. Power-Supply Rejection Ratio vs Ripple Frequency

6.13 Typical Characteristics (continued)

at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, INP = –50 mV to 50 mV, INN = GND1, and f_{IN} = 10 kHz (unless otherwise noted)

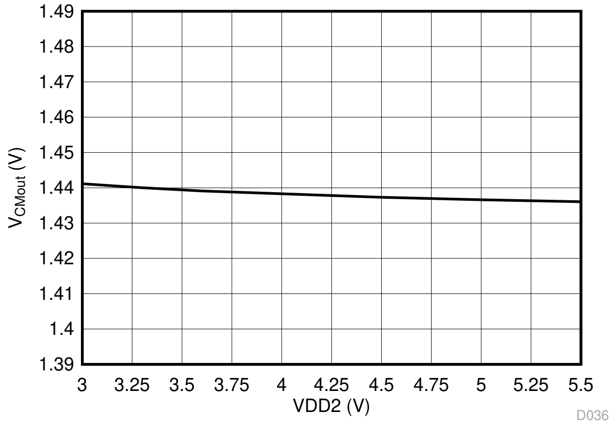


Figure 6-29. Output Common-Mode Voltage vs Low-Side Supply Voltage

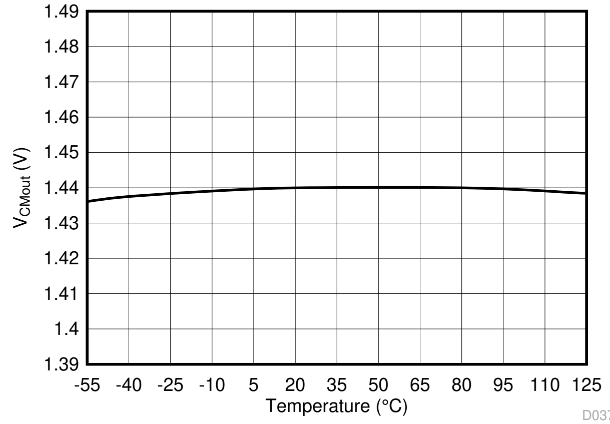


Figure 6-30. Output Common-Mode Voltage vs Temperature

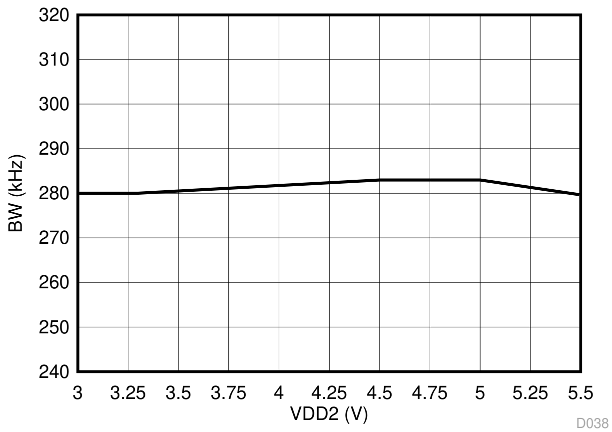


Figure 6-31. Output Bandwidth vs Low-Side Supply Voltage

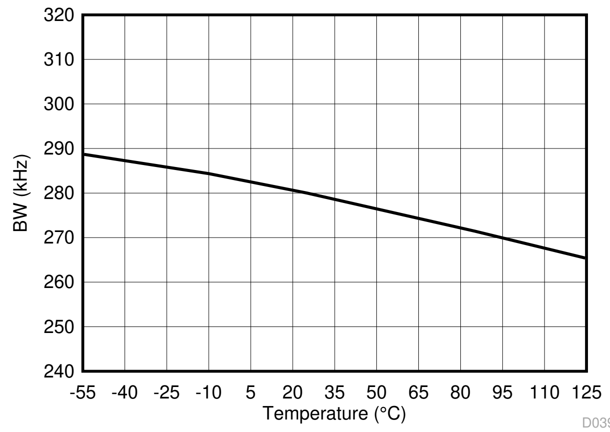


Figure 6-32. Output Bandwidth vs Temperature

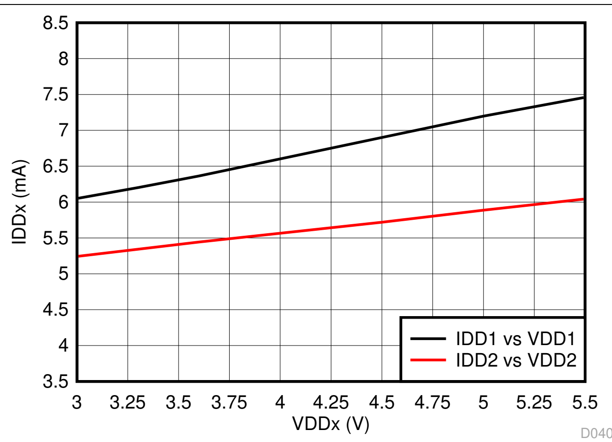


Figure 6-33. Supply Current vs Supply Voltage

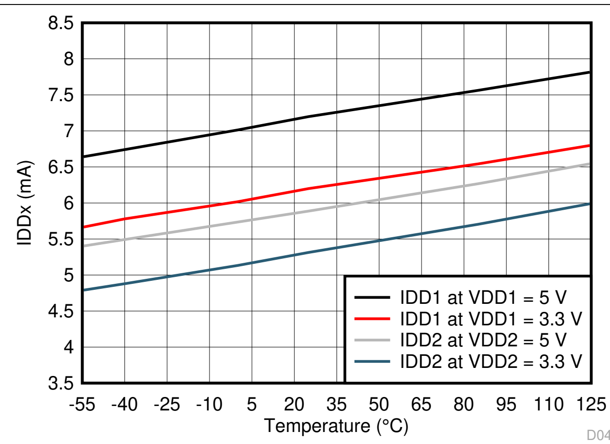


Figure 6-34. Supply Current vs Temperature

6.13 Typical Characteristics (continued)

at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, INP = –50 mV to 50 mV, INN = GND1, and f_{IN} = 10 kHz (unless otherwise noted)

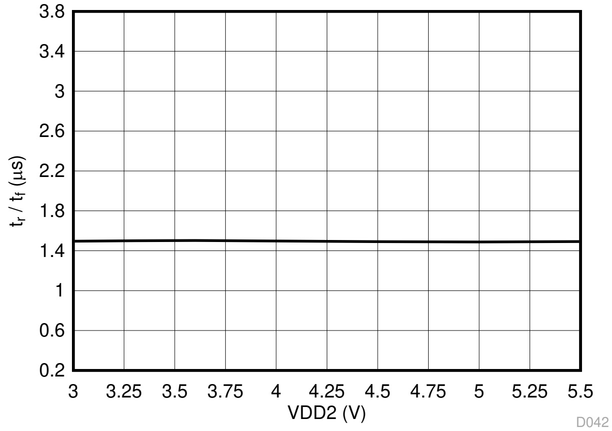


Figure 6-35. Output Rise and Fall Time vs Low-Side Supply Voltage

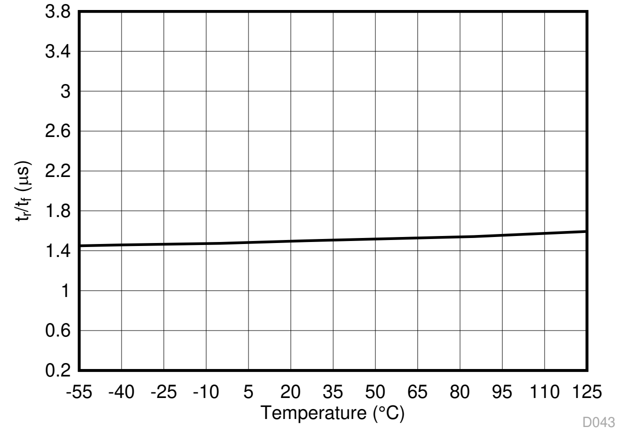


Figure 6-36. Output Rise and Fall Time vs Temperature

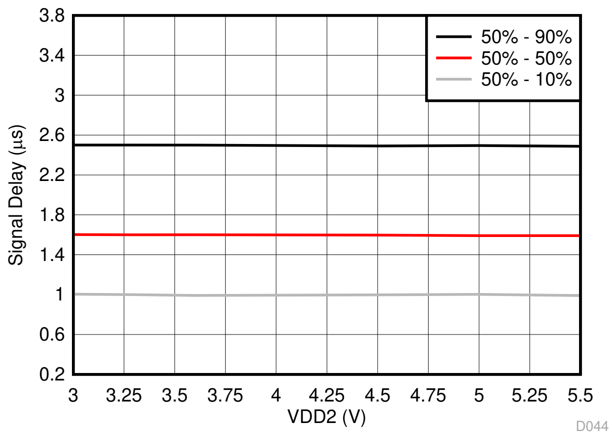


Figure 6-37. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

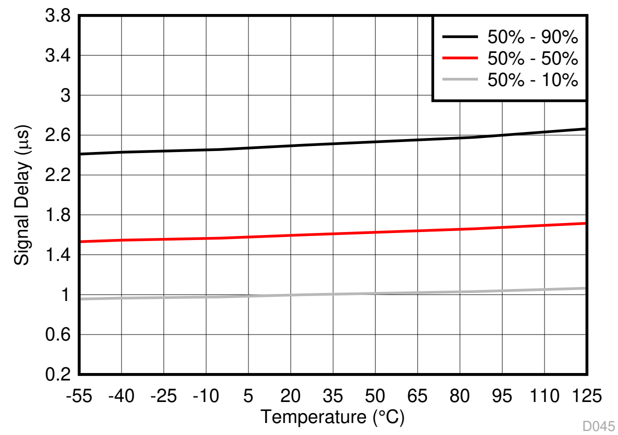


Figure 6-38. V_{IN} to V_{OUT} Signal Delay vs Temperature

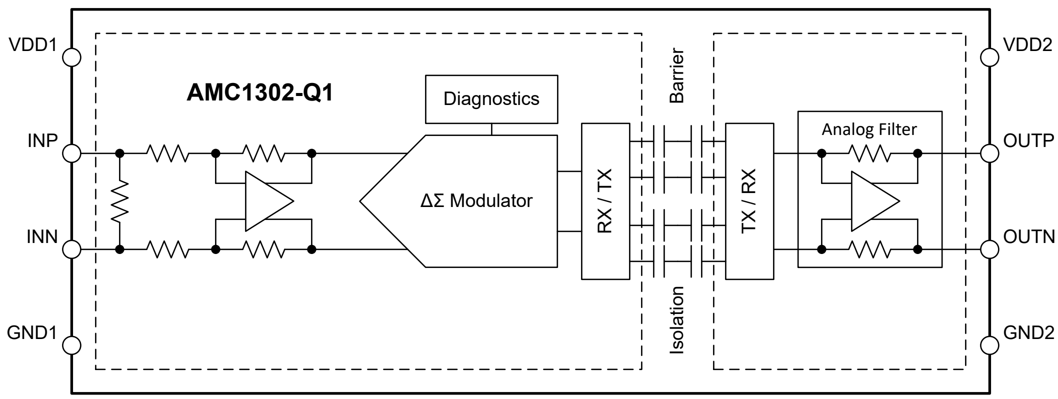
7 Detailed Description

7.1 Overview

The AMC1302-Q1 is a fully differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins that is proportional to the input signal.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation used in the AMC1302-Q1 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC1302-Q1 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R_{IND}. The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals INP and INN. First, if the input voltages V_{INP} or V_{INN} exceed the range specified in the *Absolute Maximum Ratings* table, the input currents must be limited to the absolute maximum value, because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) and within the common-mode input voltage range (V_{CM}) as specified in the *Recommended Operating Conditions* table.

7.3.2 Isolation Channel Signal Transmission

The AMC1302-Q1 uses an on-off keying (OOK) modulation scheme, as shown in Figure 7-1, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1302-Q1 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the 4th-order analog filter. The AMC1302-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

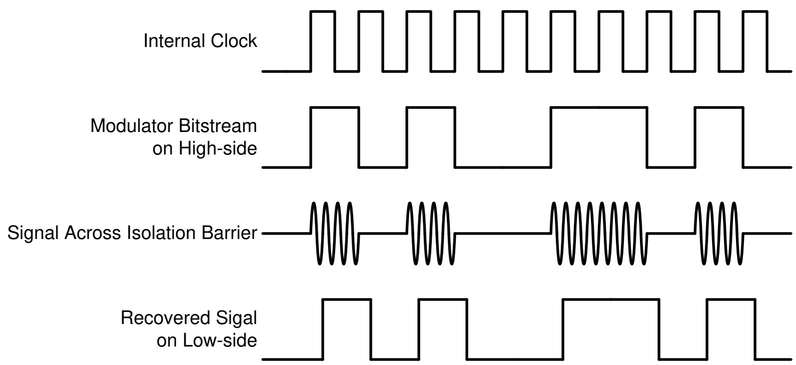


Figure 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC1302-Q1 offers a differential analog output comprised of the OUTP and OUTN pins. For differential input voltages (V_{INP} – V_{INN}) in the range from –50 mV to 50 mV, the device provides a linear response with a nominal gain of 41. For example, for a differential input voltage of 50 mV, the differential output voltage (V_{OUTP} – V_{OUTN}) is 2.05 V. At zero input (INP shorted to INN), both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For absolute differential input voltages greater than 50 mV but less than 64 mV, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in Figure 7-2, if the differential input voltage exceeds the $V_{Clipping}$ value.

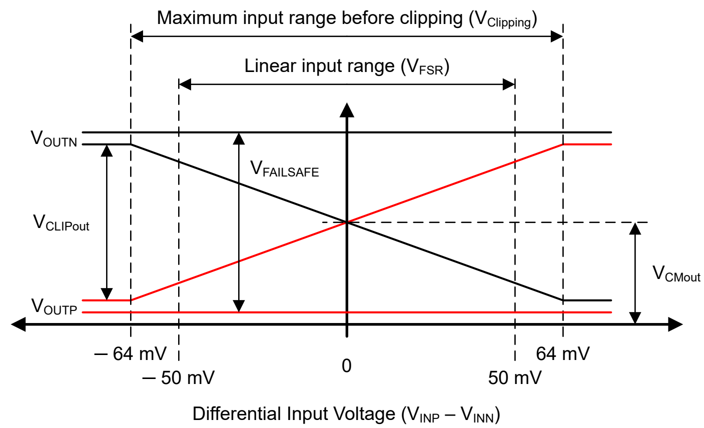


Figure 7-2. Output Behavior of the AMC1302-Q1

The AMC1302-Q1 offers a fail-safe feature that simplifies diagnostics on system level. Figure 7-2 shows the fail-safe mode, in which the AMC1302-Q1 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in two cases:

- When the high-side supply is missing or below the $VDD1_{UV}$ threshold
- When the common-mode input voltage, that is V_{CM} = (V_{INP} + V_{INN}) / 2, exceeds the common-mode overvoltage detection level V_{CMov}

Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for fail-safe detection on system level.

7.4 Device Functional Modes

The AMC1302-Q1 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The low analog input voltage range, excellent accuracy, and low temperature drift make the a high-performance solution for automotive applications where shunt-based current sensing in the presence of high common-mode voltage levels is required.

8.2 Typical Application

The AMC1302-Q1 is ideally suited for shunt-based current sensing applications where accurate current monitoring is required in the presence of high common-mode voltages.

Figure 8-1 shows the AMC1302-Q1 in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop that is sensed by the AMC1302-Q1. The AMC1302-Q1 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, reconstructs the analog signal, and presents that signal as a differential voltage on the output pins.

The differential input, differential output, and the high common-mode transient immunity (CMTI) of the AMC1302-Q1 ensure reliable and accurate operation even in high-noise environments.

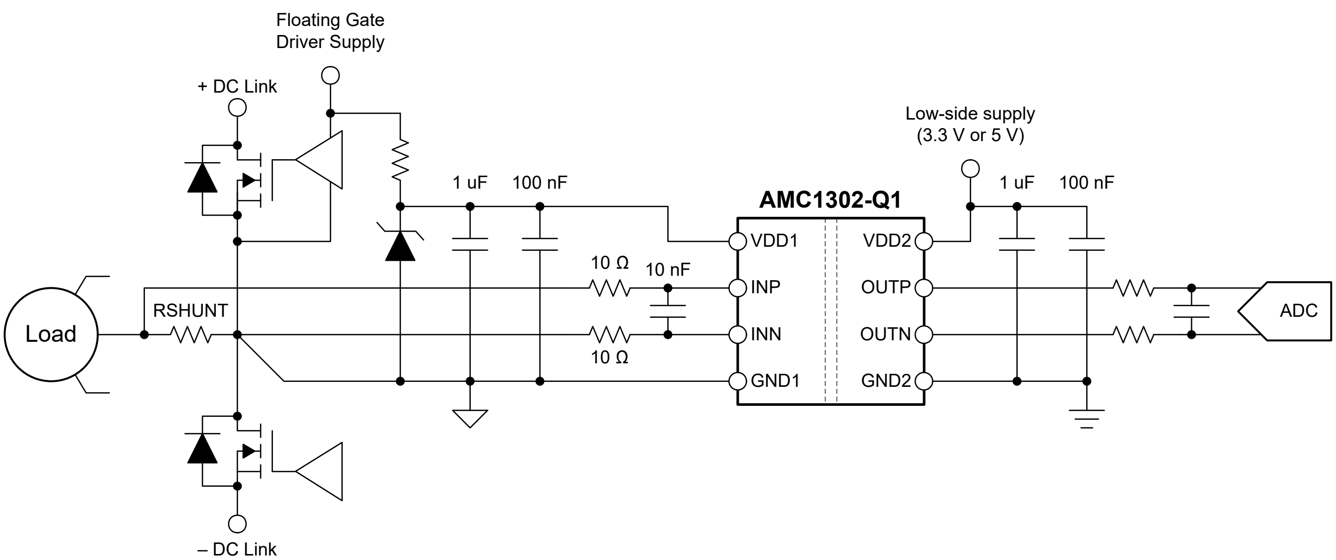


Figure 8-1. Using the AMC1302-Q1 for Current Sensing in a Typical Application

8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across RSHUNT for a linear response	±50 mV (maximum)
Signal delay (50% V_{IN} to 90% OUTP, OUTN)	3 µs (maximum)

8.2.2 Detailed Design Procedure

In Figure 8-1, the high-side power supply (VDD1) for the AMC1302-Q1 is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC1302-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC1302-Q1 are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the *Layout* section for more details.

8.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: V_{SHUNT} = I × RSHUNT.

Consider the following two restrictions when selecting the value of the shunt resistor, RSHUNT:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range for a linear response: $|V_{SHUNT}| \leq |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

8.2.2.2 Input Filter Design

TI recommends placing an RC-filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications, the structure shown in Figure 8-2 achieves excellent performance.

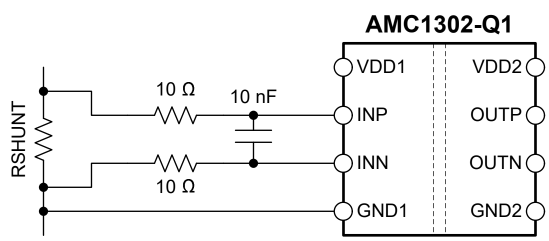


Figure 8-2. Differential Input Filter

8.2.2.3 Differential to Single-Ended Output Conversion

Figure 8-3 shows an example of a TLV313-Q1-based signal conversion and filter circuit for systems using single-ended-input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals (V_{OUTP} – V_{OUTN}) + V_{REF}. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.

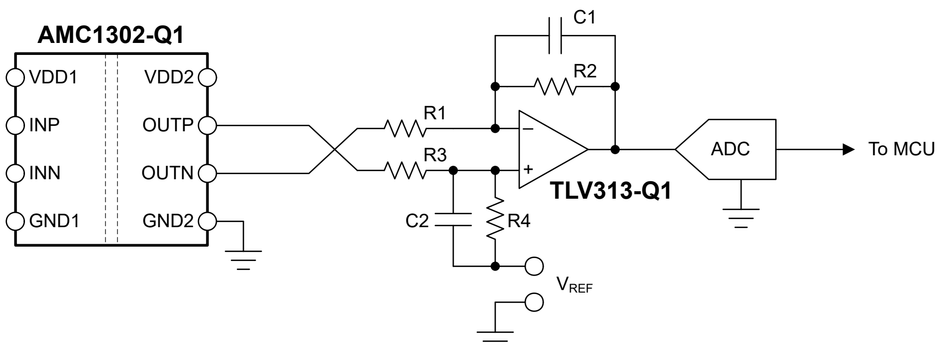


Figure 8-3. Connecting the AMC1302-Q1 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

8.2.3 Application Curve

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. Figure 8-4 shows the typical full-scale step response of the AMC1302-Q1.

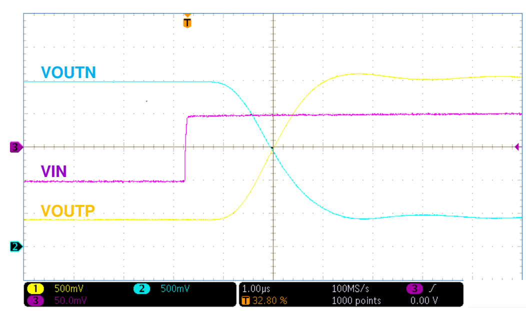


Figure 8-4. Step Response of the AMC1302-Q1

8.3 What to Do and What Not to Do

Do not leave the inputs of the AMC1302-Q1 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and the device outputs the fail-safe voltage as described in the *Analog Output* section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Do not exceed the input common-mode range as specified in the *Recommended Operating Conditions* table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the *Layout* section for more details.

9 Power Supply Recommendations

The AMC1302-Q1 does not require any specific power up sequencing. The high-side power-supply (VDD1) is decoupled with a low-ESR 100-nF capacitor (C1) parallel to a low-ESR 1-µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR 100-nF capacitor (C3) parallel to a low-ESR 1-µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

The ground reference for the high-side (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace (as shown in Figure 9-1) to make this connection instead of shorting GND1 to INN directly at the device input. If a four-terminal shunt is used, the device inputs are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt.

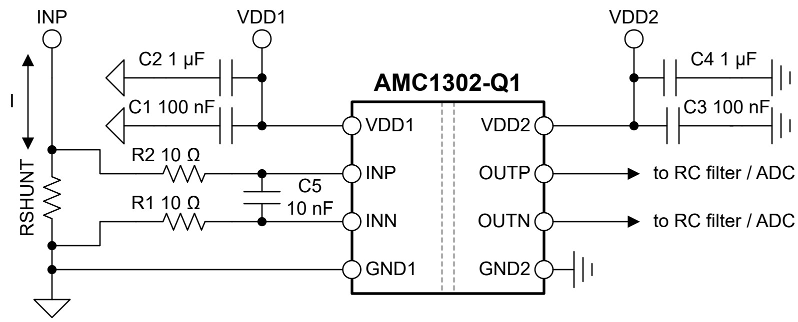


Figure 9-1. Decoupling of the AMC1302-Q1

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

10 Layout

10.1 Layout Guidelines

Figure 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1302-Q1 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1302-Q1 and keep the layout of both connections symmetrical.

10.2 Layout Example

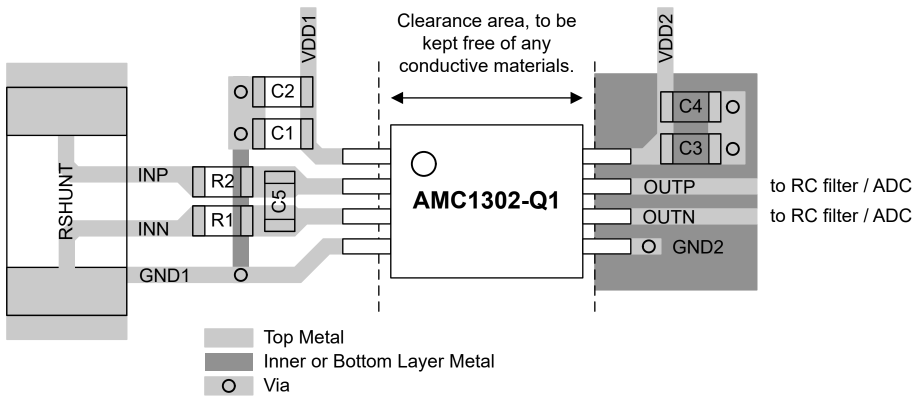


Figure 10-1. Recommended Layout of the AMC1302-Q1

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *TLVx313-Q1 Low-Power, Rail-to-Rail In/Out, 750-µV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1302QDWVQ1	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1302Q
AMC1302QDWVQ1.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1302Q
AMC1302QDWVQ1.B	Active	Production	SOIC (DWV) | 8	64 | TUBE	-	Call TI	Call TI	-40 to 125	
AMC1302QDWVRQ1	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1302Q
AMC1302QDWVRQ1.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1302Q
AMC1302QDWVRQ1.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AMC1302-Q1 :

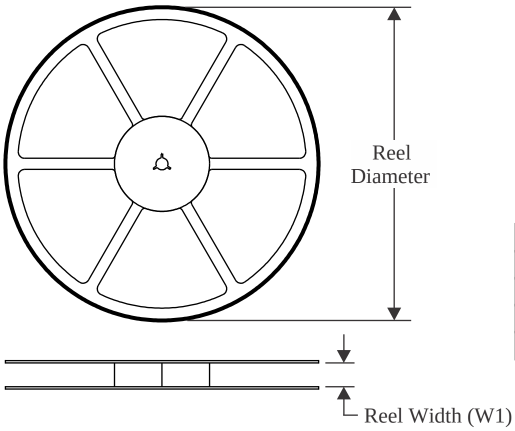
- Catalog : AMC1302

NOTE: Qualified Version Definitions:

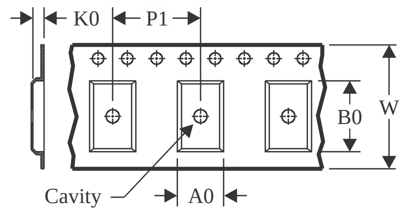
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

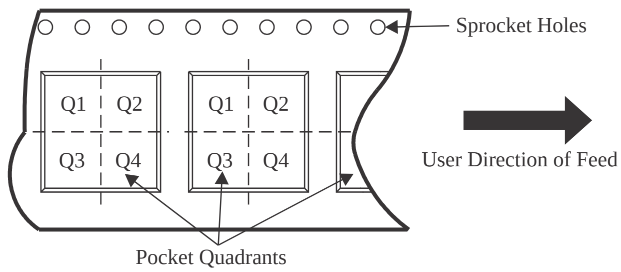


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

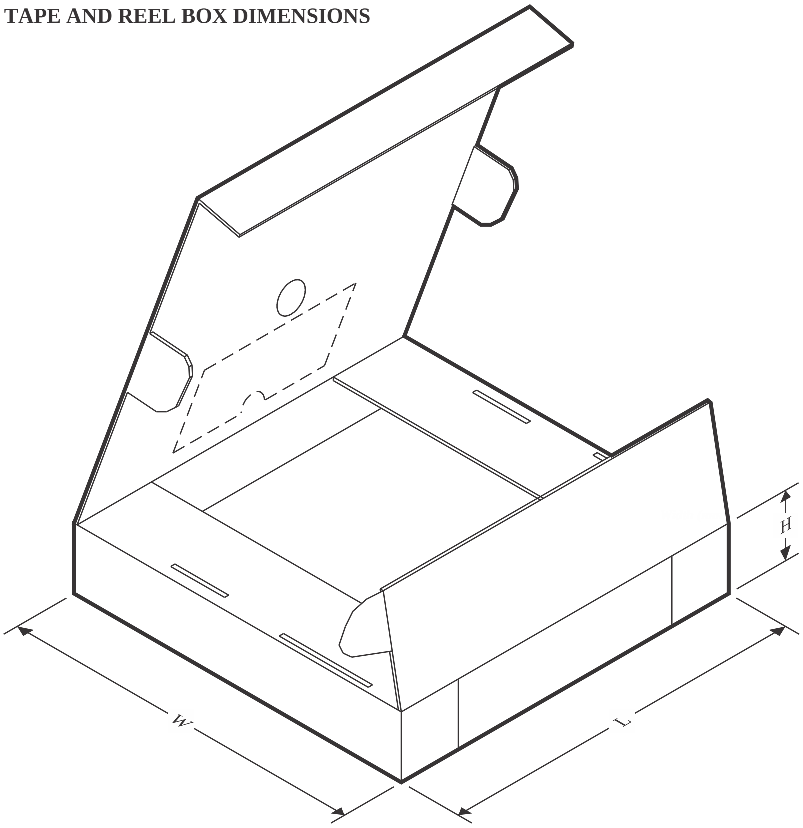
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1302QDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

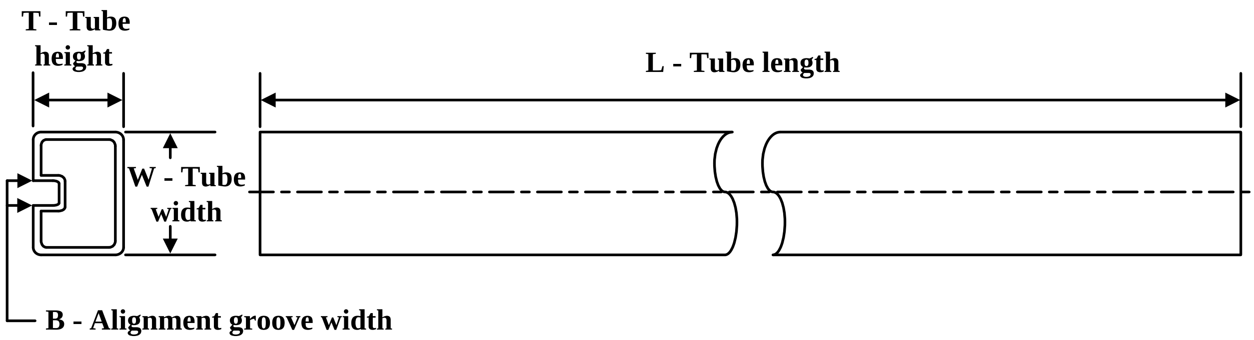
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

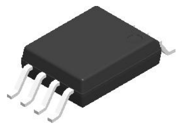
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1302QDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

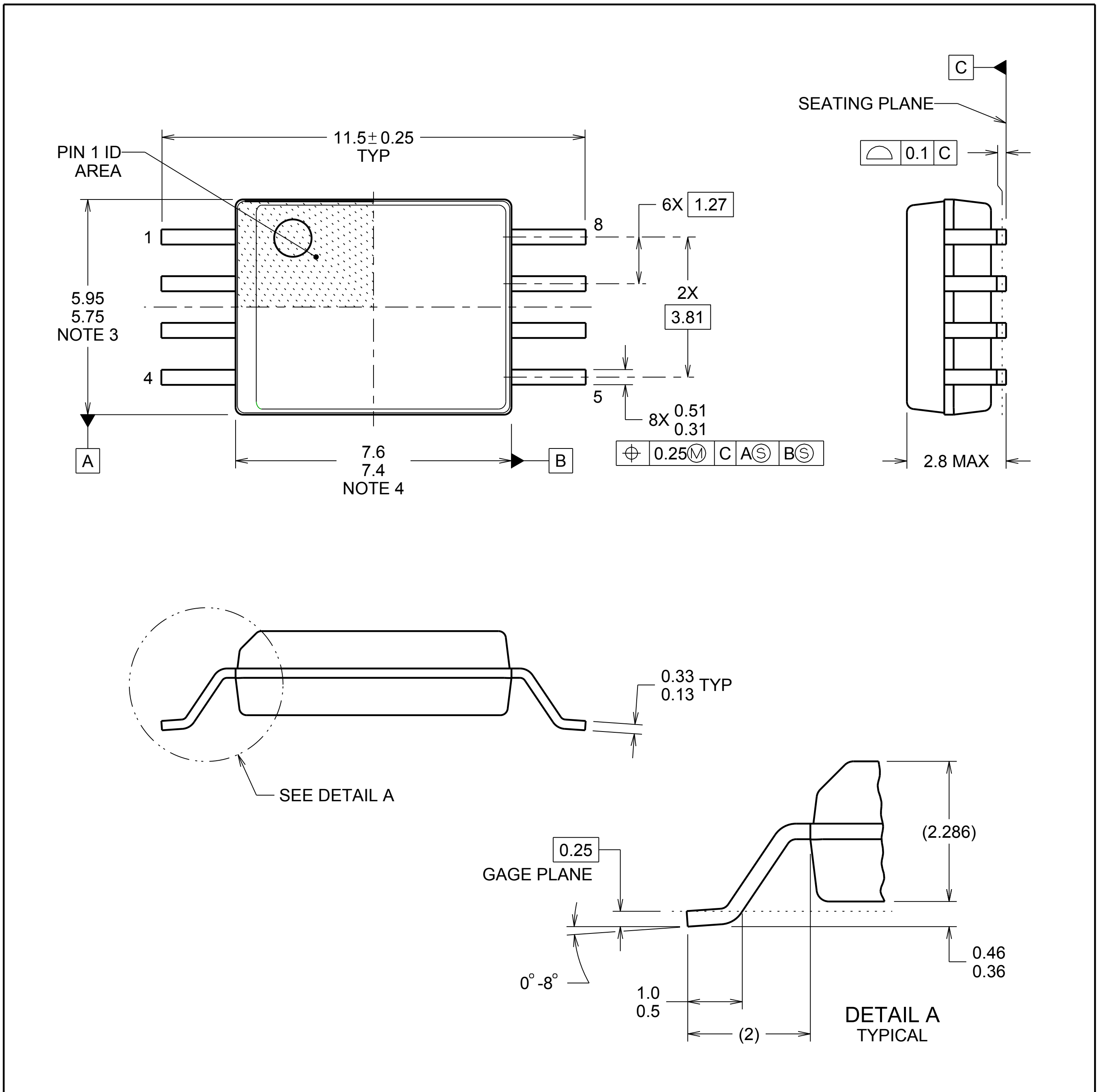
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1302QDWVQ1	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1302QDWVQ1.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6



DWV0008A

SOIC - 2.8 mm max height

SOIC



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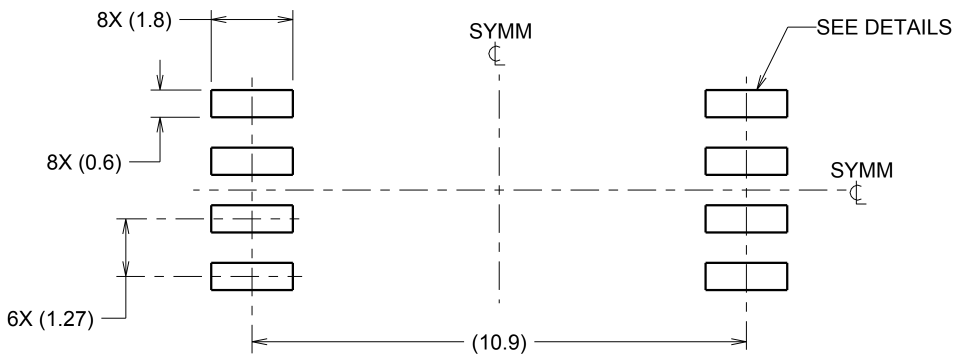
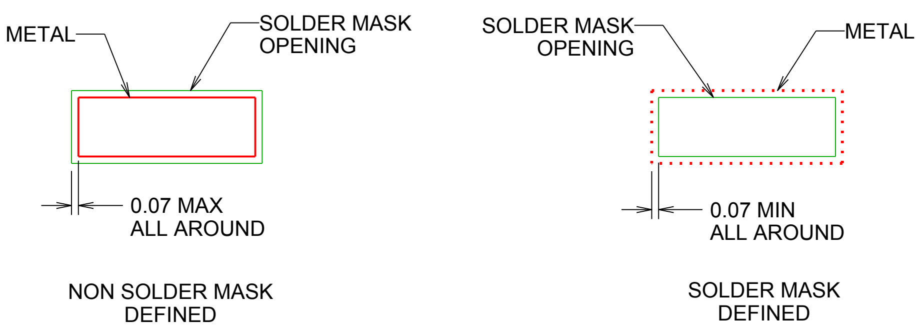
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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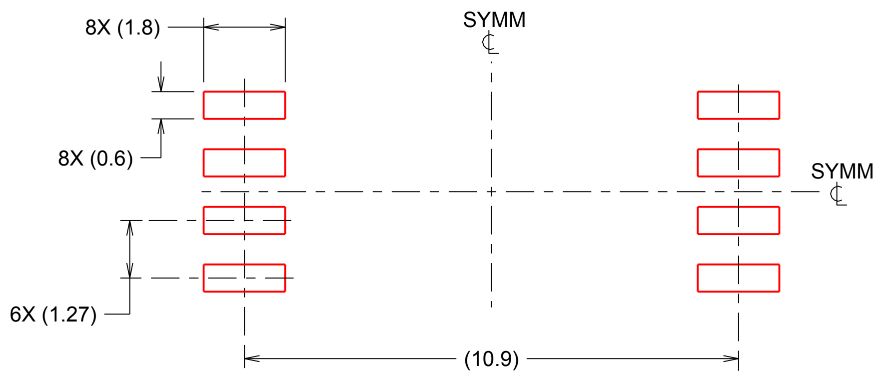
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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