

# AMC0106M25 Precision, $\pm 250\text{mV}$ Input, Functionally Isolated, Delta-Sigma Modulator With External Clock

## 1 Features

- Linear input voltage range:  $\pm 250\text{mV}$
- Supply voltage range:
  - High-side (AVDD): 3.0V to 5.5V
  - Low-side (DVDD): 2.7V to 5.5V
- Low DC errors:
  - Offset error:  $\pm 200\mu\text{V}$  (max)
  - Offset drift:  $\pm 2\mu\text{V}/^\circ\text{C}$  (max)
  - Gain error:  $\pm 0.2\%$  (max)
  - Gain drift:  $\pm 30\text{ppm}/^\circ\text{C}$  (max)
- High CMTI: 150V/ns (min)
- Missing high-side supply detection
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Functional isolation:
  - 200V<sub>RMS</sub>, 280V<sub>DC</sub> working voltage
  - 570V<sub>RMS</sub>, 800V<sub>DC</sub> transient overvoltage (60s)
- Fully specified over extended industrial temperature range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$

## 2 Applications

- [48V motor drives](#)
- [48V frequency inverters](#)
- [Analog input modules](#)
- [Power supplies](#)

## 3 Description

The AMC0106M25 is a precision, functionally isolated, delta-sigma modulator with a  $\pm 250\text{mV}$  input voltage range. The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier supports a working voltage up to 200V<sub>RMS</sub> / 280V<sub>DC</sub> and transient overvoltages up to 570V<sub>RMS</sub> / 800V<sub>DC</sub>.

With a small package size and low input voltage range, the AMC0106M25 is designed for high accuracy, isolated current sensing in space-constrained applications. The galvanic isolation barrier supports high common-mode transients and allows for isolating sensitive control circuitry from switching noise from the power stage.

The output bitstream of the AMC0106M25 is synchronized to an external clock. Combined with a sinc<sup>3</sup>, OSR 256 filter, the device achieves 16 bits of resolution with an 88dB dynamic range and a 78kSPS data rate.

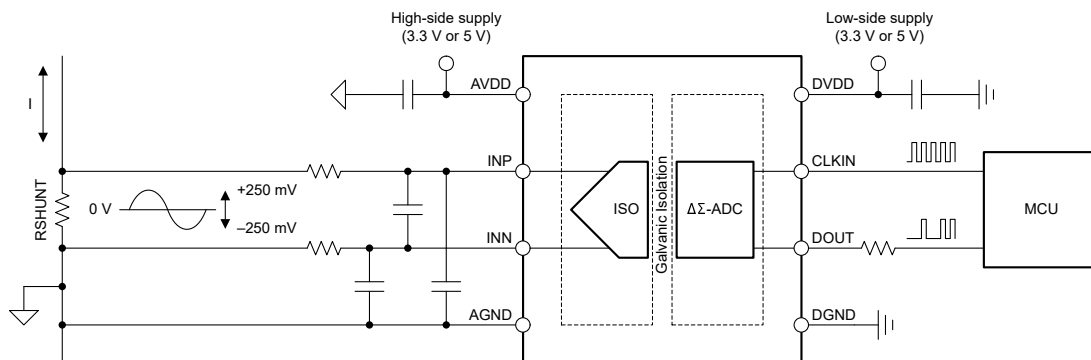
The AMC0106M25 is available in an 8-pin, 0.65mm pitch VSON package and is specified over the extended industrial temperature range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
AMC0106M25	DEN (VSON, 8)	3.5mm × 2.7mm

(1) For more information, see the [Mechanical, Packaging, and Orderable Information](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



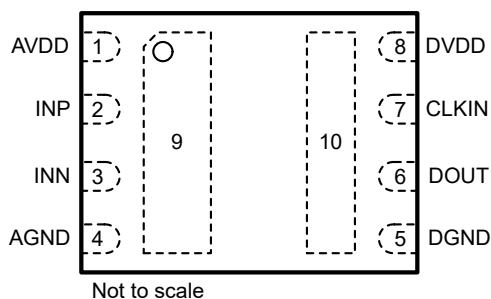
**Typical Application**



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## 4 Pin Configuration and Functions



**Figure 4-1. DEN Package, 8-Pin VSON (Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AVDD	High-side power	Analog (high-side) power supply. <sup>(1)</sup>
2	INP	Analog input	Noninverting analog input. <sup>(2)</sup>
3	INN	Analog input	Inverting analog input. <sup>(2)</sup>
4, 9 <sup>(3)</sup>	AGND	High-side ground	Analog (high-side) ground.
5, 10 <sup>(3)</sup>	DGND	Low-side ground	Digital (low-side) ground.
6	DOUT	Digital output	Modulator data output.
7	CLKIN	Digital input	Modulator clock input with internal pulldown resistor (typical value: 1.5MΩ).
8	DVDD	Low-side power	Digital (low-side) power supply. <sup>(1)</sup>

- (1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.  
 (2) See the [Input Filter Design](#) section for input filter design recommendations.  
 (3) Both pins are connected internally with a low-impedance path.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Power-supply voltage	High-side AVDD to AGND	−0.3	6.5	V
	Low-side DVDD to DGND	−0.3	6.5	
Analog input voltage	INP, INN to AGND	AGND − 4	AVDD + 0.5	V
Digital input voltage	CLKIN to DGND	DGND − 0.5	DVDD + 0.5	V
Digital output voltage	DOUT to DGND	DGND − 0.5	DVDD + 0.5	V
Transient isolation voltage <sup>(2)</sup>	AC voltage, t = 60s <sup>(3)</sup>		570	V <sub>RMS</sub>
	DC voltage, t = 60s <sup>(3)</sup>		800	V <sub>DC</sub>
Input current	Continuous, any pin except power-supply pins	−10	10	mA
Temperature	Junction, T <sub>J</sub>		150	°C
	Storage, T <sub>stg</sub>	−65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Common-mode from left-side (pins1-4) to right-side (pins5-8) of the package.
- (3) Cumulative.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	High-side power supply	AVDD to AGND	3	5.0	5.5	V
DVDD	Low-side power supply	DVDD to DGND	2.7	3.3	5.5	V
ANALOG INPUT						
V <sub>Clipping</sub>	Differential input voltage before clipping output	V <sub>IN</sub> = V <sub>INP</sub> – V <sub>INN</sub>	±320			mV
V <sub>FSR</sub>	Specified linear differential input voltage	V <sub>IN</sub> = V <sub>INP</sub> – V <sub>INN</sub>	–250	250		mV
V <sub>CM</sub>	Operating common-mode input voltage	(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to AGND	–0.16	1		V
C <sub>IN, EXT</sub>	Minimum external capacitance connected to the input	from INP to INN	10			nF
DIGITAL I/O						
V <sub>IO</sub>	Digital input/output voltage		0	DVDD		V
f <sub>CLKIN</sub>	Input clock frequency		5	20	21	MHz
t <sub>HIGH</sub>	Input clock high time		21.5	25	110	ns
t <sub>LOW</sub>	Input clock low time		21.5	25	110	ns
ISOLATION BARRIER						
V <sub>IOWM</sub>	Functional isolation working voltage <sup>(1)</sup>	AC voltage (sine wave)	200			V <sub>RMS</sub>
		DC voltage	280			V <sub>DC</sub>
TEMPERATURE RANGE						
T <sub>A</sub>	Specified ambient temperature		–40	125		°C

(1) Common-mode from left-side (pins1-4) to right-side (pins5-8) of the package.

## 5.4 Thermal Information (DEN Package)

THERMAL METRIC <sup>(1)</sup>		DEN (VSON)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	10.1	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	29.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	23.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Package Characteristics

PARAMETER		TEST CONDITIONS	VALUE	UNIT
<b>DEN PACKAGE</b>				
CLR	External clearance	Shortest pin-to-pin distance through air	$\geq 1$	mm
CPG	External creepage	Shortest pin-to-pin distance across the package surface	$\geq 1$	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	$\geq 600$	V
	Material group	According to IEC 60664-1	I	
$C_{IO}$	Capacitance, input to output <sup>(1)</sup>	$V_{IO} = 0.5 V_{PP}$ at 1MHz	$\cong 1.5$	pF
$R_{IO}$	Resistance, input to output <sup>(1)</sup>	$T_A = 25^\circ\text{C}$	$> 10^{12}$	$\Omega$

- (1) All pins on each side of the barrier are tied together, creating a two-pin device.

## 5.6 Electrical Characteristics

minimum and maximum specifications are at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $AVDD = 3.0\text{V}$  to  $5.5\text{V}$ ,  $DVDD = 2.7\text{V}$  to  $5.5\text{V}$ ,  $V_{INP} = -250\text{mV}$  to  $250\text{mV}$ ,  $V_{INN} = 0\text{V}$ , and sinc<sup>3</sup> filter with  $\text{OSR} = 256$  (unless otherwise noted); typical specifications are at  $T_A = 25^{\circ}\text{C}$ ,  $\text{CLKIN} = 20\text{MHz}$  with 50% duty cycle,  $AVDD = 5\text{V}$ , and  $DVDD = 3.3\text{V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C <sub>IN</sub>	Effective input sampling capacitance			1.8		pF
R <sub>IN</sub>	Input impedance	f <sub>CLK</sub> = 10MHz	50	55	60	kΩ
		f <sub>CLK</sub> = 20MHz	25	27.5	30	
I <sub>INP</sub>	Input current	V <sub>IN</sub> = (V <sub>INP</sub> – V <sub>INN</sub> ) = V <sub>FSR, MAX</sub> , f <sub>CLK</sub> = 10MHz		4.5		μA
		V <sub>IN</sub> = (V <sub>INP</sub> – V <sub>INN</sub> ) = V <sub>FSR, MAX</sub> , f <sub>CLK</sub> = 20MHz		9		
I <sub>INN</sub>	Input current	V <sub>IN</sub> = (V <sub>INP</sub> – V <sub>INN</sub> ) = V <sub>FSR, MAX</sub> , f <sub>CLK</sub> = 10MHz		–4.5		μA
		V <sub>IN</sub> = (V <sub>INP</sub> – V <sub>INN</sub> ) = V <sub>FSR, MAX</sub> , f <sub>CLK</sub> = 20MHz		–9		
CMTI	Common-mode transient immunity		150			V/ns
DC ACCURACY						
E <sub>O</sub>	Offset error	INP = INN = AGND, T <sub>A</sub> = 25°C	–200	30	200	μV
TCE <sub>O</sub>	Offset error temperature drift <sup>(3)</sup>		–2		2	μV/°C
E <sub>G</sub>	Gain error <sup>(1)</sup>	T <sub>A</sub> = 25°C	–0.2%	±0.03%	0.2%	
TCE <sub>G</sub>	Gain error temperature drift <sup>(4)</sup>		–30	±10	30	ppm/°C
INL	Integral nonlinearity <sup>(2)</sup>	Resolution: 16 bits	–4	±1	4	LSB
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
CMRR	Common-mode rejection ratio	INP = INN, f <sub>IN</sub> = 0Hz, V <sub>CM min</sub> ≤ V <sub>IN</sub> ≤ V <sub>CM max</sub>		–98		dB
		INP = INN, f <sub>IN</sub> from 0.1Hz to 10 kHz, V <sub>CM min</sub> ≤ V <sub>IN</sub> ≤ V <sub>CM max</sub>		–100		
PSRR	Power-supply rejection ratio	INP = INN = AGND, AVDD from 3.0V to 5.5V, DC		–87		dB
		INP = INN = AGND, AVDD from 3.0V to 5.5V, 10kHz / 100mV ripple		–87		
AC ACCURACY						
SNR	Signal-to-noise ratio	f <sub>IN</sub> = 1kHz		88		dB
SINAD	Signal-to-noise + distortion	f <sub>IN</sub> = 1kHz		88		dB
THD	Total harmonic distortion <sup>(5)</sup>	3V ≤ AVDD ≤ 5.5V, f <sub>IN</sub> = 1kHz, 5MHz ≤ f <sub>CLKIN</sub> ≤ 21MHz		–108	–86	dB
CMOS LOGIC WITH SCHMITT-TRIGGER						
I <sub>IN</sub>	Input current	DGND ≤ V <sub>IN</sub> ≤ DVDD	0		7	μA
C <sub>IN</sub>	Input capacitance			4		pF
V <sub>IH</sub>	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V <sub>IL</sub>	Low-level input voltage		–0.3		0.3 × DVDD	V
C <sub>LOAD</sub>	Output load capacitance			30		pF
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –4mA	DVDD – 0.4			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA			0.4	V

## 5.6 Electrical Characteristics (continued)

minimum and maximum specifications are at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $AVDD = 3.0\text{V}$  to  $5.5\text{V}$ ,  $DVDD = 2.7\text{V}$  to  $5.5\text{V}$ ,  $V_{\text{INP}} = -250\text{mV}$  to  $250\text{mV}$ ,  $V_{\text{INN}} = 0\text{V}$ , and sinc<sup>3</sup> filter with  $\text{OSR} = 256$  (unless otherwise noted); typical specifications are at  $T_A = 25^{\circ}\text{C}$ ,  $\text{CLKIN} = 20\text{MHz}$  with 50% duty cycle,  $AVDD = 5\text{V}$ , and  $DVDD = 3.3\text{V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
$I_{AVDD}$	High-side supply current			6.0	7.7	mA
$I_{DVDD}$	Low-side supply current	$C_{\text{LOAD}} = 15\text{pF}$		4.5	7.0	mA
$AVDD_{\text{UV}}$	High-side undervoltage detection threshold	AVDD rising	2.4	2.6	2.8	V
		AVDD falling	1.9	2.05	2.2	
$DVDD_{\text{UV}}$	Low-side undervoltage detection threshold	DVDD rising	2.3	2.5	2.7	V
		DVDD falling	1.9	2.05	2.2	

- (1) This parameter is input referred.
- (2) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
- (3) Offset error temperature drift is calculated using the box method, as described by the following equation:  

$$TCE_O = (E_{O,\text{MAX}} - E_{O,\text{MIN}}) / \text{TempRange}$$
 where  $E_{O,\text{MAX}}$  and  $E_{O,\text{MIN}}$  refer to the maximum and minimum  $E_O$  values measured within the temperature range ( $-40$  to  $125^{\circ}\text{C}$ ).
- (4) Gain error temperature drift is calculated using the box method, as described by the following equation:  

$$TCE_G (\text{ppm}) = ((E_{G,\text{MAX}} - E_{G,\text{MIN}}) / \text{TempRange}) \times 10^4$$
 where  $E_{G,\text{MAX}}$  and  $E_{G,\text{MIN}}$  refer to the maximum and minimum  $E_G$  values (in %) measured within the temperature range ( $-40$  to  $125^{\circ}\text{C}$ ).
- (5) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.



## 5.7 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>H</sub>	DOUT hold time after rising edge of CLKIN	C <sub>LOAD</sub> = 15pF	12			ns
t <sub>D</sub>	Rising edge of CLKIN to DOUT valid delay	C <sub>LOAD</sub> = 15pF			30	ns
t <sub>r</sub>	DOUT rise time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C <sub>LOAD</sub> = 15pF		2.5	6	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C <sub>LOAD</sub> = 15pF		3.2	6	
t <sub>f</sub>	DOUT fall time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C <sub>LOAD</sub> = 15pF		2.2	6	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C <sub>LOAD</sub> = 15pF		2.9	6	
t <sub>START</sub>	Device start-up time	AVDD step from 0 to 3.0V with DVDD ≥ 2.7V to bitstream valid, 0.1% settling		100		μs

## 5.8 Timing Diagrams

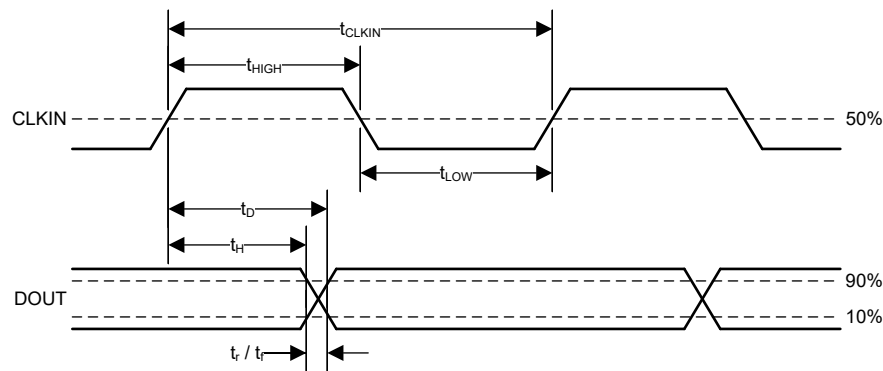


Figure 5-1. Digital Interface Timing

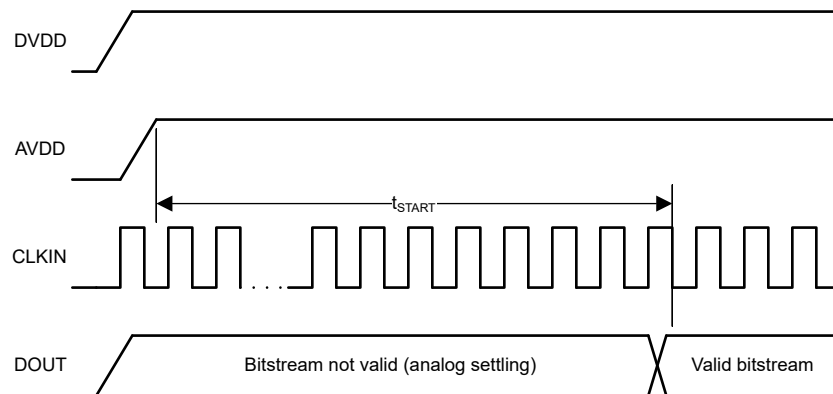


Figure 5-2. Device Start-Up Timing

## 5.9 Typical Characteristics

at  $AVDD = 5V$ ,  $DVDD = 3.3V$ ,  $V_{INP} = -250mV$  to  $+250mV$ ,  $INN = AGND$ ,  $f_{CLKIN} = 20MHz$  with 50% duty cycle, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)

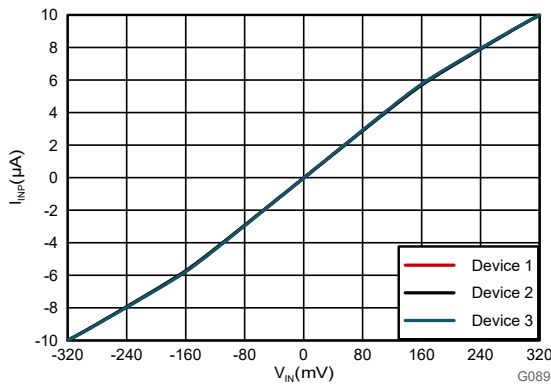


Figure 5-3. Input Current vs Input Voltage (INP Pin)

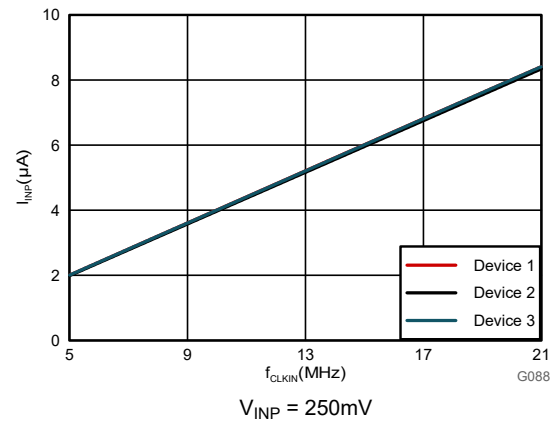
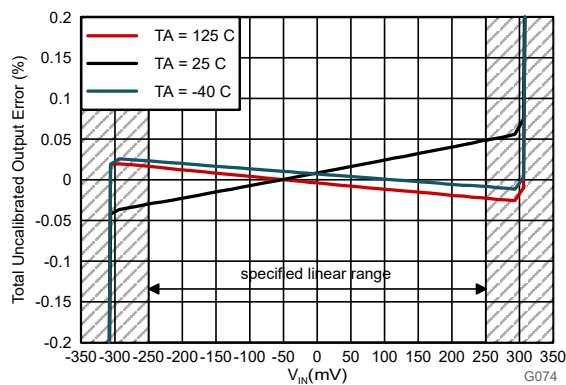


Figure 5-4. Input Current vs Clock Frequency (INP Pin)



Total uncalibrated output error (in %) is defined as:  

$$\left[ \left( \text{Output Code} / 2^{16} \right) - \left( (V_{IN} + 320mV) / 640mV \right) \right] \times 100$$
 where  $V_{IN} = (V_{INP} - V_{INN})$

Figure 5-5. Total Uncalibrated Output Error vs Input Voltage

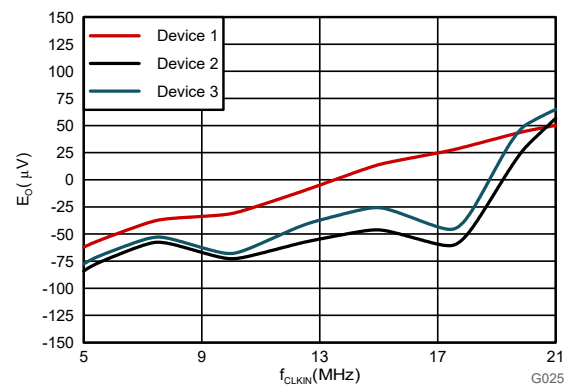


Figure 5-6. Offset Error vs Clock Frequency

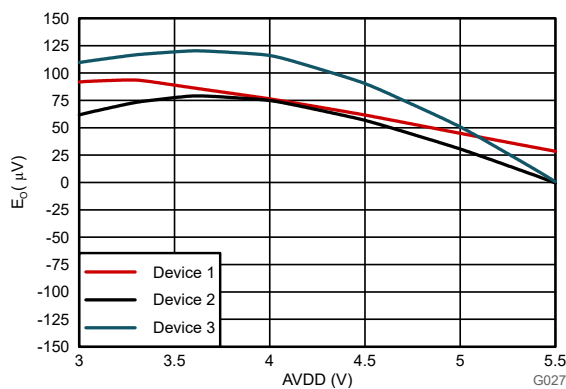


Figure 5-7. Offset Error vs High-Side Supply Voltage

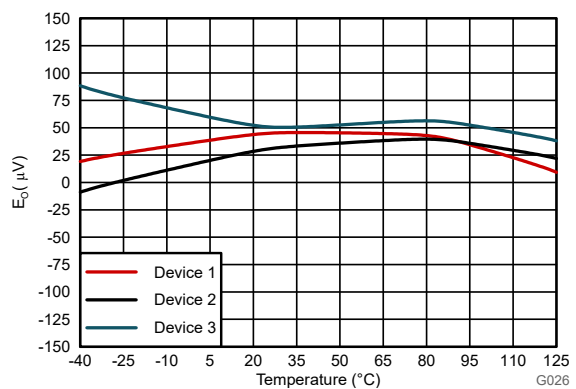
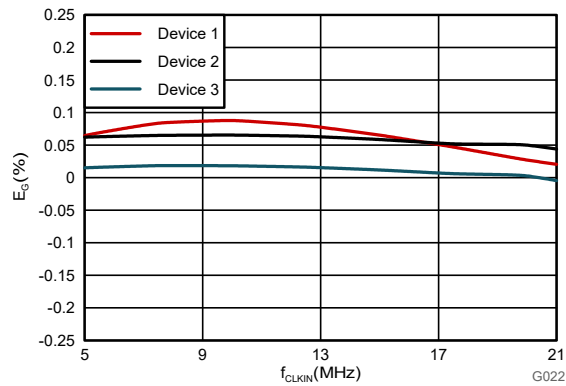


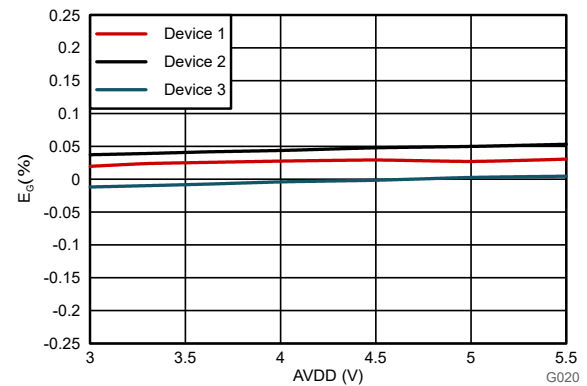
Figure 5-8. Offset Error vs Temperature

## 5.9 Typical Characteristics (continued)

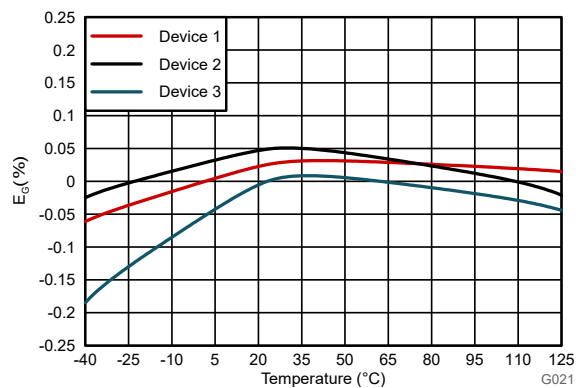
at  $AVDD = 5V$ ,  $DVDD = 3.3V$ ,  $V_{INP} = -250mV$  to  $+250mV$ ,  $INN = AGND$ ,  $f_{CLKIN} = 20MHz$  with 50% duty cycle, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)



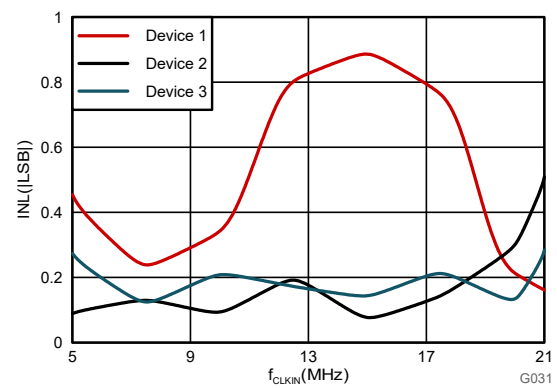
**Figure 5-9. Gain Error vs Clock Frequency**



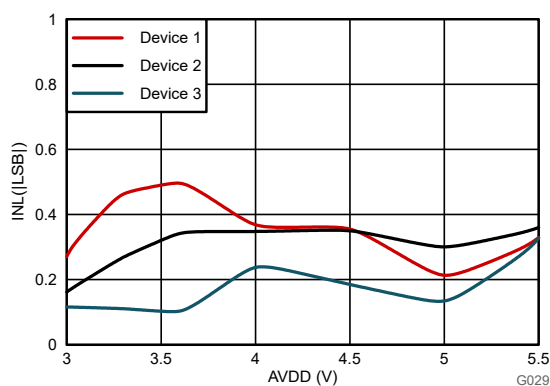
**Figure 5-10. Gain Error vs High-Side Supply Voltage**



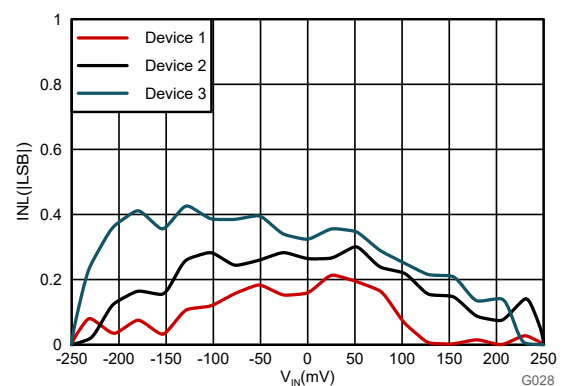
**Figure 5-11. Gain Error vs Temperature**



**Figure 5-12. Integral Nonlinearity vs Clock Frequency**



**Figure 5-13. Integral Nonlinearity vs High-Side Supply Voltage**



**Figure 5-14. Integral Nonlinearity vs Input Voltage**

## 5.9 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V,  $V_{INP} = -250\text{mV}$  to  $+250\text{mV}$ , INN = AGND,  $f_{CLKIN} = 20\text{MHz}$  with 50% duty cycle, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)

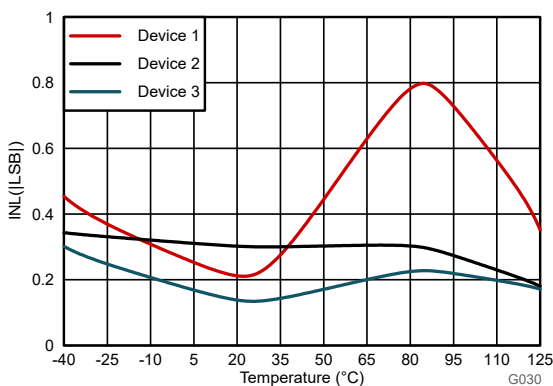


Figure 5-15. Integral Nonlinearity vs Temperature

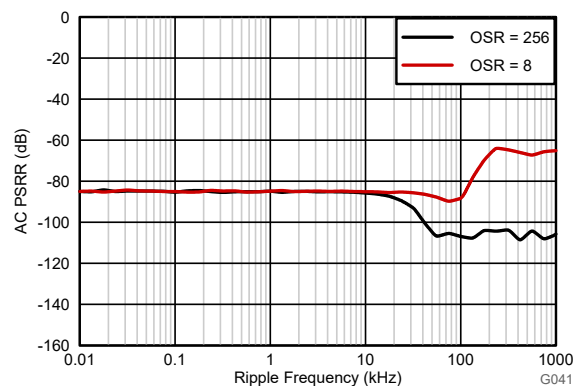


Figure 5-16. Power-Supply Rejection Ratio vs Ripple Frequency

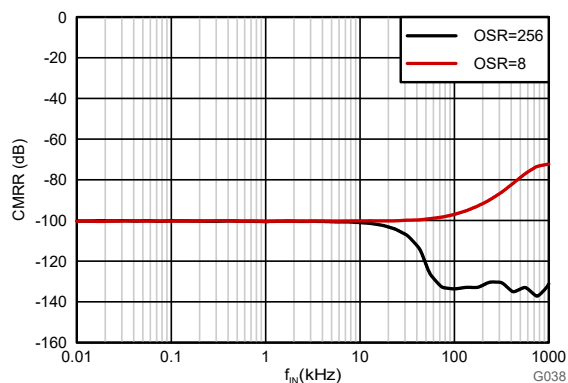


Figure 5-17. Common-Mode Rejection Ratio vs Input Signal Frequency

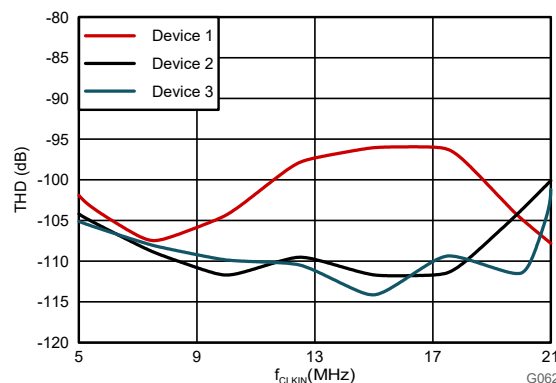


Figure 5-18. Total Harmonic Distortion vs Clock Frequency

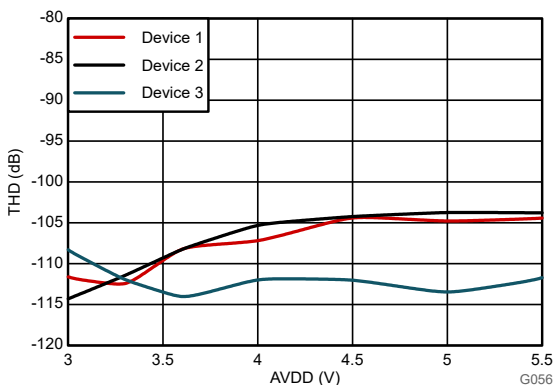


Figure 5-19. Total Harmonic Distortion vs High-Side Supply Voltage

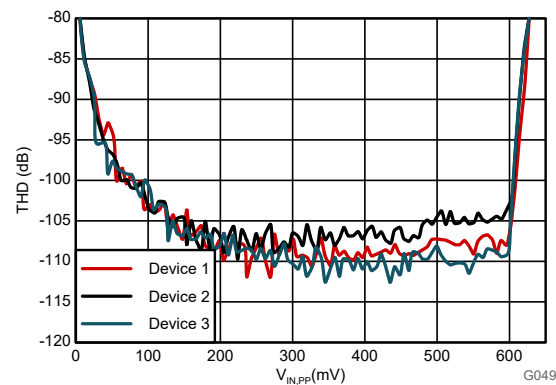
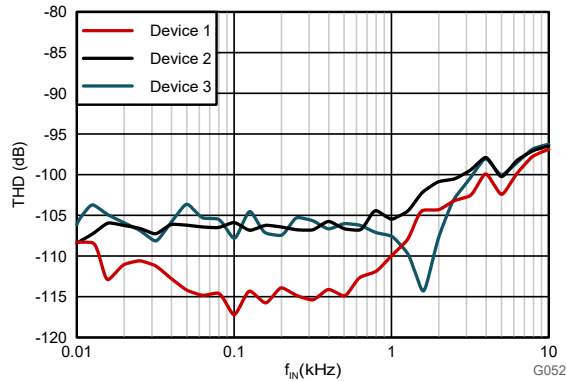


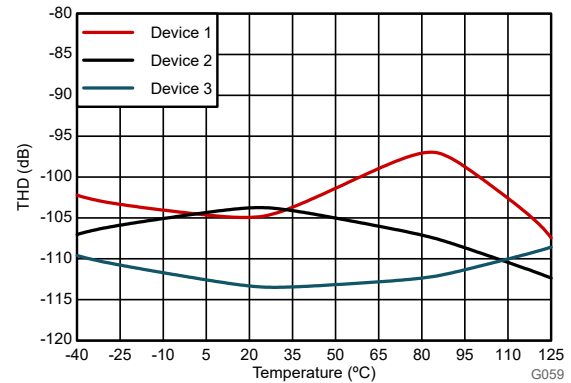
Figure 5-20. Total Harmonic Distortion vs Input Signal Amplitude

## 5.9 Typical Characteristics (continued)

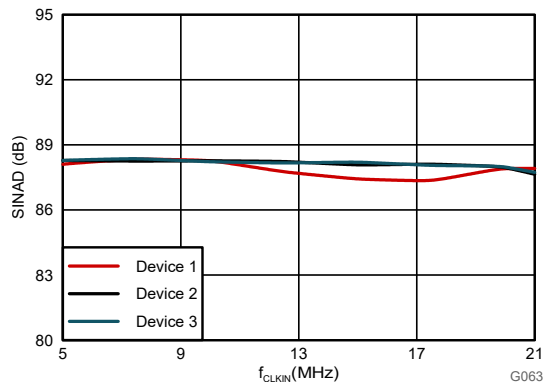
at AVDD = 5V, DVDD = 3.3V,  $V_{INP} = -250\text{mV}$  to  $+250\text{mV}$ , INN = AGND,  $f_{CLKIN} = 20\text{MHz}$  with 50% duty cycle, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)



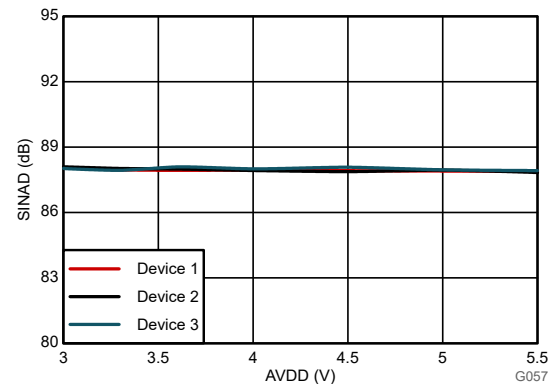
**Figure 5-21. Total Harmonic Distortion vs Input Signal Frequency**



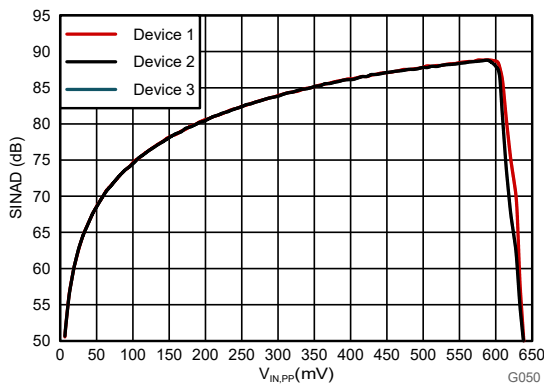
**Figure 5-22. Total Harmonic Distortion vs Temperature**



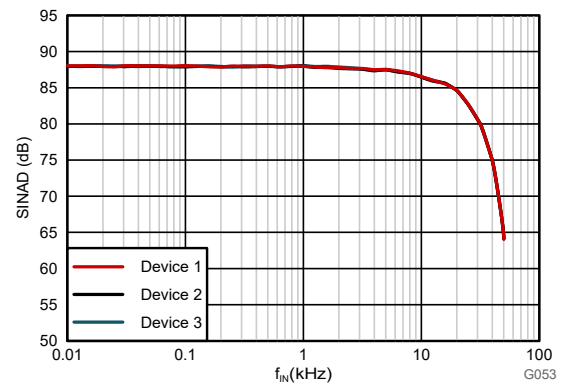
**Figure 5-23. Signal-to-Noise + Distortion vs Clock Frequency**



**Figure 5-24. Signal-to-Noise + Distortion vs High-Side Supply Voltage**



**Figure 5-25. Signal-to-Noise + Distortion vs Input Signal Amplitude**



**Figure 5-26. Signal-to-Noise + Distortion vs Input Signal Frequency**

## 5.9 Typical Characteristics (continued)

at  $AVDD = 5V$ ,  $DVDD = 3.3V$ ,  $V_{INP} = -250mV$  to  $+250mV$ ,  $INN = AGND$ ,  $f_{CLKIN} = 20MHz$  with 50% duty cycle, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)

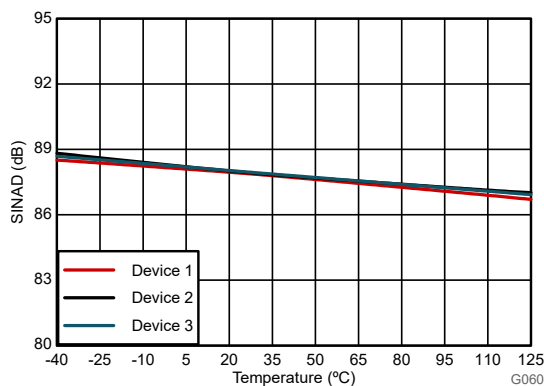


Figure 5-27. Signal-to-Noise + Distortion vs Temperature

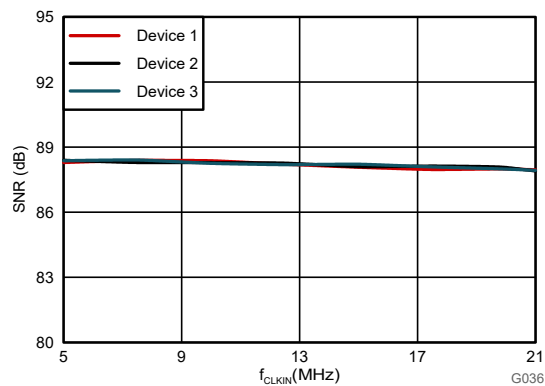


Figure 5-28. Signal-to-Noise Ratio vs Clock Frequency

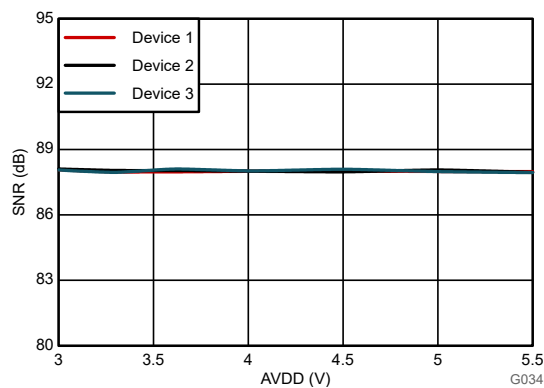


Figure 5-29. Signal-to-Noise Ratio vs High-Side Supply Voltage

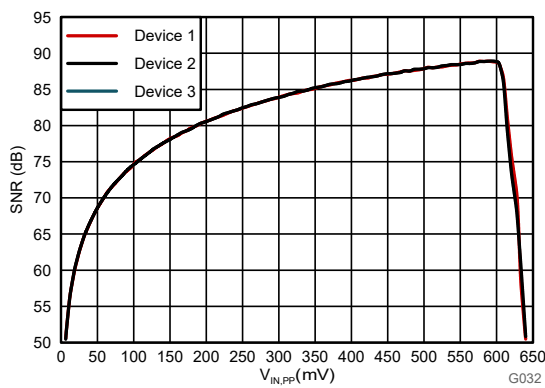


Figure 5-30. Signal-to-Noise Ratio vs Input Signal Amplitude

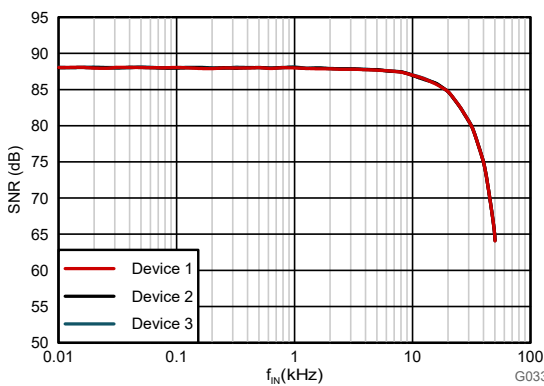


Figure 5-31. Signal-to-Noise Ratio vs Input Signal Frequency

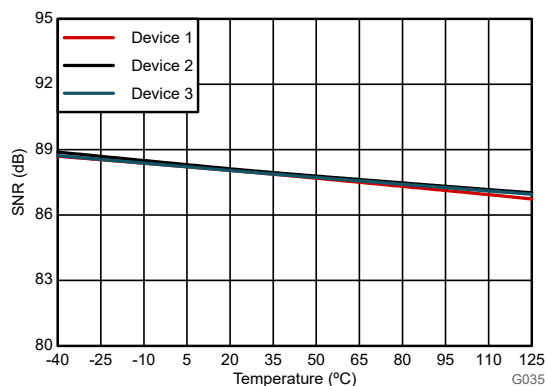


Figure 5-32. Signal-to-Noise Ratio vs Temperature

## 5.9 Typical Characteristics (continued)

at  $AVDD = 5V$ ,  $DVDD = 3.3V$ ,  $V_{INP} = -250mV$  to  $+250mV$ ,  $INN = AGND$ ,  $f_{CLKIN} = 20MHz$  with 50% duty cycle, and  $sinc^3$  filter with  $OSR = 256$  (unless otherwise noted)

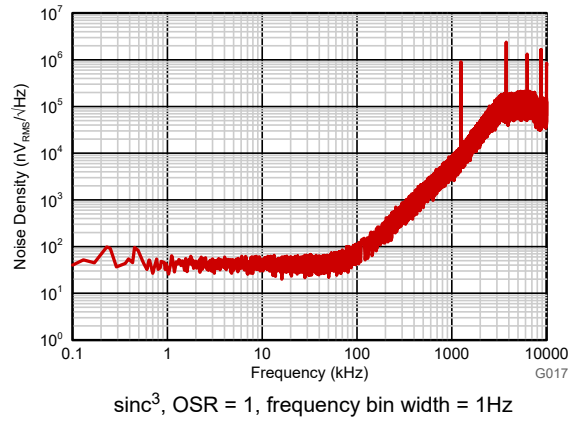


Figure 5-33. Noise Density With Both Inputs Shorted to HGND

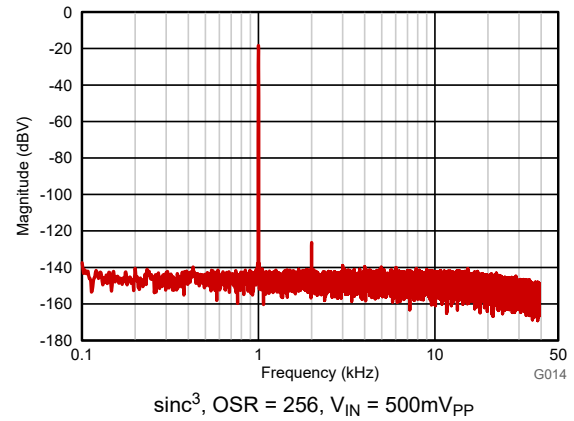


Figure 5-34. Frequency Spectrum With 1kHz Input Signal

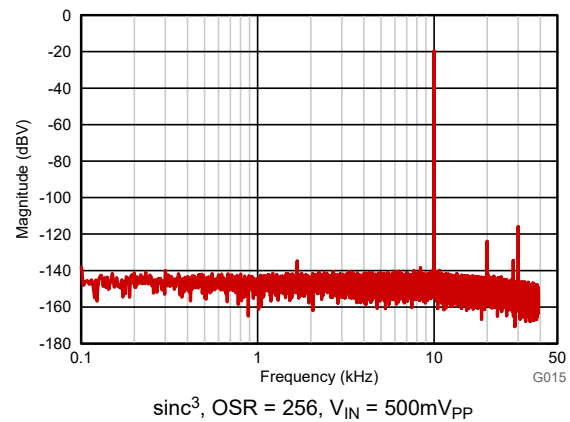


Figure 5-35. Frequency Spectrum With 10kHz Input Signal

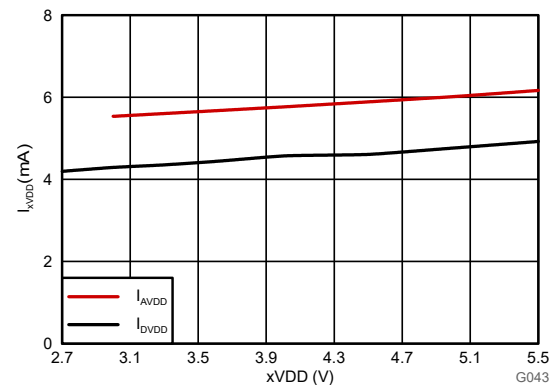


Figure 5-36. Supply Current vs Supply Voltage

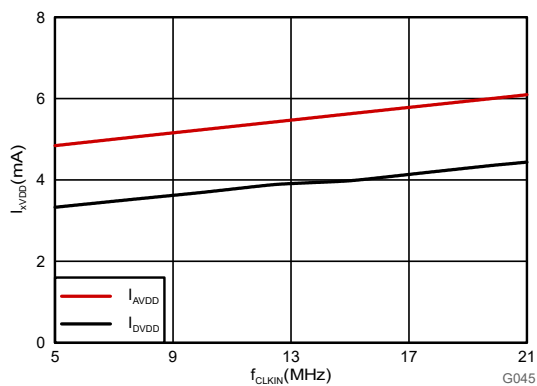


Figure 5-37. Supply Current vs Clock Frequency

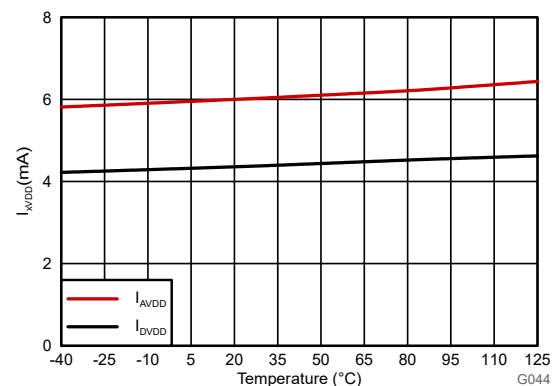


Figure 5-38. Supply Current vs Temperature

## 6 Detailed Description

### 6.1 Overview

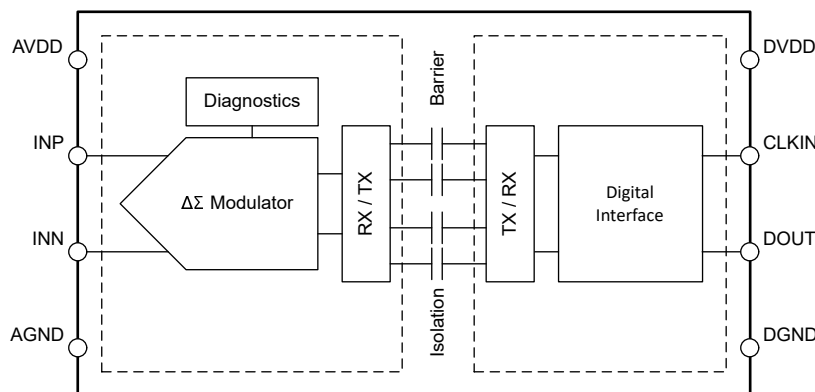
The AMC0106M25 is a single-channel, second-order, CMOS, delta-sigma ( $\Delta\Sigma$ ) modulator designed for high-resolution analog-to-digital conversions of AC signals. The differential analog input of the AMC0106M25 is implemented with a switched-capacitor circuit. The isolated output of the converter (DOUT) provides a stream of digital ones and zeros synchronous to the external clock applied to the CLKIN pin. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies. Therefore, use a digital low-pass filter, such as a sinc filter at the device output to increase overall performance. This filter also converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). Use a microcontroller ( $\mu$ C) or field-programmable gate array (FPGA) to implement the filter.

The overall performance (speed and resolution) depends on the selection of an appropriate oversampling ratio (OSR) and filter type. A higher OSR results in higher resolution while operating at a lower refresh rate. A lower OSR results in lower resolution, but provides data at a higher refresh rate. Multiple filters can run in parallel. For example, a low OSR filter for fast overcurrent detection and a high OSR filter for high resolution current measurement.

The silicon-dioxide ( $\text{SiO}_2$ ) based capacitive isolation barrier supports a high level of magnetic field immunity; see the [ISO72x Digital Isolator Magnetic-Field Immunity application note](#). The AMC0106M25 uses an on-off keying (OOK) modulation scheme to transmit data across the isolation barrier. This modulation, and the isolation barrier characteristics, result in high reliability in noisy environments and high common-mode transient immunity.

### 6.2 Functional Block Diagram



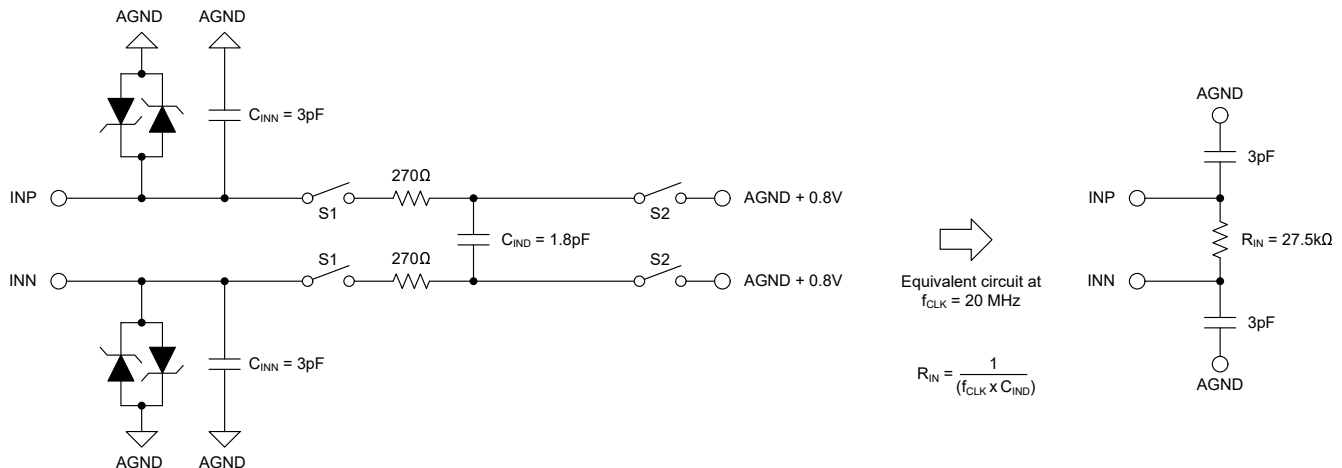


## 6.3 Feature Description

### 6.3.1 Analog Input

As shown in [Figure 6-1](#), the input of the AMC0106M25 is a fully differential, switched-capacitor circuit with a dynamic input impedance of 27.5kΩ at 20MHz.

The sampling capacitor is continuously charged and discharged with a frequency of  $f_{CLK}$ . With the S1 switches closed,  $C_{IND}$  charges to the voltage difference across  $V_{INP}$  and  $V_{INN}$ . For the discharge phase, both S1 switches open first and then both S2 switches close.  $C_{IND}$  discharges to approximately AGND + 0.8V during this phase.

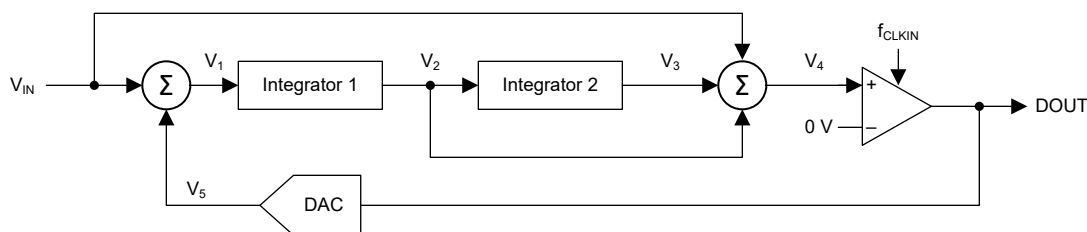


**Figure 6-1. Equivalent Input Circuit**

The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. There are two restrictions on the analog input signals (INP and INN). First, if the input voltage exceeds the input range specified in the [Absolute Maximum Ratings](#) table, limit the input current to the absolute maximum value because the electrostatic discharge (ESD) protection turns on. Second, the linearity and noise performance of the device are specified only when the differential analog input voltage remains within the specified  $V_{FSR}$  and  $V_{CM}$  ranges.  $V_{FSR}$  is the linear full-scale range and  $V_{CM}$  is the input common-mode voltage range.

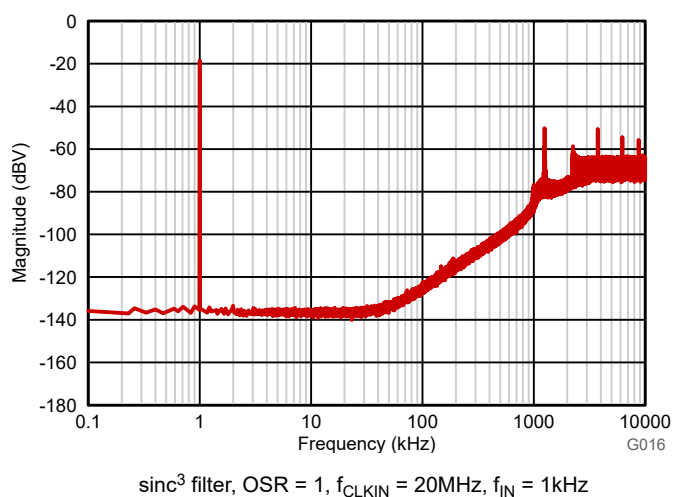
### 6.3.2 Modulator

Figure 6-2 conceptualizes the second-order, switched-capacitor, feed-forward  $\Delta\Sigma$  modulator implemented in the AMC0106M25. The output  $V_5$  of the 1-bit, digital-to-analog converter (DAC) is subtracted from the input voltage  $V_{IN} = (V_{INP} - V_{INN})$ . This subtraction provides an analog voltage  $V_1$  at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage. The result is an output voltage  $V_3$  that is summed with the input signal  $V_{IN}$  and the output of the first integrator  $V_2$ . Depending on the polarity of the resulting voltage  $V_4$ , the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage  $V_5$ . Thus, causing the integrators to progress in the opposite direction and forcing the integrator output value to track the average value of the input.



**Figure 6-2. Block Diagram of a Second-Order Modulator**

For reduced offset and offset drift, the integrators are chopper-stabilized with the chopping frequency set at  $f_{CLKIN}/16$ . Figure 6-3 shows the spur at 1.25MHz that is generated by the chopping frequency for a modulator clock of 20MHz.

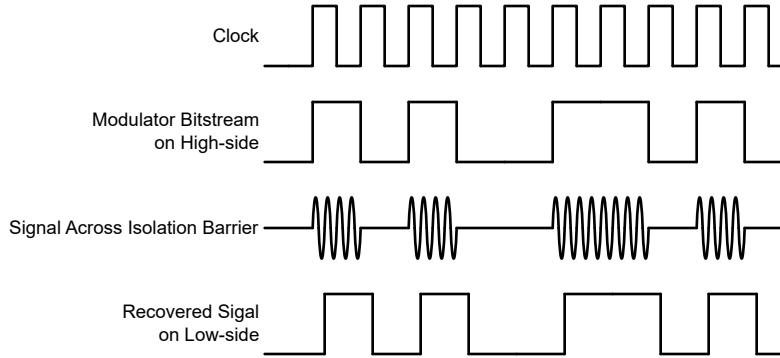


**Figure 6-3. Quantization Noise Shaping**

### 6.3.3 Isolation Channel Signal Transmission

The AMC0106M25 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO<sub>2</sub>-based isolation barrier. The transmit driver (TX) illustrated in the [Functional Block Diagram](#) transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital one. However, TX does not send a signal to represent a digital zero. The nominal frequency of the carrier used inside the AMC0106M25 is 480MHz.

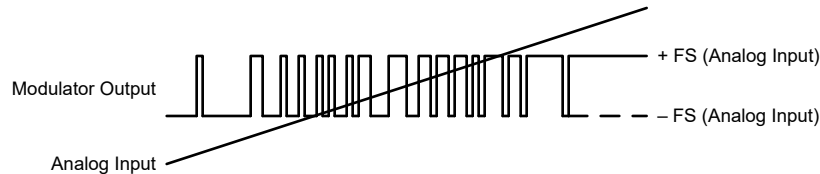
Figure 6-4 shows the concept of the on-off keying scheme.



**Figure 6-4. OOK-Based Modulation Scheme**

### 6.3.4 Digital Output

A differential input signal of 0V ideally produces a stream of ones and zeros that is high 50% of the time. A differential input of 250mV produces a stream of ones and zeros that is high 89.06% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58368. A differential input of 250mV produces a stream of ones and zeros that are high 10.94% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 7168. These input voltages are also the specified linear range of the AMC0106M25. If the input voltage value exceeds this range, the output of the modulator shows increasing nonlinear behavior as the quantization noise increases. The modulator output clips with a constant stream of zeros with an input  $\leq 320\text{mV}$  or with a constant stream of ones with an input  $\geq 320\text{mV}$ . In this case, however, the AMC0106M25 generates a single 1 or 0 every 128 clock cycles to indicate proper device function. A single 1 is generated if the input is at negative full-scale and a 0 is generated if the input is at positive full-scale. See the [Output Behavior in Case of a Full-Scale Input](#) section for more details. Figure 6-5 shows the input voltage versus the output modulator signal.



**Figure 6-5. Modulator Output vs Analog Input**

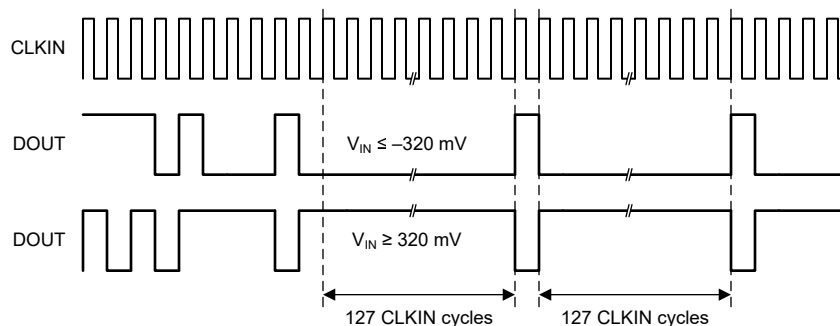
The density of ones in the output bitstream is calculated using [Equation 1](#) for any input voltage ( $V_{IN} = V_{INP} - V_{INN}$ ) value. Except for a full-scale input signal, as described in [Output Behavior in Case of a Full-Scale Input](#) section.

$$\rho = \frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

#### 6.3.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC0106M25, the device generates a single one or zero every 128 bits at DOUT. Figure 6-6 shows a timing diagram of this process. A single 1 or 0 is generated depending on

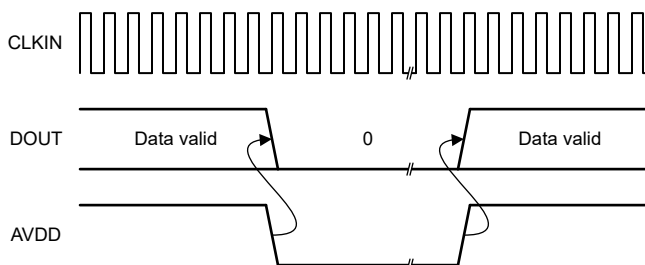
the actual polarity of the signal being sensed. A full-scale signal is defined when  $|V_{IN}| \geq |V_{Clipping}|$ . In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level.



**Figure 6-6. Full-Scale Output of the AMC0106M25**

#### 6.3.4.2 Output Behavior in Case of a Missing High-Side Supply

As shown in [Figure 6-7](#), the device provides a constant bitstream of logic 0's at the output if the high-side supply is missing. DOUT is permanently low when the high-side supply is missing. A one is not generated every 128 clock pulses, which differentiates this condition from a valid negative full-scale input. This feature helps identify high-side power-supply problems on the board.



**Figure 6-7. Output of the AMC0106M25 in Case of a Missing High-Side Supply**

## 6.4 Device Functional Modes

The AMC0106M25 operates in one of the following states:

- OFF-state: The low-side of the device (AVDD) is not supplied. The device is not responsive and DOUT is in high-impedance state. Internally, DOUT is clamped to DVDD and DGND by ESD protection diodes.
- Missing high-side supply: DVDD is supplied within the [Recommended Operating Conditions](#) but V<sub>AVDD</sub> is below the AVDD<sub>UV</sub> threshold. The device outputs a constant bitstream of logic 0's as described in the [Output Behavior in Case of a Missing High-Side Supply](#) section.
- Common-mode input violation: AVDD and DVDD are supplied within the respective recommended operating conditions. However, the common-mode input voltage  $V_{CM} = (V_{INP} + V_{INN}) / 2$  is outside the recommended operating conditions. The device outputs invalid data, independent of the differential input voltage V<sub>IN</sub>.
- Differential input voltage range violation (full-scale input): V<sub>AVDD</sub>, V<sub>DVDD</sub>, and V<sub>CM</sub> are within the recommended operating conditions. However, the differential input voltage  $V_{IN} = (V_{INP} - V_{INN})$  exceeds the clipping voltage ( $|V_{IN}| > |V_{Clipping}|$ ). The device outputs a fixed pattern as described in the [Output Behavior in Case of a Missing High-Side Supply](#) section.
- Normal operation: V<sub>AVDD</sub>, V<sub>DVDD</sub>, V<sub>CM</sub>, and V<sub>IN</sub> are within the recommended operating conditions. The device outputs a digital bitstream as explained in the [Digital Output](#) section.

**Table 6-1. Device Operational Modes**

OPERATING CONDITION	V <sub>DVDD</sub>	V <sub>AVDD</sub>	V <sub>CM</sub> (V <sub>INP</sub> + V <sub>INN</sub> ) / 2	V <sub>IN</sub> (V <sub>INP</sub> – V <sub>INN</sub> )	DEVICE RESPONSE
OFF	V <sub>DVDD</sub> < DVDD <sub>UV</sub>	Don't care	Don't care	Don't care	DOUT is in Hi-Z state. DOUT is clamped to DVDD and DGND by ESD protection diodes.
Missing high-side supply	Valid <sup>(1)</sup>	V <sub>AVDD</sub> < AVDD <sub>UV</sub>	Don't care	Don't care	DOUT is constantly low
Common-mode input voltage range violation	Valid <sup>(1)</sup>	Valid <sup>(1)</sup>	V <sub>CM</sub> < V <sub>CM, MIN</sub> or V <sub>CM</sub> > V <sub>CM, MAX</sub>	Don't care	Device outputs invalid data
Differential input voltage range violation	Valid <sup>(1)</sup>	Valid <sup>(1)</sup>	Valid <sup>(1)</sup>	$ V_{IN}  > V_{Clipping}$	Device outputs a single 1 or a single 0 every 128 <sup>th</sup> clock cycle
Normal operation	Valid <sup>(1)</sup>	Valid <sup>(1)</sup>	Valid <sup>(1)</sup>	Valid <sup>(1)</sup>	Normal Operation

(1) Valid means within recommended operating conditions.

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

Isolated modulators are widely used in application where a high-voltage domain is galvanically isolated from a low-voltage domain for safety or functional reasons. A typical application is the sensing of the phase currents in a frequency inverter.

### 7.2 Typical Application

Figure 7-1 shows a simplified schematic of a full-bridge motor drive that uses an AMC0106M25 to sense the motor current. The current flowing through an external shunt resistor RSHUNT produces a voltage drop that is sensed by the AMC0106M25. The AMC0106M25 digitizes the analog input signal on the high-side and transfers the data across the isolation barrier to the low-side. The device then outputs the digital bitstream on the DOUT pin that is synchronized to the clock applied to the CLKIN pin. The digital bitstream is processed by a low-pass digital filter in a microcontroller unit (MCU) or FPGA.

The 48V DC link voltage in this application is sensed by an [AMC0136](#) isolated modulator.

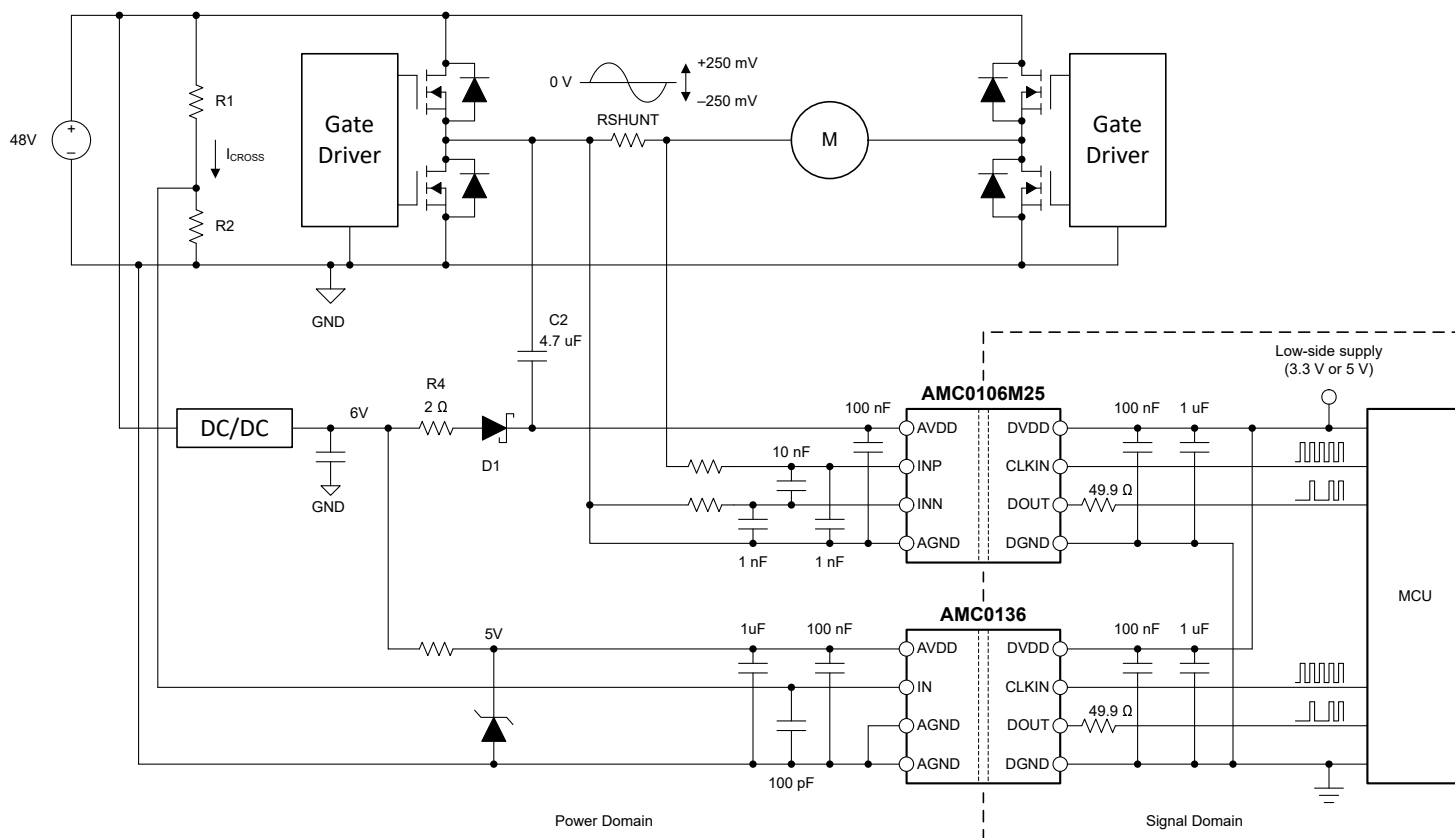


Figure 7-1. Using the AMC0106M25 for Current Sensing in a Full-Bridge 48V Motor Driver Design

The high-side power supply (AVDD) is generated from a bootstrap circuit (R4, D1, C2). The low-side supply is shared with circuitry in the signal domain. Use the optional 49.9Ω resistor on the DOUT pin for line termination to improve signal integrity on the receiving end.

The galvanic isolation barrier and high common-mode transient immunity (CMTI) of the AMC0106M25 provide reliable and accurate operation even in high-noise environments.

### 7.2.1 Design Requirements

Table 7-1 lists the parameters for this typical application.

**Table 7-1. Design Requirements**

PARAMETER	VALUE
System voltage, power-stage	48V
Bootstrap supply voltage (V <sub>BS</sub> )	6V
Maximum ripple voltage on AVDD supply (V <sub>RIPPLE</sub> )	200mV
PWM frequency	16kHz
PWM duty cycle range	5% to 95%
Linear current sensing range	±5A

### 7.2.2 Detailed Design Procedure

In Figure 7-1, the high-side power supply (AVDD) is generated from a bootstrap circuit (R4, D1, C2).

The high-side ground reference (AGND) is derived from the end of the shunt resistor connected to the negative input of the AMC0106M25 (INN). For a four-terminal shunt, connect the device inputs to the inner leads of the shunt and connect AGND to the outer leads. To minimize offset and improve accuracy, route the ground connection as a separate trace. Connect AGND directly to the shunt resistor rather than shorting AGND to INN at the input to the device. See the [Layout](#) section for more details.

#### 7.2.2.1 Shunt Resistor Sizing

The shunt resistor (RSHUNT) value is determined by the device linear input voltage range (±250mV) and the desired linear current sensing range of ±5A. RSHUNT is calculated as  $250\text{mV} / 5\text{A} = 50\text{m}\Omega$ . The peak power dissipated in the shunt resistor is  $\text{RSHUNT} \times I_{\text{PEAK}}^2 = 50\text{m}\Omega \times (5\text{A})^2 = 1.25\text{W}$ . For a linear response, operate the shunt resistor at no more than 2/3 of the rated power. Therefore, a shunt resistor with a nominal power rating of approximately 1.8W is selected.

Select a lower shunt resistor value if transient overcurrents are expected in the system that exceed the linear input voltage range of the AMC0106M25. However, if reduced linearity and lower resolution is acceptable for the overcurrent range, allow the voltage drop across the shunt to exceed the linear input voltage range up to the clipping voltage of the AMC0106M25. In any case, make sure the voltage drop caused by the maximum overcurrent does not exceed the input voltage that causes a clipping output. That is, make sure  $|V_{\text{SHUNT}}| \leq |V_{\text{Clipping}}|$ .

### 7.2.2.2 Input Filter Design

Place a differential RC filter (R1, R2, C5) in front of the isolated modulator to improve signal-to-noise performance of the signal path. Input noise with a frequency close to the  $\Delta\Sigma$  modulator sampling frequency (typically 20MHz) is folded back into the low-frequency range by the modulator. The purpose of the RC filter at the input is to attenuate high-frequency noise below the desired noise level of the measurement. Design the input filter such that:

- The filter capacitance (C5) is a minimum of 10nF
- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency ( $f_{CLKIN}$ ) of the  $\Delta\Sigma$  modulator
- The dynamic input bias current does not generate significant voltage drop across the DC impedances (R1, R2) of the input filter
- The impedances measured from the analog inputs are equal (R1 equals R2)

Capacitors C6 and C7 are optional and improve common-mode rejection at high frequencies (>1MHz). For best performance, make sure C6 matches the value of C7 and that both capacitors are 10 to 20 times lower in value than C5. NP0-type capacitors offer low temperature drift and low voltage coefficients, and are preferred for common-mode filtering. For most applications, the structure shown in Figure 7-2 achieves excellent performance.

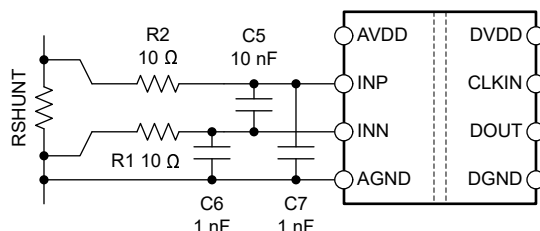


Figure 7-2. Input Filter

### 7.2.2.3 Bitstream Filtering

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). Equation 2 shows a sinc<sup>3</sup>-type filter, which is a very simple filter built with minimal effort and hardware.

$$H(z) = \left( \frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All characterization in this document is done with a sinc<sup>3</sup> filter with an oversampling ratio (OSR) of 256 and a 16-bit output word width.

The [Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications application note](#) discusses an example code. Use this example code for implementing a sinc<sup>3</sup> filter in an FPGA. This application note is available for download at [www.ti.com](http://www.ti.com).

For modulator output bitstream filtering, use a device from TI's C2000 or Sitara microcontroller families. These families support multichannel dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel. One path provides high-accuracy results for the control loop and the other provides a fast-response path for overcurrent detection.

A [delta sigma modulator filter calculator](#) is available for download at [www.ti.com](http://www.ti.com) that aids in filter design and correct OSR and filter order selection. This calculator helps achieve the desired output resolution and filter response time.



#### 7.2.2.4 Designing the Bootstrap Supply

The bootstrap capacitor (C2, [Figure 7-1](#)) is charged during the PWM on-time of the low-side FET of the left-hand-side half bridge. During the PWM off-time, C2 rises with the switch pin voltage and serves as the AMC0106M25 power supply. R4 serves as a current-limiting resistor during the charging phase, and D1 prevents reverse current from flowing back to the bootstrap supply during the discharge phase.

The voltage C2 charges up to during the PWM on-time depends on the values of the bootstrap supply and the current limiting resistor R2. Additionally, this voltage depends on the PWM duty cycle and the forward voltage of the diode D1 ( $V_{F, D1}$ ).

The voltage C2 discharges to during the PWM off-time depends on the reverse recovery time of D1. Additionally, this voltage depends on the PWM duty cycle and the current draw of the AMC0106M25 ( $I_{AVDD}$ ). To minimize switching losses, select a fast switching diode with high forward current capability.

Make sure C2 is sized to support the maximum  $I_{AVDD}$  current for the duration of the maximum PWM off-time. During this time, make sure C2 does not discharge below the minimum recommended AVDD voltage of 3V. Lower capacitance values allow faster charging and therefore support lower PWM duty cycles. However, lower values also generate more voltage ripple and limit the maximum PWM off time. In this example, a ripple voltage ( $V_{RIPPLE}$ ) of less than 200mV is targeted. The maximum PWM off-time is  $95\% \times (1 / f_{PWM}) = 0.95 \times 62.5\mu s$ , which is approximately 60μs.  $I_{AVDD, MAX}$  is specified as 8.8mA. The minimum capacitance value is calculated as  $C_{2, MIN} = I_{AVDD, MAX} \times t_{PWM-OFF, MAX} / V_{RIPPLE} = 8.8mA \times 60\mu s / 200mV = 2.6\mu F$ . A 4.7μF capacitor is selected to allow for component tolerances and adds margin to the design.

Make sure the bootstrap circuit supports recharging C2 within the minimum PWM on-time of  $5\% \times (1 / f_{PWM}) = 0.05 \times 62.5\mu s$ , or approximately 3.1μs. The average charging current during this time is  $C2 \times V_{RIPPLE} / t_{PWM-ON, MIN} = 4.7\mu F \times 200mV / 3.1\mu s$ , which is approximately 300mA. This current is the minimum forward current that diode D1 has to support. The maximum allowable voltage drop across diode D1 and current limiting resistor R4 is determined by the minimum capacitor voltage and the  $V_{BS}$  value. The minimum capacitor voltage is 3V and equivalent to  $AVDD_{MIN}$ .  $V_{BS}$  is the bootstrap supply voltage and is equal to 6V. Assume a diode forward voltage of 1V is used. Make sure R4 is  $< (V_{BS} - V_{F, D1} - V_{C2, MIN}) / I_{CHARGE} = (6V - 1V - 3V) / 300mA = 6\Omega$ . A 2Ω resistor is selected to provide margin to the design.

### 7.2.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and  $\Delta\Sigma$  modulators. Figure 7-3 shows the ENOB of the AMC0106M25 with different oversampling ratios.

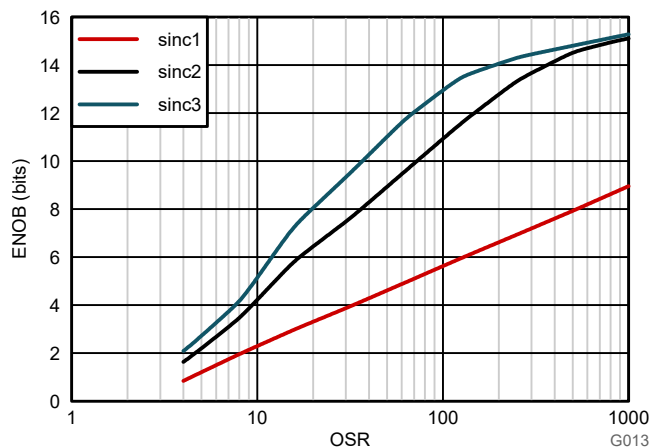


Figure 7-3. Measured Effective Number of Bits vs Oversampling Ratio

### 7.3 Best Design Practices

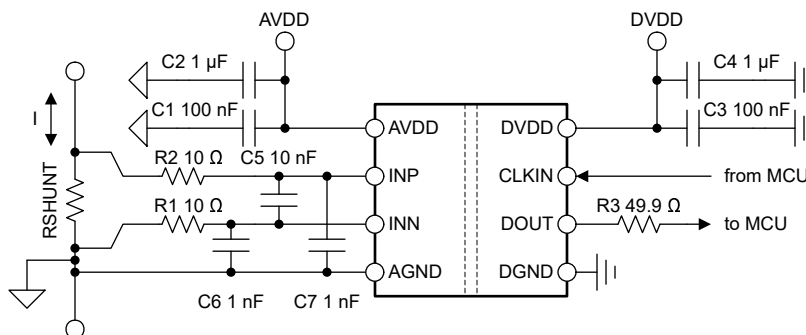
Place a minimum 10nF capacitor at the device input (from INP to INN). This capacitor helps avoid voltage droop at the input during the sampling period of the switched-capacitor input stage.

Do not leave the inputs of the AMC0106M25 unconnected (floating) when the device is powered up. If either modulator input is left floating, the output bitstream is not valid.

Connect the high-side ground (AGND) to INN, either by a hard short or through a resistive path. A DC current path between INN and AGND is required to define the input common-mode voltage. Do not exceed the input common-mode range, as specified in the [Recommended Operating Conditions](#) table. For best accuracy, route the ground connection as a separate trace that connects directly to the sense resistor. Do not short AGND to INN directly at the device input. See the [Layout](#) section for more details.

## 7.4 Power Supply Recommendations

The AMC0106M25 does not require any specific power-up sequencing. The high-side power supply (AVDD) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1 $\mu$ F capacitor (C2). The low-side power supply (DVDD) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1 $\mu$ F capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 7-4 shows a decoupling diagram for the AMC0106M25.



**Figure 7-4. Decoupling of the AMC0106M25**

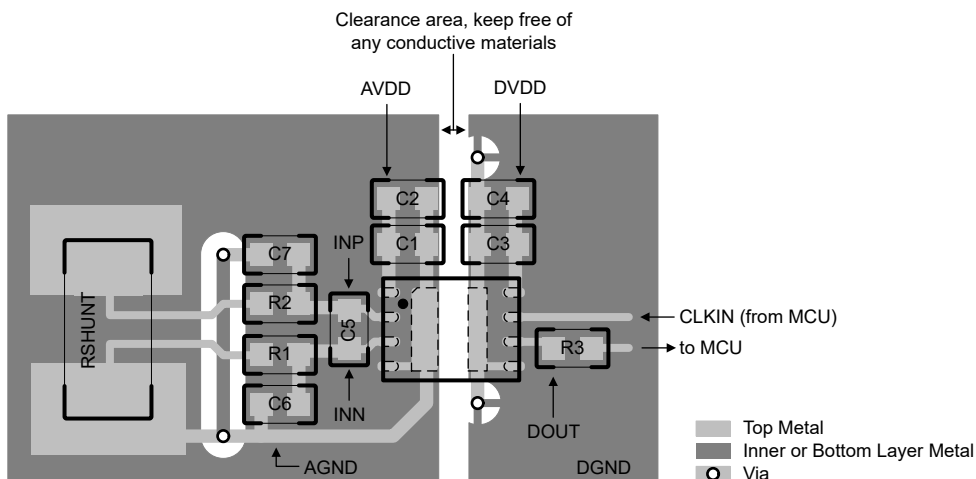
Capacitors have to provide adequate effective capacitance under the applicable DC bias conditions that are experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Take this factor into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

## 7.5 Layout

### 7.5.1 Layout Guidelines

The [Layout Example](#) section provides a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC0106M25 supply pins). This section also depicts the placement of other components required by the device. For best performance, place the sense resistor close to the device input pins (INN and INP).

### 7.5.2 Layout Example



**Figure 7-5. Recommended Layout of the AMC0106M25**

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Isolation Glossary application note](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application note](#)
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity application note](#)
- Texas Instruments, [Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications application note](#)
- Texas Instruments, [Delta Sigma Modulator Filter Calculator design tool](#)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.4 Trademarks

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### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2024) to Revision A (July 2025)	Page
• Changed document status from <i>Advance Information</i> to <i>Production Data</i> .....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">AMC0106M25DENR</a>	Active	Production	VSON (DEN)   8	5000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0106M2
<a href="#">PAMC0106M25DENR</a>	Active	Preproduction	VSON (DEN)   8	5000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
PAMC0106M25DENR.A	Active	Preproduction	VSON (DEN)   8	5000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
PAMC0106M25DENR.B	Active	Preproduction	VSON (DEN)   8	5000   LARGE T&R	-	Call TI	Call TI	-40 to 125	

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

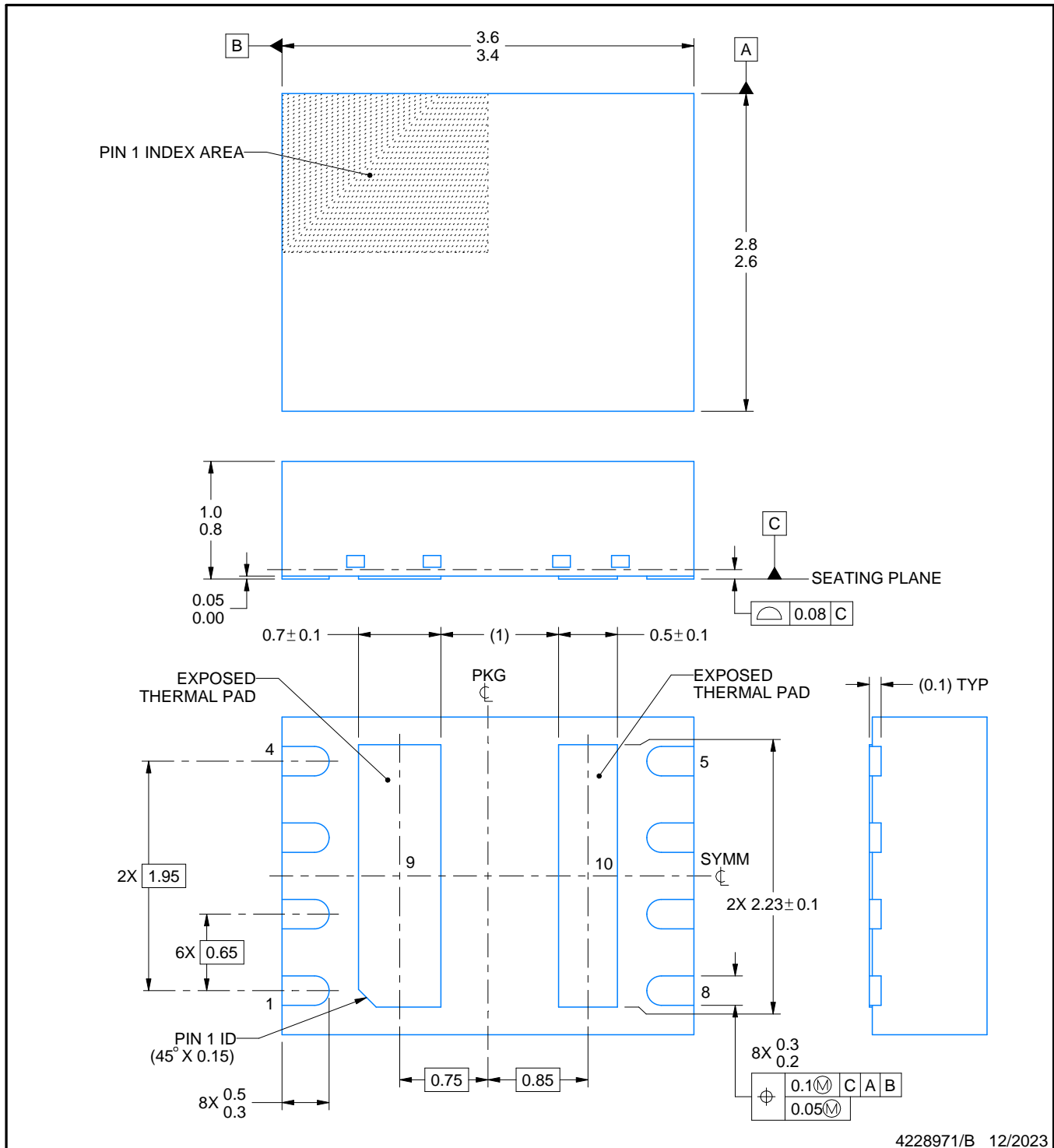
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC0106M25DENR	VSON	DEN	8	5000	330.0	12.4	3.0	3.8	1.2	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC0106M25DENR	VSON	DEN	8	5000	346.0	346.0	33.0



## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

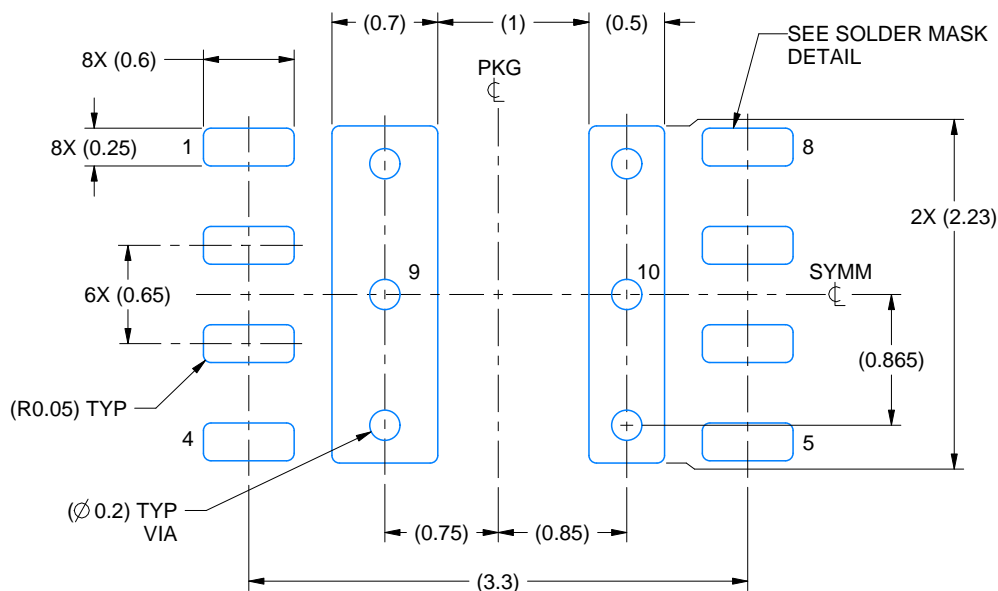


# EXAMPLE BOARD LAYOUT

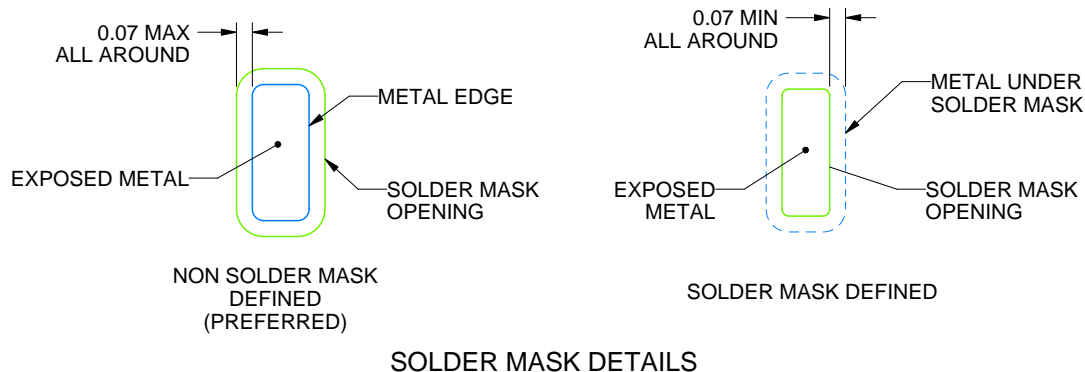
DEN0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4228971/B 12/2023

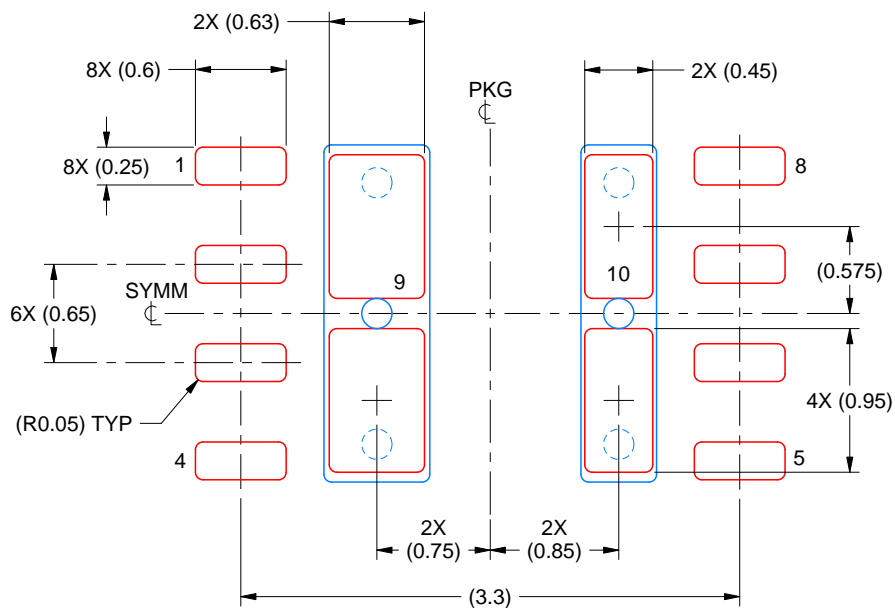
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DEN0008A**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
PADS 9 & 10: 77%

4228971/B 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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