AM26LV32E Low-Voltage High-Speed Quadruple Differential Line Receiver With ±15-KV IEC ESD Protection

1 Features

- Meets or exceeds standard TIA/EIA-422-B and ITU recommendation V.11
- Operates from a single 3.3-V power supply
- Switching rates up to 32 MHz
- ESD Protection for RS422 bus pins (See *ESD Ratings*)
- Low power dissipation: 27 mW typical
- Open circuit fail-safe
- ±7-V Common-mode input voltage range with ±200-mV sensitivity
- Accepts 5-V logic inputs with 3.3-V supply (enable inputs)
- Input hysteresis: 35 mV typical
- Pin-to-pin compatible with AM26C32, AM26LS32
- I_{off} Supports partial-power-down mode operation

2 Applications

- High-reliability automotive applications
- Configuration control and print support
- ATM and cash counters
- Smart grid
- AC and servo motor drives

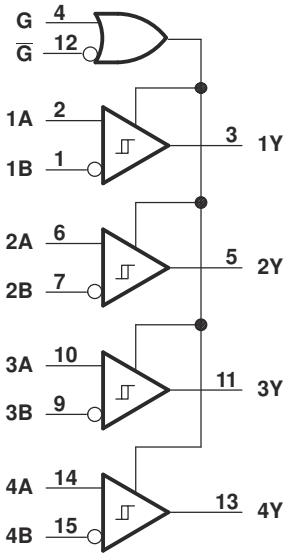
3 Description

The AM26LV32E device consists of quadruple differential line receivers with 3-state outputs. This device is designed to meet TIA/EIA-422-B and ITU recommendation V.11 drivers with reduced supply voltage. The device is optimized for balanced bus transmission at switching rates up to 32 MHz. The 3-state outputs permit connection directly to a bus-organized system. The AM26LV32E has an internal fail-safe circuitry that prevents the device from putting an unknown voltage signal at the receiver outputs. In the open fail-safe, a high state is produced at the respective output. This device is supported for partial-power-down applications using I_{off}. I_{off} circuitry disables the outputs, preventing damaging current back-flow through the device when it is powered down.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AM26LV32E	SO (16)	10.2 mm × 7.8 mm
	SOIC (16)	9.9 mm x 6 mm
	VQFN (16)	4 mm x 3.5 mm
	TSSOP (16)	5 mm x 6.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2020) to Revision E (August 2023) **Page**

- Changed the Device Information table to the *Package Information* table....1
- Changed the *Thermal Information* 5
- Changed the *Typical Characteristics* 6

Changes from Revision C (July 2018) to Revision D (December 2020) **Page**

- Changed feature From: *Open Circuit, Short Circuit, and Terminated Fail-Safe* To: *Open Circuit Fail-Safe* 1
- Deleted text from the Description: *shorted fail-safe, and terminated fail-safe* To: *Open Circuit Fail-Safe* 1
- Deleted text from the last paragraph in Input Fail-Safe Circuitry: *terminated or short* 8
- Deleted text from Table 8-1: *shorted, or terminated* 9

Changes from Revision B (July 2015) to Revision C (July 2018) **Page**

- Changed the pinout image appearance 3
- Changed the A and B Input signals on the waveform of Figure 7-1 7

Changes from Revision A (May 2008) to Revision B (July 2015) **Page**

- Added *Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section* 1

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5 Pin Configuration and Functions

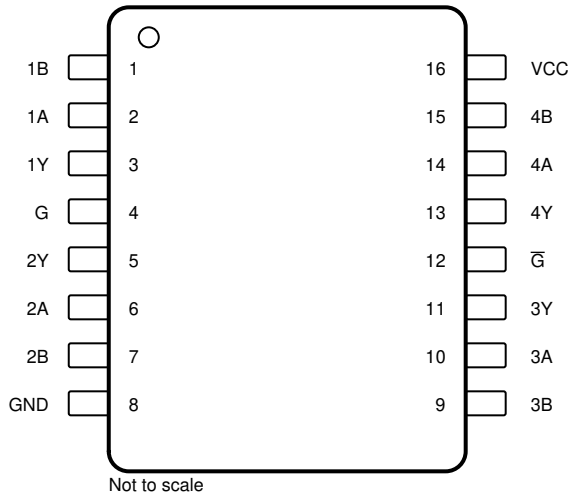

Figure 5-1. D, NS, or PW Package, 16-Pin SOIC, SO, or TSSOP (Top View)

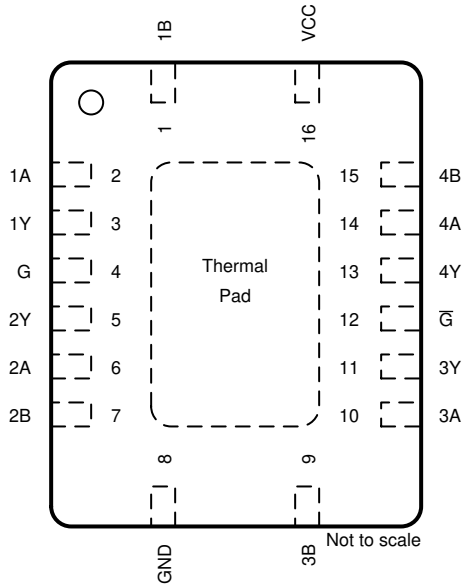

Figure 5-2. RGY Package 16-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1A	2	I	RS422/RS485 differential input (noninverting)
1B	1	I	RS422/RS485 differential input (inverting)
1Y	3	O	Logic level output
2A	6	I	RS422/RS485 differential input (noninverting)
2B	7	I	RS422/RS485 differential input (inverting)
2Y	5	O	Logic level output
3A	10	I	RS422/RS485 differential input (noninverting)
3B	9	I	RS422/RS485 differential input (inverting)
3Y	11	O	Logic level output
4A	14	I	RS422/RS485 differential input (noninverting)
4B	15	I	RS422/RS485 differential input (inverting)
4Y	13	O	Logic level output
G	4	I	Active-high select
$\overline{G}$	12	I	Active-low select
GND	8	—	Ground
V_{CC}	16	—	Power Supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		-0.5	6	V
V_I	Input voltage	A or B inputs	–14	14	V
		G or $\overline{G}$ inputs	–0.5	6	
V_{ID}	Differential input voltage(4)		–14	14	V
V_O	Output voltage		–0.5	6	V
I_O	Output current			±20	mA
I_{IK}	Input clamp current	V_I < 0		-20	mA
I_{OK}	Output clamp current	V_O < 0		-20	mA
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential input voltage are with respect to the network GND.
(3) This device is designed to meet TIA/EIA-422-B and ITU.
(4) Differential input voltage is measured at the non-inverting input with respect to the corresponding inverting input.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V
		IEC61000-4-2, Contact Gap Discharge	±8000	
		IEC61000-4-2, Air Gap Discharge	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±15000 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IC}	Common-mode input voltage	–7		7	V
V_{ID}	Differential input voltage	–7		7	V
I_{OH}	High-level output current			–5	mA
I_{OL}	Low-level output current			5	mA
T_A	Operating free-air temperature	–40		85	°C

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6.4 Thermal Information

THERMAL METRIC(1)		AM26LV32E								UNIT
		D (SOIC)	DR (SOIC-Reel)	PW (TSSOP)	PWR (TSSOP-Reel)	NS (SOP)	NSR (SOP-Reel)	RGY (VQFN)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.1	84.6	109	107.5	69	88.5	92	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.4	43.5	34	38.4	34	46.2	40	46.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	43.2	N/A	53.7	N/A	50.7	N/A	24.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	N/A	10.4	N/A	3.2	N/A	13.5	N/A	2.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	N/A	42.8	N/A	53.1	N/A	50.3	N/A	24.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	N/A	8.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended ranges of common-mode input, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input					0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input			–0.2			V
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT-}$)				35		mV
V_{IK}	Input clamp voltage, G and $\overline{G}$	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –5 mA		2.4	3.2		V
		V_{ID} = 200 mV, I_{OH} = –100 µA		V_{CC} – 0.1			
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 5 mA			0.17	0.5	V
		V_{ID} = –200 mV, I_{OL} = 100 µA				0.1	
I_{OZ}	High-impedance state output current	$V_O = V_{CC}$ or GND				±50	µA
I_{off}	Output current with power off	V_{CC} = 0 V, V_O = 0 or 5.5 V				±100	µA
I_I	Line input current	Other input at 0 V	V_I = 10 V			1.5	mA
			V_I = –10 V			–2.5	
I_I	Enable input current, G and $\overline{G}$	$V_I = V_{CC}$ or GND				±1	µA
r_i	Input resistance	V_{IC} = –7 V to 7 V, Other input at 0 V		4	17		kΩ
I_{CC}	Supply current (total package)	G, $\overline{G} = V_{CC}$ or GND, No load, Line inputs open			8	17	mA
C_{pd}	Power dissipation capacitance	One channel			150		pF

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6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 7-1	8	16	26	ns
t_{PHL}	Propagation delay time, high- to low-level output		8	16	26	ns
t_t	Transition time	See Figure 7-1		5		ns
t_{PZH}	Output-enable time to high-level	See Figure 7-2		17	40	ns
t_{PZL}	Output-enable time to low-level	See Figure 7-2		10	40	ns
t_{PHZ}	Output-disable time from high-level	See Figure 7-2		20	40	ns
t_{PLZ}	Output-disable time from low-level	See Figure 7-2		16	40	ns
$t_{sk(p)}$	Pulse skew	See Figure 7-1 Figure 7-2		4	6	ns
$t_{sk(o)}$	Pulse skew	See Figure 7-1 Figure 7-2		4	6	ns
$t_{sk(pp)}$	Pulse skew (device to device)	See Figure 7-1 Figure 7-2		6	9	ns
$f_{(max)}$	Maximum operating frequency	See Figure 7-1		32		MHz

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.7 Typical Characteristics

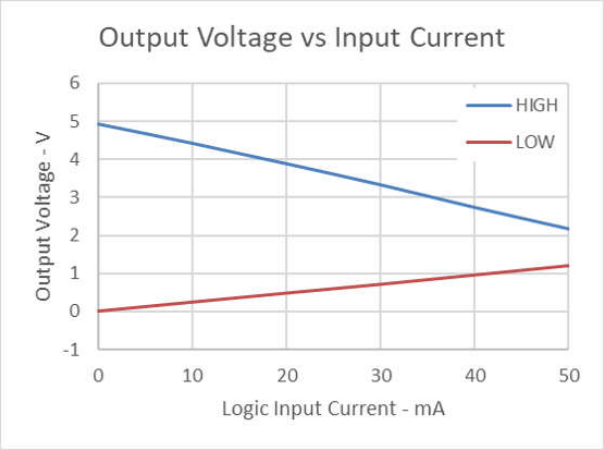

Figure 6-1. Output Voltage vs Input Current

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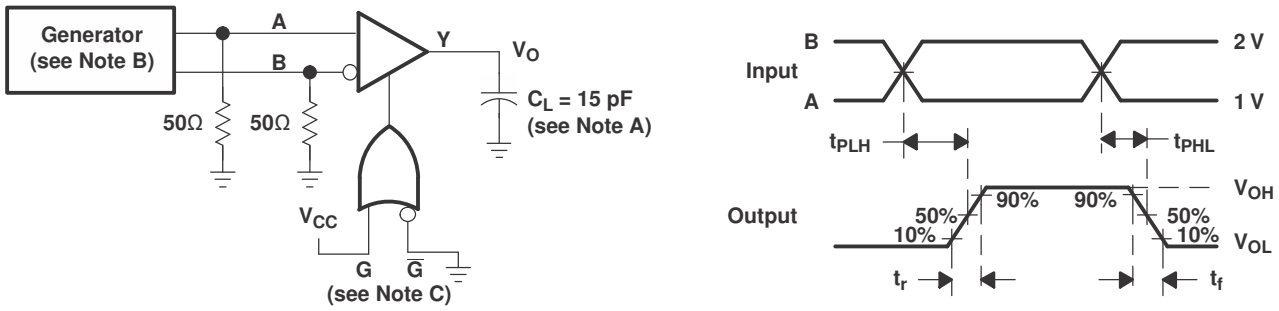
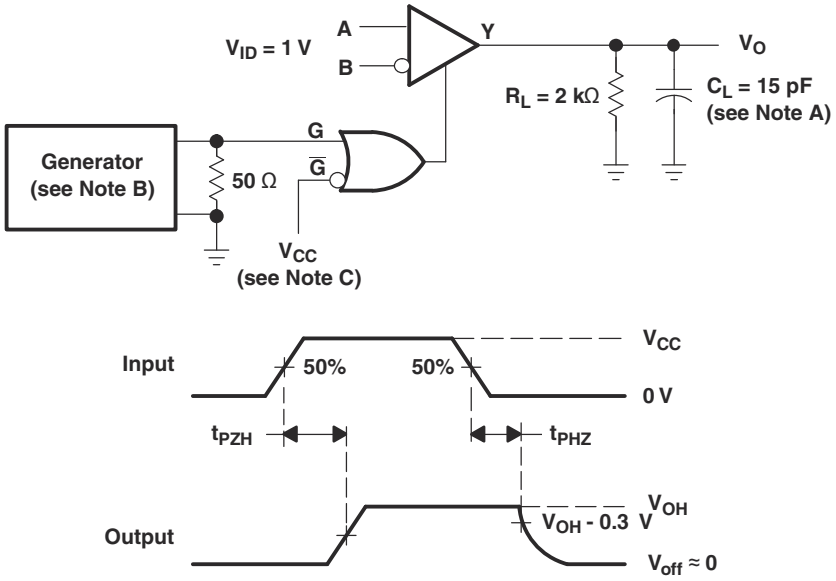
7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

Figure 7-1. Switching Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_r = t_f = 6 ns.

Figure 7-2. Enable/Disable Time Test Circuit and Output Voltage Waveforms

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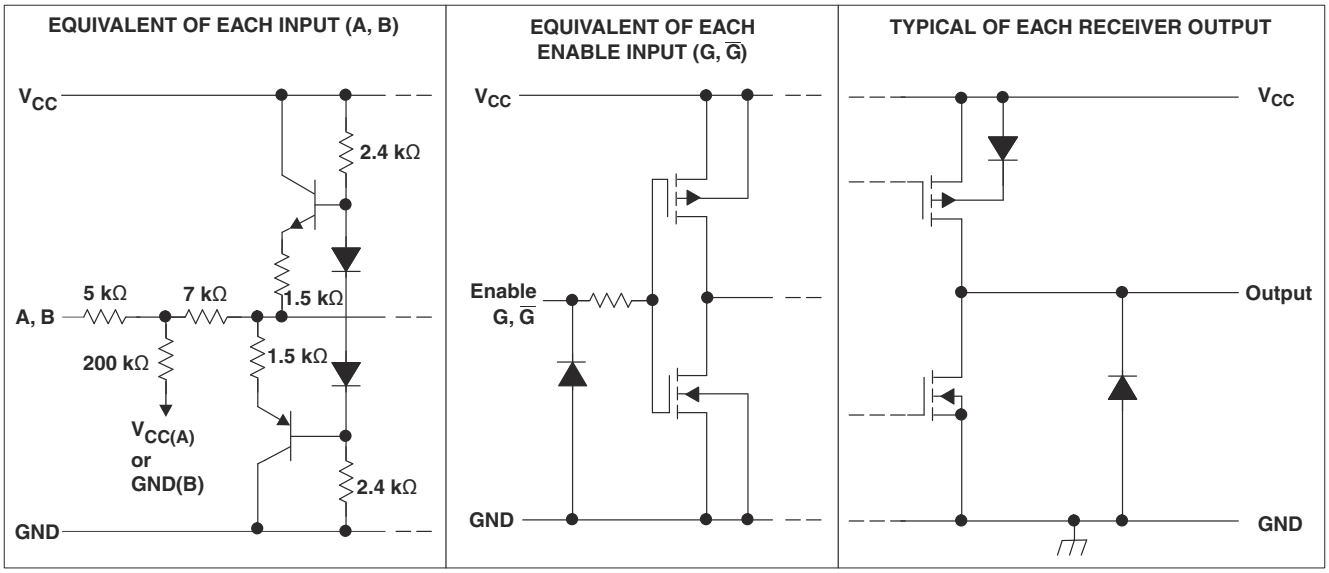
8 Detailed Description

8.1 Overview

The AM26LV32E is a low-voltage, quadruple-differential line receiver that meets the necessary requirements for NSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11. This device allows a low power or low voltage MCU to interface with heavy machinery, subsystems and other devices through long wires of up to 1000 m, giving any design a reliable and easy to use connection. As with any RS422 interface, the AM26LV32E works in a differential voltage range, which enables very good signal integrity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ±7-V Common-Mode Range With ±200-mV Sensitivity

For a common-mode voltage varying from –7 V to 7 V, the input voltage is acceptable in low ranges greater than 200 mV as a standard.

8.3.2 Input Fail-Safe Circuitry

RS-485 specifies that the receiver output state should be logic high for differential input voltages of $V_{AB} \geq +200$ mV and logic low for $V_{AB} \leq -200$ mV. For input voltages in between these limits, a receiver's output state is not defined and can randomly assume high or low. Removing the uncertainty of random output states, modern transceiver designs include internal biasing circuits that put the receiver output into a defined state (typically high) in the absence of a valid input signal. A loss of input signal can be caused by:

- an open circuit caused by a wire break or the unintentional disconnection of a transceiver from the bus
- a short circuit due to an insulation fault, connecting both conductors of a differential pair to one another
- an idle bus when none of the bus transceivers are active.

An open circuit caused by a wire break or the unintentional disconnection of a transceiver from the bus. The AM26LV32E has an internal circuit that ensures functionality during an open failure.

8.3.3 Active-High and Active-Low

The device can be configure using the G and $\overline{G}$ logic inputs to select receiver output. The high voltage or logic 1 on the G pin, allows the device to operate on an active-high and having a low voltage or logic 0 on the $\overline{G}$ enables active low operation. These are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

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8.4 Device Functional Modes

8.4.1 Enable and Disable

The receivers implemented in these RS422 devices can be configured using the G and $\overline{G}$ pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

Table 8-1. Function Table (Each Driver)

DIFFERENTIAL INPUT	ENABLES[1]		OUTPUT
	G	$\overline{G}$	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
–0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq$ –0.2 V	H	X	L
	X	L	L
Open	H	X	H
	X	L	H
X	L	H	Z

(1) H = high-level, L = low-level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, ac termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) illustrate the usefulness and robustness of RS-422 (and, indirectly, RS- 485). Similar results can be obtained if 485-compliant devices and termination techniques are used. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LV31E and AM26LV32E, respectively, were tested at room temperature with a 3.3-V supply voltage. Two plots per termination technique are shown. In each plot, the top waveform is the driver input and the bottom waveform is the receiver output. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable; the second plot shows input waveforms to the receiver at the far end of the cable.

9.2 Typical Application

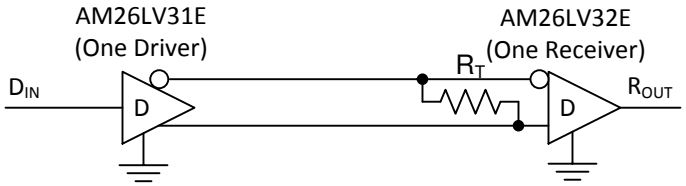

Figure 9-1. Differential Terminated Configuration

9.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, R_T, must be within 20% of the characteristic impedance, R_{OUT} , of the cable and can vary from about 80 Ω to 120 Ω.

9.2.2 Detailed Design Procedure

Figure 9-1 shows a configuration with R_T as termination. Although reflections are present at the receiver inputs at a data signaling rate of 200 kbps with no termination, the RS-422-compliant receiver reads only the input differential voltage and produces a clean signal at the output.

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9.2.3 Application Curve

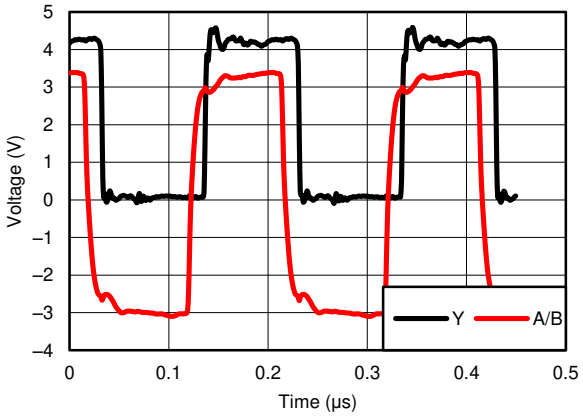

Figure 9-2. Differential 120-Ω Terminated Output Waveforms (CAT 5E Cable)

10 Power Supply Recommendations

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

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11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

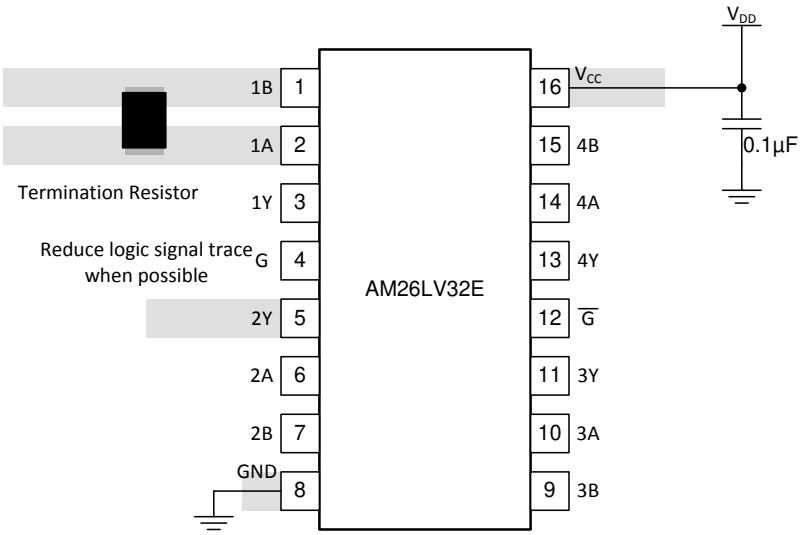

Figure 11-1. Trace Layout on PCB and Recommendations

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AM26LV32EIDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV32EI
AM26LV32EIDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV32EI
AM26LV32EIDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV32EI
AM26LV32EINSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV32EI
AM26LV32EINSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV32EI
AM26LV32EINSRG4	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV32EI
AM26LV32EINSRG4.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV32EI
AM26LV32EIPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB32
AM26LV32EIPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB32
AM26LV32EIPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB32
AM26LV32EIRGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB32
AM26LV32EIRGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB32
AM26LV32EIRGYRG4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB32

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AM26LV32E :

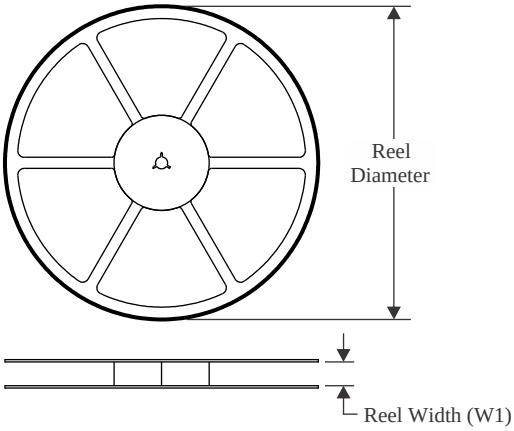
- Enhanced Product : AM26LV32E-EP

NOTE: Qualified Version Definitions:

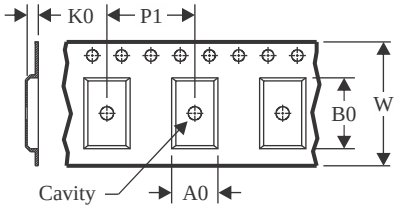
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

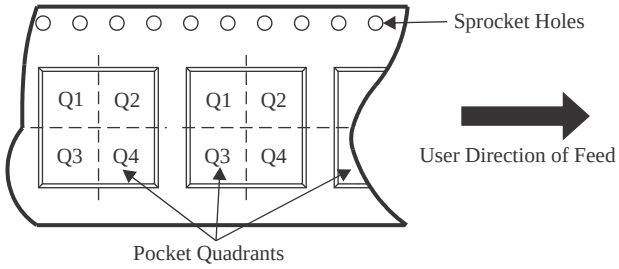


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

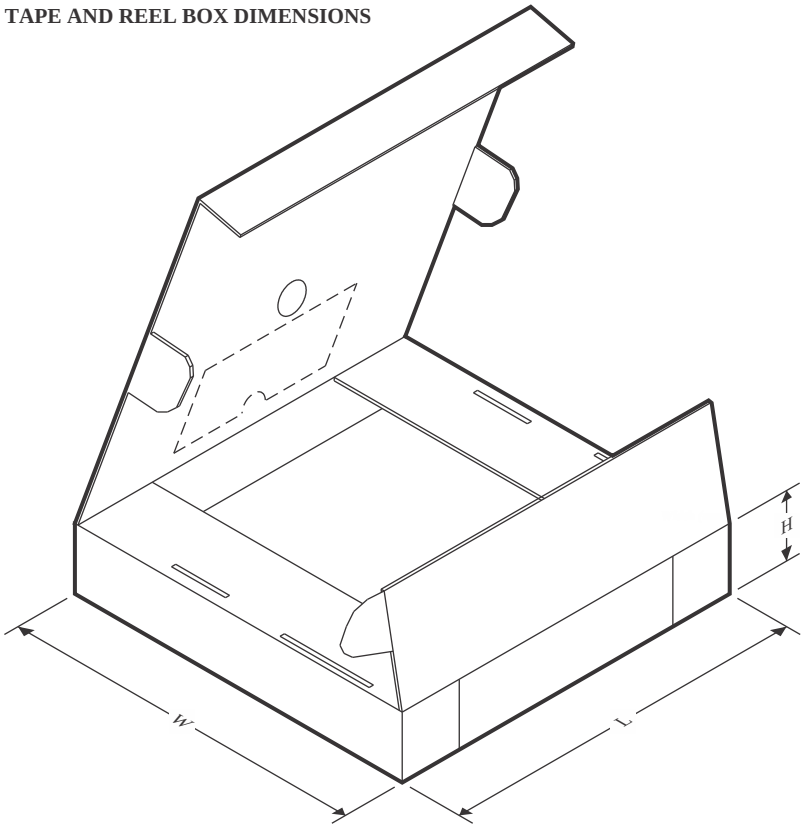
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

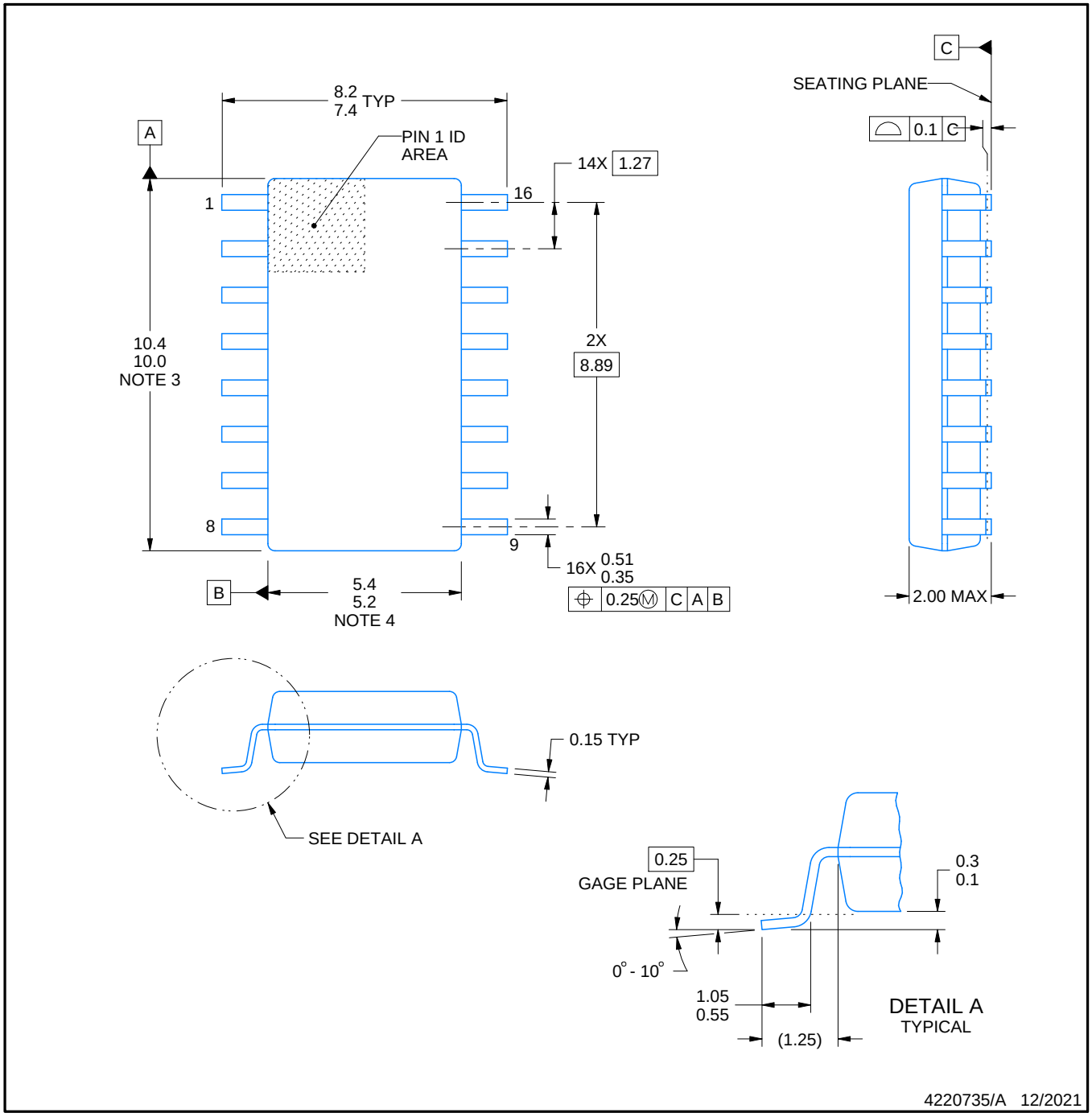
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV32EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV32EINSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
AM26LV32EINSRG4	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
AM26LV32EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LV32EIRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



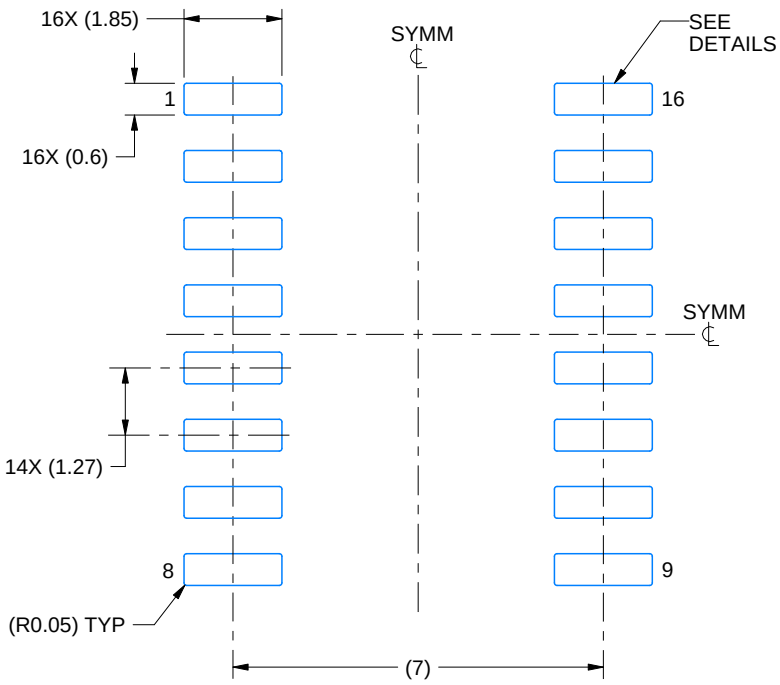
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV32EIDR	SOIC	D	16	2500	353.0	353.0	32.0
AM26LV32EINSR	SOP	NS	16	2000	353.0	353.0	32.0
AM26LV32EINSRG4	SOP	NS	16	2000	353.0	353.0	32.0
AM26LV32EIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
AM26LV32EIRGYR	VQFN	RGY	16	3000	360.0	360.0	36.0

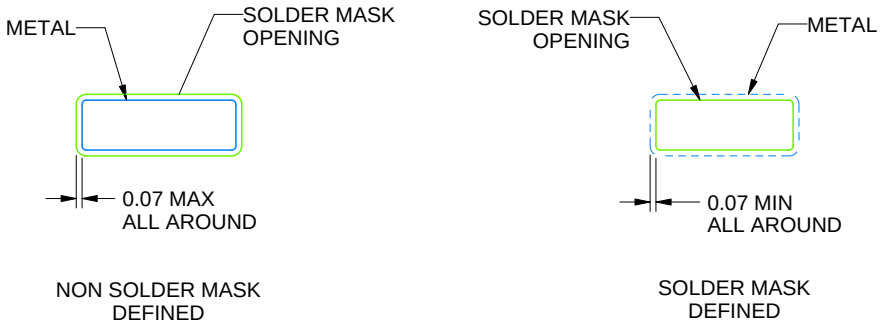


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

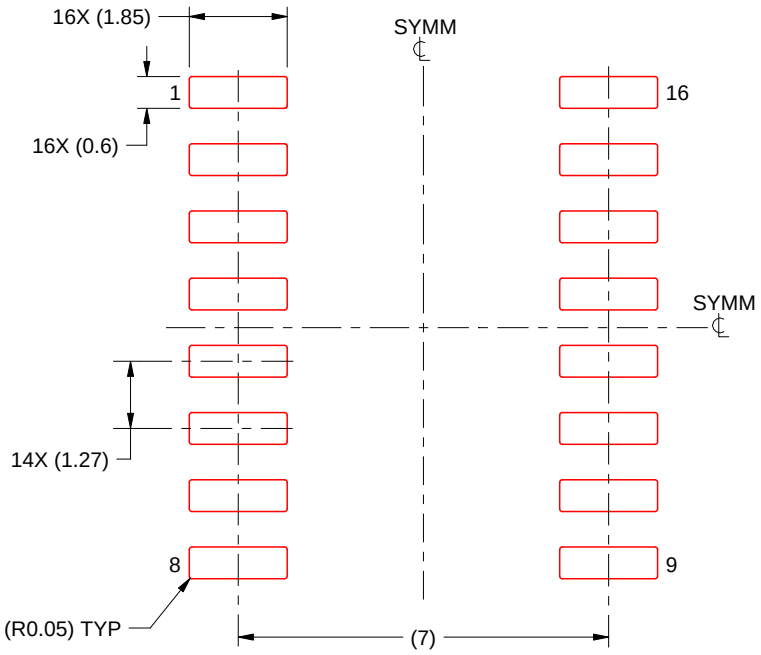


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



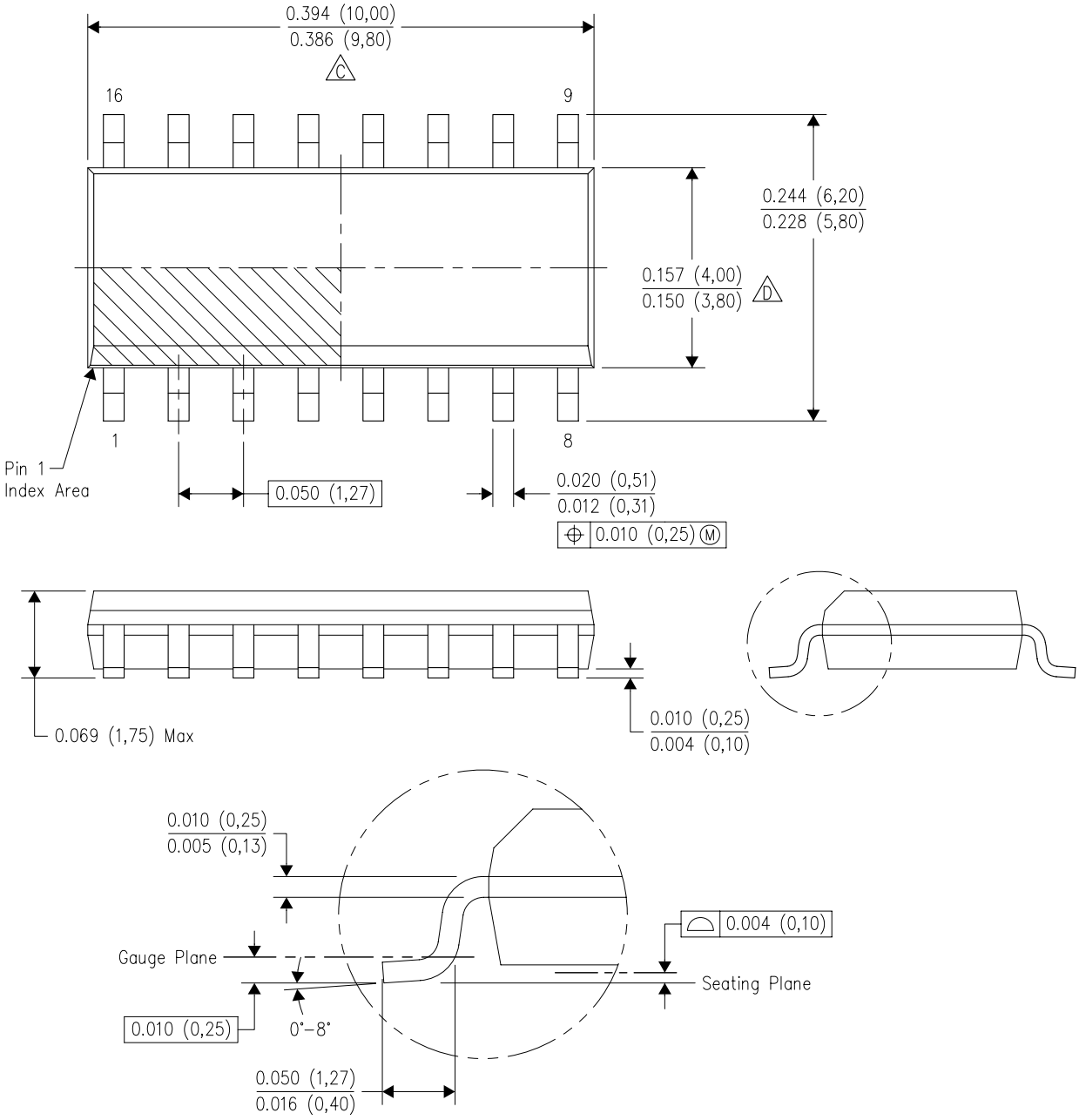
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



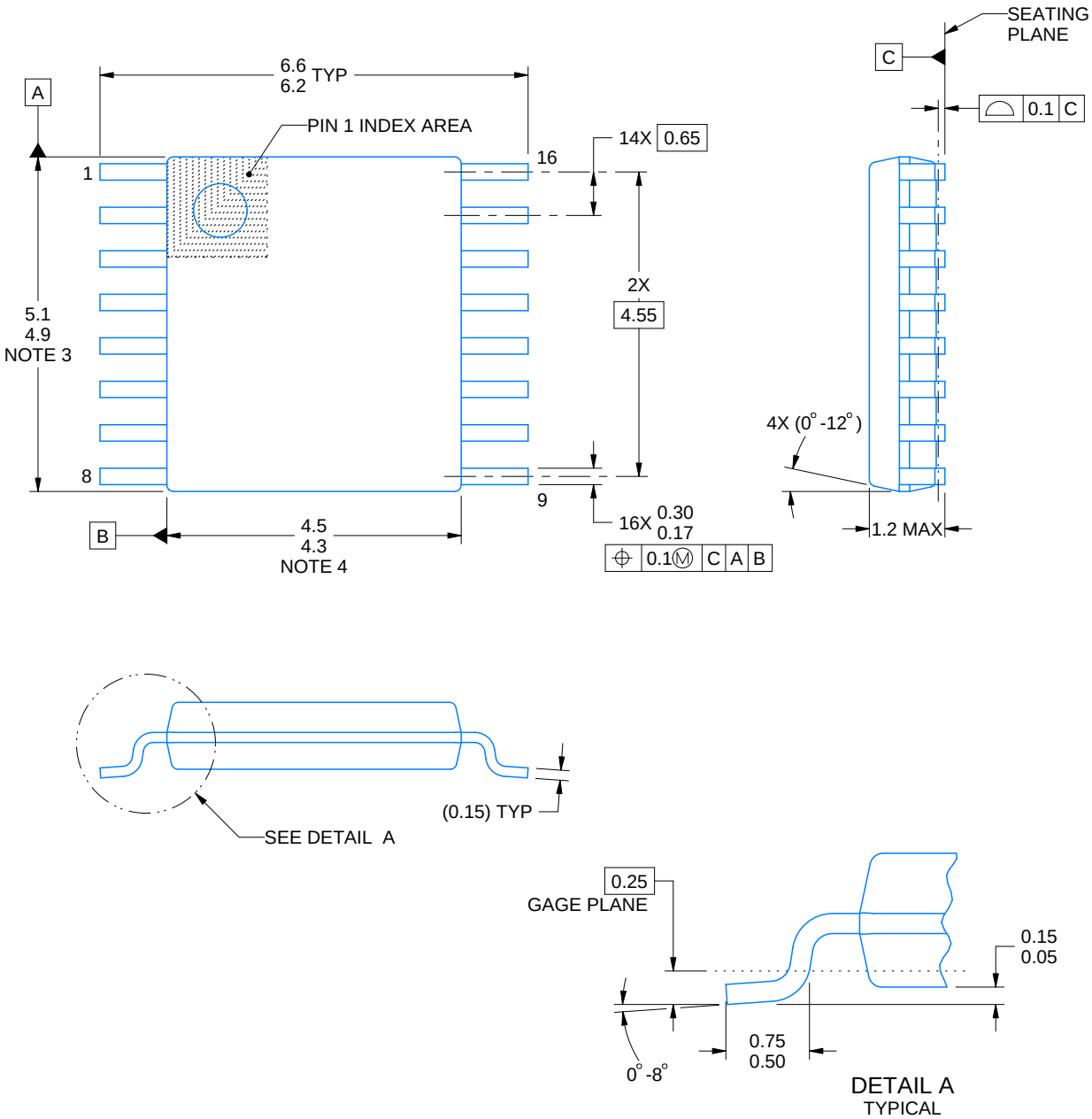
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

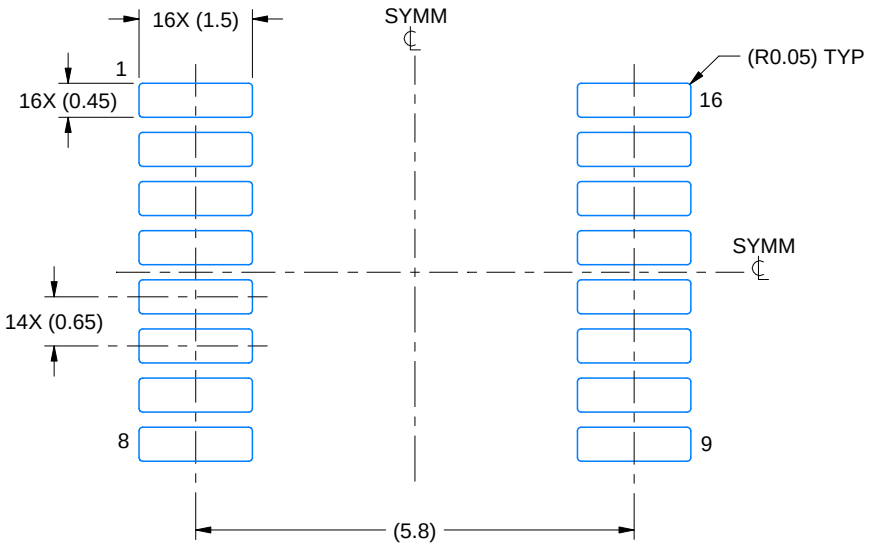
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

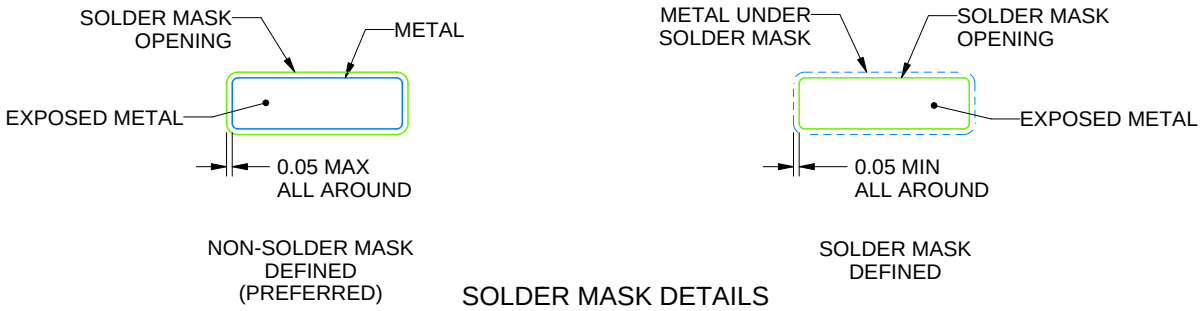


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

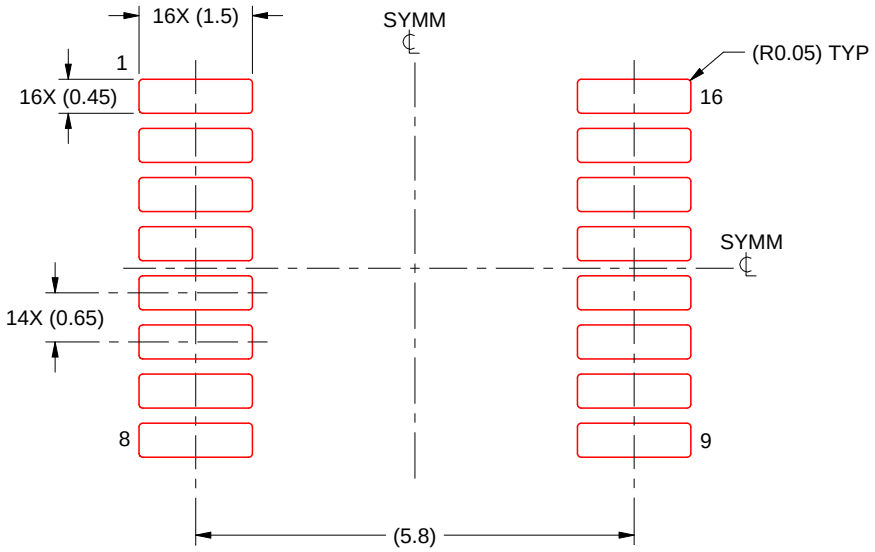


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



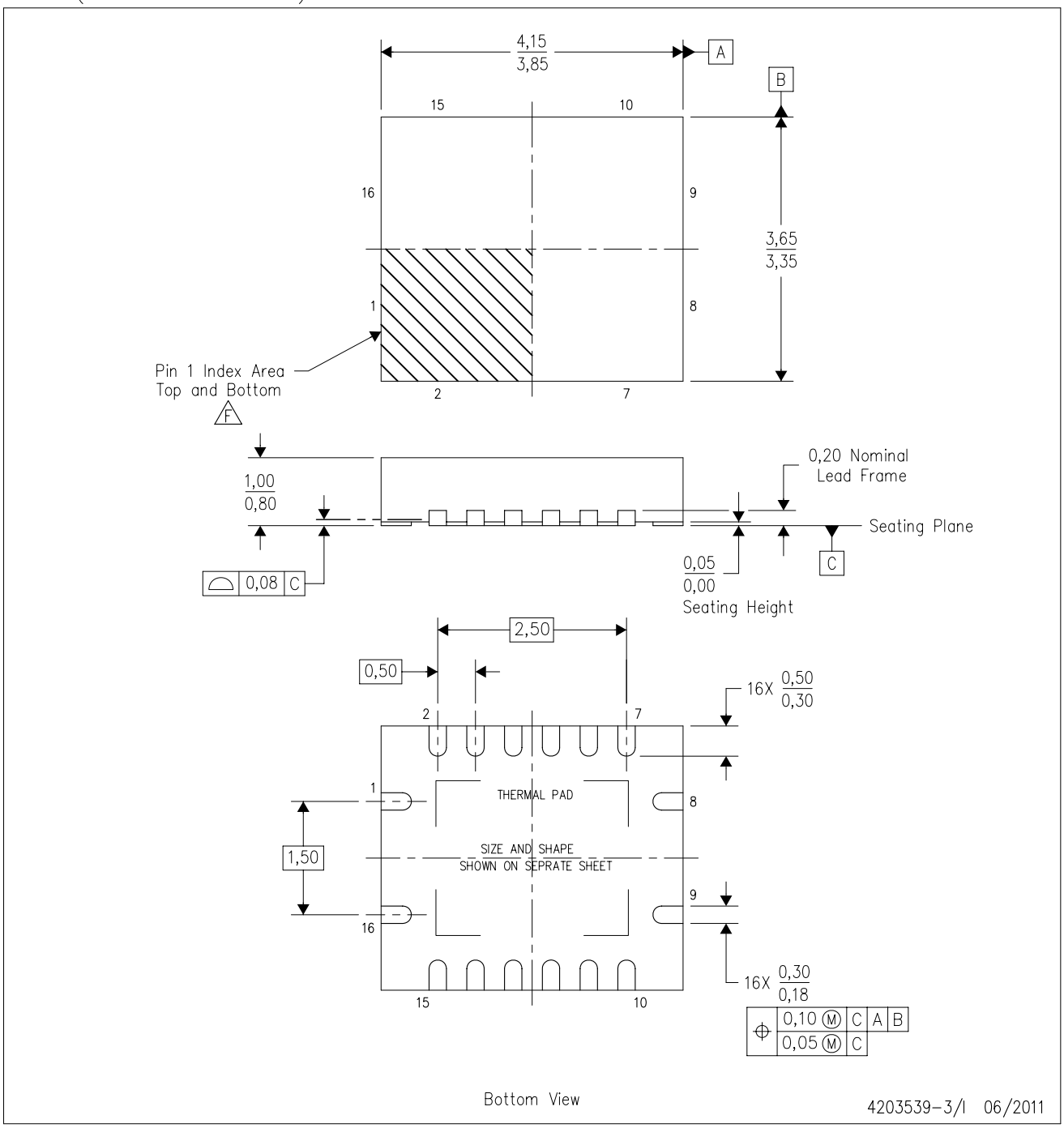
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

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