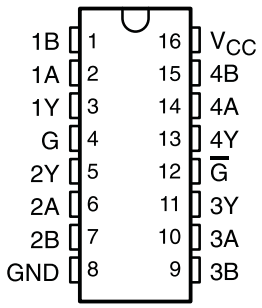
QML CLASS V RS-422 QUADRUPLE DIFFERENTIAL LINE RECEIVER

Check for Samples: AM26LS33A-SP

FEATURES

- **AM26LS33A Devices Meet or Exceed the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendations V.10 and V.11**
- **±15-V Common-Mode Range With ±500-mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operate From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output-Enable Inputs**
- **Input Impedance . . . 12 kΩ Minimum**
- **Designed to Be Interchangeable With Advanced Micro Device AM26LS33™**
- **QML-V Qualified, SMD 5962-78020**
- **Military Temperature Range (-55°C to 125°C)**
- **Rad-Tolerant: 25 kRad (Si) TID** (1)

J PACKAGE
(TOP VIEW)



(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/sec. Radiation Lot Acceptance Testing is available - contact factory for details.

DESCRIPTION

The AM26LS33A is a quadruple differential line receiver for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that, if the inputs are open, the outputs always are high.

Compared to the AM26LS33, the AM26LS33A incorporates an additional stage of amplification to improve sensitivity. The input impedance has been increased, resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this does not affect interchangeability in most applications.

The AM26LS33A is characterized for operation over the temperature range of –55°C to 125°C.

ORDERING INFORMATION(1)

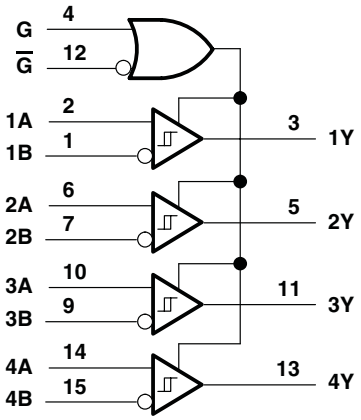
T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP - J	5962-7802007VEA	5962-7802007VEA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

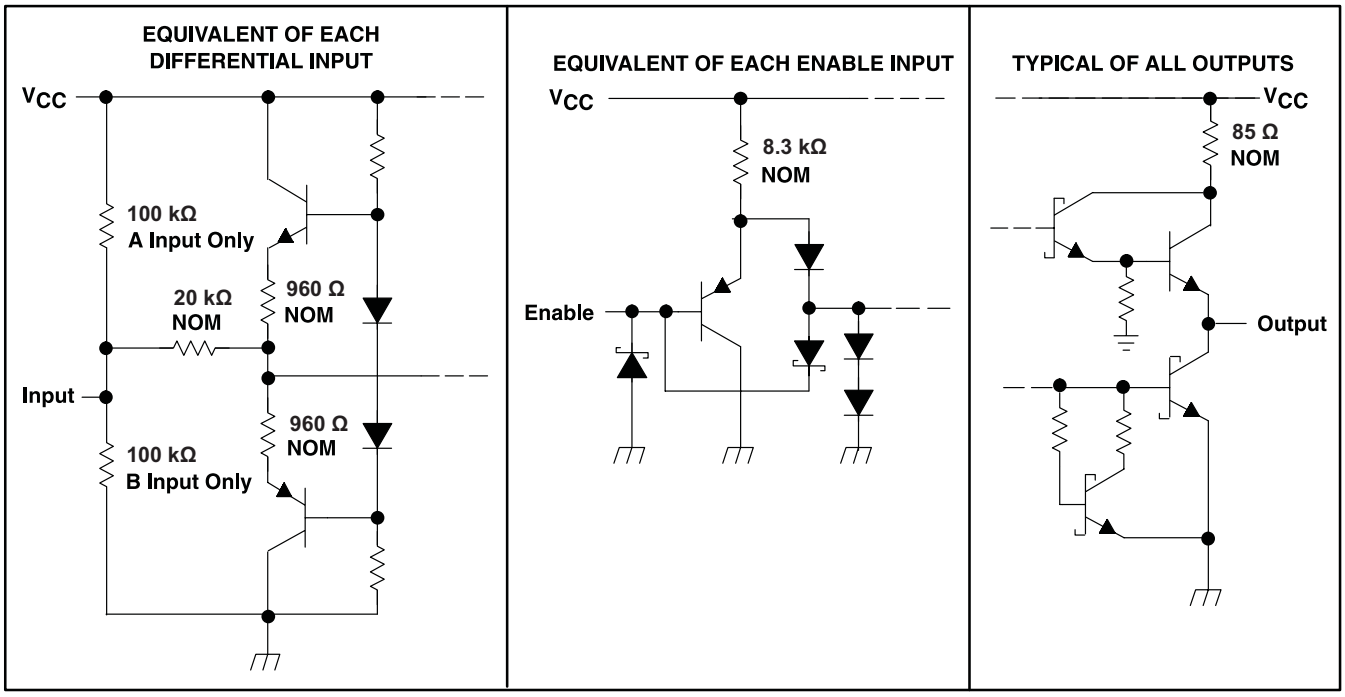
Table 1. FUNCTION TABLE
Each Receiver

DIFFERENTIAL A–B	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} \leq V_{ID} \leq V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATICS OF INPUTS AND OUTPUTS

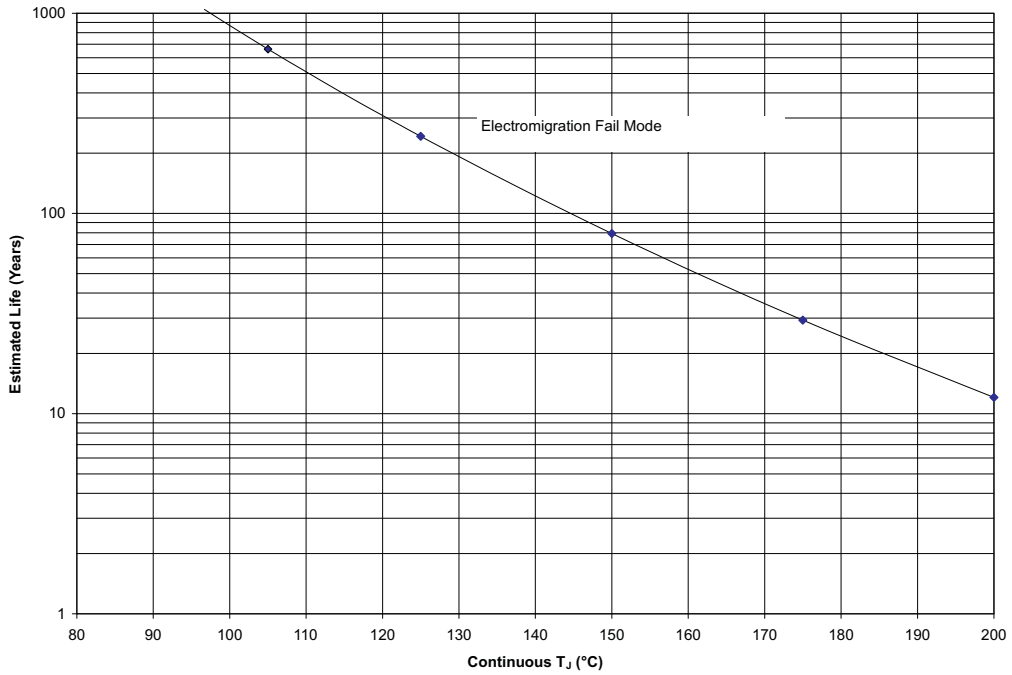


ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			7	V
V_I	Input voltage	Any differential input		±25	V
		Other inputs		7	
V_{ID}	Differential input voltage(3)			±25	V
	Continuous total power dissipation		See Dissipation Ratings Table		
	Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds			300	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground terminal.
(3) Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.



A. See datasheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. AM26LS33A 16/J Package Operating Life Derating Chart

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{IC}	Common-mode input voltage			±15	V
I_{OH}	High-level output current			–440	μA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	-55		125	°C

ELECTRICAL CHARACTERISTICS

over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = V_{OH}$min, I_{OH} = –440 μA -15 V ≤ VIC ≤ 15 V				0.5	V
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.45 V , I_{OL} = 8 mA -15 V ≤ VIC ≤ 15 V		–0.5(2)			V
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)				50		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = 4.5 V,	I_I = –18 mA			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, V_{ID} = 1 V, $V_{I(G)}$ = 0.8 V, I_{OH} = –440 μA		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, V_{ID} = –1 V, $V_{I(G)}$ = 0.8 V	I_{OL}= 4 mA			0.4	V
			I_{OL}= 8 mA			0.45	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = 5.5 V	V_O = 2.4 V			20	μA
			V_O = 0.4 V			–20	
I_I	Line input current	V_I = 15 V,	Other input at –10 V to 15 V			1.2	mA
		V_I = –15 V,	Other input at –15 V to 10 V			–1.7	
$I_{I(EN)}$	Enable input current	V_I = 5.5 V, V_{CC} = 5.5 V				100	μA
I_H	High-level enable current	V_I = 2.7 V, V_{CC} = 5.5 V				20	μA
I_L	Low-level enable current	V_I = 0.4 V, V_{CC} = 5.5 V				–0.36	mA
r_i	Input resistance	V_{IC} = –15 V to 15 V,	One input to ac ground	12	15		kΩ
I_{OS}	Short-circuit output current(3)	V_{CC} = MAX, V_{ID} = 1 V, V_O = 0 V		–15		–85	mA
I_{CC}	Supply current	V_{CC} = MAX, data inputs = GND,	All outputs disabled		52	70	mA

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.
(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
(3) Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

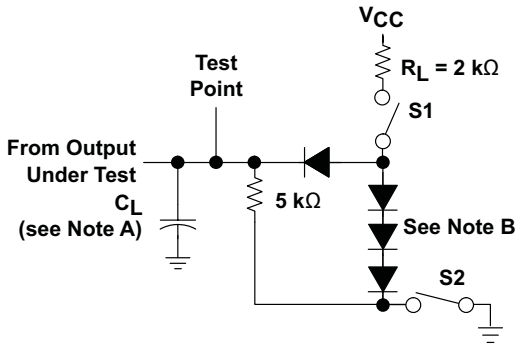
SWITCHING CHARACTERISTICS

V_{CC} = 5 V, over operating free-air temperature (unless otherwise noted)

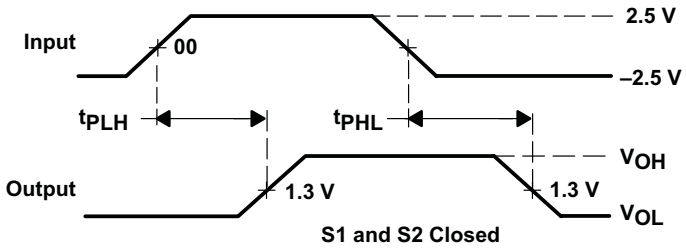
PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 2		20	35	ns
			T_A = –55°C to 125°C			53	
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 2		22	35	ns
			T_A = –55°C to 125°C			53	
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 2		17	25	ns
			T_A = –55°C to 125°C			38	
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 2		20	25	ns
			T_A = –55°C to 125°C			38	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 2		21	30	ns
			T_A = –55°C to 125°C			45	
t_{PLZ}	Output disable time from low level	C_L = 15 pF,	See Figure 2		30	40	ns
			T_A = –55°C to 125°C			60	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

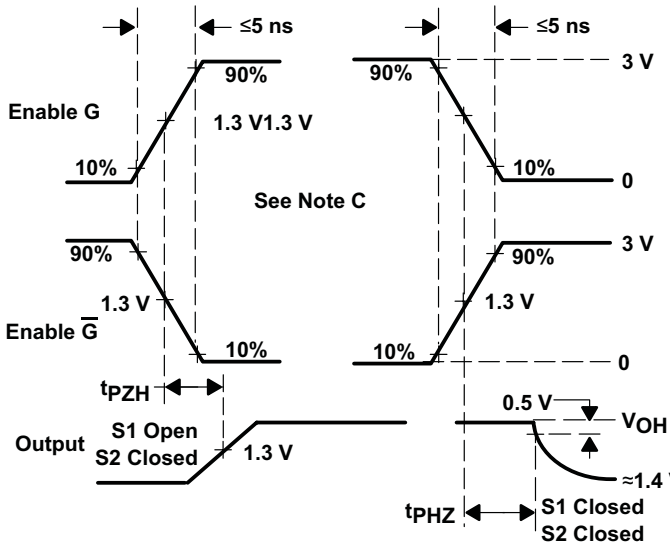
PARAMETER MEASUREMENT INFORMATION



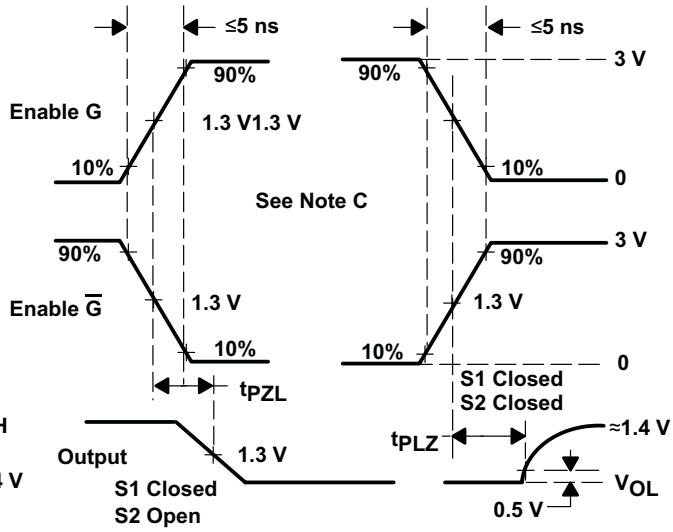
TEST CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



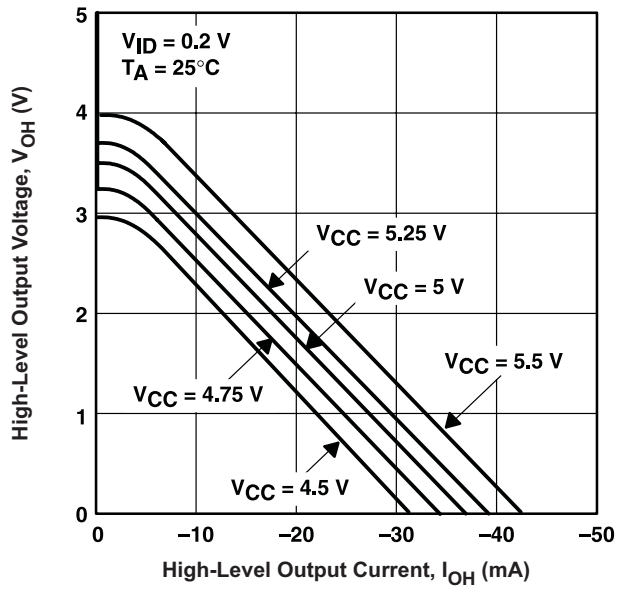
VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT



† V_{CC} = 5.5 V and V_{CC} = 4.5 V applies to M-suffix devices only.

Figure 3.

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

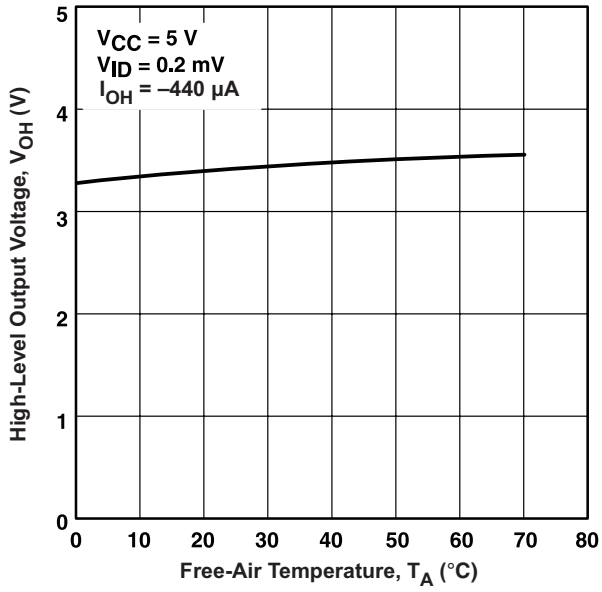


Figure 4.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

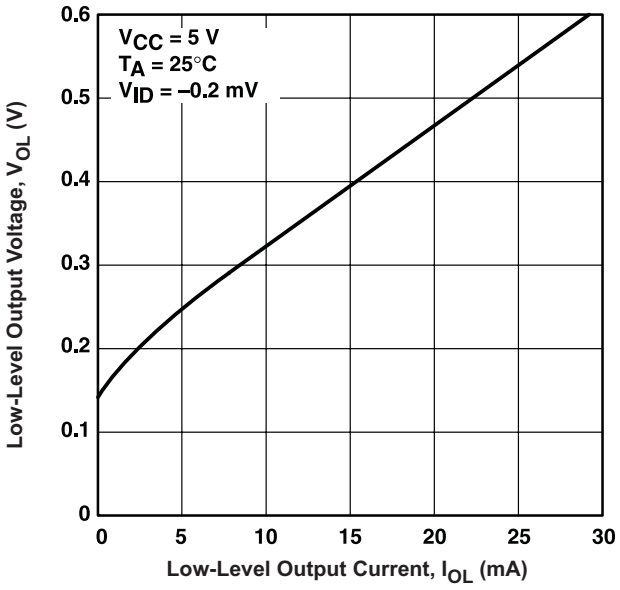


Figure 5.

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

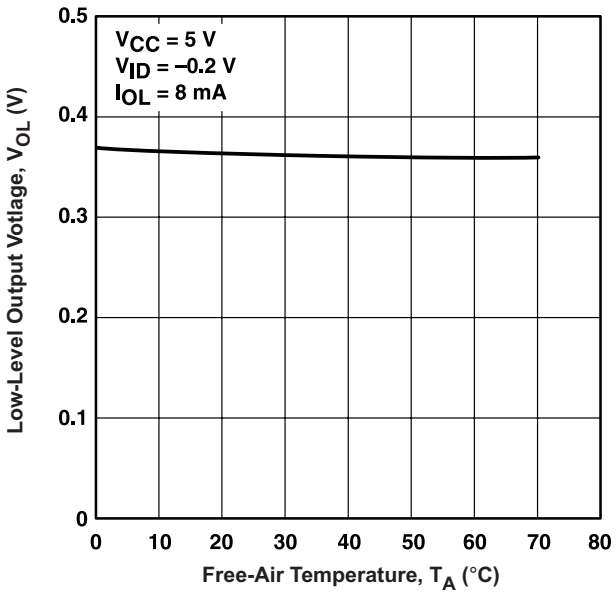


Figure 6.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

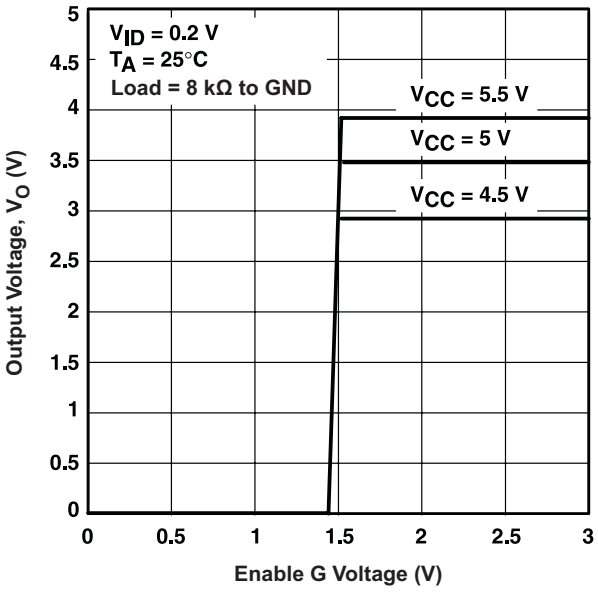


Figure 7.

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

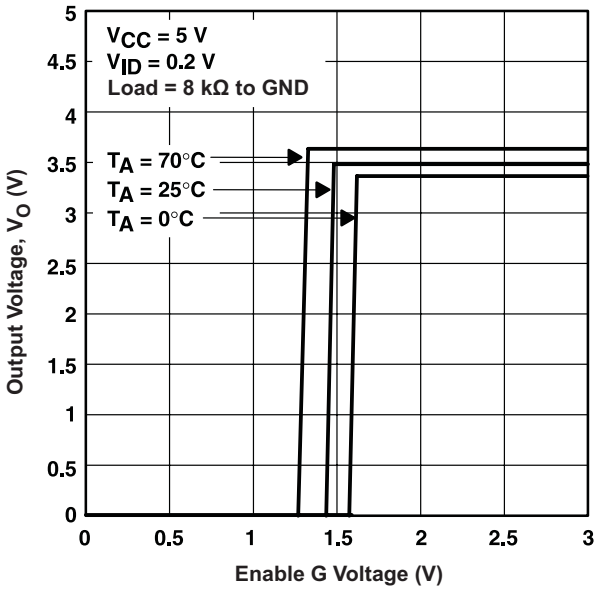


Figure 8.

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

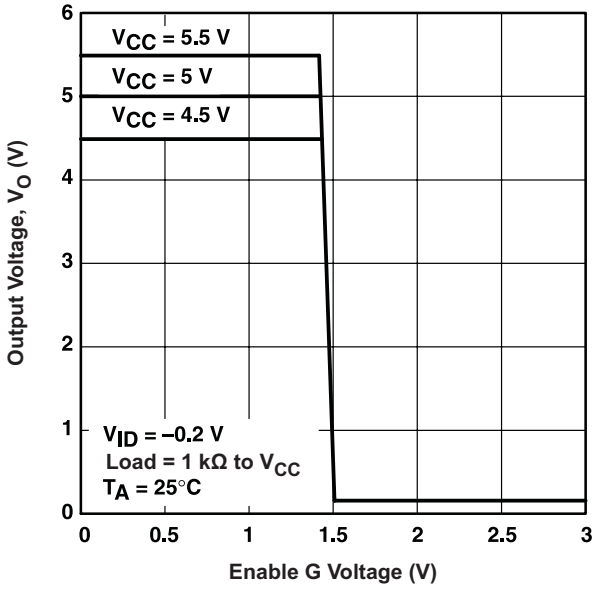


Figure 9.

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

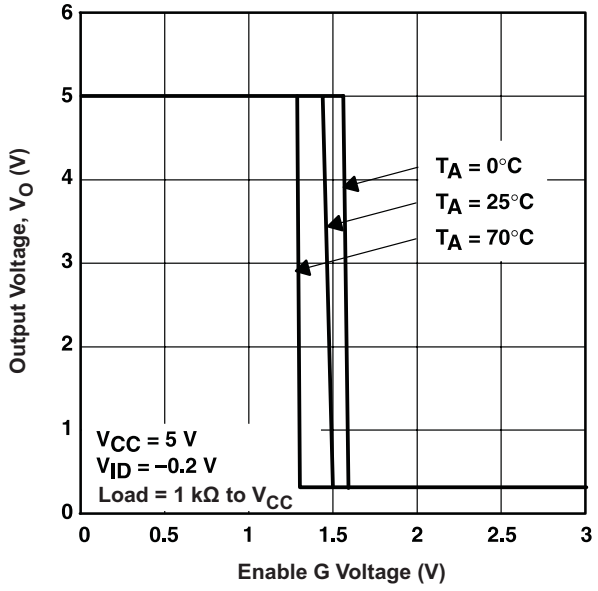


Figure 10.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

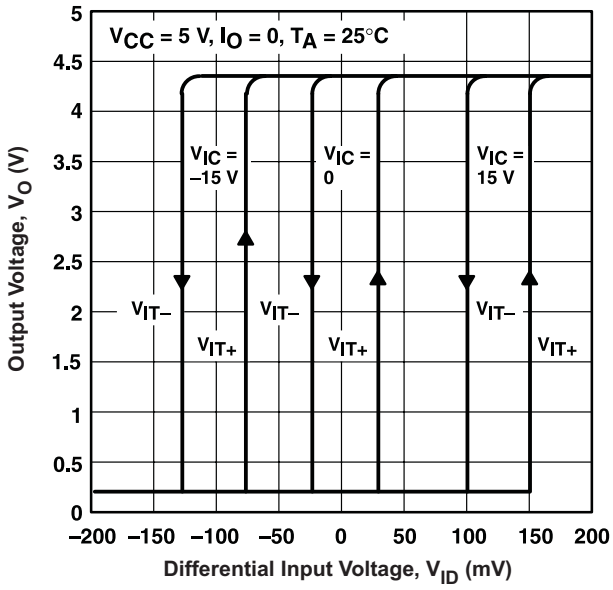
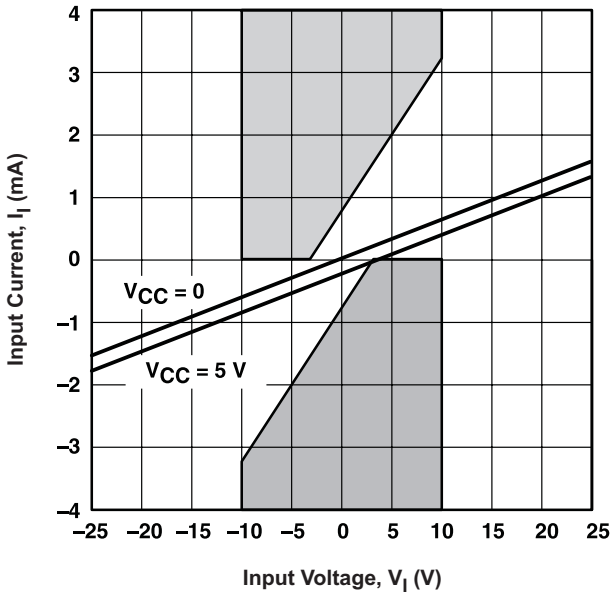


Figure 11.

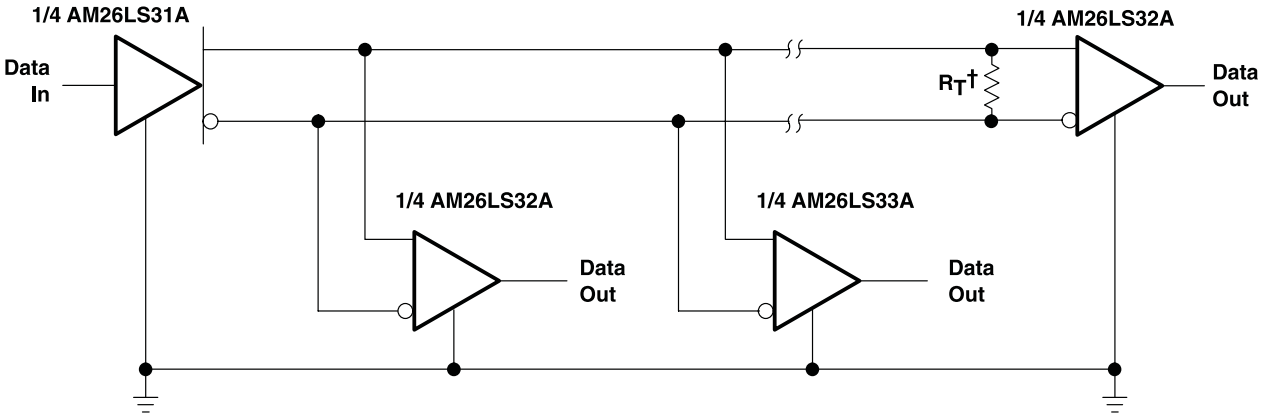
INPUT CURRENT vs INPUT VOLTAGE



The unshaded area shows requirements of paragraph 4.2.1 of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B.

Figure 12.

APPLICATION INFORMATION



† R_T equals the characteristic impedance of the line.

Figure 13. Circuit with Multiple Receivers

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-7802007VEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802007VE A
5962-7802007VEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802007VE A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

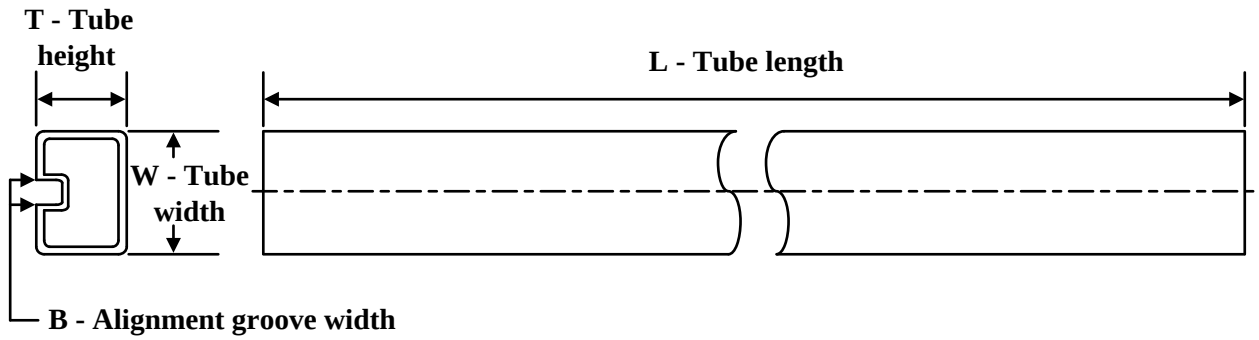
OTHER QUALIFIED VERSIONS OF AM26LS33A-SP :

- Catalog : AM26LS33A
- Military : AM26LS33AM

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



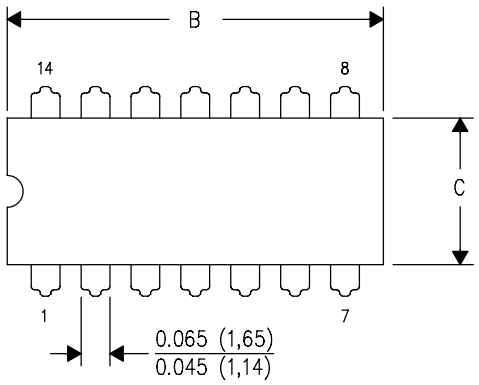
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-7802007VEA	J	CDIP	16	25	506.98	15.24	13440	NA
5962-7802007VEA.A	J	CDIP	16	25	506.98	15.24	13440	NA

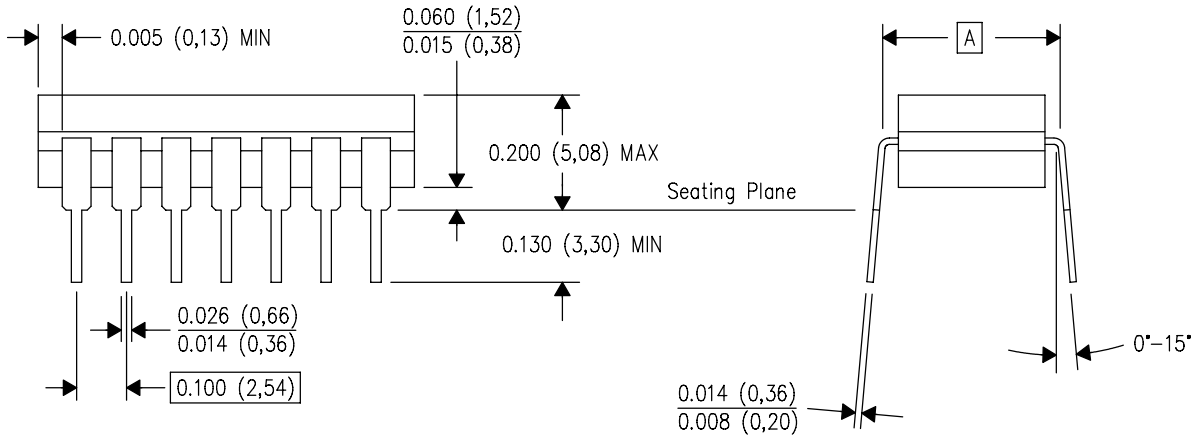
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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