ALM2403-Q1 Automotive, Low-Distortion, Dual-Channel Operational Amplifier With Integrated Protection for Resolver Drive

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional-safety capable
  - Documentation available to aid functional safety system design
- High output current drive: 500 mA, peak (per channel)
  - Replaces discrete op amps and transistors
- Wide supply range for both supplies (up to 24 V)
- Overtemperature shutdown
- Current limit
- Shutdown pin for low I_Q applications
- 21-MHz gain bandwidth with 50-V/µs slew rate
- Package: 14-pin HTSSOP (PWP)

2 Applications

- Resolver-based automotive and industrial applications
- Inverter and motor control
- Brake system
- Electric power steering (EPS)
- Rearview mirror module
- Automotive eMirrors
- Servo drive power stage module
- Flight control system

3 Description

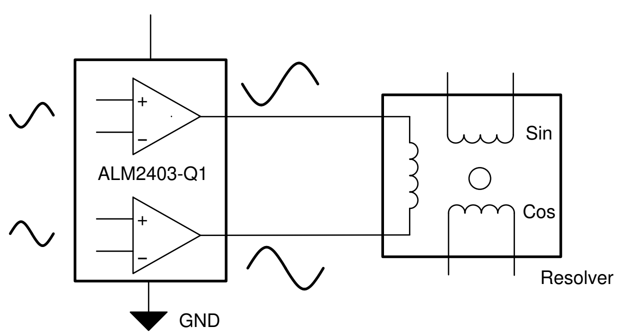
The ALM2403-Q1 is a dual-power op amp with features and performance that make this device preferable for resolver-based applications. The high-gain bandwidth and slew rate of the device, along with a continuous high-output current-drive capability, make this device an excellent choice to provide the low distortion and differential high-amplitude excitation required for exciting the resolver primary coil. Current limiting and overtemperature detection enhance overall system robustness, especially when driving analog signals over wires that are susceptible to faults.

The small HTSSOP package with thermal pad and low $R_{\theta JA}$ allows high currents to be delivered to loads while minimizing board space. The higher gain bandwidth of the ALM2403-Q1 allows the device to be configured as a filter stage while still providing high output drive, thus significantly reducing the total solution size of a resolver drive signal chain. This reduced solution size is a key advantage offered by the ALM2403-Q1 when used in automotive and industrial applications.

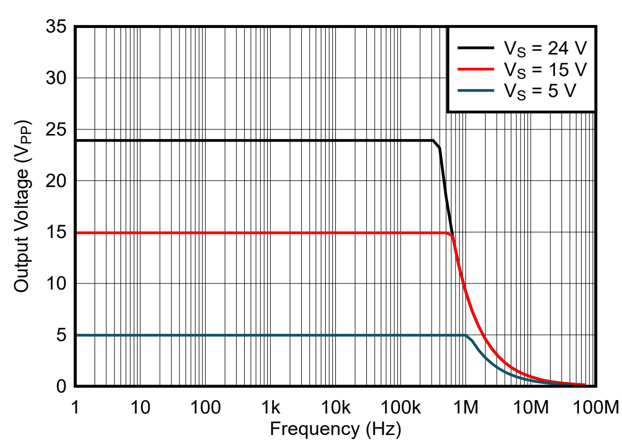
Package Information

PART NUMBER	PACKAGE[(1)]	BODY SIZE (NOM)
ALM2403-Q1	HTSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Schematic



Output Voltage vs Frequency

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2020) to Revision A (March 2023) — **Page**

- Changed output current from 650 mA to 500 mA in *Features* 1
- Changed title and Y-axis unit in front-page plot 1
- Changed pin names to synchronize pin naming throughout document.....3
- Changed thermal pad description text for clarity.....3
- Changed voltage range for V_{OTF/SH_DN} in the *Absolute Maximum Ratings* 4
- Changed all V_S voltages to single-supply nomenclature in the *Electrical Characteristics* and *Typical Chacteristics* 5
- Deleted test conditions from enable high and low input voltages in the *Electrical Characteristics* 5
- Moved shutdown current parameter to Power Supply section in the *Electrical Characteristics* 5
- Changed Figures 6-12 through 6-16 to correct axis units and values.....7
- Changed functional block diagram to correct inaccuracies.....12
- Changed EMC capacitance from 50 nF to 10 nF in Table 8-1, *Design Parameters* 16
- Added test condition to first bullet of *Detailed Design Procedure* 17
- Changed R3 to R2 in 2nd paragraph of *Filter Design* section.....17
- Changed terms in Equation 4 to Equation 6 for clarity.....18
- Changed Figure 8-4, *2nd-Order MFB LP Filter AC Output Characteristics* 19
- Changed values in Table 8-2, *Signal Attenuation vs Frequency* 19
- Changed Figure 8-6, *ALM2403-Q1 Layout Example*, to match EVM layout.....20

5 Pin Configuration and Functions

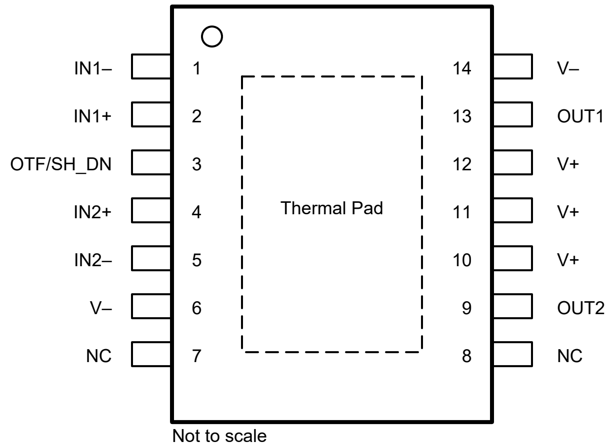


Figure 5-1. PWP Package, 14-Pin HTSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN1–	Input	Inverting op amp input for channel 1
2	IN1+	Input	Noninverting op amp input for channel 1
3	OTF/SH_DN	Input/Output	Overtemperature flag and shutdown (see Table 7-1, *Shutdown Truth Table*)
4	IN2+	Input	Noninverting op amp input for channel 2
5	IN2–	Input	Inverting op amp input for channel 2
6, 14	V–	—	Negative supply pin (both negative supply pins must be used and connected together)
7, 8	NC	—	No internal connection (do not connect)
9	OUT2	Output	Op amp output for channel 2
10, 11, 12	V+	—	Positive supply pin
13	OUT1	Output	Op amp output for channel 1
Thermal Pad	Thermal Pad	—	Connect the exposed thermal pad to the most negative supply on the device, V–, for best thermal performance. The thermal pad can also be left floating electrically; the heat spread of the pad can be thermally maximized and conducted into the PCB.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_S	Supply voltage	Single-supply, V_S = (V+) – GND		26	V
		Dual-supply, V_S = (V+) – (V–)		±13	
	Signal input voltage	Common-mode	(V–) – 0.7	(V+) + 0.7	V
		Differential		(V+) – (V–) + 0.2	
V_{OTF/SH_DN}	OTF/SH_DN pin voltage		(V–) – 0.2	(V–) + 5.7	V
	Signal input current			±10	mA
	Output short circuit[(2)]		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)] HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply, V_S = (V+) – GND	5		24	V
		Dual-supply, V_S = (V+) – (V–)	±2.5		±12	
T_A	Operating temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		ALM2403-Q1 PWP (HTSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = V+ = 24 V, V– = GND, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±6	±25	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±15	±50	µV/°C
PSRR	Power-supply rejection ratio	V_S = 5 V to 24 V		±10	±47	µV/V
		V_S = 5 V to 24 V, T_A = –40°C to +125°C			±50	µV/V
	Channel separation	f = 10 kHz		120		dB
INPUT BIAS CURRENT						
I_B	Input bias current			10	±100	pA
		T_A = –40°C to +125°C			±100	nA
I_{OS}	Input offset current			10	±200	pA
		T_A = –40°C to +125°C			±100	nA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		8		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz		150		$nV/\sqrt{Hz}$
		f = 100 kHz		22		$nV/\sqrt{Hz}$
i_N	Input current noise	f = 1 kHz		48		$fA/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V–) – 0.5 V < V_{CM} < (V+) + 0.5 V, 10 V ≤ V_S < 24 V	49	72		dB
		(V–) – 0.2 V < V_{CM} < (V+) + 0.2 V, T_A = –40°C to +125°C, 10 V < V_S < 24 V	52			dB
		(V–) + 2.5 V < V_{CM} < (V+) – 2.5 V, 10 V < V_S < 24 V	80	94		dB
		(V–) + 2.5 V < V_{CM} < (V+) – 2.5 V, T_A = –40°C to +125°C, 10 V < V_S < 24 V	75			dB
		(V–) – 0.5 V < V_{CM} < (V+) + 0.5 V, 5 V < V_S < 24 V	44	59		dB
INPUT CAPACITANCE						
Z_{ID}	Differential			1 || 2		GΩ || pF
Z_{ICM}	Common-mode			1 || 2		GΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.5 V < V_O < (V+) – 0.5 V, V_S = 24 V	103	111		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, V_S = 24 V, T_A = –40°C to +125°C	96			dB
		(V–) + 1.5 V < V_O < (V+) – 1.5 V, R_L = 225 Ω, V_S = 24 V	96	104		dB
		(V–) + 1.5 V < V_O < (V+) – 1.5 V, R_L = 225 Ω, V_S = 24 V, T_A = –40°C to +125°C	94			dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 24 V		21		MHz
SR	Slew rate	10-V step, gain = +1		50		V/µs
t_S	Settling time	To 0.1%, 10-V step , gain = +1, C_L = 10 pF		0.31		µs
		To 0.1%, 10-V step , gain = –1, C_L = 10 pF		0.40		µs
	Overload recovery time	V_{IN} × gain > V_S		0.28		µs
THD+N	Total harmonic distortion + noise	V_S = 15 V, V_O = 10 Vpp, gain = –1, f = 10 kHz, R_L = 100 Ω		74		dB

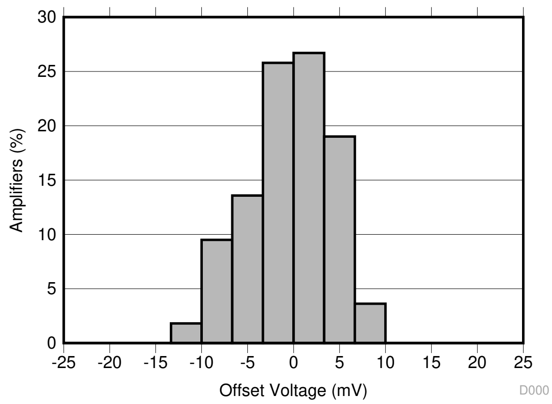
6.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = V+ = 24 V, V– = GND, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	I_{OUT} = ±5 mA		35	60	mV
I_{SC}	Short-circuit current	Sinking		400		mA
		Sourcing		500		
ENABLE						
V_{IH_OTF}	Enable high input voltage		1.2			V
V_{IL_OTF}	Enable low input voltage				0.5	V
	Enable hysteresis			220		mV
t_{OTF/SH_DN}	Enable start-up time			5		μs
POWER SUPPLY						
I_Q	Total quiescent current	I_O = 0 A		3.6	5.5	mA
		I_O = 0 A, T_A = –40°C to +125°C			6	
I_{SD}	Shutdown current	V_{OTF/SH_DN} = 0 V			260	μA
TEMPERATURE						
	Thermal shutdown			172		°C
	Thermal shutdown recovery			150		°C

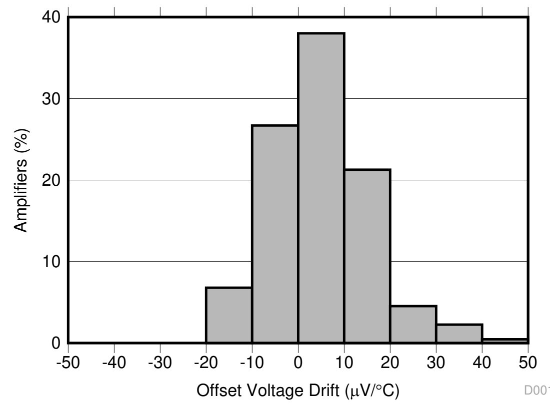
6.6 Typical Characteristics

at T_A= 25°C, V_S = 24 V, V_{CM} = V_S/2, and R_L = 10 kΩ (unless otherwise noted)



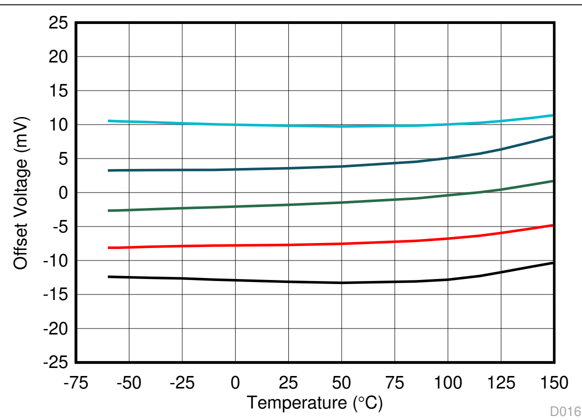
235 channels

Figure 6-1. Offset Voltage Production Distribution



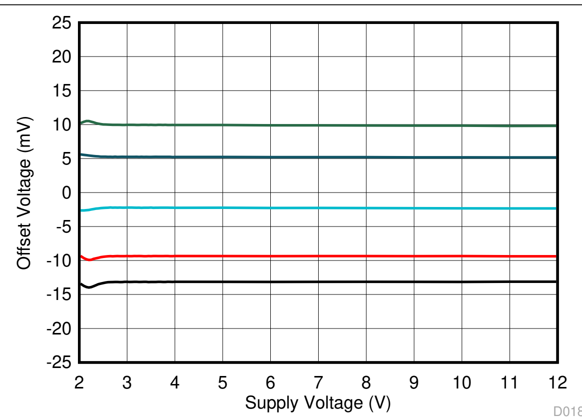
235 channels

Figure 6-2. Offset Voltage Drift Production Distribution



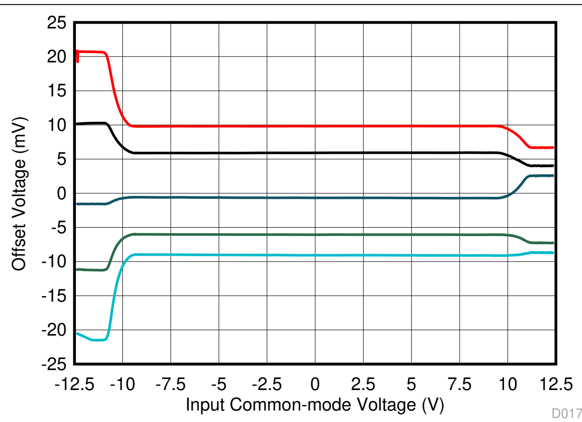
5 typical units

Figure 6-3. Offset voltage vs Temperature



5 typical units

Figure 6-4. Offset Voltage vs Power Supply



5 typical units

Figure 6-5. Offset Voltage vs Input Common-Mode Voltage

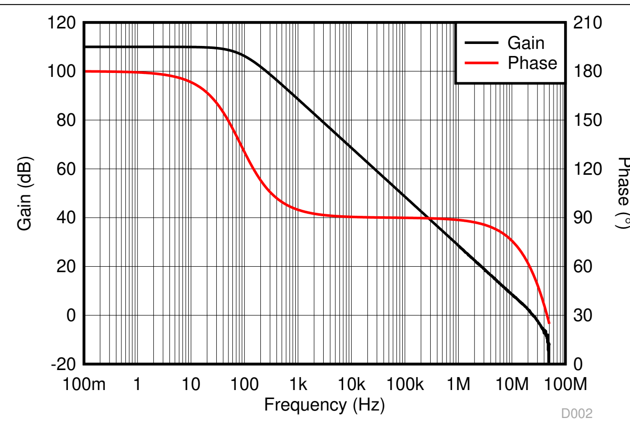
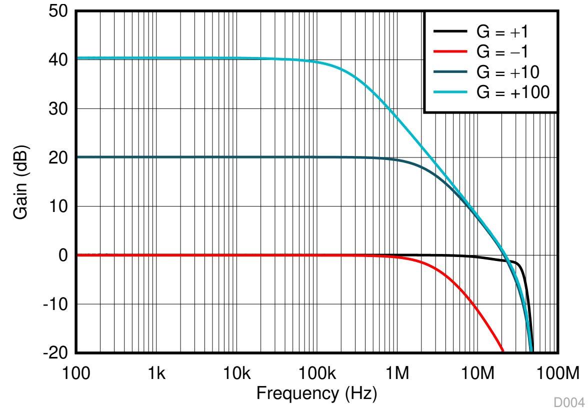


Figure 6-6. Open-Loop Gain and Phase vs Frequency

6.6 Typical Characteristics (continued)

at T_A= 25°C, V_S = 24 V, V_{CM} = V_S/2, and R_L = 10 kΩ (unless otherwise noted)



C_{LOAD} = 200 nF, R_L = 50 Ω

Figure 6-7. Closed-Loop Gain vs Frequency

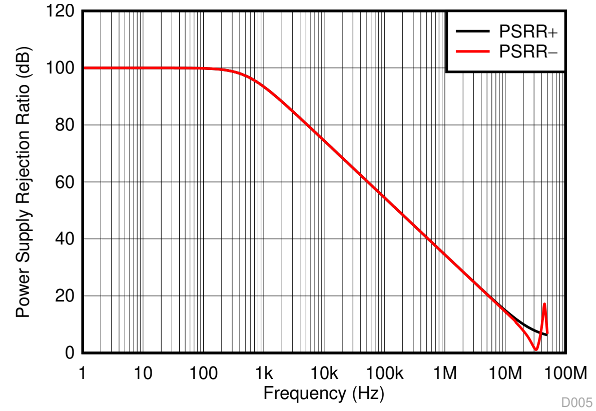


Figure 6-8. PSRR vs Frequency

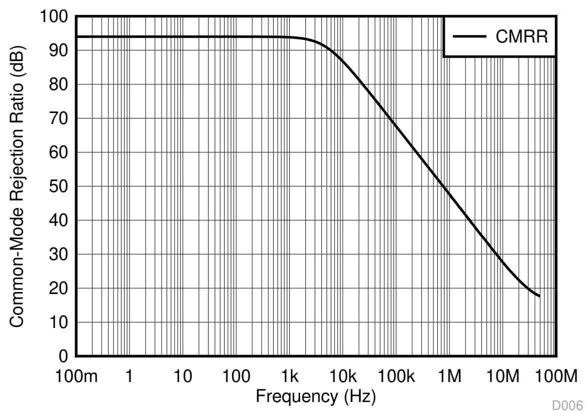
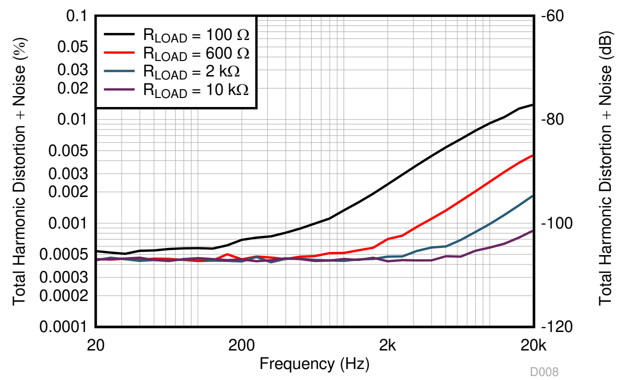
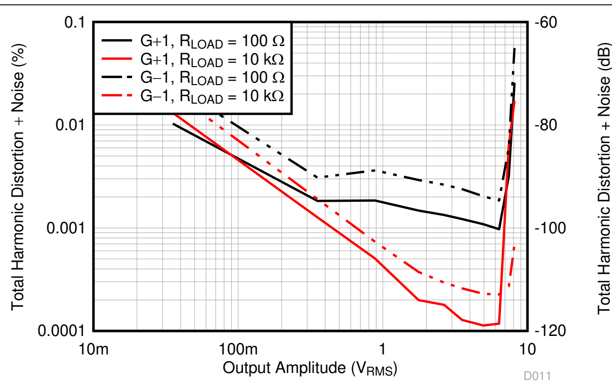


Figure 6-9. CMRR vs Frequency



V_O = 10 V_{PP}, gain = 1 V/V,
measurement bandwidth = 80 kHz

Figure 6-10. THD+N Ratio vs Frequency



Input signal frequency = 1 kHz,
measurement bandwidth = 80 kHz

Figure 6-11. THD+N vs Output Amplitude

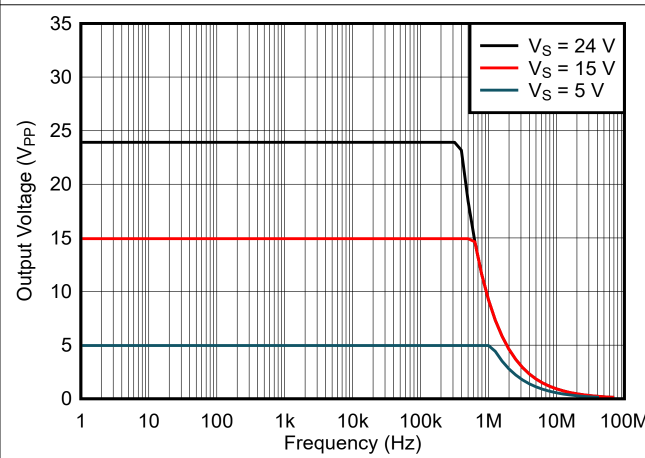


Figure 6-12. Output Voltage vs Frequency

6.6 Typical Characteristics (continued)

at T_A= 25°C, V_S = 24 V, V_{CM} = V_S/2, and R_L = 10 kΩ (unless otherwise noted)

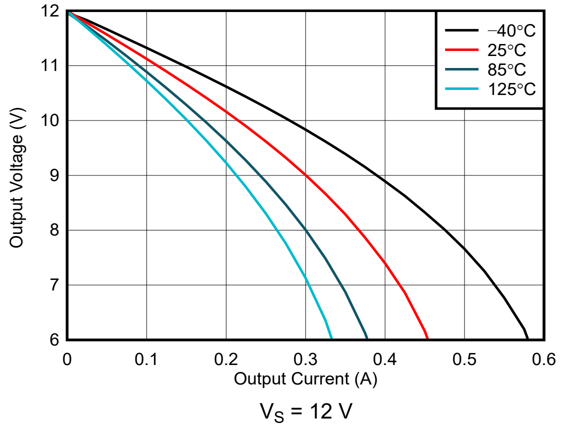


Figure 6-13. Output Voltage Swing vs Output Source Current

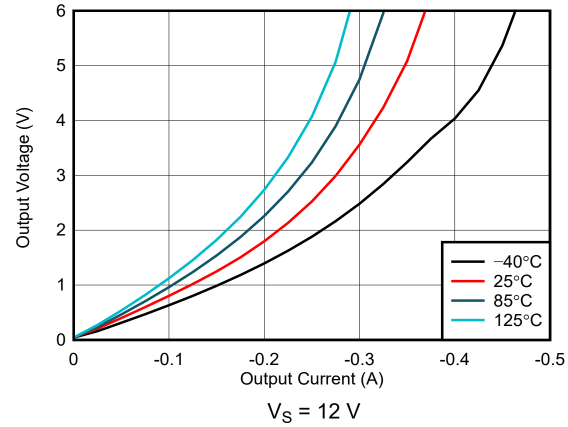


Figure 6-14. Output Voltage Swing vs Output Sink Current

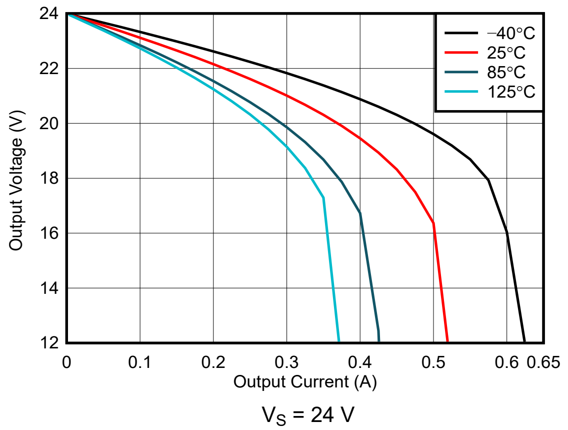


Figure 6-15. Output Voltage Swing vs Output Source Current

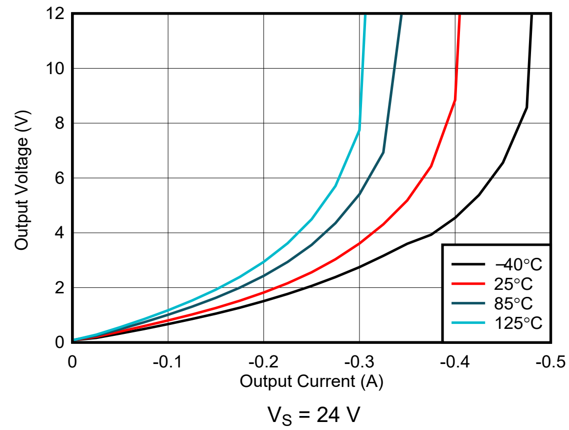


Figure 6-16. Output Voltage Swing vs Output Sink Current

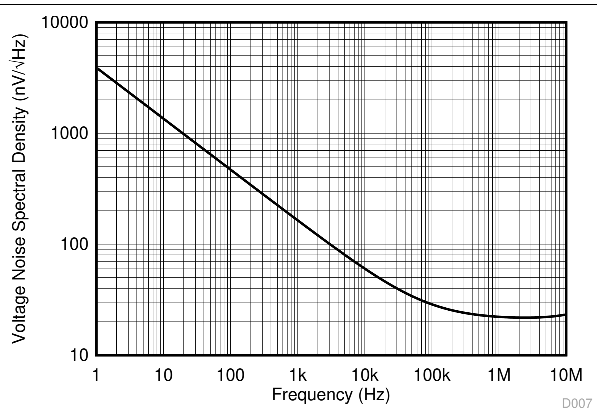


Figure 6-17. Input Voltage Spectral Noise Density vs Frequency

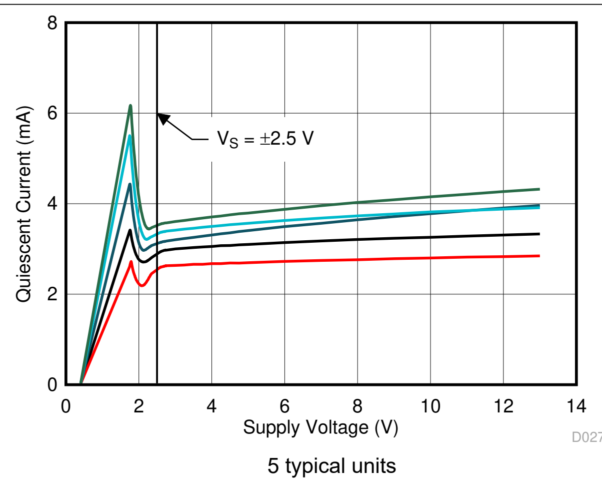
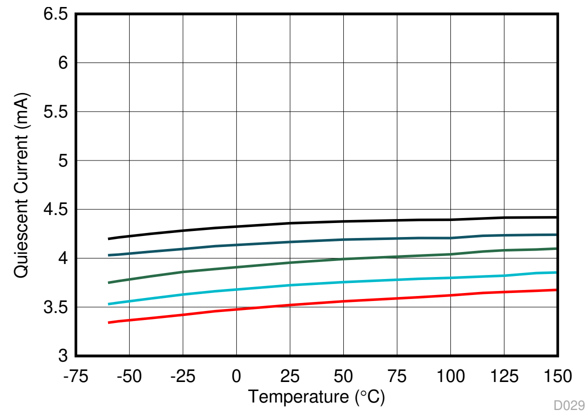


Figure 6-18. Quiescent Current vs Power Supply

6.6 Typical Characteristics (continued)

at T_A= 25°C, V_S = 24 V, V_{CM} = V_S/2, and R_L = 10 kΩ (unless otherwise noted)



5 typical units

Figure 6-19. Quiescent Current vs Temperature

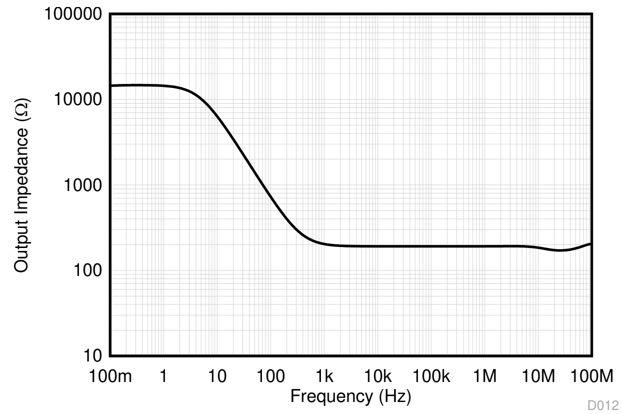
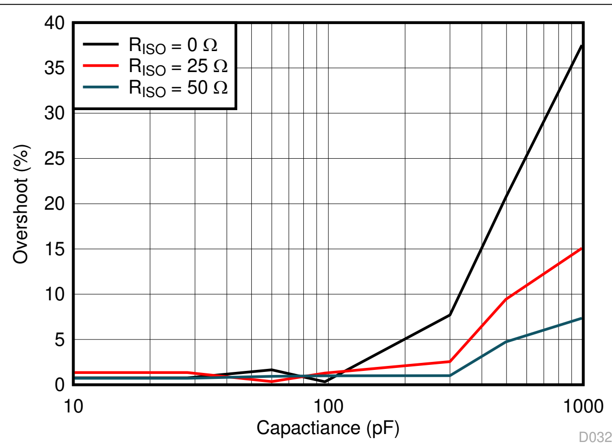
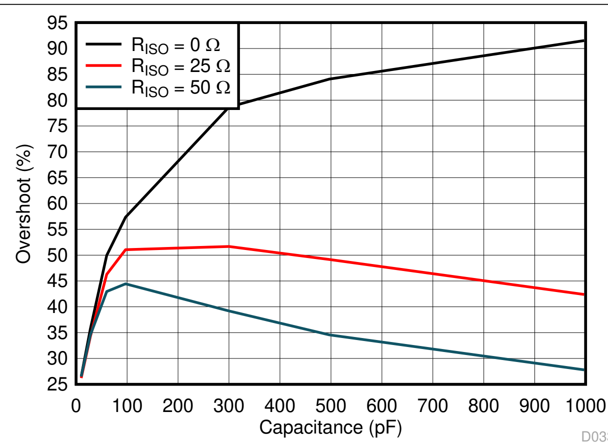


Figure 6-20. Open-Loop Output Impedance vs Frequency



10-mV output step, gain = –1 V/V

Figure 6-21. Small-Signal Overshoot vs Capacitive Load



10-mV output step, gain = 1 V/V

Figure 6-22. Small-Signal Overshoot vs Capacitive Load

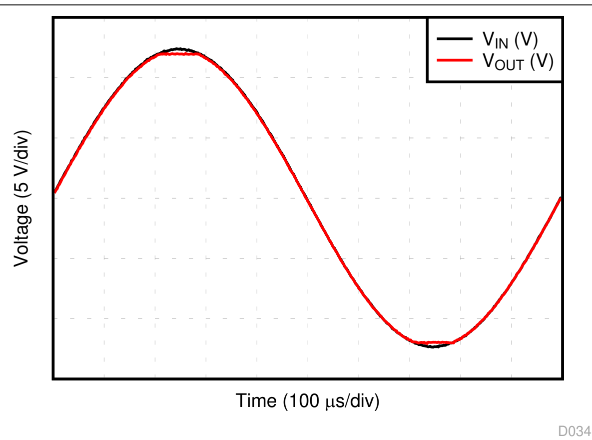
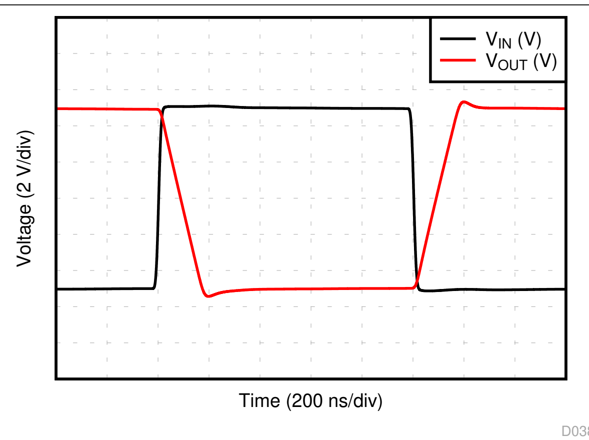


Figure 6-23. No Phase Reversal

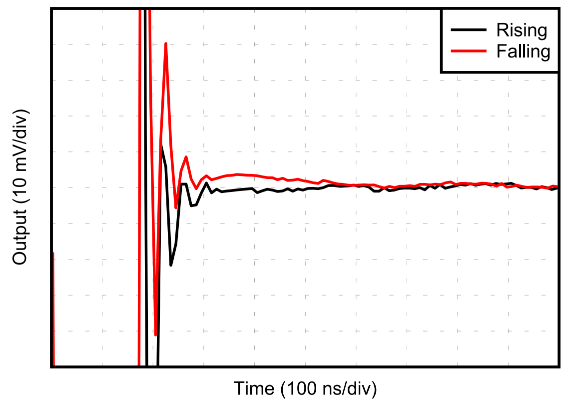


Gain = –1 V/V

Figure 6-24. Large-Signal Step Response

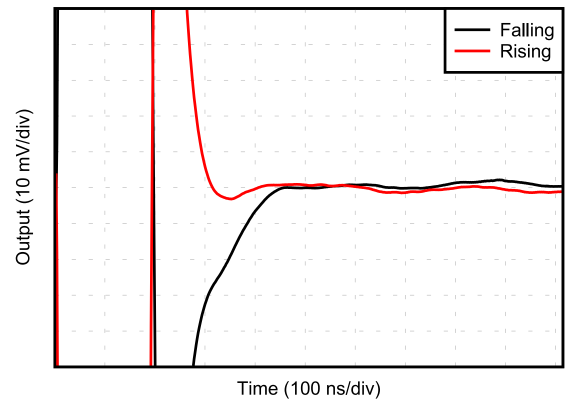
6.6 Typical Characteristics (continued)

at T_A= 25°C, V_S = 24 V, V_{CM} = V_S/2, and R_L = 10 kΩ (unless otherwise noted)



G = 1 V/V, V_{IN} = 10 V_{PP}

Figure 6-25. Settling Time



G = –1 V/V, V_{IN} = 10 V_{PP}

Figure 6-26. Settling Time

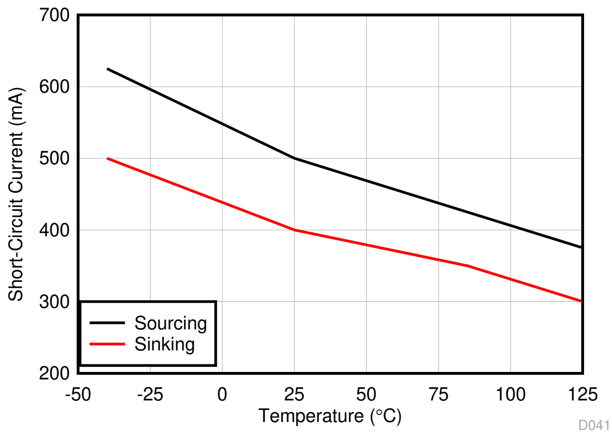
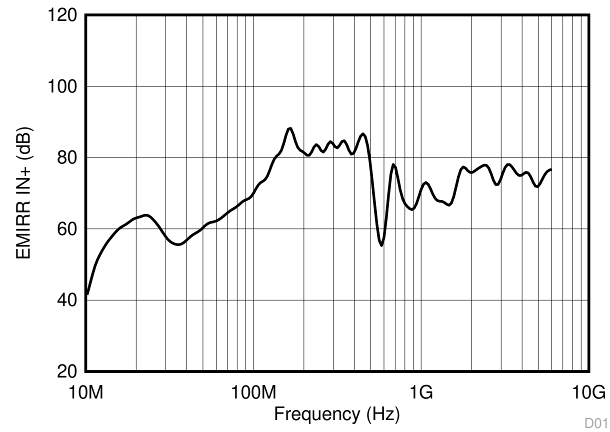


Figure 6-27. Short-Circuit Current vs Temperature



P_{RF_PEAK} = –10 dBm

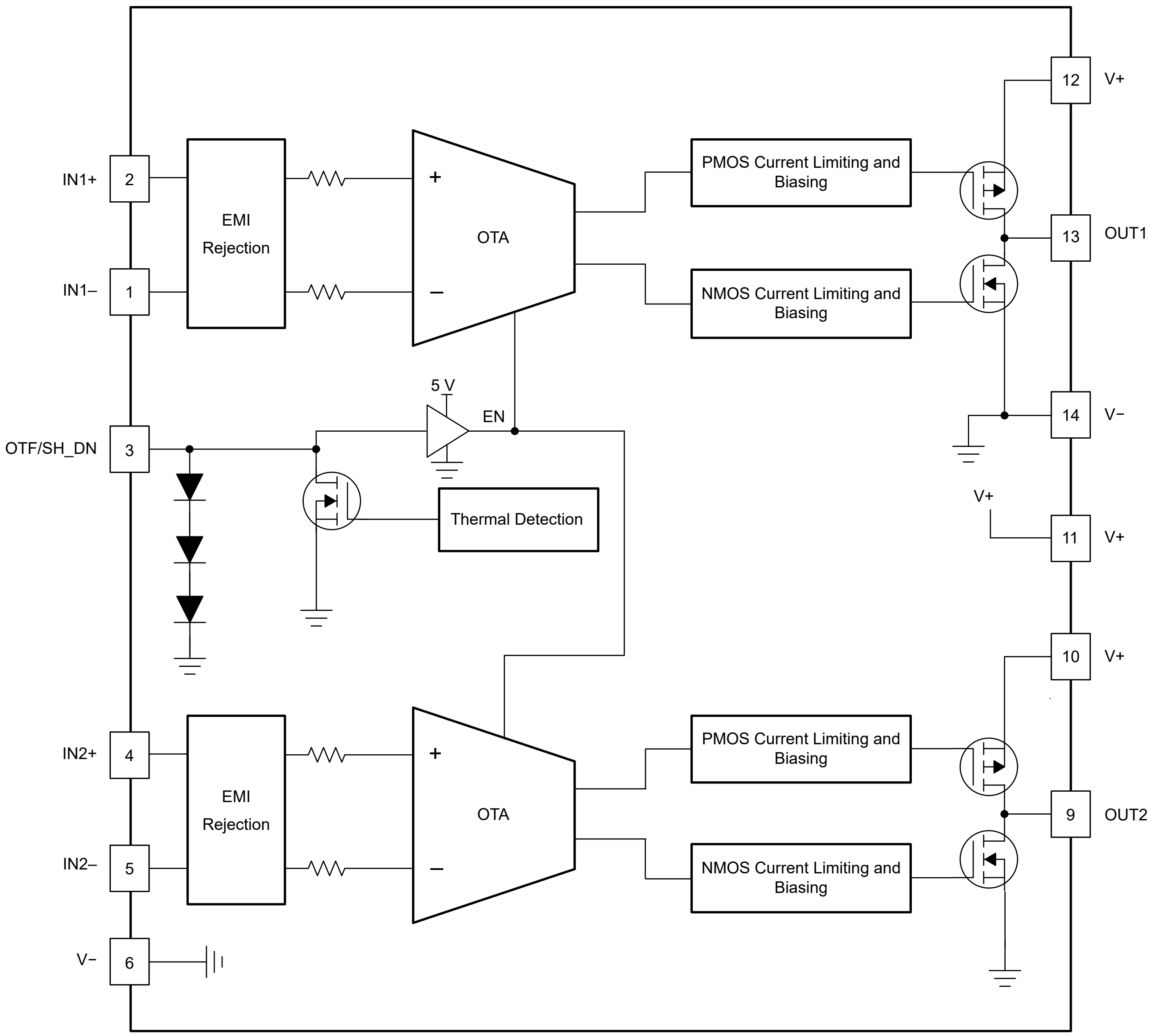
Figure 6-28. EMIRR vs Frequency

7 Detailed Description

7.1 Overview

The ALM2403-Q1 is a dual-power op amp qualified for use in automotive applications. Key features for this device are low offset voltage, high output current drive capability, and high FPBW capability. The device also offers protection features such as thermal shutdown and current limit. The 14-pin HTSSOP package minimizes board space and power dissipation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Overtemperature and Shutdown Pin (OTF/SH_DN)

The overtemperature and shutdown pin, OTF/SH_DN, is bidirectional and allows both op amps to be put into a low I_Q state (approximately 200 µA per amplifier) when forced low or to less than V_{IL_OTF}. As a result of being bidirectional, and the respective enable and disable functionality, this pin must be pulled high or greater than V_{IH_OTF} through a pullup resistor. The use of a 10-kΩ pullup resistor leads to a drive current of approximately 210 µA when used with a pullup voltage of 3.3 V.

When the junction temperature of the ALM2403-Q1 exceeds the specified limits, OTF/SH_DN goes low to alert the application that both the outputs have turned off because of an overtemperature event.

When OTF/SH_DN is pulled low and the op amps are shut down, the op amps are in an open loop, even when there is negative feedback applied. This occurrence is due to the loss of the open-loop gain in the op amps when the biasing is disabled.

7.3.2 Thermal Shutdown

If the die temperature exceeds safe limits, all outputs are disabled, and the OTF/SH_DN pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The OTF/SH_DN pin is released after operation has resumed.

When operating the die at a high temperature, the op amp toggles on and off between the thermal shutdown hysteresis. In this event, the safe limits for the die temperature must be taken in to account. Do not continuously operate the device in thermal hysteresis for long periods of time.

7.3.3 Current-Limit and Short-Circuit Protection

Each op amp in the ALM2403-Q1 has separate internal current limiting for the PMOS (high-side) and NMOS (low-side) output transistors. If the output is shorted to ground, then the PMOS (high-side) current limit is activated, and limits the current to 500 mA nominally. If the output is shorted to supply, then the NMOS (low-side) current limit is activated and limits the current to 400 mA nominally at 25°C. The current limit value is inversely proportional to temperature; therefore, the current limit value increases at low temperatures.

When current is limited, the safe limits for the die temperature must be taken in to account. With too much power dissipation, the die temperature can surpass thermal shutdown limits; the op amp shuts down and reactivates after the die has fallen below thermal limits.

CAUTION

Do not continuously operate the device in thermal hysteresis for long periods of time because this action may cause irreversible damage to the device.

7.3.4 Input Common-Mode Range

The input common-mode range of the ALM2403-Q1 is between (V–) – 0.2 V and (V+) + 0.2 V. Staying within this range allows the op amps to perform and operate within specification. Operating beyond these limits can cause distortion and nonlinearities.

7.3.5 Reverse Body Diodes in Output-Stage Transistors

Designed as a high-voltage, high current operational amplifier, the ALM2403-Q1 delivers robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. Different load conditions change the ability of the amplifier to swing close to the rails.

Each output transistor has internal reverse diodes between drain and source that conduct if the output is forced to greater than the supply or less than ground (reverse current flow). These diodes can be used as flyback protection in inductive-load-driving applications. Limit the use of these diodes to pulsed operation in order to minimize junction temperature overheating due to ($V_F \times I_F$). Internal current-limiting circuitry does not operate when current is flown in the reverse direction and the reverse diodes are active. A method to protect these reverse body diodes is shown in Section 8.2.2.1.2.

7.3.6 EMI Filtering

Op amps vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op-amp pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The ALM2403-Q1 incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 990 MHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

7.4 Device Functional Modes

7.4.1 Open-Loop and Closed-Loop Operation

As a result of the very-high, open-loop dc gain of the ALM2403-Q1, the device functions as a comparator in open loop for most applications. A majority of electrical characteristics are verified in negative feedback, closed-loop configurations. Certain dc electrical characteristics, like offset, may have a higher drift across temperature and lifetime when continuously operated in open loop over the lifetime of the device.

7.4.2 Shutdown

When the OTF/SH_DN pin is left floating or is grounded, the op amp shuts down to a low I_Q state and does not operate; the op amp outputs go to a high-impedance state.

Table 7-1. Shutdown Truth Table

PIN NAME	LOGIC STATE	OP AMP STATE
OTF/SH_DN	High (> VIH_OTF)	Operating
	Low (< VIL_OTF)	Shutdown (low I_Q state)

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ALM2403-Q1 is a dual-power op amp with performance and protection features that are optimal for many applications. For op amps, there are many general design consideration that must be taken into account. The following subsections describe what to consider for most closed-loop applications. Section 8.2 gives a specific example of the ALM2403-Q1 being used in a resolver application.

8.1.1 Capacitive Load and Stability

The ALM2403-Q1 is designed for applications where driving a capacitive load is required. As with all op amps, specific instances can occur where the ALM2403-Q1 device can become unstable. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op amp in a unity-gain (1-V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to become unstable compared to an amplifier operated at a higher-noise gain. The capacitive load, in conjunction with the op-amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in a unity-gain configuration, the ALM2403-Q1 remains stable with a pure capacitive load up to approximately 30 pF. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (R_S; typically, 100 mΩ to 10 Ω) in series with the output, as shown in Figure 8-1. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads.

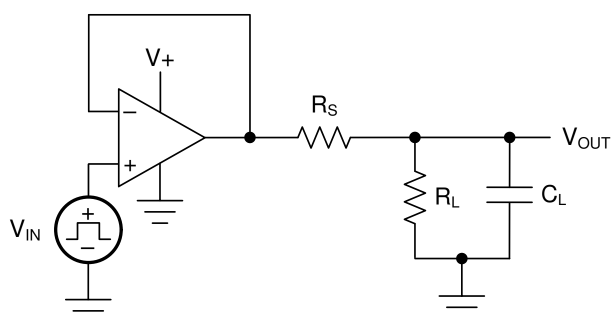


Figure 8-1. Capacitive Load Drive

8.2 Typical Application

High-power ac and brushless dc (BLDC) motor-drive applications need position feedback to efficiently and accurately drive the motor. Position feedback can be achieved by using optical encoders, hall sensors, or resolvers. Resolvers are the main choice when environmental or longevity requirements are challenging and extensive.

A resolver acts as a transformer with one primary coil and two secondary coils. The primary coil, or excitation coil, is located on the rotor of the resolver. As the rotor of the resolver spins, the excitation coil induces a current into the sine and cosine sensing coils. These coils are oriented 90 degrees from one another, and the voltage from the sine and cosine coils is translated into a vector position by the microcontroller or resolver-to-digital converter chip.

Resolver excitation coils can have a very low dc resistance (< 100 Ω), requiring a sink and a source of up to 200 mA from the excitation driver. The ALM2403-Q1 can source and sink this current while providing current-limiting and thermal-shutdown protection. Incorporating these protections in a resolver design can increase the life of the end product.

The input to the ALM2403-Q1 can be an analog sine wave generated by the resolver-to-digital converter chip or a pulse-width modulation (PWM) signal generated from a microcontroller I/O pin. In the case of the latter, a filter stage is needed to extract a lower bandwidth sine wave from the PWM signal. This sine wave would then be the input signal to the ALM2403-Q1. As a result of high gain bandwidth, the ALM2403-Q1 can be configured as a filter stage while providing the required output drive. This configuration significantly reduces the total solution size and design complexity of the resolver-drive signal chain. The fundamental design steps to achieve this functionality are shown in this application example, and can be applied to other inductive-load applications as well.

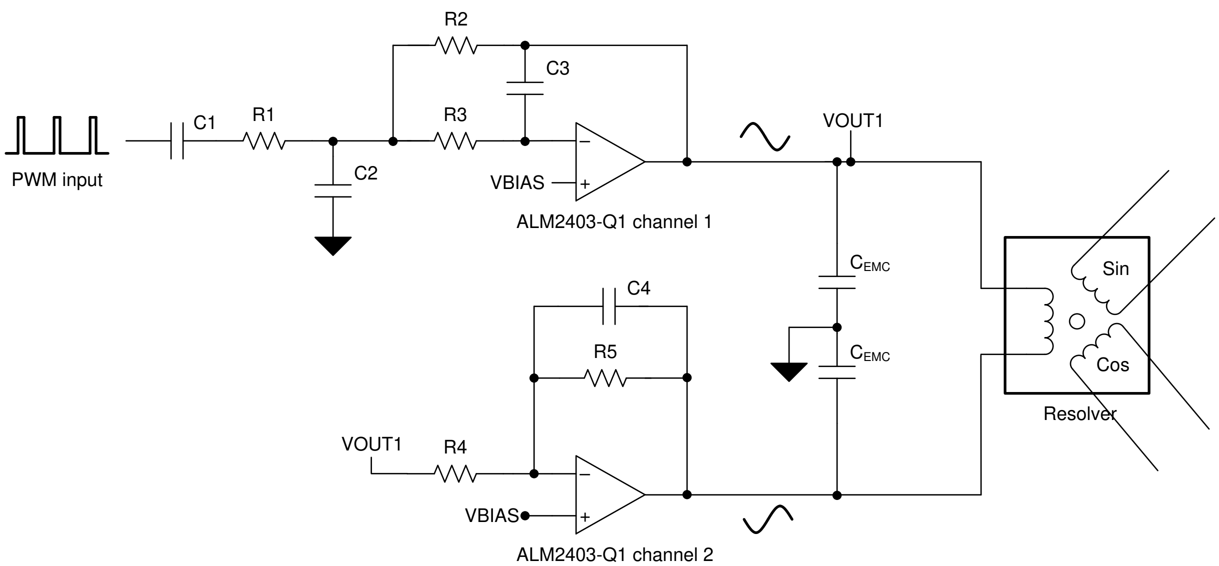


Figure 8-2. Resolver-Based Application

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Ambient temperature range	–40°C to +125°C
Available supply voltages	15 V
EMC capacitance (CL)	10 nF
Resolver excitation input voltage	7 V_{RMS}
Excitation frequency	10 kHz
PWM signal frequency	320 kHz
PWM signal amplitude	3.3 V
Functional safety capable	Yes
Short-to-battery protection	Yes

8.2.2 Detailed Design Procedure

When using the ALM2403-Q1 in a resolver application, determine:

- Resolver excitation input impedance or resistance and inductance: Z_O = 100 + j188, R = 100 Ω, and L = 3 mH at 10 kHz
- Resolver transformation ratio (V_{SINCOS} / V_{EXC}): 0.5 V/V at 10 kHz
- Package and $R_{\theta JA}$: HTSSOP, 46.9°C/W
- Op amp maximum junction temperature: 150°C
- Op amp bandwidth: 21 MHz
- Op amp slew rate: 50 V/µS

8.2.2.1 Resolver Excitation Amplifier Combined With MFB 2nd-Order, Low-Pass Filter

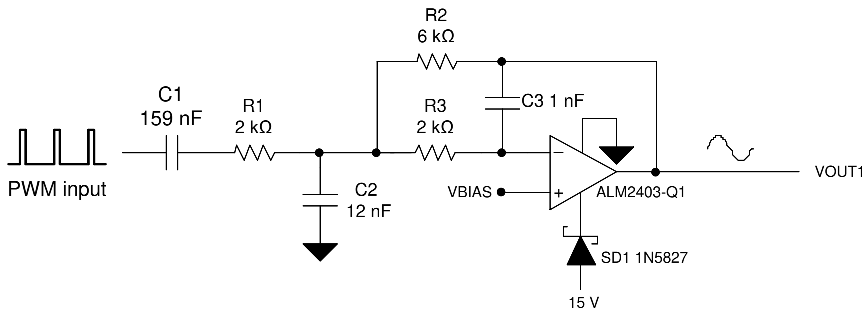


Figure 8-3. Two-Pole MFB Filter

When designing a low-pass filter, the most important design criteria is to decide the corner frequency. In this design example, the resolver excitation frequency is 10 kHz and PWM frequency is 320 kHz. Thus, we want to make sure that the low-pass filter corner frequency is greater than 10 kHz, and there is maximum attenuation of harmonic interference generated from the PWM signal. Figure 8-3 shows a single channel of the ALM2403-Q1 configured as a 2-pole multiple feedback (MFB) filter with a –40 dB/decade rolloff. The MFB topology enables a steep rolloff while reducing BOM count. The output from this circuit is a sine wave that can then be inverted using the second channel of the ALM2403-Q1; see Figure 8-2. Thus, both ALM2403-Q1 channels combined provide the required resolver excitation signal.

8.2.2.1.1 Filter Design

The corner frequency of the 2nd-order MFB filter is set to approximately twenty times less than the PWM frequency. The corner frequency defined at –3 dB is shown in Equation 1.

$$f_p = \frac{1}{2 \times \pi \times \sqrt{R_3 \times C_3 \times R_2 \times C_2}} \tag{1}$$

The 2nd-order MFB active filter uses an inverted input topology and the op amp gain is determined by the ratios of resistors R2 and R1:

$$\text{Gain} = -\frac{R_2}{R_1} \tag{2}$$

The gain settings are based on the output drive requirements and PWM signal amplitude. With different gain settings, the filter characteristics, such as rolloff, can change. The design must be fine-tuned to meet optimal performance needs.

The quality (Q) factor of the low-pass filter is configured with Q = 1. The purpose of designing for this Q factor is to minimize attenuation around the corner frequency of 10 kHz, thus extending the pass-band gain. The Q factor of the 2nd-order MFB filter is given by Equation 3:

$$Q = \frac{\sqrt{C_2 / C_3}}{\sqrt{R_3 / R_2} + \sqrt{R_2 / R_3} + \sqrt{R_3 \times R_2 / R_1}} \tag{3}$$

8.2.2.1.2 Short-to-Battery Protection

Resolver-based applications require the power op amp stage to provide the resolver excitation signal over long cables. In many applications, such as automotive traction inverters, the cables are housed in a harness and a short-circuit condition between different cables in the same harness can occur. In this situation, the output of the ALM2403-Q1 can see a higher voltage than provided at the positive supply pin. This condition causes the body diode in the output stage PMOS to become forward-biased and start conducting. As a precaution, use a blocking diode in series with the positive power supply; see also Figure 8-3.

For related information, see the *ALM2403-Q1 Overvoltage Protection of Resolver-Based Circuits* application note.

8.2.2.2 Power Dissipation and Thermal Reliability

Power dissipation is critical to many industrial and automotive applications. Resolvers are typically chosen over other position feedback techniques because of reliability and accuracy in harsh conditions and high temperatures.

The ALM2403-Q1 is capable of high output current with power-supply voltages up to 24 V. Internal power dissipation increases when operating at high supply voltages. The power dissipated in the op amp (P_{OPA}) is calculated using Equation 4:

$$P_{OPA} = (V_S - V_{OUT}) \times I_{OUT} = (V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L} \tag{4}$$

To calculate the worst-case power dissipation in the op amp, the ac and dc cases must be considered separately.

In the case of constant output current (dc) to a resistive load, the maximum power dissipation in the op amp occurs when the output voltage is half the positive supply voltage. This calculation assumes that the op amp is sourcing current from the positive supply to a grounded load. If the op amp sinks current from a grounded load, modify Equation 5 to include the negative supply voltage instead of the positive.

$$P_{OPA(MAX\_DC)} = P_{OPA}\left(\frac{V_S}{2}\right) = \frac{(V_S)^2}{4 \times R_L} \tag{5}$$

The ac maximum of average power dissipation in the op amp for a sinusoidal output current (ac) to a resistive load occurs when the peak output voltage is 2/π times the supply voltage, given symmetrical supply voltages, as shown in Equation 6:

$$P_{OPA(PEAK\_AC)} = P_{OPA}\left(\frac{2 \times V_S}{\pi}\right) = \frac{2 \times (V_S)^2}{\pi^2 \times R_L} \tag{6}$$

After the total power dissipation is determined, the junction temperature at the worst expected ambient temperature case must be determined by using Equation 7:

$$T_{J(MAX)} = P_{OPA} \times R_{\theta JA} + T_{A(MAX)} \tag{7}$$

8.2.2.2.1 Improving Package Thermal Performance

The value of $R_{\theta JA}$ depends on the printed circuit board (PCB) layout. An external heat sink, a cooling mechanism such as a cold air fan, or both, can help reduce $R_{\theta JA}$, and thus improve device thermal capabilities. See TI's design support web page at www.ti.com/thermal for general guidance on improving device thermal performance.

8.2.3 Application Curves

The roll of characteristics and output waveform for the designed MFB filter are shown in Figure 8-4 and Figure 8-5. The attenuation is specified in Table 8-2.

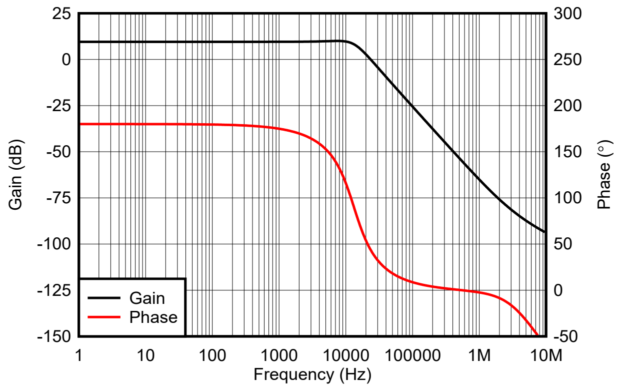


Figure 8-4. 2nd-Order MFB LP Filter AC Output Characteristics

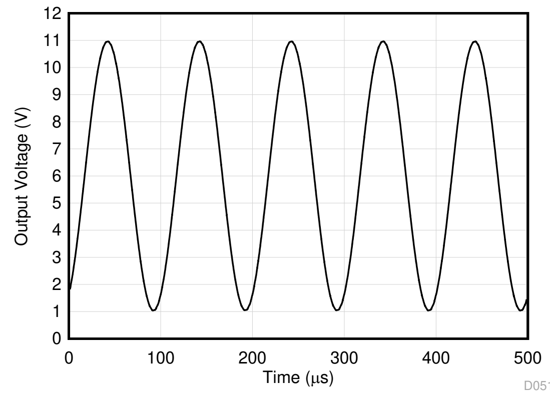


Figure 8-5. 2nd-Order MFB LP Filter DC Output

Table 8-2. Signal Attenuation vs Frequency

2ND-ORDER MFB LPF FREQUENCY (kHz)	ATTENUATION (dB)
DC	9.54
10.0	9.70
15.4	6.54
19	3.54
30	–4.38
320	–45.9

8.3 Power Supply Recommendations

The ALM2403-Q1 is recommended for continuous operation from 5 V to 24 V (±2.5 V to ±12 V) for V_S, and many specifications apply from –40°C to +125°C.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling from noisy or high-impedance power supplies.

CAUTION

Supply voltages larger than 26 V can permanently damage the device (see *Section 6.1*).

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes.

A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.

- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If keeping the traces separate is not possible, then cross the sensitive trace perpendicular, as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

8.4.2 Layout Example

This layout does not verify optimum thermal impedance performance. See TI's design support web page at www.ti.com/thermal for general guidance on improving device thermal performance.

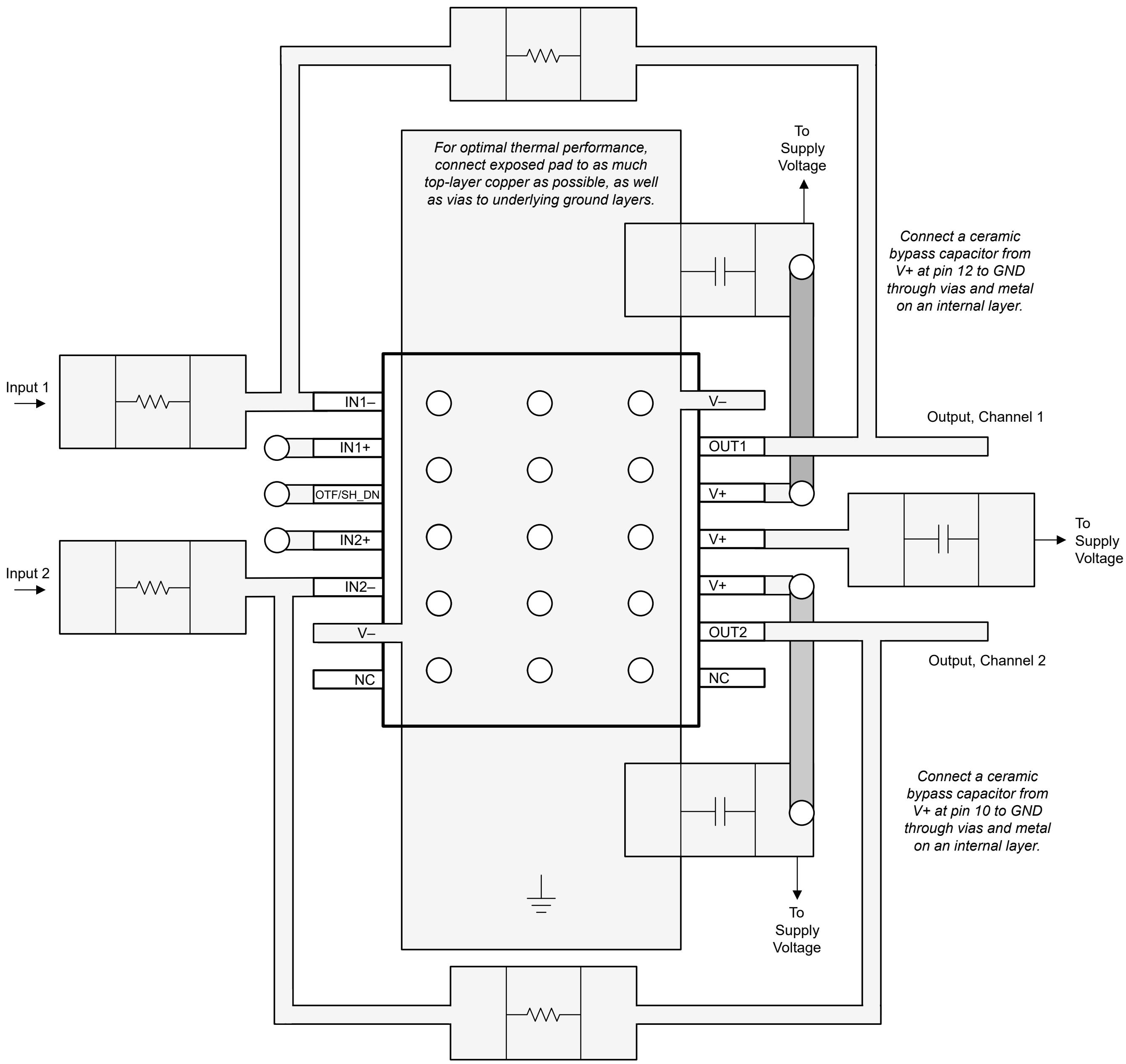


Figure 8-6. ALM2403-Q1 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following: ALM2403-Q1 Evaluation Module user's guide.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ALM2403QPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	A2403Q
ALM2403QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	A2403Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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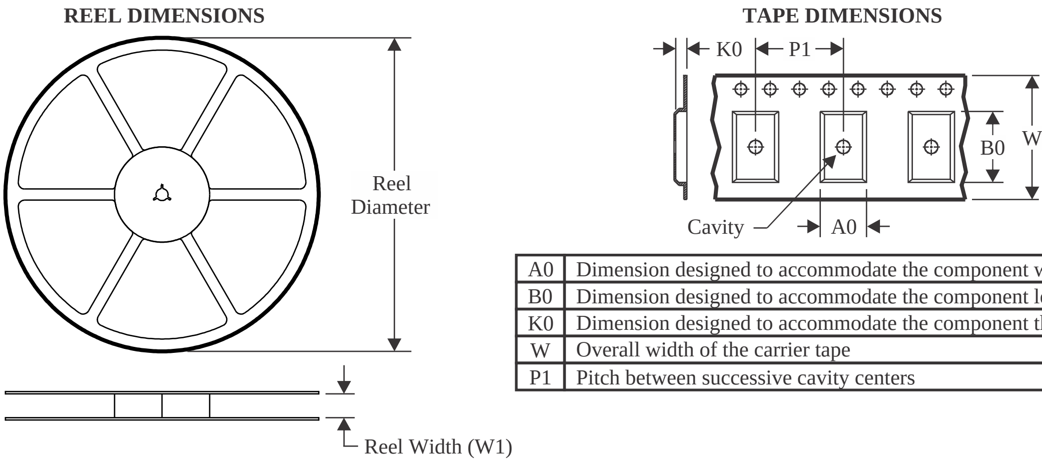
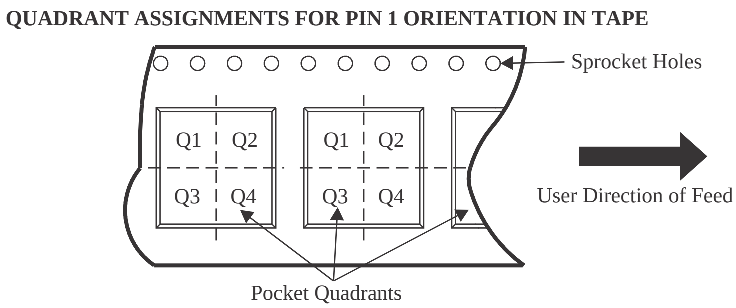
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



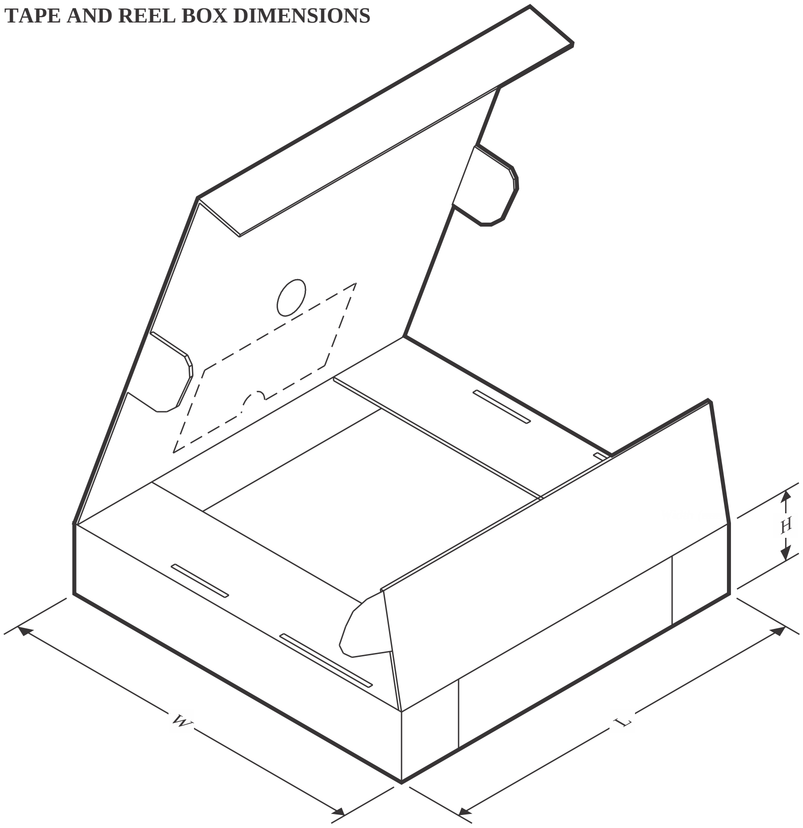
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ALM2403QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ALM2403QPWPRQ1	HTSSOP	PWP	14	2000	353.0	353.0	32.0

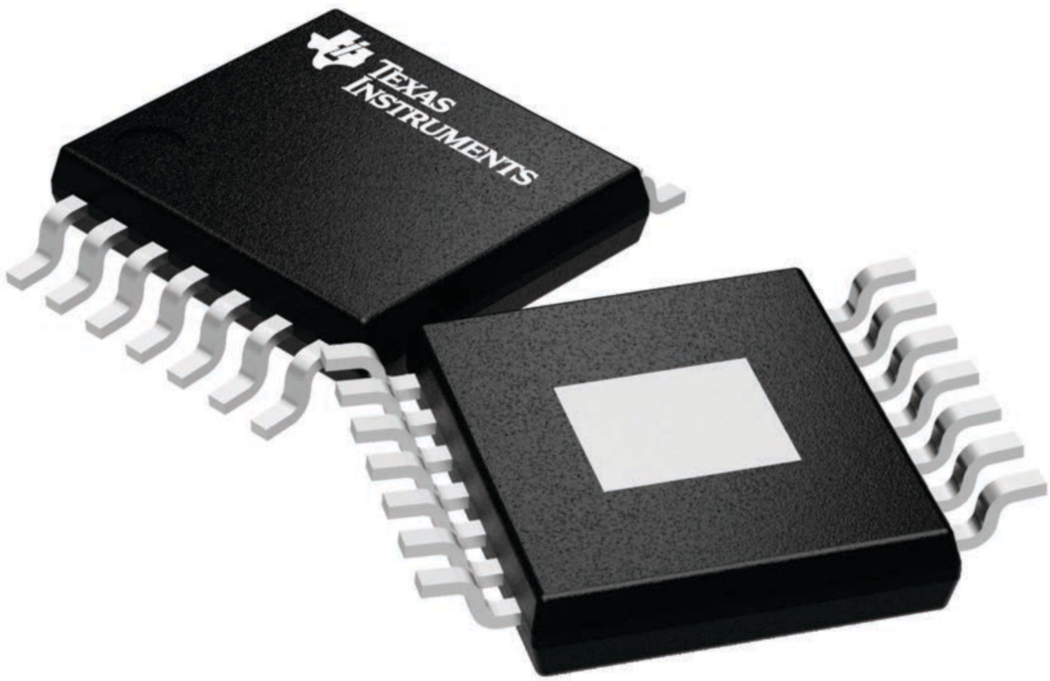
PWP 14

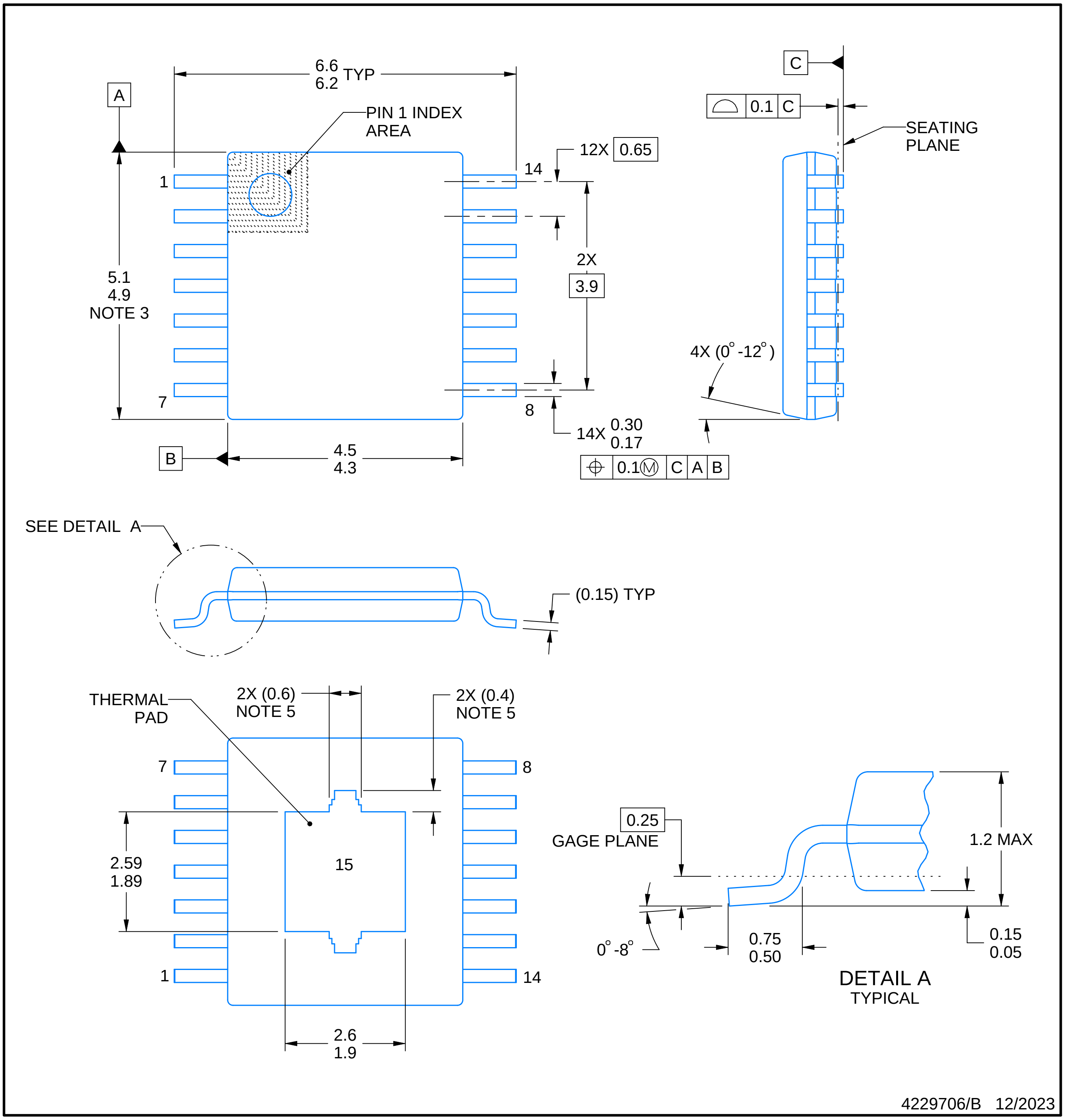
PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

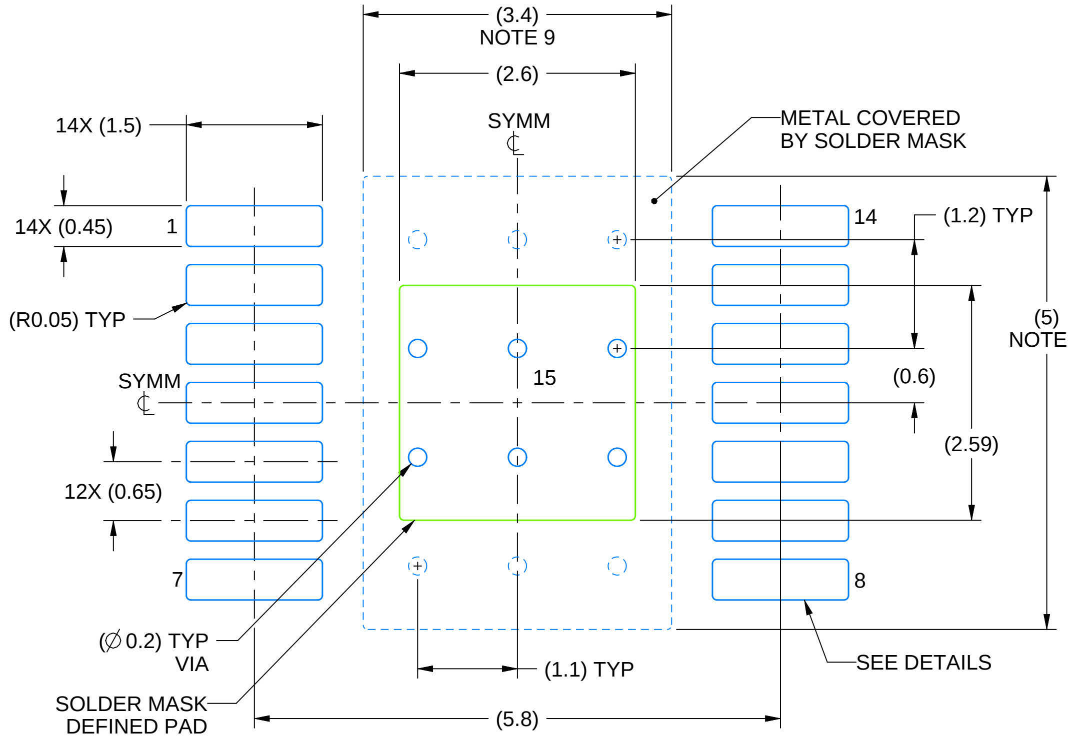




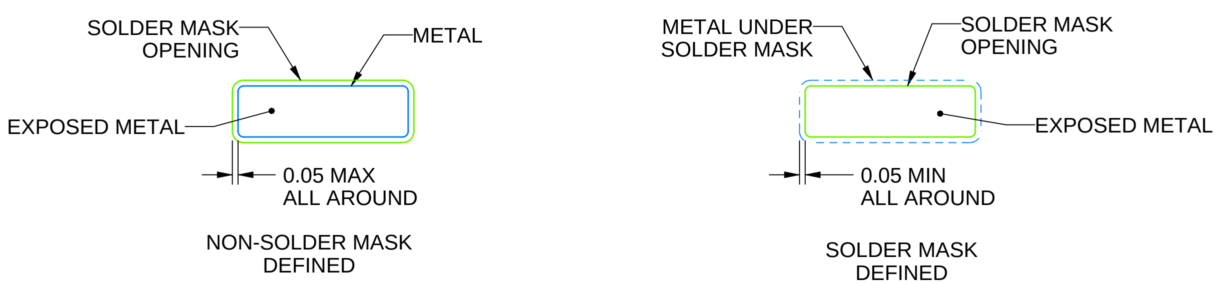
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

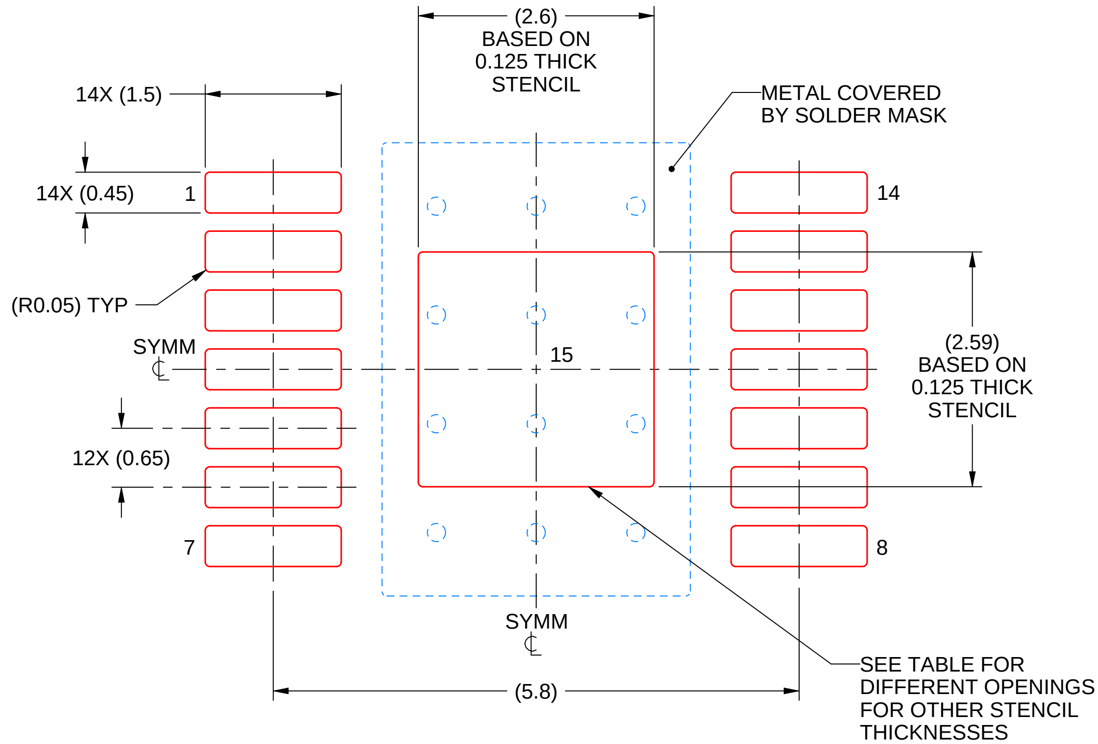


SOLDER MASK DETAILS

4229706/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.