

# AFE7950 4T6R RF Sampling AFE with 12GSPS DACs and 3GSPS ADCs

## 1 Features

- [Request full data sheet](#)
- Quad RF sampling 12GSPS transmit DACs
- Quad RF sampling 3GSPS receive ADCs
- Dual RF sampling 3GSPS feedback (auxilliary RX) ADCs
- Maximum RF signal bandwidth:
  - 4TX or 2FB: 1200MHz or 2TX: 2400MHz
  - RX: 1200MHz (no FB), 600MHz (with FB)
- RF frequency range:
  - TX: 600MHz - 12GHz
  - RX/FB: 600MHz -12GHz
- Digital step attenuators (DSA):
  - TX: 40dB range, 0.125dB steps
  - RX or FB: 25dB range, 0.5dB steps
- Single or dual-band DUC or DDCs for TX and RX
- 16x NCOs per TX or RX and FB
- Optional Internal PLL or VCO for DAC or ADC clocks or external clock at DAC or ADC sample rate
- SerDes data interface:
  - JESD204B and JESD204C compatible
  - 8 SerDes transceivers up to 29.5Gbps
  - Subclass 1 multi-device synchronization
- Package: 17mm × 17mm FCBGA, 0.8mm pitch

## 2 Applications

- [Radar](#)
- [Seeker front end](#)
- [Defense radio](#)
- Tactical communications infrastructure
- [Wireless communications test](#)

## 3 Description

The AFE7950 is a high performance, wide bandwidth multi-channel transceiver, integrating four RF sampling transmitter chains, four RF sampling receiver chains and two RF sampling feedback chains (six RF sampling ADCs total). With operation up to 12 GHz, this device enables direct RF sampling in the L, S, C and X-band frequency ranges without the need for additional frequency conversions stages. This improvement in density and flexibility enables high-channel-count, multi-mission systems.

The TX signal paths support interpolation and digital up conversion options that deliver up to 1200MHz of signal bandwidth for four TX or 2400MHz for two TX. The output of the DUCs drives a 12GSPS DAC (digital to analog converter) with a mixed mode output option to enhance 2nd Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40-dB range and 1dB analog and 0.125dB digital steps.

Each receiver chain includes a 25dB range DSA (Digital Step Attenuator), followed by a 3GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. Flexible decimation options provide optimization of data bandwidth up to 1200MHz for four RX without FB paths or 600MHz with two FB paths (1200MHz BW each).

### Package Information

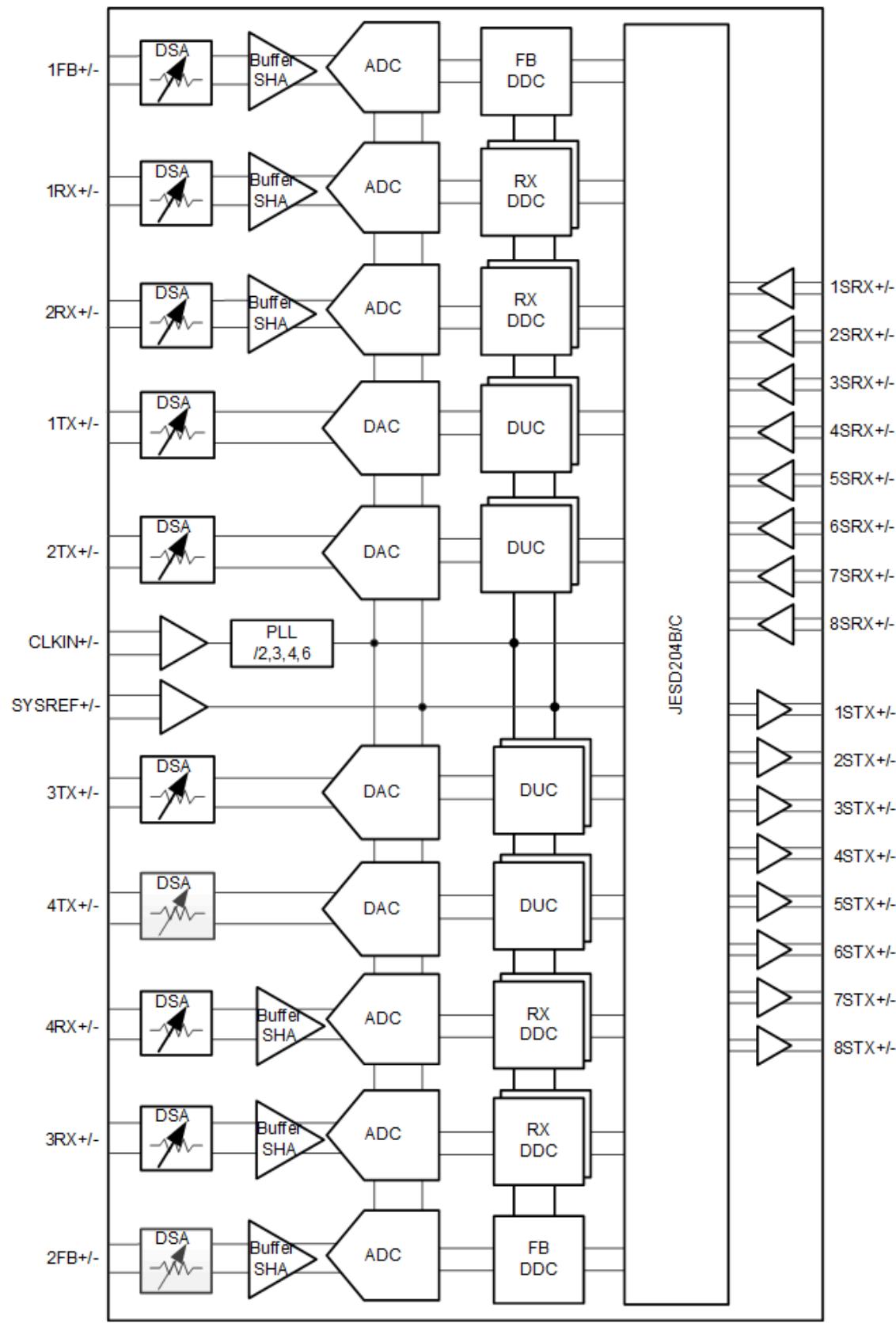
PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
AFE7950	FC-BGA	17mm × 17mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

**Functional Block Diagram**

## Table of Contents

<b>1 Features.....</b>	<b>1</b>	4.9 Power Supply Electrical Characteristics.....	<b>21</b>
<b>2 Applications.....</b>	<b>1</b>	4.10 Timing Requirements.....	<b>27</b>
<b>3 Description.....</b>	<b>1</b>	4.11 Switching Characteristics.....	<b>28</b>
<b>4 Specifications.....</b>	<b>4</b>	4.12 Typical Characteristics.....	<b>29</b>
4.1 Absolute Maximum Ratings.....	4	<b>5 Revision History.....</b>	<b>134</b>
4.2 ESD Ratings.....	5	<b>6 Device and Documentation Support.....</b>	<b>136</b>
4.3 Recommended Operating Conditions.....	6	6.1 Receiving Notification of Documentation Updates..	<b>136</b>
4.4 Thermal Information.....	6	6.2 Support Resources.....	<b>136</b>
4.5 Transmitter Electrical Characteristics.....	7	6.3 Trademarks.....	<b>136</b>
4.6 RF ADC Electrical Characteristics.....	14	6.4 Electrostatic Discharge Caution.....	<b>136</b>
4.7 PLL/VCO/Clock Electrical Characteristics.....	18	6.5 Glossary.....	<b>136</b>
4.8 Digital Electrical Characteristics.....	20	<b>7 Mechanical, Packaging, and Orderable Information</b>	<b>136</b>

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	-0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	-0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVCO, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	-0.5	2.1	V
Pin Voltage Range	{1/2/3/4}RXIN+/-	-0.5	VDDRX1P8+0.3	V
	1FBIN+/-, 2FB+/-	-0.5	VDDFB1P8+0.3	V
	{1/2/3/4}TXOUT+/-	-0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	-0.3	1.4	V
	{1:8}SRX+/-	-0.3	1.4	V
	{1:8}STX+/-	-0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	-0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	-0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	-0.3	VDDA1P8+0.3	V
$P_{MAX}(xRXIN+/-)$	Peak differential RF input power at device pins, $f_{IN}$ = 830 MHz, DSA = 20dB		16.7	dBm
	Peak differential RF input power at device pins, $f_{IN}$ = 1760 MHz, DSA = 20dB		17.0	dBm
	Peak differential RF input power at device pins, $f_{IN}$ = 2610 MHz, DSA = 20dB		18	dBm
	Peak differential RF input power at device pins, $f_{IN}$ = 3610 MHz, DSA = 20dB		18.5	dBm
	Peak differential RF input power at device pins, $f_{IN}$ = 4910 MHz, DSA = 20dB		19.3	dBm
	Peak differential RF input power at device pins, $f_{IN}$ = 8150 MHz, DSA = 20dB		21.3	dBm
	Peak differential RF input power at device pins, $f_{IN}$ = 9610 MHz, DSA = 20dB		23.5	dBm
Peak Input Current	any input		20	mA
$T_J$	Junction temperature		150	°C
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 4.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	1000
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins	150

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/TXENC/PLL/PLLVCO/FB/FBCLK/GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T <sub>A</sub>	Ambient temperature	-40		85	°C
T <sub>J</sub>	Operating Junction Temperature			110 <sup>(1)</sup>	°C
	Maximum Operating Junction Temperature	125			°C

- (1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to [SBAA403 application note](#) for additional details

## 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		AFE7950	UNIT
		ABJ or ALK (FC-BGA)	
		400 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	16.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.42	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	4.85	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.12	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	4.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 4.5 Transmitter Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC <sub>RES</sub>	DAC resolution			14		bits
$f_{\text{RFout}}$	RF output frequency range	$f_{\text{DAC}} = 12 \text{ GSPS}, 1^{\text{st}} \text{ Nyquist}$	600	6000		MHz
		$f_{\text{DAC}} = 12 \text{ GSPS}, 2^{\text{nd}} \text{ Nyquist}$	6000	12000		
		$f_{\text{DAC}} = 9 \text{ GSPS}, 1^{\text{st}} \text{ Nyquist}$	600	4500		
		$f_{\text{DAC}} = 9 \text{ GSPS}, 2^{\text{nd}} \text{ Nyquist}$	4500	9000		
		$f_{\text{DAC}} = 6 \text{ GSPS}, 1^{\text{st}} \text{ Nyquist}$	600	3000		
		$f_{\text{DAC}} = 6 \text{ GSPS}, 2^{\text{nd}} \text{ Nyquist}$	3000	6000		
$P_{\text{max\_FS}}$	Max Full Scale Output Power, max gain 1 tone, at device pins	$f_{\text{out}} = 850 \text{ MHz}, f_{\text{DAC}} = 5898.24 \text{ MSPS}, -0.5\text{dBFS}$		4.2		dBm
		$f_{\text{out}} = 1800 \text{ MHz}, f_{\text{DAC}} = 5898.24 \text{ MSPS}, -0.5\text{dBFS}$		4.6		dBm
		$f_{\text{out}} = 2600 \text{ MHz}, f_{\text{DAC}} = 8847.36 \text{ MSPS}, -0.5\text{dBFS}$		4.0		dBm
		$f_{\text{out}} = 3500 \text{ MHz}, -0.5\text{dBFS}$		3.9		dBm
		$f_{\text{out}} = 4900 \text{ MHz}, -0.5\text{dBFS}$		3.1		dBm
		$f_{\text{out}} = 3500 \text{ MHz}, f_{\text{DAC}} = 5898.24 \text{ MSPS}, -0.5\text{dBFS}, \text{straight mode}$		1.0		dBm
		$f_{\text{out}} = 4900 \text{ MHz}, f_{\text{DAC}} = 5898.24 \text{ MSPS}, -0.5\text{dBFS}, \text{straight mode}$		0.1		dBm
		$f_{\text{out}} = 4900 \text{ MHz}, f_{\text{DAC}} = 8847.36 \text{ MSPS}, -0.5\text{dBFS}, \text{straight mode}$		-0.7		dBm
		$f_{\text{out}} = 8100 \text{ MHz}, -0.1\text{dBFS}, \text{mixed mode}$		-2.8		dBm
		$f_{\text{out}} = 9600 \text{ MHz}, -0.1\text{dBFS}, \text{mixed mode}$		-4.3		dBm
R <sub>TERM</sub>	Output termination resistor	Default setting	50			$\Omega$
ATT <sub>range</sub>	DSA Attenuation range			40		dB
ATT <sub>step</sub>	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, before calibration		$\pm 0.2$		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, after calibration		$\pm 0.1$		dB
ATT <sub>phase-err</sub>	DSA Gain Steps Phase accuracy, any 8dB range	$f_{\text{out}} = 850\text{MHz}^{(2)}$		$\pm 1$		deg
		$f_{\text{out}} = 1800\text{MHz}^{(2)}$		$\pm 1$		deg
		$f_{\text{out}} = 2600\text{MHz}^{(2)}$		$\pm 1$		deg
		$f_{\text{out}} = 3500\text{MHz}^{(2)}$		$\pm 1$		
		$f_{\text{out}} = 4900\text{MHz}^{(2)}$		$\pm 1$		deg
		$f_{\text{out}} = 8100\text{MHz}^{(2)}$		$\pm 2$		deg
		$f_{\text{out}} = 9600\text{MHz}^{(2)}$		$\pm 2$		deg
G <sub>flat</sub>	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, $F_{\text{out}} < 4.9\text{G}$		1.2		

## 4.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MHz}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion, 2 tones at $f_{\text{IF}} \pm 10 \text{ MHz}$	$f_{\text{out}} = 850\text{MHz}, -7\text{dBFS}$ each tone	-66			dBc
		$f_{\text{out}} = 1800\text{MHz}, -7\text{dBFS}$ each tone	-63			dBc
		$f_{\text{out}} = 2600\text{MHz}, -7\text{dBFS}$ each tone	-62			dBc
		$f_{\text{out}} = 3500\text{MHz}, -7\text{dBFS}$ each tone	-61			dBc
		$f_{\text{out}} = 4900\text{MHz}, -7\text{dBFS}$ each tone	-57			dBc
		$f_{\text{out}} = 8100\text{MHz}, -7\text{dBFS}$ each tone	-55			dBc
		$f_{\text{out}} = 9600\text{MHz}, -7\text{dBFS}$ each tone	-52			dBc
		$f_{\text{out}} = 850\text{MHz}, -13\text{dBFS}$ each tone	-74.4			dBc
		$f_{\text{out}} = 1800\text{MHz}, -13\text{dBFS}$ each tone	-71.1			dBc
		$f_{\text{out}} = 2600\text{MHz}, -13\text{dBFS}$ each tone	-73			dBc
		$f_{\text{out}} = 3500\text{MHz}, -13\text{dBFS}$ each tone	-72			dBc
		$f_{\text{out}} = 4900\text{MHz}, -13\text{dBFS}$ each tone	-67.8			dBc
		$f_{\text{out}} = 8100\text{MHz}, -13\text{dBFS}$ each tone	-64			dBc
		$f_{\text{out}} = 9600\text{MHz}, -13\text{dBFS}$ each tone	-68			dBc
		$f_{\text{out}} = 850 \text{ MHz}$	50.8			dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	$f_{\text{out}} = 1800 \text{ MHz}$	51.9			dBc
		$f_{\text{out}} = 2600 \text{ MHz}$	42			dBc
		$f_{\text{out}} = 3500 \text{ MHz}$	44			dBc
		$f_{\text{out}} = 4900 \text{ MHz}$	46.1			dBc
		$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode	-51.9			dBc
f <sub>s</sub> /2 - f <sub>OUT</sub>	Interleaving Image	$f_{\text{DAC}} = 8847.36 \text{ MSPS}$ , interleave mode	-46.0			dBc
		$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode	-41			dBc
		$f_{\text{out}} = 850 \text{ MHz}$	-49			dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 1800 \text{ MHz}$	-53			dBc
		$f_{\text{out}} = 2600 \text{ MHz}$	-50			dBc
		$f_{\text{out}} = 3500 \text{ MHz}$	-48			dBc
		$f_{\text{out}} = 4900 \text{ MHz}$	-47			dBc
		$f_{\text{out}} = 8100 \text{ MHz}$	-50			dBc
		$f_{\text{out}} = 9600 \text{ MHz}$	-53			dBc
		$f_{\text{out}} = 850 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$	-60			dBc
		$f_{\text{out}} = 1800 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$	-64			dBc
		$f_{\text{out}} = 2600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$	-45			dBc
		$f_{\text{out}} = 3500 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$	-57			dBc
		$f_{\text{out}} = 4900 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$	-58			dBc
		$f_{\text{out}} = 8100 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$	-60			dBc
		$f_{\text{out}} = 9600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$	-62			dBc

## 4.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850 \text{ MHz}$		-62		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		-55		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		-57		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		-60		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		-54		dBc
		$f_{\text{out}} = 8100 \text{ MHz}$		-54		dBc
		$f_{\text{out}} = 9600 \text{ MHz}$		-56		dBc
		$f_{\text{out}} = 850 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
		$f_{\text{out}} = 1800 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 2600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 3500 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 4900 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-78		dBc
		$f_{\text{out}} = 8100 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-82		dBc
		$f_{\text{out}} = 9600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
HD $n$ , $n \geq 4$	Harmonic Distortion $n \geq 4$ (within Nyquist zone)	$f_{\text{out}} = 850 \text{ MHz}$		-81		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		-88		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		-86		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		-79		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		-86		dBc
		$f_{\text{out}} = 8100 \text{ MHz}$		-87		dBc
		$f_{\text{out}} = 9600 \text{ MHz}$		-85		dBc
		$f_{\text{out}} = 850 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-93		dBc
		$f_{\text{out}} = 1800 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-98		dBc
		$f_{\text{out}} = 2600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 3500 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 4900 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 8100 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 9600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	$f_{\text{out}} = 850 \text{ MHz}$		68.5		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		79.4		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		77		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		75		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		76		dBc
		$f_{\text{out}} = 8100 \text{ MHz}$		61		dBc
		$f_{\text{out}} = 9600 \text{ MHz}$		64		dBc
$f_S/4$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-64		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-75		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-67		dBFS
$f_S/2$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-49		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-48		dBFS
		$f_{\text{DAC}} = 11796.48 \text{ MSPS}$		-48		dBFS

## 4.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3*f <sub>s</sub> /4	Fixed Spur	2nd Nyquist, $f_{\text{DAC}} = 5898.24\text{MSPS}$	-76			dBFS
		2nd Nyquist, $f_{\text{DAC}} = 8847.36\text{MSPS}$	-89			dBFS
		2nd Nyquist, $f_{\text{DAC}} = 11796.48\text{MSPS}$	-63			dBFS
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 0.85\text{ GHz}$	Atten=0dB, Pout=-13dBFS	-68.5			dBc
		Atten=20dB, Pout=-13dBFS	-67.2			dBc
		Atten=28dB, Pout=-13dBFS	-64.5			dBc
		Atten=39dB, Pout=-13dBFS	-53.9			dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 1.8425\text{ GHz}$	Atten=0dB, Pout=-13dBFS	-70.7			dBc
		Atten=20dB, Pout=-13dBFS	-68.3			dBc
		Atten=28dB, Pout=-13dBFS	-62.9			dBc
		Atten=39dB, Pout=-13dBFS	-52.0			dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 2.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS	-71			dBc
		Atten=20dB, Pout=-13dBFS	-68			dBc
		Atten=28dB, Pout=-13dBFS	-62			dBc
		Atten=39dB, Pout=-13dBFS	-51.3			dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS	-70			dBc
		Atten=20dB, Pout=-13dBFS	-67			dBc
		Atten=28dB, Pout=-13dBFS	-60			dBc
		Atten=39dB, Pout=-13dBFS	-49.8			dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS	-68.8			dBc
		Atten=20dB, Pout=-13dBFS	-65.9			dBc
		Atten=28dB, Pout=-13dBFS	-60.6			dBc
		Atten=39dB, Pout=-13dBFS	-49.5			dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 2.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS	-65			dBc
		Atten=20dB, Pout=-13dBFS	-62			dBc
		Atten=20dB, Pout=-13dBFS	-55			dBc
		Atten=39dB, Pout=-13dBFS	-44.3			dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS	-64			dBc
		Atten=20dB, Pout=-13dBFS	-59			dBc
		Atten=28dB, Pout=-13dBFS	-52			dBc
		Atten=39dB, Pout=-13dBFS	-41.1			dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS	-64.1			dBc
		Atten=20dB, Pout=-13dBFS	-60.4			dBc
		Atten=28dB, Pout=-13dBFS	-53.5			dBc
		Atten=39dB, Pout=-13dBFS	-42.5			dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 8.1\text{ GHz}$	Atten=0dB, Pout=-13dBFS	-58			dBc
		Atten=20dB, Pout=-13dBFS	-53			dBc
		Atten=28dB, Pout=-13dBFS	-46			dBc
		Atten=39dB, Pout=-13dBFS	-36			dBc

## 4.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-57		dBc
		Atten=20dB, Pout=-13dBFS		-50		dBc
		Atten=28dB, Pout=-13dBFS		-42		dBc
		Atten=39dB, Pout=-13dBFS		-31		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	$F_{\text{out}} = 0.85\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.2		%
		$F_{\text{out}} = 1.8425\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.3		%
		$F_{\text{out}} = 2.6\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.28		%
		$F_{\text{out}} = 3.5\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.38		%
		$F_{\text{out}} = 4.9\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.4		%
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-157.6		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-153.3		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-147.9		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-136.9		dBFS/Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 1.8\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-158.4		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-152.2		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-145.6		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-134.6		dBFS/Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-157		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-151		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-144		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-133.0		dBFS/Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $F_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-158		dBFS/Hz
		Atten=20dB, Pout=-13dBFS		-150		dBFS/Hz
		Atten=28dB, Pout=-13dBFS		-143		dBFS/Hz
		Atten=39dB, Pout=-13dBFS		-131.8		dBFS/Hz

## 4.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $F_{\text{out}} = 4.9 \text{ GHz}$	Atten=0dB, Pout=-13dBFS		-155.5		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147.8		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140.8		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129.6		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 50MHz offset $F_{\text{out}} = 8.1 \text{ GHz}$	Atten=0dB, Pout=-13dBFS		-153		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 50MHz offset $F_{\text{out}} = 9.6 \text{ GHz}$	Atten=0dB, Pout=-13dBFS		-152		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
S22	Output Return Loss, <6GHz, +/- fc * 10%	with matching		-17		dB
	Output Return Loss, >8GHz, +/- fc * 10%	with matching		-10		dB
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT <sup>(1)</sup>	$f_{\text{out}} = 900 \text{ MHz}, f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-49		dB
		$f_{\text{out}} = 1850 \text{ MHz}, f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-59		dB
		$f_{\text{out}} = 2600 \text{ MHz}, f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-65		dB
		$f_{\text{out}} = 3500 \text{ MHz}, f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-66		dB
		$f_{\text{out}} = 4900 \text{ MHz}, f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-60		dB
		$f_{\text{out}} = 900 \text{ MHz}, f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-90		dB
		$f_{\text{out}} = 1850 \text{ MHz}, f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-91		dB
		$f_{\text{out}} = 2600 \text{ MHz}, f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-93		dB
		$f_{\text{out}} = 3500 \text{ MHz}, f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-94		dB
		$f_{\text{out}} = 4900 \text{ MHz}, f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-83		dB

## 4.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN <sub>TXADD</sub>	Additive Phase Noise External Clock Mode <sup>(3)</sup>	$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{Hz}$		-88		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 1\text{kHz}$		-102		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 10\text{kHz}$		-110		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{kHz}$		-123		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 1\text{MHz}$		-136		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 10\text{MHz}$		-143		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{MHz}$		-146		dBc/Hz

- (1) Measured with differential 50 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
- (2) After DSA calibration procedure
- (3) Single side band, input clock phase noise subtracted.

## 4.6 RF ADC Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC <sub>RES</sub>	ADC resolution			14		bits
F <sub>RFin</sub>	RF input frequency range		600	12000		MHz
P <sub>FS_CW,min</sub>	Min Full scale input power, at device pins <sup>(1)</sup>	f <sub>IN</sub> = 830 MHz, DSA=0dB		-2.9		dBm
		f <sub>IN</sub> = 1760 MHz, DSA=0dB		-2.8		dBm
		f <sub>IN</sub> = 2610 MHz, DSA=0dB		-1.8		dBm
		f <sub>IN</sub> = 3610 MHz, DSA=0dB		-0.4		dBm
		f <sub>IN</sub> = 4910 MHz, DSA=0dB		0.1		dBm
		f <sub>IN</sub> = 8150 MHz, DSA=0dB		2.1		dBm
		f <sub>IN</sub> = 9610 MHz, DSA=0dB		4.3		dBm
S11	Input Return Loss	with matching network		-12.0		dB
ATT <sub>range</sub>	DSA Attenuation range			25.0		dB
ATT <sub>step</sub>	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F <sub>in</sub> =3610MHz, after calibration		±0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	F <sub>in</sub> =3610MHz, after calibration		±0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F <sub>in</sub> =4910MHz, after calibration		±1.8		deg
NSD	Noise Density (small signal)	f <sub>IN</sub> = 830 MHz, DSA = 3dB <sup>(3)</sup>		-155.2		dBFS/Hz
		f <sub>IN</sub> = 1760 MHz, DSA = 3dB <sup>(3)</sup>		-155.0		dBFS/Hz
		f <sub>IN</sub> = 2610 MHz, DSA = 3dB <sup>(3)</sup>		-154.4		dBFS/Hz
		f <sub>IN</sub> = 3610 MHz, DSA = 3dB <sup>(3)</sup>		-154.1		dBFS/Hz
		f <sub>IN</sub> = 4910 MHz, DSA = 3dB <sup>(3)</sup>		-155.1		dBFS/Hz
		f <sub>IN</sub> = 8150 MHz, DSA = 3dB <sup>(3)</sup>		-150		dBFS/Hz
		f <sub>IN</sub> = 9610 MHz, DSA = 3dB <sup>(3)</sup>		-151		dBFS/Hz
		f <sub>IN</sub> = 830 MHz, 3<=Atten<=22		-156.0		dBFS/Hz
		f <sub>IN</sub> = 1760 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f <sub>IN</sub> = 2610 MHz, 3<=Atten<=25		-155.7		dBFS/Hz
		f <sub>IN</sub> = 3610 MHz, 3<=Atten<=25		-155.4		dBFS/Hz
		f <sub>IN</sub> = 4910 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f <sub>IN</sub> = 8150 MHz, 3<=Atten<=25		-152.5		dBFS/Hz
		f <sub>IN</sub> = 9610 MHz, 3<=Atten<=25		-152.5		dBFS/Hz
NF <sub>min</sub>	Noise Figure min DSA Atten=0 - 3dB	f <sub>IN</sub> = 830 MHz		19.1		dB
		f <sub>IN</sub> = 1760 MHz		19.0		dB
		f <sub>IN</sub> = 2610 MHz		20.9		dB
		f <sub>IN</sub> = 3610 MHz		22.8		dB
		f <sub>IN</sub> = 4910 MHz		22.4		dB
		f <sub>IN</sub> = 8150 MHz		27.3		dB
		f <sub>IN</sub> = 9610 MHz		30		dB

## 4.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise Figure DSA Atten=4dB	$f_{\text{IN}} = 830 \text{ MHz}^{(4)}$		20.0		dB
		$f_{\text{IN}} = 1760 \text{ MHz}^{(4)}$		20.6		dB
		$f_{\text{IN}} = 2610 \text{ MHz}^{(4)}$		21.9		dB
		$f_{\text{IN}} = 3610 \text{ MHz}^{(4)}$		23.5		dB
		$f_{\text{IN}} = 4910 \text{ MHz}^{(4)}$		22.3		dB
		$f_{\text{IN}} = 8150 \text{ MHz}^{(4)}$		27.9		dB
		$f_{\text{IN}} = 9610 \text{ MHz}^{(4)}$		30.7		dB
$\text{NF}_{\text{max}}$	Noise Figure DSA Atten=20dB	$f_{\text{IN}} = 830 \text{ MHz}$		34.7		dB
		$f_{\text{IN}} = 1760 \text{ MHz}$		35.2		dB
		$f_{\text{IN}} = 2610 \text{ MHz}$		36.0		dB
		$f_{\text{IN}} = 3610 \text{ MHz}$		37.3		dB
		$f_{\text{IN}} = 4910 \text{ MHz}$		37.6		dB
		$f_{\text{IN}} = 8150 \text{ MHz}$		42.8		dB
		$f_{\text{IN}} = 9610 \text{ MHz}$		45		dB
IMD3	3 <sup>rd</sup> order intermodulation 2 tones at at $f_{\text{IN}} \pm 10\text{MHz}$ -7dBFS each tone	$f_{\text{IN}} = 840 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-82.4		dBc
		$f_{\text{IN}} = 1770 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-84.1		dBc
		$f_{\text{IN}} = 2610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-74		dBc
		$f_{\text{IN}} = 3610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-77		dBc
		$f_{\text{IN}} = 4920 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-75.9		dBc
		$f_{\text{IN}} = 8150 \text{ MHz}, 3 \leq \text{Atten} \leq 12,$ 25MHz tone spacing		-55		dBc
		$f_{\text{IN}} = 9610 \text{ MHz}, 3 \leq \text{Atten} \leq 12,$ 25MHz tone spacing		-60		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, $A_{\text{IN}} = -3$ dBFS	$f_{\text{IN}} = 830 \text{ MHz}$		88.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		80.6		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		84		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		78.9		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		78		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		71		dBFS
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -3$ dBFS <sup>(2)</sup>	$f_{\text{IN}} = 830 \text{ MHz}$		-85.5		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-90.5		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-87		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-84.2		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-70		dBFS

## 4.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -3 \text{ dBFS}$	$f_{\text{IN}} = 830 \text{ MHz}$		-80.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-85.3		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-86		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-75.4		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-70		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -3 \text{ dBFS}$	$f_{\text{IN}} = 830 \text{ MHz}$		-88.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-80.6		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-84		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-81.7		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-78		dBFS
SFDR	Spurious Free Dynamic Range $A_{\text{IN}} = -13 \text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830 \text{ MHz}$		89.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		88.8		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		95		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		90		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		89.8		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		83		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		80		dBFS
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -13 \text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830 \text{ MHz}$ , with board trim		-79.0		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$ , with board trim		-101.6		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$ , with board trim		-100		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$ , with board trim		-101		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$ , with board trim		-99.1		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$ , with board trim		-107		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$ , with board trim		-107		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -13 \text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830 \text{ MHz}$		-95.4		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-95.2		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-98		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-97		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-94		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-100		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-102		dBFS

## 4.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -13 \text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830 \text{ MHz}$		-89.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-88.8		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-83		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-80		dBFS
RX-RX Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN	$f_{\text{IN}} = 830 \text{ MHz}$		-76.6		dBc
		$f_{\text{IN}} = 1760 \text{ MHz}$		-70.9		dBc
		$f_{\text{IN}} = 2610 \text{ MHz}$		-73.5		dBc
		$f_{\text{IN}} = 3610 \text{ MHz}$		-76.9		dBc
		$f_{\text{IN}} = 4910 \text{ MHz}$		-65.3		dBc
		$f_{\text{IN}} = 8150 \text{ MHz}$		-64		dBc
		$f_{\text{IN}} = 9610 \text{ MHz}$		-60		dBc
TX-FB Isolation	Near Channel: 2TXOUT to 1FBIN 4TXOUT to 2FBIN	$f_{\text{IN}} = 830 \text{ MHz}$		-84.3		dBc
		$f_{\text{IN}} = 1760 \text{ MHz}$		-87.7		dBc
		$f_{\text{IN}} = 2610 \text{ MHz}$		-85		dBc
		$f_{\text{IN}} = 3610 \text{ MHz}$		-75		dBc
		$f_{\text{IN}} = 4910 \text{ MHz}$		-81.5		dBc
		$f_{\text{IN}} = 8150 \text{ MHz}$		-71		dBc
		$f_{\text{IN}} = 9610 \text{ MHz}$		-69		dBc
TX-RX Isolation	Far Channel: 2TXOUT to 1RXIN 4TXOUT to 3RXIN	$f_{\text{IN}} = 830 \text{ MHz}$		-85.9		dBc
		$f_{\text{IN}} = 1760 \text{ MHz}$		-86.9		dBc
		$f_{\text{IN}} = 2610 \text{ MHz}$		-91		dBc
		$f_{\text{IN}} = 3610 \text{ MHz}$		-83		dBc
		$f_{\text{IN}} = 4910 \text{ MHz}$		-81.9		dBc
		$f_{\text{IN}} = 8150 \text{ MHz}$		-68		dBc
		$f_{\text{IN}} = 9610 \text{ MHz}$		-68		dBc

- (1) The input fullscale at minimum attenuation can be reduced by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
- (2) NLE correction of HD2
- (3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
- (4) NF increase 1dB per DSA 1dB above DSA = 3dB

## 4.7 PLL/VCO/Clock Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; Reference clock input frequency 491.52MHz (unless otherwise noted),  $f_{\text{DAC}} = f_{\text{VCO}}$ ,  $f_{\text{OUT}} = f_{\text{DAC}}/4$ , normalized to  $f_{\text{VCO}}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{VCO}1}$	VCO1 min frequency			7.2		GHz
	VCO1 max frequency		7.68			GHz
$f_{\text{VCO}2}$	VCO2 min frequency			8.8		GHz
	VCO2 max frequency		9.1			GHz
$f_{\text{VCO}3}$	VCO3 min frequency			9.7		GHz
	VCO3 max frequency		10.24			GHz
$f_{\text{VCO}4}$	VCO4 min frequency			11.6		GHz
	VCO4 max frequency		12.08			GHz
$\text{DIV}_{\text{DAC}}$	DAC sample rate divider		1, 2 or 3			
$\text{DIV}_{\text{FBAD}}_c$	ADC sample rate divider from DAC sample rate		1, 2, 3, 4, 6 or 8			
$\text{DIV}_{\text{RXAD}}_c$	ADC sample rate divider		1, 2, 3, 4, 6 or 8			
$\text{PN}_{\text{VCO}}$	Closed Loop Phase Noise $F_{\text{PLL}} = 11.79848 \text{ GHz}$ $F_{\text{REF}} = 491.52 \text{ MHz}$	600kHz	-113			$\text{dBc}/\text{Hz}$
		800kHz	-116			$\text{dBc}/\text{Hz}$
		1MHz	-119			$\text{dBc}/\text{Hz}$
		1.8MHz	-125			$\text{dBc}/\text{Hz}$
		5MHz	-133			$\text{dBc}/\text{Hz}$
		50MHz	-141			$\text{dBc}/\text{Hz}$
	Closed Loop Phase Noise $F_{\text{PLL}} = 8.84736 \text{ GHz}$ $F_{\text{REF}} = 491.52 \text{ MHz}$	600kHz	-114			$\text{dBc}/\text{Hz}$
		800kHz	-118			$\text{dBc}/\text{Hz}$
		1MHz	-120			$\text{dBc}/\text{Hz}$
		1.8MHz	-127			$\text{dBc}/\text{Hz}$
		5MHz	-135			$\text{dBc}/\text{Hz}$
		50MHz	-142			$\text{dBc}/\text{Hz}$
$F_{\text{rms}}$	Clock PLL integrated phase error <sup>(1)</sup>	600kHz	-113			$\text{dBc}/\text{Hz}$
		800kHz	-116			$\text{dBc}/\text{Hz}$
		1MHz	-119			$\text{dBc}/\text{Hz}$
		1.8MHz	-125			$\text{dBc}/\text{Hz}$
		5MHz	-134			$\text{dBc}/\text{Hz}$
		50MHz	-140			$\text{dBc}/\text{Hz}$
$f_{\text{PFD}}$	PFD frequency	600kHz	-116			$\text{dBc}/\text{Hz}$
		800kHz	-119			$\text{dBc}/\text{Hz}$
		1MHz	-122			$\text{dBc}/\text{Hz}$
		1.8MHz	-127			$\text{dBc}/\text{Hz}$
		5MHz	-136			$\text{dBc}/\text{Hz}$
		50MHz	-143			$\text{dBc}/\text{Hz}$
$\text{PN}_{\text{pll\_flat}}$	$f_{\text{VCO}} = 11796.48 \text{ MHz}$	$f_{\text{PLL}} = 11.79848 \text{ GHz}, [1\text{kHz}, 100\text{MHz}]$	-43.4			$\text{dBc}/\text{Hz}$
		$f_{\text{PLL}} = 8.8536 \text{ GHz}, [1\text{kHz}, 100\text{MHz}]$	-47.6			$\text{dBc}/\text{Hz}$
		$f_{\text{PLL}} = 9.8304 \text{ GHz}, [1\text{kHz}, 100\text{MHz}]$	-46.2			$\text{dBc}/\text{Hz}$
$f_{\text{REF}}$	Input Clock frequency		0.1	500	12	GHz

## 4.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; Reference clock input frequency 491.52MHz (unless otherwise noted),  $f_{\text{DAC}} = f_{\text{VCO}}$ ,  $f_{\text{OUT}} = f_{\text{DAC}}/4$ , normalized to  $f_{\text{VCO}}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>SS</sub>	Input Clock level		0.6		1.8	V <sub>ppdiff</sub>
Coupling			AC Coupling Only			
REFCLK input impedance <sup>(2)</sup>	Parallel resistance		100			$\Omega$
	Parallel capacitance		0.5			pF

(1) Single Sideband, not including the reference clock contribution

(2) Refer to S11 data available from TI for impedance vs frequency

## 4.8 Digital Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CML SerDes Inputs [8:1]SRX+/-</b>						
$V_{\text{SRDIFF}}$	SerDes Receiver Input Amplitude	differential	100	1200		mVpp
$V_{\text{SRCOM}}$	SerDes Input Common Mode		0.4	0.5	0.6	V
$Z_{\text{SRdiff}}$	SerDes Internal Differential Termination <sup>(1)</sup>		100			$\Omega$
$F_{\text{SerDes}}$	SerDes Bit Rate	Full rate mode	19	29.5		Gbps
		Half rate mode	9.5	16.25		Gbps
		Quarter rate mode	4.75	8.125		Gbps
	Insertion Loss Tolerance <sup>(2)</sup>	Serdes supply = 1.8V	25			dB
$T_J$	Total Jitter Tolerance			0.42		UI
<b>CML SerDes Outputs [8:1]STX+/-</b>						
$V_{\text{STDIFF}}$	SerDes Transmitter Output Amplitude	differential	500	1000		mVpp
$V_{\text{STCOM}}$	SerDes Output Common Mode		0.4	0.45	0.55	V
$Z_{\text{STdiff}}$	SerDes Output Impedance		100			$\Omega$
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range			7		dB
TTJ	Output total jitter			0.21		UI
<b>CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1</b>						
$V_{\text{IH}}$	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
$V_{\text{IL}}$	Low-Level Input Voltage			0.4×VDD1 P8GPIO		V
$I_{\text{IH}}$	High-Level Input Current		-250	250		$\mu\text{A}$
$I_{\text{IL}}$	Low-Level Input Current		-250	250		$\mu\text{A}$
$C_L$	CMOS input capacitance		2			pF
$V_{\text{OH}}$	High-Level Ouput Voltage		VDD1P8G PIO-0.2			V
$V_{\text{OL}}$	Low-Level Output Voltage			0.2		V
<b>Differential Inputs: SYSREF+/- Mode A</b>						
$\text{Clock}_{\text{MODE}}$			PLL Clock Mode Only			
$F_{\text{SYSREFMAX}}$	SYSREF Input Frequency Maximum		40			MHz
$V_{\text{SWINGSRMAX}}$	SYSREF Input Swing Maximum		1.8			$V_{\text{ppdiff}}^{(3)}$
$V_{\text{SWINGSRMIN}}$	SYSREF Input Swing Minimum	$f_{\text{REF}} < 500\text{MHz}$	0.3			$V_{\text{ppdiff}}^{(3)}$
$V_{\text{SWINGSRMIN}}$	SYSREF Input Swing Minimum	$f_{\text{REF}} > 500\text{MHz}$	0.6			$V_{\text{ppdiff}}^{(3)}$
$V_{\text{COMSRMAX}}$	SYSREF Input Common Mode Voltage Maximum		0.8			V
$V_{\text{COMSRMIN}}$	SYSREF Input Common Mode Voltage Minimum		0.6			V
$Z_T$	Input termination	differential	100 <sup>(1)</sup>			$\Omega$
$C_L$	Input capacitance	Each pin to GND	0.5			pF
<b>LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-</b>						
$V_{\text{ICOM}}$	Input Common Voltage		1.2			V
$V_{\text{ID}}$	Differential Input Voltage swing		450			$V_{\text{ppdiff}}^{(3)}$

## 4.8 Digital Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_T$	Input termination	differential		100		$\Omega$
<b>LVDS Outputs: 0SYNCOUT+- and 1SYNCOUT+-</b>						
$V_{O\text{COM}}$	Output Common Voltage			1.2		V
$V_{OD}$	Differential Output Voltage swing			500		$V_{\text{ppdiff}}^{(3)}$
$Z_T$	Internal Termination			100		$\Omega$

(1) SYSREF termination is programmable between  $100\Omega$ ,  $150\Omega$  and  $300\Omega$

(2) Loss tolerance is bump to bump from STX to SRX

(3)  $V_{\text{ppdiff}}$  is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

## 4.9 Power Supply Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4T2F - FDD FB 100% on, no RX TX/FB Rate: 491.52 Msps Single Band: 12x Int, FB 6x Dec $f_{\text{DAC}} = 5898.24$ SPS $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = 1.85$ GHz 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1	948.2			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		533.7			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		77.3			mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 2: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Dual Band: 12x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 8847.36\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{OUT}}=f_{\text{IN}}= 1.9, 2.6$ GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1	299.4			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		804.5			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		49.1			mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9		2041.3			mA
$P_{\text{diss}}$	Power Dissipation		6027.1			mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Dual Band: 12x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 8847.36\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{OUT}}=f_{\text{IN}}= 1.9, 2.6$ GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1	820.4			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		735.2			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		74.4			mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 2: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Dual Band: 12x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 8847.36\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{OUT}}=f_{\text{IN}}= 1.9, 2.6$ GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1	289.0			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		822.0			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		45.6			mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9		2263.8			mA
$P_{\text{diss}}$	Power Dissipation		6359.2			mW

## 4.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4T4R2F - FDD FB 100% on TX Dual Band: 12x Int, FB 6x Dec RX Dual Band: RX 24x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1	1668.6			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		965.1			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		77.6			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 3: 4T4R2F - FDD FB 100% on TX Dual Band: 12x Int, FB 6x Dec RX Dual Band: RX 24x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1	893.4			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		879.5			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		50.7			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		3826.9			mA
$P_{\text{diss}}$	Power Dissipation		10513.0			mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 4T4R2F - FDD FB 100% on 7.5 GSPS DAC, 2.5 GSPS ADC Single Band: 15x Int, FB 5x Dec Dual Band: RX 20x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 7372.8\text{ MSPS}$ $f_{\text{ADC}} = 2457.6\text{ MSPS}$ $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-16-16-1	1611.5			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		694.5			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		72.8			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 4: 4T4R2F - FDD FB 100% on 7.5 GSPS DAC, 2.5 GSPS ADC Single Band: 15x Int, FB 5x Dec Dual Band: RX 20x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 7372.8\text{ MSPS}$ $f_{\text{ADC}} = 2457.6\text{ MSPS}$ $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-16-16-1	768.5			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		940.5			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		45.5			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		3000.5			mA
$P_{\text{diss}}$	Power Dissipation		9087.4			mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 3.5\text{ GHz}$ $f_{\text{RX}} = 3.5\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1	821.8			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		808.5			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		77.4			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 5: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 3.5\text{ GHz}$ $f_{\text{RX}} = 3.5\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1	289.5			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		682.0			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		49.0			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		2123.3			mA
$P_{\text{diss}}$	Power Dissipation		6209.3			mW

## 4.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7a: TDD 4T1FB (RX iin Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode RX 3G : 368.64M. 16 bit, Standby Serdess: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx	658.1			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		431.1			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		75.3			mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 7a: TDD 4T1FB (RX iin Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode RX 3G : 368.64M. 16 bit, Standby Serdess: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx	189.2			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		1041.1			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		39.0			mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9	Mode 7a: TDD 4T1FB (RX iin Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode RX 3G : 368.64M. 16 bit, Standby Serdess: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx	2208.7			mA
$P_{\text{diss}}$	Power Dissipation		5607.0			mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		789.5			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		471.3			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		73.4			mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 7a: TDD 4T1FB (RX iin Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode, Standby RX 3G : 368.64M. 16 bit Serdess: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx	599.3			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		169.6			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		39.1			mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9	Mode 7a: TDD 4T1FB (RX iin Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode, Standby RX 3G : 368.64M. 16 bit Serdess: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx	1645.3			mA
$P_{\text{diss}}$	Power Dissipation		4851.9			mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		691.0			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		441.2			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		74.8			mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 7a: TDD 4T1FB (RX iin Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode, 75% on RX 3G : 368.64M. 16 bit 25% on Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx	291.7			mA
$I_{VDD1P2}$	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		823.2			mA
$I_{VDD1P2}$	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		39.0			mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9	Mode 7a: TDD 4T1FB (RX iin Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode, 75% on RX 3G : 368.64M. 16 bit 25% on Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx	2067.9			mA
$P_{\text{diss}}$	Power Dissipation		5418.2			mW

## 4.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		1283.8		mA
$I_{VDD1P8}$	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		752.0		mA
$I_{VDD1P8}$	Group 3C: VDD1P8PLL + VDD1P8PLLVCO	Mode 7d: FDD 4T4R1FB TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx	74.6		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX		750.5		mA
$I_{VDD1P2}$	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		1077.6		mA
$I_{VDD1P2}$	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		47.7		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9		2695.5		mA
$P_{\text{diss}}$	Power Dissipation		8475.5		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		20.3		mA
$I_{VDD1P8}$	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		292.8		mA
$I_{VDD1P8}$	Group 3C: VDD1P8PLL + VDD1P8PLLVCO	Mode 8: same configuration as mode 7, Sleep Mode. SLEEP pin is pull high.	12.6		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX		4.6		mA
$I_{VDD1P2}$	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		54.3		mA
$I_{VDD1P2}$	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		15.3		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9		313.1		mA
$P_{\text{diss}}$	Power Dissipation		956.8		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		1593.2		mA
$I_{VDD1P8}$	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8	Mode 9: 4T4R2F - FDD FB 100% on TX Single Band: 24x Int, FB 12x Dec RX Single Band: RX 24x TX/FB Rate 245.76 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 5898.24 \text{ MSPS}$ $f_{\text{ADC}} = 2949.12 \text{ MSPS}$ $f_{\text{TX}} = 0.85 \text{ GHz}$ $f_{\text{RX}} = 0.8 \text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-8-8-1	840.6		mA
$I_{VDD1P8}$	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		77.3		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX		905.0		mA
$I_{VDD1P2}$	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		817.7		mA
$I_{VDD1P2}$	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		52.1		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9		2405.2		mA
$P_{\text{diss}}$	Power Dissipation		8814.3		mW

## 4.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 10: 4T4R2F - FDD FB 100% on TX Single Band: 18x Int, FB 6x Dec RX Single Band: RX 12x TX/FB Rate 491.52 Msps RX Rate 245.76 Msps $f_{\text{DAC}} = 8847.36\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = 1.85\text{ GHz}$ $f_{\text{RX}} = 1.75\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 8-8-2-1, FB: 4-4-2-1, RX: 4-8-4-1	1626.2			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		976.4			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		74.6			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 10: 4T4R2F - FDD FB 100% on TX Single Band: 18x Int, FB 6x Dec RX Single Band: RX 12x TX/FB Rate 491.52 Msps RX Rate 245.76 Msps $f_{\text{DAC}} = 8847.36\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = 1.85\text{ GHz}$ $f_{\text{RX}} = 1.75\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 8-8-2-1, FB: 4-4-2-1, RX: 4-8-4-1	902.7			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		1111.9			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		48.0			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		3578.9			mA
$P_{\text{diss}}$	Power Dissipation		10515.0			mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11a: TDD 4T1FB (RX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	800			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		840			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		73			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 11a: TDD 4T1FB (RX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	190			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		1440			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		75			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		3070			mA
$P_{\text{diss}}$	Power Dissipation		8010			mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11b: TDD 4R (TX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	750			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		890			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		72			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 11b: TDD 4R (TX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	610			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		280			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		72			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		2360			mA
$P_{\text{diss}}$	Power Dissipation		6460			mW

## 4.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11c: TDD 4T4R1FB average TX/FB: 75%, RX 25% Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48 \text{ MSPS}$ $f_{\text{ADC}} = 2949.12 \text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8 \text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	790			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		850			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		73			mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 11c: TDD 4T4R1FB average TX/FB: 75%, RX 25% Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48 \text{ MSPS}$ $f_{\text{ADC}} = 2949.12 \text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8 \text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	300			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		1150			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		75			mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9		2890			mA
$P_{\text{diss}}$	Power Dissipation		7620			mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11d: FDD 4T4R Single Band: 8x Int, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48 \text{ MSPS}$ $f_{\text{ADC}} = 2949.12 \text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8 \text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	1260			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		940			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO		73			mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX	Mode 11d: FDD 4T4R Single Band: 8x Int, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48 \text{ MSPS}$ $f_{\text{ADC}} = 2949.12 \text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8 \text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	630			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		1480			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		78			mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9		4200			mA
$P_{\text{diss}}$	Power Dissipation		10640			mW

## 4.10 Timing Requirements

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
<b>Timing: SYSREF+/-</b>					
$t_s(\text{SYSREF})$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_h(\text{SYSREF})$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
<b>Timing: Serial ports</b>					
$t_s(\text{SENB})$	Setup Time, SENB to Rising Edge of SCLK		15		ns
$t_h(\text{SENB})$	Hold Time, SENB after last Rising Edge of SCLK <sup>(1)</sup>		$5 + t_{\text{SCLK}}$		ns
$t_s(\text{SDIO})$	Setup Time, SDIO valid to Rising Edge of SCLK		15		ns
$t_h(\text{SDIO})$	Hold Time, SDIO valid after Rising Edge of SCLK		5		ns
$t_{(\text{SCLK})_W}$	Minimum SCLK period: registers write		25		ns
$t_{(\text{SCLK})_R}$	Minimum SCLK period: registers read		50		ns
$t_d(\text{data\_out})$	Minimum Data Output delay after Falling Edge of SCLK		0		ns
	Maximum Data Output delay after Falling Edge of SCLK		15		ns
$t_{\text{RESET}}$	Minimum RESETZ Pulse Width		1		ms

(1) SDEN\\ need to be held one more extra clock cycle with the last SCLK edge

## 4.11 Switching Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

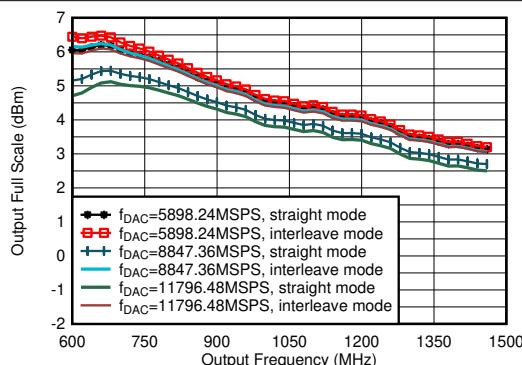
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TX Channel Latency</b>					
	SerDes Receiver Analog Delay	Full rate	2.8		ns
$t_{\text{JESD}\text{TX}}$	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)	152		interface clock cycles <sup>(1)</sup>
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)	176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)	124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)	97		
<b>RX Channel Latency</b>					
	SerDes Transmitter Analog Delay		3.6		ns
$t_{\text{JESDRX}}$	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)	92		interface clock cycles <sup>(1)</sup>
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)	108		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)	153		
<b>FB Channel Latency</b>					
	SerDes Transmitter Analog Delay		3.6		ns
$t_{\text{JESDFB}}$	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation	151		interface clock cycles <sup>(1)</sup>
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation	177		

(1) Interface clock cycles is the period of the digital interface sample rate, e.g. 1GSPS = 1ns.

## 4.12 Typical Characteristics

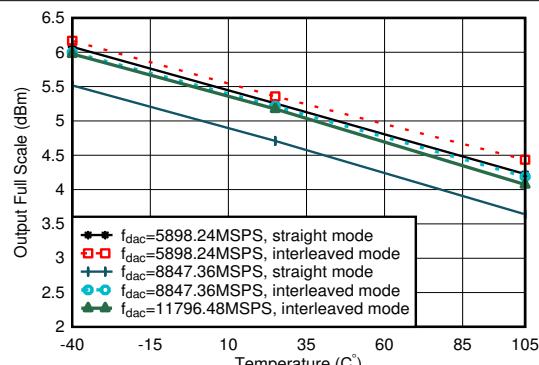
### 4.12.1 TX Typical Characteristics 800 MHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



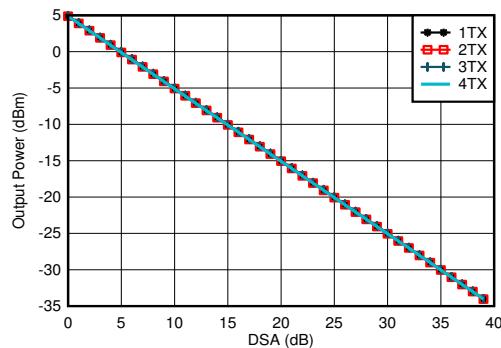
including PCB and cable losses,  $A_{\text{out}} = -0.5\text{dFBS}$ , DSA = 0, 0.8 GHz matching

**Figure 4-1. TX Output Fullscale vs Output Frequency**



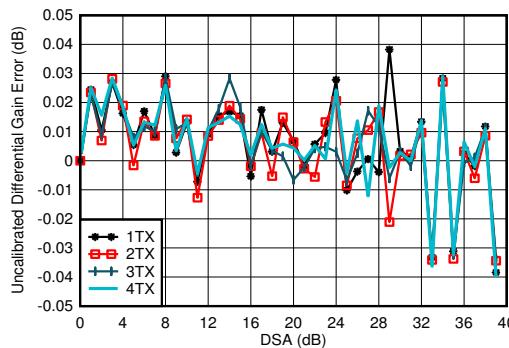
including PCB and cable losses,  $A_{\text{out}} = -0.5\text{dFBS}$ , DSA = 0, 0.8 GHz matching

**Figure 4-2. TX Output Fullscale vs Temperature**



$f_{\text{DAC}} = 11796.48 \text{ MSPS}$ , interleave mode,  $A_{\text{out}} = -0.5\text{dFBS}$ , matching 0.8 GHz

**Figure 4-3. TX Output Power vs DSA Setting and Channel at 0.85 GHz**

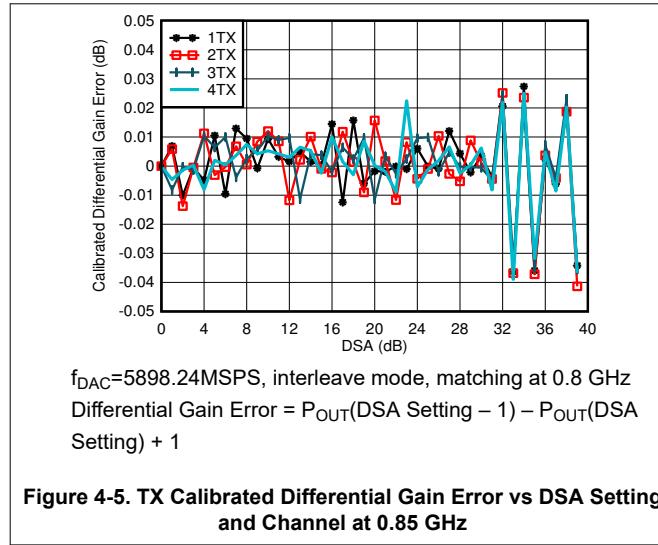


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-4. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz**

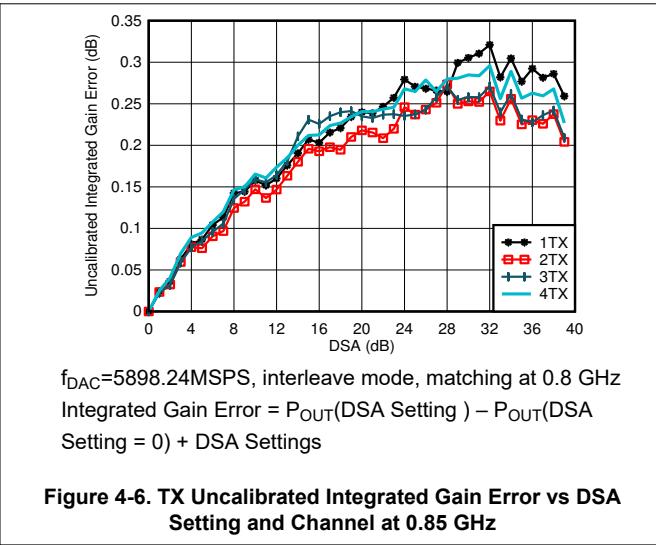
#### 4.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



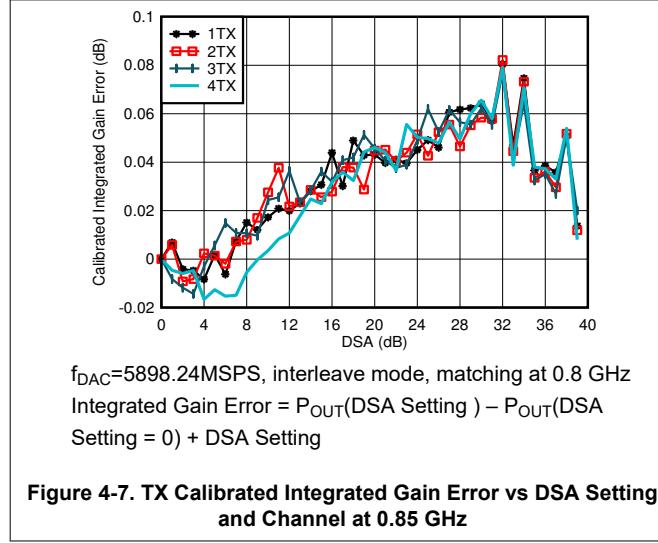
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 4-5. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



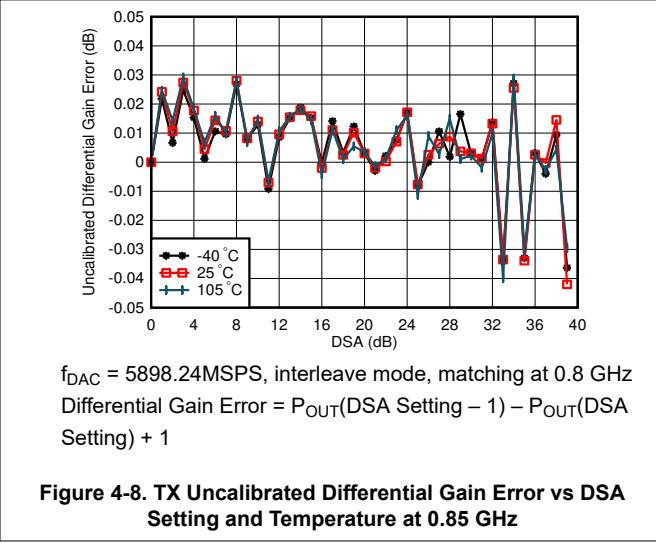
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} ) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Settings}$

Figure 4-6. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} ) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

Figure 4-7. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz

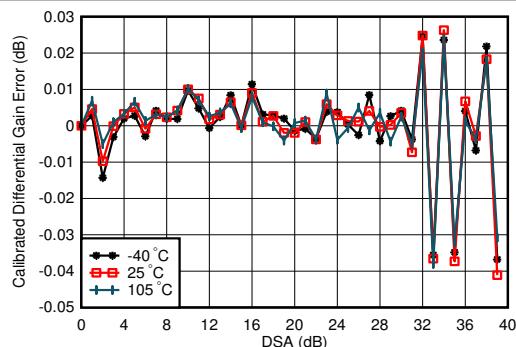


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 4-8. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz

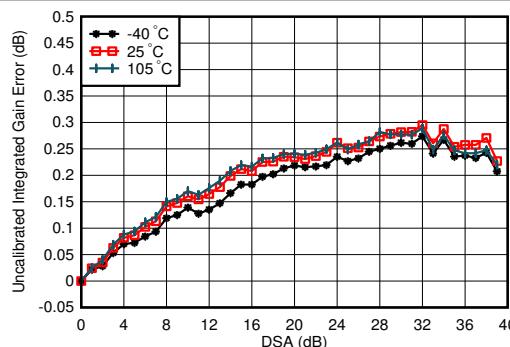
#### 4.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



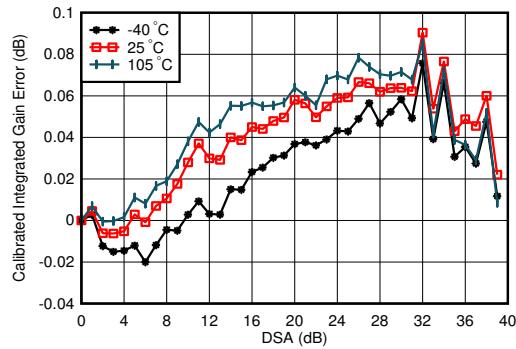
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-9. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz**



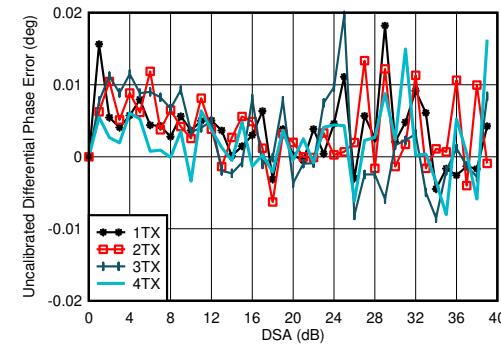
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} ) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 4-10. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} ) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 4-11. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz**

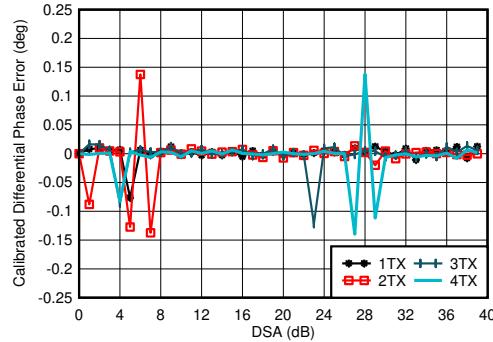


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-12. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz**

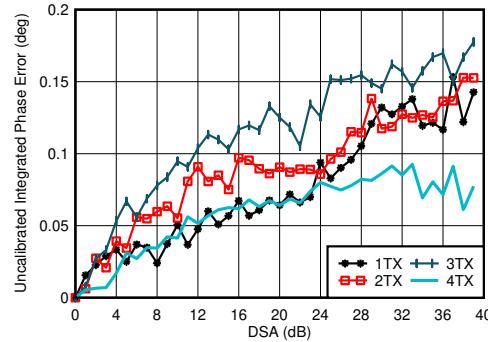
#### 4.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



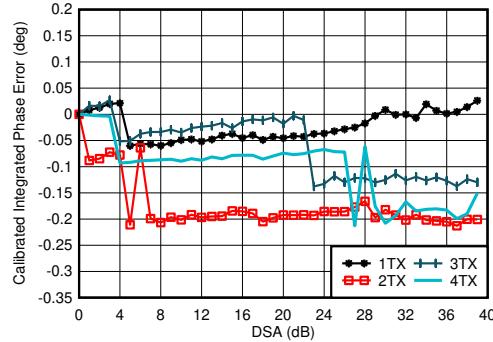
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
 Phase DNL spike may occur at any DSA setting.

**Figure 4-13. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz**



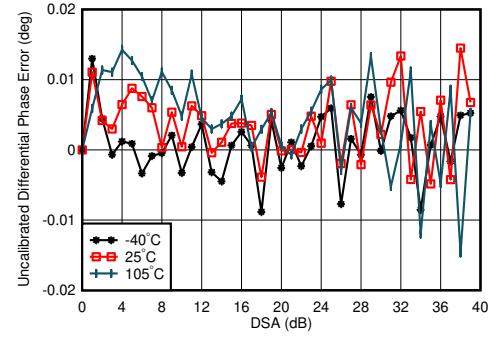
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 4-14. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 4-15. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz**

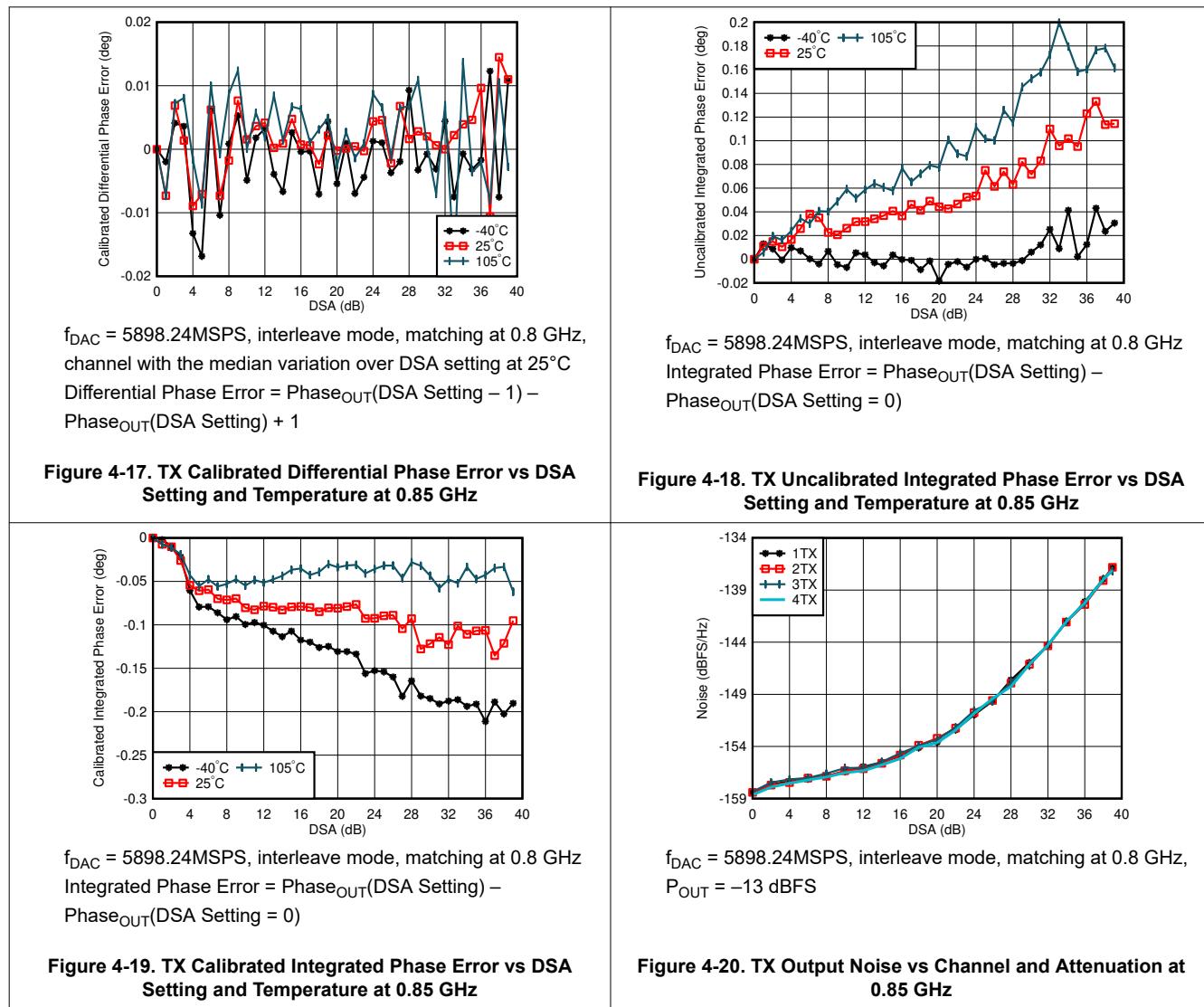


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-16. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz**

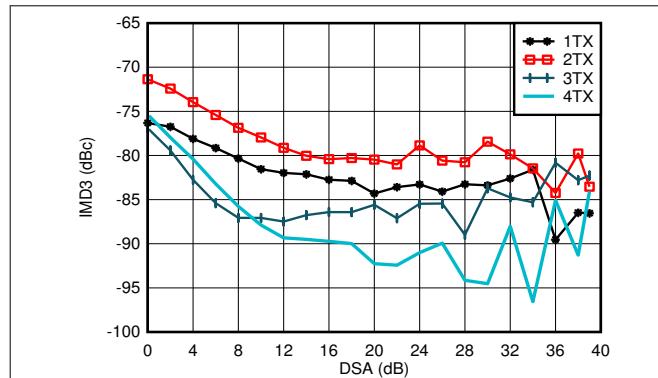
#### 4.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



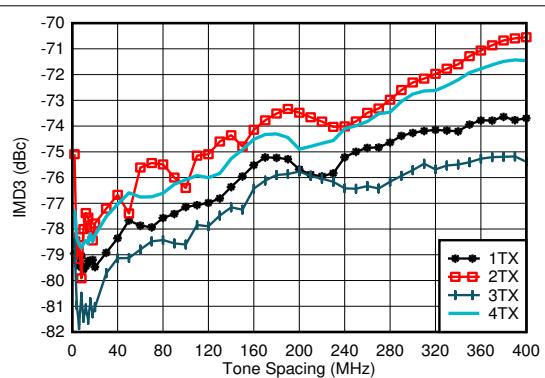
#### 4.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



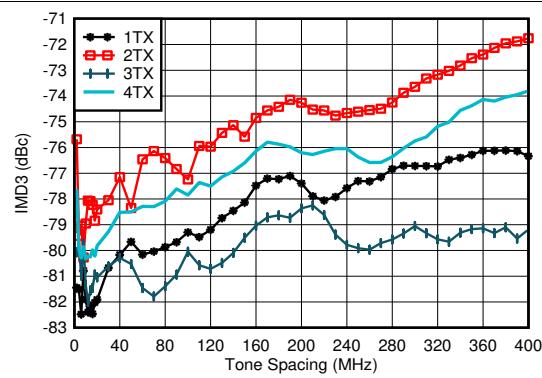
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 0.85 \text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone

Figure 4-21. TX IMD3 vs DSA Setting at 0.85 GHz



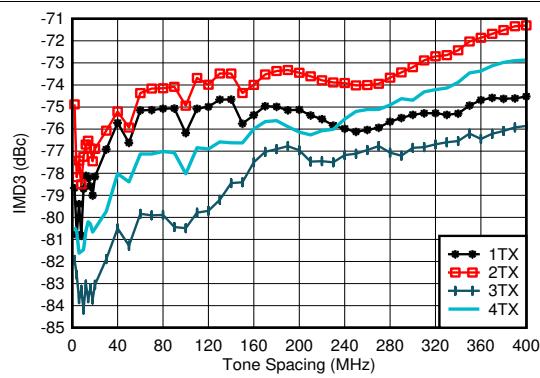
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85 \text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone

Figure 4-22. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



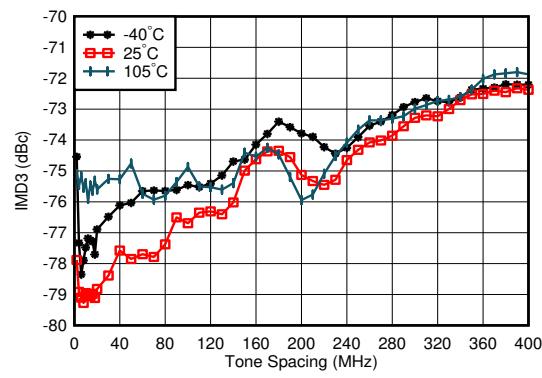
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85 \text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone

Figure 4-23. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



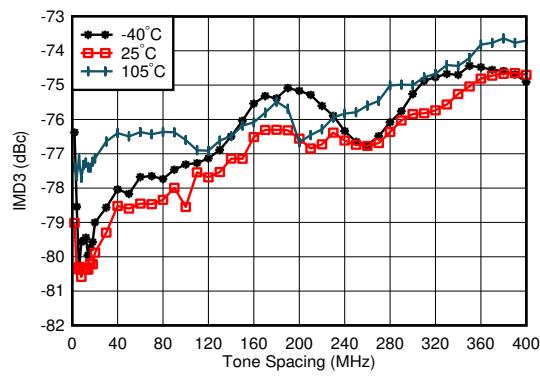
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 0.85 \text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone

Figure 4-24. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85 \text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone, worst channel

Figure 4-25. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

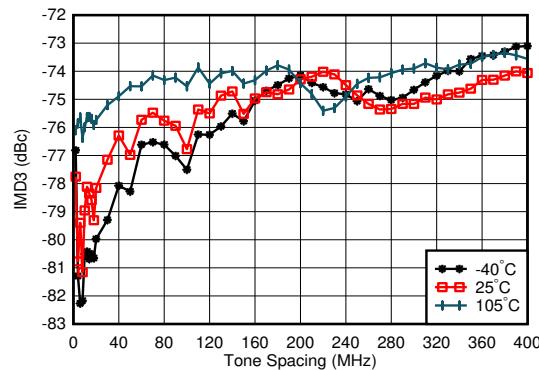


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85 \text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone, worst channel

Figure 4-26. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

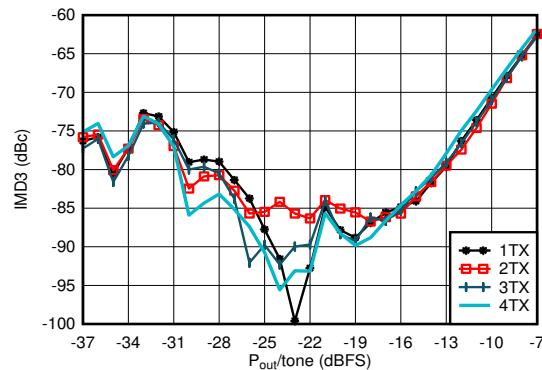
#### 4.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



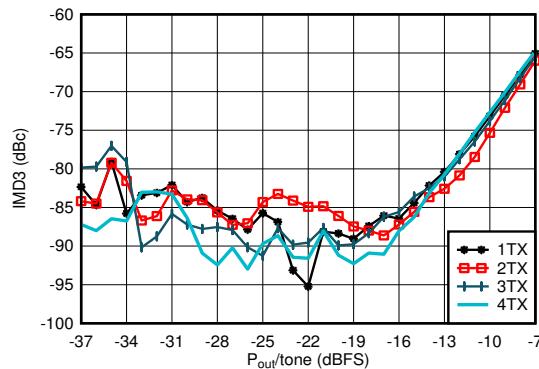
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85 \text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone, worst channel

**Figure 4-27. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz**



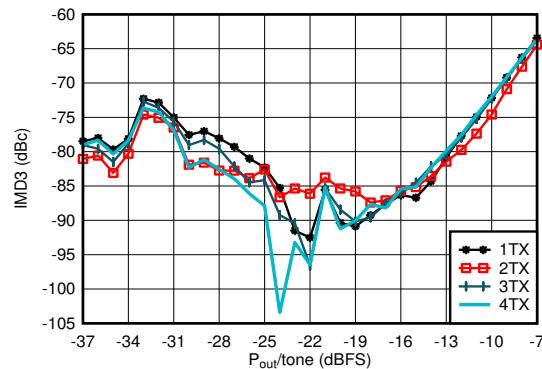
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85 \text{ GHz}$ ,  $f_{\text{SPACING}} = 20 \text{ MHz}$ , matching at 0.8 GHz

**Figure 4-28. TX IMD3 vs Digital Level at 0.85 GHz**



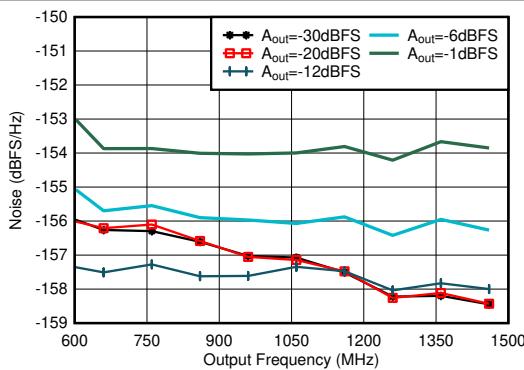
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85 \text{ GHz}$ ,  $f_{\text{SPACING}} = 20 \text{ MHz}$ , matching at 0.8 GHz

**Figure 4-29. TX IMD3 vs Digital Level at 0.85 GHz**



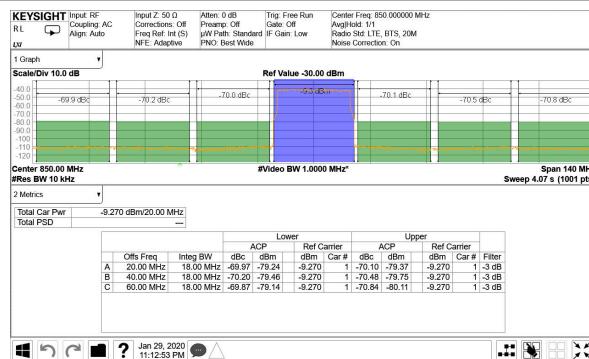
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 0.85 \text{ GHz}$ ,  $f_{\text{SPACING}} = 20 \text{ MHz}$ , matching at 0.8 GHz

**Figure 4-30. TX IMD3 vs Digital Level at 0.85 GHz**



Matching at 2.6 GHz, Single tone,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, 40-MHz offset, DSA = 0dB

**Figure 4-31. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz**



TM1.1,  $P_{\text{OUT\_RMS}} = -13 \text{ dBFS}$

**Figure 4-32. TX 20-MHz LTE Output Spectrum at 0.85 GHz**

#### 4.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

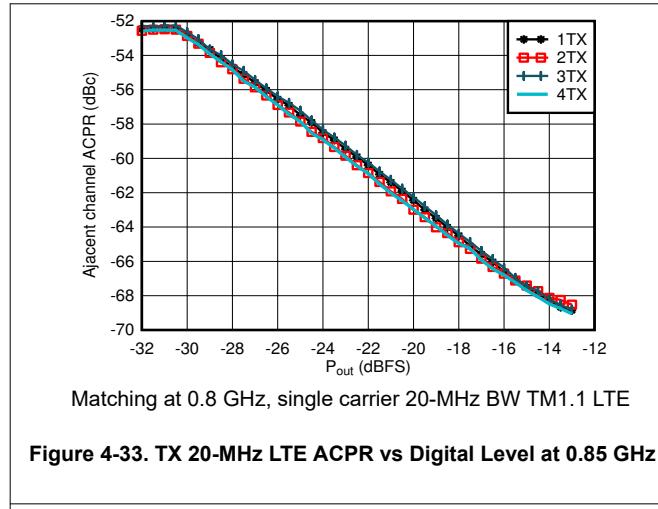


Figure 4-33. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz

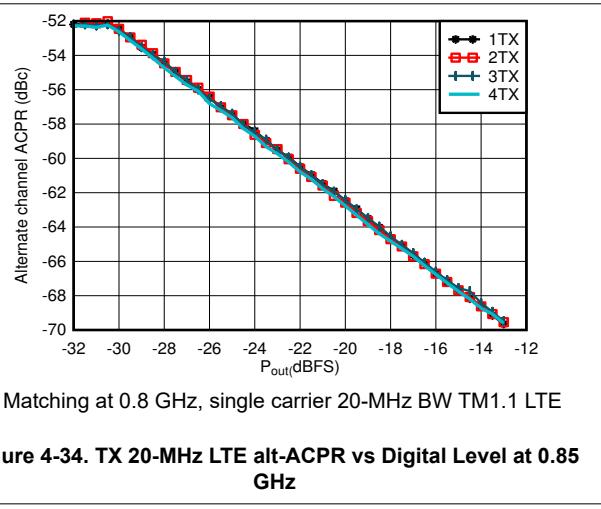


Figure 4-34. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz

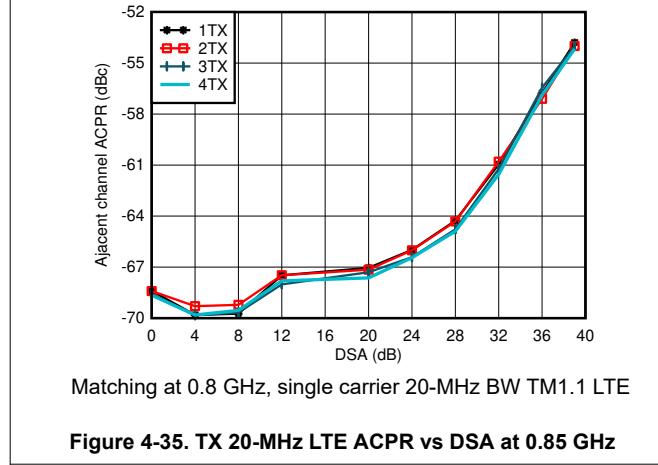


Figure 4-35. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz

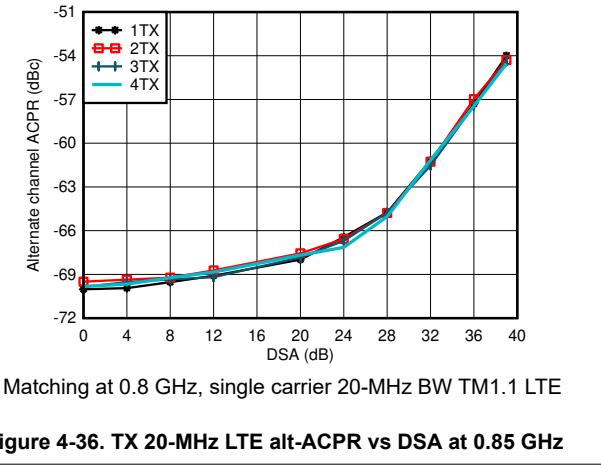


Figure 4-36. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz

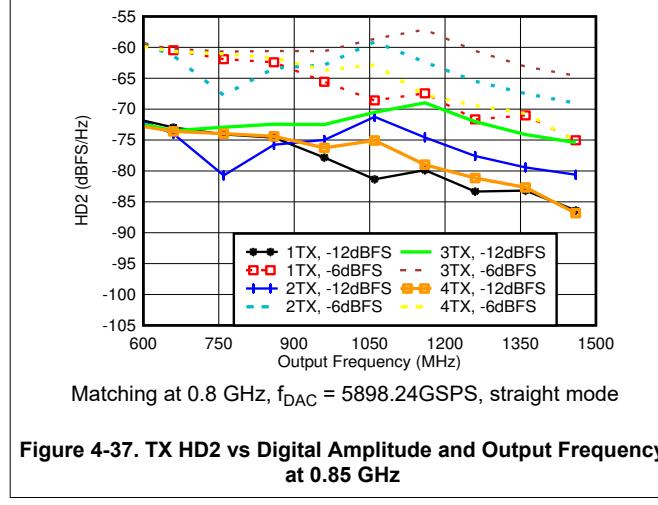


Figure 4-37. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz

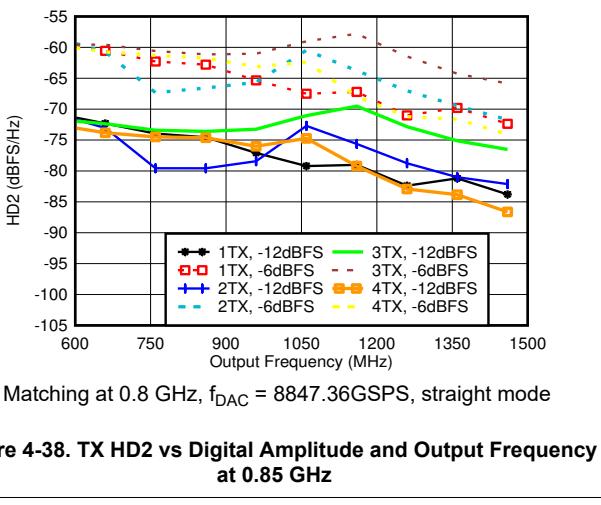
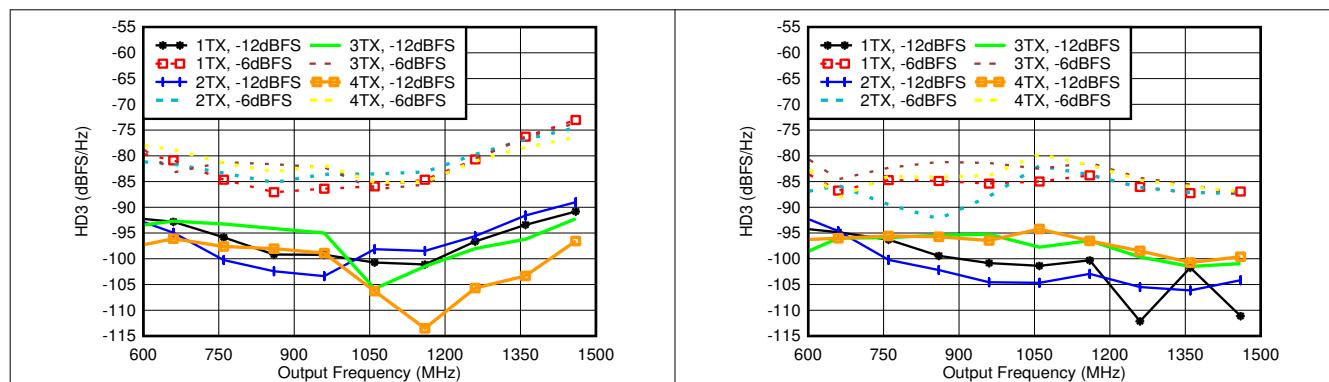


Figure 4-38. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz

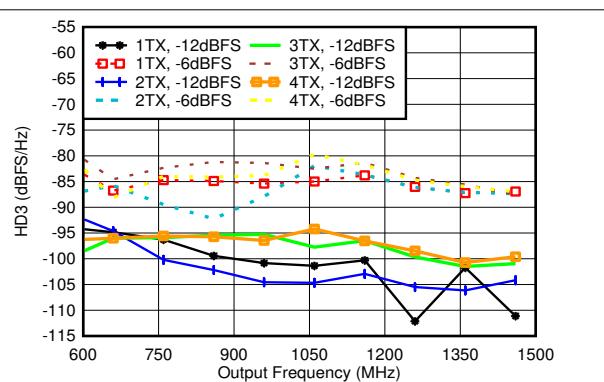
#### 4.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



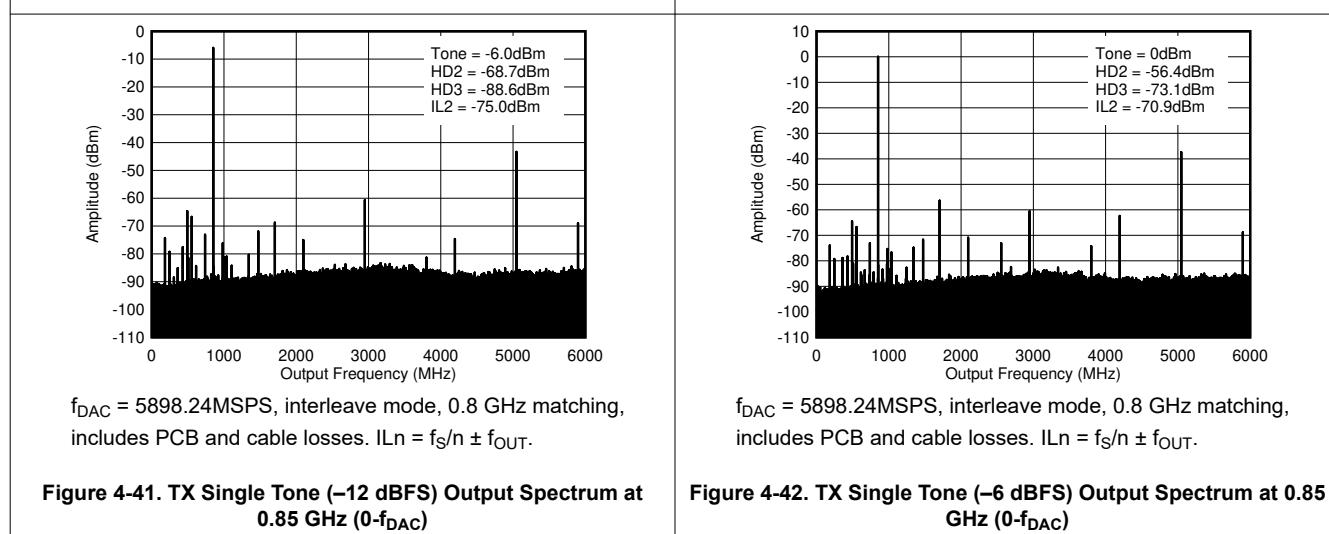
Matching at 0.8 GHz,  $f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode, normalized to output power at harmonic frequency

**Figure 4-39. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz**



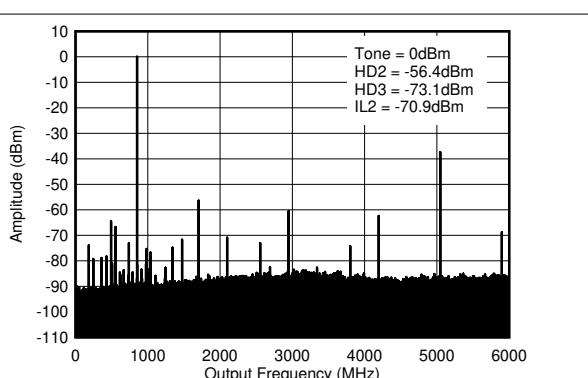
Matching at 0.8 GHz,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, normalized to output power at harmonic frequency

**Figure 4-40. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz**



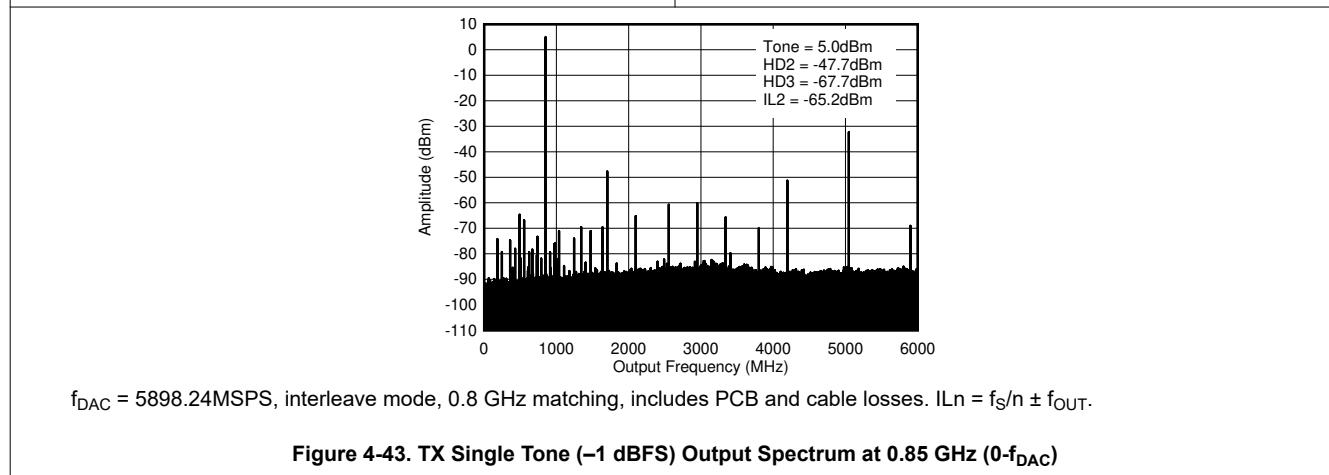
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ .

**Figure 4-41. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz (0-f<sub>DAC</sub>)**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ .

**Figure 4-42. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz (0-f<sub>DAC</sub>)**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ .

**Figure 4-43. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz (0-f<sub>DAC</sub>)**

#### 4.12.2 TX Typical Characteristics at 1.8 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

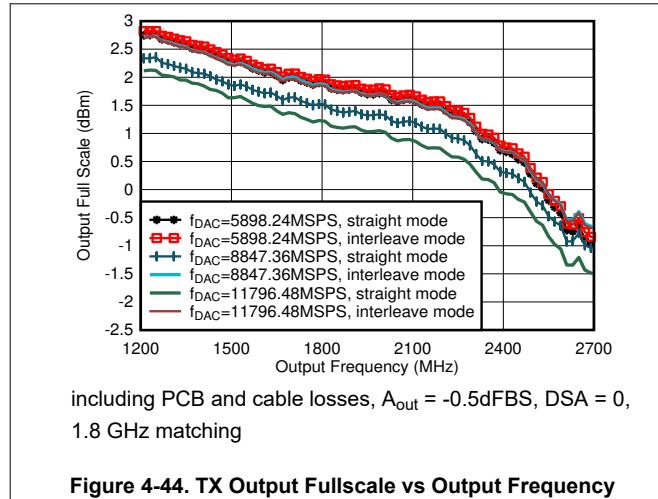


Figure 4-44. TX Output Fullscale vs Output Frequency

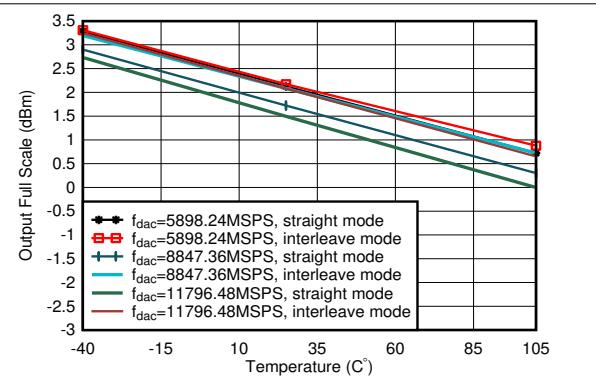


Figure 4-45. TX Output Power vs Temperature at 1.8 GHz

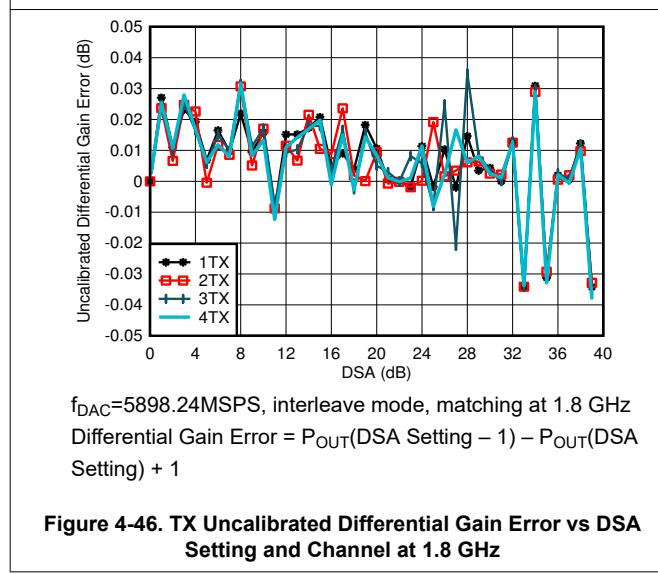


Figure 4-46. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz

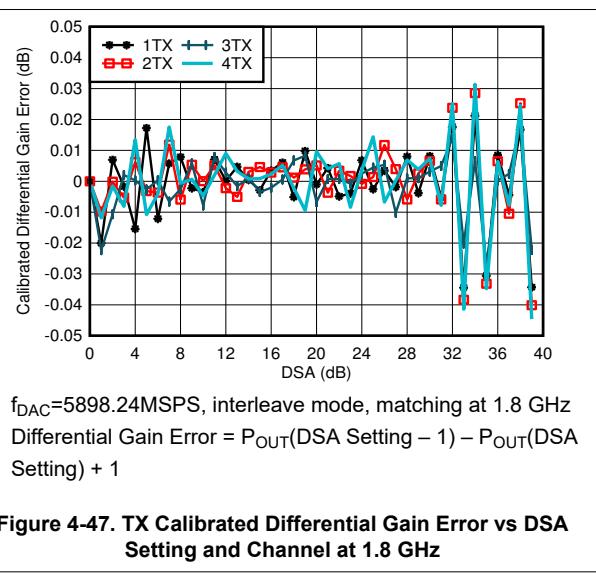
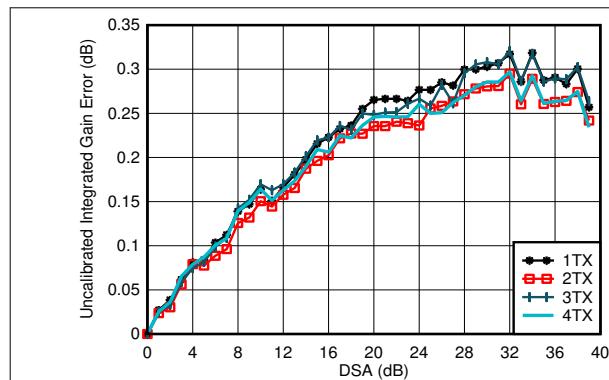


Figure 4-47. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz

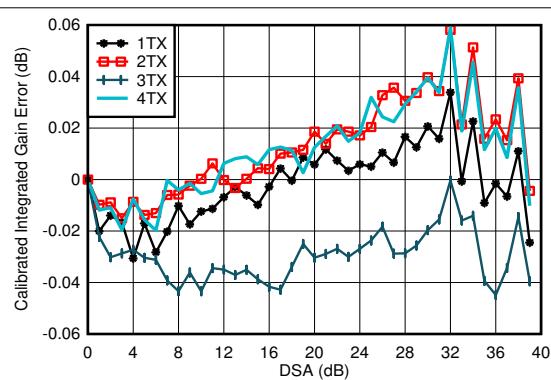
#### 4.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



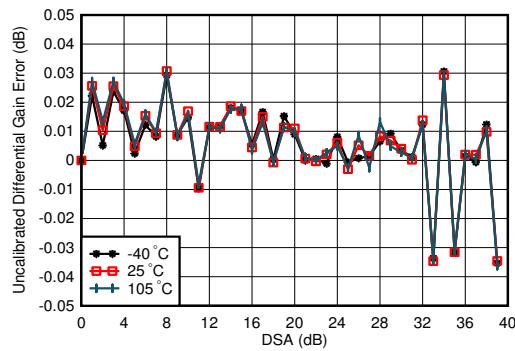
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-48. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz**



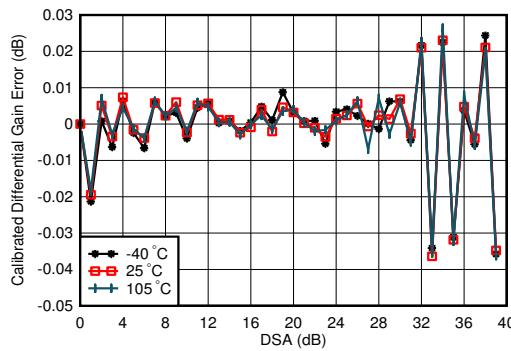
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-49. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-50. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz**

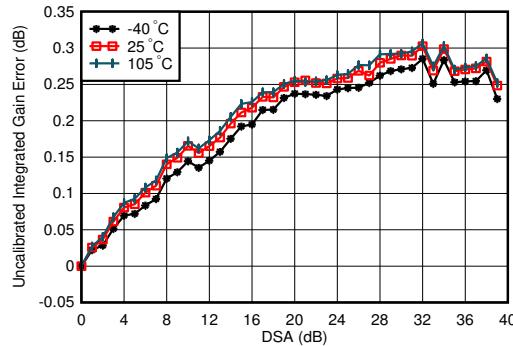


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-51. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz**

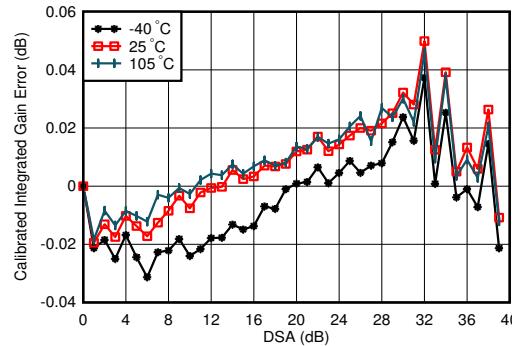
#### 4.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



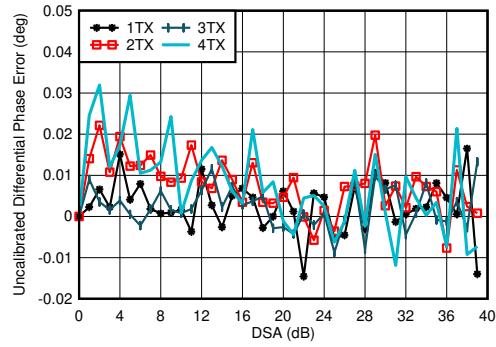
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-52. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz**



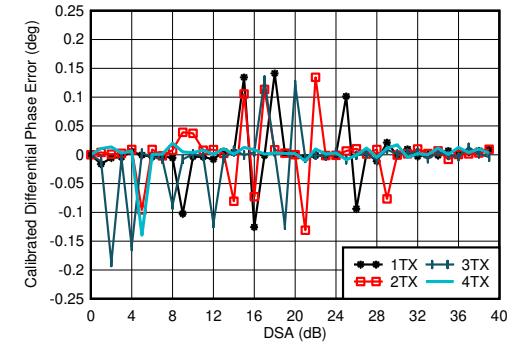
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-53. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-54. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz**

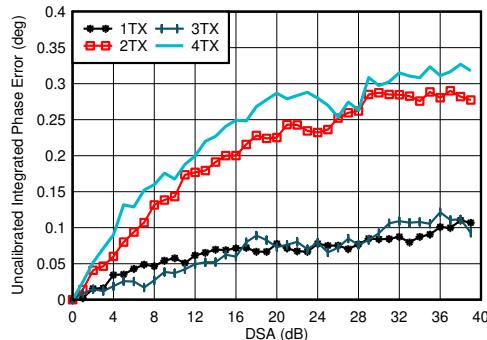


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
 Phase DNL spike may occur at any DSA setting.

**Figure 4-55. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz**

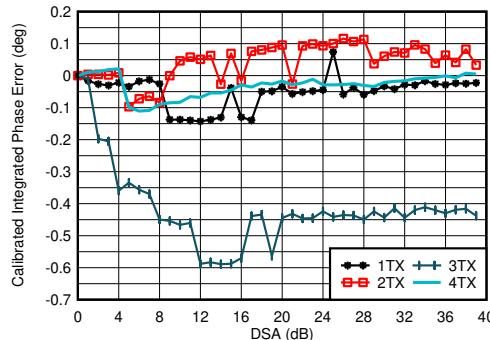
#### 4.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



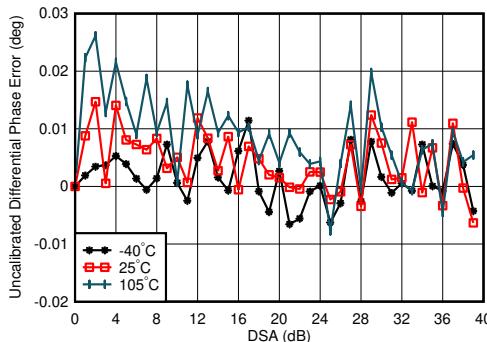
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 4-56. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz**



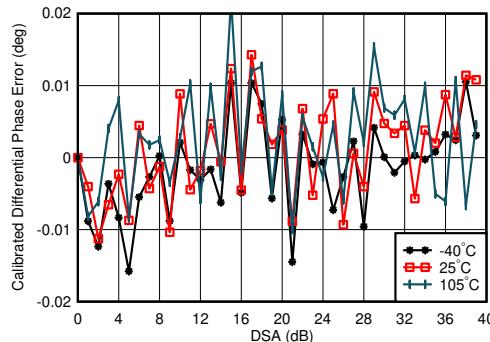
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 4-57. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Differential Phase Error = Phase<sub>OUT</sub>(DSA Setting – 1) – Phase<sub>OUT</sub>(DSA Setting)

**Figure 4-58. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz**

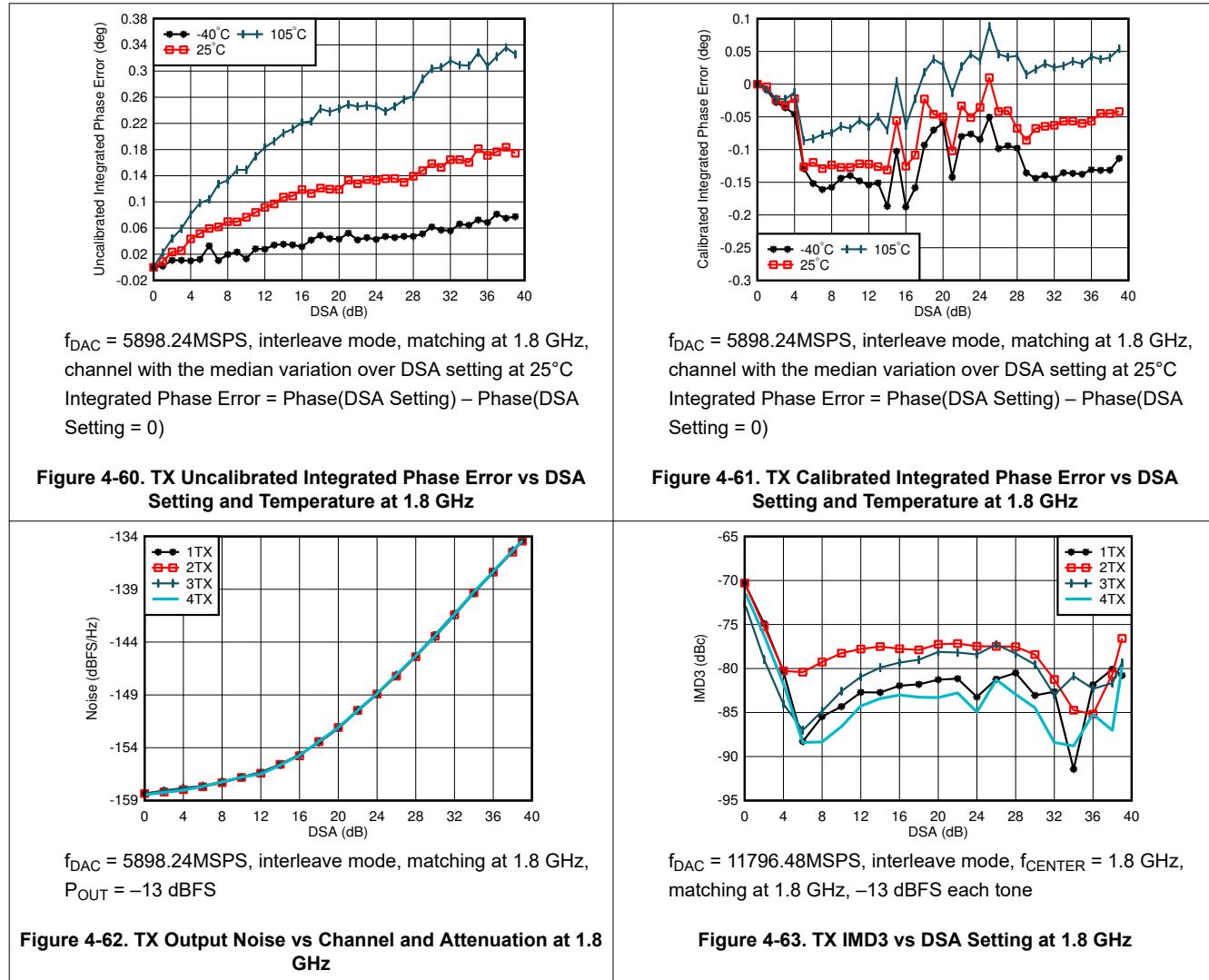


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz,  
channel with the median variation over DSA setting at 25°C  
Differential Phase Error = Phase<sub>OUT</sub>(DSA Setting – 1) – Phase<sub>OUT</sub>(DSA Setting)

**Figure 4-59. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz**

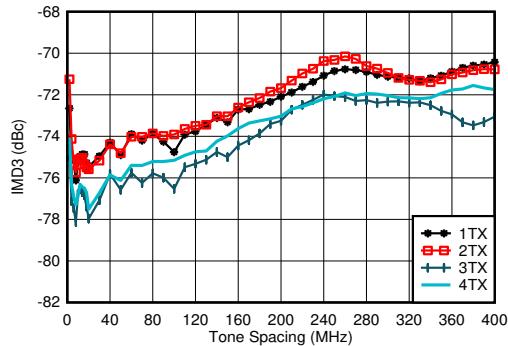
#### 4.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



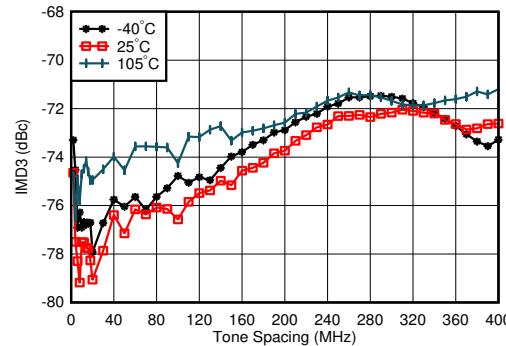
#### 4.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



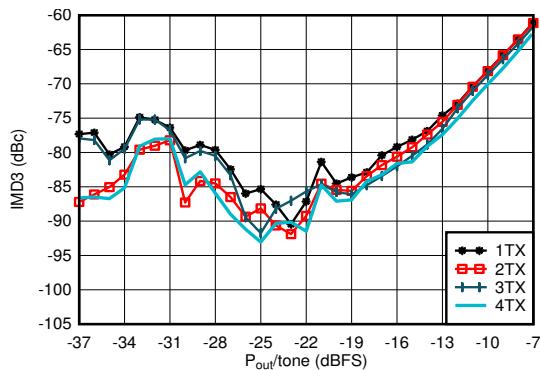
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 1.8 \text{ GHz}$ , matching at 1.8 GHz,  $-13 \text{ dBFS}$  each tone

Figure 4-64. TX IMD3 vs Tone Spacing and Channel at 1.8 GHz



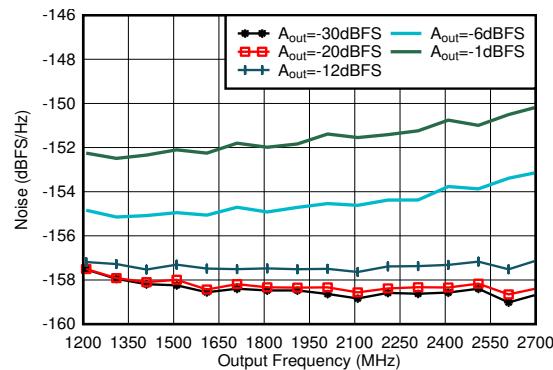
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 1.8 \text{ GHz}$ , matching at 1.8 GHz,  $-13 \text{ dBFS}$  each tone, worst channel

Figure 4-65. TX IMD3 vs Tone Spacing and Temperature at 1.8 GHz



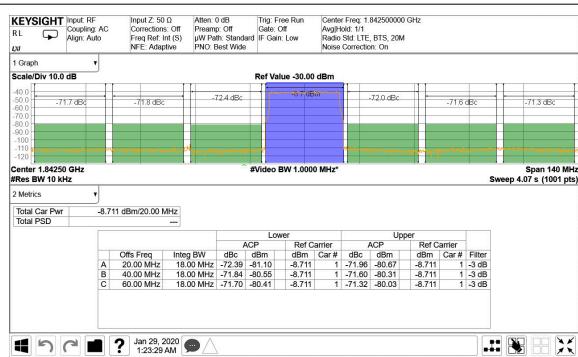
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 1.8 \text{ GHz}$ ,  $f_{\text{SPACING}} = 20 \text{ MHz}$ , matching at 1.8 GHz

Figure 4-66. TX IMD3 vs Digital Level at 1.8 GHz



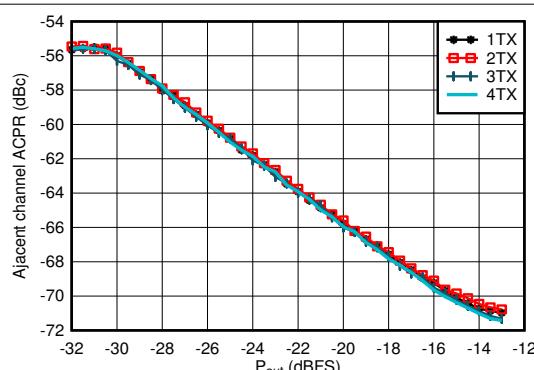
Matching at 2.6 GHz, Single tone,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, 40-MHz offset

Figure 4-67. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz



TM1.1,  $P_{\text{OUT RMS}} = -13 \text{ dBFS}$

Figure 4-68. TX 20-MHz LTE Output Spectrum at 1.8425 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 4-69. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz

#### 4.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

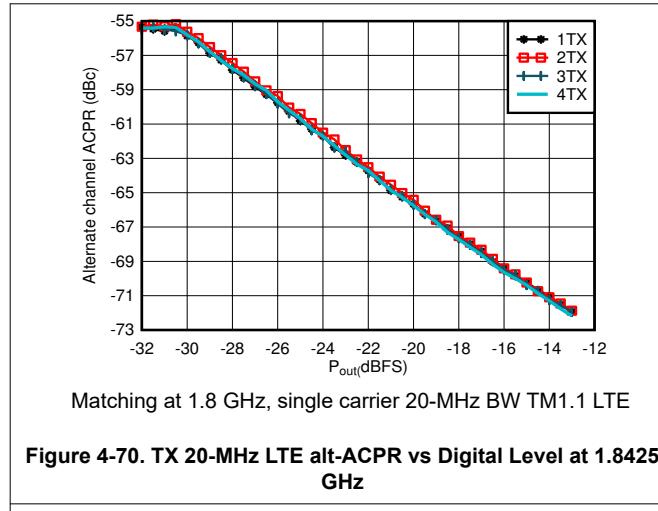


Figure 4-70. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz

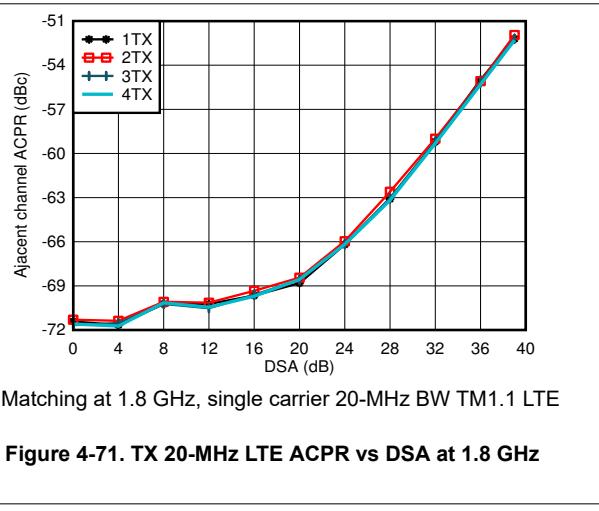


Figure 4-71. TX 20-MHz LTE ACPR vs DSA at 1.8 GHz

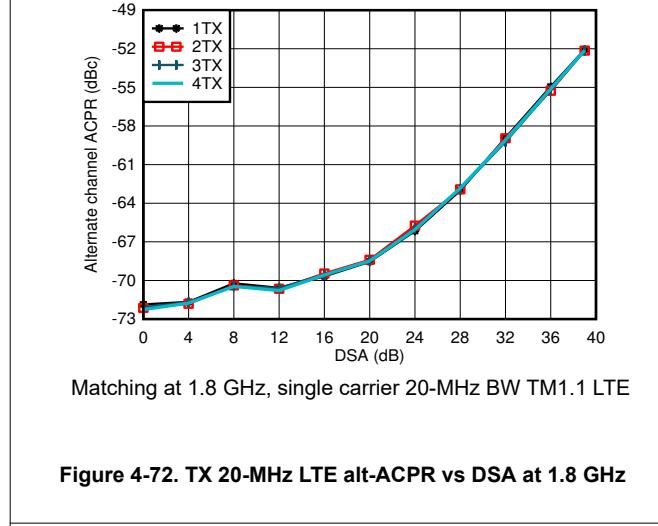


Figure 4-72. TX 20-MHz LTE alt-ACPR vs DSA at 1.8 GHz

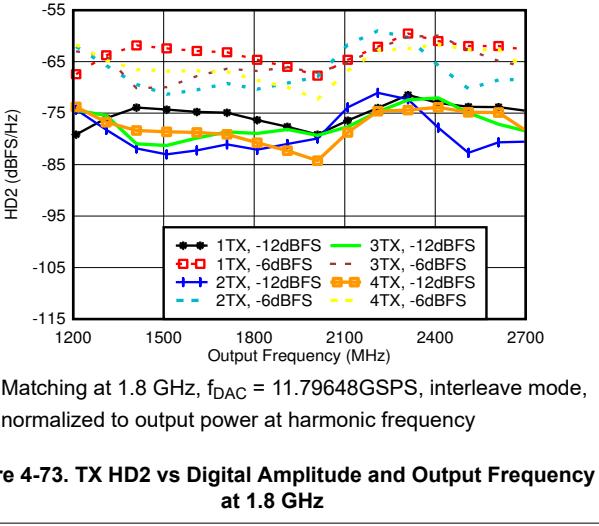


Figure 4-73. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz

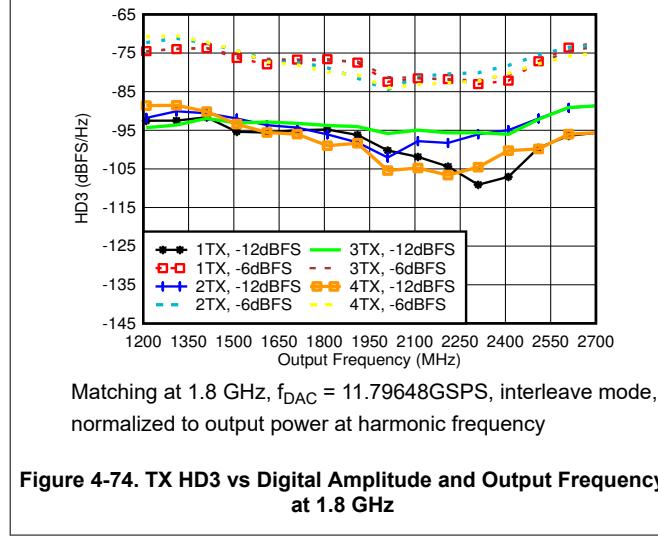


Figure 4-74. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz

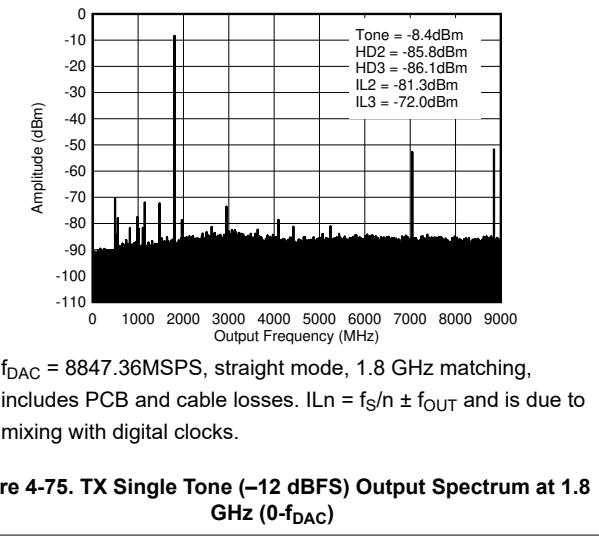
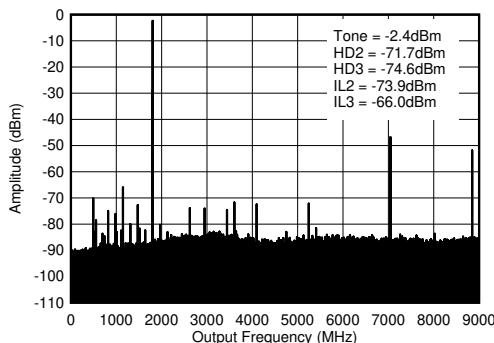


Figure 4-75. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz (0- $f_{\text{DAC}}$ )

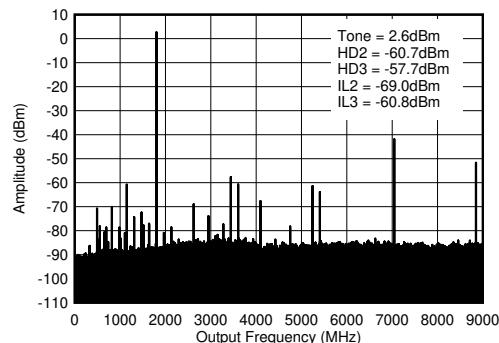
#### 4.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 4-76. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz (0- $f_{\text{DAC}}$ )**

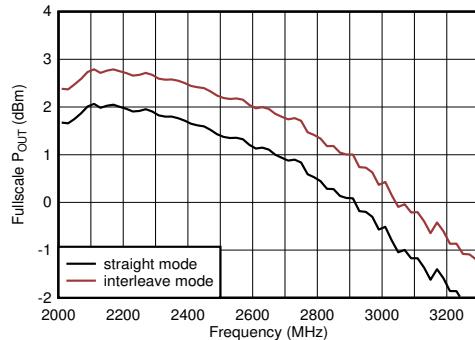


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 4-77. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz (0- $f_{\text{DAC}}$ )**

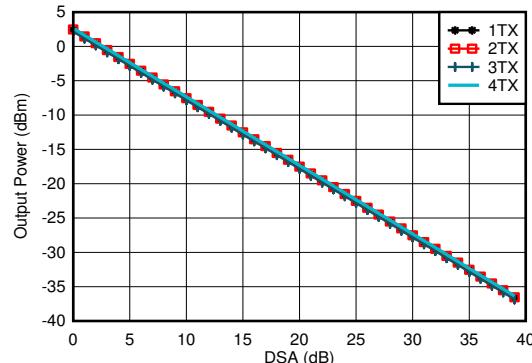
#### 4.12.3 TX Typical Characteristics at 2.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



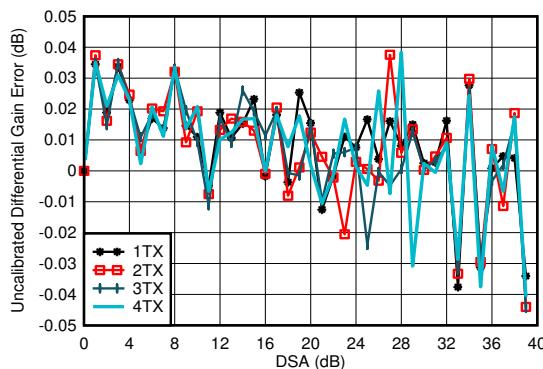
Including PCB and cable losses,  $A_{\text{out}} = -0.5 \text{ dBFS}$ , DSA = 0,  
2.6 GHz matching

Figure 4-78. TX Full Scale vs RF Frequency at 11796.48MSPS



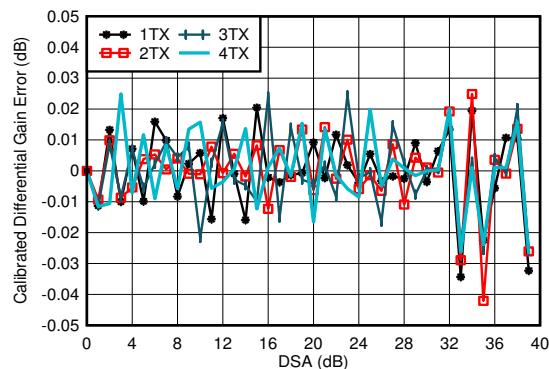
$f_{\text{DAC}} = 8847.36 \text{ MSPS}$ ,  $A_{\text{out}} = -0.5 \text{ dBFS}$ , matching 2.6 GHz

Figure 4-79. TX Output Power vs DSA Setting and Channel at 2.6 GHz



$f_{\text{DAC}} = 8847.36 \text{ MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 4-80. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz

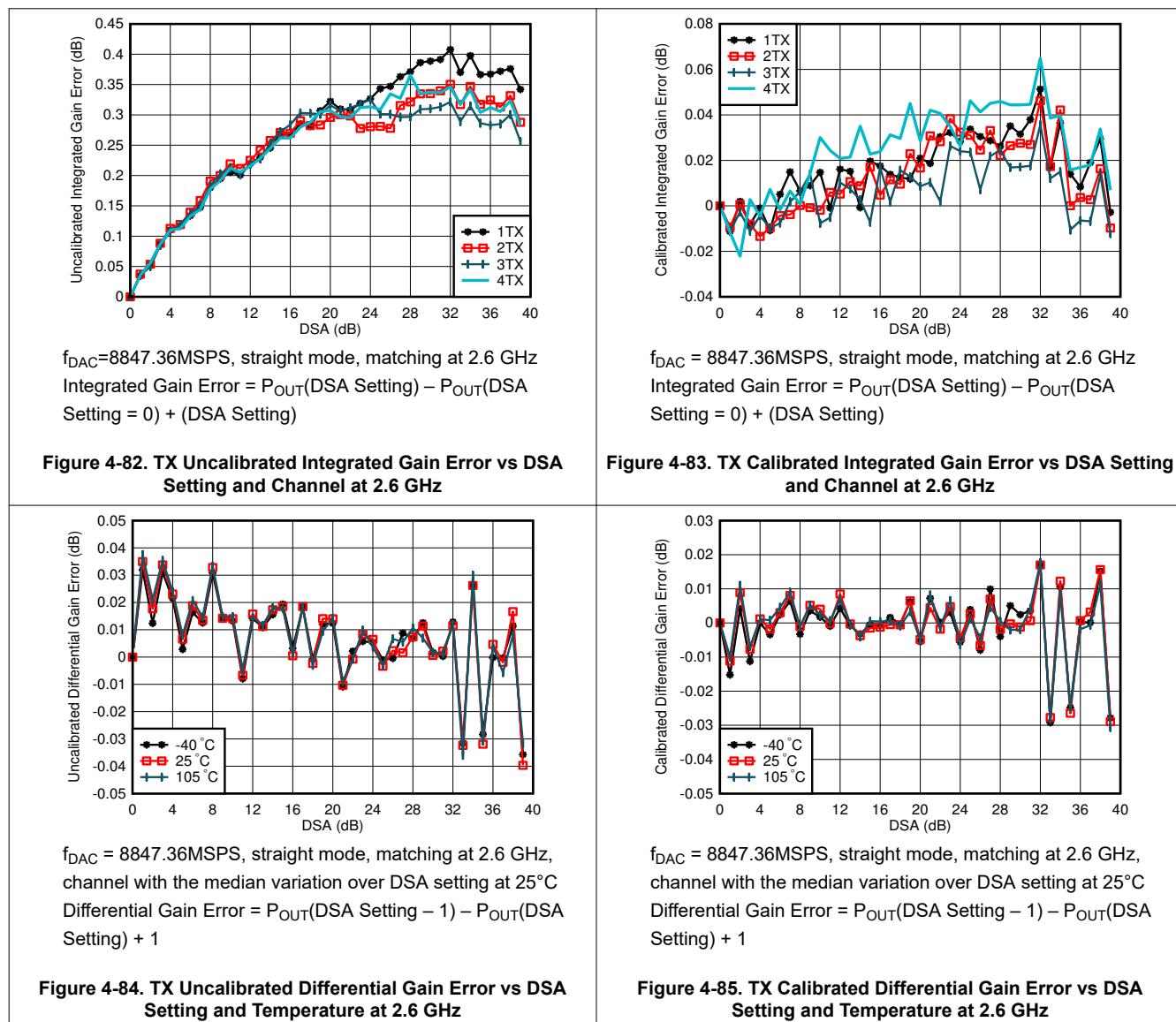


$f_{\text{DAC}} = 8847.36 \text{ MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 4-81. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz

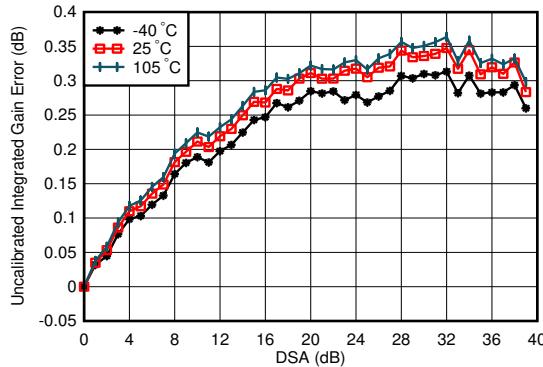
#### 4.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



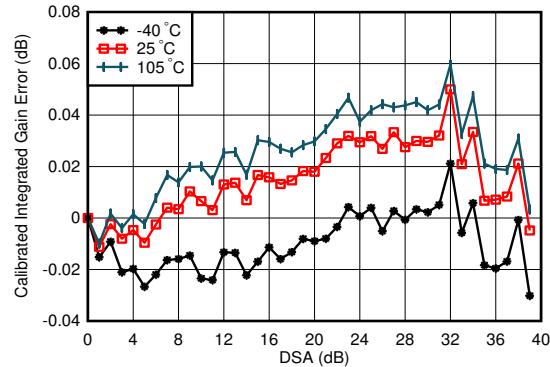
#### 4.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



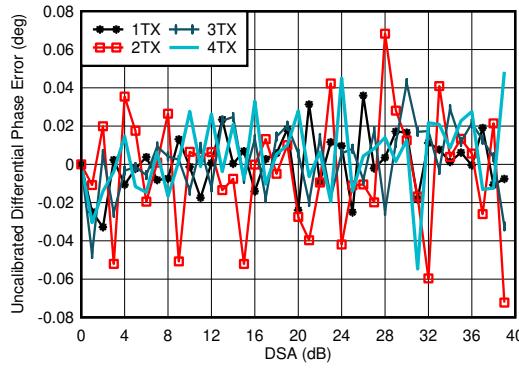
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-86. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz**



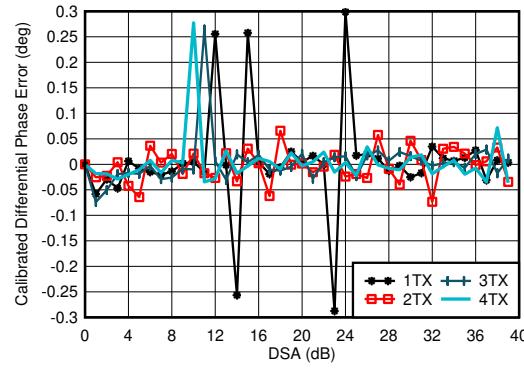
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-87. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-88. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz**

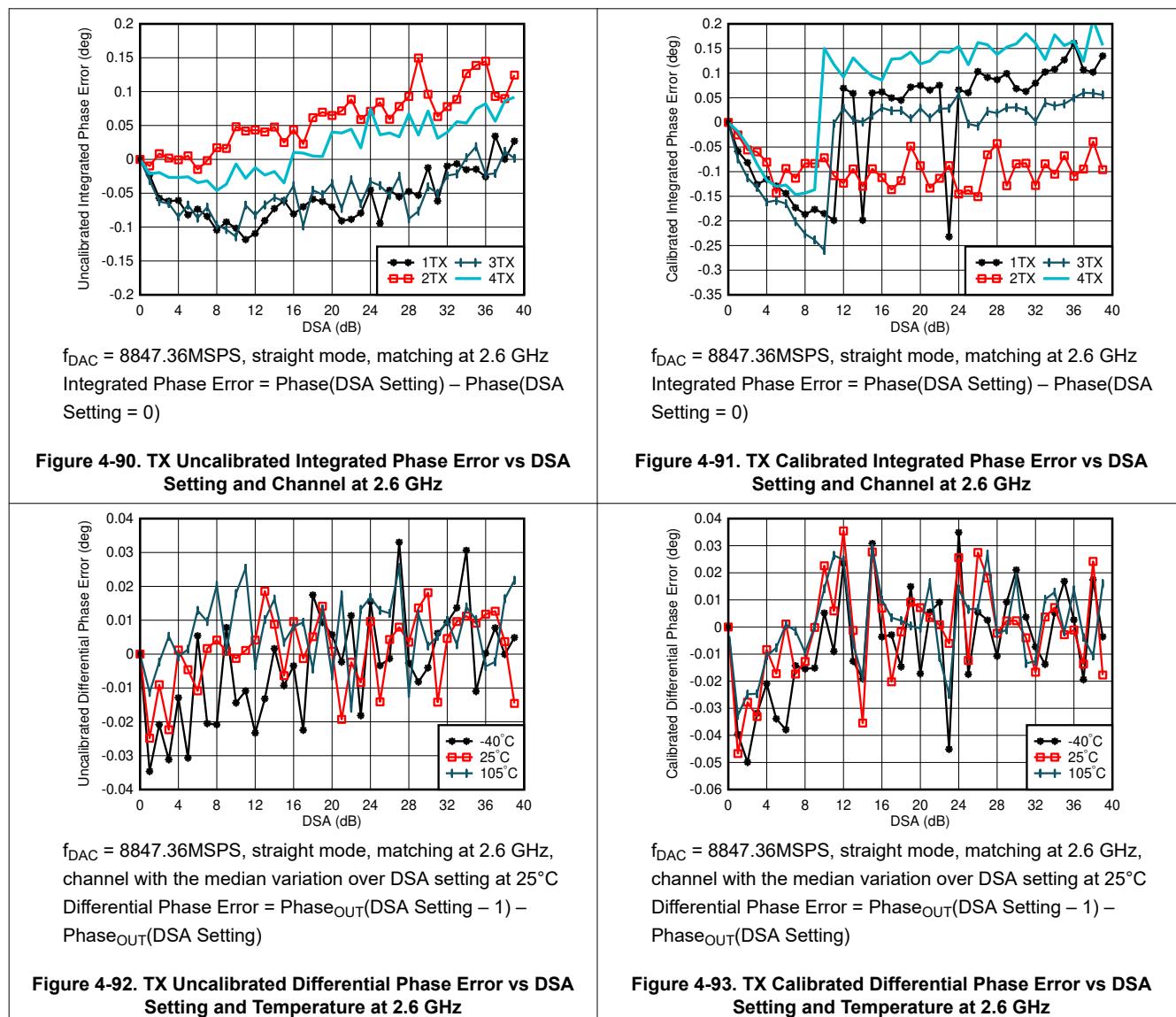


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
Phase DNL spike may occur at any DSA setting.

**Figure 4-89. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz**

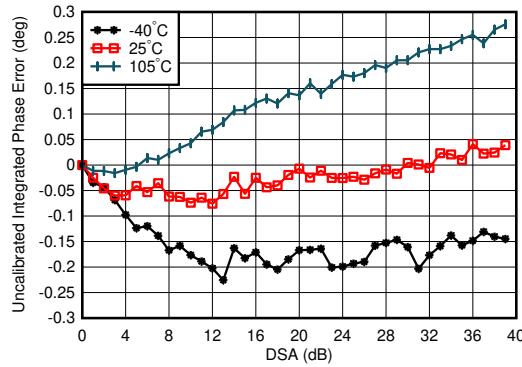
#### 4.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



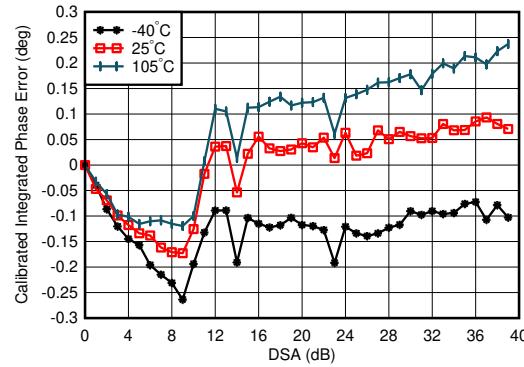
#### 4.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



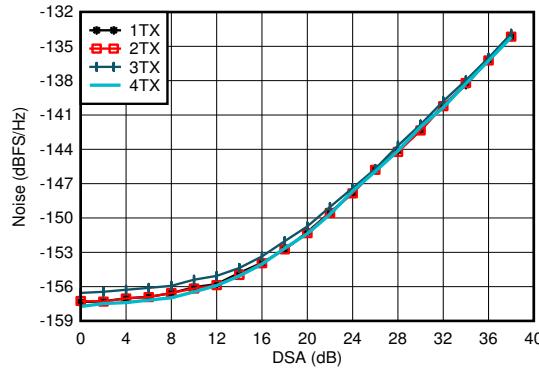
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 4-94. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz**



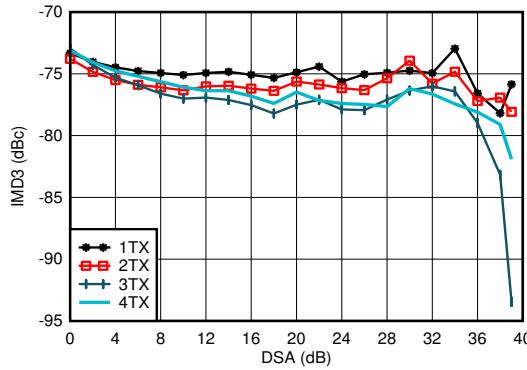
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 4-95. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz,  
 $P_{\text{OUT}} = -13 \text{ dBFS}$

**Figure 4-96. TX Output Noise vs Channel and Attenuation at 2.6 GHz**

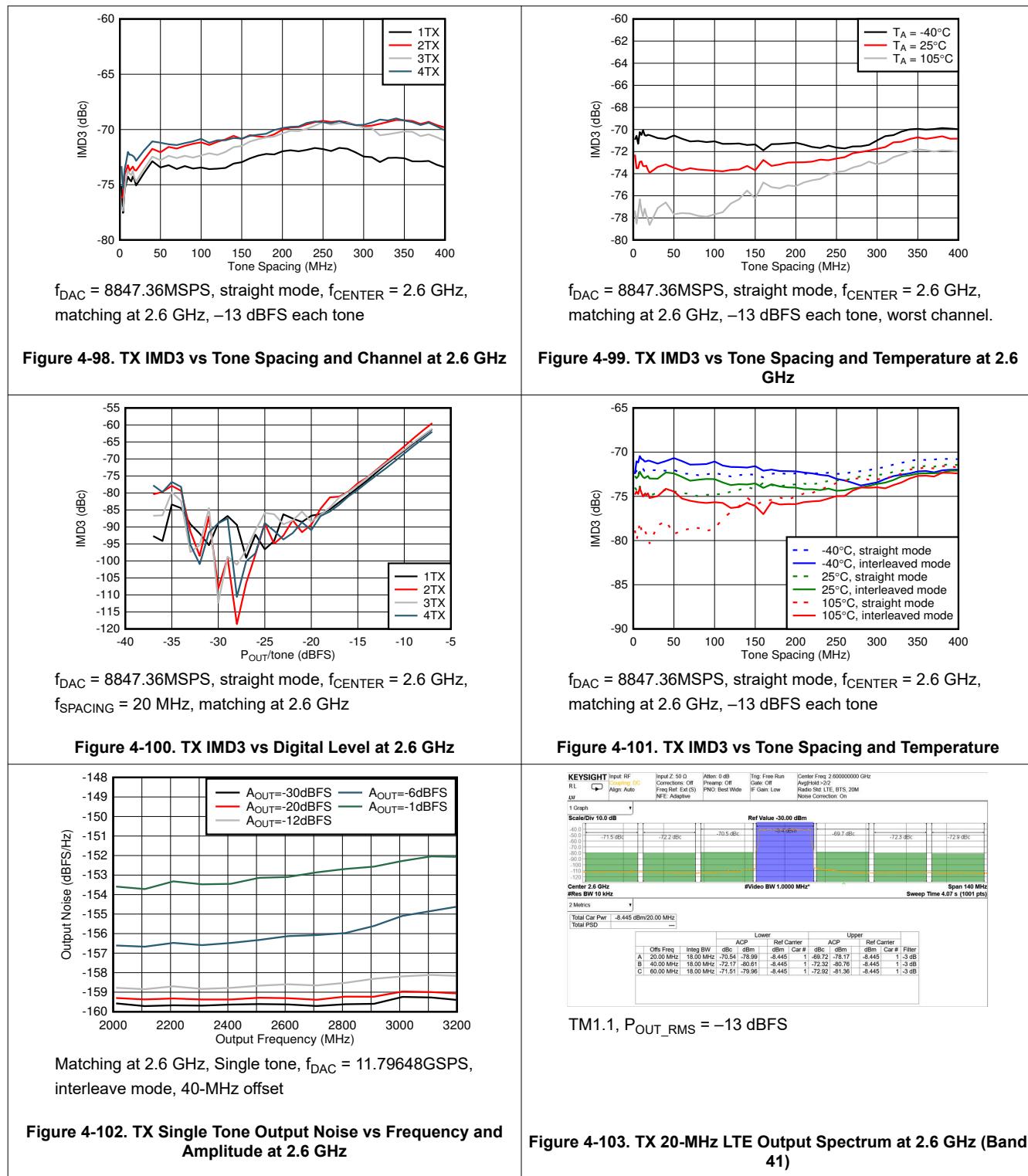


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6 \text{ GHz}$ , matching at 2.6 GHz, -13 dBFS each tone

**Figure 4-97. TX IMD3 vs DSA Setting at 2.6 GHz**

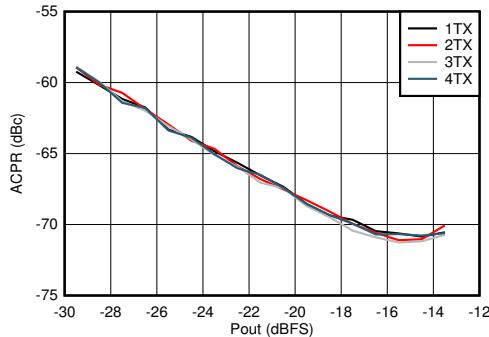
#### 4.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



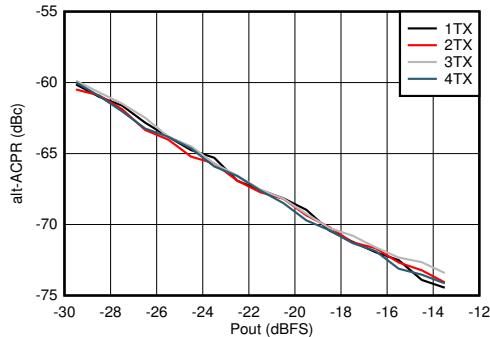
#### 4.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



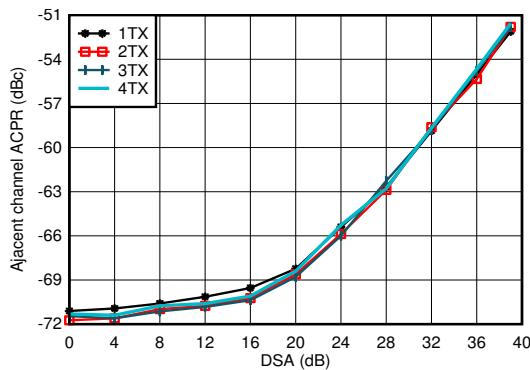
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 4-104. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz



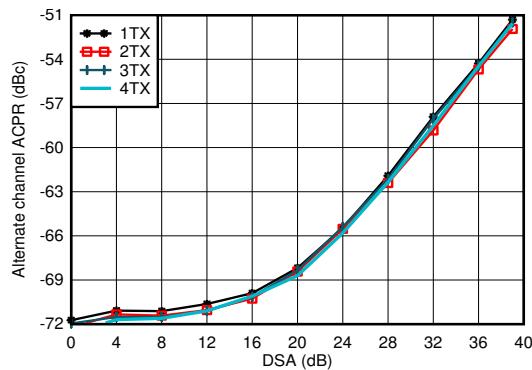
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 4-105. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz



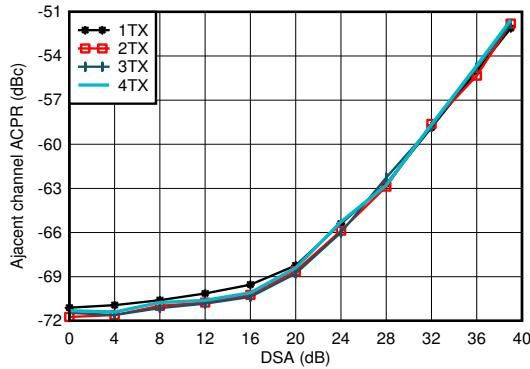
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 4-106. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz



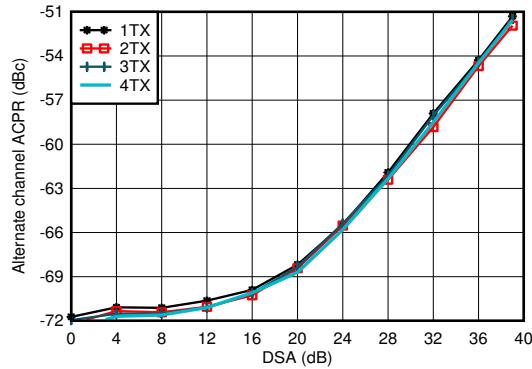
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 4-107. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz



Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 4-108. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz



Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 4-109. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz

#### 4.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

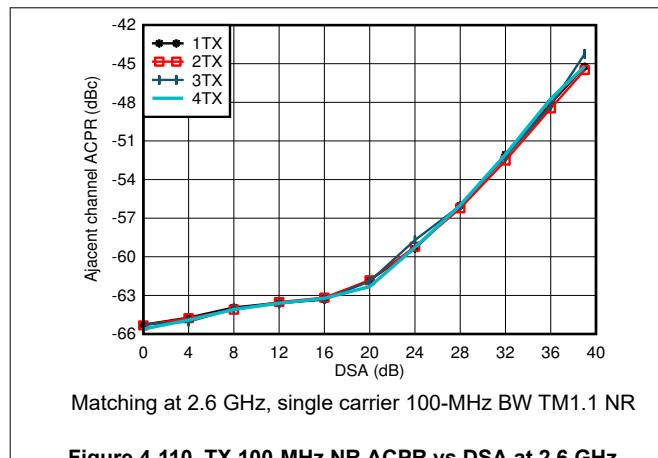


Figure 4-110. TX 100-MHz NR ACPR vs DSA at 2.6 GHz

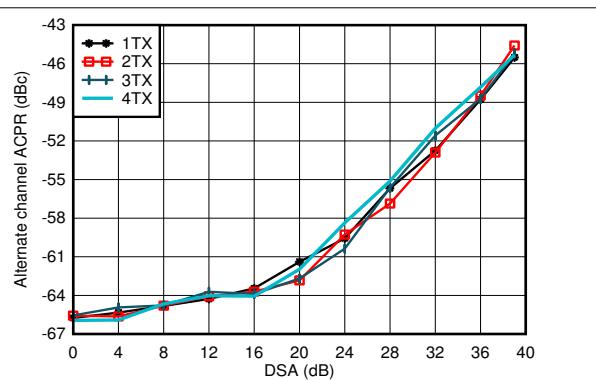


Figure 4-111. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz

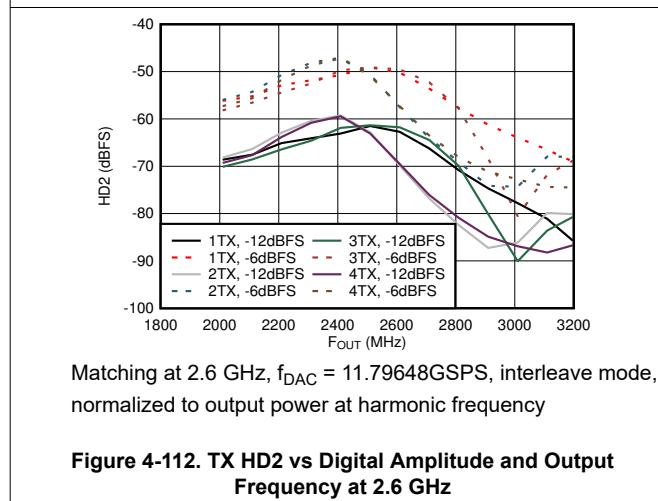


Figure 4-112. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz

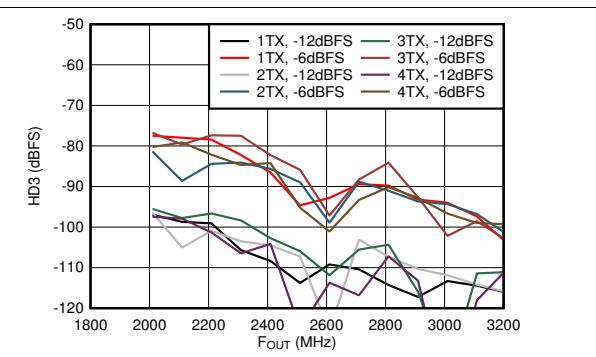
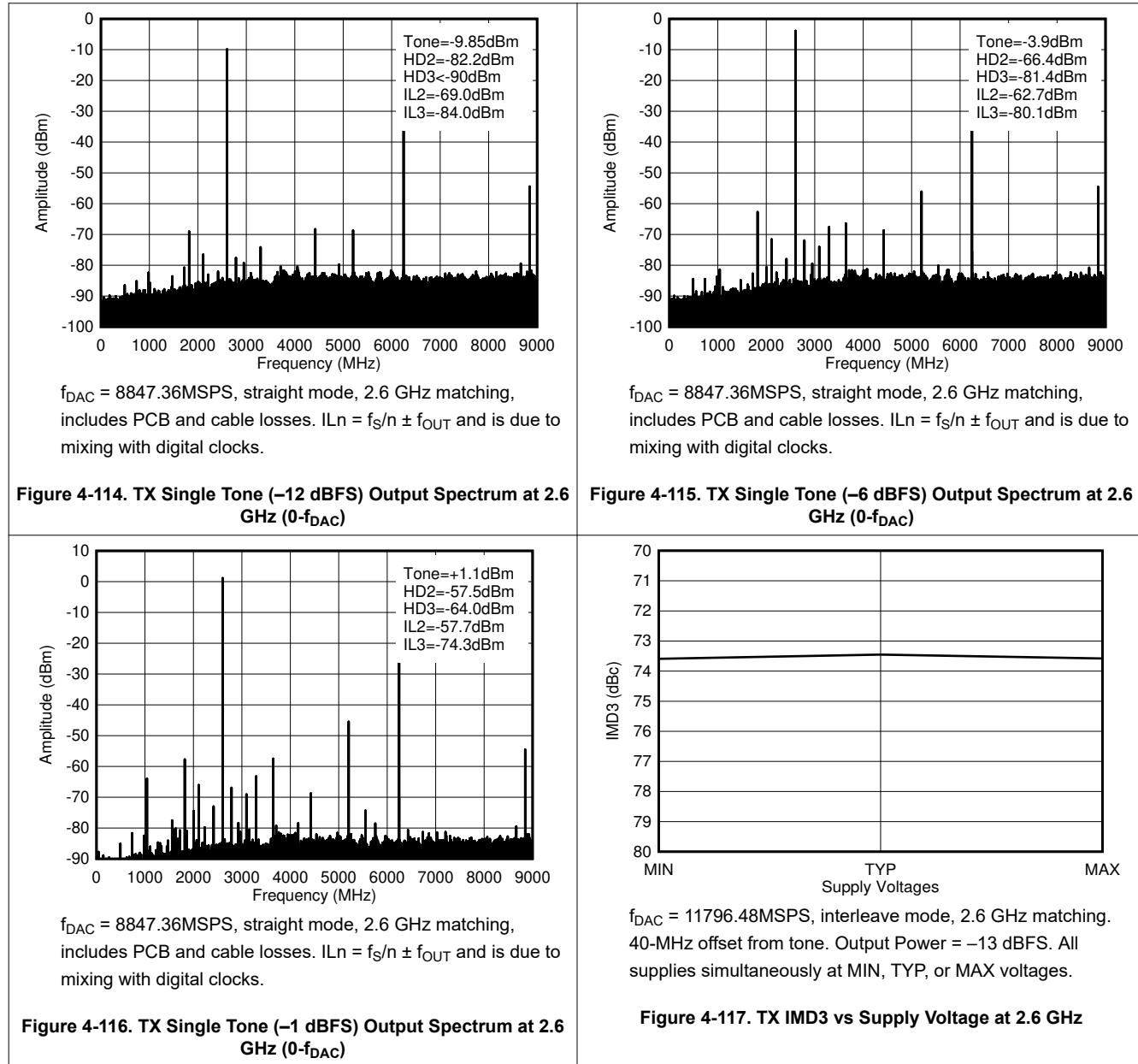


Figure 4-113. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz

#### 4.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



#### 4.12.4 TX Typical Characteristics at 3.5 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

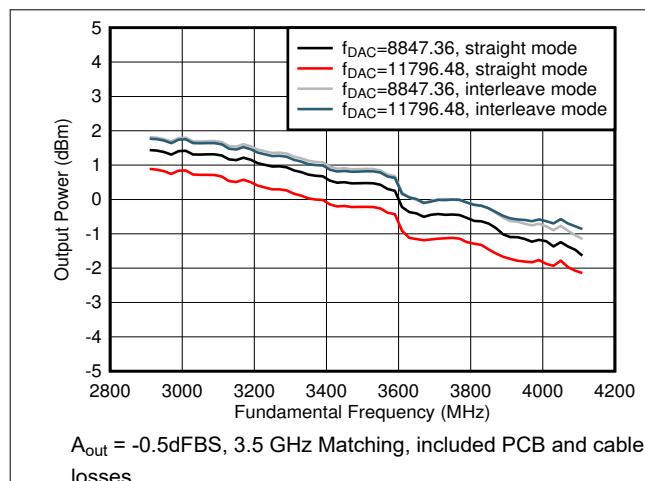


Figure 4-118. TX Output Power vs Frequency

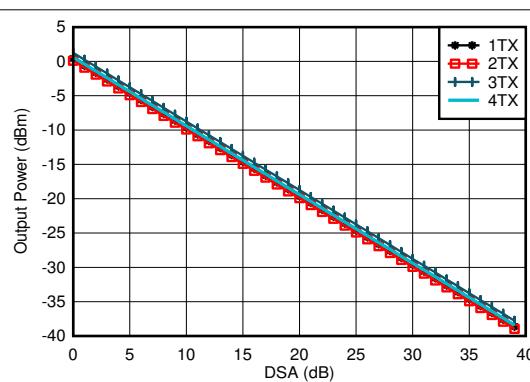


Figure 4-119. TX Output Power vs DSA Setting at 3.5 GHz

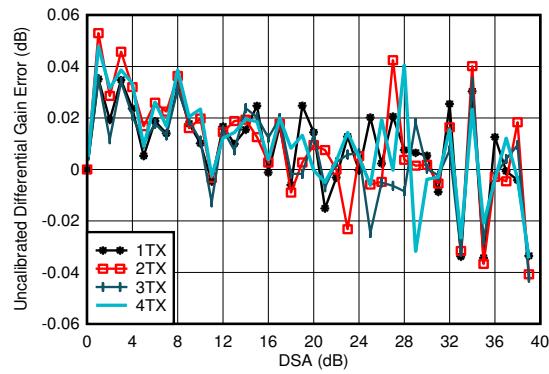


Figure 4-120. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz

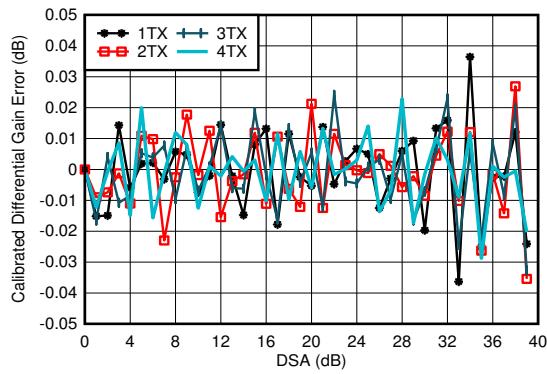
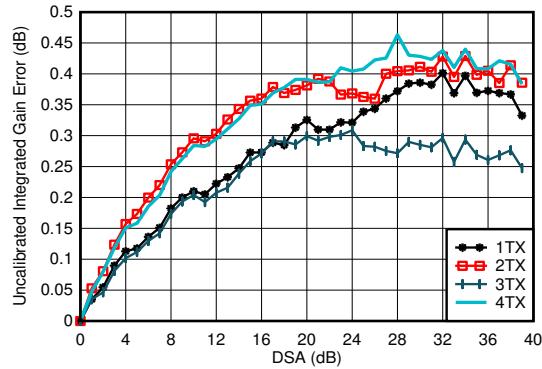


Figure 4-121. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz

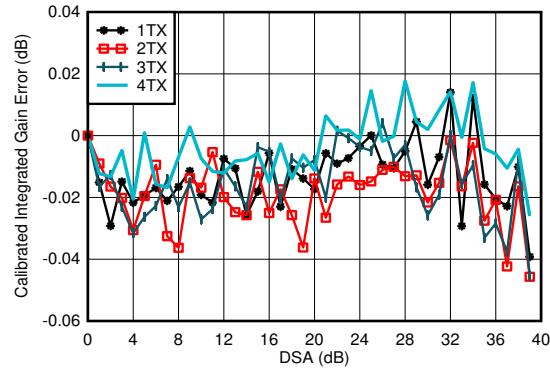
#### 4.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



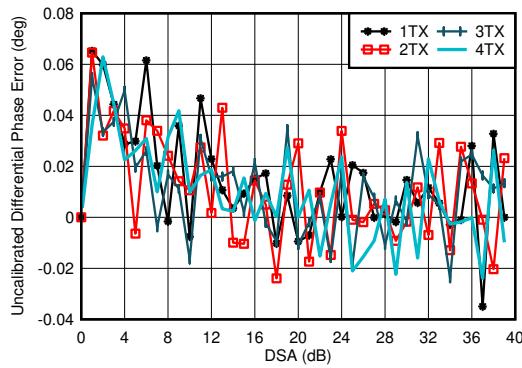
3.5 GHz Matching, included PCB and cable losses  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-122. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz**



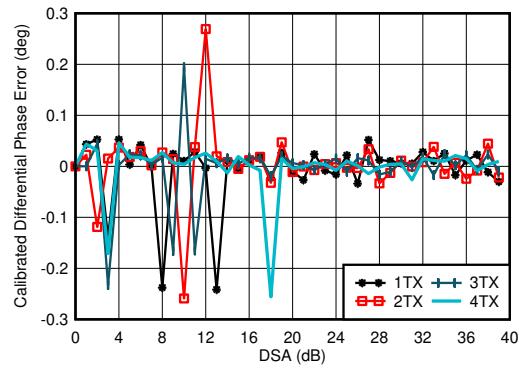
3.5 GHz Matching, included PCB and cable losses  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-123. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz**



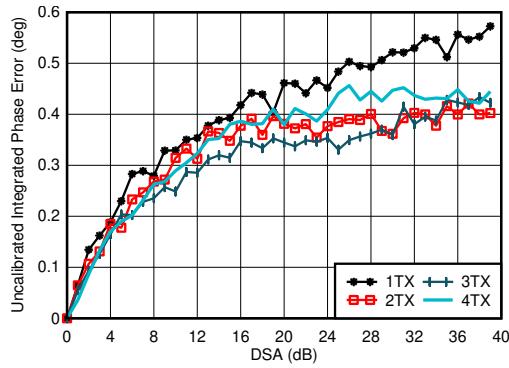
3.5 GHz Matching, included PCB and cable losses

**Figure 4-124. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz**



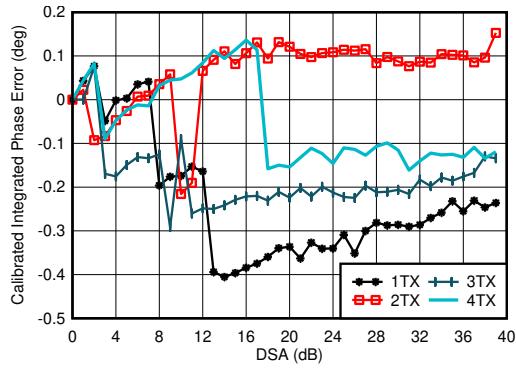
3.5 GHz Matching, included PCB and cable losses  
 Phase DNL spike may occur at any DSA setting.

**Figure 4-125. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz**



3.5 GHz Matching, included PCB and cable losses

**Figure 4-126. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz**

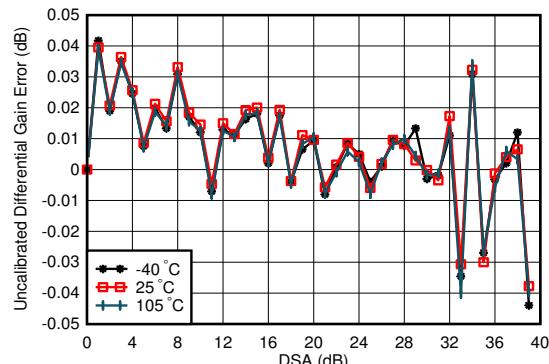


3.5 GHz Matching, included PCB and cable losses

**Figure 4-127. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz**

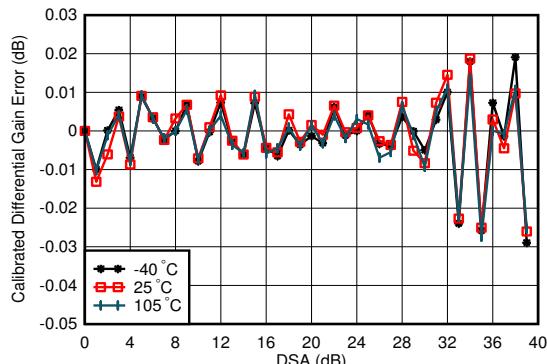
#### 4.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



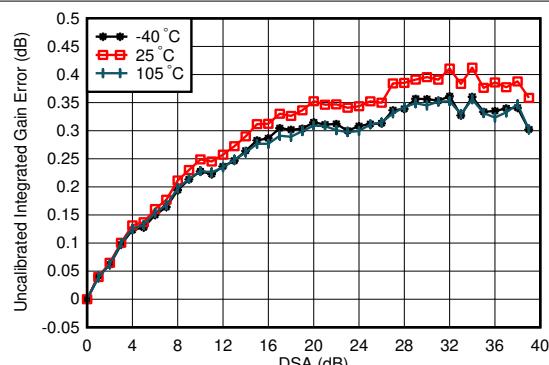
3.5 GHz Matching, 1TX

**Figure 4-128. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz**



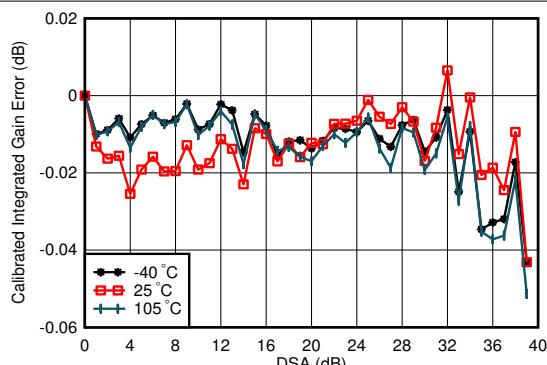
3.5 GHz Matching, 1TX, Calibrated at 25°C

**Figure 4-129. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz**



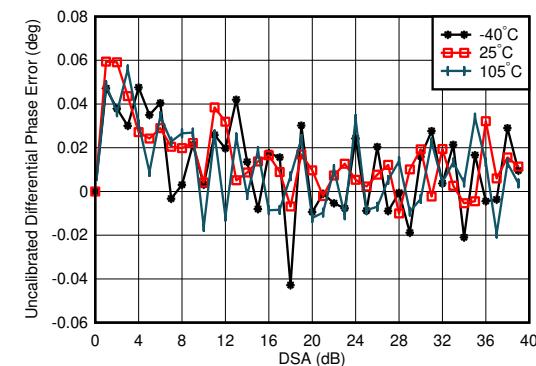
3.5 GHz Matching, 1TX

**Figure 4-130. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz**



3.5 GHz Matching, 1TX, Calibrated at 25°C

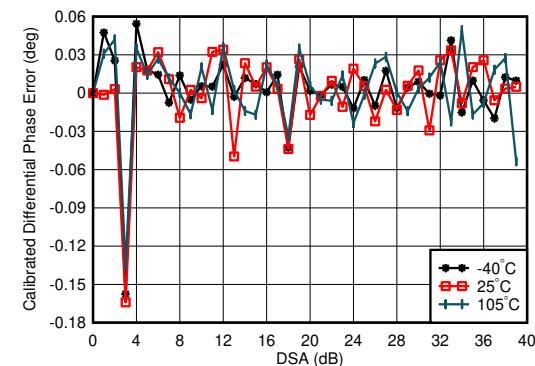
**Figure 4-131. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz**



3.5 GHz Matching, 1TX

Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-132. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz**



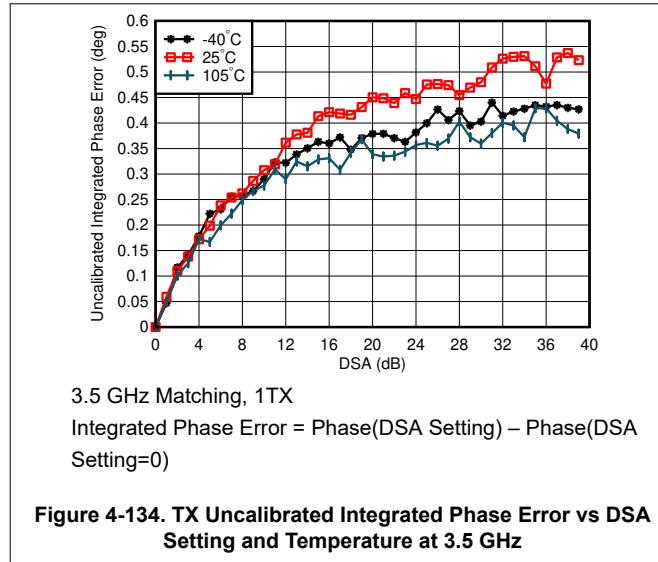
3.5 GHz Matching, 1TX, Calibrated at 25°C

Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

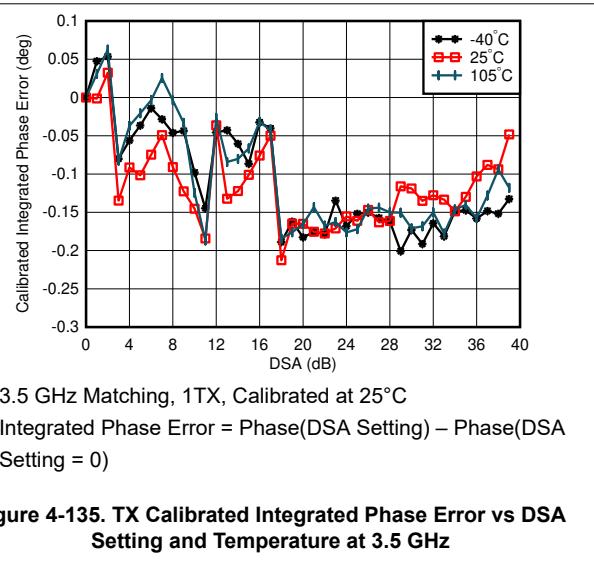
**Figure 4-133. TX Calibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz**

#### 4.12.4 TX Typical Characteristics at 3.5 GHz (continued)

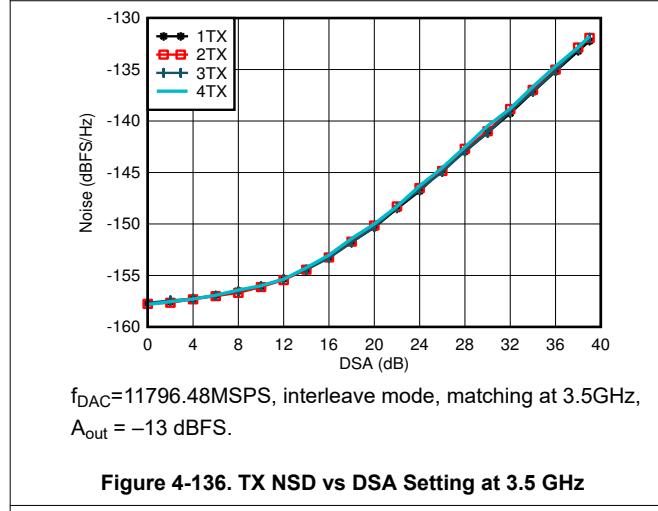
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



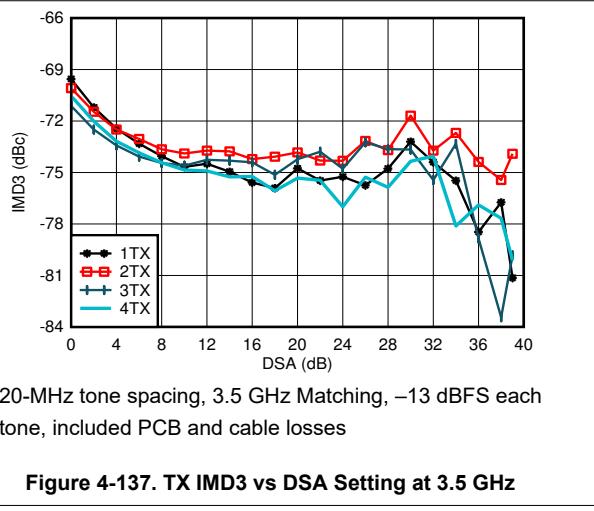
**Figure 4-134. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz**



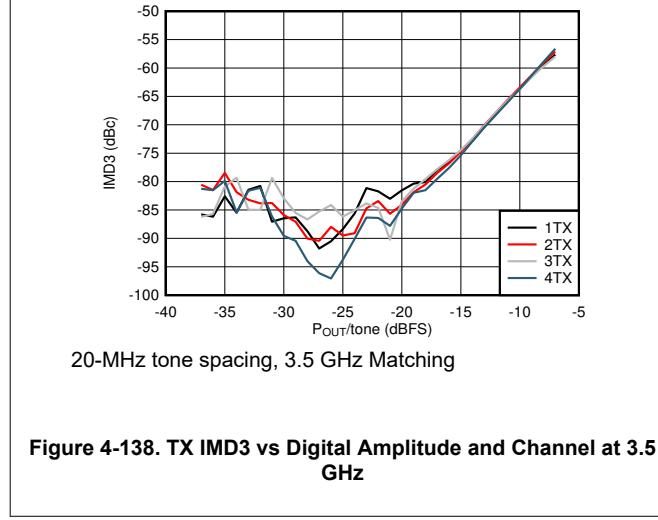
**Figure 4-135. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz**



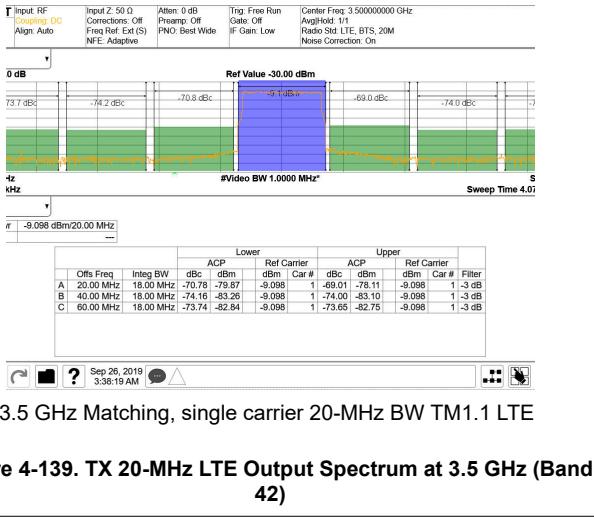
**Figure 4-136. TX NSD vs DSA Setting at 3.5 GHz**



**Figure 4-137. TX IMD3 vs DSA Setting at 3.5 GHz**



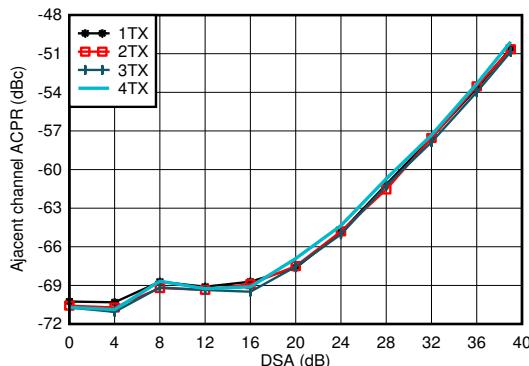
**Figure 4-138. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz**



**Figure 4-139. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)**

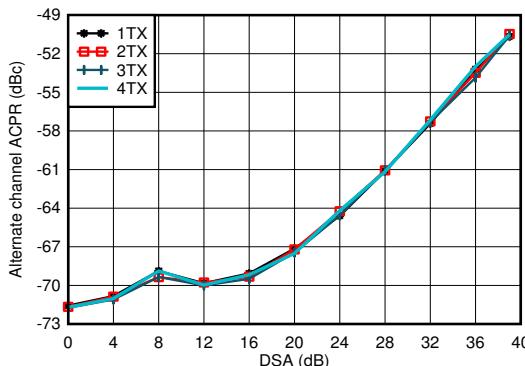
#### 4.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



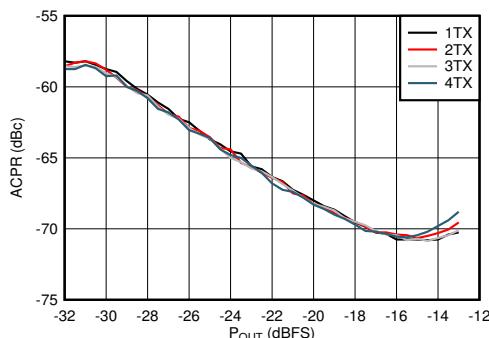
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 4-140. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz



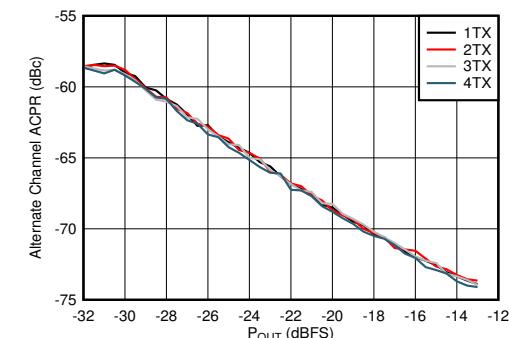
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 4-141. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz



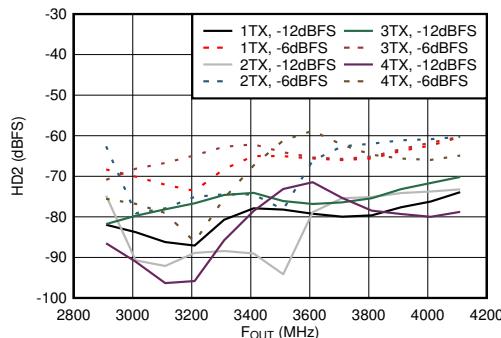
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 4-142. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz



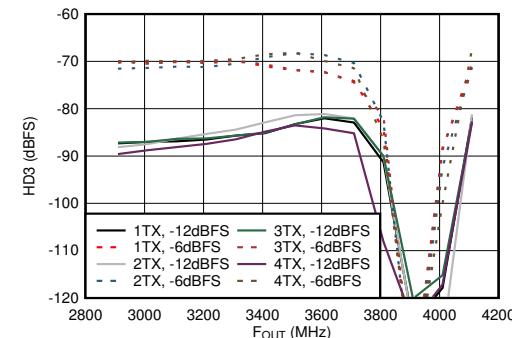
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 4-143. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz



Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

Figure 4-144. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz

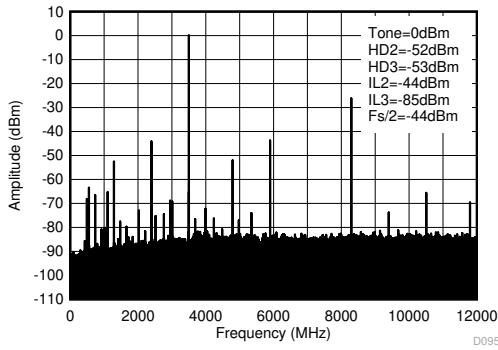


Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

Figure 4-145. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz

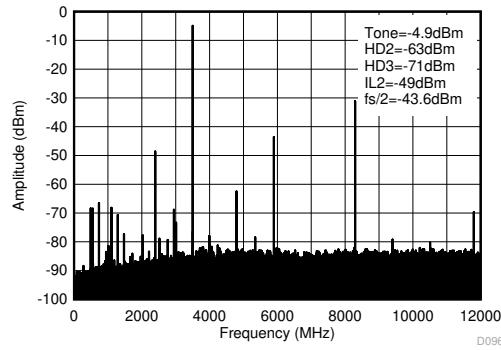
#### 4.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



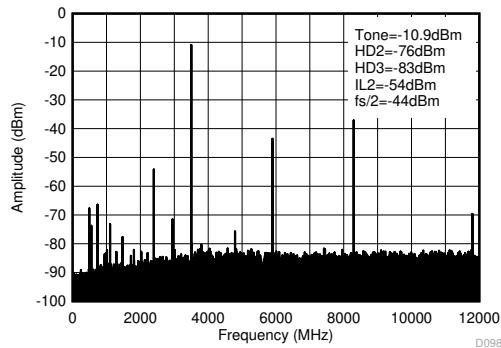
Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 4-146. TX Single Tone ( $-1 \text{ dBFS}$ ) Output Spectrum at 3.5 GHz ( $0 - f_{\text{DAC}}$ )**



Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 4-147. TX Single Tone ( $-6 \text{ dBFS}$ ) Output Spectrum at 3.5 GHz ( $0 - f_{\text{DAC}}$ )**

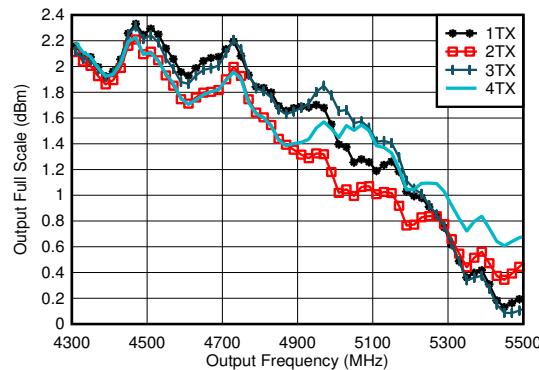


Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 4-148. TX Single Tone ( $-12 \text{ dBFS}$ ) Output Spectrum at 3.5 GHz ( $0 - f_{\text{DAC}}$ )**

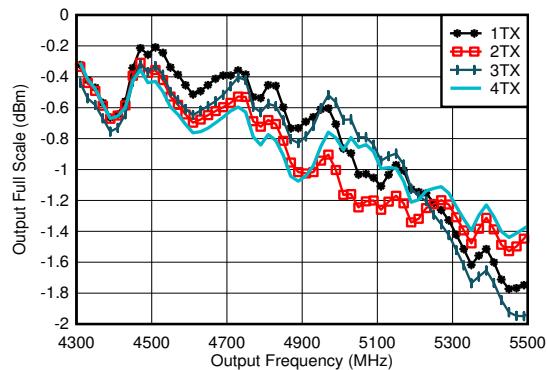
#### 4.12.5 TX Typical Characteristics at 4.9 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



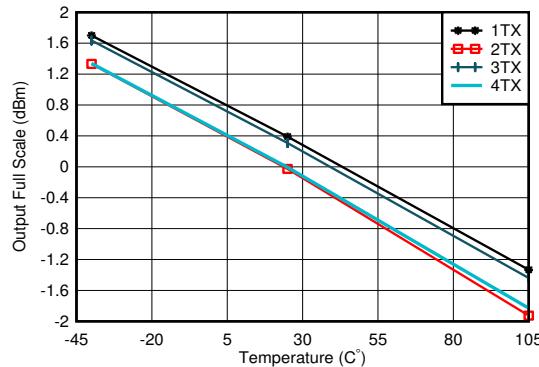
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5\text{dFBS}$ , DSA = 0, 4.9 GHz matching

**Figure 4-149. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS**



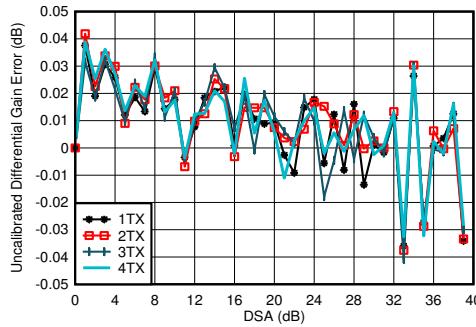
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5\text{dFBS}$ , DSA = 0, 4.9 GHz matching

**Figure 4-150. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode, 2nd Nyquist Zone**



$f_{\text{DAC}} = 11796.48 \text{ MSPS}$ ,  $A_{\text{out}} = -0.5\text{dFBS}$ , matching 4.9 GHz

**Figure 4-151. TX Output Power vs DSA Setting and Channel at 4.9 GHz**

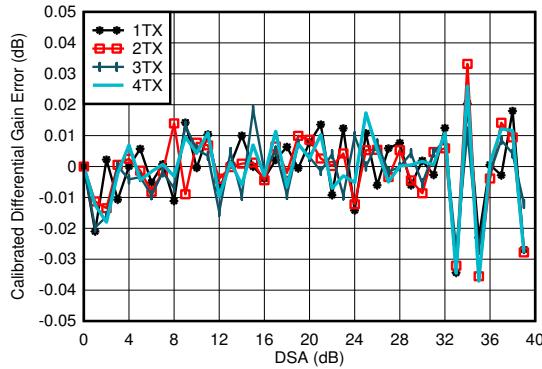


$f_{\text{DAC}} = 11796.48 \text{ MSPS}$ , interleave mode, matching at 4.9 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-152. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz**

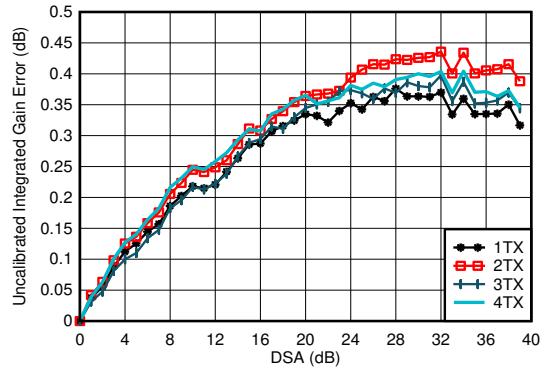
#### 4.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



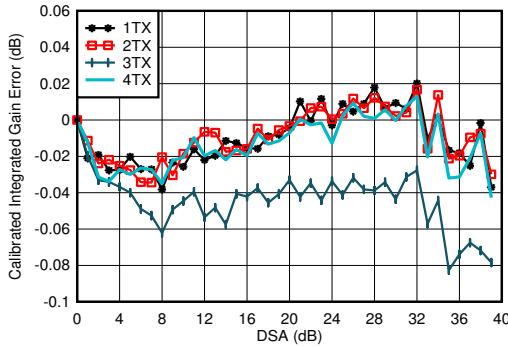
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-153. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz**



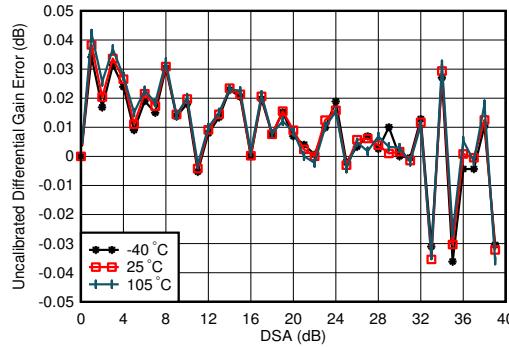
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-154. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-155. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-156. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz**

#### 4.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

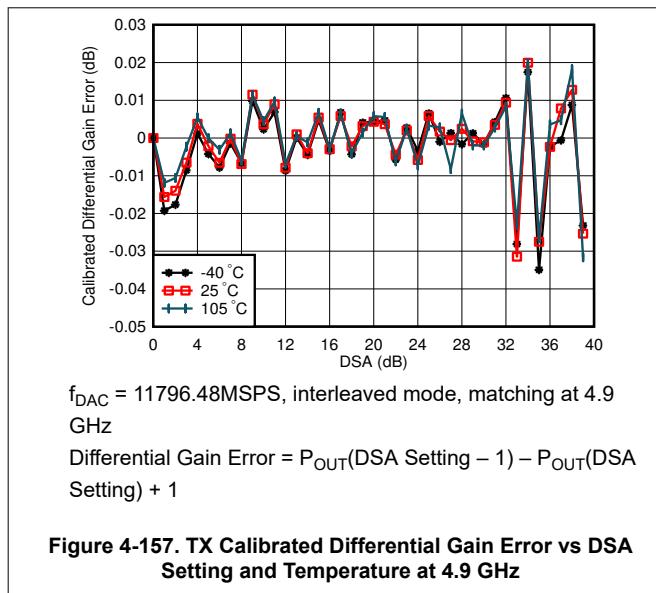


Figure 4-157. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz

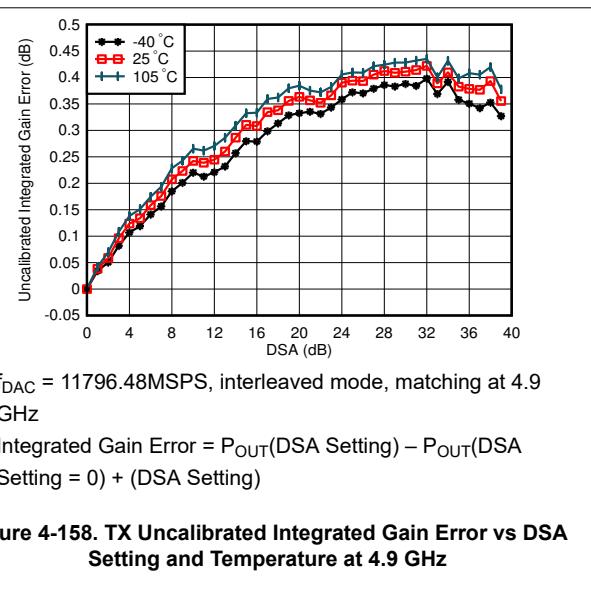


Figure 4-158. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz

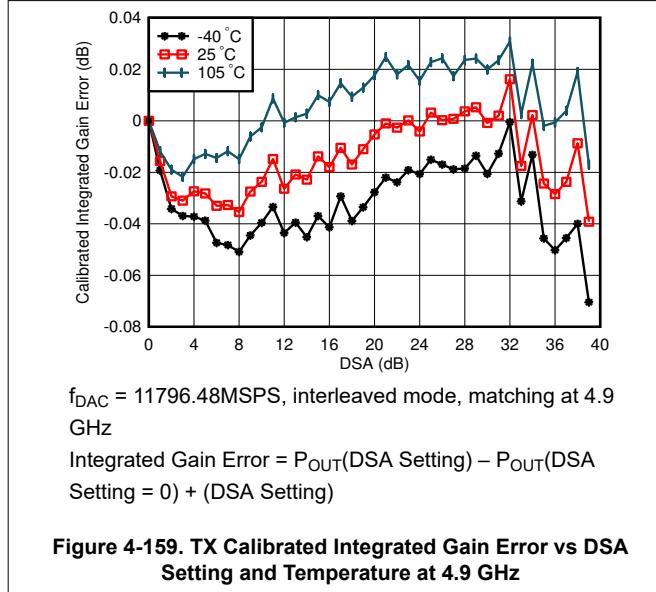


Figure 4-159. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz

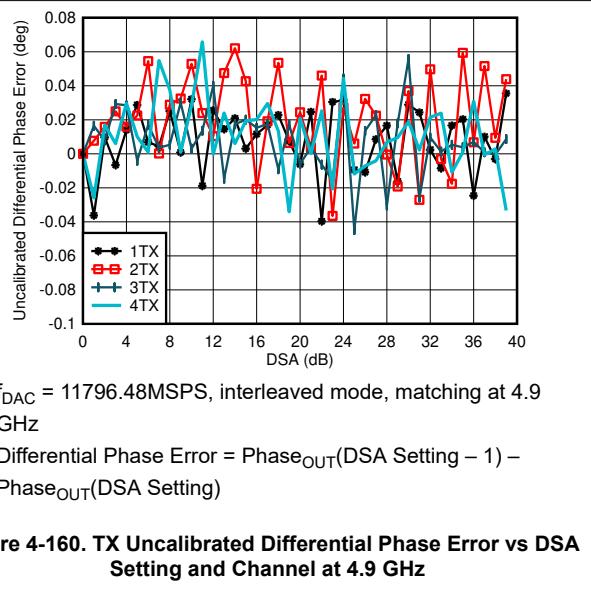
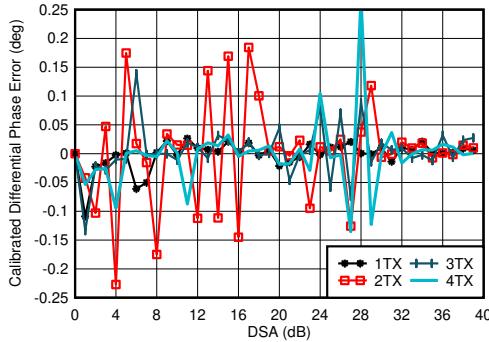


Figure 4-160. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

#### 4.12.5 TX Typical Characteristics at 4.9 GHz (continued)

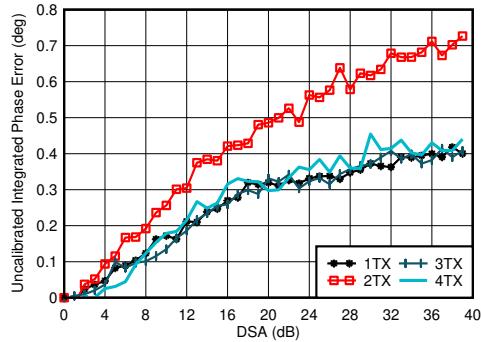
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz

Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
 Phase DNL spike may occur at any DSA setting.

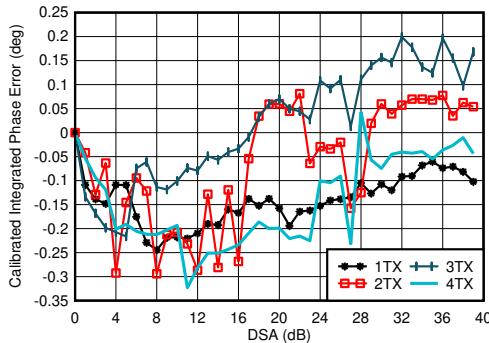
Figure 4-161. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz

Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

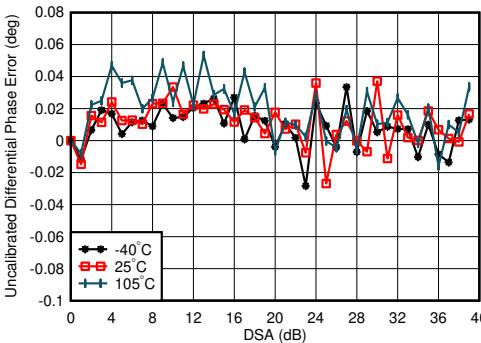
Figure 4-162. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz

Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 4-163. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



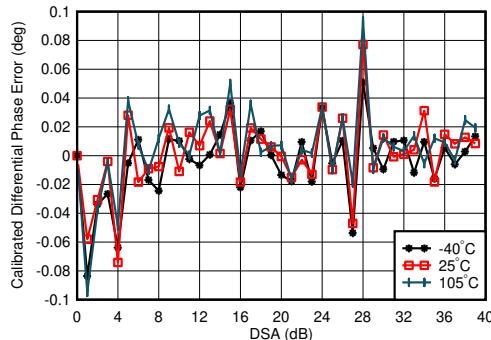
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz

Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 4-164. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz

#### 4.12.5 TX Typical Characteristics at 4.9 GHz (continued)

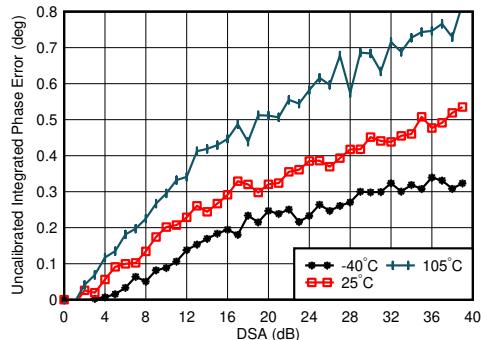
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz

Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

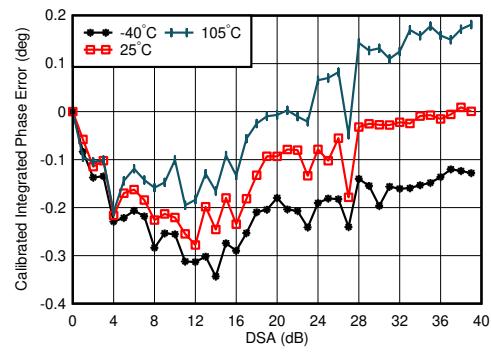
**Figure 4-165. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz

Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

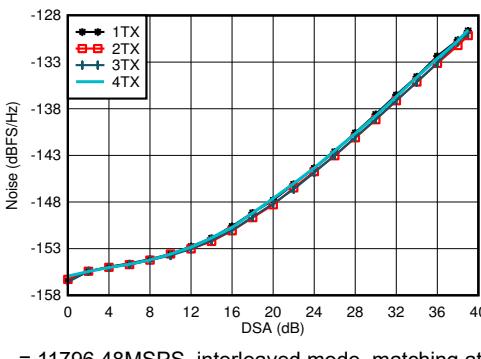
**Figure 4-166. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz, channel with the median variation over DSA setting at 25°C

Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-167. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz**

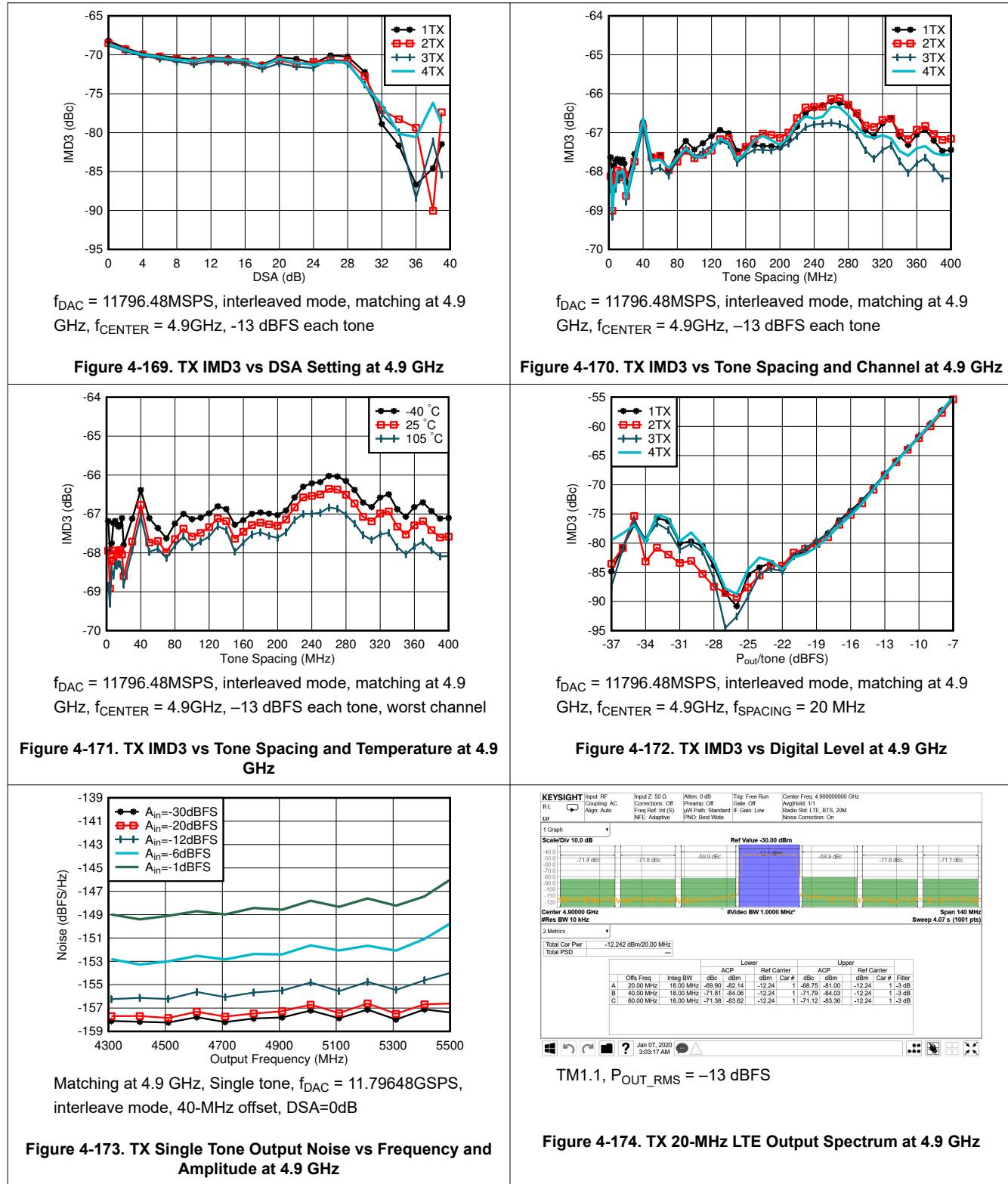


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $P_{\text{OUT}} = -13 \text{ dBFS}$

**Figure 4-168. TX Output Noise vs Channel and Attenuation at 2.6 GHz**

#### 4.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



#### 4.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

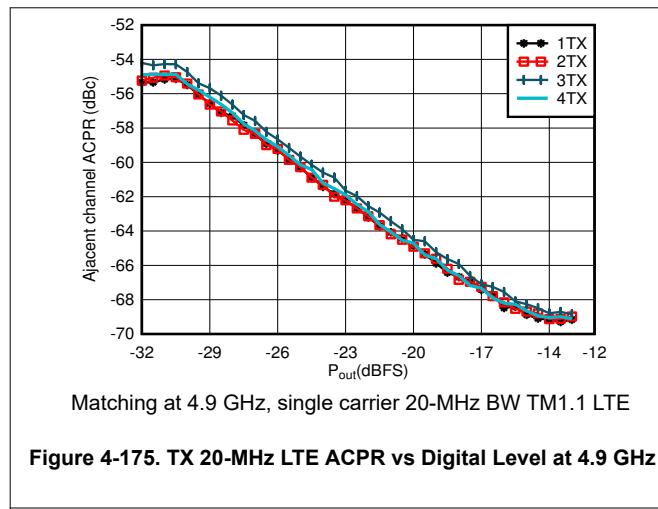


Figure 4-175. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz

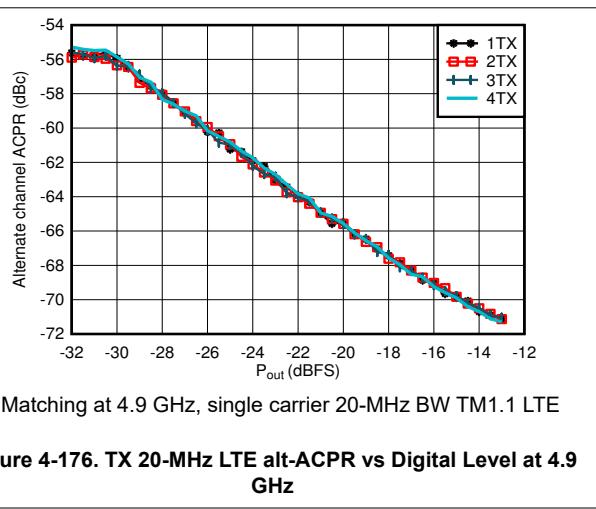


Figure 4-176. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz

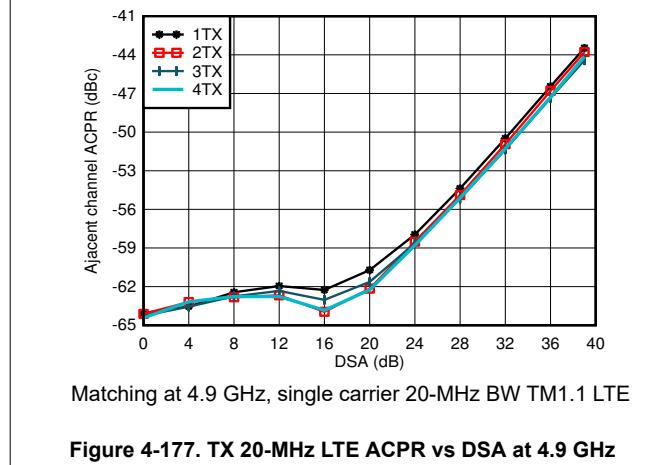


Figure 4-177. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz

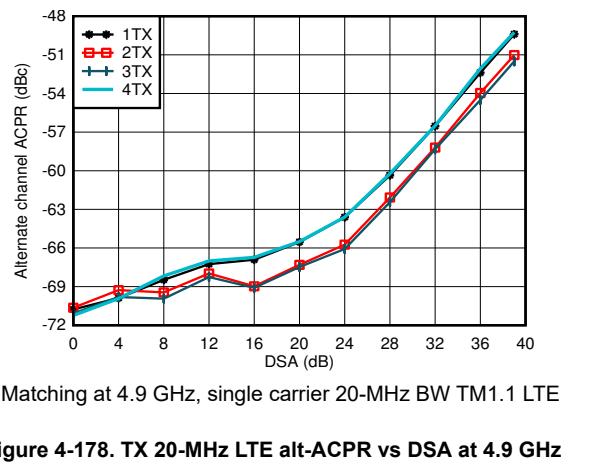


Figure 4-178. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz

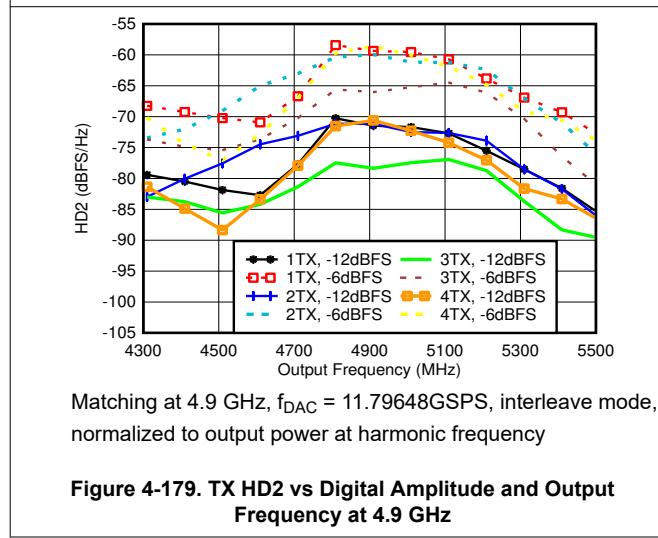


Figure 4-179. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz

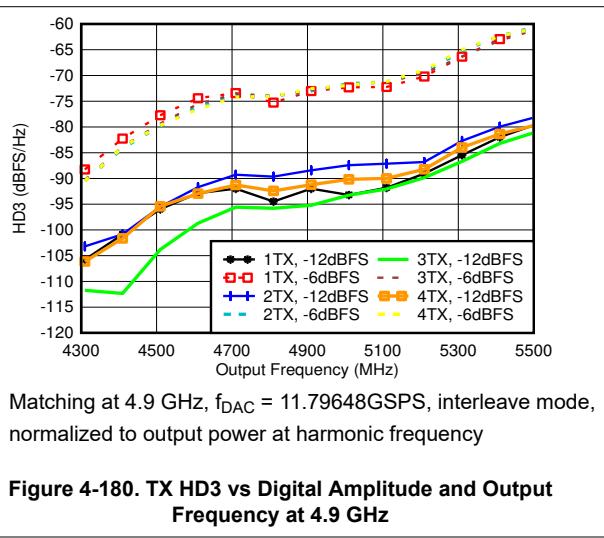
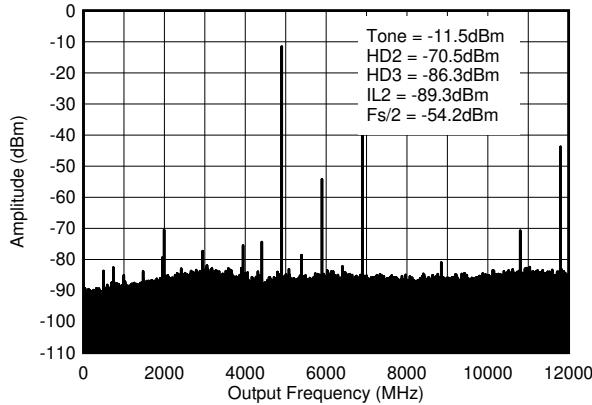


Figure 4-180. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz

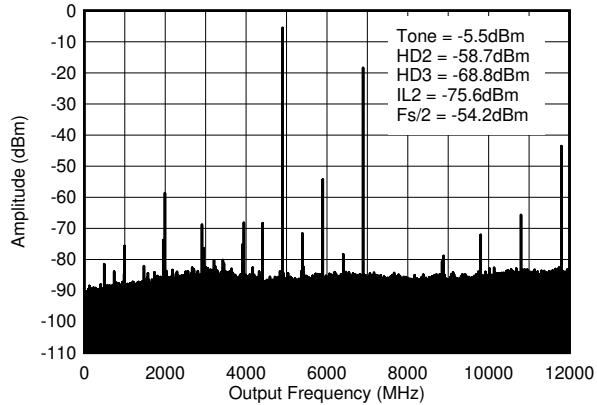
#### 4.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



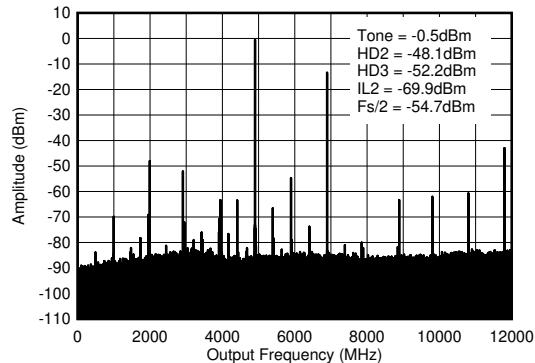
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_S/n \pm f_{\text{OUT}}$ .

**Figure 4-181. TX Single Tone (-12 dBFS) Output Spectrum at 4.9 GHz (0- $f_{\text{DAC}}$ )**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_S/n \pm f_{\text{OUT}}$ .

**Figure 4-182. TX Single Tone (-6 dBFS) Output Spectrum at 4.9 GHz (0- $f_{\text{DAC}}$ )**

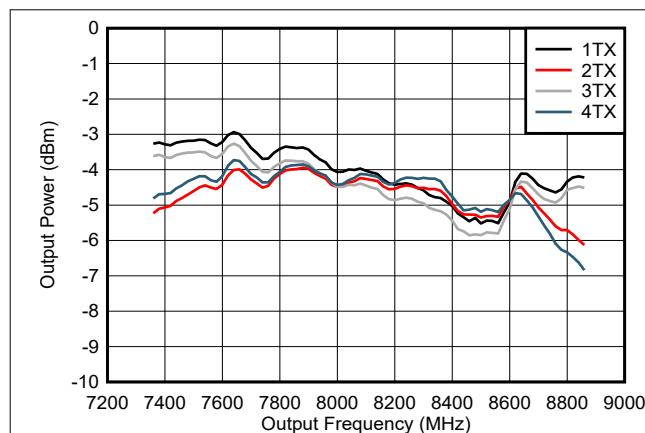


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_S/n \pm f_{\text{OUT}}$ .

**Figure 4-183. TX Single Tone (-1 dBFS) Output Spectrum at 4.9 GHz (0- $f_{\text{DAC}}$ )**

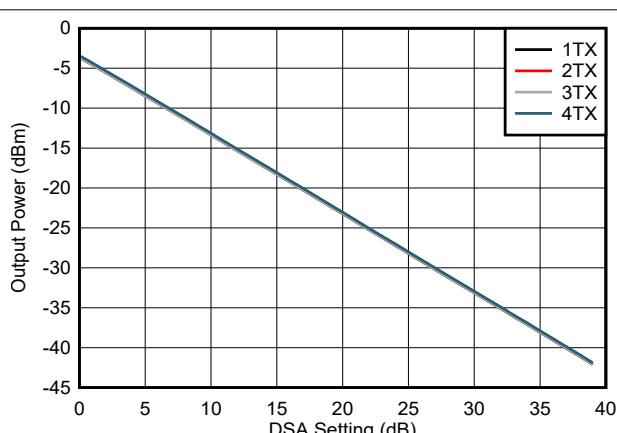
#### 4.12.6 TX Typical Characteristics at 8.1 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching



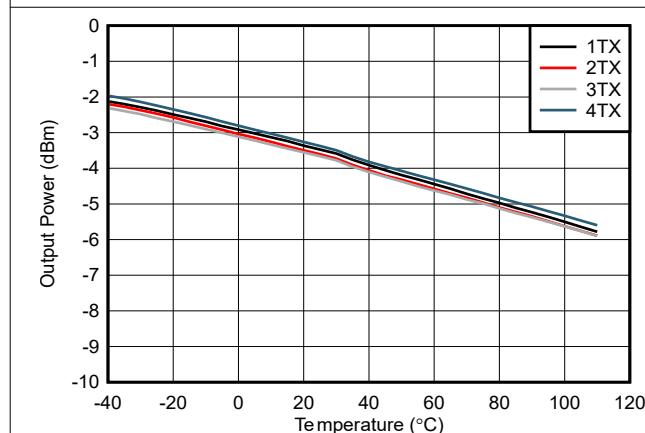
includes PCB and cable losses.

**Figure 4-184. TX Output Power vs Frequency at 8.11 GHz**



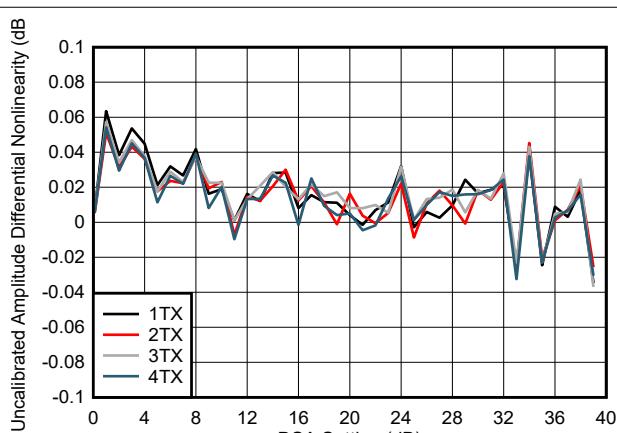
includes PCB and cable losses.

**Figure 4-185. TX Output Power vs DSA Setting at 8.11 GHz**



includes PCB and cable losses.

**Figure 4-186. TX Output Power vs Temperature at 8.11 GHz**



**Figure 4-187. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11 GHz**

#### 4.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

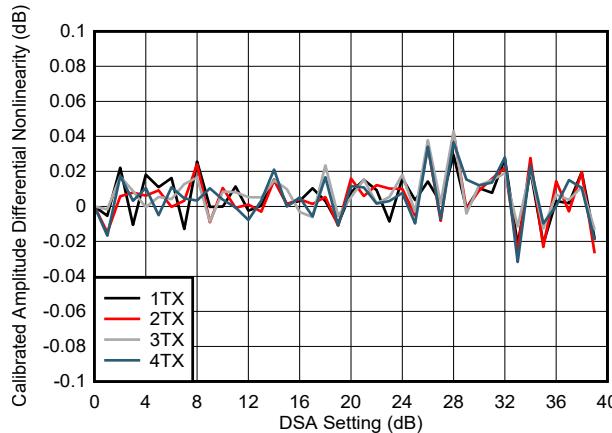


Figure 4-188. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11 GHz

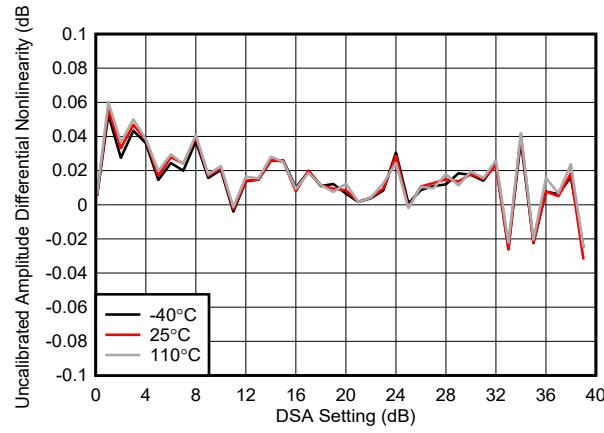


Figure 4-189. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11 GHz

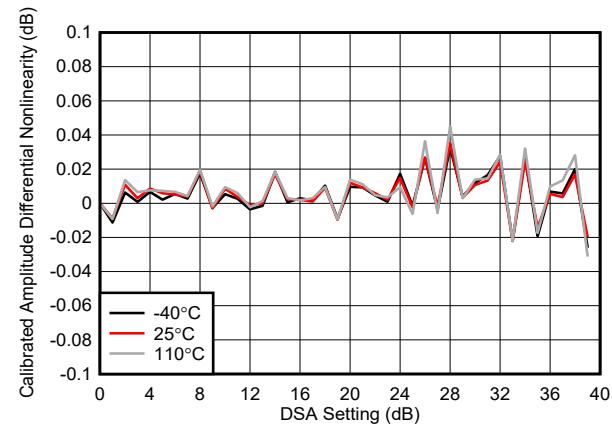


Figure 4-190. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11 GHz

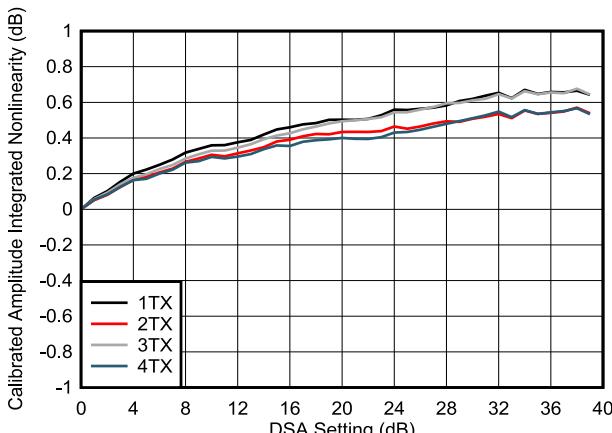


Figure 4-191. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz

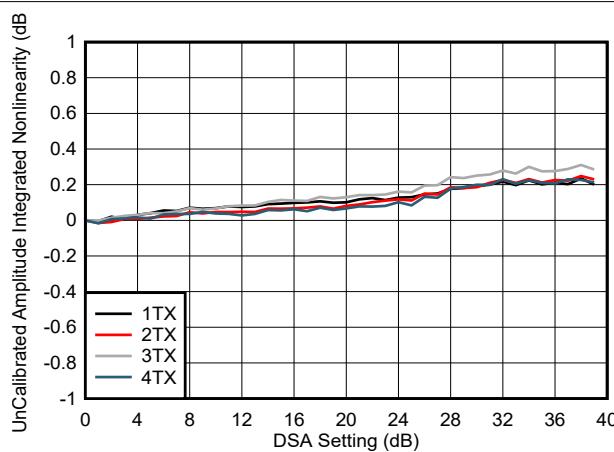


Figure 4-192. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz

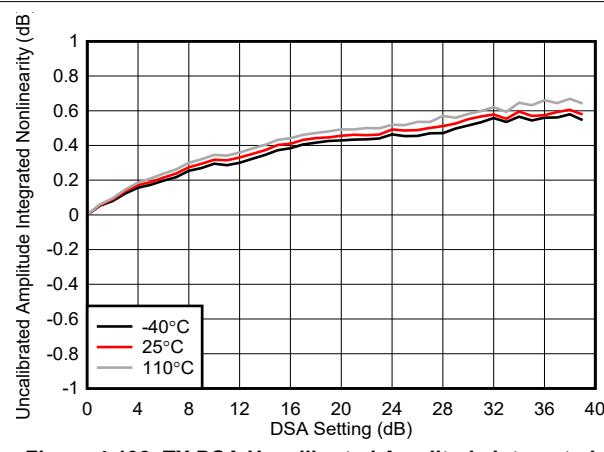


Figure 4-193. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz

#### 4.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

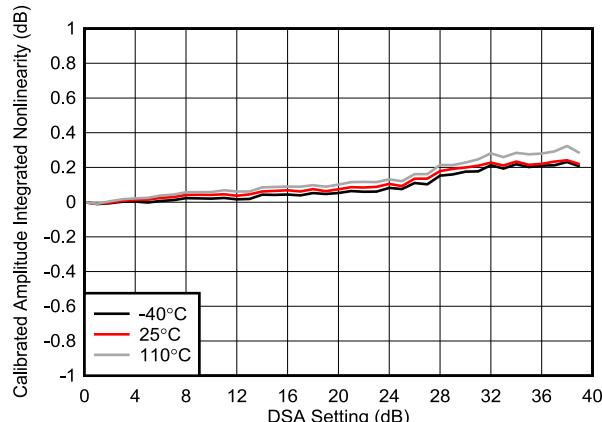


Figure 4-194. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz

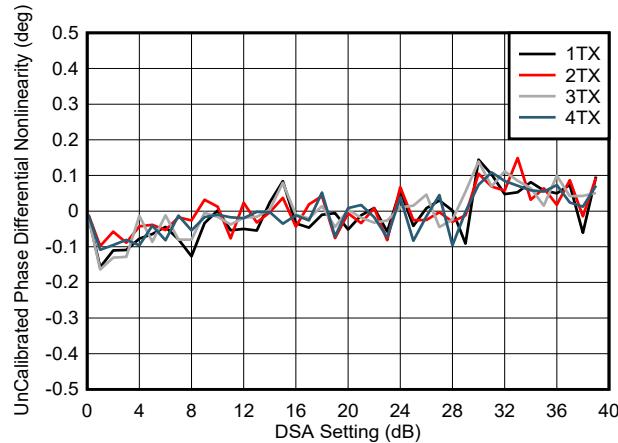


Figure 4-195. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11 GHz

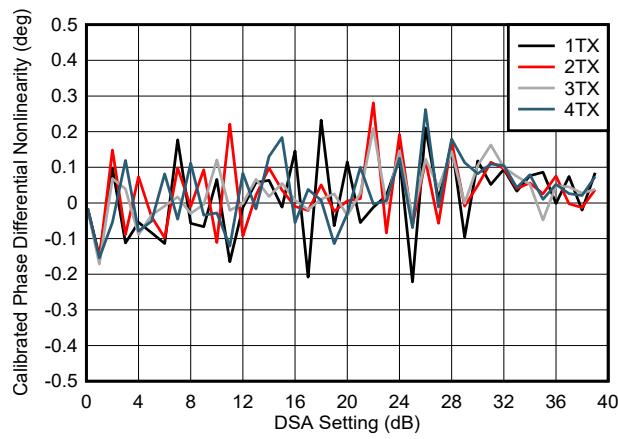


Figure 4-196. TX DSA Calibrated Phase Differential Nonlinearity at 8.11 GHz

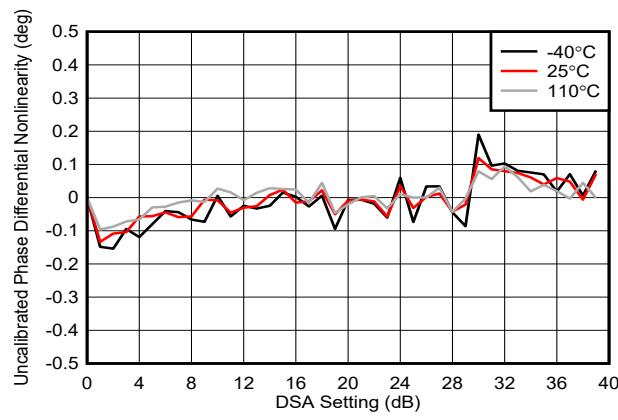


Figure 4-197. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11 GHz

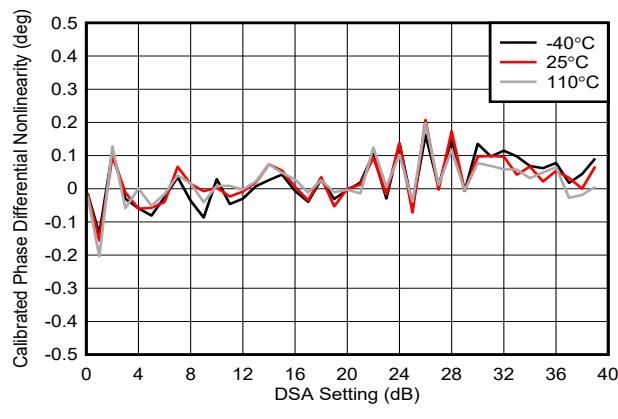


Figure 4-198. TX DSA Calibrated Phase Differential Nonlinearity at 8.11 GHz

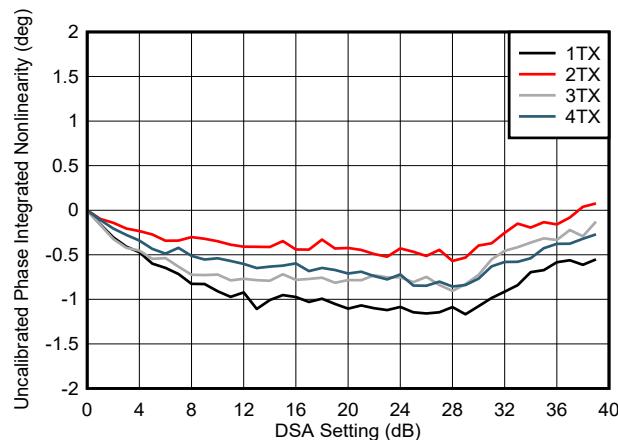


Figure 4-199. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11 GHz

#### 4.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

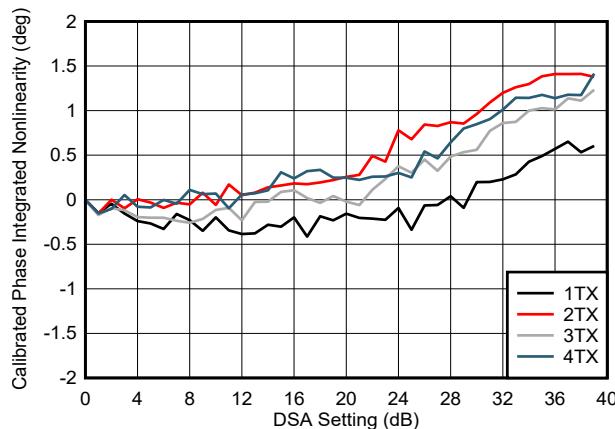


Figure 4-200. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11 GHz

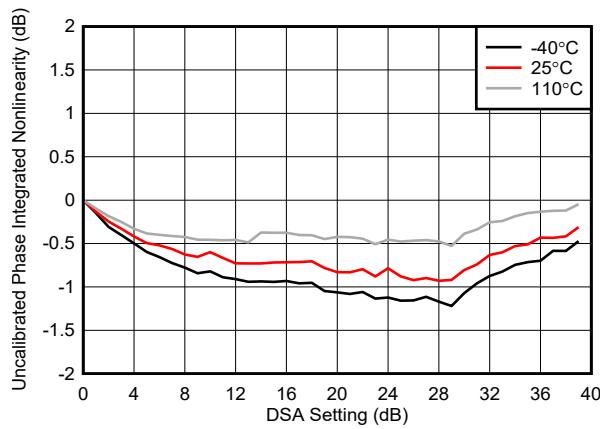


Figure 4-201. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11 GHz

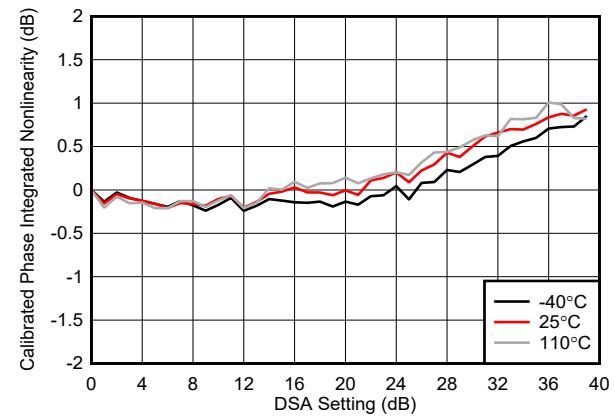


Figure 4-202. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11 GHz

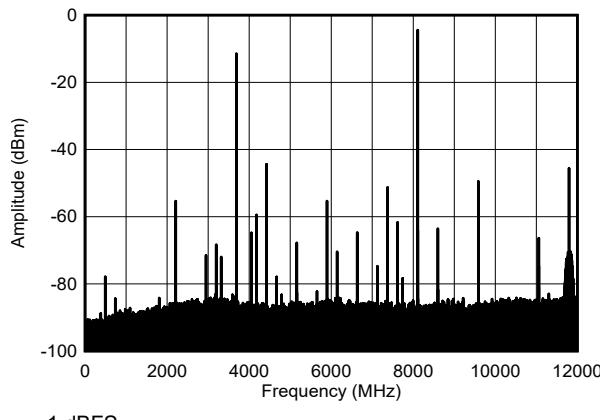


Figure 4-203. TX Single Tone Output Spectrum at 8.11 GHz

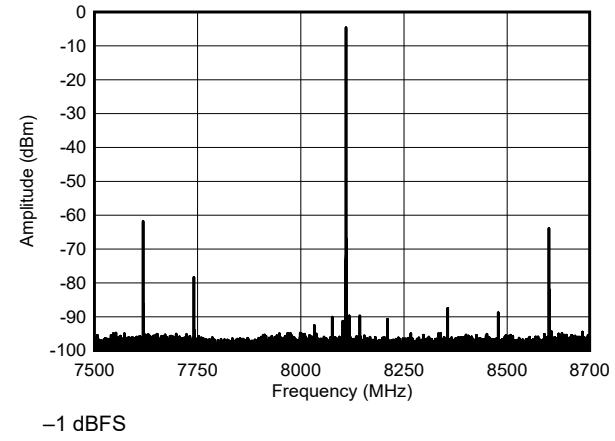


Figure 4-204. TX Single Tone Output Spectrum at 8.11 GHz

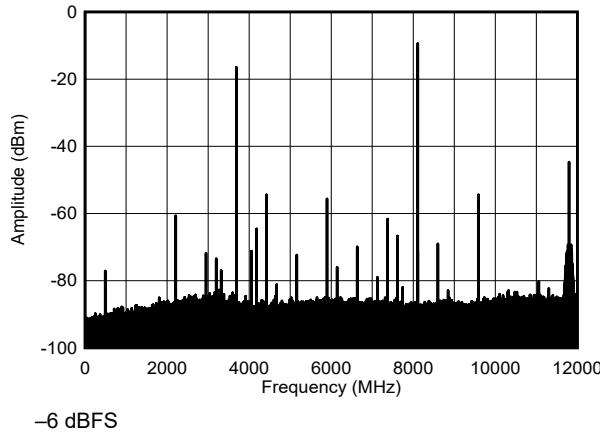


Figure 4-205. TX Single Tone Output Spectrum at 8.11 GHz

#### 4.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

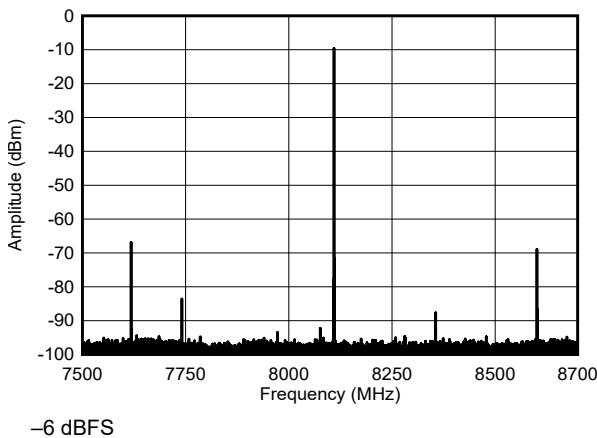


Figure 4-206. TX Single Tone Output Spectrum at 8.11 GHz

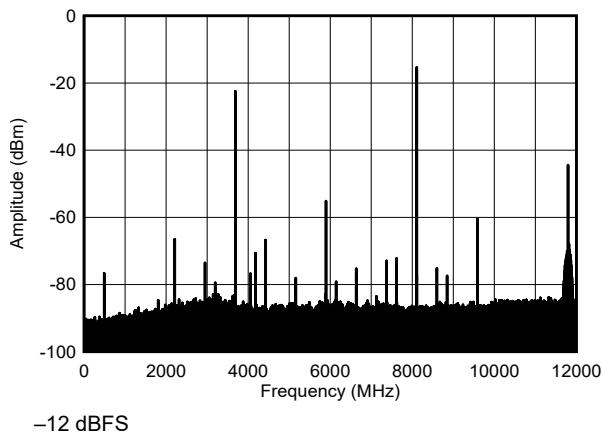


Figure 4-207. TX Single Tone Output Spectrum at 8.11 GHz

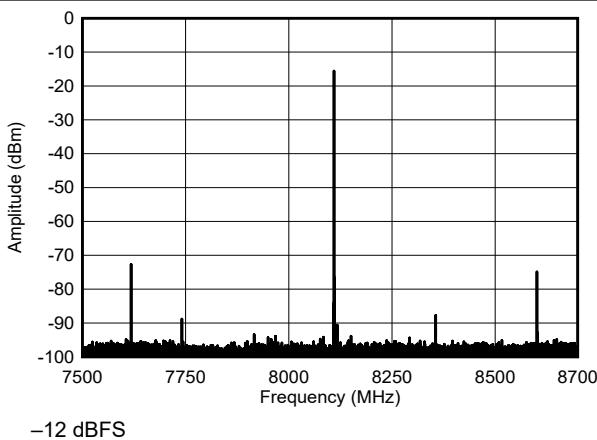


Figure 4-208. TX Single Tone Output Spectrum at 8.11 GHz

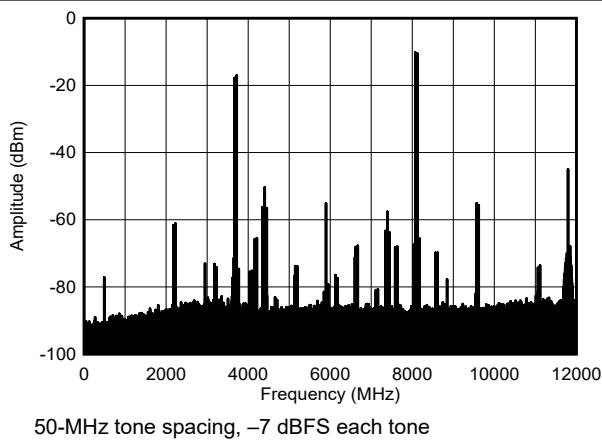
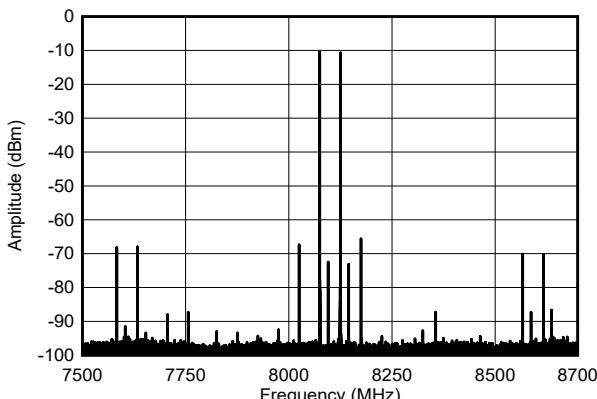
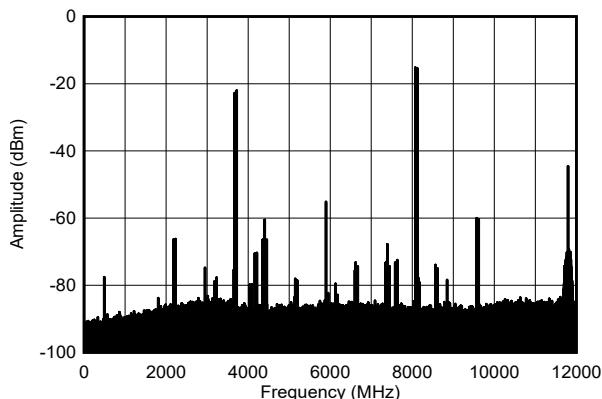


Figure 4-209. TX Dual Tone Output Spectrum at 8.11 GHz



50-MHz tone spacing, -7 dBFS each tone

Figure 4-210. TX Dual Tone Output Spectrum at 8.11 GHz



50-MHz tone spacing, -12 dBFS each tone

Figure 4-211. TX Dual Tone Output Spectrum at 8.11 GHz

#### 4.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

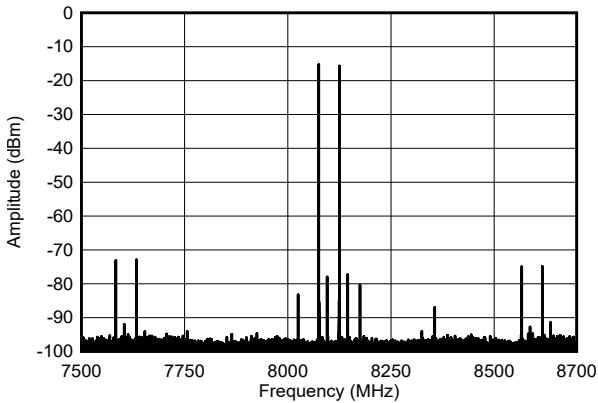


Figure 4-212. TX Dual Tone Output Spectrum at 8.11 GHz

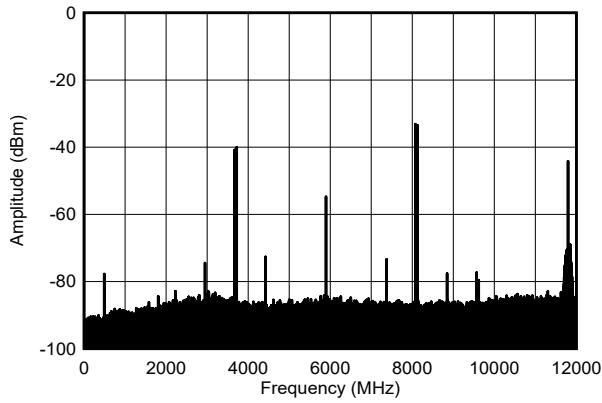


Figure 4-213. TX Dual Tone Output Spectrum at 8.11 GHz

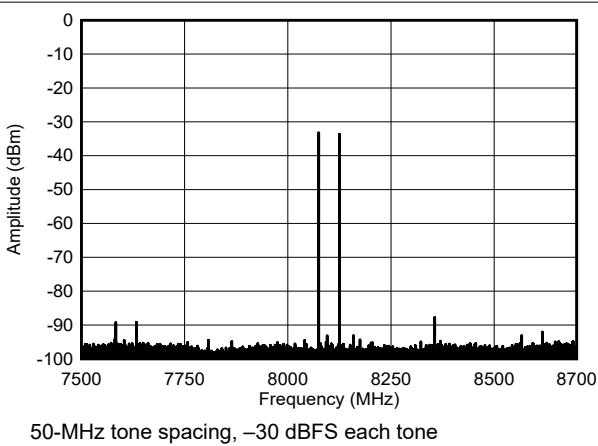


Figure 4-214. TX Dual Tone Output Spectrum at 8.11 GHz

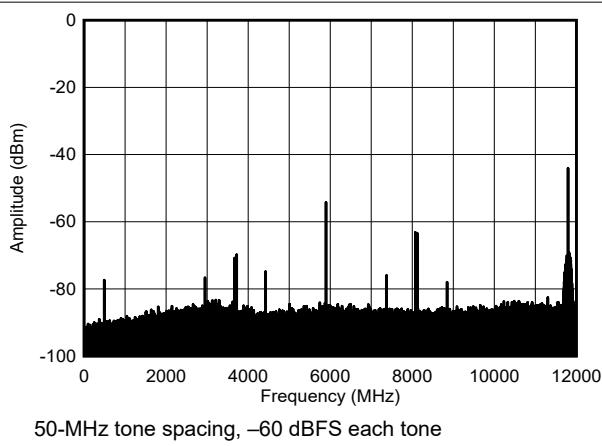


Figure 4-215. TX Dual Tone Output Spectrum at 8.11 GHz

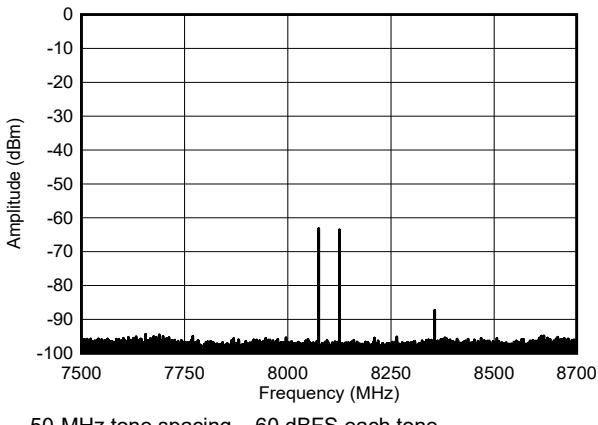


Figure 4-216. TX Dual Tone Output Spectrum at 8.11 GHz

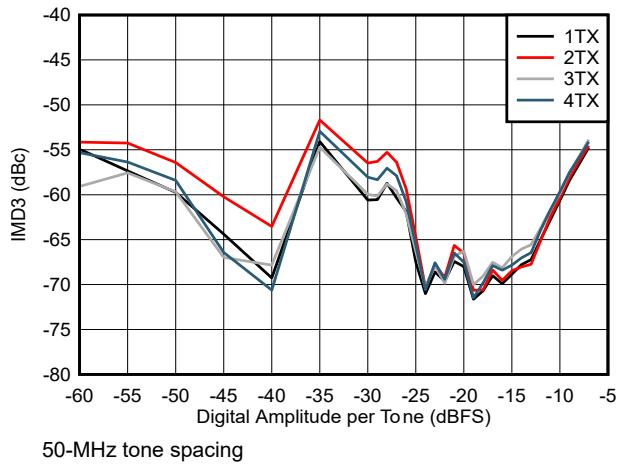
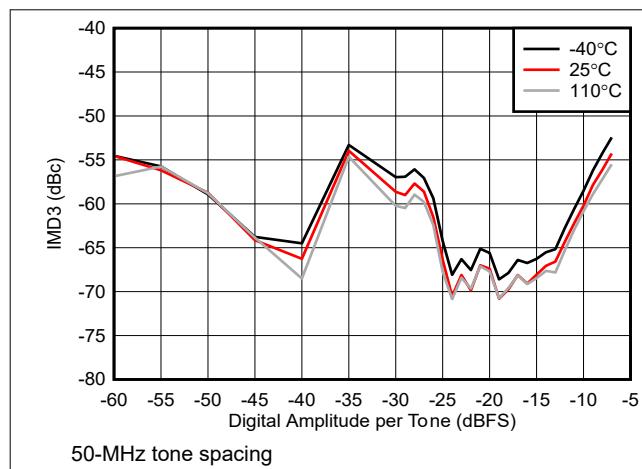


Figure 4-217. TX IMD3 vs Digital Amplitude at 8.11 GHz

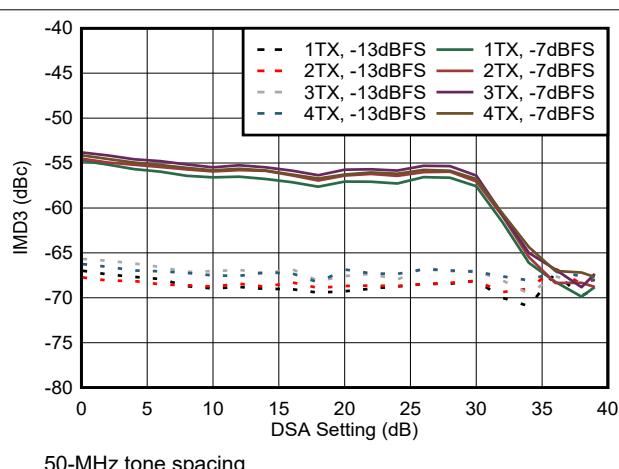
#### 4.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching



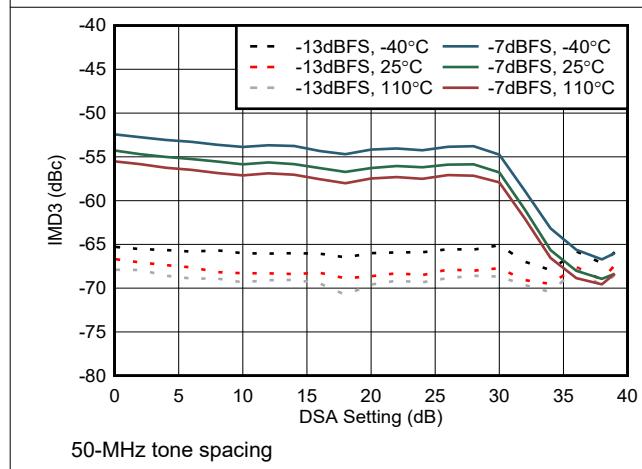
50-MHz tone spacing

Figure 4-218. TX IMD3 vs Digital Amplitude at 8.11 GHz



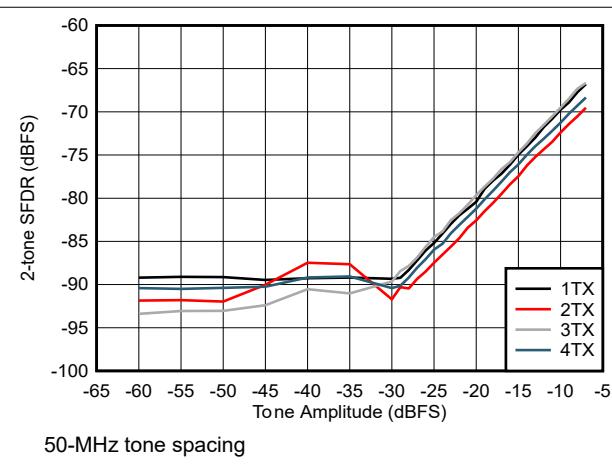
50-MHz tone spacing

Figure 4-219. TX IMD3 vs DSA Setting at 8.11 GHz



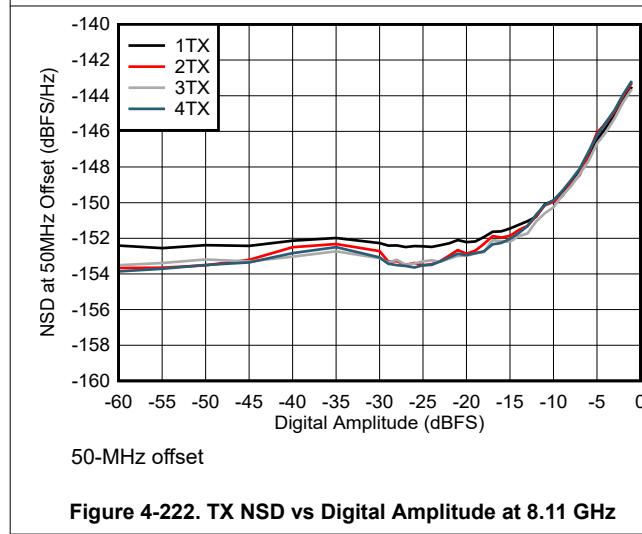
50-MHz tone spacing

Figure 4-220. TX IMD3 vs DSA Setting at 8.11 GHz



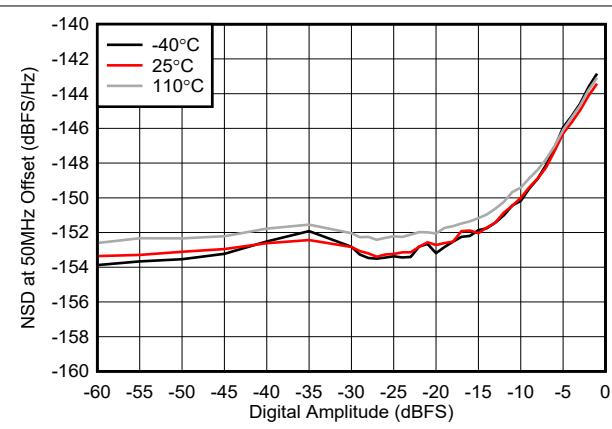
50-MHz tone spacing

Figure 4-221. TX 2-Tone SFDR vs Digital Amplitude at 8.11 GHz



50-MHz offset

Figure 4-222. TX NSD vs Digital Amplitude at 8.11 GHz



50-MHz offset

Figure 4-223. TX NSD vs Digital Amplitude at 8.11 GHz

#### 4.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

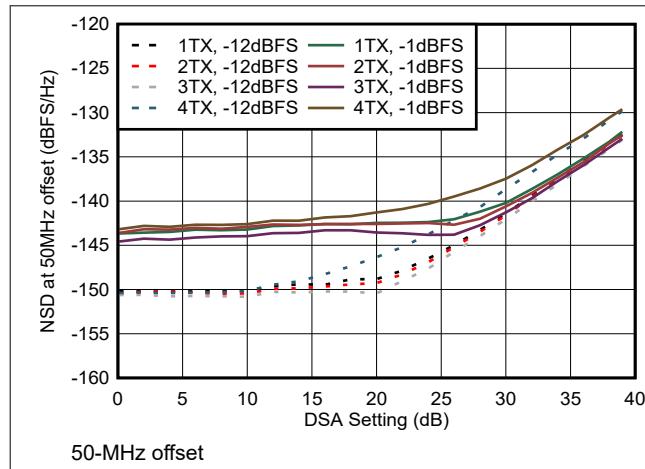


Figure 4-224. TX NSD vs DSA Setting at 8.11 GHz

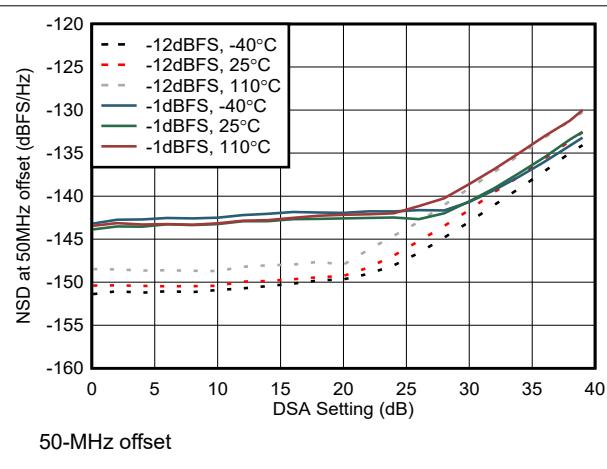


Figure 4-225. TX NSD vs DSA Setting at 8.11 GHz

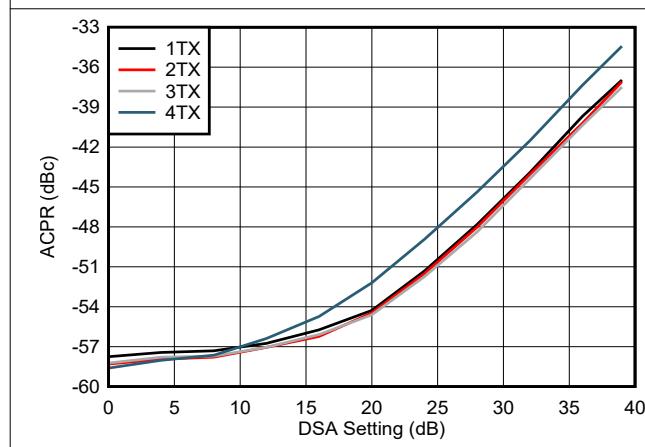


Figure 4-226. TX NR100MHz ACPR vs DSA Setting 8.11 GHz

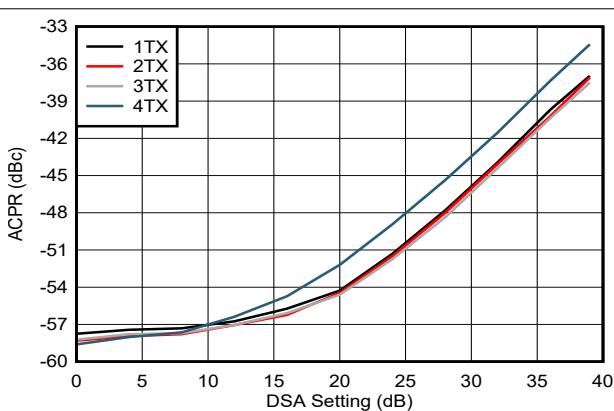


Figure 4-227. TX NR100MHz alt-ACPR vs DSA Setting 8.11 GHz

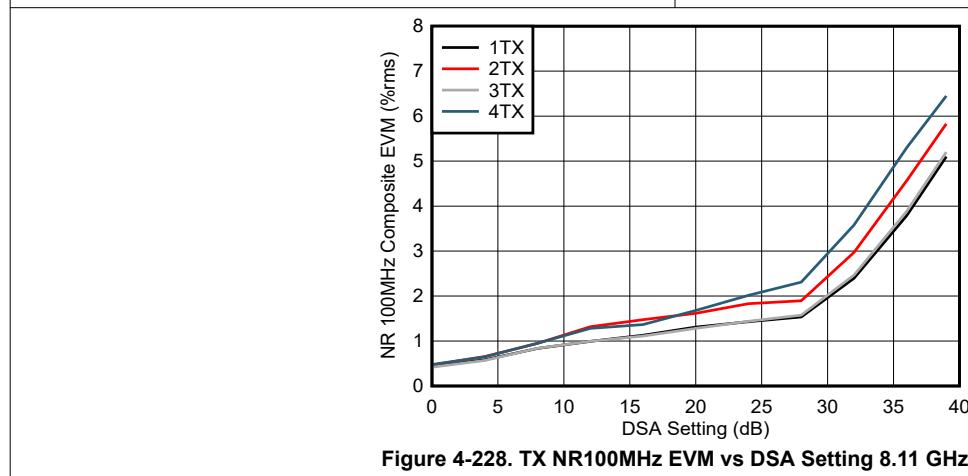


Figure 4-228. TX NR100MHz EVM vs DSA Setting 8.11 GHz

#### 4.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, 8.1 GHz matching

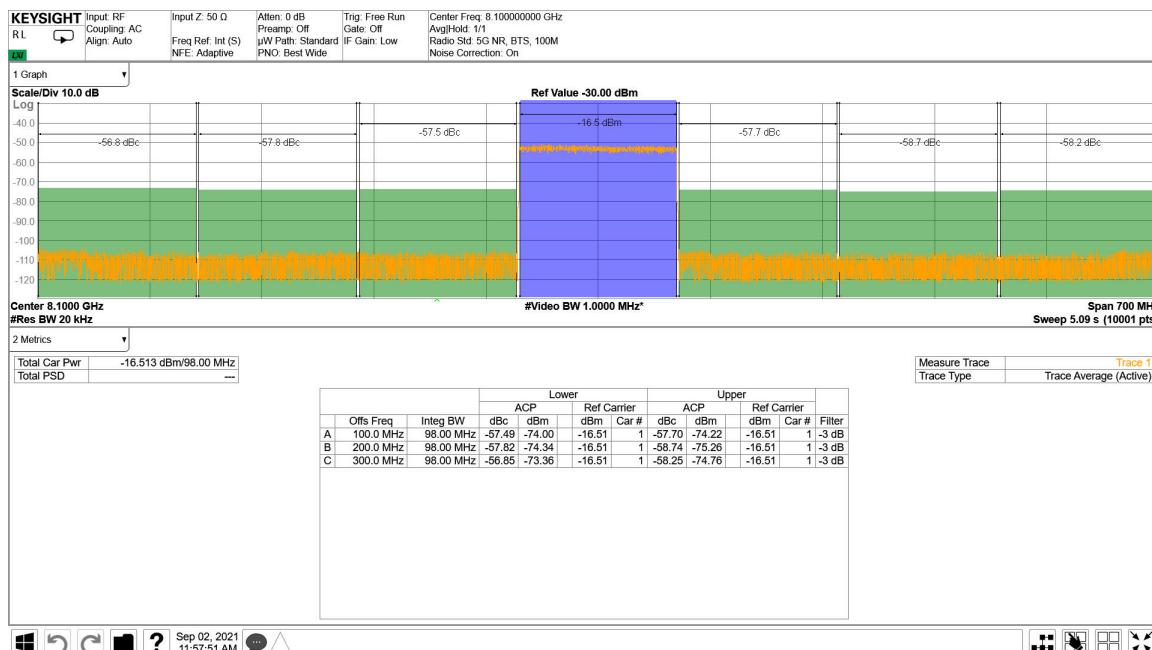


Figure 4-229. TX 100MHz NR Output Spectrum at 8.11 GHz

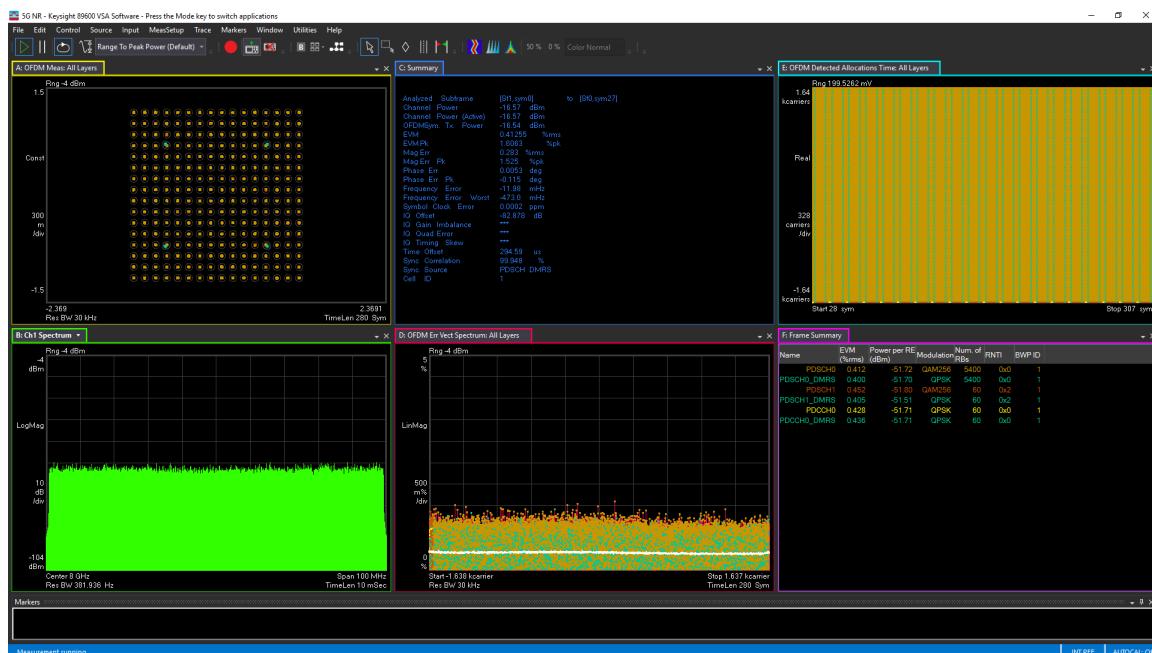


Figure 4-230. TX 100MHz NR EVM at 8.11 GHz

#### 4.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{OUT}} = -1 \text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

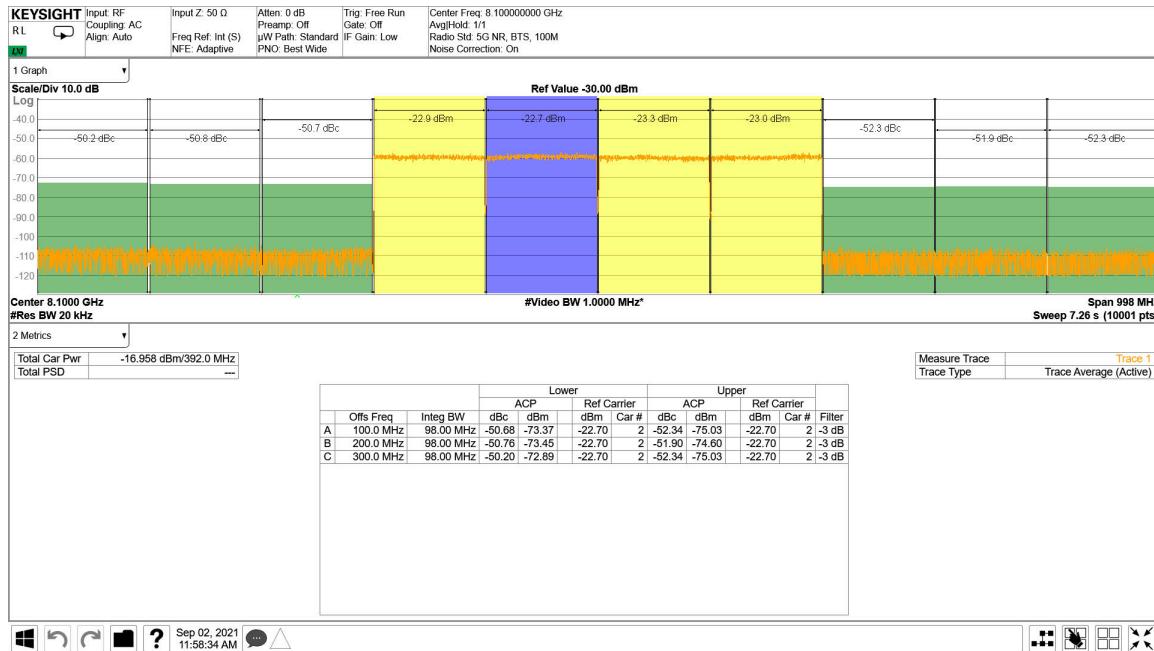


Figure 4-231. TX 4x100MHz NR Output Spectrum 8.11 GHz

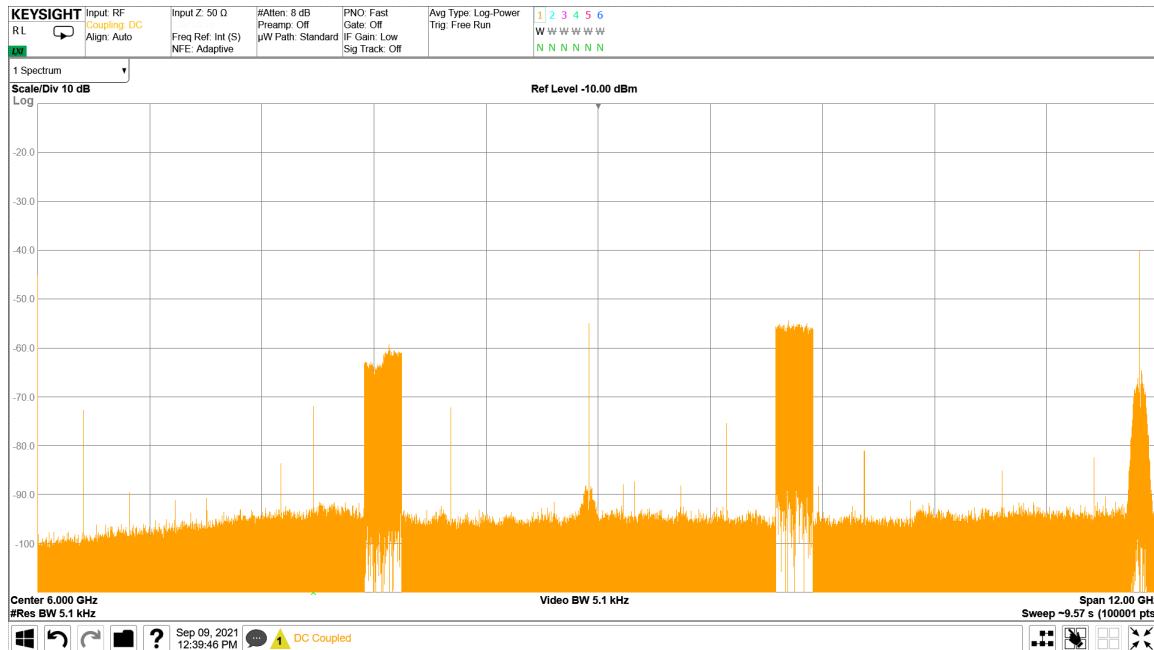
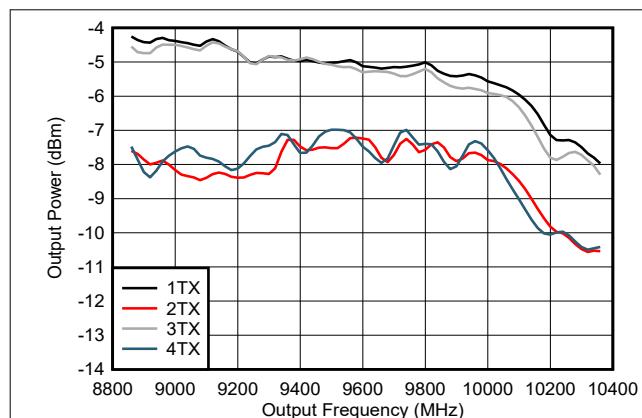


Figure 4-232. TX 4x100MHz NR Output Spectrum 8.11 GHz

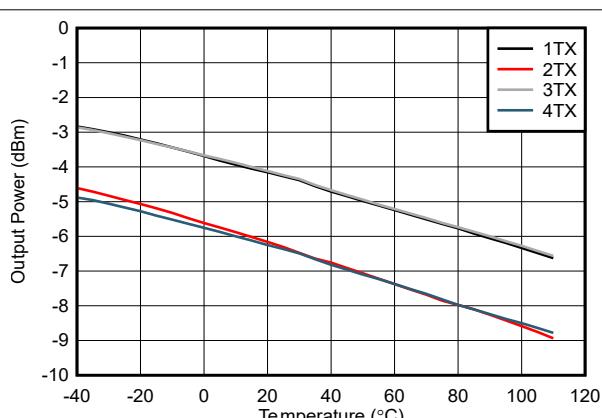
#### 4.12.7 TX Typical Characteristics at 9.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching



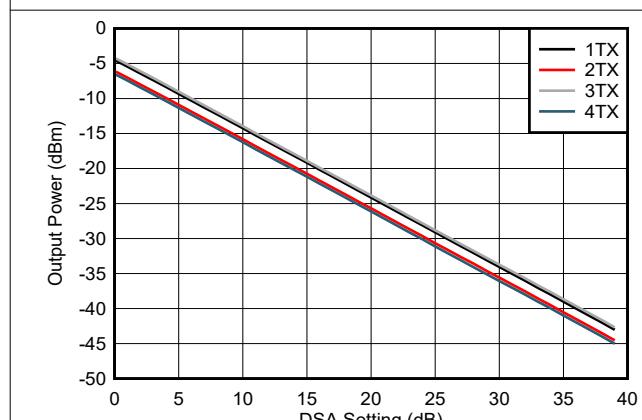
Includes PCB and cable losses.

**Figure 4-233. TX Output Power vs Frequency at 9.61 GHz**



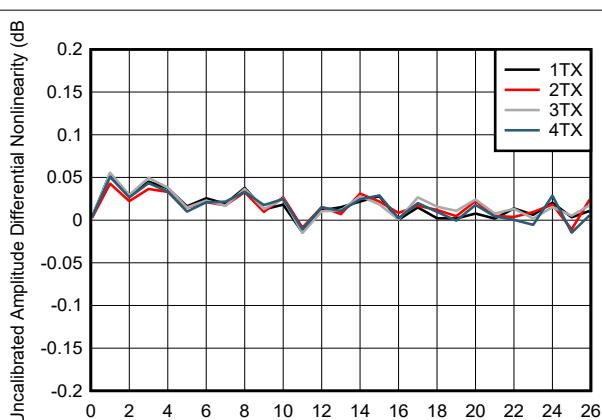
Includes PCB and cable losses.

**Figure 4-234. TX Output Power vs Frequency at 9.61 GHz**

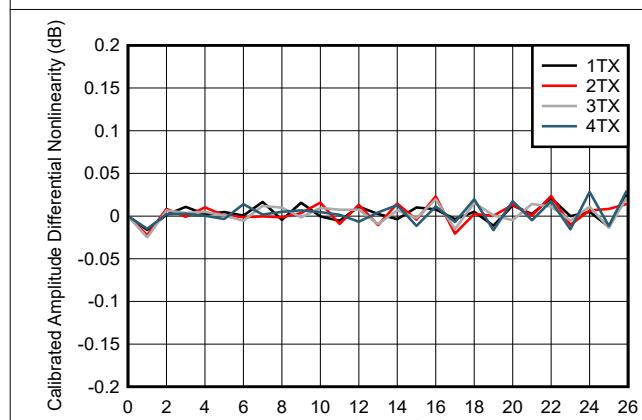


Includes PCB and cable losses.

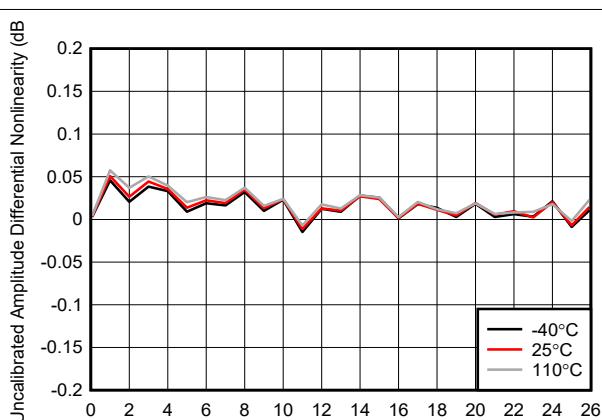
**Figure 4-235. TX Output Power vs DSA Setting at 9.61 GHz**



**Figure 4-236. TX DSA Uncalibrated Amplitude Differential Nonlinearity**



**Figure 4-237. TX DSA Calibrated Amplitude Differential Nonlinearity**



**Figure 4-238. TX DSA Uncalibrated Amplitude Differential Nonlinearity**

#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching

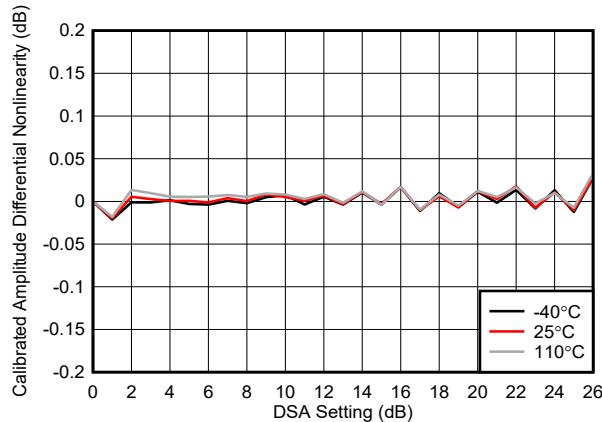


Figure 4-239. TX DSA Calibrated Amplitude Differential Nonlinearity

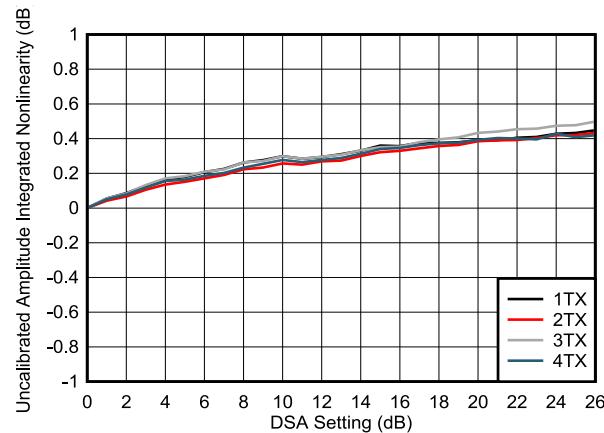


Figure 4-240. TX DSA Uncalibrated Amplitude Integrated Nonlinearity

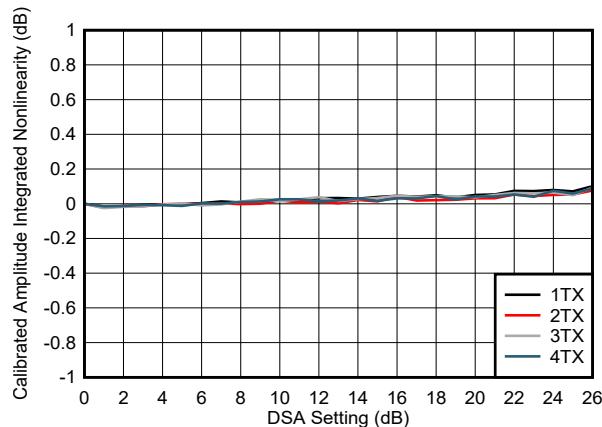


Figure 4-241. TX DSA Calibrated Amplitude Integrated Nonlinearity

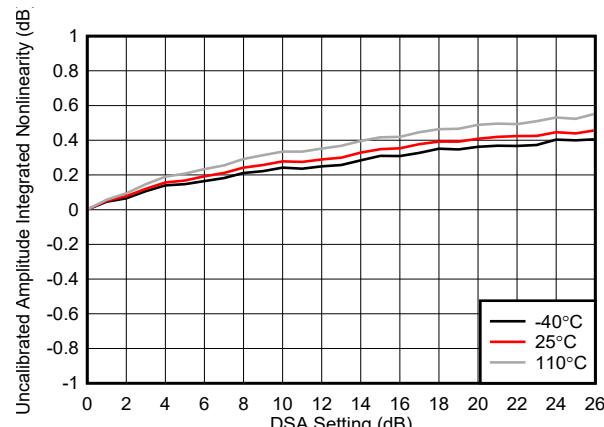


Figure 4-242. TX DSA Uncalibrated Amplitude Integrated Nonlinearity

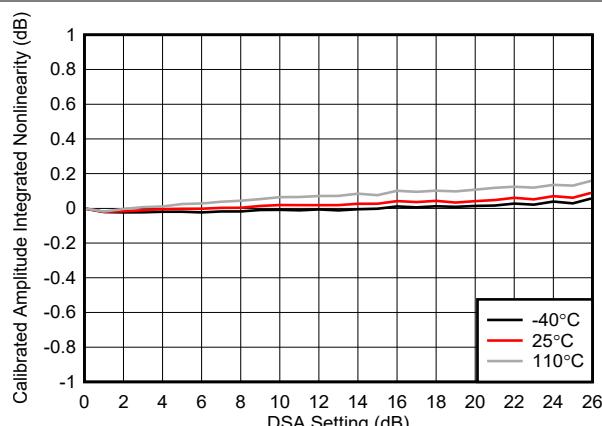


Figure 4-243. TX DSA Calibrated Amplitude Integrated Nonlinearity

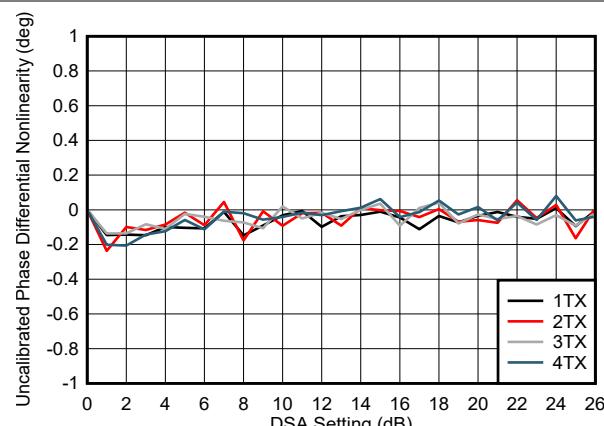


Figure 4-244. TX DSA Uncalibrated Phase Differential Nonlinearity

#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching

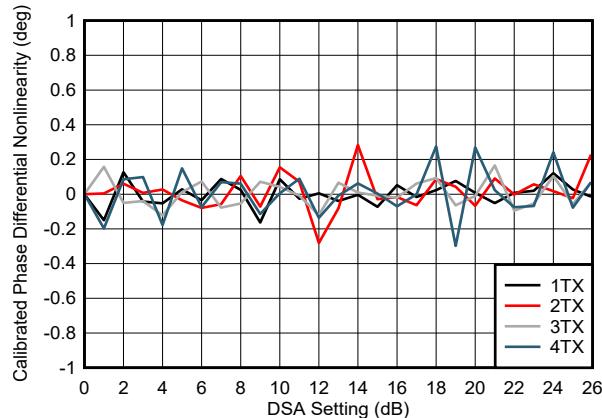


Figure 4-245. TX DSA Calibrated Phase Differential Nonlinearity

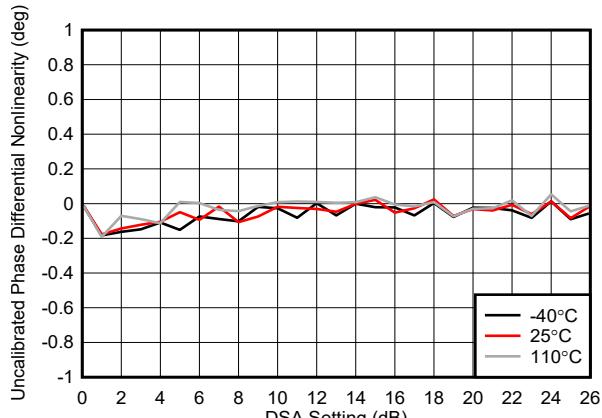


Figure 4-246. TX DSA Uncalibrated Phase Differential Nonlinearity

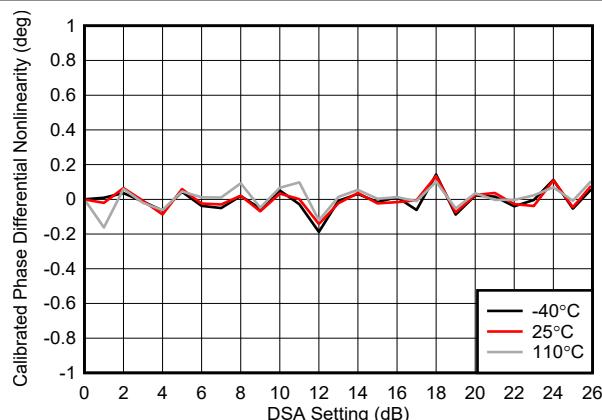


Figure 4-247. TX DSA Calibrated Phase Differential Nonlinearity

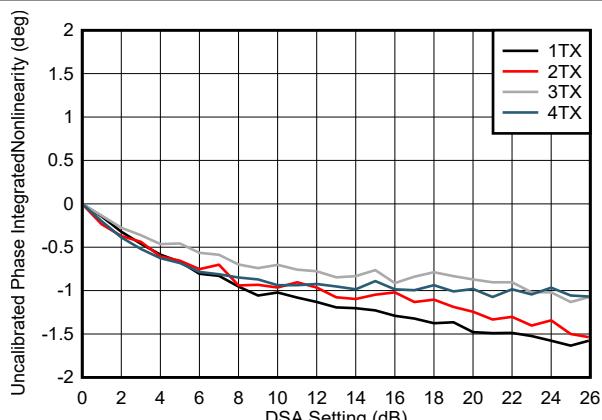


Figure 4-248. TX DSA Uncalibrated Phase Integrated Nonlinearity

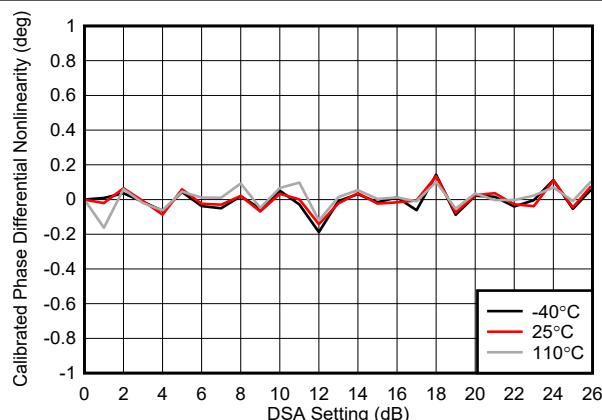


Figure 4-249. TX DSA Calibrated Phase Integrated Nonlinearity

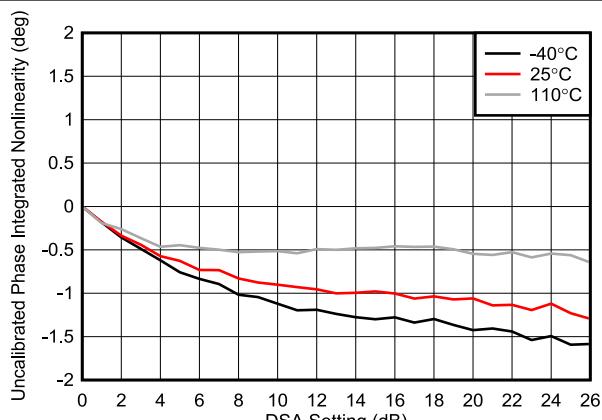


Figure 4-250. TX DSA Uncalibrated Phase Integrated Nonlinearity

#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching

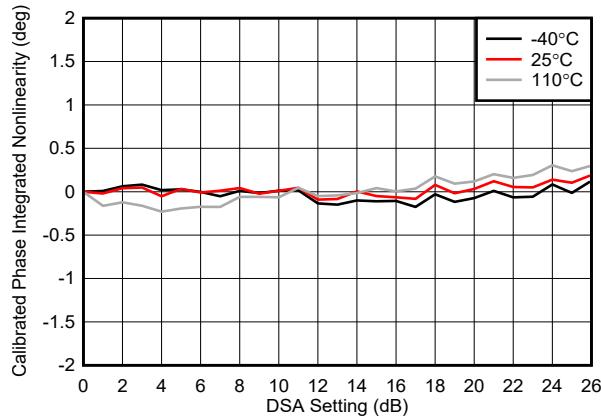


Figure 4-251. TX DSA Calibrated Amplitude Integrated Nonlinearity

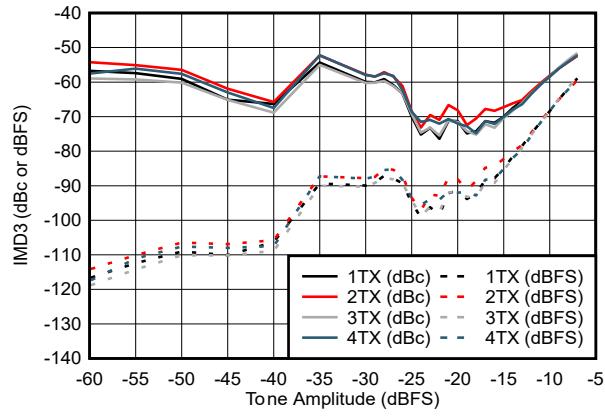


Figure 4-252. TX IMD3 vs Digital Amplitude at 9.61 GHz

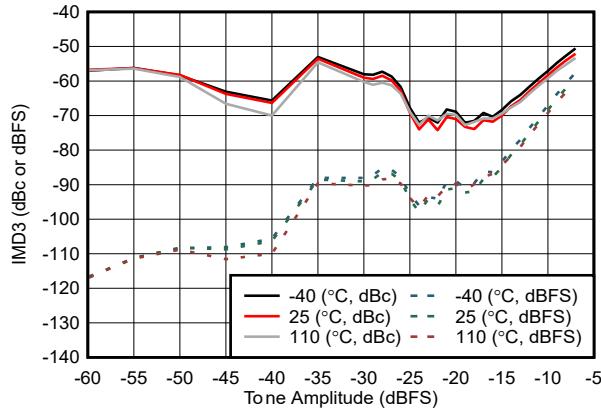


Figure 4-253. TX IMD3 vs Digital Amplitude at 9.61 GHz

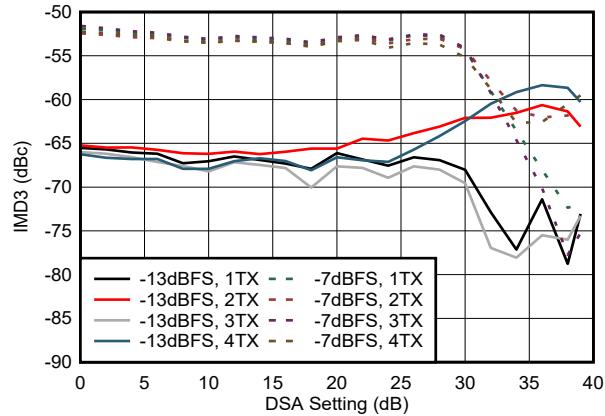
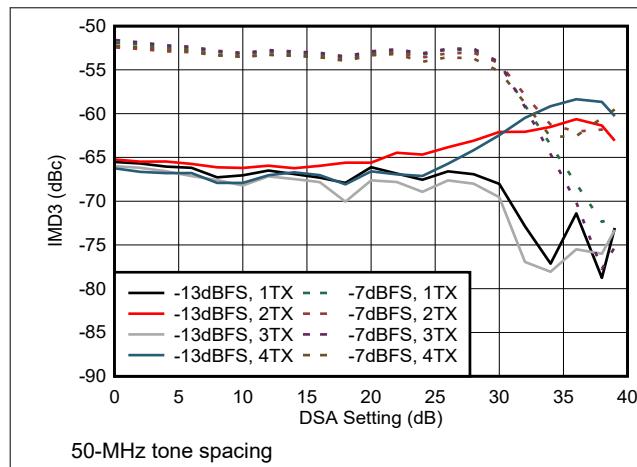


Figure 4-254. TX IMD3 vs DSA Setting at 9.61 GHz

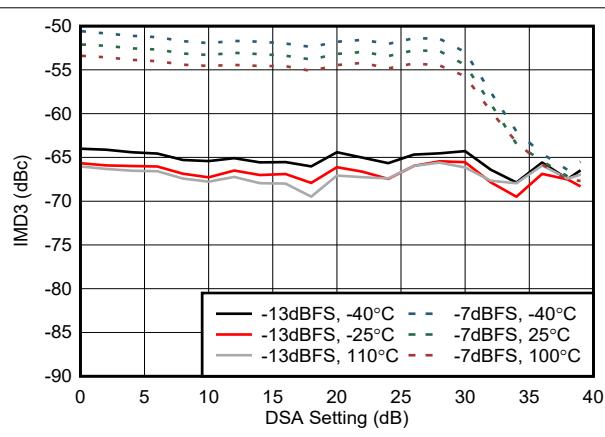
#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching



50-MHz tone spacing

Figure 4-255. TX IMD3 vs DSA Setting at 9.61 GHz



50-MHz tone spacing

Figure 4-256. TX IMD3 vs DSA Setting at 9.61 GHz

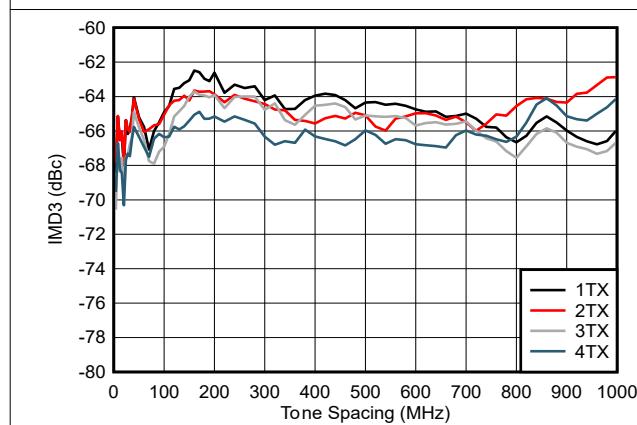


Figure 4-257. TX IMD3 vs Tone Spacing at 9.61 GHz

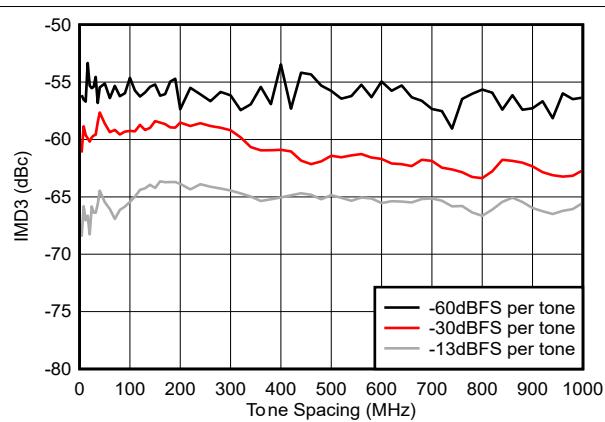


Figure 4-258. TX IMD3 vs Tone Spacing at 9.61 GHz

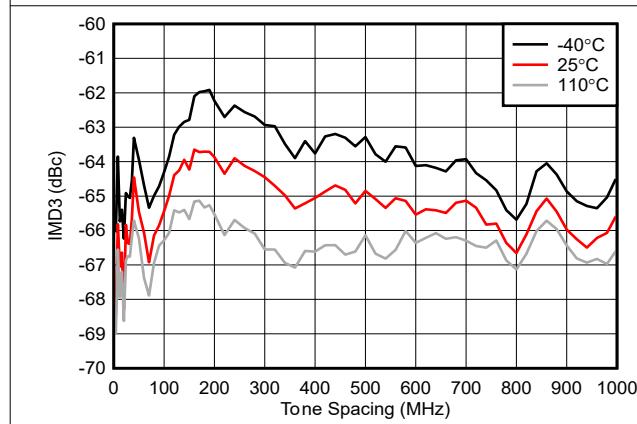


Figure 4-259. TX IMD3 vs Tone Spacing at 9.61 GHz

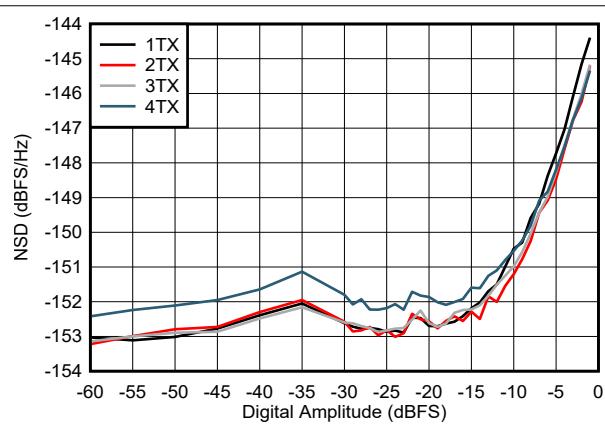


Figure 4-260. TX NSD vs Digital Amplitude at 9.61 GHz

#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching

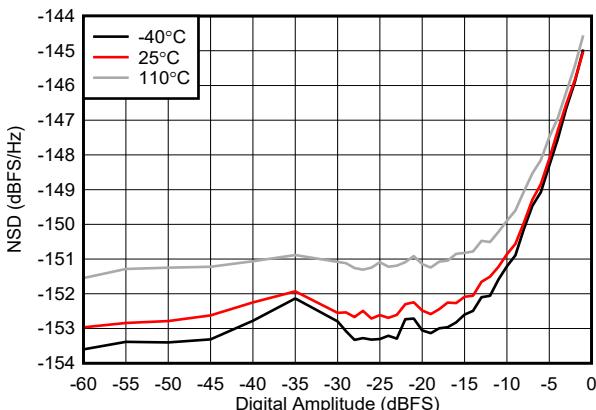


Figure 4-261. TX NSD vs Digital Amplitude at 9.61 GHz

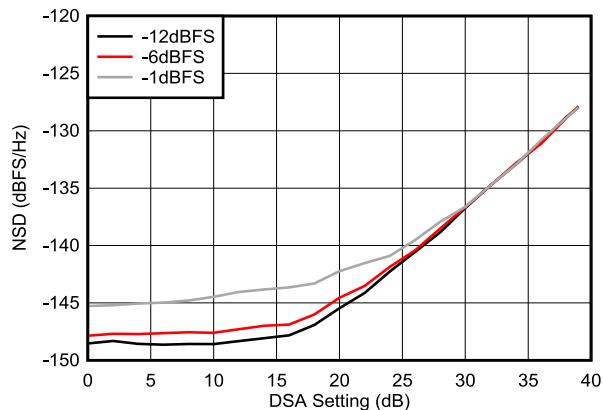


Figure 4-262. TX NSD vs DSA Setting at 9.61 GHz

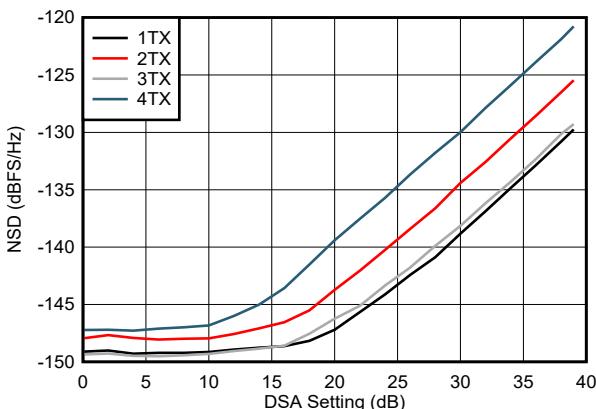


Figure 4-263. TX NSD vs DSA Setting at 9.61 GHz

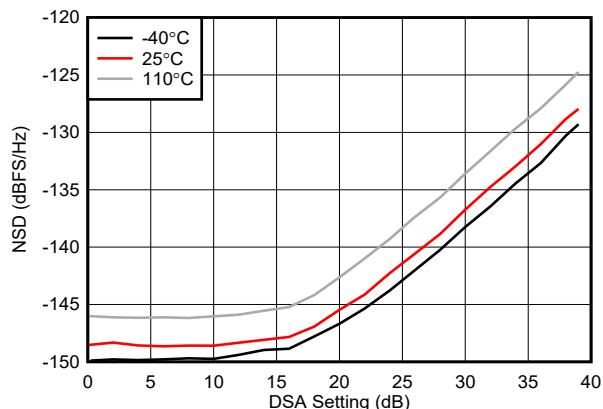
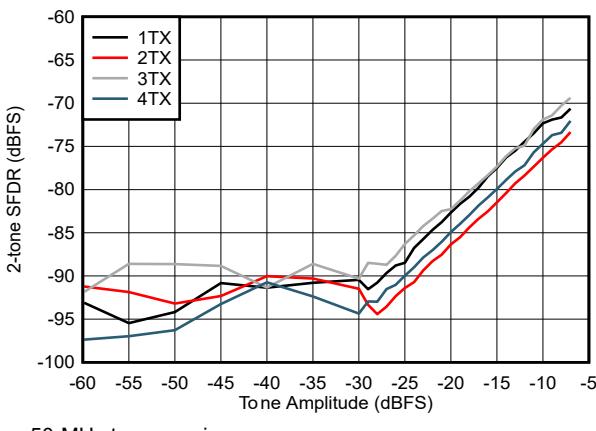
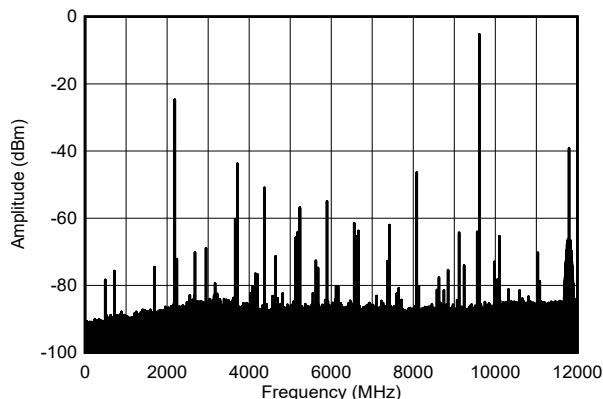


Figure 4-264. TX NSD vs DSA Setting at 9.61 GHz



50-MHz tone spacing

Figure 4-265. TX 2-tone SFDR vs Digital Amplitude at 9.61 GHz

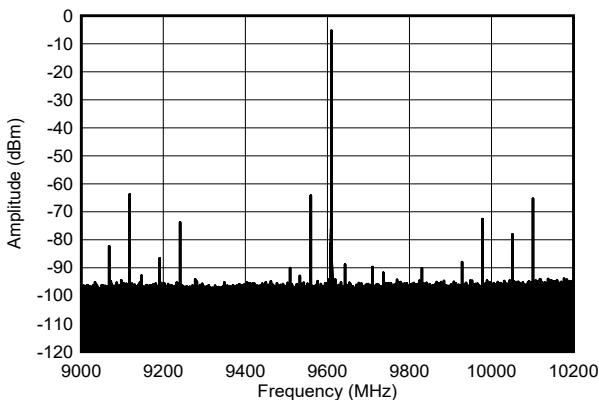


Includes PCB and cable losses.

Figure 4-266. TX Single Tone Spectrum at 9.61 GHz and -1dBFS (wideband)

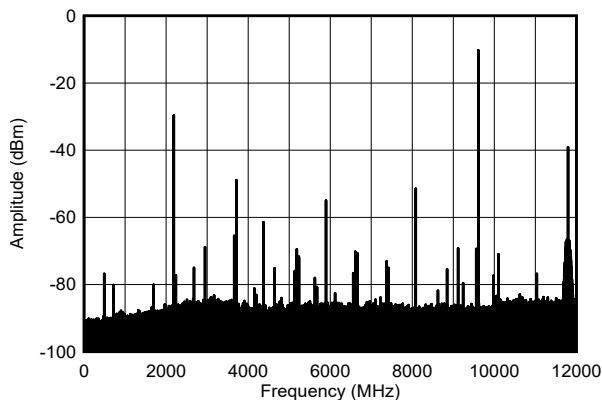
#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching



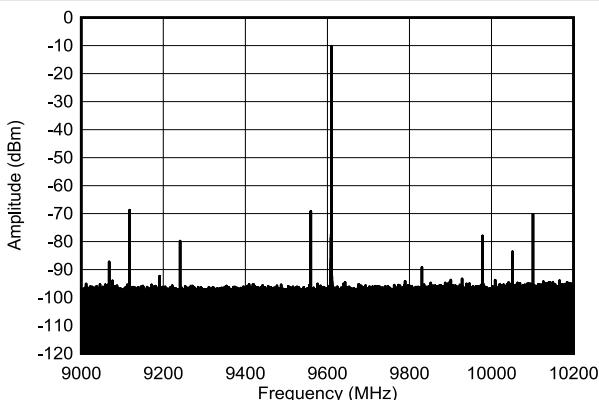
Includes PCB and cable losses.

**Figure 4-267. TX Single Tone Spectrum at 9.61 GHz and -1dBFS (1.2GHz BW)**



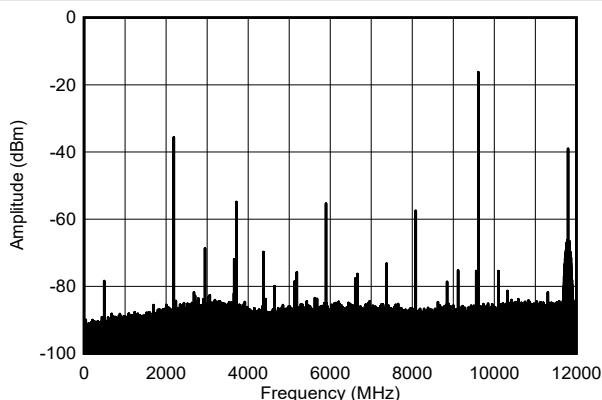
Includes PCB and cable losses.

**Figure 4-268. TX Single Tone Spectrum at 9.61 GHz and -6dBFS (wideband)**



Includes PCB and cable losses.

**Figure 4-269. TX Single Tone Spectrum at 9.61 GHz and -6dBFS (1.2GHz BW)**

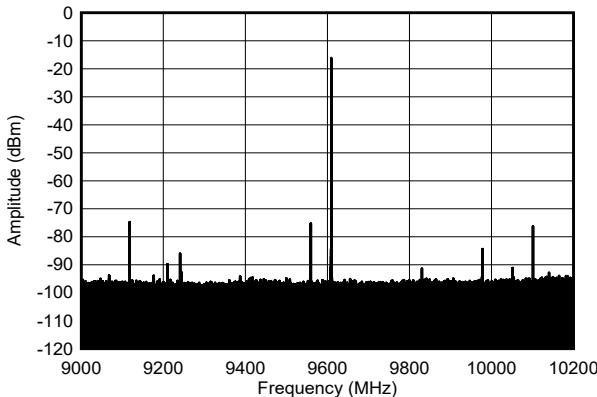


Includes PCB and cable losses.

**Figure 4-270. TX Single Tone Spectrum at 9.61 GHz and -12dBFS (wideband)**

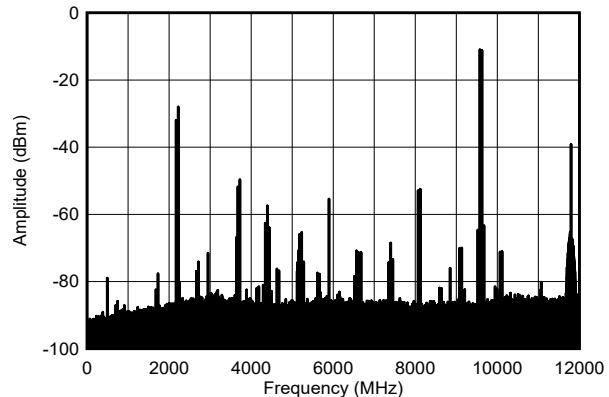
#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching



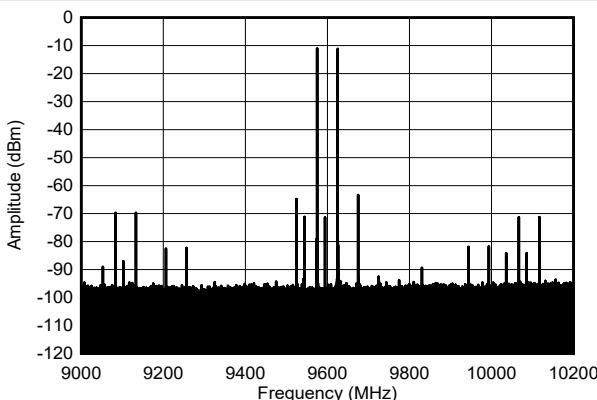
Includes PCB and cable losses.

**Figure 4-271. TX Single Tone Spectrum at 9.61 GHz and -12dBFS (1.2GHz BW)**



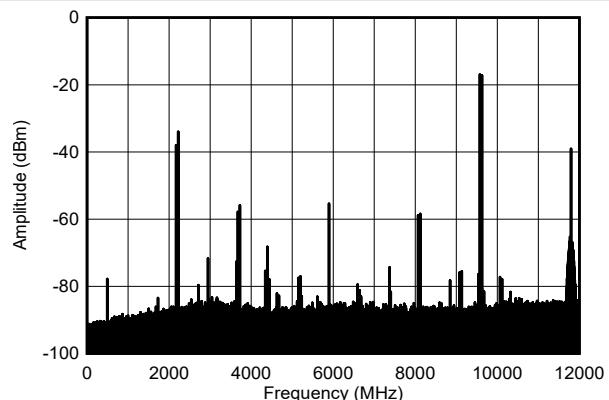
Includes PCB and cable losses, 50-MHz tone spacing.

**Figure 4-272. TX 2-Tone Spectrum at 9.61 GHz and -7dBFS (wideband)**



Includes PCB and cable losses, 50-MHz tone spacing.

**Figure 4-273. TX 2-Tone Spectrum at 9.61 GHz and -7dBFS (1.2GHz BW)**

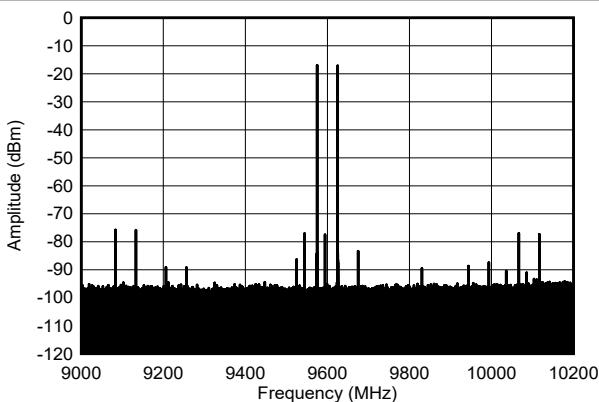


Includes PCB and cable losses, 50-MHz tone spacing.

**Figure 4-274. TX 2-Tone Spectrum at 9.61 GHz and -13dBFS (wideband)**

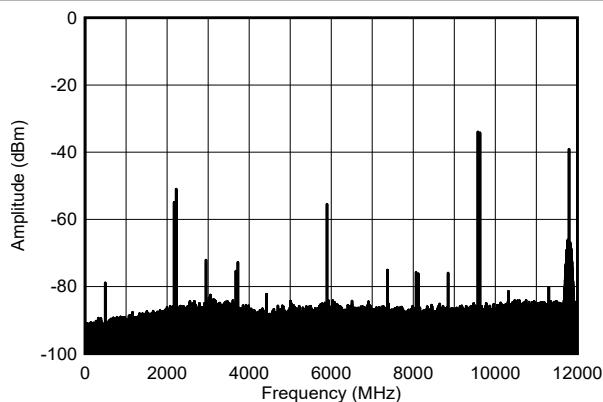
#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching



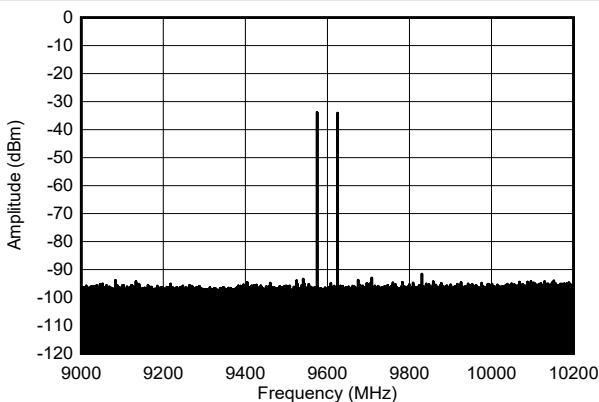
Includes PCB and cable losses, 50-MHz tone spacing.

**Figure 4-275. TX 2-Tone Spectrum at 9.61 GHz and -13dBFS (1.2GHz BW)**



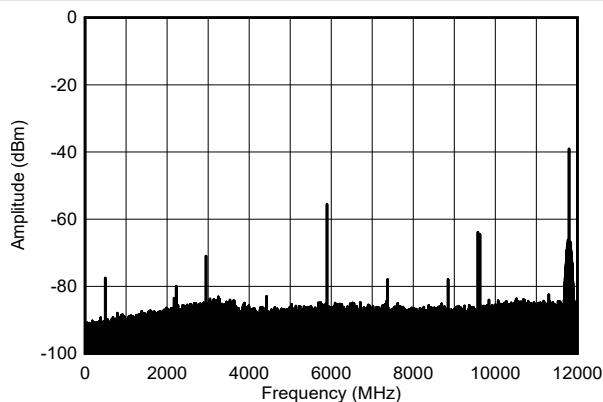
Includes PCB and cable losses, 50-MHz tone spacing.

**Figure 4-276. TX 2-Tone Spectrum at 9.61 GHz and -30dBFS Each (wideband)**



Includes PCB and cable losses, 50-MHz tone spacing.

**Figure 4-277. TX 2-Tone Spectrum at 9.61 GHz and -30dBFS Each (1.2GHz BW)**

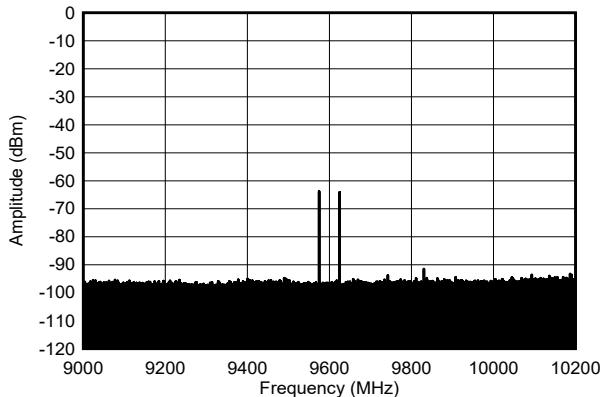


Includes PCB and cable losses, 50-MHz tone spacing.

**Figure 4-278. TX 2-Tone Spectrum at 9.61 GHz and -60dBFS Each (wideband)**

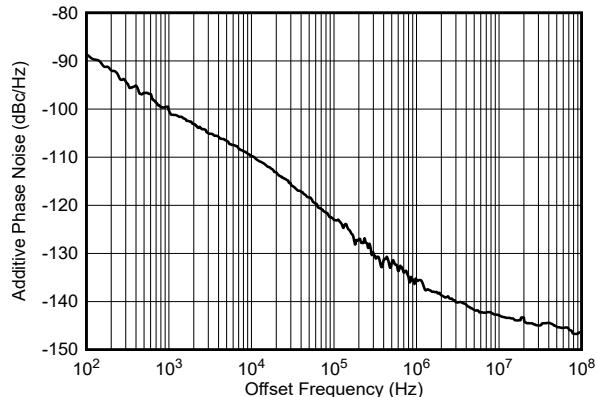
#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching



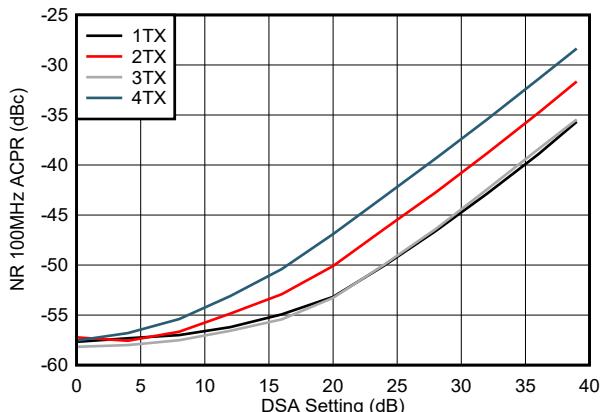
Includes PCB and cable losses, 50-MHz tone spacing.

**Figure 4-279. TX 2-Tone Spectrum at 9.61 GHz and -60dBFS Each (1.2GHz BW)**

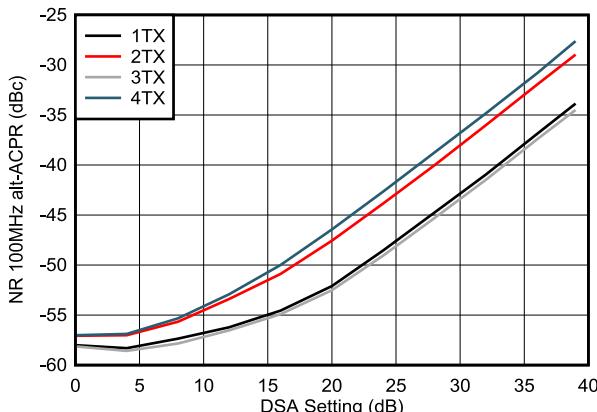


Single sideband, external clock mode, input clock phase noise removed

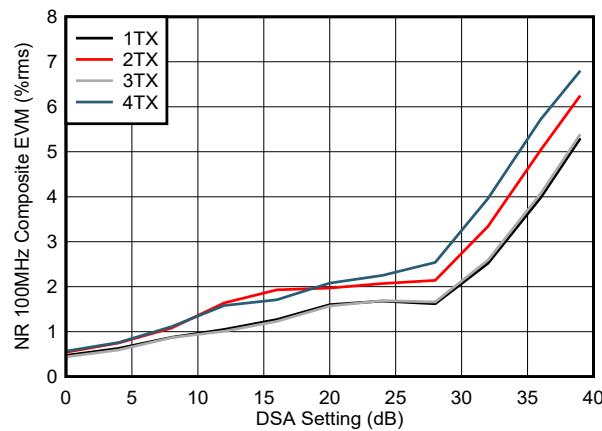
**Figure 4-280. TX Additive Phase Noise vs Offset Frequency at 9.61 GHz**



**Figure 4-281. TX NR100MHz ACPR vs DSA Setting at 9.61 GHz**



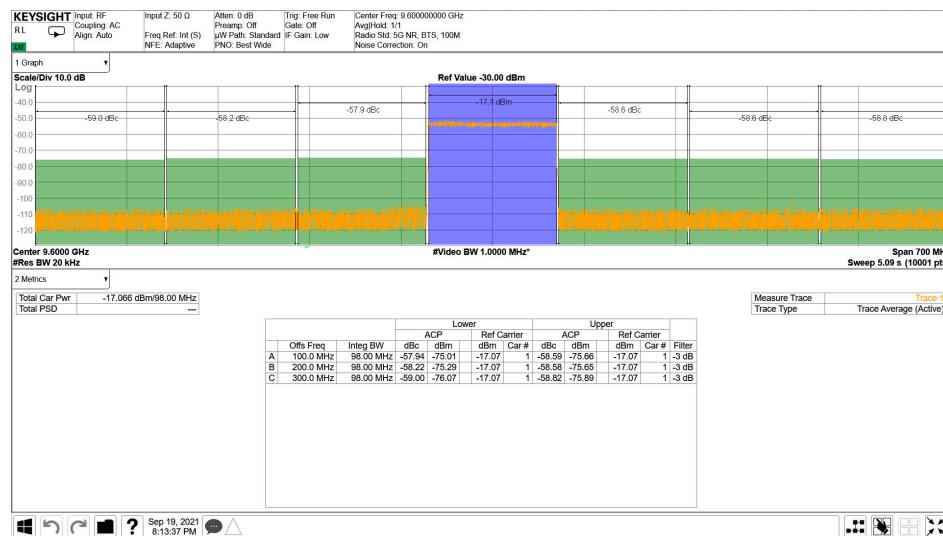
**Figure 4-282. TX NR100MHz alt-ACPR vs DSA Setting at 9.61 GHz**



**Figure 4-283. TX NR100MHz EVM vs DSA Setting at 9.61 GHz**

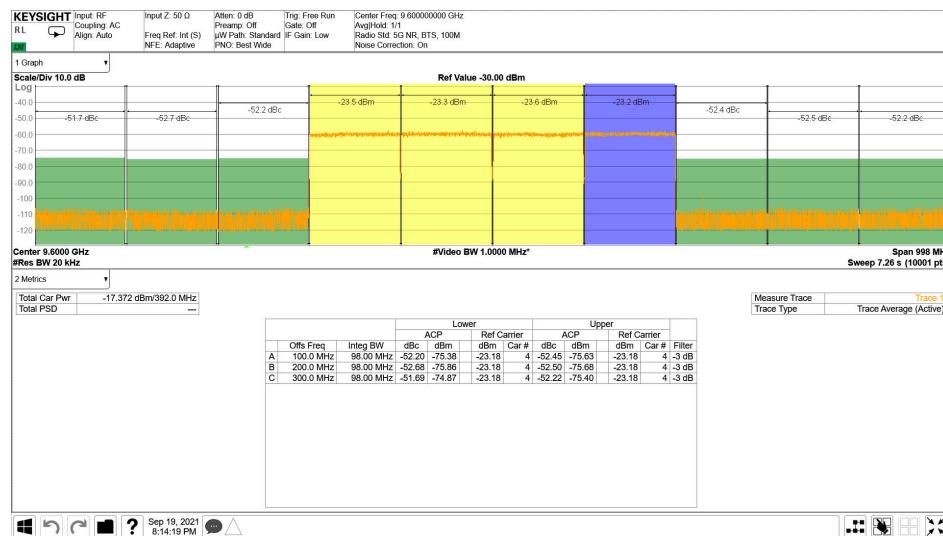
#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching



Includes PCB and cable losses.

Figure 4-284. TX NR100MHz Output Spectrum at 9.61 GHz

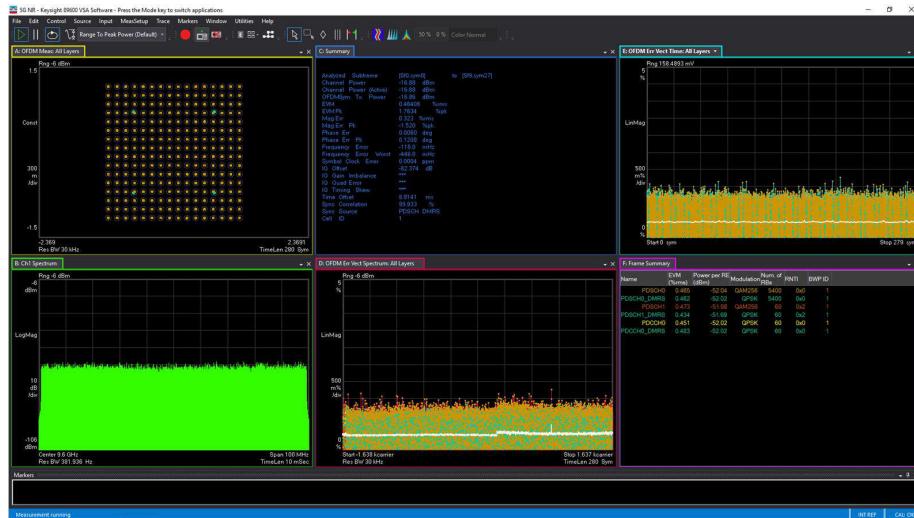


Includes PCB and cable losses.

Figure 4-285. TX 4xNR100MHz Output Spectrum at 9.61 GHz

#### 4.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56 MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6 GHz matching



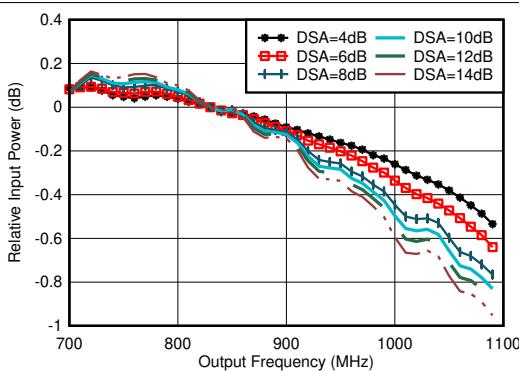
#### Note

Includes PCB and cable losses.

Figure 4-286. TX 100MHz NR EVM at 9.61 GHz

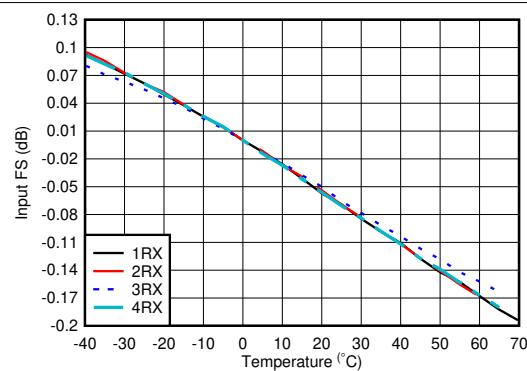
#### 4.12.8 RX Typical Characteristics at 800 MHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 0.8 GHz matching, normalized to 830 MHz

Figure 4-287. RX In-Band Gain Flatness for Channel 1RX,  $f_{\text{IN}} = 830\text{ MHz}$

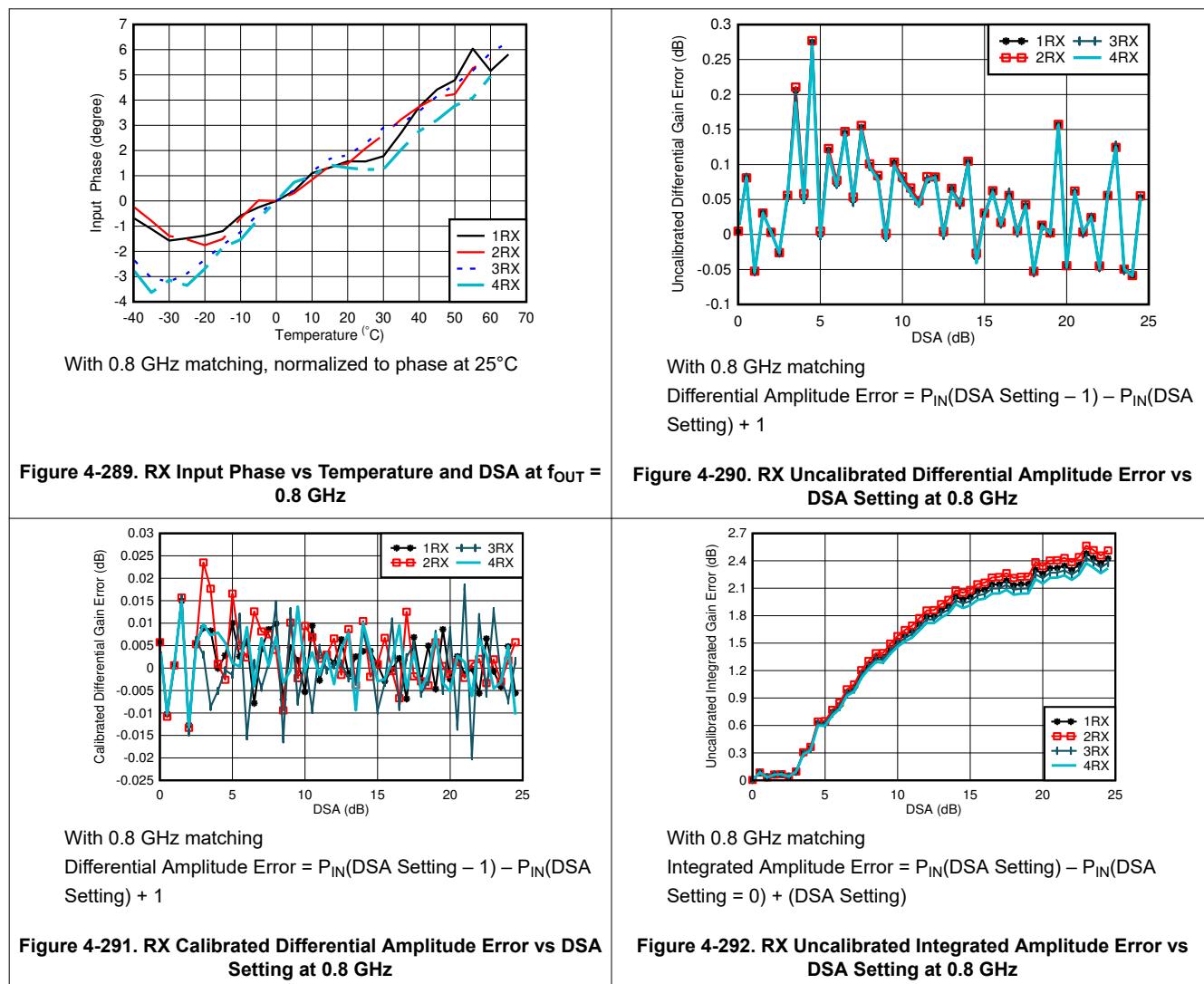


With 0.8 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

Figure 4-288. RX Input Fullscale vs Temperature and Channel at 800MHz

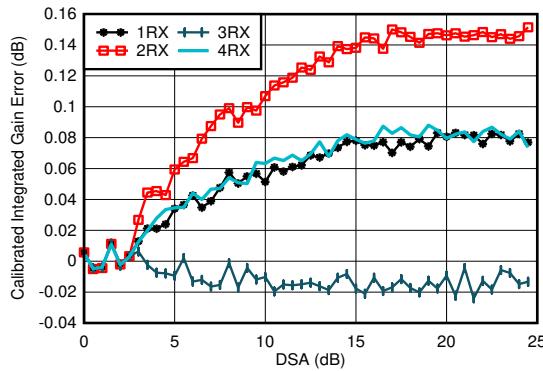
#### 4.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



#### 4.12.8 RX Typical Characteristics at 800 MHz (continued)

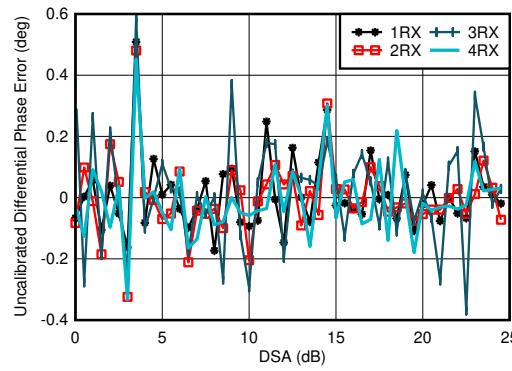
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



With 0.8 GHz matching

Integrated Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

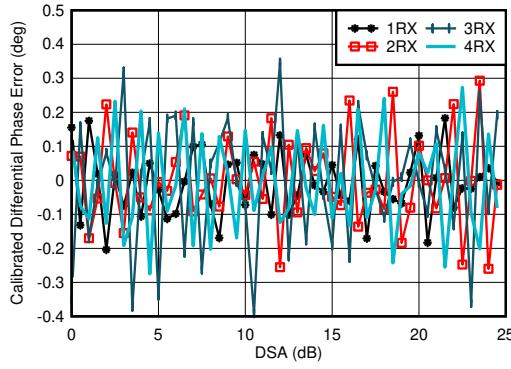
**Figure 4-293. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz**



With 0.8 GHz matching

Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

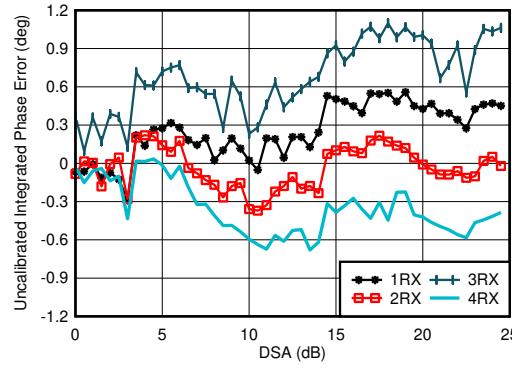
**Figure 4-294. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz**



With 0.8 GHz matching

Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

**Figure 4-295. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz**



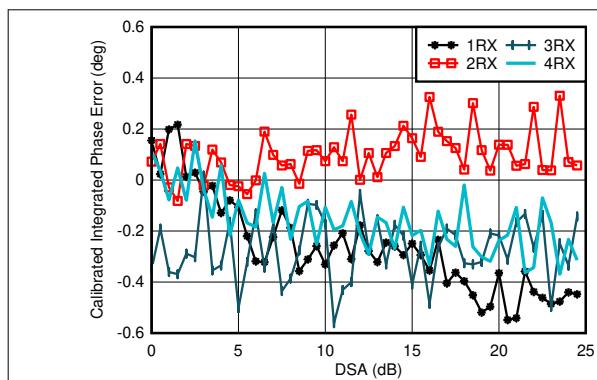
With 0.8 GHz matching

Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-296. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz**

#### 4.12.8 RX Typical Characteristics at 800 MHz (continued)

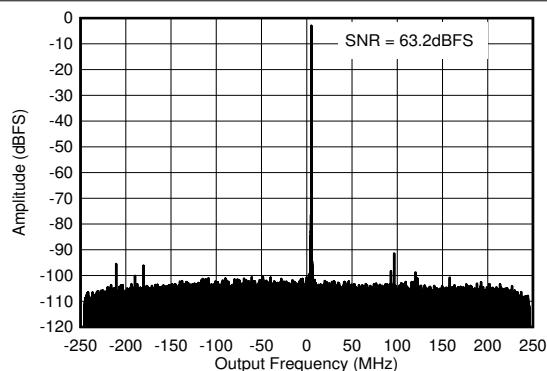
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



With 0.8 GHz matching

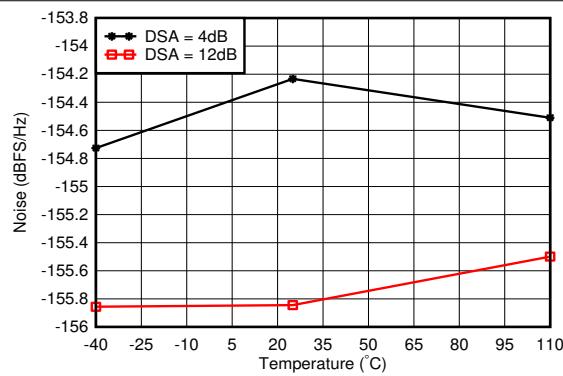
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 4-297. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz**



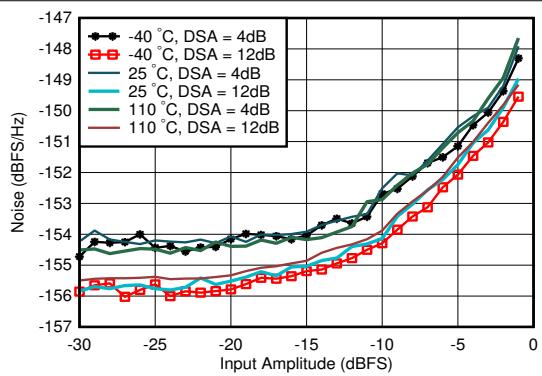
With 0.8 GHz matching,  $f_{\text{IN}} = 840$  MHz,  $A_{\text{IN}} = -3$  dBFS

**Figure 4-298. RX Output FFT at 0.8 GHz**



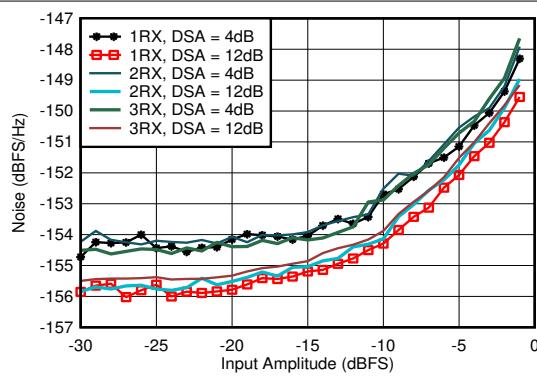
With 0.8 GHz matching, 12.5-MHz offset from tone

**Figure 4-299. RX Noise Spectral Density vs Temperature at 0.8 GHz**



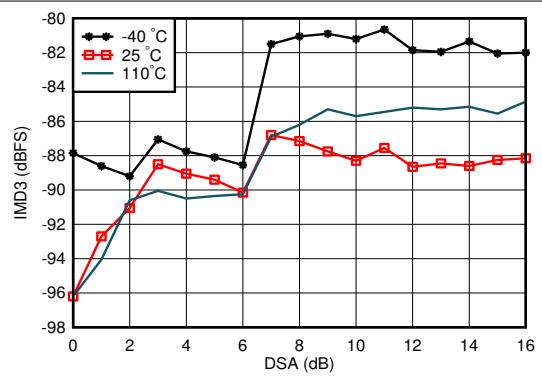
With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 4-300. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz**



With 0.8 GHz matching, 12.5-MHz offset from tone

**Figure 4-301. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz**

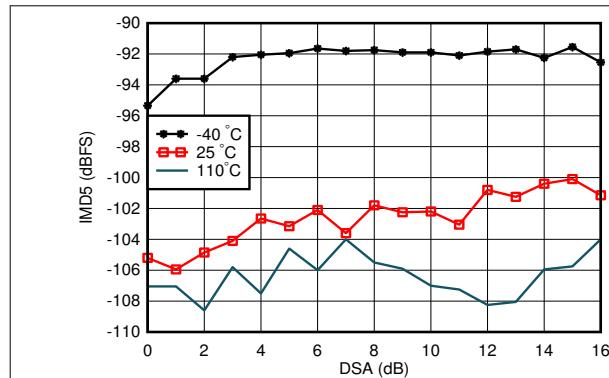


With 0.8 GHz matching, each tone  $-7$  dBFS, tone spacing = 20 MHz

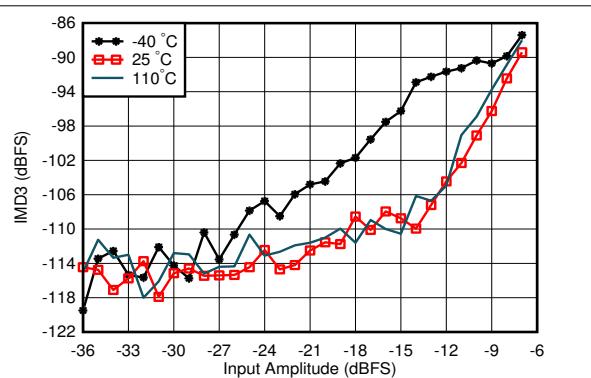
**Figure 4-302. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz**

#### 4.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.

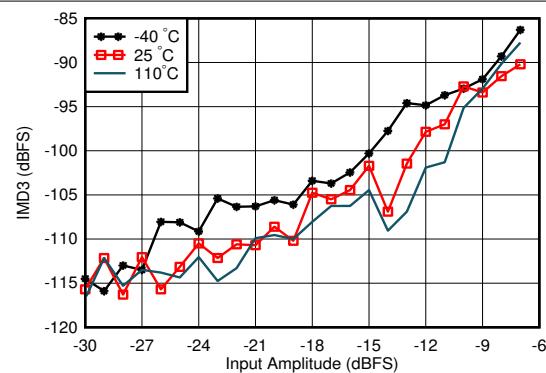


With 0.8 GHz matching, each tone -7 dBFS, tone spacing = 20 MHz

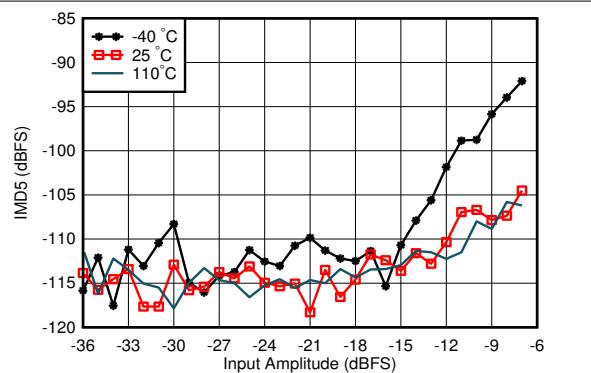


With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

**Figure 4-303. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz**



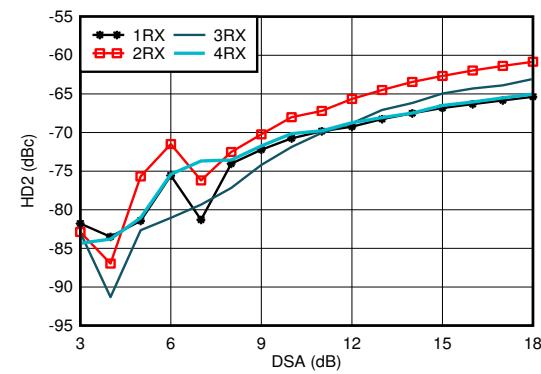
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB



With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

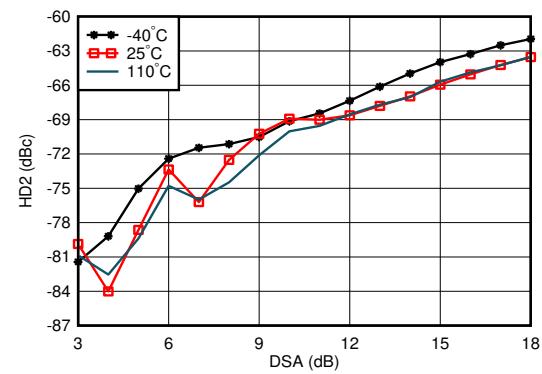
**Figure 4-305. RX IMD3 vs Input Level and Temperature at 0.8 GHz**

**Figure 4-306. RX IMD5 vs Input Level and Temperature at 0.8 GHz**



With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 4-307. RX HD2 vs DSA Setting and Channel at 0.8 GHz**

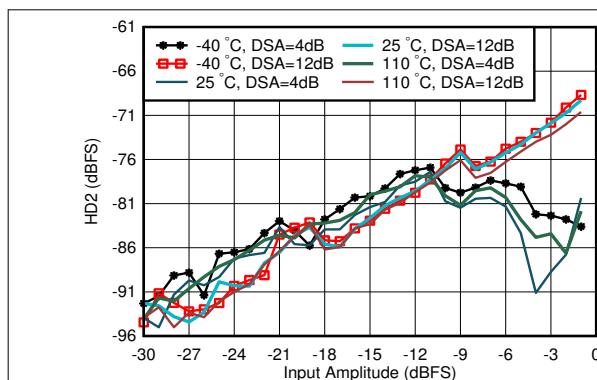


With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 4-308. RX HD2 vs DSA Setting and Temperature at 0.8 GHz**

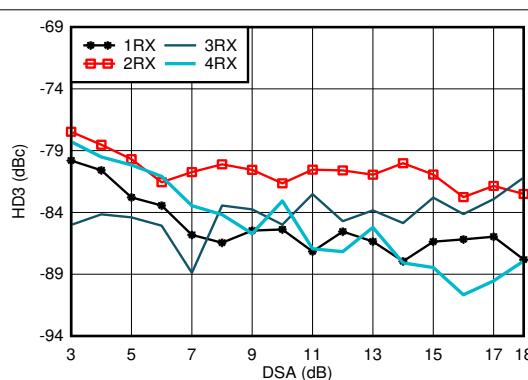
#### 4.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



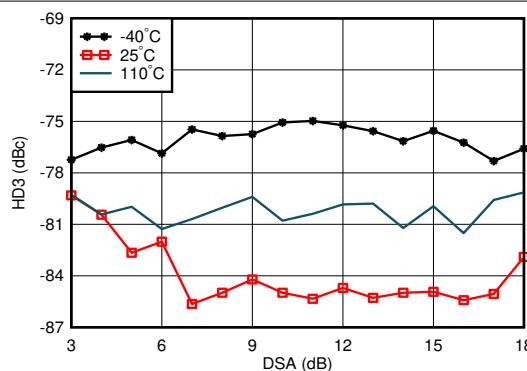
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 4-309. RX HD2 vs Input Level and Temperature at 0.8 GHz**



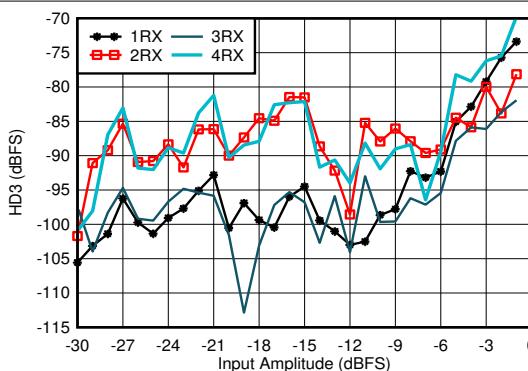
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-310. RX HD3 vs DSA Setting and Channel at 0.8 GHz**



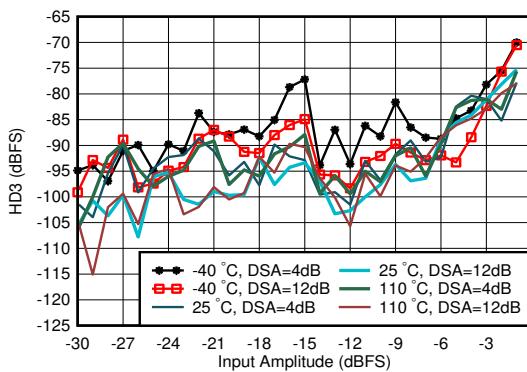
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-311. RX HD3 vs DSA Setting and Temperature at 0.8 GHz**



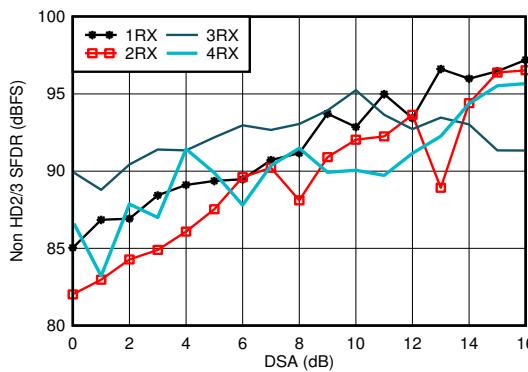
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-312. RX HD3 vs Input Level and Channel at 0.8 GHz**



With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-313. RX HD3 vs Input Level and Temperature at 0.8 GHz**

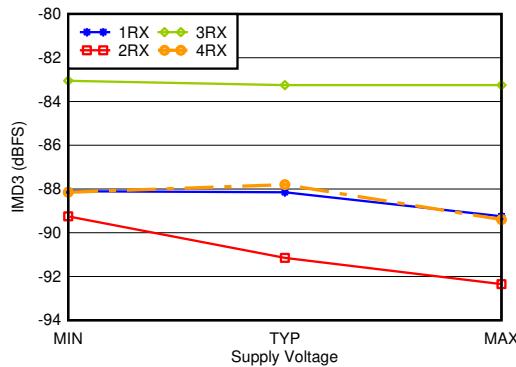


With 0.8 GHz matching

**Figure 4-314. RX Non-HD2/3 vs DSA Setting at 0.8 GHz**

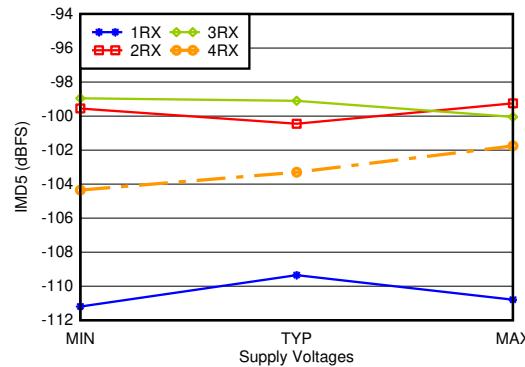
#### 4.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



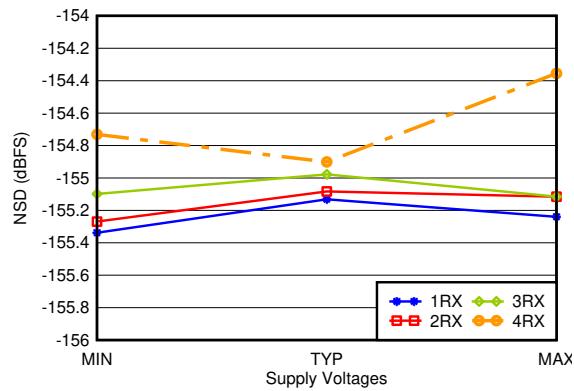
With 0.8 GHz matching,  $-7$  dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-315. RX IMD3 vs Supply and Channel at 0.8 GHz



With 0.8 GHz matching,  $-7$  dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-316. RX IMD5 vs Supply and Channel at 0.8 GHz

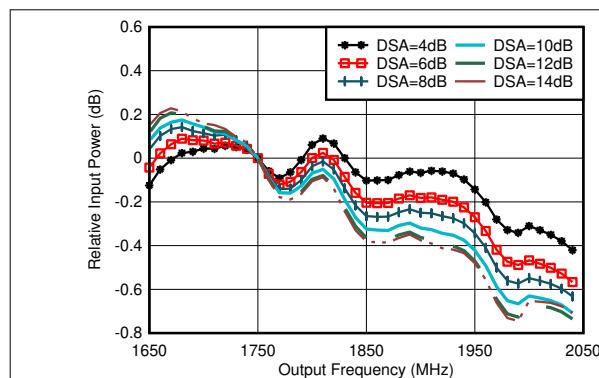


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

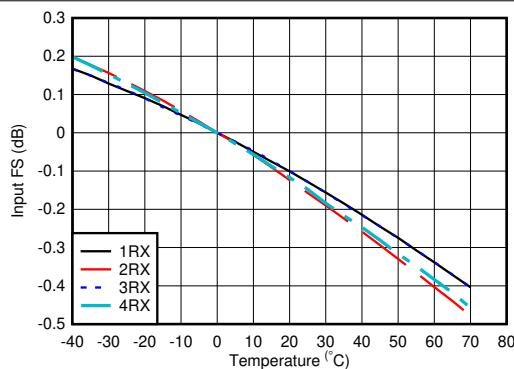
Figure 4-317. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

#### 4.12.9 RX Typical Characteristics at 1.75 GHz – 1.9 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



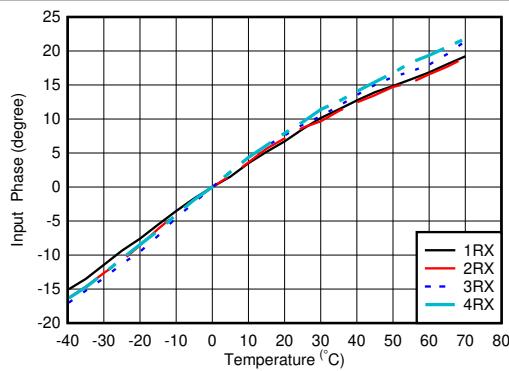
With 1.8 GHz matching, normalized to 1.75 GHz



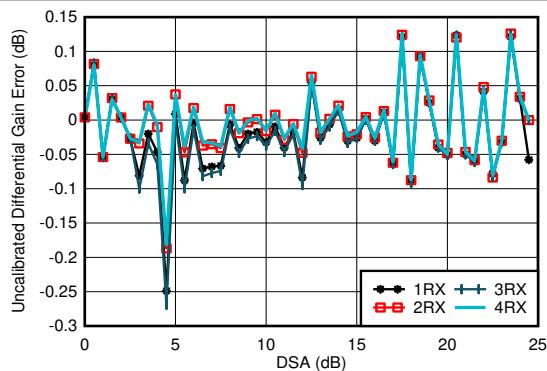
With 1.8 GHz matching, normalized to fullscale at 25°C for each channel

Figure 4-318. RX In-Band Gain Flatness,  $f_{\text{IN}} = 1750$  MHz

Figure 4-319. RX Input Fullscale vs Temperature and Channel at 1.75 GHz



With 2.6 GHz matching, normalized to phase at 25°C



With 1.8 GHz matching

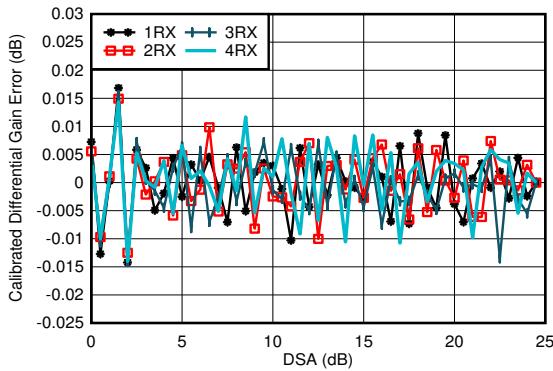
Differential Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 4-320. RX Input Phase vs Temperature and DSA at  $f_{\text{IN}} = 1.75$  GHz

Figure 4-321. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz

#### 4.12.9 RX Typical Characteristics at 1.75 GHz – 1.9 GHz (continued)

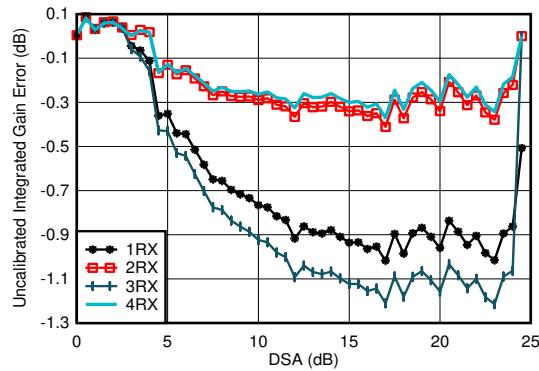
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



With 1.8 GHz matching

$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

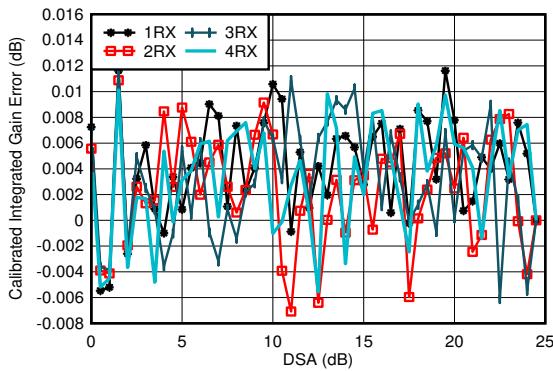
**Figure 4-322. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz**



With 1.8 GHz matching

$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

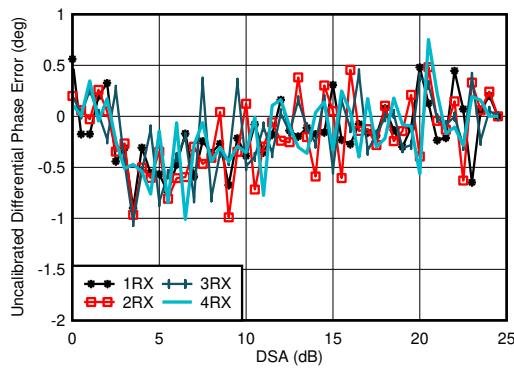
**Figure 4-323. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz**



With 1.8 GHz matching

$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

**Figure 4-324. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz**



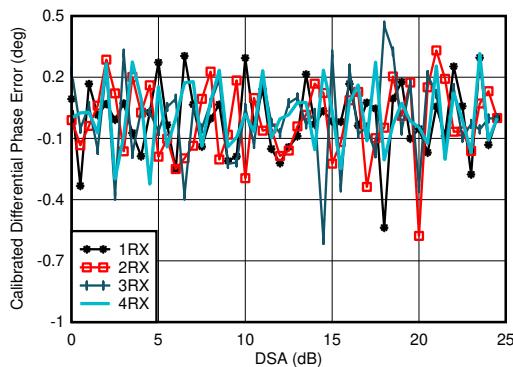
With 1.8 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

**Figure 4-325. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz**

#### 4.12.9 RX Typical Characteristics at 1.75 GHz – 1.9 GHz (continued)

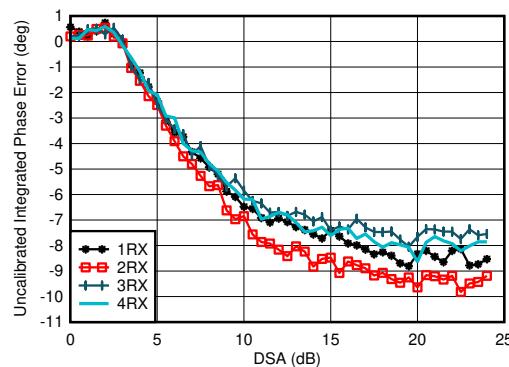
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



With 1.8 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

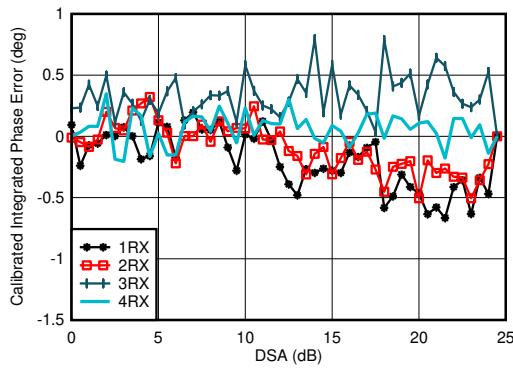
**Figure 4-326. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz**



With 1.8 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

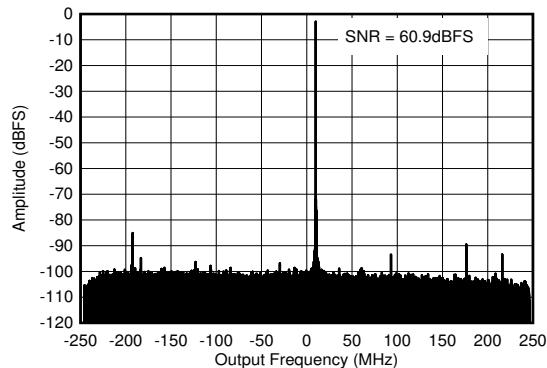
**Figure 4-327. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz**



With 1.8 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 4-328. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz**

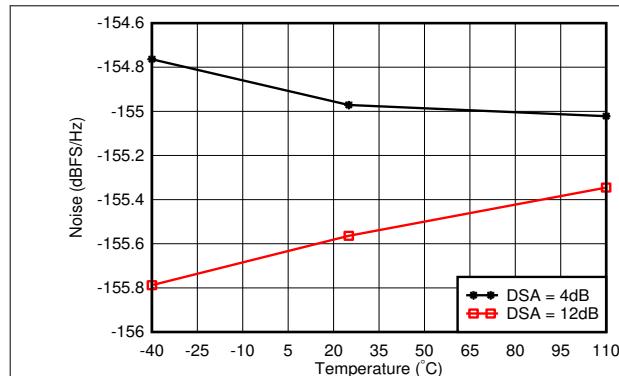


With 1.8 GHz matching,  $f_{\text{IN}} = 2610$  MHz,  $A_{\text{IN}} = -3$  dBFS

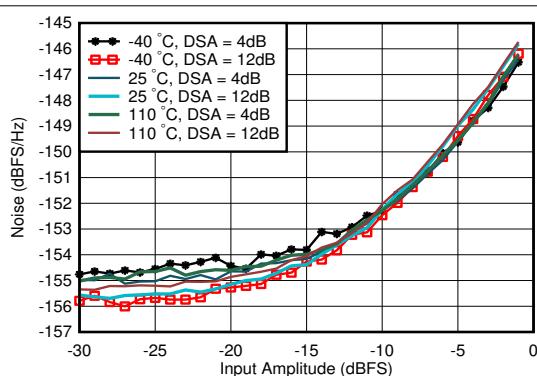
**Figure 4-329. RX Output FFT at 1.75 GHz**

#### 4.12.9 RX Typical Characteristics at 1.75 GHz – 1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.

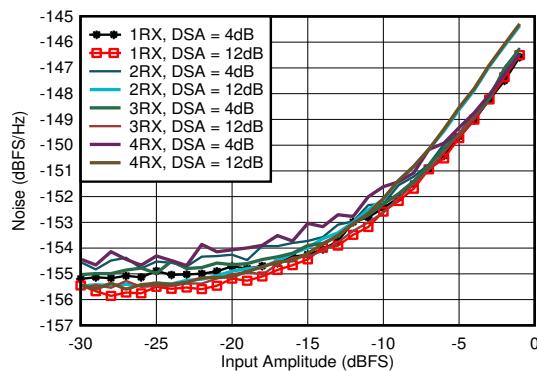


With 1.8 GHz matching, 12.5-MHz offset from tone



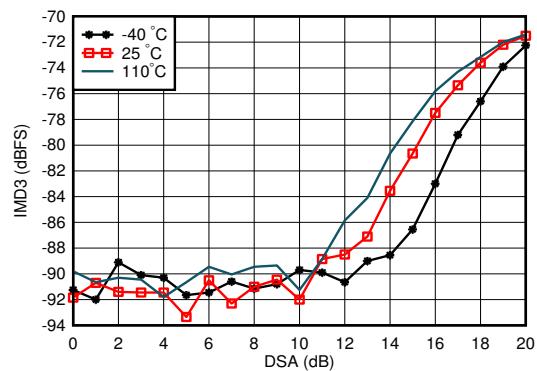
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 4-330. RX Noise Spectral Density vs Temperature at 1.75 GHz**

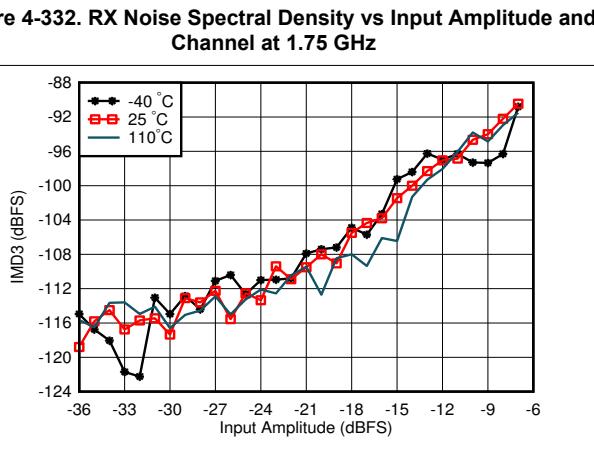


With 1.8 GHz matching, 12.5-MHz offset from tone

**Figure 4-332. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz**

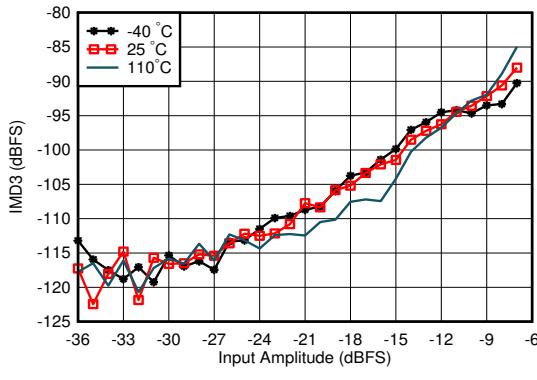


With 1.8 GHz matching, each tone -7 dBFS, tone spacing = 20 MHz



With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

**Figure 4-334. RX IMD3 vs Input Level and Temperature at 1.75 GHz**

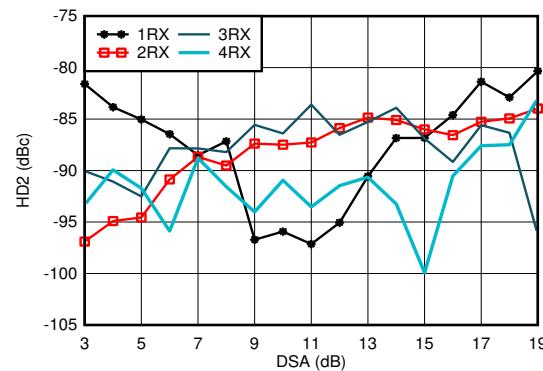


With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 4-335. RX IMD3 vs Input Level and Temperature at 1.75 GHz**

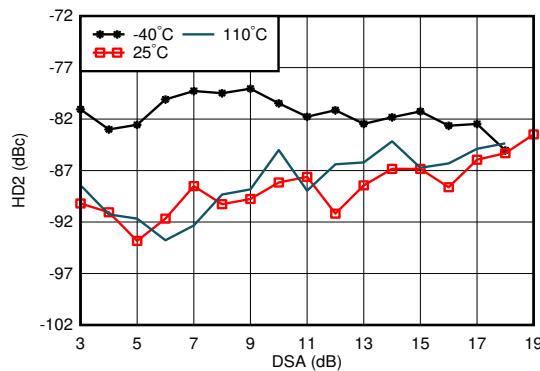
#### 4.12.9 RX Typical Characteristics at 1.75 GHz – 1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



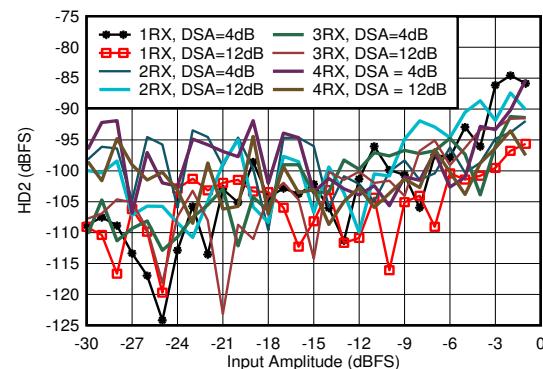
With 1.8 GHz matching,  $f_{\text{in}} = 1900$ MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-336. RX HD2 vs DSA Setting and Channel at 1.9 GHz



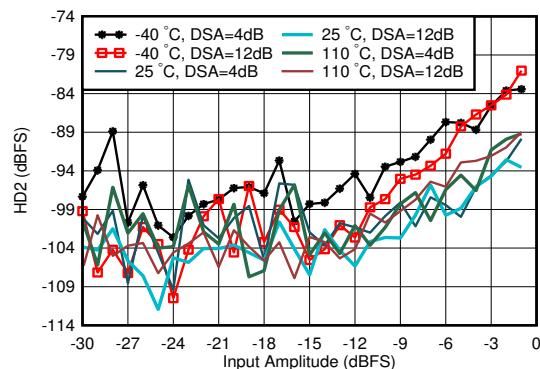
With 1.8 GHz matching,  $f_{\text{in}} = 1900$ MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-337. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



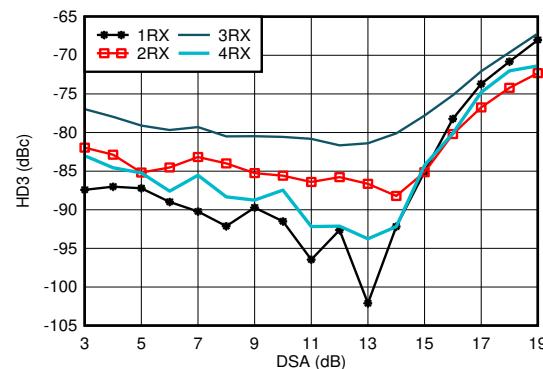
With 1.8 GHz matching,  $f_{\text{in}} = 1900$ MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-338. RX HD2 vs Input Amplitude and Channel at 1.9 GHz



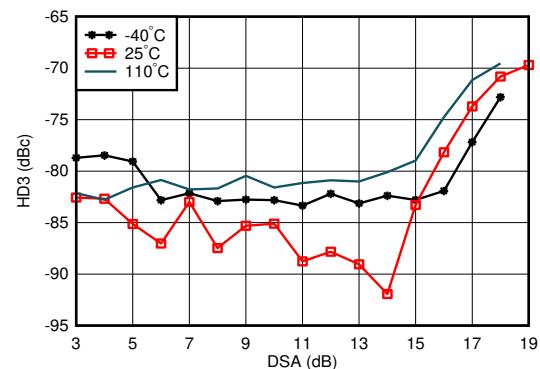
With 1.8 GHz matching,  $f_{\text{in}} = 1900$ MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-339. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz



With 1.8 GHz matching,  $f_{\text{in}} = 1900$ MHz, DDC bypass mode (TI only mode for characterization)

Figure 4-340. RX HD3 vs DSA Setting and Channel at 1.9 GHz

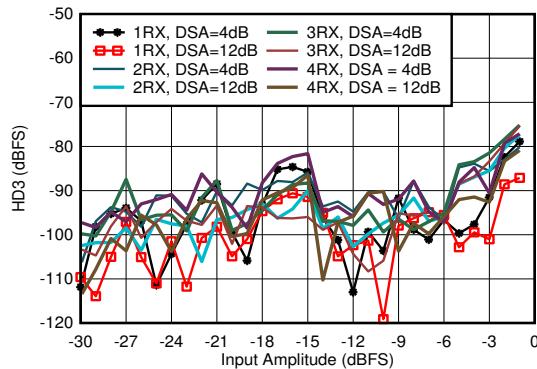


With 1.8 GHz matching,  $f_{\text{in}} = 1900$ MHz, DDC bypass mode (TI only mode for characterization)

Figure 4-341. RX HD3 vs DSA Setting and Temperature at 1.9 GHz

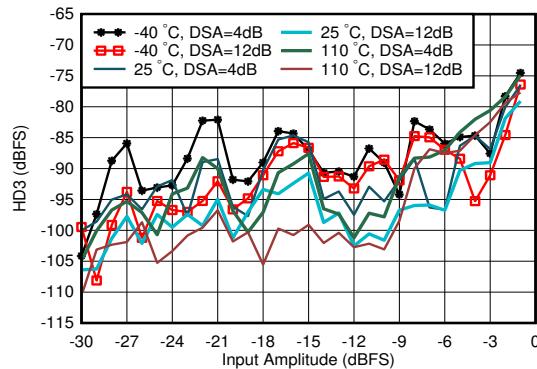
#### 4.12.9 RX Typical Characteristics at 1.75 GHz – 1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



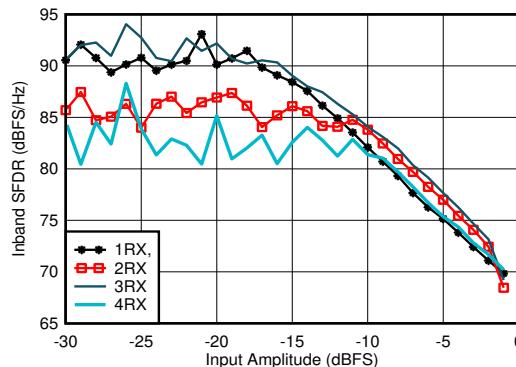
With 1.8 GHz matching,  $f_{\text{in}} = 1900$ MHz, DDC bypass mode (TI only mode for characterization)

Figure 4-342. RX HD3 vs Input Level and Channel at 1.9 GHz



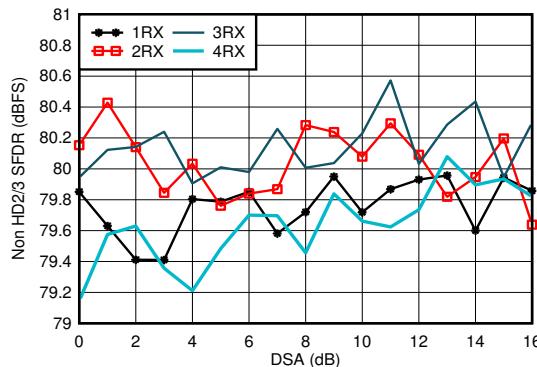
With 1.8 GHz matching,  $f_{\text{in}} = 1900$ MHz, DDC bypass mode (TI only mode for characterization)

Figure 4-343. RX HD3 vs Input Level and Temperature at 1.9 GHz



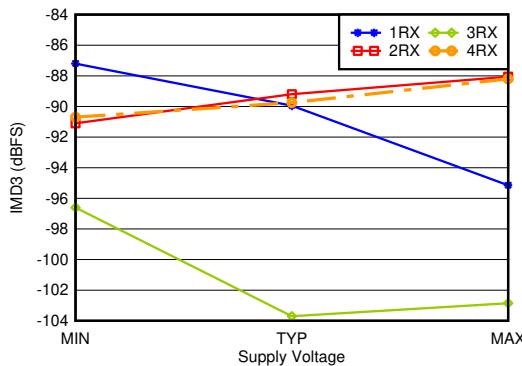
With 1.8 GHz matching, decimated by 3

Figure 4-344. RX In-Band SFDR (\pm400 MHz) vs Input Amplitude at 1.75 GHz



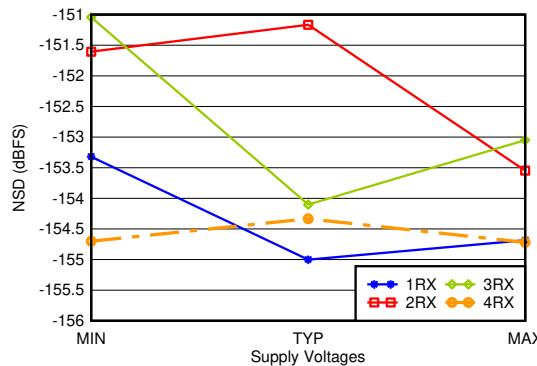
With 1.8 GHz matching

Figure 4-345. RX Non-HD2/3 vs DSA Setting at 1.75 GHz



With 1.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-346. RX IMD3 vs Supply and Channel at 1.75 GHz

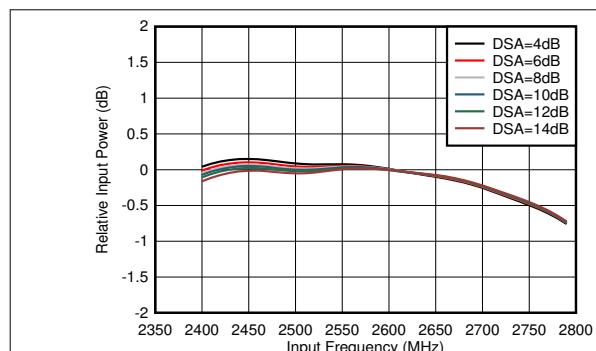


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-347. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

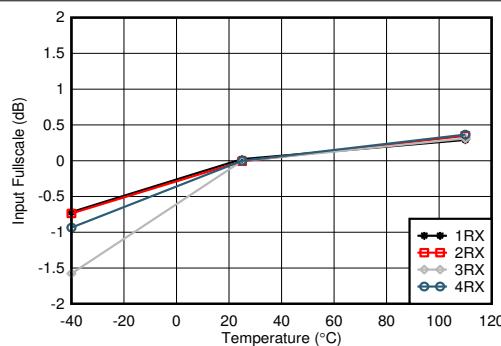
#### 4.12.10 RX Typical Characteristics at 2.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



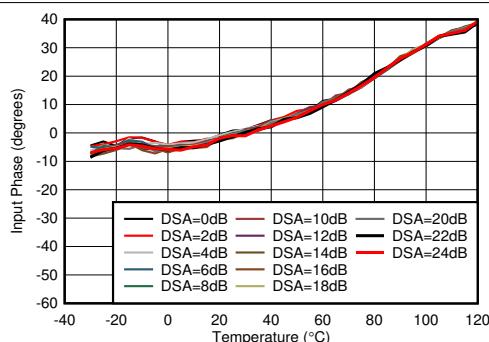
With matching, normalized to power at 2.6 GHz for each DSA setting

Figure 4-348. RX Inband Gain Flatness,  $f_{\text{IN}} = 2600 \text{ MHz}$



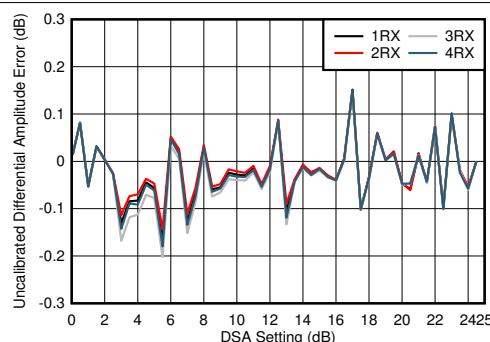
With 2.6 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

Figure 4-349. RX Input Fullscale vs Temperature and Channel at 2.6 GHz



With 2.6 GHz matching, normalized to phase at  $25^\circ\text{C}$

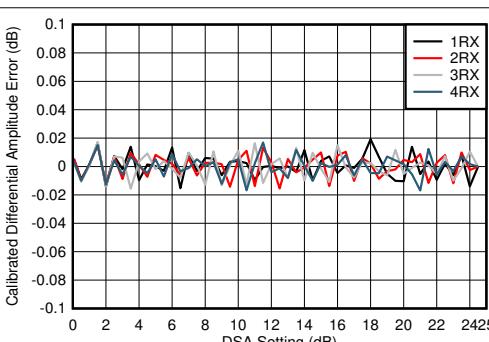
Figure 4-350. RX Input Phase vs Temperature and DSA at  $f_{\text{OUT}} = 2.6 \text{ GHz}$



With 2.6 GHz matching

$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

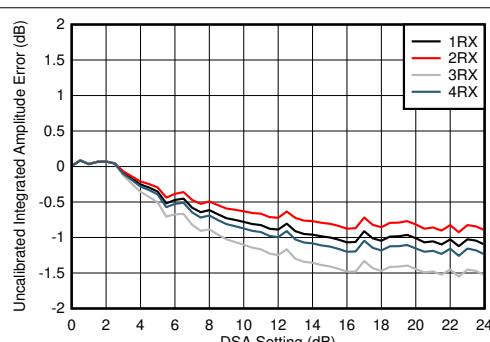
Figure 4-351. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 2.6 GHz



With 2.6 GHz matching

$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

Figure 4-352. RX Calibrated Differential Amplitude Error vs DSA Setting at 2.6 GHz



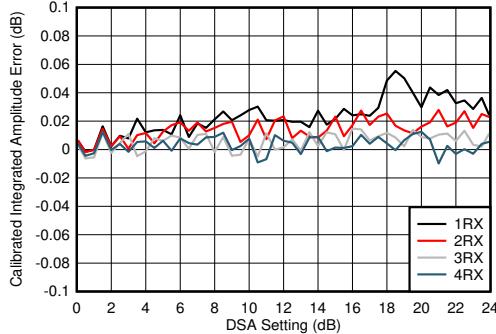
With 2.6 GHz matching

$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

Figure 4-353. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz

#### 4.12.10 RX Typical Characteristics at 2.6 GHz (continued)

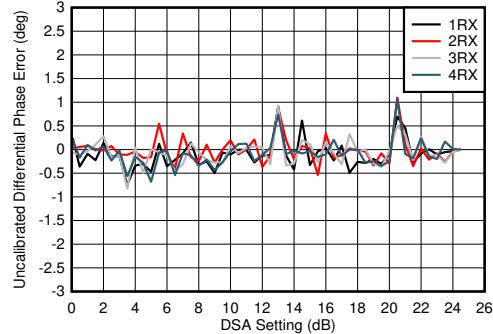
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



With 2.6 GHz matching

$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

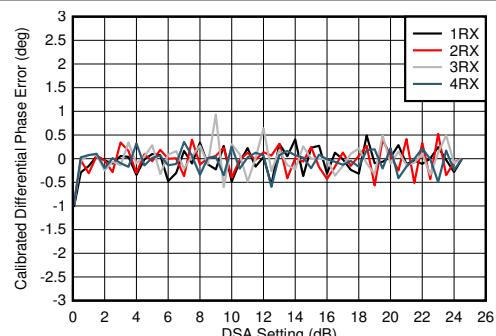
**Figure 4-354. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz**



With 2.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

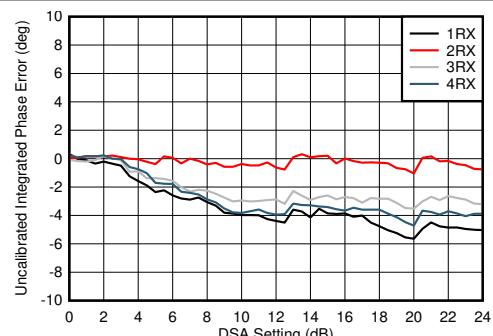
**Figure 4-355. RX Uncalibrated Differential Phase Error vs DSA Setting at 2.6 GHz**



With 2.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

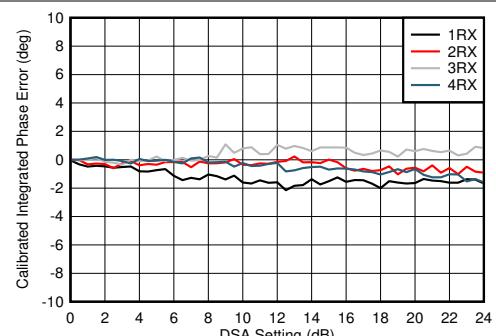
**Figure 4-356. RX Calibrated Differential Phase Error vs DSA Setting at 2.6 GHz**



With 2.6 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

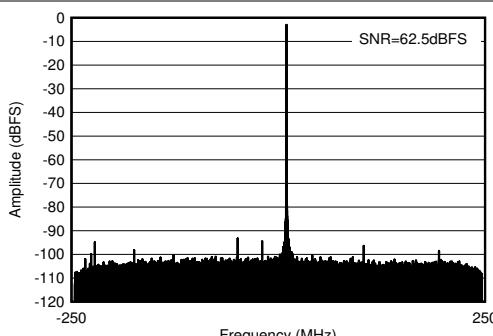
**Figure 4-357. RX Uncalibrated Integrated Phase Error vs DSA Setting at 2.6 GHz**



With 2.6 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 4-358. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz**

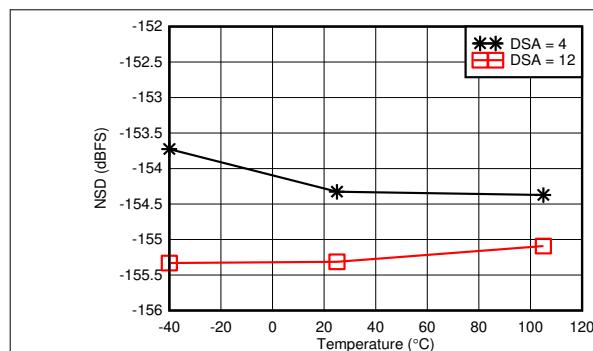


With 2.6 GHz matching,  $f_{\text{IN}} = 2610 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$

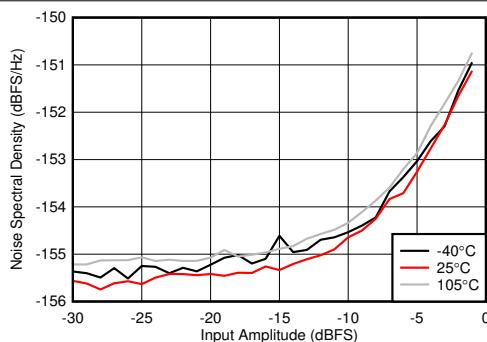
**Figure 4-359. RX Output FFT at 2.6 GHz**

#### 4.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



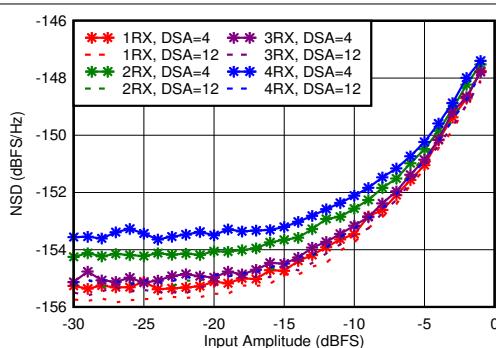
With 2.6 GHz matching, 12.5-MHz offset from tone



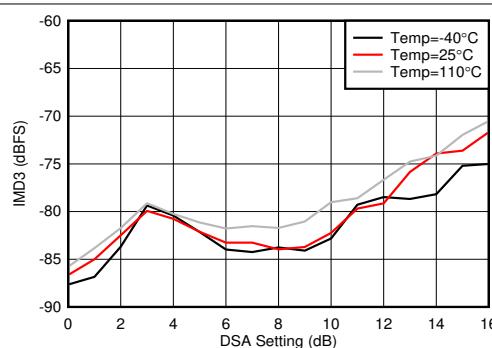
With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 4-360. RX Noise Spectral Density vs Temperature at 2.6 GHz**

**Figure 4-361. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz**



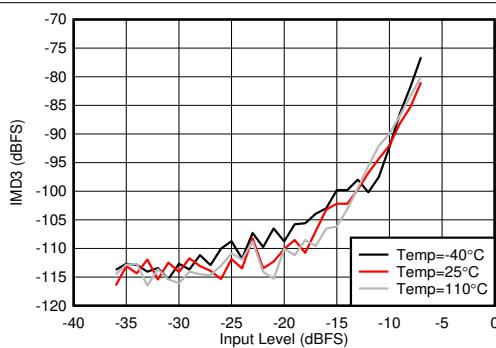
With 2.6 GHz matching, 12.5-MHz offset from tone



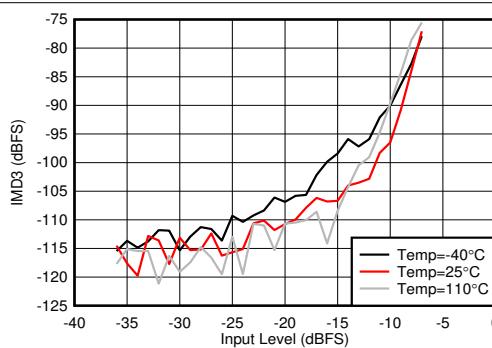
With 2.6 GHz matching, each tone -7 dBFS, tone spacing = 20 MHz

**Figure 4-362. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz**

**Figure 4-363. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz**



With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB



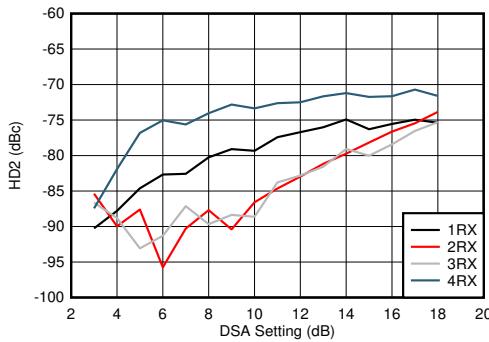
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 4-364. RX IMD3 vs Input Level and Temperature at 2.6 GHz**

**Figure 4-365. RX IMD3 vs Input Level and Temperature at 2.6 GHz**

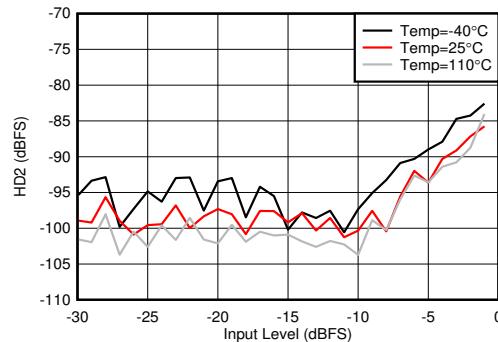
#### 4.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



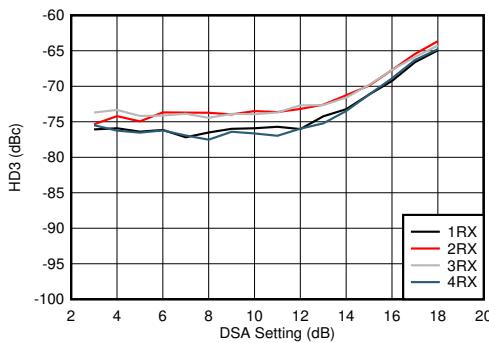
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-366. RX HD2 vs DSA Setting and Channel at 2.6 GHz



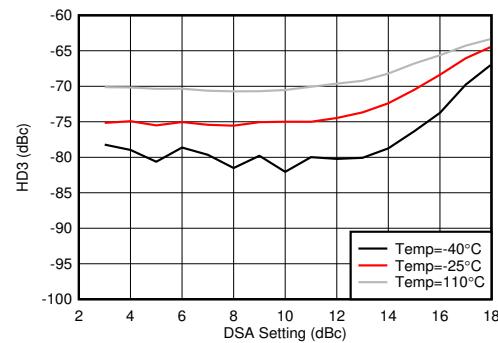
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-367. RX HD2 vs Input Level and Temperature at 2.6 GHz



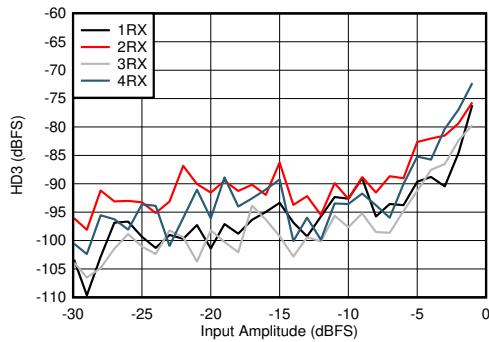
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-368. RX HD3 vs DSA Setting and Channel at 2.6 GHz



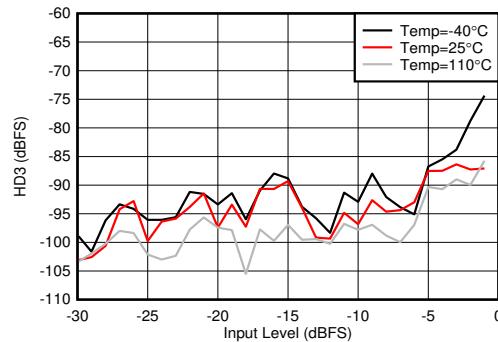
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-369. RX HD3 vs DSA Setting and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-370. RX HD3 vs Input Level and Channel at 2.6 GHz

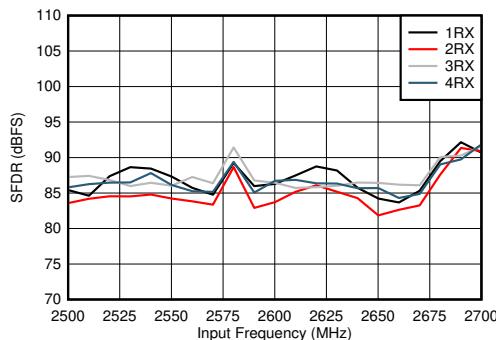


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-371. RX HD3 vs Input Level and Temperature at 2.6 GHz

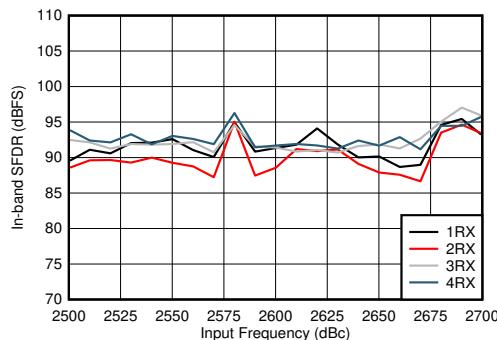
#### 4.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



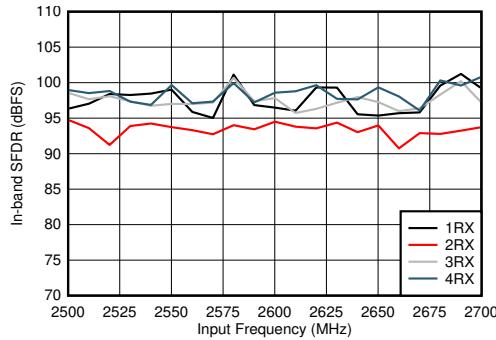
With 2.6 GHz matching

**Figure 4-372. RX In-Band SFDR ( $\pm 200 \text{ MHz}$ ) vs Frequency With  $A_{\text{IN}} = -1 \text{ dBFS}$  at 2.6 GHz**



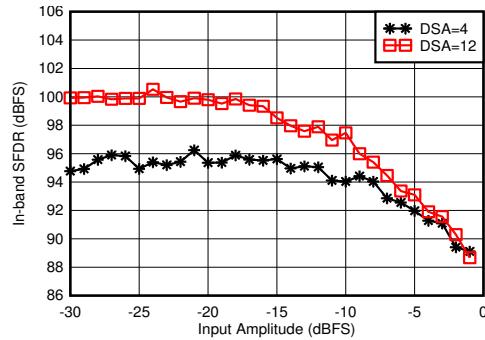
With 2.6 GHz matching

**Figure 4-373. RX In-Band SFDR ( $\pm 200 \text{ MHz}$ ) vs Frequency With  $A_{\text{IN}} = -6 \text{ dBFS}$  at 2.6 GHz**



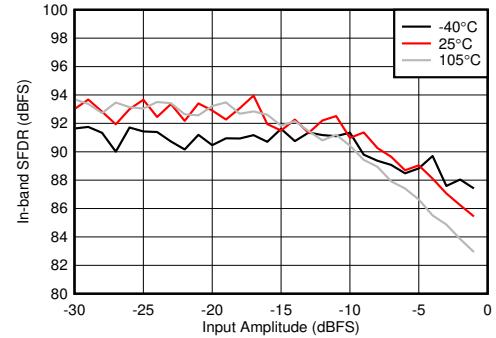
With 2.6 GHz matching

**Figure 4-374. RX In-Band SFDR ( $\pm 200 \text{ MHz}$ ) vs Frequency With  $A_{\text{IN}} = -12 \text{ dBFS}$  at 2.6 GHz**



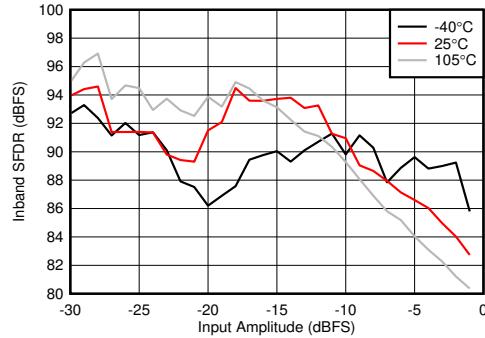
With 2.6 GHz matching

**Figure 4-375. RX In-Band SFDR ( $\pm 200 \text{ MHz}$ ) vs Input Amplitude at 2.6 GHz**



With 2.6 GHz matching

**Figure 4-376. RX In-Band SFDR ( $\pm 200 \text{ MHz}$ ) vs Input Amplitude and Temperature at 2.6 GHz**

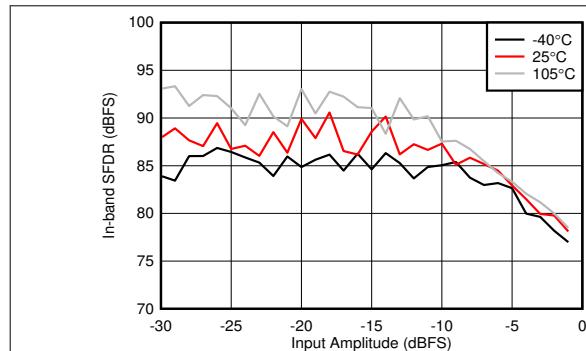


With 2.6 GHz matching, decimate by 8, DSA Setting = 12 dB

**Figure 4-377. RX Inband SFDR ( $\pm 150 \text{ MHz}$ ) vs Input Amplitude and Temperature at 2.6 GHz**

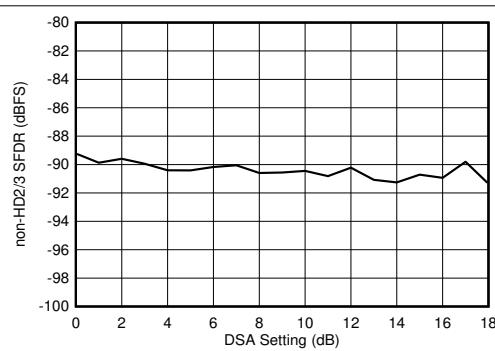
#### 4.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



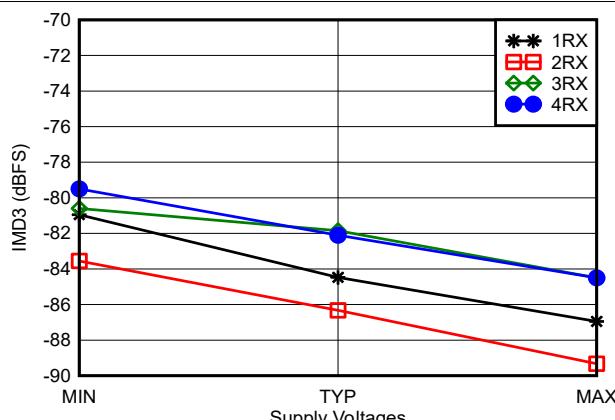
With 2.6 GHz matching, decimate by 4

**Figure 4-378. RX In-Band SFDR ( $\pm 300$  MHz) vs Input Amplitude and Temperature at 2.6 GHz**



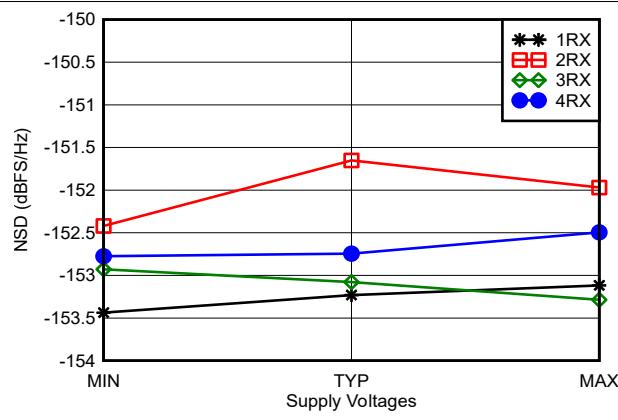
With 2.6 GHz matching

**Figure 4-379. RX Non-HD2/3 vs DSA Setting at 2.6 GHz**



With 2.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 4-380. RX IMD3 vs Supply and Channel at 2.6 GHz**

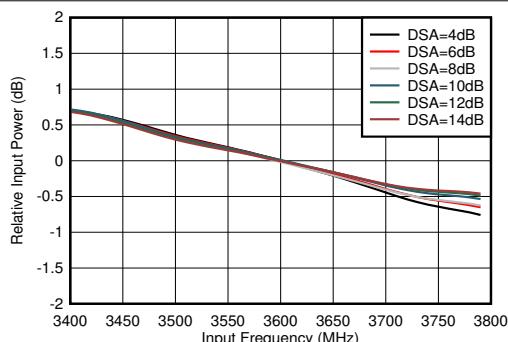


With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 4-381. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz**

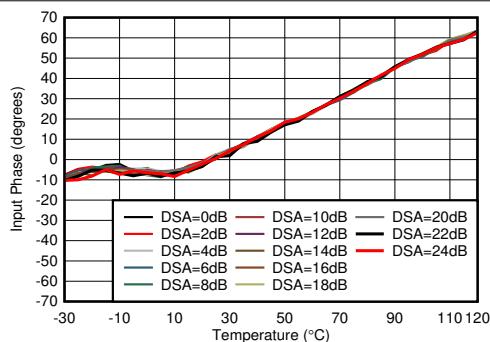
#### 4.12.11 RX Typical Characteristics at 3.5 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



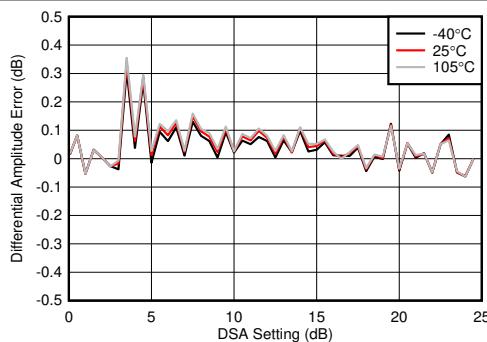
With 3.6 GHz matching, normalized to 3.6 GHz

**Figure 4-382. RX In-Band Gain Flatness,  $f_{\text{IN}} = 3600 \text{ MHz}$**



With 3.6 GHz matching, normalized to phase at  $25^\circ\text{C}$

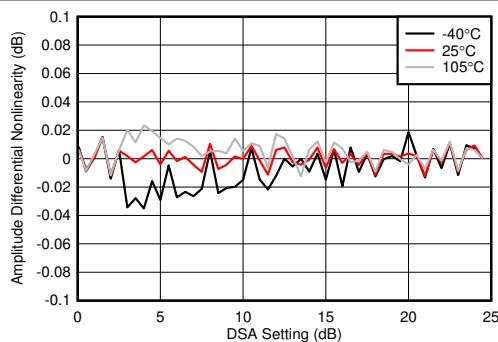
**Figure 4-383. RX Input Phase vs Temperature at 3.6 GHz**



With 3.6 GHz matching

Differential Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

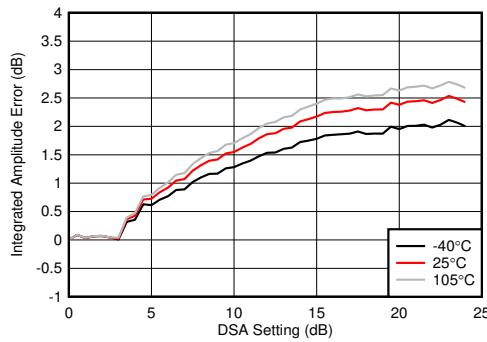
**Figure 4-384. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching

Differential Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

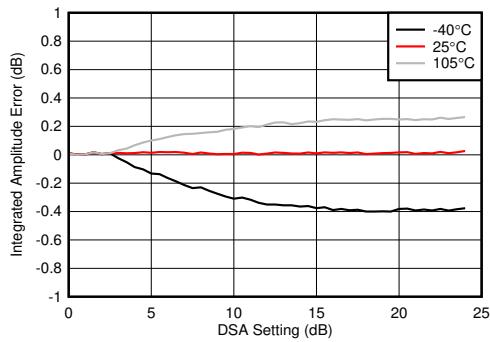
**Figure 4-385. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching

Integrated Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-386. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz**



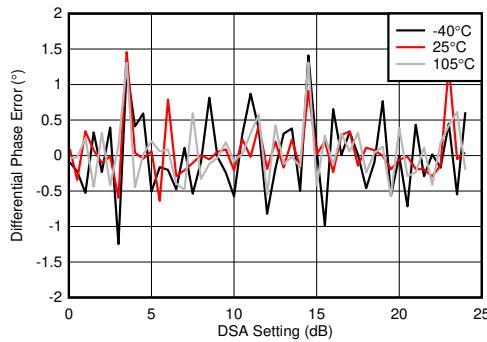
With 3.6 GHz matching

Integrated Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-387. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz**

#### 4.12.11 RX Typical Characteristics at 3.5 GHz (continued)

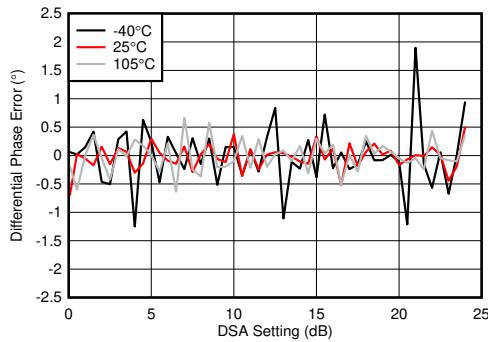
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

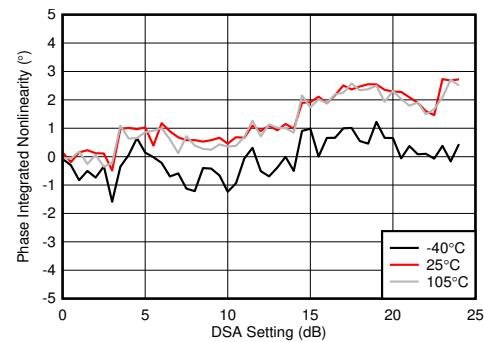
**Figure 4-388. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

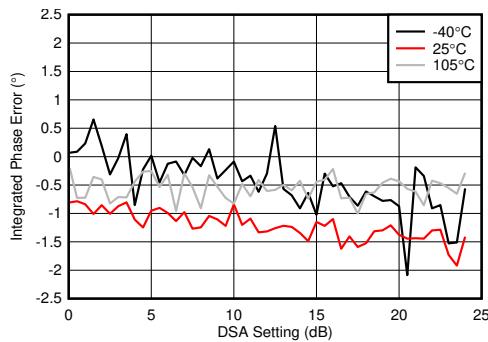
**Figure 4-389. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

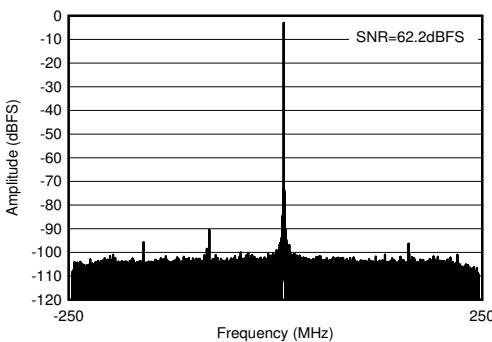
**Figure 4-390. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching

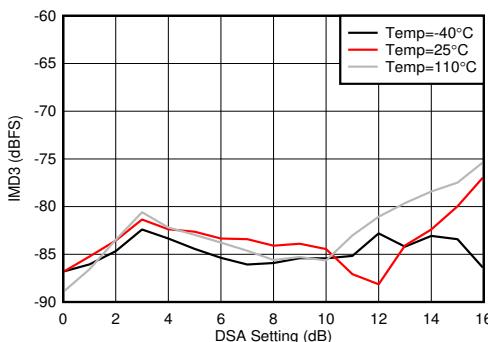
$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 4-391. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching,  $f_{\text{IN}} = 3610$  MHz,  $A_{\text{IN}} = -3$  dBFS

**Figure 4-392. RX Output FFT at 3.6 GHz**

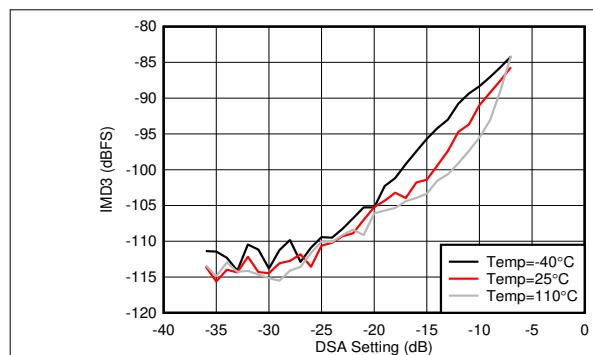


With 3.5 GHz matching, each tone at  $-7$  dBFS, 20-MHz tone spacing

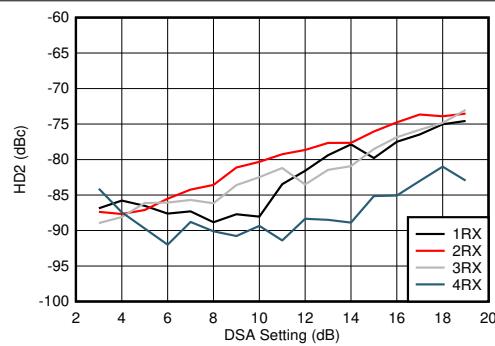
**Figure 4-393. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz**

#### 4.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.

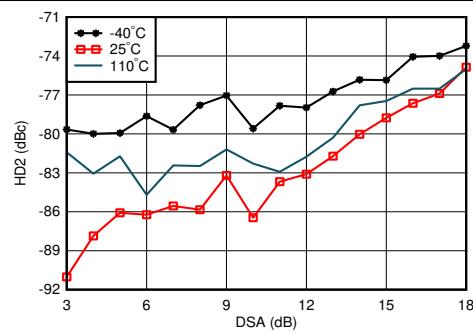


With 3.5 GHz matching, 20-MHz tone spacing



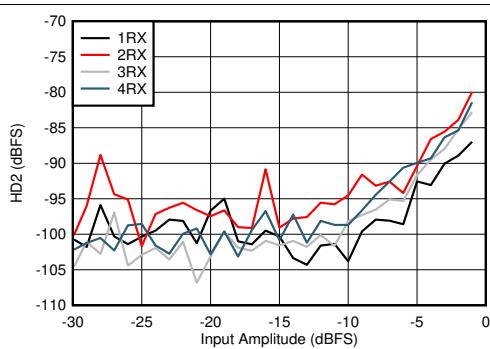
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-394. RX IMD3 vs Input Level and Temperature at 3.6 GHz**



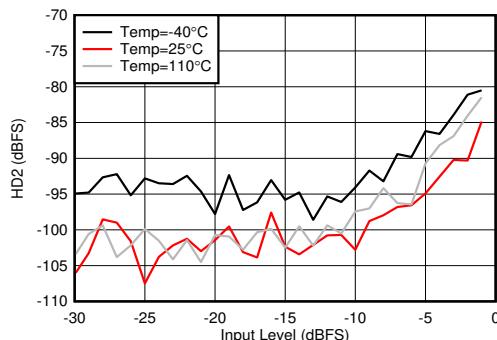
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-396. RX HD2 vs DSA Setting and Temperature at 3.6 GHz**



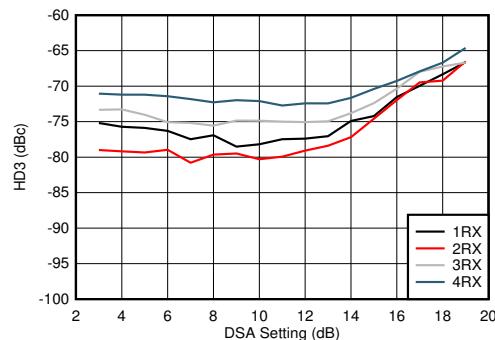
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-397. RX HD2 vs Input Level and Channel at 3.6 GHz**



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-398. RX HD2 vs Input Level and Temperature at 3.6 GHz**

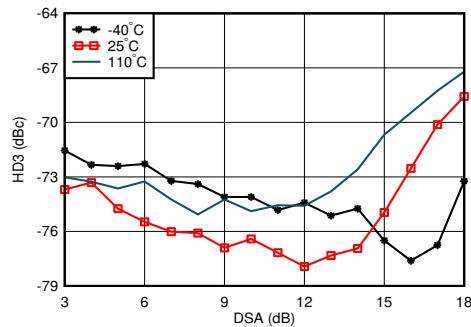


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-399. RX HD3 vs DSA Setting and Channel at 3.6 GHz**

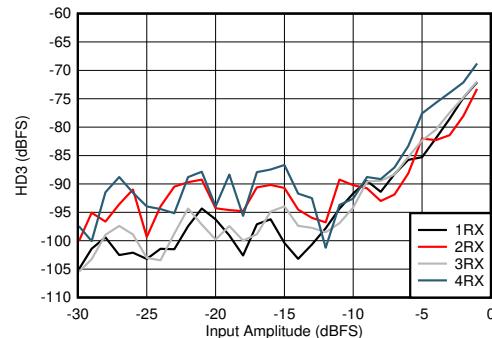
#### 4.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



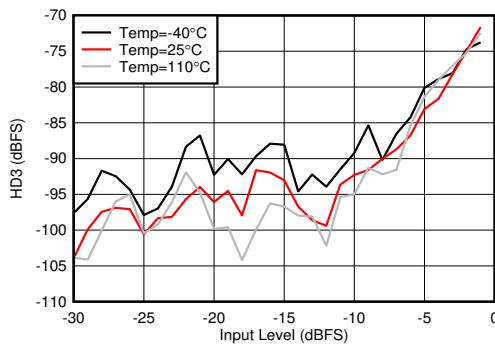
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-400. RX HD3 vs DSA Setting and Temperature at 3.6 GHz**



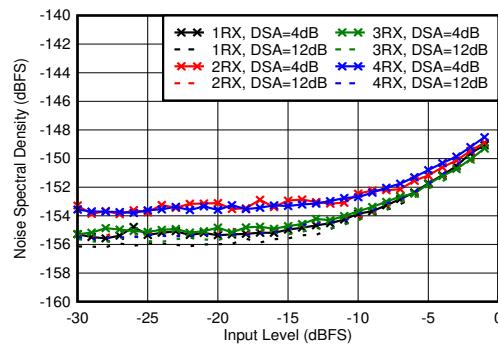
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-401. RX HD3 vs Input Level and Channel at 3.6 GHz**



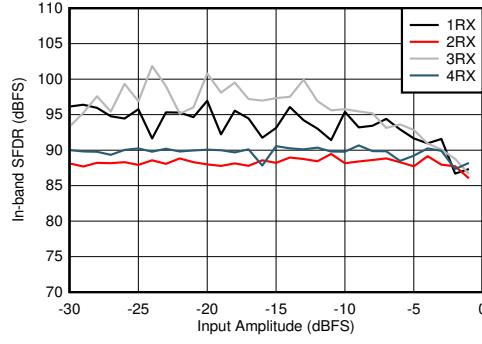
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-402. RX HD3 vs Input Level and Temperature at 3.6 GHz**



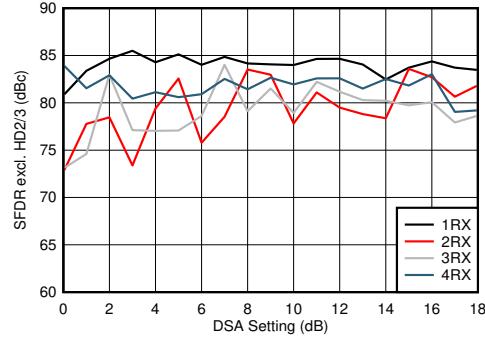
With 3.5 GHz matching, 12.5-MHz offset from tone

**Figure 4-403. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz**



With 3.5 GHz matching

**Figure 4-404. RX In-Band SFDR (±200 MHz) vs Input Level and Channel at 3.6 GHz**

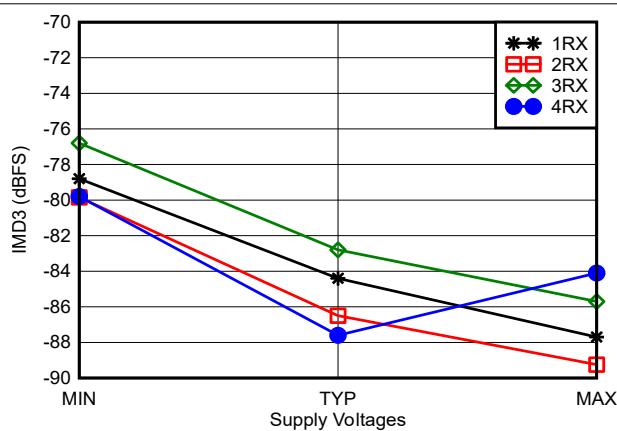


With 3.5 GHz matching

**Figure 4-405. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz**

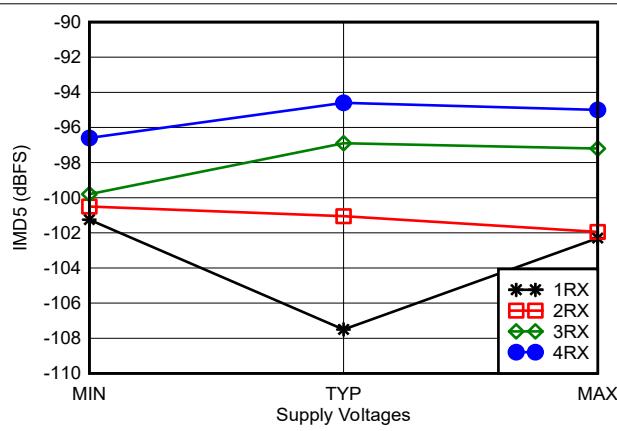
#### 4.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



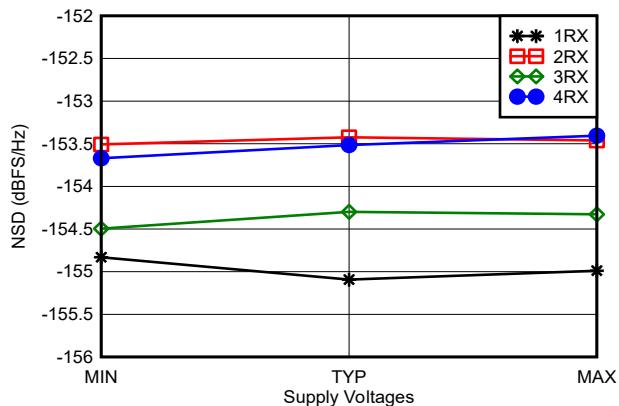
With 3.6 GHz matching,  $-7$  dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 4-406. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz**



With 3.6 GHz matching,  $-7$  dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 4-407. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz**

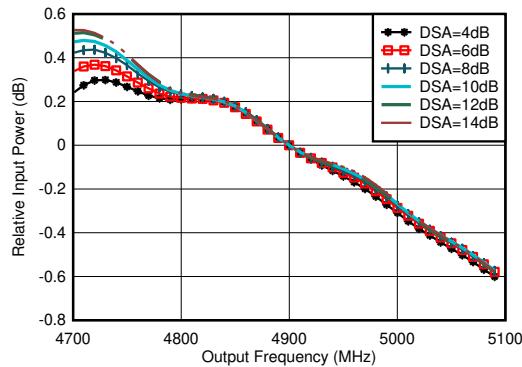


With 3.6 GHz matching, tone at  $-20$  dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 4-408. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz**

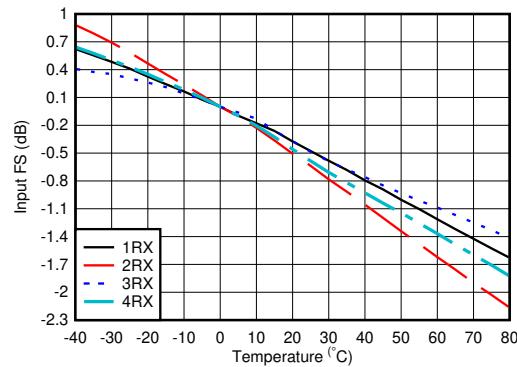
#### 4.12.12 RX Typical Characteristics at 4.9 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



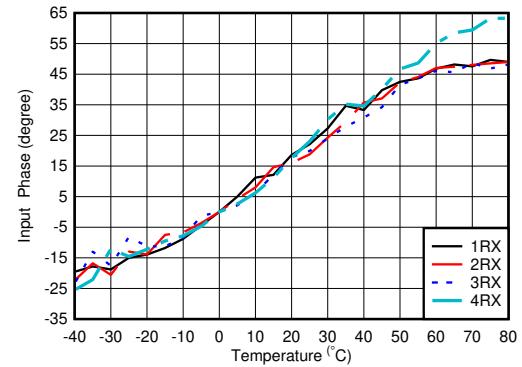
With matching, normalized to power at 4.9GHz for each DSA setting

Figure 4-409. RX Inband Gain Flatness,  $f_{\text{IN}} = 4900$  MHz



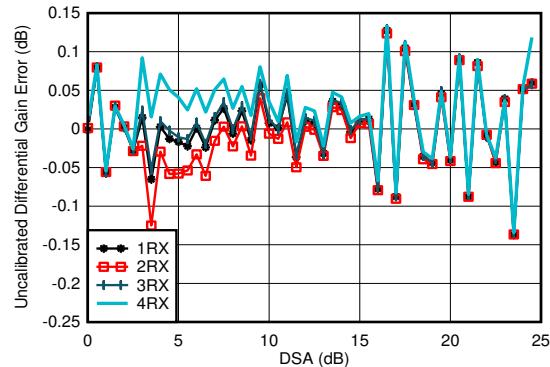
With 4.9 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

Figure 4-410. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at  $25^\circ\text{C}$

Figure 4-411. RX Input Phase vs Temperature and DSA at  $f_{\text{OUT}} = 4.9$  GHz

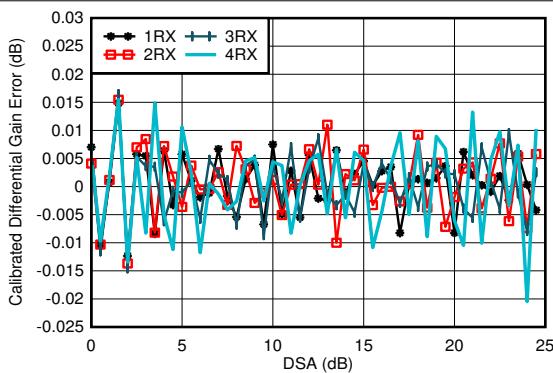


With 4.9 GHz matching  
 $\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 4-412. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz

#### 4.12.12 RX Typical Characteristics at 4.9 GHz (continued)

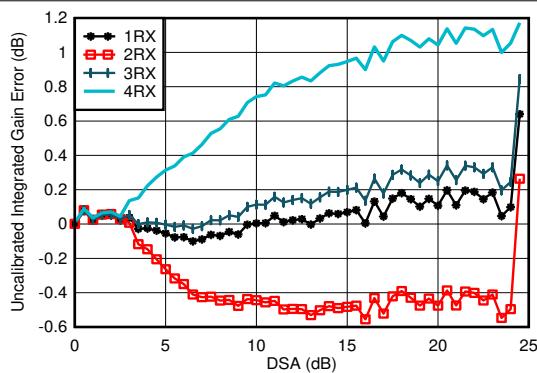
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



With 4.9 GHz matching

$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

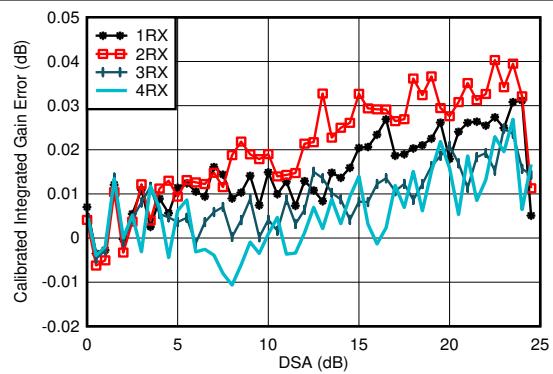
**Figure 4-413. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching

$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

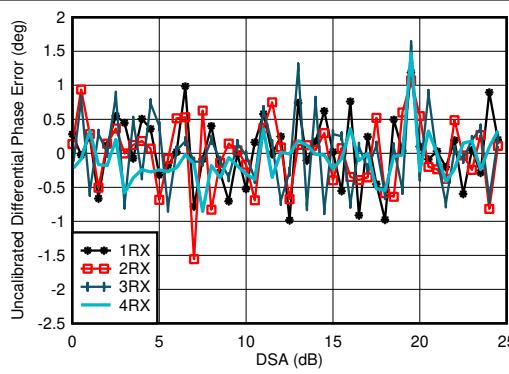
**Figure 4-414. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching

$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

**Figure 4-415. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz**



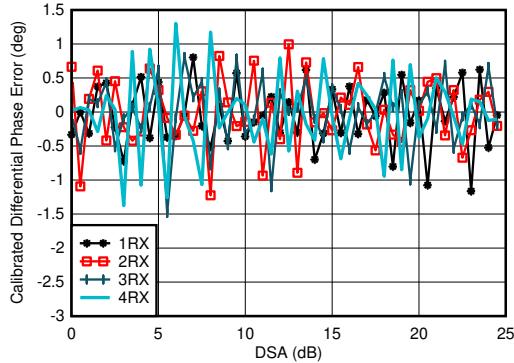
With 4.9 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

**Figure 4-416. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz**

#### 4.12.12 RX Typical Characteristics at 4.9 GHz (continued)

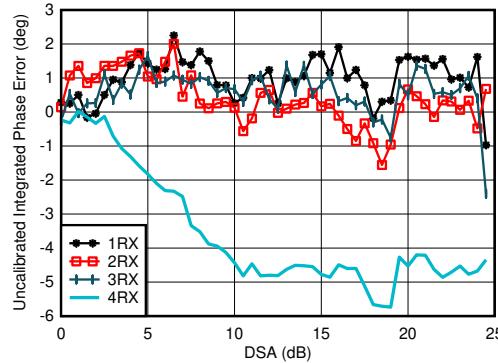
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



With 4.9 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

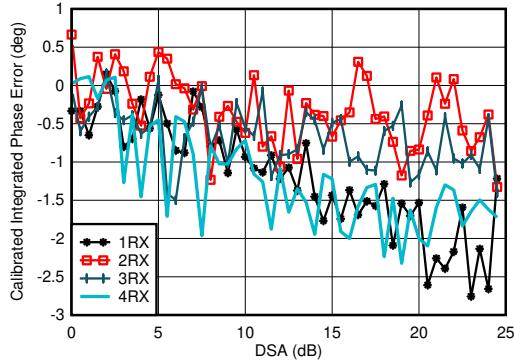
**Figure 4-417. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

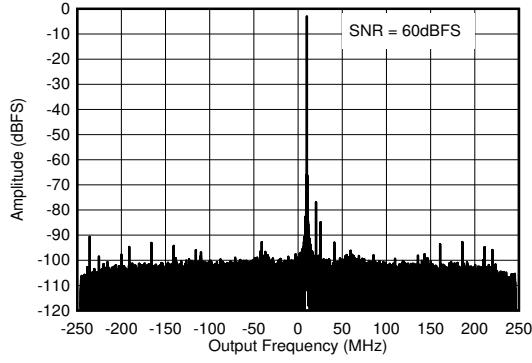
**Figure 4-418. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 4-419. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz**

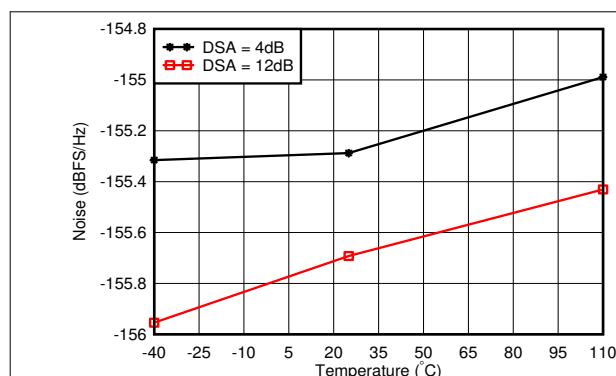


With 4.9 GHz matching,  $f_{\text{IN}} = 4910$  MHz,  $A_{\text{IN}} = -3$  dBFS

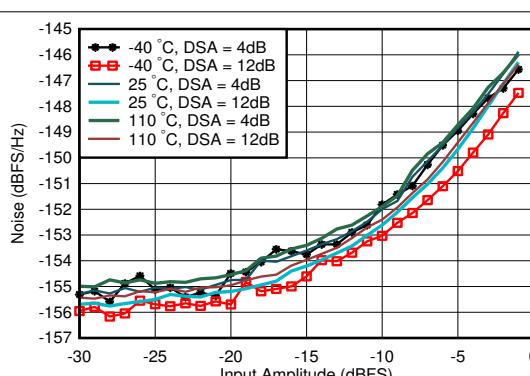
**Figure 4-420. RX Output FFT at 4.9 GHz**

#### 4.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



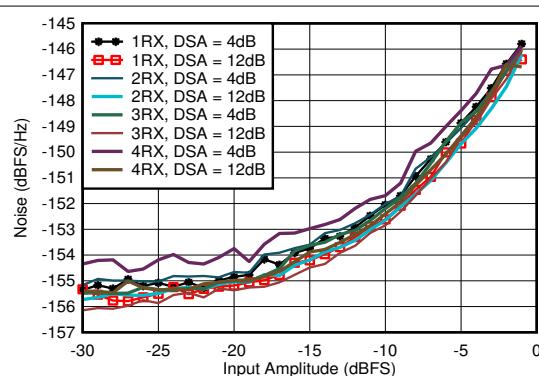
With 4.9 GHz matching, 12.5-MHz offset from tone



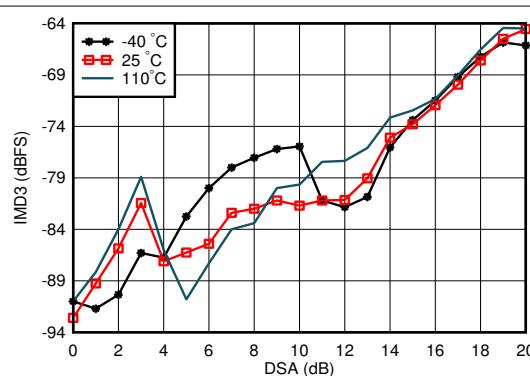
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 4-421. RX Noise Spectral Density vs Temperature at 4.9 GHz**

**Figure 4-422. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz**



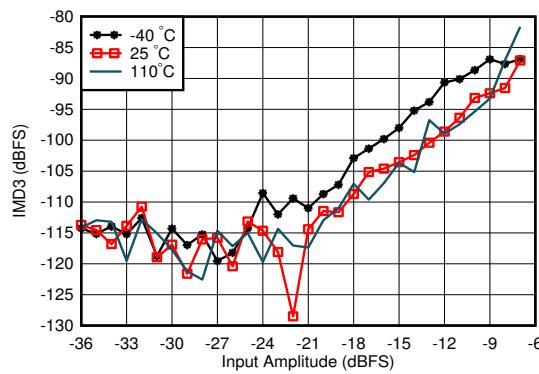
With 4.9 GHz matching, 12.5-MHz offset from tone



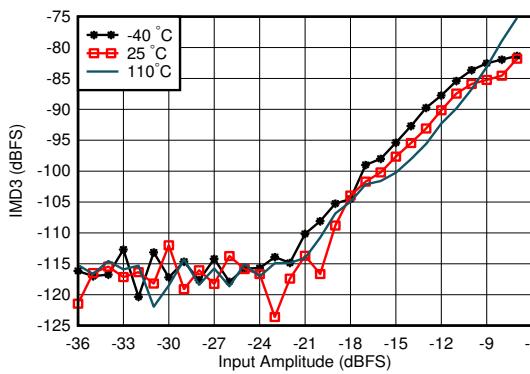
With 4.9 GHz matching, each tone -7 dBFS, tone spacing = 20 MHz

**Figure 4-423. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz**

**Figure 4-424. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz**



With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB



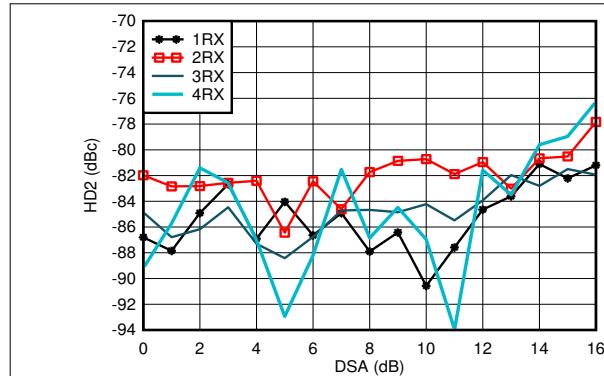
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 4-425. RX IMD3 vs Input Level and Temperature at 4.9 GHz**

**Figure 4-426. RX IMD3 vs Input Level and Temperature at 4.9 GHz**

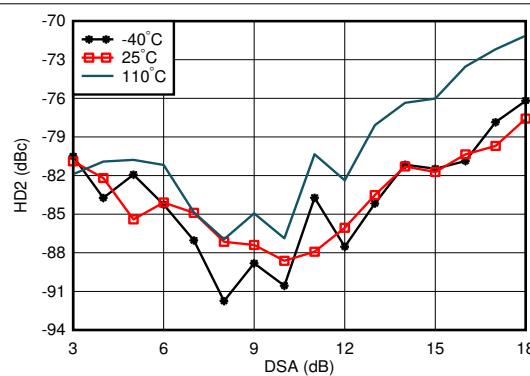
#### 4.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



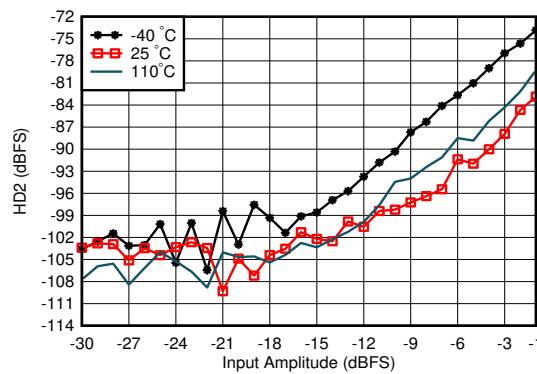
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-427. RX HD2 vs DSA Setting and Channel at 4.9 GHz



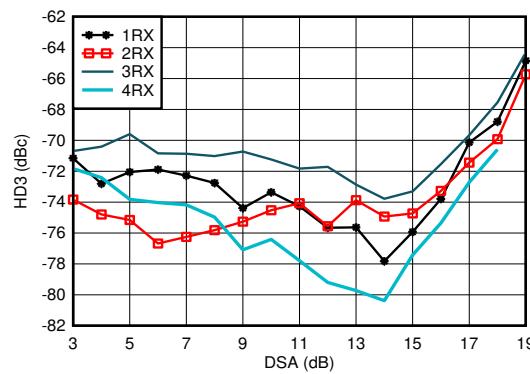
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-428. RX HD2 vs DSA and Temperature at 4.9 GHz



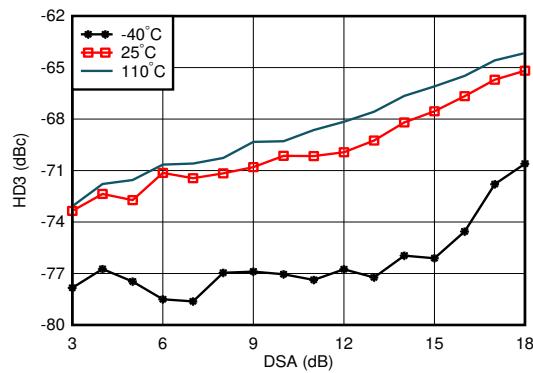
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-429. RX HD2 vs Input Level and Temperature at 4.9 GHz



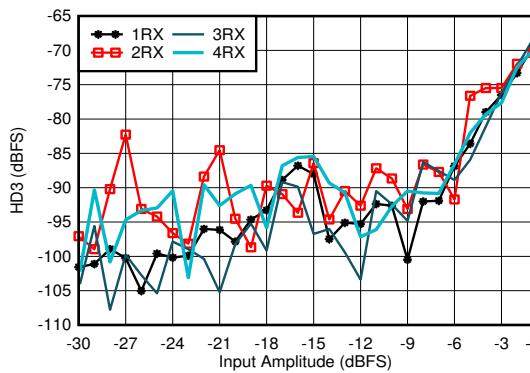
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-430. RX HD3 vs DSA Setting and Channel at 4.9 GHz



With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-431. RX HD3 vs DSA Setting and Temperature at 4.9 GHz

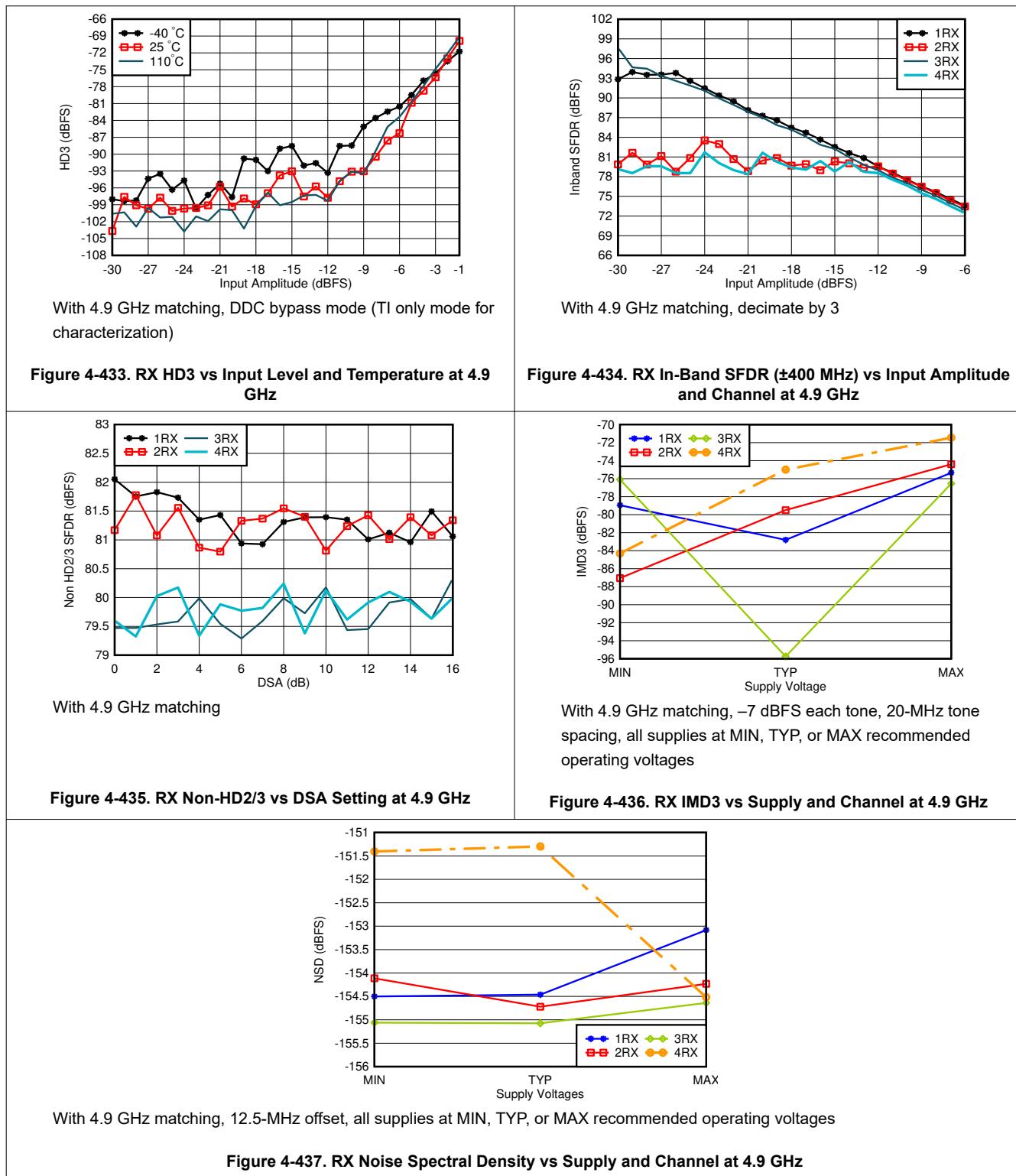


With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-432. RX HD3 vs Input Level and Channel at 4.9 GHz

#### 4.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



#### 4.12.13 RX Typical Characteristics at 8.1GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.

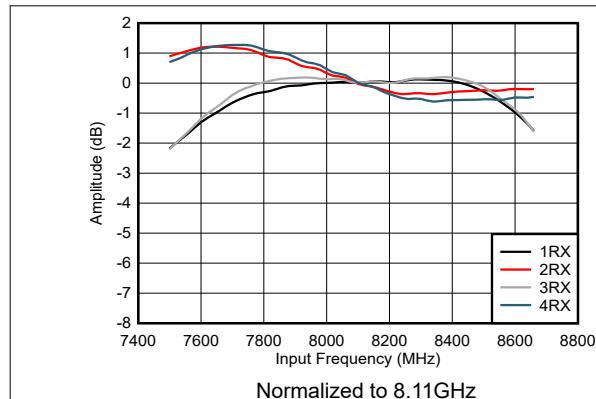


Figure 4-438. RX Amplitude vs Frequency and Channel

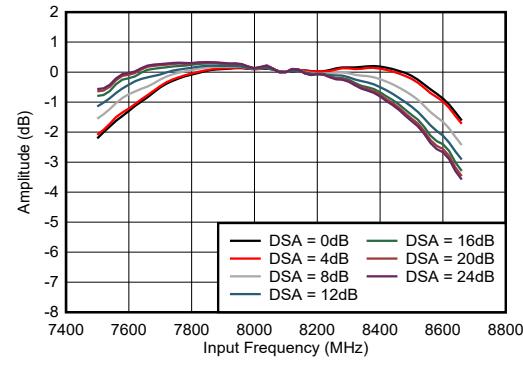


Figure 4-439. RX Amplitude vs Frequency and DSA Setting

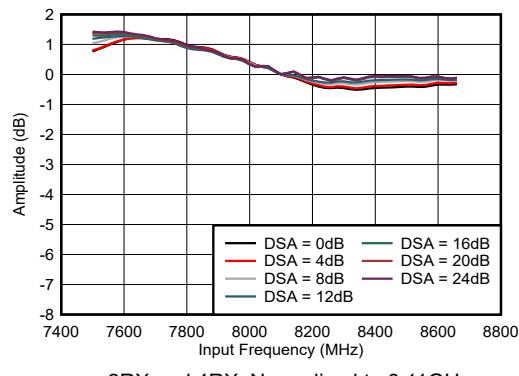


Figure 4-440. RX Amplitude vs Frequency and DSA Setting

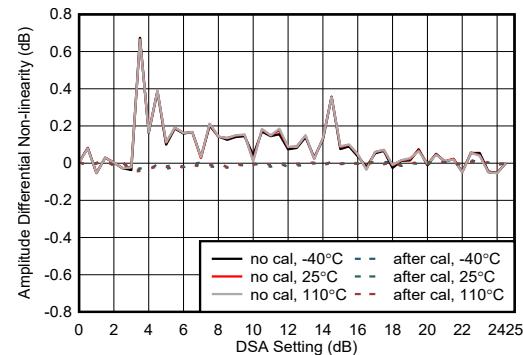


Figure 4-441. RX Amplitude Differential Nonlinearity at 8.11GHz

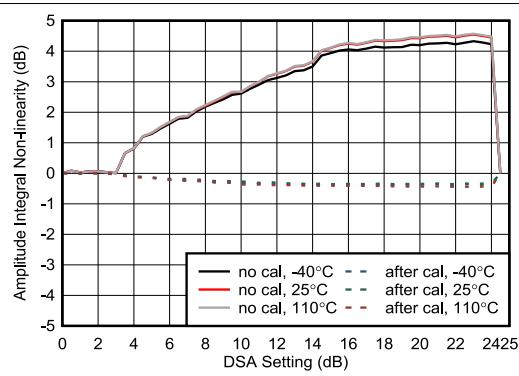


Figure 4-442. RX Amplitude Integrated Nonlinearity at 8.11GHz

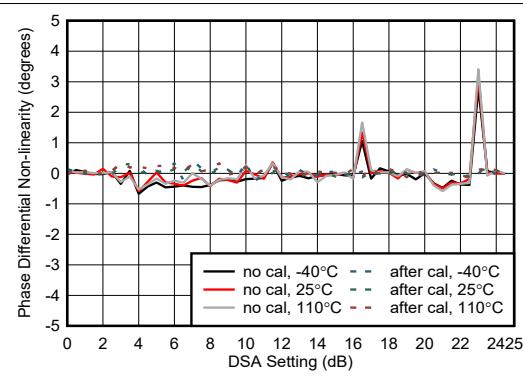


Figure 4-443. RX Phase Differential Nonlinearity at 8.11GHz

#### 4.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.

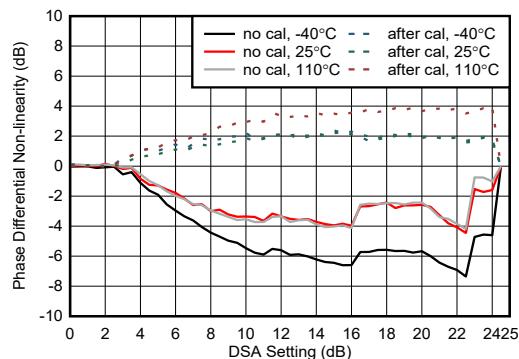


Figure 4-444. RX Phase Differential Nonlinearity at 8.11GHz

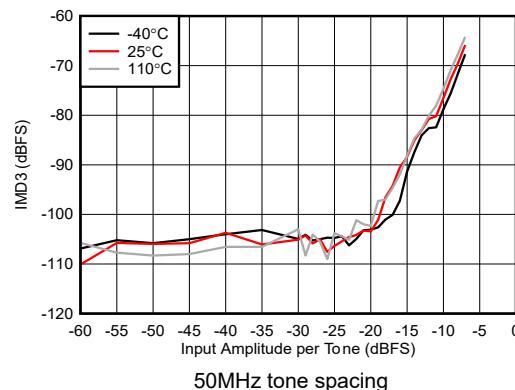


Figure 4-445. RX IMD3 vs Input Amplitude at 8.11GHz

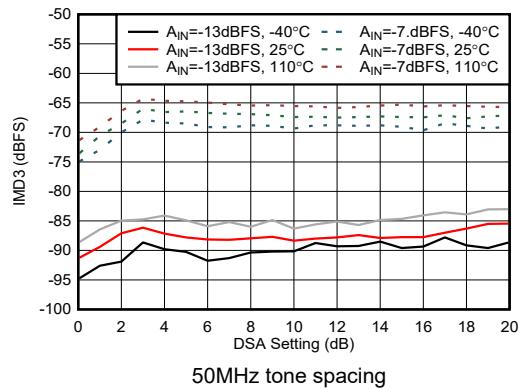


Figure 4-446. RX IMD3 vs DSA Setting at 8.11GHz

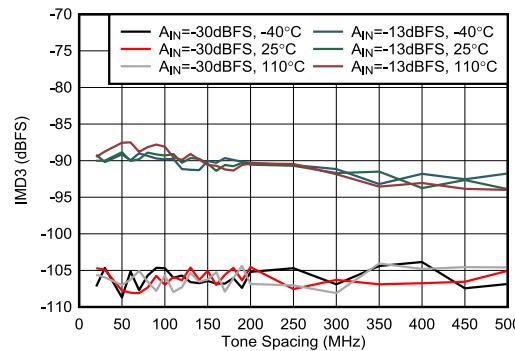


Figure 4-447. RX IMD3 vs Tone Spacing at 8.11GHz

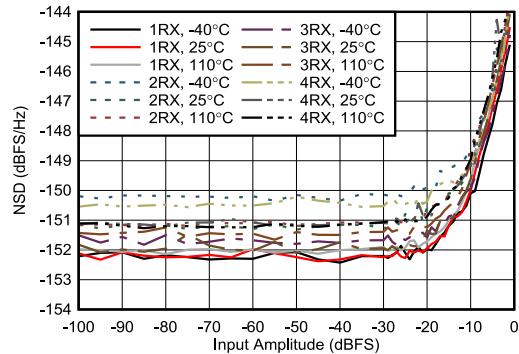


Figure 4-448. RX NSD vs Digital Amplitude at 8.11GHz

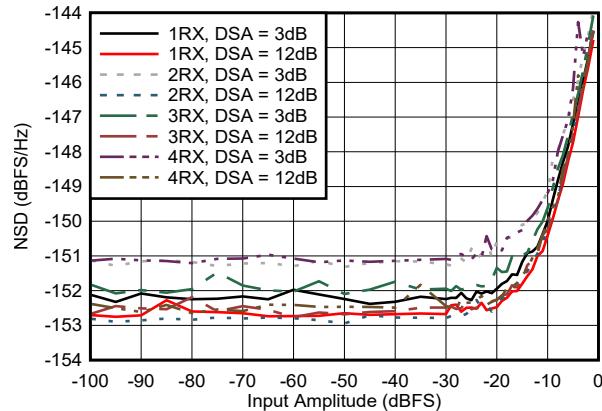


Figure 4-449. RX NSD vs Digital Amplitude at 8.11GHz

#### 4.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.

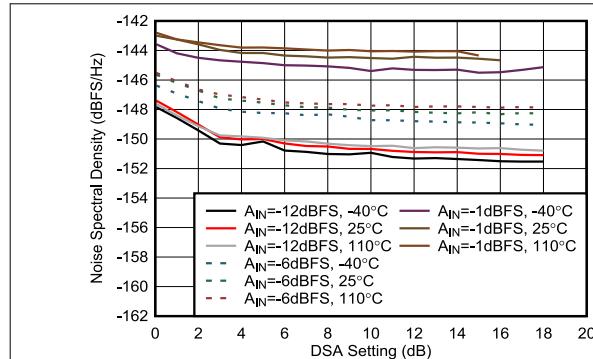


Figure 4-450. RX NSD vs DSA Setting at 8.11GHz

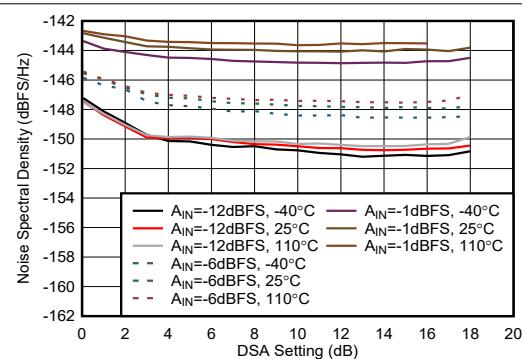


Figure 4-451. RX NSD vs DSA Setting at 8.11GHz

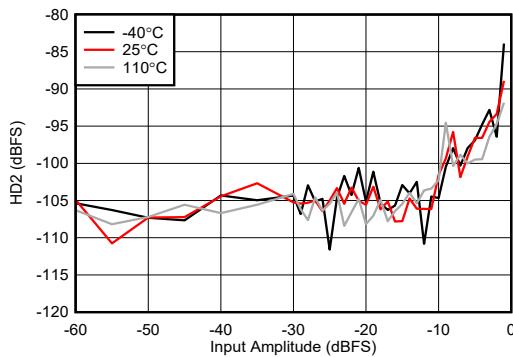


Figure 4-452. RX HD2 vs Digital Amplitude at 8.11GHz

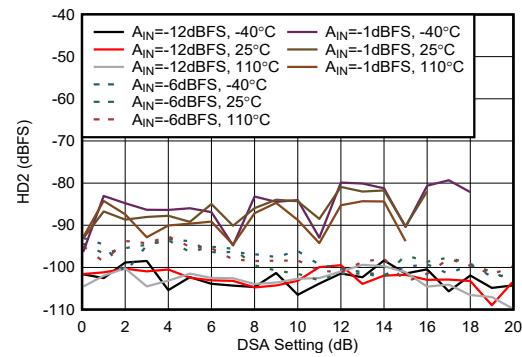


Figure 4-453. RX HD2 vs DSA Setting at 8.11GHz

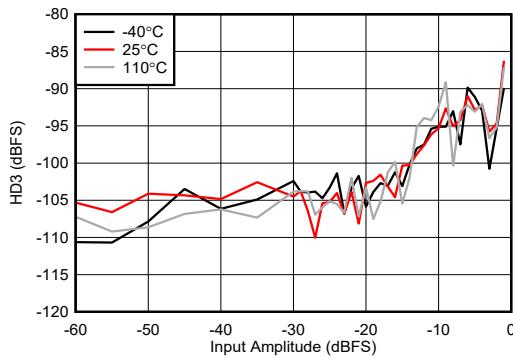


Figure 4-454. RX HD3 vs Digital Amplitude at 8.11GHz

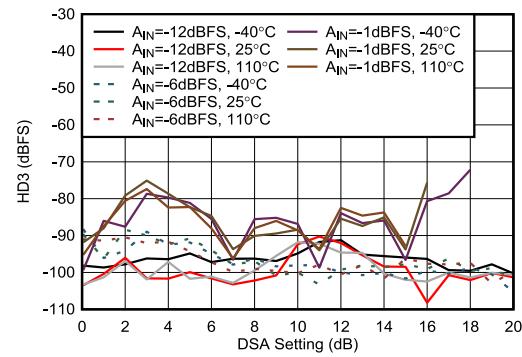


Figure 4-455. RX HD3 vs DSA Setting at 8.11GHz

#### 4.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.

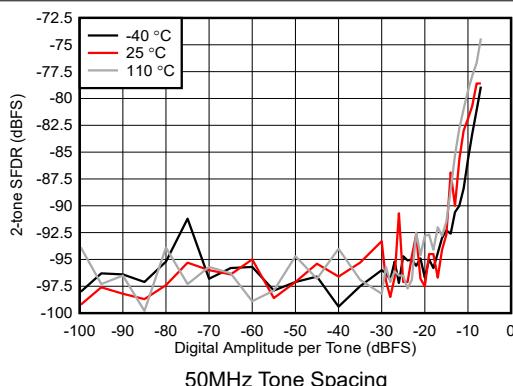


Figure 4-456. RX 2-tone SFDR vs Digital Amplitude at 8.11GHz

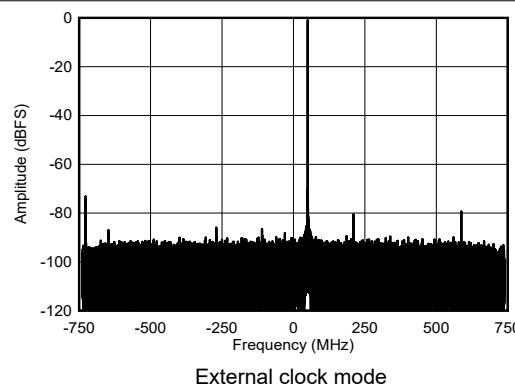


Figure 4-457. RX Single Tone Output FFT at 8.11GHz, -1dBFS

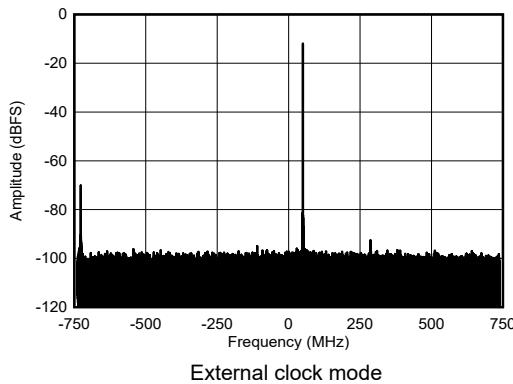


Figure 4-458. RX Single Tone Output FFT at 8.11GHz, -12dBFS

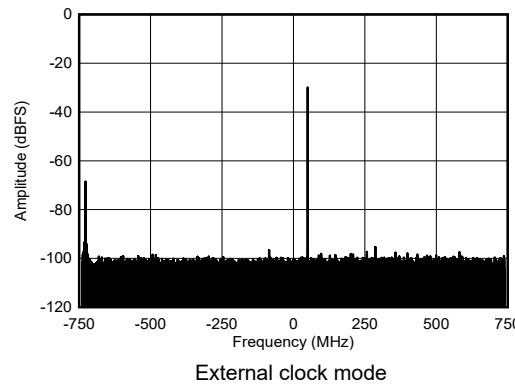


Figure 4-459. RX Single Tone Output FFT at 8.11GHz, -30dBFS

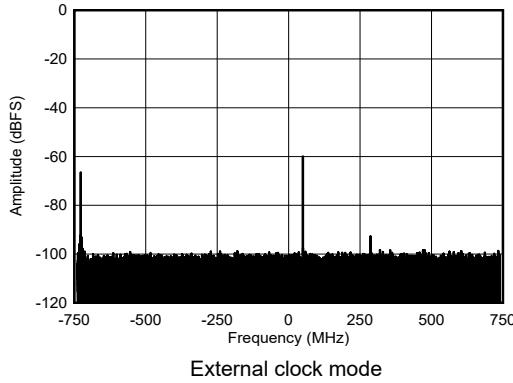


Figure 4-460. RX Single Tone Output FFT at 8.11GHz, -60dBFS

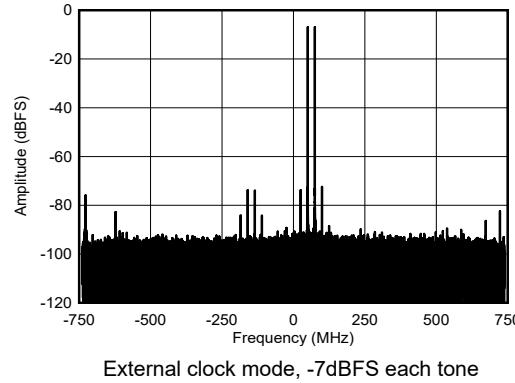
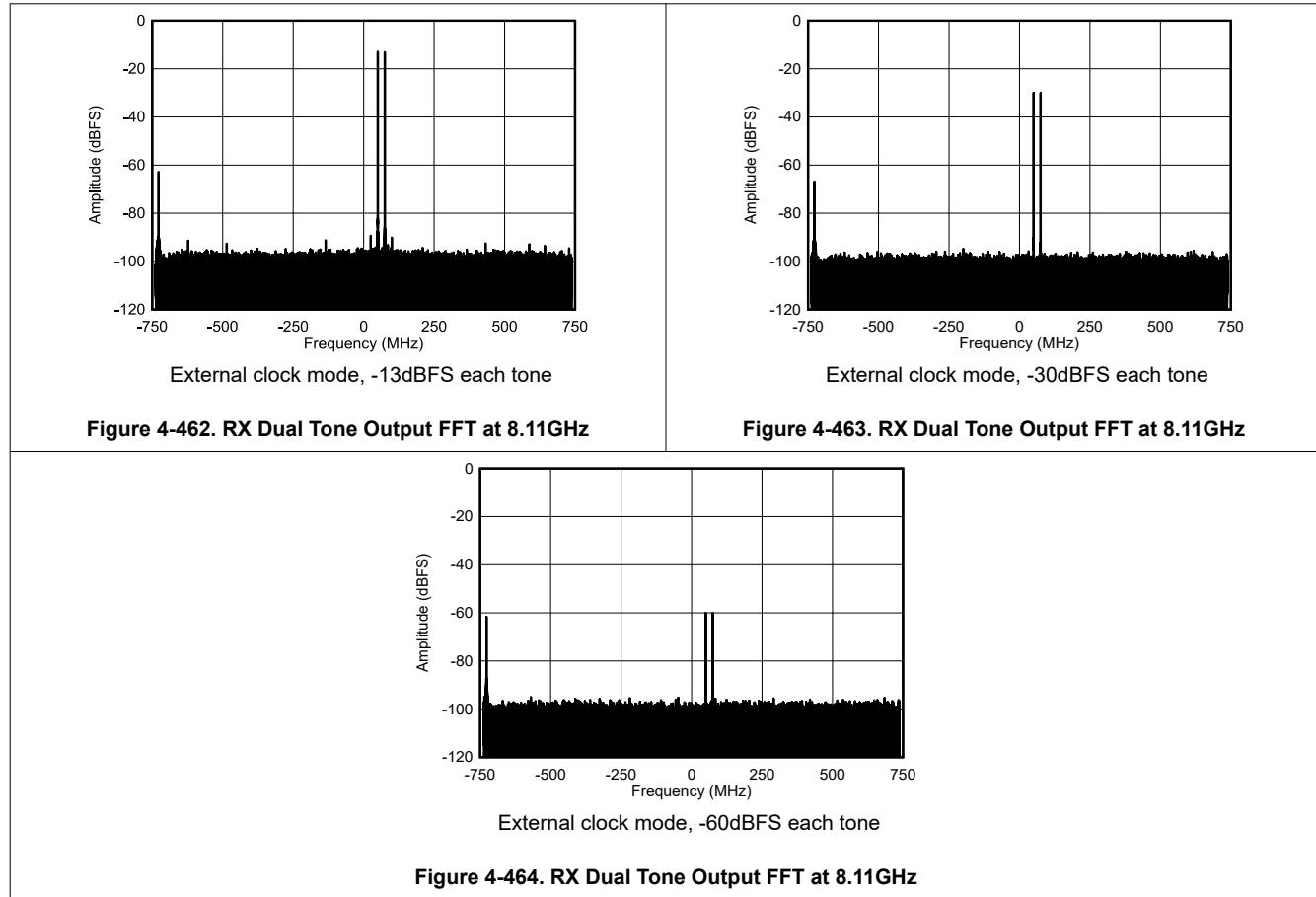


Figure 4-461. RX Dual Tone Output FFT at 8.11GHz

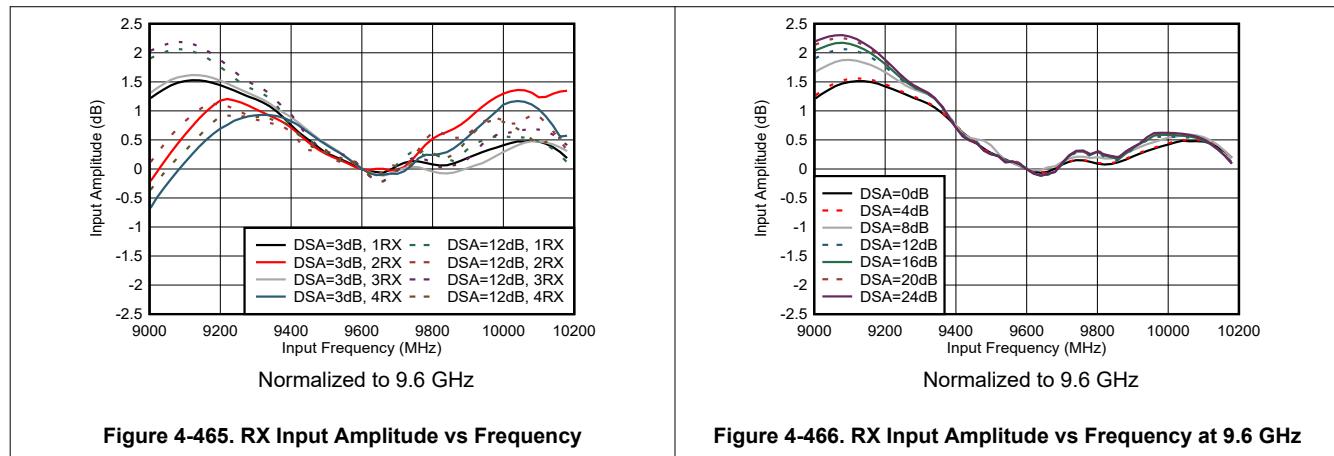
#### 4.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.



#### 4.12.14 RX Typical Characteristics at 9.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.



#### 4.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.

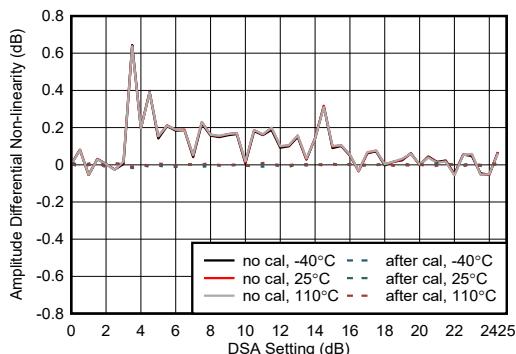


Figure 4-467. RX Amplitude Differential Non-Linearity at 9.6 GHz

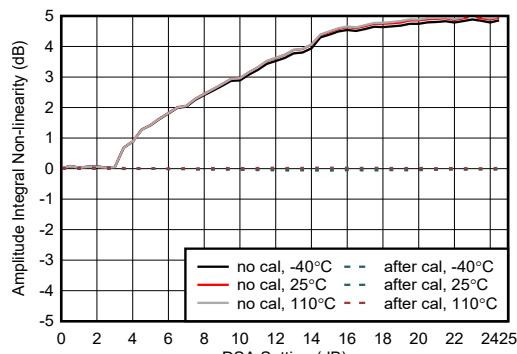


Figure 4-468. RX Amplitude Integrated Non-linearity at 9.6 GHz

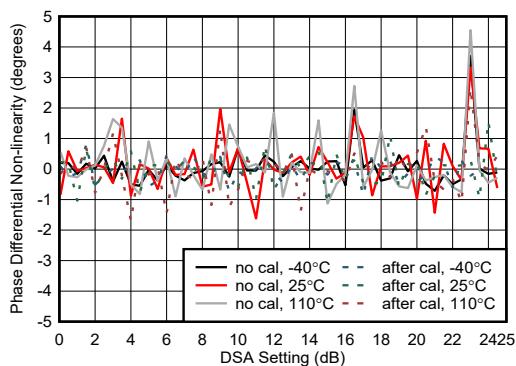


Figure 4-469. RX Phase Differential Non-linearity at 9.6 GHz

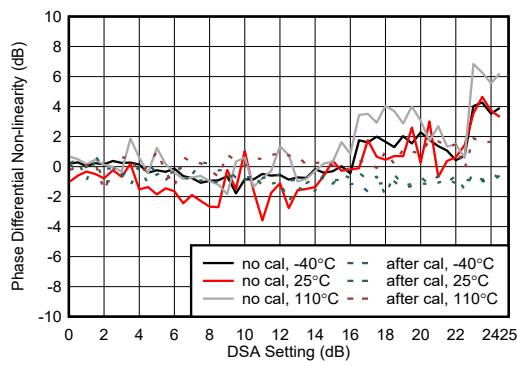


Figure 4-470. RX Phase Integrated Non-linearity at 9.6 GHz

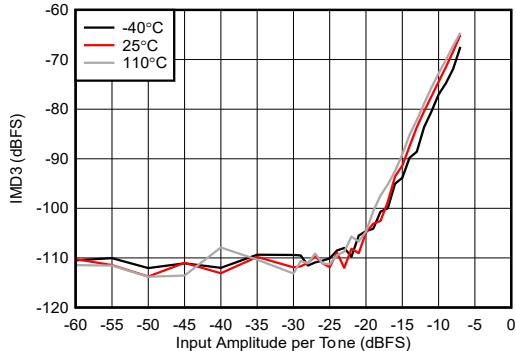


Figure 4-471. RX IMD3 vs Digital Amplitude at 9.6 GHz

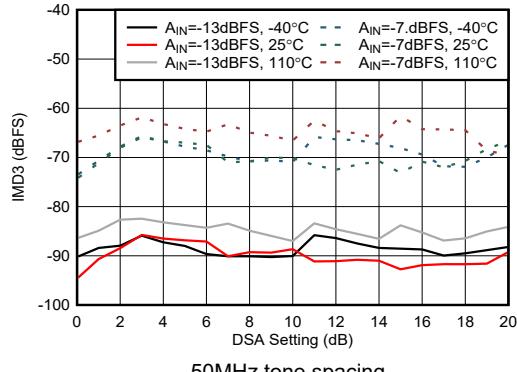


Figure 4-472. RX IMD3 vs DSA Setting at 9.6 GHz

#### 4.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.

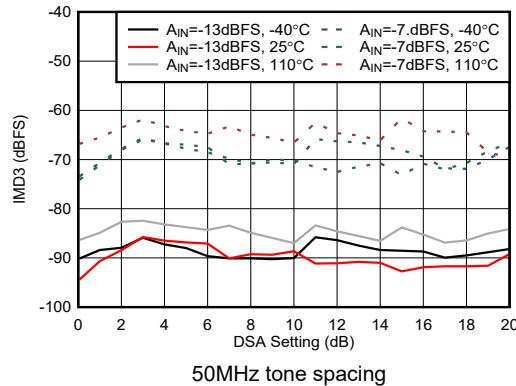


Figure 4-473. RX IMD3 vs DSA Setting at 9.6 GHz

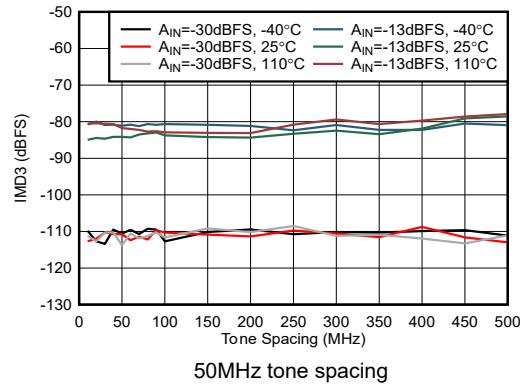


Figure 4-474. RX IMD3 vs Tone Spacing at 9.6 GHz

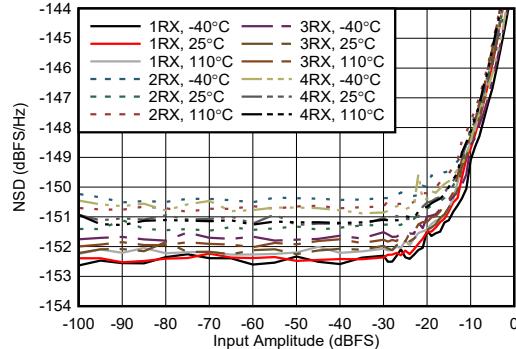


Figure 4-475. RX NSD vs Digital Amplitude at 9.6 GHz

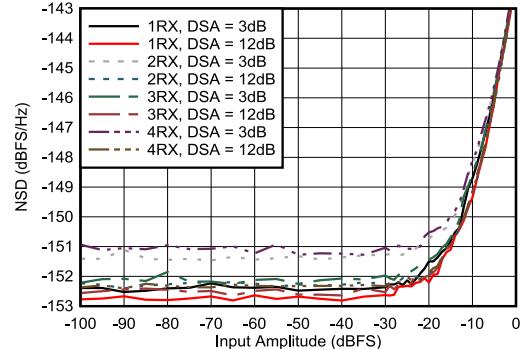


Figure 4-476. RX NSD vs Digital Amplitude at 9.6 GHz

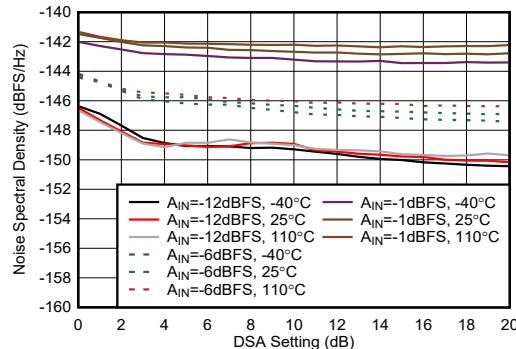


Figure 4-477. RX NSD vs DSA Setting at 9.6 GHz

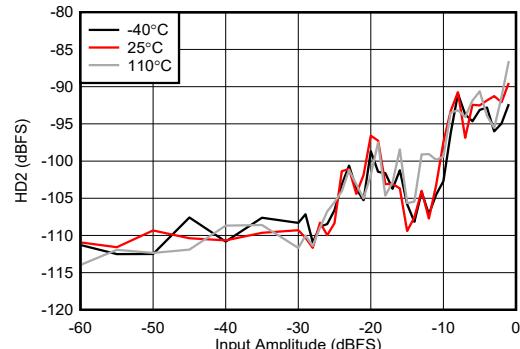


Figure 4-478. RX HD2 vs Digital Level at 9.6 GHz

#### 4.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.

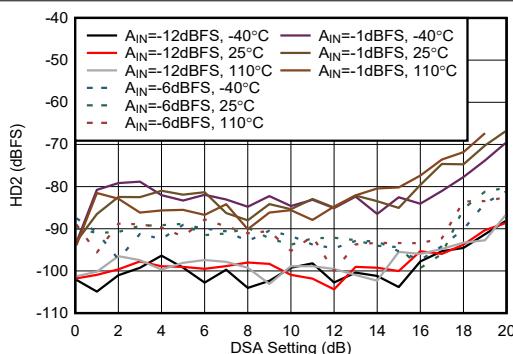


Figure 4-479. RX HD2 vs DSA Setting at 9.6 GHz

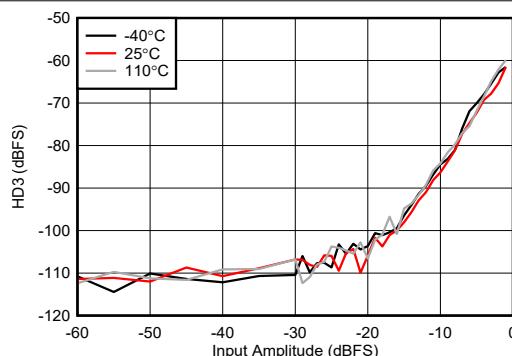


Figure 4-480. RX HD3 vs Digital Level at 9.6 GHz

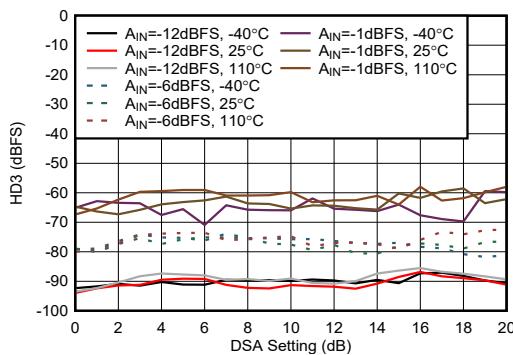


Figure 4-481. RX HD3 vs DSA Setting at 9.6 GHz

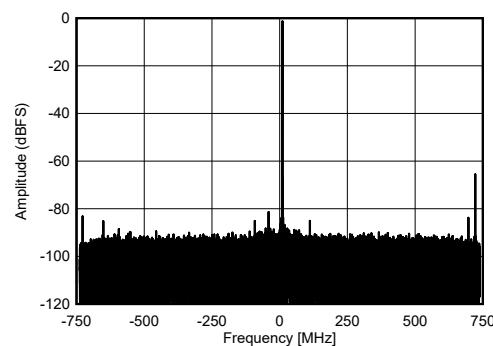
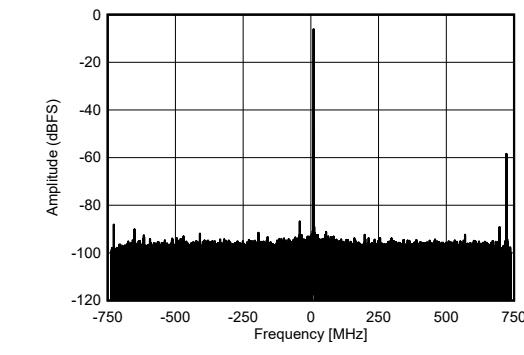
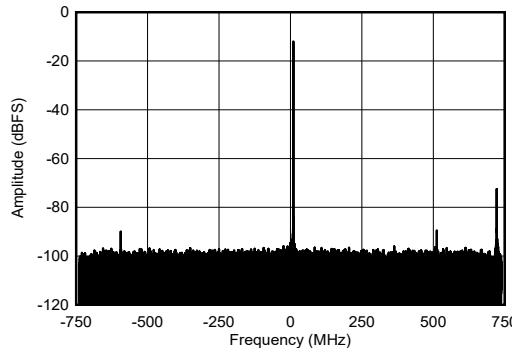


Figure 4-482. RX Single Tone Output FFT at 9.61 GHz



-6 dBFS

Figure 4-483. RX Single Tone Output FFT at 9.61 GHz



-12 dBFS.

Figure 4-484. RX Single Tone Output FFT at 9.61 GHz

#### 4.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.

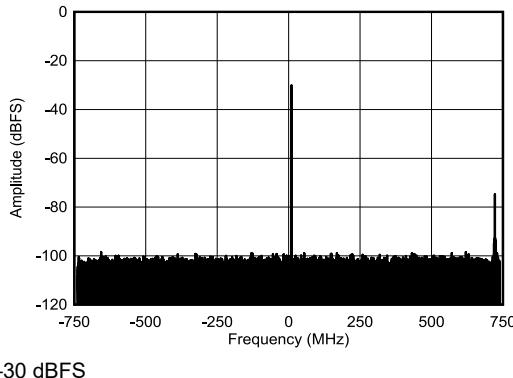


Figure 4-485. RX Single Tone Output FFT at 9.61 GHz

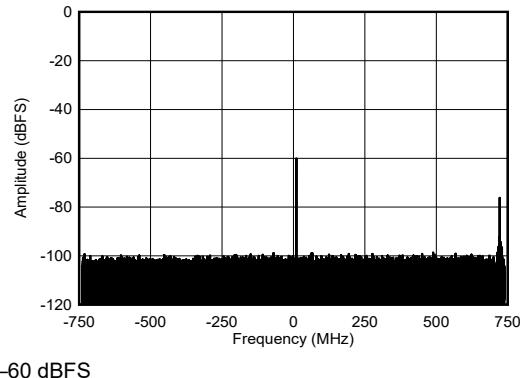


Figure 4-486. RX Single Tone Output FFT at 9.61 GHz

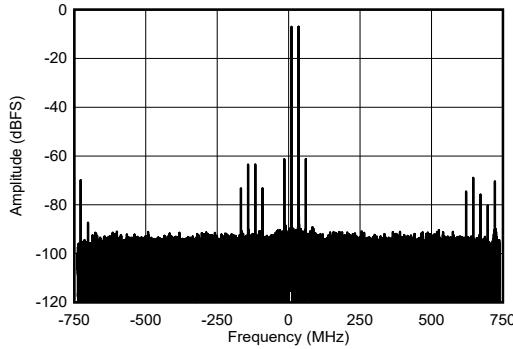


Figure 4-487. RX Two Tone Output FFT at 9.61 GHz

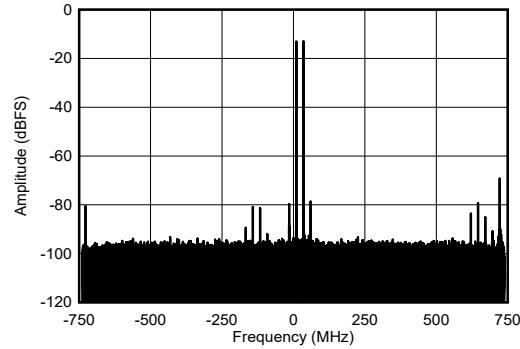


Figure 4-488. RX Two Tone Output FFT at 9.61 GHz

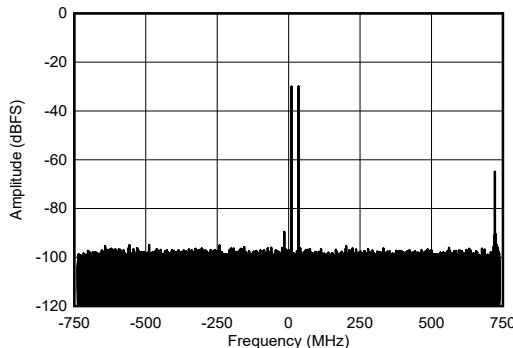


Figure 4-489. RX Two Tone Output FFT at 9.61 GHz

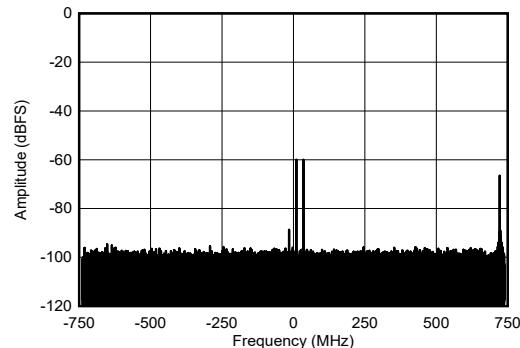
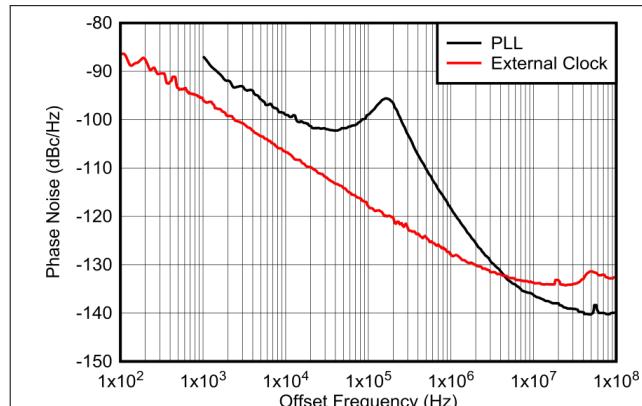


Figure 4-490. RX Two Tone Output FFT at 9.61 GHz

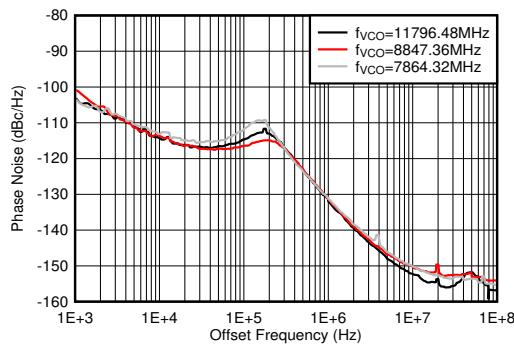
#### 4.12.15 PLL and Clock Typical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted,  $f_{\text{REF}} = 491.52 \text{ MHz}$ , Phase noise measured at TX output



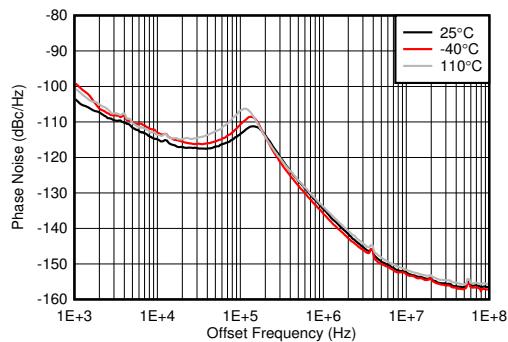
measured at TX output, normalized to 12GHz by  
 $20 \times \log(12\text{GHz}/F_{\text{OUT}})$

**Figure 4-491. Phase Noise vs Offset Frequency for PLL and External Clock at 12GHz**



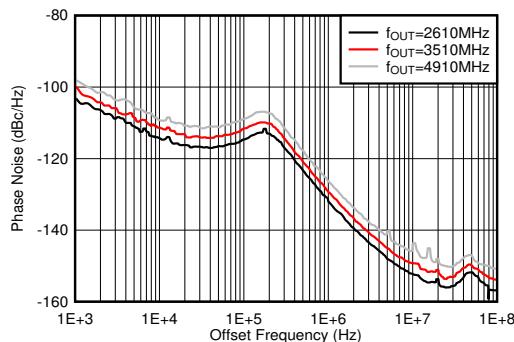
PLL enabled,  $f_{\text{REF}} = 491.52\text{MSPS}$ , measured at 2TXOUT

**Figure 4-492. Phase Noise vs Offset Frequency and  $f_{\text{VCO}}$  at  $f_{\text{OUT}} = 2610 \text{ MHz}$**



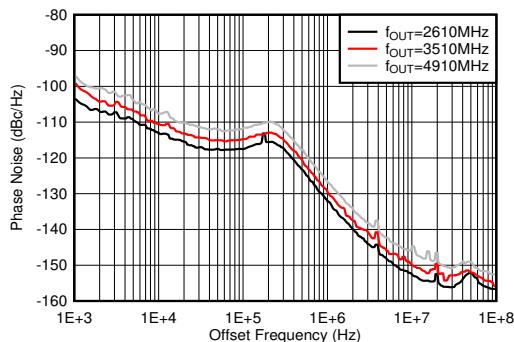
PLL enabled,  $f_{\text{VCO}} = 11796.48 \text{ MHz}$ ,  $f_{\text{REF}} = 491.52\text{MSPS}$ , measured at 2TXOUT

**Figure 4-493. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at  $f_{\text{OUT}} = 1910 \text{ MHz}$**



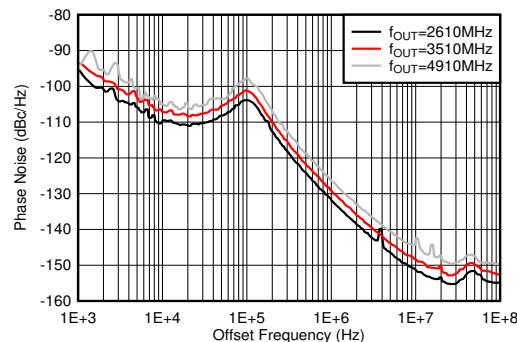
PLL enabled,  $f_{\text{VCO}} = 11796.48 \text{ MHz}$ ,  $f_{\text{REF}} = 491.52\text{MSPS}$ , measured at 2TXOUT

**Figure 4-494. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{\text{OUT}}$  at  $25^\circ\text{C}$**



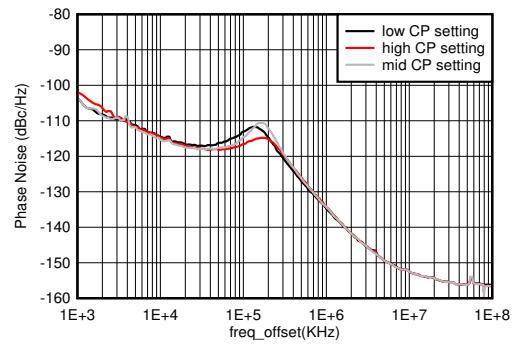
PLL enabled,  $f_{VCO} = 11796.48$  MHz,  $f_{REF} = 491.52$ MSPS,  
measured at 2TXOUT

**Figure 4-495. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{OUT}$  at  $-40^{\circ}\text{C}$**



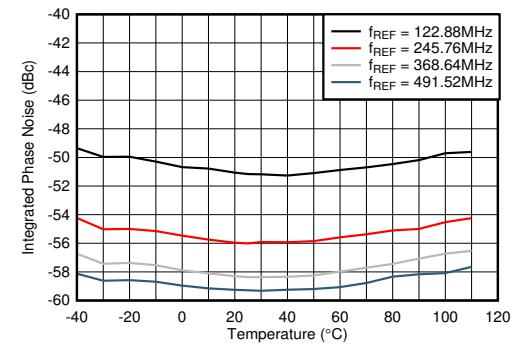
PLL enabled,  $f_{VCO} = 11796.48$  MHz,  $f_{REF} = 491.52$ MSPS,  
measured at 2TXOUT

**Figure 4-496. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{OUT}$  at  $110^{\circ}\text{C}$**



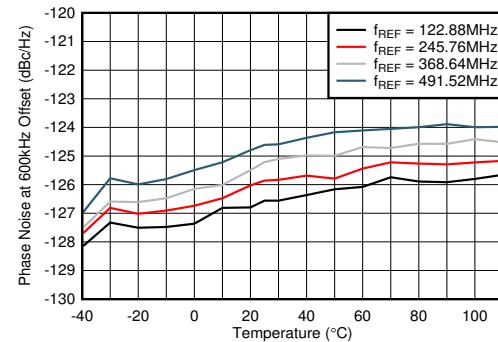
PLL enabled,  $f_{VCO} = 11796.48$  MHz,  $f_{REF} = 491.52$ MSPS,  
measured at 2TXOUT

**Figure 4-497. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at  $f_{OUT} = 2.6$  GHz**



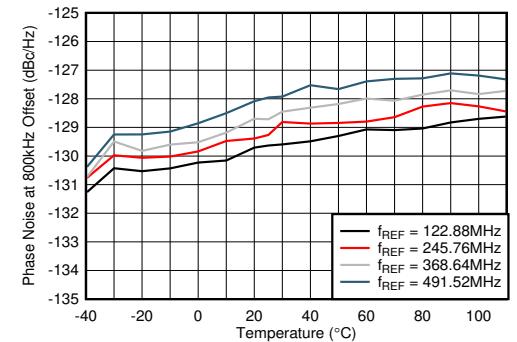
PLL enabled,  $f_{VCO} = 11796.48$  MHz, 1-kHz to 100-MHz,  
single-sided integration bandwidth, measured at 2TXOUT

**Figure 4-498. Integrated Phase Noise for 12-GHz VCO vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



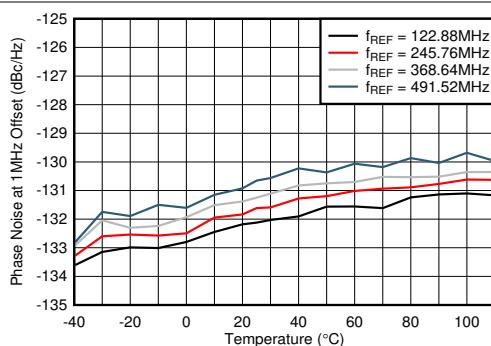
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 4-499. Phase Noise for 12-GHz VCO at 600kHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



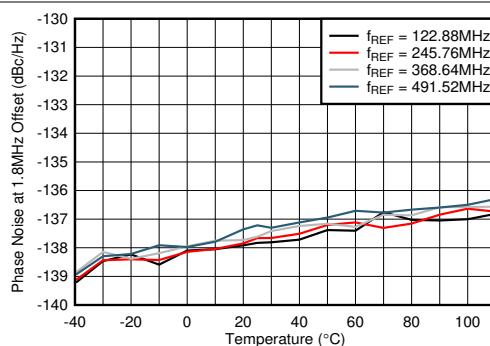
A. PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 4-500. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



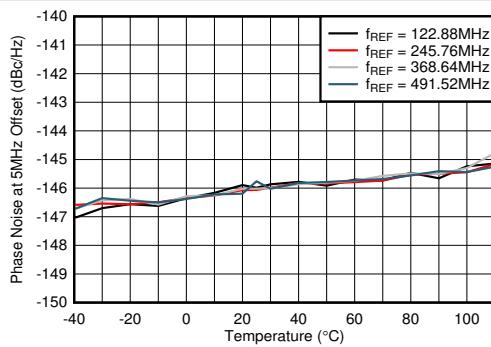
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 4-501. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



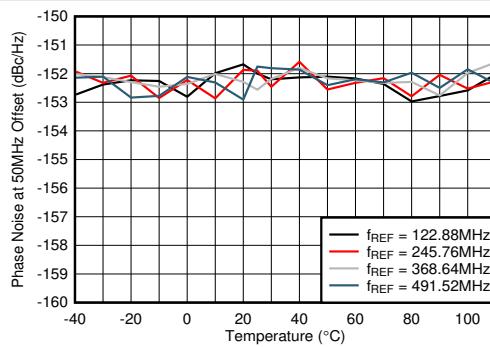
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 4-502. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



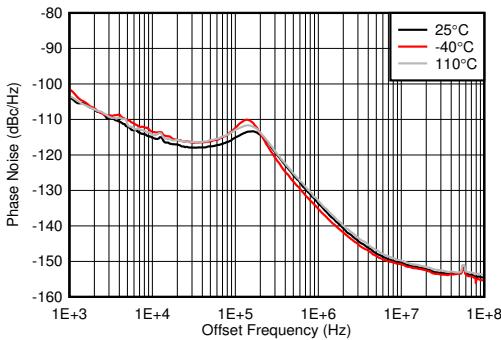
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 4-503. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



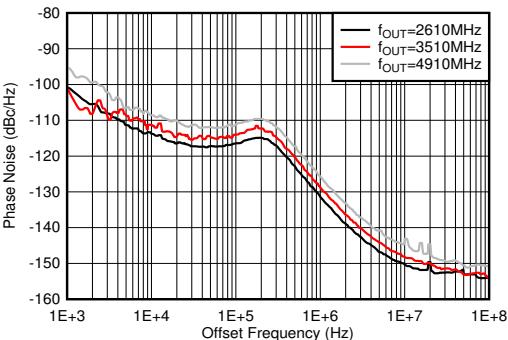
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 4-504. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



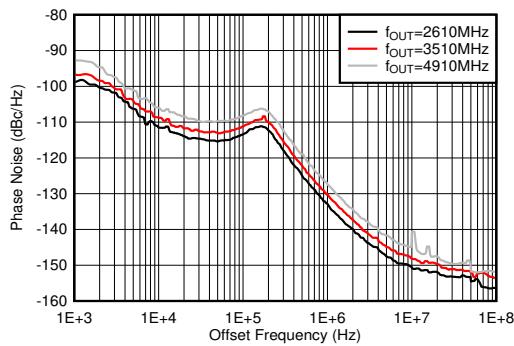
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 4-505. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**



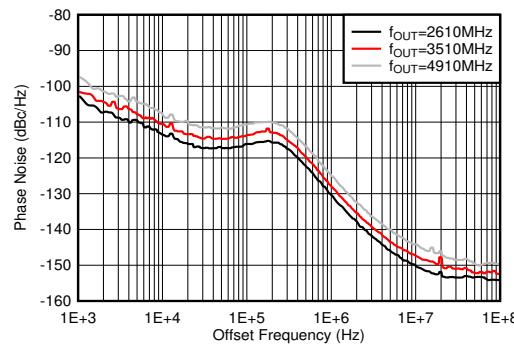
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 4-506. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 25°C**



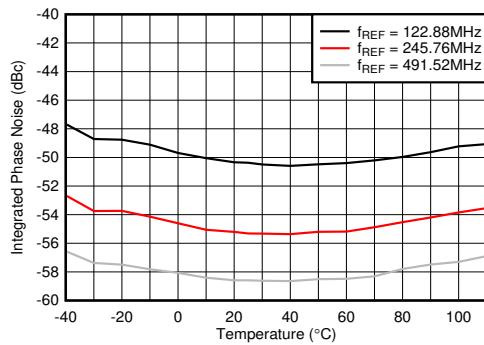
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS,  
measured at 2TXOUT

**Figure 4-507. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at  $-40^{\circ}\text{C}$**



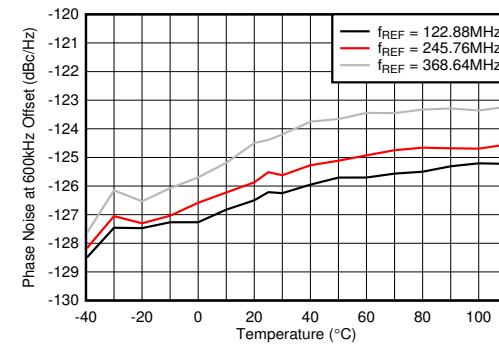
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS,  
measured at 2TXOUT

**Figure 4-508. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at  $110^{\circ}\text{C}$**



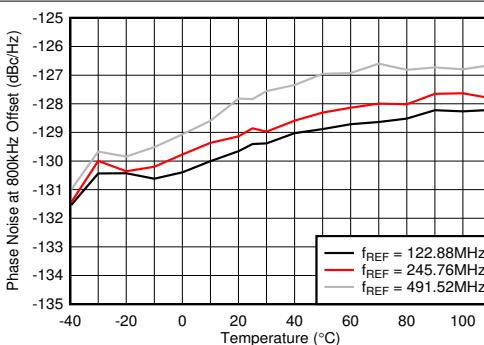
PLL enabled,  $f_{VCO} = 9830.4$  MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

**Figure 4-509. Integrated Phase Noise for 10-GHz VCO vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



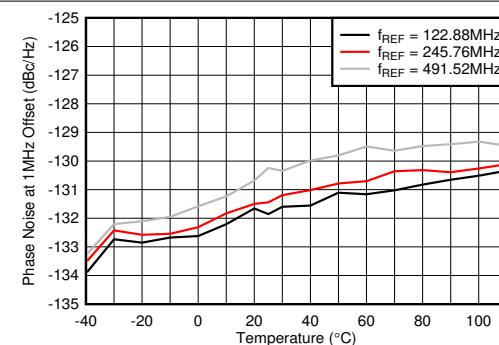
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**Figure 4-510. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



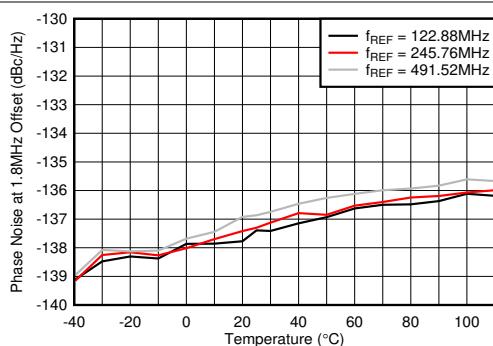
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**Figure 4-511. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



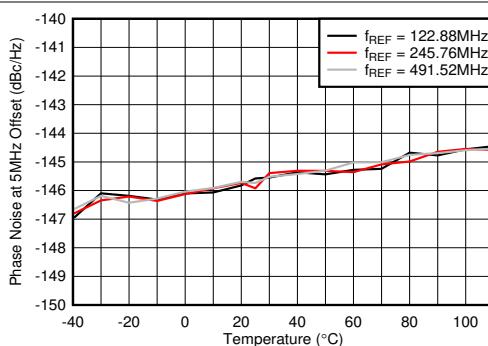
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**Figure 4-512. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



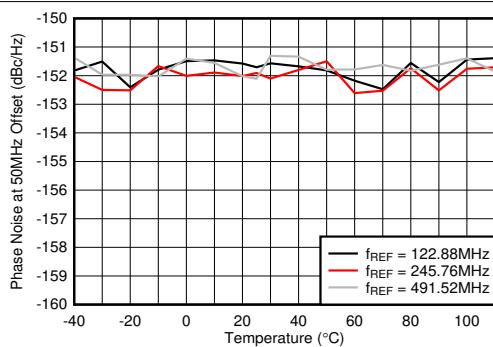
PLL enabled, f<sub>VCO</sub> = 9830.4 MHz, measured at 2TXOUT

**Figure 4-513. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and f<sub>REF</sub> at f<sub>OUT</sub> = 2.6 GHz**



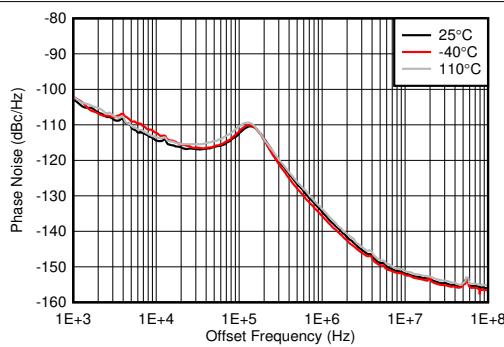
PLL enabled, f<sub>VCO</sub> = 9830.4 MHz, measured at 2TXOUT

**Figure 4-514. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f<sub>REF</sub> at f<sub>OUT</sub> = 2.6 GHz**



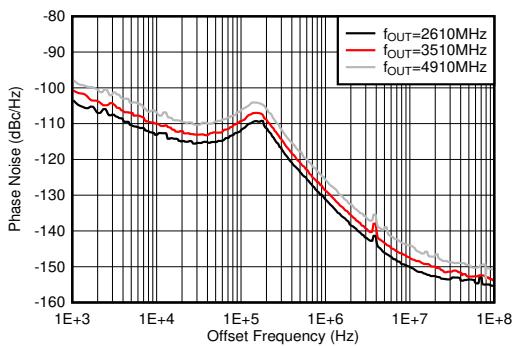
PLL enabled, f<sub>VCO</sub> = 9830.4 MHz, measured at 2TXOUT

**Figure 4-515. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f<sub>REF</sub> at f<sub>OUT</sub> = 2.6 GHz**



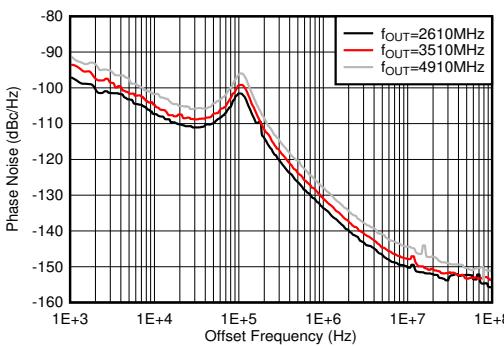
PLL enabled, f<sub>VCO</sub> = 8847.36 MHz, f<sub>REF</sub> = 491.52MSPS, measured at 2TXOUT

**Figure 4-516. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at f<sub>OUT</sub> = 1910 MHz**



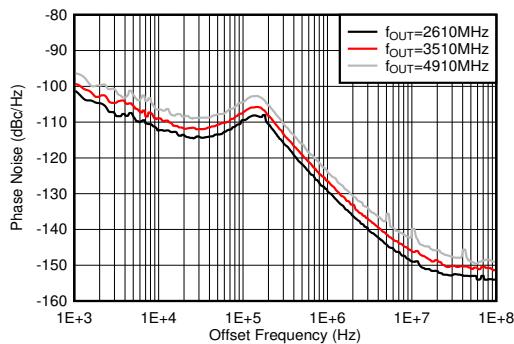
PLL enabled, f<sub>VCO</sub> = 8847.36 MHz, f<sub>REF</sub> = 491.52MSPS, measured at 2TXOUT

**Figure 4-517. Phase Noise for 9-GHz VCO vs Offset Frequency and f<sub>OUT</sub> at 25°C**



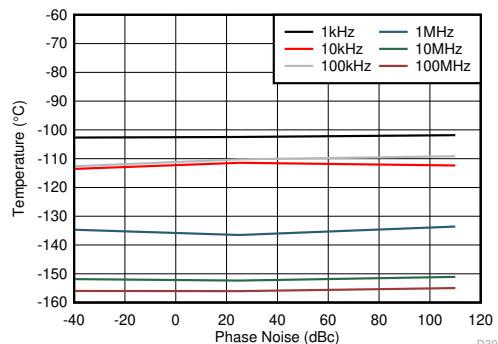
PLL enabled, f<sub>VCO</sub> = 8847.36 MHz, f<sub>REF</sub> = 491.52MSPS, measured at 2TXOUT

**Figure 4-518. Phase Noise for 9-GHz VCO vs Offset Frequency and f<sub>OUT</sub> at -40°C**



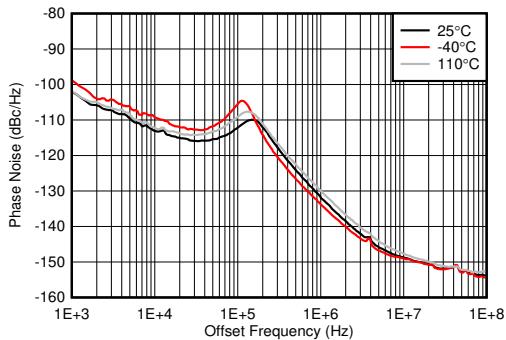
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS,  
measured at 2TXOUT

**Figure 4-519. Phase Noise for 9-GHz VCO vs Offset Frequency and  $f_{OUT}$  at  $110^{\circ}\text{C}$**



PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS,  
minimum LPF BW, measured at 2TXOUT

**Figure 4-520. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at  $f_{OUT} = 2.6$  GHz**



PLL enabled,  $f_{VCO} = 7864.32$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 4-521. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from June 13, 2023 to May 1, 2025 (from Revision D (June 2023) to Revision E (May 2025))

Page

- RX Input Max Power moved from RF ADC Electrical Characteristics to Absolute Maximum Ratings.....4

### Changes from July 12, 2022 to June 12, 2023 (from Revision C (July 2022) to Revision D (June 2023))

Page

- Changed the Packaging Information table to include note 2.....1
- Changed  $I_{IH}$  and  $I_{IL}$  units to  $\mu\text{A}$ .....20
- Removed dither from conditions.....29
- Removed "TX Clock Dither Enabled" from conditions.....29
- Changed captions to read 1.8 GHz in 1.8 GHz section and removed dither from conditions.....38
- Removed "TX Clock Dither Enabled" from conditions.....38
- Removed dither from conditions.....46
- Removed "TX Clock Dither Enabled" from conditions.....46
- Changed OTX to 1TX in plot notes and removed dither from conditions and dither plot.....55

---

• Removed "TX Clock Dither Enabled" from conditions.....	55
• Removed dither from conditions.....	61
• Removed "TX Clock Dither Enabled" from conditions.....	61
• Changed 0TX - 3TX to 1TX - 4TX in plot legends.....	69
• Removed TX dither plot and TX dither in conditions.....	69
• Removed "TX Clock Dither Enabled" from conditions.....	69
• Removed dither from conditions.....	79
• Swapped TX input rate and $f_{REF}$ frequency in header.....	79
• Removed "TX Clock Dither Enabled" from conditions.....	79
• Changed 0RX - 3RX to 1RX - 4RX in plot captions and notes.....	109

---

**Changes from March 9, 2022 to July 12, 2022 (from Revision B (March 2022) to Revision C (July 2022))**

	<b>Page</b>
• Removed dither from conditions.....	29
• Changed captions to read 1.8 GHz in 1.8 GHz section and removed dither from conditions.....	38
• Removed dither from conditions.....	46
• Changed 0TX to 1TX in plot notes and removed dither from conditions and dither plot.....	55
• Removed dither from conditions.....	61
• Changed 0TX - 3TX to 1TX - 4TX in plot legends.....	69
• Removed TX dither plot and TX dither in conditions.....	69
• Removed dither from conditions.....	79
• Changed 0RX - 3RX to 1RX - 4RX in plot captions and notes.....	109

---

**Changes from Revision A (August 2021) to Revision B (March 2022)**

	<b>Page</b>
• Added <i>Feature</i> to Request the full data sheet.....	1
• Added the <a href="#">Specification</a> tables to the data sheet.....	4

---

**Changes from Revision \* (February 2021) to Revision A (August 2021)**

	<b>Page</b>
• Changed the data sheet status From: <i>Advanced Information</i> To: <i>Production</i> data.....	1

---

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.



ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 6.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE7950IABJ	Active	Production	FCBGA (ABJ)   400	90   JEDEC TRAY (5+1)	Yes	SNAGCU   SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7950I
AFE7950IABJ.B	Active	Production	FCBGA (ABJ)   400	90   JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 85	
AFE7950IALK	Active	Production	FCBGA (ALK)   400	90   JEDEC TRAY (5+1)	No	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7950 SNPB
AFE7950IALK.B	Active	Production	FCBGA (ALK)   400	90   JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 85	

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a " ~ " will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

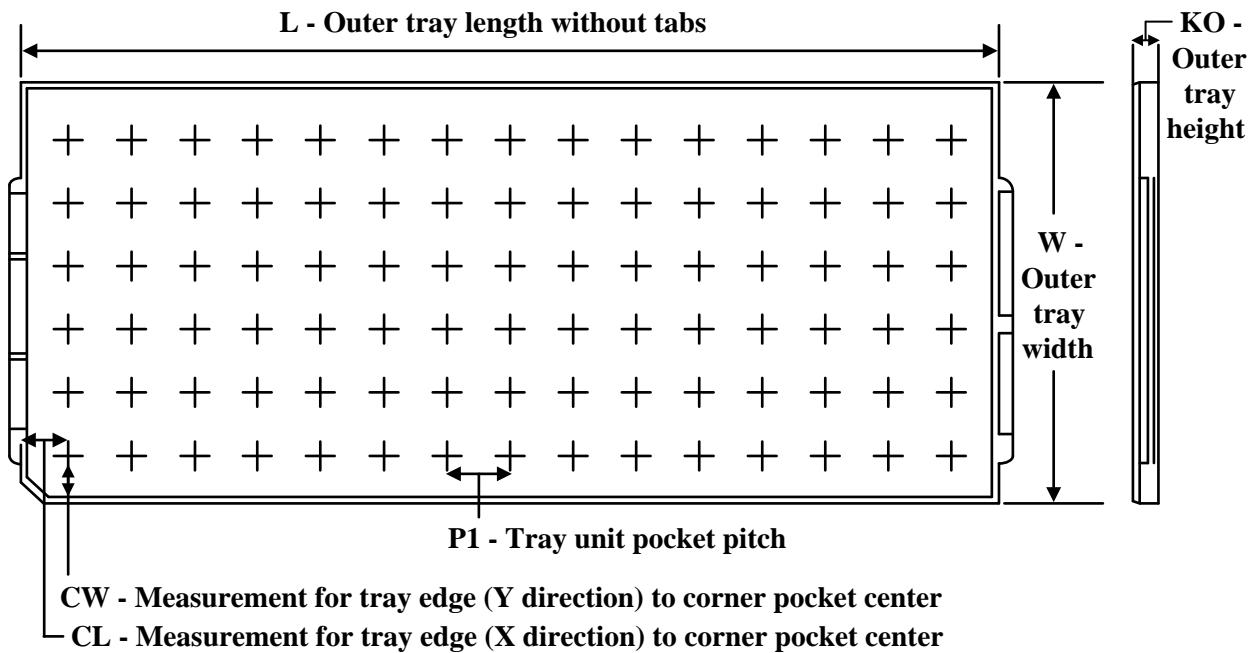
**OTHER QUALIFIED VERSIONS OF AFE7950 :**

- Space : [AFE7950-SP](#)

NOTE: Qualified Version Definitions:

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

---

**TRAY**


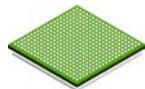
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	KO (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE7950IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7950IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7950IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7950IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2

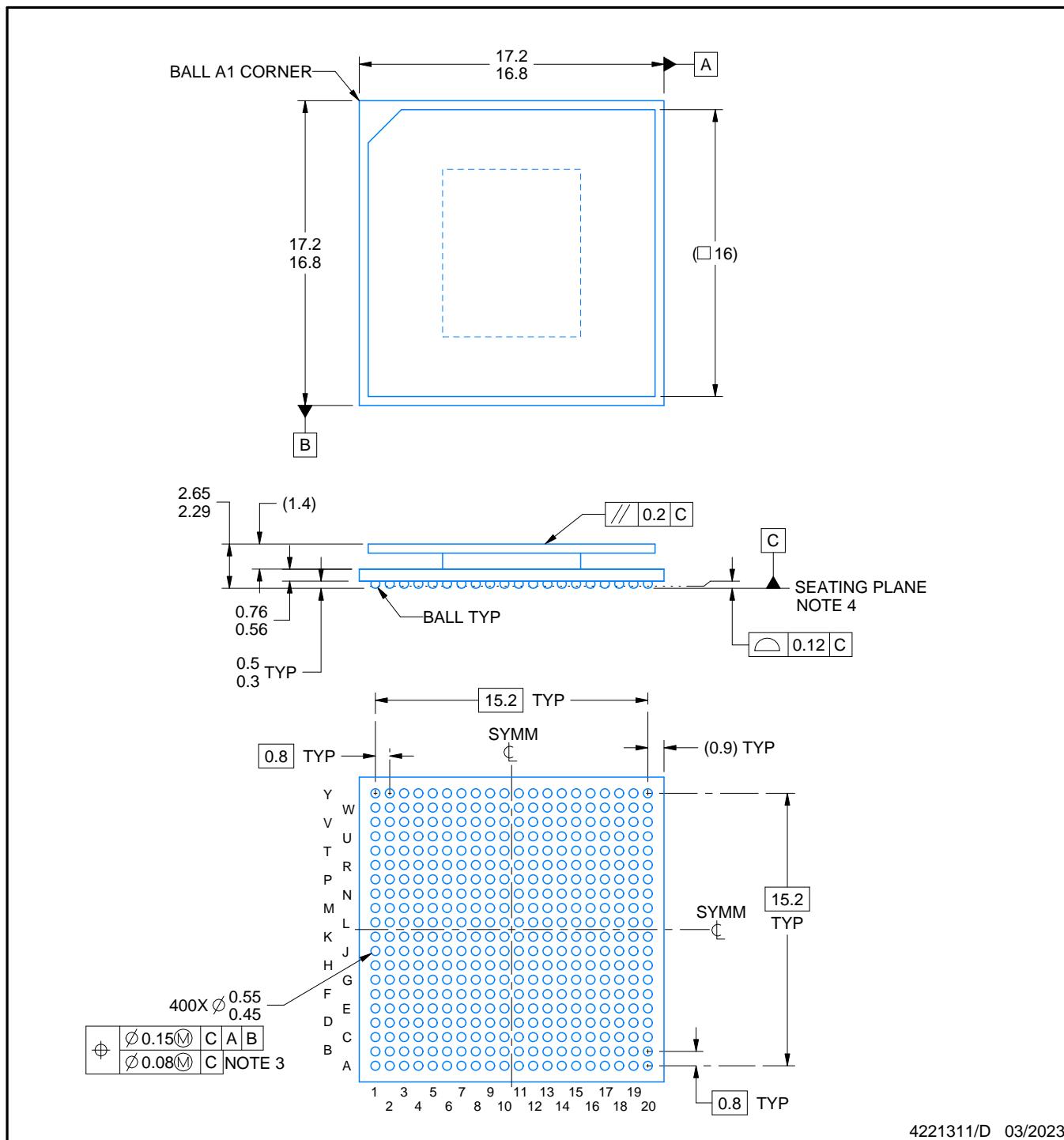
# PACKAGE OUTLINE

**ABJ0400A**



**FCCBGA - 2.65 mm max height**

BALL GRID ARRAY



4221311/D 03/2023

## NOTES:

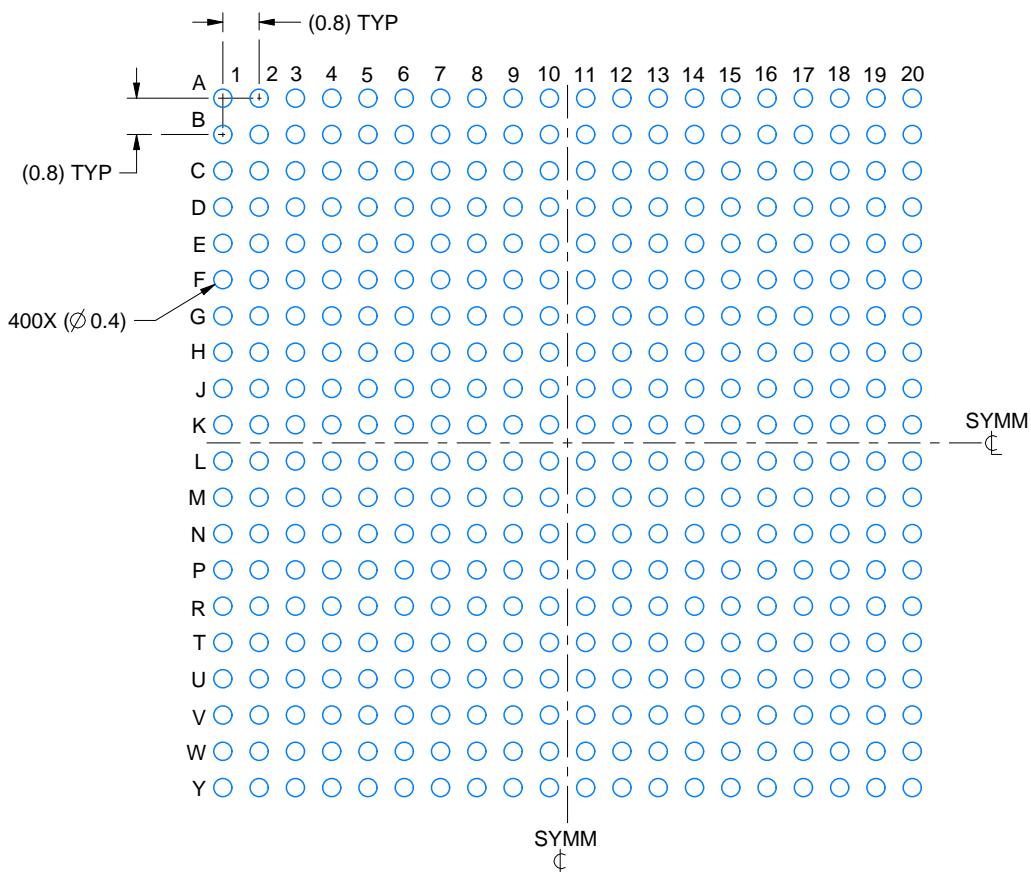
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
- Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
- The lids are electrically floating (e.g. not tied to GND).

# EXAMPLE BOARD LAYOUT

ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



4221311/D 03/2023

NOTES: (continued)

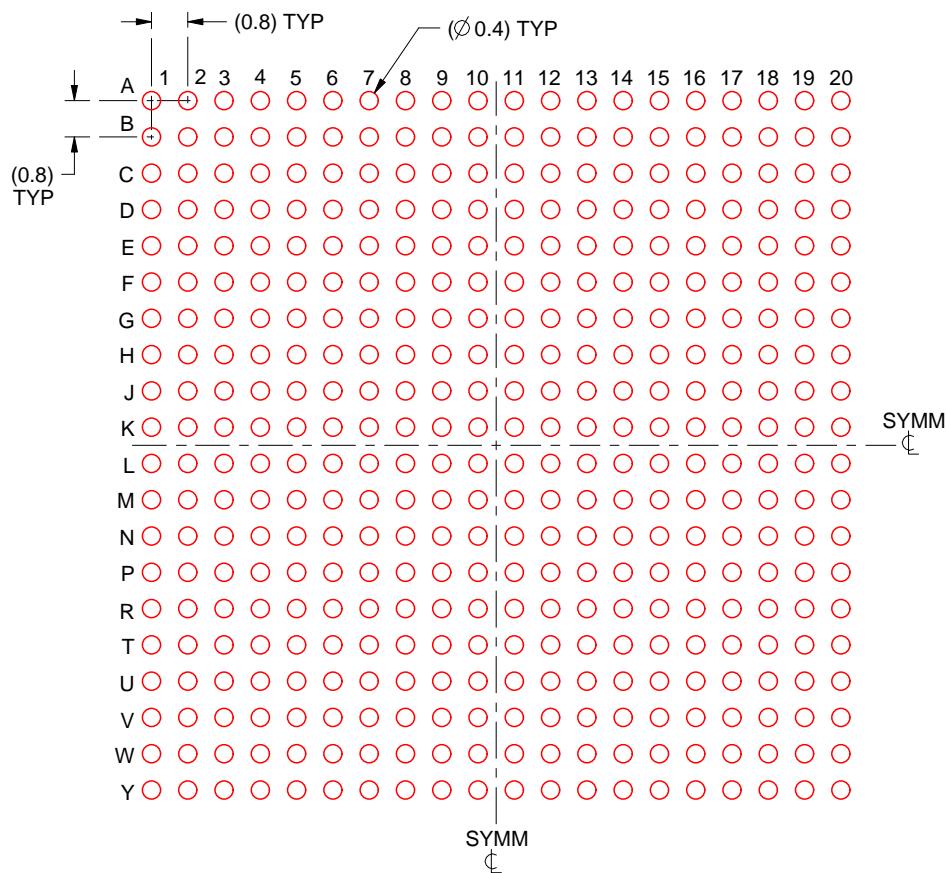
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.  
For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.15 mm THICK STENCIL  
SCALE:6X

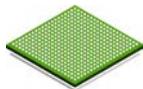
4221311/D 03/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

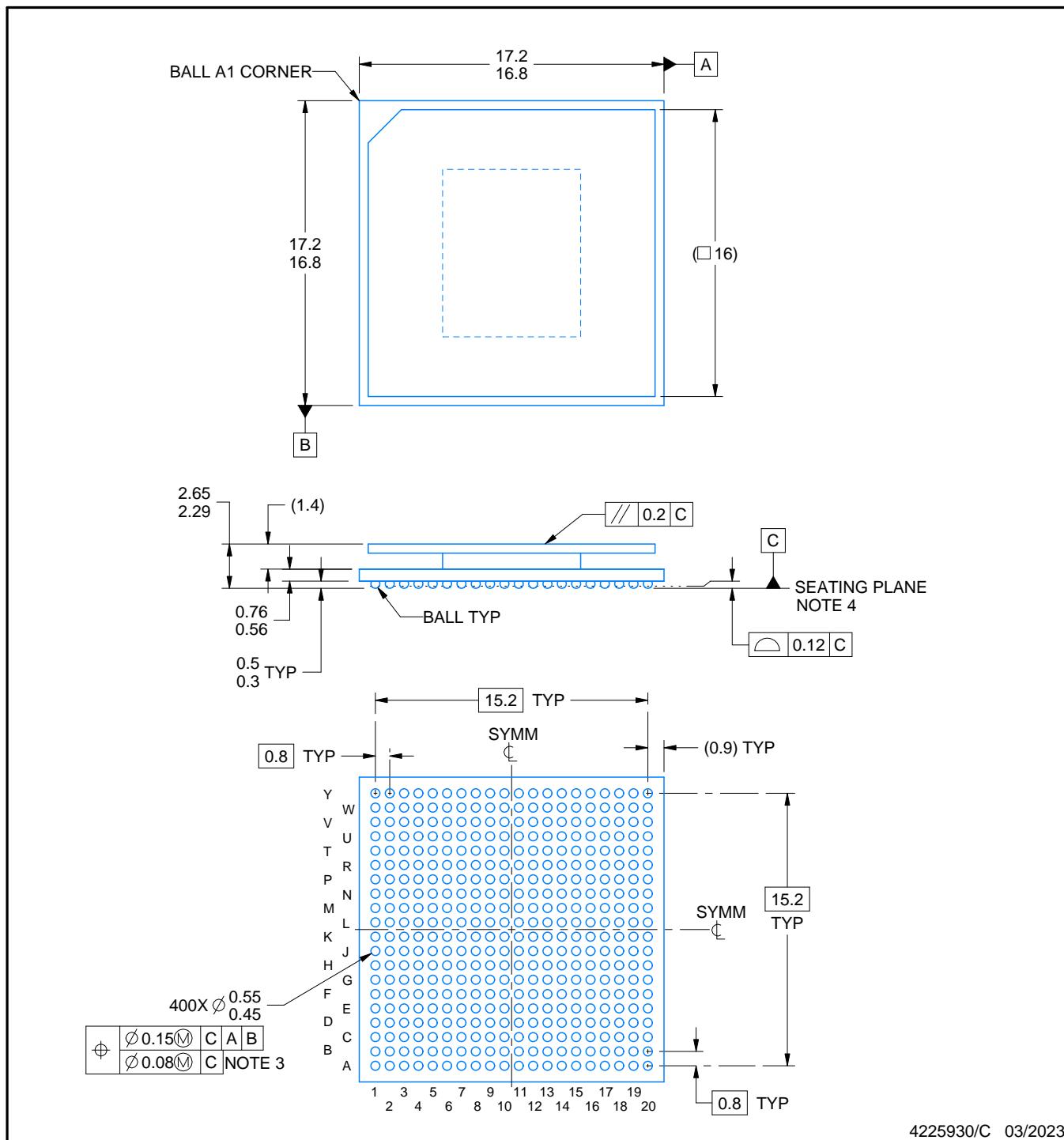
# PACKAGE OUTLINE

**ALK0400A**



**FCCBGA - 2.65 mm max height**

BALL GRID ARRAY



4225930/C 03/2023

## NOTES:

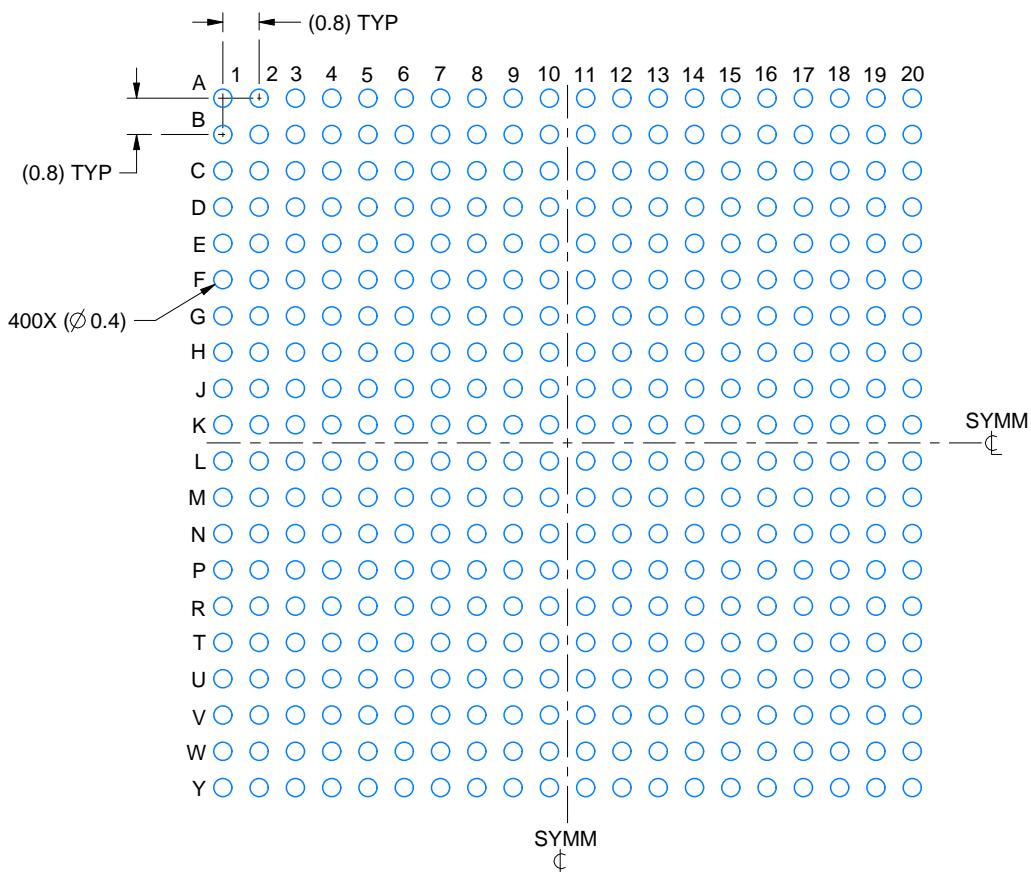
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
- Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
- Pb-Free die bump and SnPb solder ball.
- The lids are electrically floating (e.g. not tied to GND).

# EXAMPLE BOARD LAYOUT

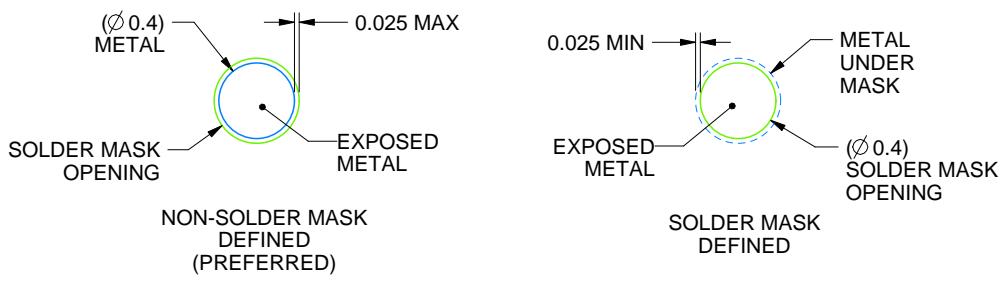
ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

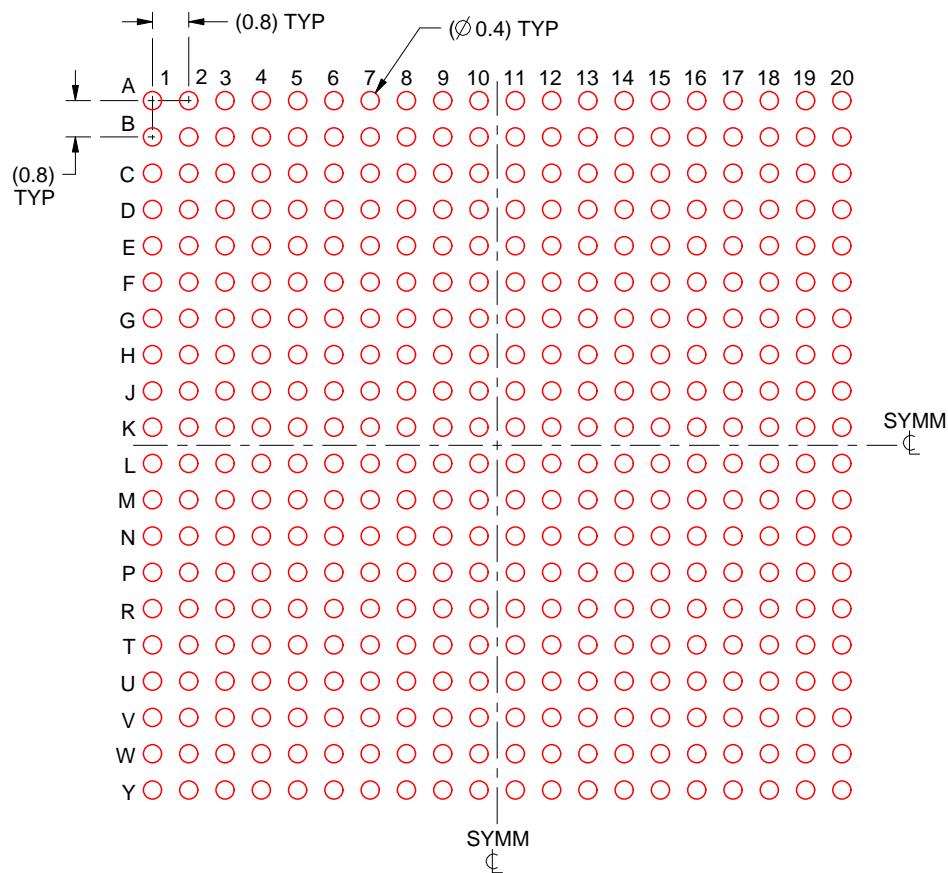
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.  
For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

**ALK0400A**

**FCBGA - 2.65 mm max height**

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.15 mm THICK STENCIL  
SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## **IMPORTANT NOTICE AND DISCLAIMER**

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated