AFE7901 4T4R RF Sampling AFE with 12GSPS DACs and 3GSPS ADCs

1 Features

- Request full data sheet
- Quad RF sampling 12GSPS transmit DACs
- Quad RF sampling 3GSPS receive ADCs
- Maximum RF signal bandwidth per TX or RX: 400MHz
- RF frequency range: 5MHz - 7.4GHz
- Digital step attenuators (DSA):
  – TX: 40dB range, 0.125dB steps
  – RX: 25dB range, 0.5dB steps
- Single or dual-band DUC or DDCs for TX and RX
- 16x NCOs per TX or RX
- Optional Internal PLL or VCO for DAC or ADC clocks or external clock at DAC or ADC sample rate
- Sysref Alignment Detector
- SerDes data interface:
  – JESD204B and JESD204C compatible
  – 8 SerDes transceivers up to 29.5Gbps
  – Subclass 1 multi-device synchronization
- Package: 17mm × 17mm FCBGA, 0.8mm pitch

2 Applications

- Radar
- Seeker front end
- Defense radio
- Tactical communications infrastructure
- Wireless communications test

3 Description

The AFE7901 is a high performance, wide bandwidth multi-channel transceiver, integrating four RF sampling transmitter chains and four RF sampling receiver chains. With operation up to 7.4GHz, this device enables direct RF sampling in the L, S and C-band frequency ranges without the need for additional frequency conversions stages. This improvement in density and flexibility enables high-channel-count, multi-mission systems.

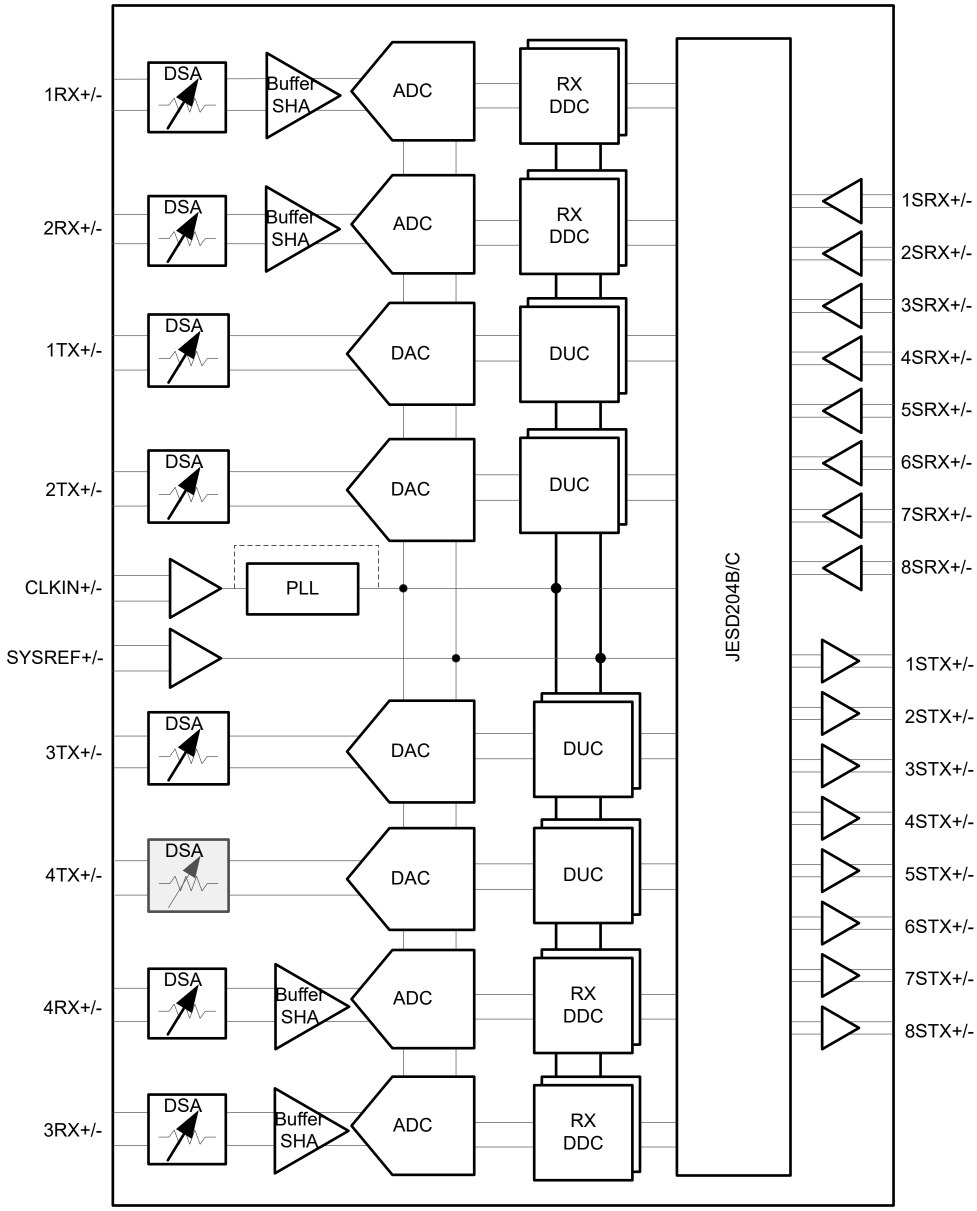
The TX signal paths support interpolation and digital up conversion options that deliver up to 400MHz of signal bandwidth per TX path using a single or dual digital up converter. The output of the DUCs drives a 12GSPS DAC (digital to analog converter) with a mixed mode output option to enhance 2nd Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40dB range and 1dB analog and 0.125dB digital steps.

Each receiver chain includes a 25dB range DSA (Digital Step Attenuator), followed by a 3GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. Flexible decimation options provide optimization of signal bandwidth up to 400MHz using one or two digital down converters (DDCs).

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AFE7901	FC-BGA	17mm × 17mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

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4 Pin Configuration and Functions

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
20	VDD1P2 TXCLK	2TXOUT+	2TXOUT-	VDD1P2 TXCLK	VDD1P8TX	1TXOUT-	1TXOUT+	VDD1P8TX	VSSTX	VDD1P2 PLLCLK REF	VDD1P8 PLLVCO	VSSTX	VDD1P8TX	3TXOUT+	3TXOUT-	VDD1P8TX	VDD1P2 TXCLK	4TXOUT-	4TXOUT+	VDD1P2 TXCLK	20
19	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTX	VSSTX	PLL_LDOUT	SYSREF+	SYSREF-	VSSPLL	VSSTX	VSSTX	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK	19
18	VSSFBCLK	VSSFBCLK	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSPLL CLKREF	VDD1P2 PLLCLK REF	VDD1P2 PLLCLK REF	VSSPLL CLKREF	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSFBCLK	VSSFBCLK	18
17	VDD1P8 FBCLK	VSSFB	VSSTX	VDD1P2 TXENC	VSSTXENC	VSSTX	VDD1P8 TXDAC	VDD1P8 TXDAC	VSS PLLRXCML	REFCLK+	REFCLK-	VSS PLLRXCML	VDD1P8 TXDAC	VDD1P8 TXDAC	VSSTX	VSSTXENC	VDD1P2 TXENC	VSSTX	VSSFB	VDD1P8 FBCLK	17
16	NC	VSSFB	VDD1P8FB	VDD1P2FB	VSSTXENC	GTR_7_SPIB2SEN	GTR_17_SPIB1CLK	GTR_14_SPIB1SEN	VSSPLL FBCML	VDD1P8PLL	VDD1P8PLL	VSSPLL FBCML	GTL_7_ALARM1	GTL_15_GPIO3	GTL_18_SPIASDO	VSSTXENC	VDD1P2FB	VDD1P8FB	VSSFB	NC	16
15	NC	VSSFB	VDD1P8FB	VDD1P2FB	VDD1P2FB	GTR_15_RESETZ	GTR_13_TRST	GTR_3_TXTDD1	GTR_9_SPIB2SDO	VDD1P2 PLLRXCML	VDD1P2 PLLFBCML	GTL_3_AUX0	GTL_2_ALARM2	GTL_4_SPIACLK	GTL_6_RXTDD2	VDD1P2FB	VDD1P2FB	VDD1P8FB	VSSFB	NC	15
14	VDD1P8 FBCLK	VSSFB	VSSFB	VDD1P2FB	VDD1P2RX	GTR_5_TDO	GTR_18_TDI	GTR_4_TCLK	GTR_2_SPIB2CLK	GTR_8_FBTDD1	GTL_8_AUX1	GTL_9_AUX2	GTL_17_SPIASDIO	GTL_1_SPEEP	GTL_5_SPIASEN	VDD1P2RX	VDD1P2FB	VSSFB	VSSFB	VDD1P8 FBCLK	14
13	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_0_RXGSWAP	GTR_6_SPIB2_SDIO	GND_ESD	DVDD0P9	DVDD0P9	GND_ESD	GTL_0_GPIO2	GTL_11_AUX3	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX	13
12	1RXIN+	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_11_SPIB1_SDO	GTR_1_GPIO1	DGND	DVDD0P9	DVDD0P9	DGND	GTL_13_AUX4	GTL_12_BIST1	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	3RXIN+	12
11	1RXIN-	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P2RX	VDD1P2RX	GTR_10_TMS	GTR_12_SPIB1_SDIO	DGND	DVDD0P9	DVDD0P9	DGND	GTL_14_AUX5	GTL_10_BIST0	VDD1P2RX	VDD1P2RX	VDD1P8RX	VDD1P8RX	VSSRX	3RXIN-	11
10	VDD1P2RX	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_6_RXBLNB	GBR_5_FSPIDB	DGND	DVDD0P9	DVDD0P9	DGND	GBL_5_GPIO15	GBL_6_GPIO16	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRX	VDD1P2RX	10
9	VDD1P8 RXCLK	VSSRXCLK	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_9_SYNCB_OUT0-	GBR_7_SYNCB_OUT0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_7_SYNCB_OUT1+	GBL_9_SYNCB_OUT1-	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRXCLK	VDD1P8 RXCLK	9
8	2RXIN-	VSSRX	VSSRXCLK	GND_ESD	GBR_10_FSPICLKA	VDD1P8RX	GBR_13_GPIO8	GBR_8_SYNCB_IN0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_8_SYNCB_IN1+	GBL_13_GPIO19	VDD1P8RX	GBL_10_GPIO17	GND_ESD	VSSRXCLK	VSSRX	4RXIN-	8
7	2RXIN+	VSSRX	VSSRXCLK	GND_ESD	GBR_11_RXTDD1	GBR_14_FSPIDA	GBR_12_GPIO7	GBR_17_SYNCB_IN0-	DGND	DVDD0P9	DVDD0P9	DGND	GBL_17_SYNCB_IN1-	GBL_12_FSPICLKD	GBL_14_FSPIDD	GBL_11_GPIO18	GND_ESD	VSSRXCLK	VSSRX	4RXIN+	7
6	VDD1P8 RXCLK	VSSRXCLK	GBR_0_GPIO4	GBR_19_GPIO12	GBR_16_GPIO10	GBR_1_GPIO5	GBR_15_GPIO9	VDD1P8 GPIO	DGND	DVDD0P9	DVDD0P9	DGND	VDD1P8 GPIO	GBL_15_FSPIDC	GBL_1_FBTDD2	GBL_16_RXCLNB	GBL_19_GPIO20	GBL_0_GPIO13	VSSRXCLK	VDD1P8 RXCLK	6
5	VSSRXCLK	VSSRXCLK	GBR_18_GPIO11	GBR_2_RXALNB	GBR_4_GPIO6	GBR_3_FSPICLKB	IFORCE	VSSGPIO	DGND	DVDD0P9	DVDD0P9	DGND	VSSGPIO	VSENSE	GBL_3_GPIO14	GBL_4_RXDLNB	GBL_2_FSPICLKC	GBL_18_TXTDD2	VSSRXCLK	VSSRXCLK	5
4	VSST	VSST	1STX+	VDDT0P9	2STX+	VDDA1P8	3STX-	VDDA1P8	4STX-	VSST	VSST	5STX-	VDDA1P8	6STX-	VDDA1P8	7STX+	VDDT0P9	8STX+	VSST	VSST	4
3	1SRX+	VSST	1STX-	VDDT0P9	2STX-	VDDA1P8	3STX+	VDDA1P8	4STX+	SERDES_AMUX1	SERDES_AMUX2	5STX+	VDDA1P8	6STX+	VDDA1P8	7STX-	VDDT0P9	8STX-	VSST	8SRX+	3
2	1SRX-	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST	DVDD0P9	DVDD0P9	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST	8SRX-	2
1	VSST	2SRX+	2SRX-	VSST	3SRX+	3SRX-	VSST	4SRX+	4SRX-	VSST	VSST	5SRX-	5SRX+	VSST	6SRX-	6SRX+	VSST	7SRX-	7SRX+	VSST	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

TX Outputs
RX Inputs
Clock Inputs
Serdes Receivers
Serdes Transmitters
MISC Analog
GPIO
0.9V Supplies
1.2V Supplies
1.8V Supplies
GROUND

Figure 4-1. FCBGA Package, 400-Pin (Top View)

Table 4-1. Pin Functions

BALL NAME	BALL NUMBER	TYPE[(1)]	DESCRIPTION
RF INTERFACES			
NC	A15, A16, Y15, Y16	I	Do not connect.
1RXIN–	A11	I	Receiver Channel 1 RF input: negative terminal. Unused RX inputs can be left open.
1RXIN+	A12	I	Receiver Channel 1 RF input: positive terminal. Unused RX inputs can be left open.
2RXIN–	A8	I	Receiver Channel 2 RF input: negative terminal. Unused RX inputs can be left open.

Table 4-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE[(1)]	DESCRIPTION
2RXIN+	A7	I	Receiver Channel 2 RF input: positive terminal. Unused RX inputs can be left open.
3RXIN–	Y11	I	Receiver Channel 3 RF input: negative terminal.
3RXIN+	Y12	I	Receiver Channel 3 RF input: positive terminal. Unused RX inputs can be left open.
4RXIN–	Y8	I	Receiver Channel 4 RF input: negative terminal. Unused RX inputs can be left open.
4RXIN+	Y7	I	Receiver Channel 4 RF input: positive terminal. Unused RX inputs can be left open.
1TXOUT–	F20	O	Transmitter Channel 1 RF output: negative terminal. Connect to 1.8V when not used.
1TXOUT+	G20	O	Transmitter Channel 1 RF output: positive terminal. Connect to 1.8V when not used.
2TXOUT–	C20	O	Transmitter Channel 2 RF output: negative terminal. Connect to 1.8V when not used.
2TXOUT+	B20	O	Transmitter Channel 2 RF output: positive terminal. Connect to 1.8V when not used.
3TXOUT–	R20	O	Transmitter Channel 3 RF output: negative terminal. Connect to 1.8V when not used.
3TXOUT+	P20	O	Transmitter Channel 3 RF output: positive terminal. Connect to 1.8V when not used.
4TXOUT–	V20	O	Transmitter Channel 4 RF output: negative terminal. Connect to 1.8V when not used.
4TXOUT+	W20	O	Transmitter Channel 4 RF output: positive terminal. Connect to 1.8V when not used.
DIFFERENTIAL CLOCKS INPUTS			
REFCLK–	L17	I	Reference Clock Inputs: negative terminal
REFCLK+	K17	I	Reference Clock Inputs: positive terminal
SYSREF–	L19	I	SYSREEF inputs: negative terminals
SYSREF+	K19	I	SYSREEF inputs: positive terminals
SerDes CML INTERFACE			
1SRX–	A2	I	CML SerDes Interface Lane 1 input: negative terminal. Unused Serdes inputs can be left open.
1SRX+	A3	I	CML SerDes Interface Lane 1 input: positive terminal. Unused Serdes inputs can be left open.
2SRX–	C1	I	CML SerDes Interface Lane 2 input: negative terminal. Unused Serdes inputs can be left open.
2SRX+	B1	I	CML SerDes Interface Lane 2 input: positive terminal. Unused Serdes inputs can be left open.
3SRX–	F1	I	CML SerDes Interface Lane 3 input: negative terminal
3SRX+	E1	I	CML SerDes Interface Lane 3 input: positive terminal. Unused Serdes inputs can be left open.
4SRX–	J1	I	CML SerDes Interface Lane 4 input: negative terminal
4SRX+	H1	I	CML SerDes Interface Lane 4 input: positive terminal
5SRX–	M1	I	CML SerDes Interface Lane 5 input: negative terminal. Unused Serdes inputs can be left open.
5SRX+	N1	I	CML SerDes Interface Lane 5 input: positive terminal
6SRX–	R1	I	CML SerDes Interface Lane 6 input: negative terminal
6SRX+	T1	I	CML SerDes Interface Lane 6 input: positive terminal. Unused Serdes inputs can be left open.

Table 4-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE[(1)]	DESCRIPTION
7SRX–	V1	I	CML SerDes Interface Lane 7 input: negative terminal
7SRX+	W1	I	CML SerDes Interface Lane 7 input: positive terminal. Unused Serdes inputs can be left open.
8SRX–	Y2	I	CML SerDes Interface Lane 8 input: negative terminal
8SRX+	Y3	I	CML SerDes Interface Lane 8 input: positive terminal. Unused Serdes inputs can be left open.
1STX–	C3	O	CML SerDes Interface Lane 1 output: negative terminal. Unused Serdes outputs can be left open.
1STX+	C4	O	CML SerDes Interface Lane 1 output: positive terminal. Unused Serdes outputs can be left open.
2STX–	E3	O	CML SerDes Interface Lane 2 output: negative terminal. Unused Serdes outputs can be left open.
2STX+	E4	O	CML SerDes Interface Lane 2 output: positive terminal. Unused Serdes outputs can be left open.
3STX–	G4	O	CML SerDes Interface Lane 3 output: negative terminal. Unused Serdes outputs can be left open.
3STX+	G3	O	CML SerDes Interface Lane 3 output: positive terminal. Unused Serdes outputs can be left open.
4STX–	J4	O	CML SerDes Interface Lane 4 output: negative terminal. Unused Serdes outputs can be left open.
4STX+	J3	O	CML SerDes Interface Lane 4 output: positive terminal. Unused Serdes outputs can be left open.
5STX–	M4	O	CML SerDes Interface Lane 5 output: negative terminal. Unused Serdes outputs can be left open.
5STX+	M3	O	CML SerDes Interface Lane 5 output: positive terminal. Unused Serdes outputs can be left open.
6STX–	P4	O	CML SerDes Interface Lane 6 output: negative terminal. Unused Serdes outputs can be left open.
6STX+	P3	O	CML SerDes Interface Lane 6 output: positive terminal. Unused Serdes outputs can be left open.
7STX–	T3	O	CML SerDes Interface Lane 7 output: negative terminal. Unused Serdes outputs can be left open.
7STX+	T4	O	CML SerDes Interface Lane 7 output: positive terminal. Unused Serdes outputs can be left open.
8STX–	V3	O	CML SerDes Interface Lane 8 output: negative terminal. Unused Serdes outputs can be left open.
8STX+	V4	O	CML SerDes Interface Lane 8 output: positive terminal. Unused Serdes outputs can be left open.
GPIO FUNCTIONS			
GBL_0_GPIO13	V6	I/O	GPIO.
GBL_1_FBTDD2	R6	I/O	Default location of FB TDD2 input signal.
GBL_2_FSPICLKC	U5	I/O	Default and recommended location of FSPI C clock (FSPI for factory use only, available as generic GPIO).
GBL_3_GPIO14	R5	I/O	GPIO.
GBL_4_RXDLNB	T5	I/O	Default location of RX channel D AGC LNA Bypass output signal.
GBL_5_GPIO15	N10	I/O	GPIO.
GBL_6_GPIO16	P10	I/O	GPIO.

Table 4-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE(1)	DESCRIPTION
GBL_7_SYNCB_OUT1+	N9	I/O	Default location of JESD Sync\ 1 output differential positive terminal.
GBL_8_SYNCB_IN1+	N8	I/O	Default location of JESD Sync\ 1 input differential positive terminal.
GBL_9_SYNCB_OUT1–	P9	I/O	Default location of JESD Sync\ 1 output differential negative terminal.
GBL_10_GPIO17	T8	I/O	GPIO.
GBL_11_GPIO18	T7	I/O	GPIO.
GBL_12_FSPICLKD	P7	I/O	Default and recommended location of FSPI D clock (FSPI for factory use only, available as generic GPIO).
GBL_13_GPIO19	P8	I/O	GPIO.
GBL_14_FSPIDD	R7	I/O	Default and recommended location of FSPI D data (FSPI for factory use only, available as generic GPIO).
GBL_15_FSPIDC	P6	I/O	Default and recommended location of FSPI C clock (FSPI for factory use only, available as generic GPIO).
GBL_16_RXCLNB	T6	I/O	Default location of RX channel C AGC LNA Bypass output signal.
GBL_17_SYNCB_IN1–	N7	I/O	Default location of JESD Sync\ 1 input differential negative terminal.
GBL_18_TXTDD2	V5	I/O	Default location of TX TDD2 input signal.
GBL_19_GPIO20	U6	I/O	GPIO.
GBR_0_GPIO4	C6	I/O	GPIO.
GBR_1_GPIO5	F6	I/O	GPIO.
GBR_2_RXALNB	D5	I/O	Default location of RX channel A AGC LNA Bypass output signal.
GBR_3_FSPICLKB	F5	I/O	Default and recommended location of FSPI B clock (FSPI for factory use only, available as generic GPIO).
GBR_4_GPIO6	E5	I/O	GPIO.
GBR_5_FSPIDB	H10	I/O	Default and recommended location of FSPI B data (FSPI for factory use only, available as generic GPIO).
GBR_6_RXBLNB	G10	I/O	Default location of RX channel B AGC LNA Bypass output signal.
GBR_7_SYNCB_OUT0+	H9	I/O	Default location of JESD Sync\ 0 output differential positive terminal.
GBR_8_SYNCB_IN0+	H8	I/O	Default location of JESD Sync\ 0 input differential positive terminal.
GBR_9_SYNCB_OUT0–	G9	I/O	Default location of JESD Sync\ 0 output differential negative terminal.
GBR_10_FSPICLKA	E8	I/O	Default location of FSPI A clock (FSPI for factory use only, available as generic GPIO).
GBR_11_RXTDD1	E7	I/O	Default location of RX TDD1 input signal.
GBR_12_GPIO7	G7	I/O	GPIO.
GBR_13_GPIO8	G8	I/O	GPIO.
GBR_14_FSPIDA	F7	I/O	Default and recommended location of FSPI A clock (FSPI for factory use only, available as generic GPIO).
GBR_15_GPIO9	G6	I/O	GPIO.
GBR_16_GPIO10	E6	I/O	GPIO.
GBR_17_SYNCB_IN0–	H7	I/O	Default location of JESD Sync\ 0 input differential negative terminal.
GBR_18_GPIO11	C5	I/O	GPIO.
GBR_19_GPIO12	D6	I/O	GPIO.

Table 4-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE[(1)]	DESCRIPTION
GTL_0_GPIO2	N13	I/O	GPIO.
GTL_1_SLEEP	P14	I/O	Default location of Sleep input signal.
GTL_2_ALARM2	N15	I/O	Default location of Alarm 2 output signal.
GTL_3_AUX0	M15	I/O	GPIO or auxiliary low-speed ADC input 0
GTL_4_SPIACLK	P15	I/O	Fixed Location of SPI A Clock.
GTL_5_SPIASEN	R14	I/O	Fixed Location of SPI A Send Enable.
GTL_6_RXTDD2	R15	I/O	Default location of RX TDD2 input signal.
GTL_7_ALARM1	N16	I/O	Default location of Alarm 1 output signal.
GTL_8_AUX1	L14	I/O	GPIO or auxiliary low-speed ADC input 1.
GTL_9_AUX2	M14	I/O	GPIO or auxiliary low-speed ADC input 2.
GTL_10_BIST0	P11	I/O	Fixed Location for BIST0 Function. Set low when using JTAG, set high for normal operation.
GTL_11_AUX3	P13	I/O	GPIO or auxiliary low-speed ADC input 3.
GTL_12_BIST1	P12	I/O	Fixed Location for BIST1 Function. Set high when using JTAG, set low for normal operation.
GTL_13_AUX4	N12	I/O	GPIO or auxiliary low-speed ADC input 4.
GTL_14_AUX5	N11	I/O	GPIO or auxiliary low-speed ADC input 5.
GTL_15_GPIO3	P16	I/O	GPIO.
GTL_17_SPIASDIO	N14	I/O	Fixed Location of SPI A Serial Data Input (3- and 4-wire mode) or Output (3 wire mode only).
GTL_18_SPIASDO	R16	I/O	Fixed Location of SPI A Serial Data Output in 4-wire mode.
GTR_0_RXGSWAP	G13	I/O	Default location of RX gain swap input.
GTR_1_GPIO1	H12	I/O	GPIO.
GTR_2_SPIB2CLK	J14	I/O	Default and recommended location of SPI B2 clock.
GTR_3_TXTDD1	H15	I/O	Default location of TX TDD1 input signal.
GTR_4_TCLK	H14	I/O	Fixed location for JTAG Test Clock.
GTR_5_TDO	F14	I/O	Fixed location for JTAG Test Data Out.
GTR_6_SPIB2_SDIO	H13	I/O	Default and recommended location of SPI B2 serial data input/output.
GTR_7_SPIB2SEN	F16	I/O	Default and recommended location of SPI B2 enable input.
GTR_8_FBTDD1	K14	I/O	Default location of FB TDD1 input signal.
GTR_9_SPIB2SDO	J15	I/O	Default and recommended location of SPI B2 serial data output (4-wire mode)
GTR_10_TMS	G11	I/O	Fixed location for JTAG Test Mode Select.
GTR_11_SPIB1_SDO	G12	I/O	Default and recommended location of SPI B1 serial data output (4-wire mode).
GTR_12_SPIB_SDIO	H11	I/O	Default and recommended location of SPI B1 serial data input/output.
GTR_13_TRST	G15	I/O	Fixed location for JTAG Test Reset. Must be pulled low when the JTAG port is not used.
GTR_14_SPIB1SEN	H16	I/O	Default and recommended location of SPI B1 enable input.
GTR_15_RESETZ	F15	I/O	Fixed Location for reset function. Chip Reset to default register settings.
GTR_17_SPIB1CLK	G16	I/O	Default and recommended location of SPI B1 clock.
GTR_18_TDI	G14	I/O	Fixed location for JTAG Test Data Input.
POWER SUPPLIES			
DVDD	K2, K5, K6, K7, K8, K9, K10, K11, K12, K13, L2, L5, L6, L7, L8, L9, L10, L11, L12, L13	—	0.9V digital power supply

Table 4-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE(1)	DESCRIPTION
VDD1P2FB	D14, D15, D16, E15, U14, U15, U16, T15	—	1.2V supply for FB ADCs.
VDD1P8FB	C15, C16, V15, V16	—	1.8V supply for FB ADC.
VDD1P8FBCLK	A14, A17, Y17, Y14	—	1.8V supply for FB ADC clock.
VDD1P2PLLCLKREF	K20, K18, L18	—	1.2V supply for PLL.
VDDPLL1P2FBCML	L15	—	1.2V supply for PLL clock distribution to FB ADC.
VDDPLL1P2RXCML	K15	—	1.2V supply for clock distribution to RX ADC.
VDD1P8PLL	K16, L16	—	1.8V supply for PLL.
VDD1P8PLLVCO	L20	—	1.8V supply for PLL/VCO. This is a sensitive net and requires extra care in layout.
VDD1P2RX	A10, A13, E11, E12, E13, E14,F11, F12, F13, R11, R12, R13, T11, T12, T13, T14, Y10, Y13	—	1.2V supply for RX ADCs.
VDD1P8RX	C9, C10, C11, D9, D10, D11, E9, E10, F8, F9, F10, R8, R9, R10, T9, T10, U9, U10, U11, V9, V10, V11	—	1.8V supply for RX ADCs.
VDD1P8RXCLK	A6, A9, Y6, Y9	—	1.8V supply for RX ADC clocks.
VDD1P2TXENC	D17, U17	—	1.2V supply for DAC encoder.
VDD1P2TXCLK	A20, D20, U20, Y20	—	1.2V supply for DAC clock.
VDD1P8TX	E20, H20, N20, T20	—	1.8V supply for DAC.
VDD1P8TXDAC	G17, H17, N17, P17	—	1.8V supply for DAC.
VDD1P8GPIO	H6, N6	—	1.8V supply for GPIO.
VDDA1P8	F3, F4, H3, H4, R3, R4, N3, N4	—	SerDes analog 1.8V power supply.
VDDT0P9	D3, D4, U3, U4	—	SerDes digital 0.9V power supply.
GROUNDS			
DGND	J5, J6, J7, J8, J9, J10, J11, J12, M5, M6, M7, M8, M9, M10, M11, M12	—	Digital core ground
VSSGPIO	H5, N5	—	GPIO ground.
VSSFB	B14, B15, B16, B17, C14, V14, W14, W15, W16, W17	—	Ground for FB ADC supply.
VSSFBCLK	A18, B18, W18, Y18	—	Ground for FB ADC 1.8V clock supply.
GND_ESD	D7, D8, J13, M13, U7, U8	—	Ground for ESD protection circuits.
VSSRX	B7, B8, B10, B11, B12, C12, D12, B13, C13, D13, W7, W8, W10, W11, W13, U12, V12, W12, U13, V13	—	Ground for RX ADC.
VSSRXCLK	A5, B5, B6, B9, C7, C8, W5, W6, W9, Y5, V7, V8	—	Ground for RX ADC clocks.
VSSTX	B19, C17, C18, C19, D18, E18, E19, F17, F18, F19, G18, G19, H18, H19, J20, M20, N18, N19, P18, P19, R17, R18, R19, T18, T19, U18, V17, V18, V19, W19	—	Ground for TX DAC.
VSSTXENC	E16, E17, T16, T17	—	Ground for TX DAC encoder.
VSSTXCLK	A19, D19, U19, Y19	—	Ground for TX DAC clock.
VSSPLL	M19	—	Ground for PLL.
VSSPLLFBCML	J16, M16	—	Ground for FB ADC clock.

Table 4-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE(1)	DESCRIPTION
VSSPLLCLKREF	J18, M18	—	Ground for CLKREF PLL.
VSSPLLRXCML	J17, M17	—	Ground for RX ADC clock.
VSST	A1, A4, B2, B3, B4, C2, D1, D2, E2, F2, G1, G2, H2, J2, K1, K4, L1, L4, M2, N2, P1, P2, R2, T2, U1, U2, V2, W2, W3, W4, Y1, Y4	—	SerDes ground.
OTHERS			
IFORCE	G5	—	Reserved for TI use only. Do not connect.
PLL_LDOUT	J19	—	Connect with 100nF capacitor to GND
SerDes_AMUX1	K3	—	Analog test pin for SerDes lane 1-4, can be left floating
SerDes_AMUX2	L3	—	Analog test pin for SerDes lane 5-8, can be left floating
VSENSE	P5	—	Process test: sense voltage (TI use only). Do not connect.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	–0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	–0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVCO, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	–0.5	2.1	V
Pin Volatge Range	{1/2/3/4}RXIN+/-	–0.5	VDDRX1P8+0.3	V
	1FBIN+/-, 2FB+/-	–0.5	VDDFB1P8+0.3	V
	{1/2/3/4}TXOUT+/-	–0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	–0.3	1.4	V
	{1:8}SRX+/-	–0.3	1.4	V
	{1:8}STX+/-	–0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	–0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	–0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	–0.3	VDDA1P8+0.3	V
P_{MAX}(xRXIN+/-)	f_{IN} = 5 MHz, DSA = 20dB		19.7	dBm
	f_{IN} = 30 MHz, DSA = 20dB		17.8	
	f_{IN} = 410 MHz, DSA = 20dB		17.6	
	f_{IN} = 830 MHz, DSA = 20dB		16.7	
	f_{IN} = 1760 MHz, DSA = 20dB		17.0	
	f_{IN} = 2610 MHz, DSA = 20dB		18	
	f_{IN} = 3610 MHz, DSA = 20dB		18.5	
	f_{IN} = 4910 MHz, DSA = 20dB		19.3	
Peak Input Current	any input		20	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/TXENC/PLL/PLLVCO/FB/FBCLK/GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T_A	Ambient temperature	–40		85	°C
T_J	Operating Junction Temperature			110[1]	°C
	Maximum Operating Junction Temperature	125			°C

(1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to SBAA403 application note for additional details

5.4 Thermal Information AFE79xx

THERMAL METRIC[1]		17mmx17mm FC-BGA	UNIT
		400 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.85	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.12	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Transmitter Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC_{RES}	DAC resolution			14		bits
f_{RFout}	RF output frequency range	f_{DAC} = 12 GSPS, 1st Nyquist	5		6000	MHz
		f_{DAC} = 9 GSPS, 1st Nyquist	5		4500	
		f_{DAC} = 9 GSPS, 2nd Nyquist	4500		7400	
		f_{DAC} = 6 GSPS, 1st Nyquist	5		3000	
		f_{DAC} = 6 GSPS, 2nd Nyquist	3000		6000	
P_{max_FS}	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 10 MHz, f_{DAC} = 6GSPS, -0.1dBFS		6.5		dBm
		f_{out} = 30 MHz, f_{DAC} = 6GSPS, -0.1dBFS		6.5		dBm
		f_{out} = 400 MHz, f_{DAC} = 6GSPS, -0.1dBFS		5.6		dBm
		f_{out} = 850 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		4.3		dBm
		f_{out} = 1800 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		3.2		dBm
		f_{out} = 2600 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS		2.3		dBm
		f_{out} = 3500 MHz, -0.5dBFS		2.9		dBm
		fout = 4900 MHz, -0.5dBFS		-0.6		dBm
		f_{out} = 3500 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		-2.3		dBm
		f_{out} = 4900 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		-3.4		dBm
		f_{out} = 4900 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS, straight mode		-3.9		dBm
R_{TERM}	Output termination resistor	Default setting		100		Ω
ATT_{range}	DSA Attenuation range			40		dB
ATT_{step}	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL) (2)	0 < Atten < 40dB, after calibration		±0.1		dB
		0 < Atten < 40dB, before calibration		±0.2		
ATT_{step}	DSA Gain Steps Phase accuracy, any 8dB range(2)	f_{out} = 30MHz		±1		deg
		f_{out} = 400MHz		±1		deg
		f_{out} = 850MHz		±1		deg
		f_{out} = 1800MHz		±1		deg
		f_{out} =2600MHz		±1		deg
		f_{out} = 3500MHz		±1		
		f_{out} = 4900MHz		±1		deg
G_{flat}	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F_{out} < 4.9G		1.2		

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion	f_{DAC} =6 GSPS, f_{out} = 5MHz ±1MHz, -7dBFS each tone		-48		dBc
		f_{DAC} =6 GSPS, f_{out} = 30MHz ±1MHz, -7dBFS each tone		-47		dBc
		f_{DAC} =6 GSPS, f_{out} = 400MHz ±2MHz, -7dBFS each tone		-51		dBc
		f_{out} = 850MHz ±10MHz, -7dBFS each tone		-61		dBc
		f_{out} = 1800MHz ±10MHz, -7dBFS each tone		-62		dBc
		f_{out} = 2600MHz ±10MHz, -7dBFS each tone		-64		dBc
		f_{out} = 3500MHz ±10MHz, -7dBFS each tone		-63		dBc
		f_{out} = 4900MHz ±10MHz, -7dBFS each tone		-64		dBc
		f_{out} = 5MHz ±1MHz, -13dBFS each tone		-72		dBc
		f_{DAC} =6 GSPS, f_{out} = 30MHz ±1MHz, -13dBFS each tone		-71		dBc
		f_{DAC} =6 GSPS, f_{out} = 400MHz ±2MHz, -13dBFS each tone		-72		dBc
		f_{out} = 850MHz ±10MHz, -13dBFS each tone		-73		dBc
		f_{out} = 1800MHz ±10MHz, -13dBFS each tone		-75		dBc
		f_{out} = 2600MHz ±10MHz, -13dBFS each tone		-79		dBc
		f_{out} = 3500MHz ±10MHz, -13dBFS each tone		-77		dBc
		f_{out} = 4900MHz ±10MHz, -13dBFS each tone		-77		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	f_{out} = 30 MHz, f_{DAC} = 6000 MSPS, interleave mode, 20Gbps SerDes rate		45		dBc
		f_{out} = 400 MHz, f_{DAC} = 6000 MSPS, interleave mode, 20Gbps SerDes rate		48		dBc
		f_{out} = 850 MHz, f_{DAC} = 11796.48 MSPS		62		dBc
		f_{out} = 1800 MHz, f_{DAC} = 11796.48 MSPS		56		dBc
		f_{out} = 2600 MHz, f_{DAC} = 11796.48 MSPS		39		dBc
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS		42		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		60		dBc

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_S/2$ - f_{OUT}	Interleaving Image	f_{DAC} = 5898.24MSPS, interleave mode		-47		dBc
		f_{DAC} = 8847.36 MSPS, interleave mode		-43		dBc
		f_{DAC} = 11796.48MSPS, interleave mode		-43		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-72		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-75		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-73		dBc
		f_{out} = 400 MHz		-46		dBc
		f_{out} = 850 MHz		-65		dBc
		f_{out} = 1800 MHz		-68		dBc
		f_{out} = 2600 MHz		-47		dBc
		f_{out} = 3500 MHz		-59		dBc
		f_{out}= 4900 MHz		-48		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-74		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-67		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-58		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-69		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-59		dBc
HD3	3rd Harmonic Distortion (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-46		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-48		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-49		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz		-49		dBc
		f_{out} = 850 MHz		-56		dBc
		f_{out} = 1800 MHz		-58		dBc
		f_{out} = 2600 MHz		-60		dBc
		f_{out} = 3500 MHz		-63		dBc
		f_{out}= 4900 MHz		-66		dBc
		f_{DAC} =6 GSPS, f_{out} = 5 MHz, A_{OUT}=-12dBFS		-83		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz, A_{OUT}=-12dBFS		-83		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz, A_{OUT}=-12dBFS		-82		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz, A_{OUT}=-12dBFS		-79		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-84		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-79		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-84		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-88		dBc

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-58		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-60		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-61		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz		-50		dBc
		f_{out} = 850 MHz		-85		dBc
		f_{out} = 1800 MHz		-90		dBc
		f_{out} = 2600 MHz		-84		dBc
		f_{out} = 3500 MHz		-86		dBc
		f_{out}= 4900 MHz		-87		dBc
		f_{DAC} =6 GSPS, f_{out} = 5 MHz, A_{OUT}=-12dBFS		-92		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz, A_{OUT}=-12dBFS		-94		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz, A_{OUT}=-12dBFS		-93		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz, A_{OUT}=-12dBFS		-85		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-89		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-92		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-88		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-89		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	f_{DAC} =6 GSPS, f_{out} = 400 MHz		87		dBc
		f_{out} = 850 MHz, f_{DAC} = 11796.48 MSPS		84		dBc
		f_{out} = 1800 MHz, f_{DAC} = 11796.48 MSPS		78		dBc
		f_{out} = 2600 MHz, f_{DAC} = 11796.48 MSPS		80		dBc
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS		81		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		74		dBc
f_S/4	Fixed Spur	f_{DAC} = 5898.24MSPS, f_{OUT}=f_{DAC}/4-50MHz		-95		dBFS
		f_{DAC} = 8847.36MSPS, f_{OUT}=f_{DAC}/4-50MHz		-88		dBFS
		f_{DAC} = 11796.48MSPS, f_{OUT}=f_{DAC}/4-50MHz		-76		dBFS
f_S/2	Fixed Spur	f_{DAC} = 5898.24MSPS, f_{OUT}=f_{DAC}/2-50MHz		-52		dBFS
		f_{DAC} = 8847.36MSPS, f_{OUT}=f_{DAC}/2-50MHz		-45		dBFS
		f_{DAC} = 11796.48 MSPS, f_{OUT}=f_{DAC}/2-50MHz		-49		dBFS

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$3*f_S/4$	Fixed Spur	2nd Nyquist, f_{DAC} = 5898.24MSPS, f_{OUT}=3*f_{DAC}/4-50MHz		-82		dBFS
		2nd Nyquist, f_{DAC} = 8847.36MSPS, f_{OUT}=3*f_{DAC}/4-50MHz		-75		dBFS
		2nd Nyquist, f_{DAC} = 11796.48MSPS, f_{OUT}=3*f_{DAC}/4-50MHz		-49		dBFS
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 0.85 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-70		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-62		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-51		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 1.8425 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-71		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-61		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-50		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-72		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-60		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-49		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-71		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-65		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-58		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-47		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-69		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-64		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-58		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-47		dBc

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-65		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-59		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-53		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-41		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-63		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-56		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-49		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-38		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-63		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-56		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-51		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-41		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	F_{out} =0.85 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.16		%
		F_{out} =1.8425 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.21		%
		F_{out} =2.6 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.24		%
		F_{out} =3.5 GHz, P_{OUT}=-13dBFs		0.27		%
		F_{out} =4.9 GHz, P_{OUT}=-13dBFs		0.38		%
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 5 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-148		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-143		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-139		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-129		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 30 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-154		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-146		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-142		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-132		dBFS/Hz

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 100 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-158		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-150		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-146		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-136		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 400 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-160		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-153		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-150		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-139		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 0.85 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-158.8		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-152.7		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-148.7		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-137.9		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 1.8 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-157.9		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-151.3		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-145.6		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-134.8		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 2.6 GHz	Atten=0dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-158.3		dBFS/Hz
		Atten=20dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-151.6		dBFS/Hz
		Atten=28dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-144.9		dBFS/Hz
		Atten=39dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-134.0		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-158.2		dBFS/Hz
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-150.9		dBFS/Hz
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-144.4		dBFS/Hz
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-133.4		dBFS/Hz

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-154.6		dBFS/Hz
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-147.0		dBFS/Hz
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-140.7		dBFS/Hz
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-129.9		dBFS/Hz
S22	Output Return Loss, +/- fc * 10%	with matching		-12		dB
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT(1)	f_{out} = 10 MHz, f_{DAC} =6000MSPS, straight mode(3)		-96		dB
		f_{out} = 30 MHz, f_{DAC} = 6000MSPS, straight mode(3)		-97		dB
		f_{out} = 100 MHz, f_{DAC} = 6000MSPS, straight mode(3)		-102		dB
		f_{out} = 400 MHz, f_{DAC} = 6000MSPS, straight mode(4)		-85		dB
		f_{out} = 900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-80		dB
		f_{out} = 1850 MHz, f_{DAC} = 8847.36MSPS, straight mode		-77		dB
		f_{out} = 2600 MHz, f_{DAC} = 8847.36MSPS, straight mode		-64		dB
		f_{out} = 3500 MHz, f_{DAC} = 8847.36MSPS, straight mode		-61		dB
		f_{out}= 4900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-60		dB
Isolation	Far Channel: 1/2TXOUT to 3/4TXOUT	f_{out} = 10 MHz, f_{DAC} =6000MSPS, straight mode(3)		-104		dB
		f_{out} = 30 MHz, f_{DAC} = 6000MSPS, straight mode(3)		-100		dB
		f_{out} = 100 MHz, f_{DAC} = 6000MSPS, straight mode(3)		-105		dB
		f_{out} = 400 MH, f_{DAC} = 6000MSPS, straight mode(4)		-97		dB
		f_{out} = 900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-90		dB
		f_{out} = 1850 MHz, f_{DAC} = 8847.36MSPS, straight mode		-91		dB
		f_{out} = 2600 MHz, f_{DAC} = 8847.36MSPS, straight mode		-93		dB
		f_{out} = 3500 MHz, f_{DAC} = 8847.36MSPS, straight mode		-94		dB
		f_{out}= 4900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-83.2		dB

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN_{TXADD}	Additive Phase Noise External Clock Mode (5)	f_{out} = 3.7GHz, f_{OFFSET} = 100Hz		-97		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 1kHz		-106		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 10kHz		-117		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 100kHz		-128		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 1MHz		-138		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 10MHz		-144		dBc/Hz

(1) Measured with differential 100 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
(2) After DSA calibration procedure
(3) measured with 1µH DC feed inductor
(4) measured with 0.39µH DC feed inductor
(5) Input clock phase noise subtracted.

5.6 RF ADC Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC_{RES}	ADC resolution			14		bits
F_{RFin}	RF input frequency range		5		7400	MHz
$P_{FS\_CW,min}$	Min Full scale input power, at device pins (1)	f_{IN} = 5 MHz, DSA=0dB, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-0.4		dBm
		f_{IN} = 30 MHz, DSA=0dB, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-2.2		dBm
		f_{IN} = 410 MHz, DSA=0dB, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 12		-2.5		dBm
		f_{IN} = 830 MHz, DSA=0dB		-2.9		dBm
		f_{IN} = 1760 MHz, DSA=0dB		-2.8		dBm
		f_{IN} = 2610 MHz, DSA=0dB		-1.8		dBm
		f_{IN} = 3610 MHz, DSA=0dB		-0.4		dBm
		f_{IN} = 4910 MHz, DSA=0dB		0.1		dBm
R_{TERM}	Input reference impedance			100.0		Ω
ATT_{range}	DSA Attenuation range			25.0		dB
ATT_{step}	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F_{in}=3610MHz, after calibration		0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=3610MHz, after calibration		0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=4910MHz, after calibration		1.8		deg
G_{flat}	Gain flatness	Measured Over 80MHz BW		0.2		dB
		Measured Over 200MHz BW		0.5		dB
		Measured Over 400MHz BW		1.1		dB

5.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Density (3) (small signal = -30dBFS)	f_{IN} = 5 MHz, DSA = 3dB, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-147.1		dBFS/Hz
		f_{IN} = 30 MHz, DSA = 3dB, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-150.7		dBFS/Hz
		f_{IN} = 410 MHz, DSA = 3dB, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-155.4		dBFS/Hz
		f_{IN} = 830 MHz, DSA = 3dB		-156.2		dBFS/Hz
		f_{IN} = 1760 MHz, DSA = 3dB		-156.0		dBFS/Hz
		f_{IN} = 2610 MHz, DSA = 3dB		-155.4		dBFS/Hz
		f_{IN} = 3610 MHz, DSA = 3dB		-155.1		dBFS/Hz
		f_{IN} = 4910 MHz, DSA = 3dB		-155.1		dBFS/Hz
		f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48, 3<=Atten<=22		-147.8		dBFS/Hz
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24, 3<=Atten<=22		-151.5		dBFS/Hz
		f_{IN} = 410 MHz, 3<=Atten<=22, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-156.6		dBFS/Hz
		f_{IN} = 830 MHz, 3<=Atten<=22		-156.0		dBFS/Hz
		f_{IN} = 1760 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f_{IN} = 2610 MHz, 3<=Atten<=25		-155.7		dBFS/Hz
		f_{IN} = 3610 MHz, 3<=Atten<=25		-155.4		dBFS/Hz
		f_{IN} = 4910 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
NF_{min}	Noise Figure min DSA Atten=0 - 3dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		29.4		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		24.5		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		19.3		dB
		f_{IN} = 830 MHz		19.1		dB
		f_{IN} = 1760 MHz		19.0		dB
		f_{IN} = 2610 MHz		20.9		dB
		f_{IN} = 3610 MHz		22.8		dB
		f_{IN} = 4910 MHz		22.4		dB

5.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise Figure(4) DSA Atten=4dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		30.6		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		25.1		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		20.1		dB
		f_{IN} = 830 MHz		20.0		dB
		f_{IN} = 1760 MHz		20.6		dB
		f_{IN} = 2610 MHz		21.9		dB
		f_{IN} = 3610 MHz		23.5		dB
		f_{IN} = 4910 MHz		22.3		dB
NF_{max}	Noise Figure DSA Atten=20dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		45.9		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		40.2		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		35.0		dB
		f_{IN} = 830 MHz		34.7		dB
		f_{IN} = 1760 MHz		35.2		dB
		f_{IN} = 2610 MHz		36.0		dB
		f_{IN} = 3610 MHz		37.3		dB
		f_{IN} = 4910 MHz		37.6		dB
IMD3	3rd order intermodulation 2 tones at at f_{IN} ± 10MHz -7dBFS each tone	f_{IN} = 30±1 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-82		dBc
		f_{IN} = 400MHz and 405MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-75		dBc
		f_{IN} = 840 MHz		-82		dBc
		f_{IN} = 1770 MHz		-84		dBc
		f_{IN} = 2610 MHz		-74		dBc
		f_{IN} = 3610 MHz		-77		dBc
		f_{IN} = 4920 MHz		-76		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		78		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		100		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		94		dBFS
		f_{IN} = 830 MHz		88		dBFS
		f_{IN} = 1760 MHz		81		dBFS
		f_{IN} = 2610 MHz		88		dBFS
		f_{IN} = 3610 MHz		84		dBFS
		f_{IN} = 4910 MHz		79		dBFS

5.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion A_{IN} = -3 dBFS(2)	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-84		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-90		dBFS
		f_{IN} = 830 MHz		-86		dBFS
		f_{IN} = 1760 MHz		-90		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-87		dBFS
		f_{IN} = 4910 MHz		-84		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-78		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-96		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-94		dBFS
		f_{IN} = 830 MHz		-80		dBFS
		f_{IN} = 1760 MHz		-85		dBFS
		f_{IN} = 2610 MHz		-86		dBFS
		f_{IN} = 3610 MHz		-78		dBFS
		f_{IN} = 4910 MHz		-75		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-94		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-94		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-94		dBFS
		f_{IN} = 830 MHz		-88		dBFS
		f_{IN} = 1760 MHz		-81		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-84		dBFS
		f_{IN} = 4910 MHz		-82		dBFS
SFDR	Spurious Free Dynamic Range A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		101		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		105		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		95		dBFS
		f_{IN} = 830 MHz		89		dBFS
		f_{IN} = 1760 MHz		89		dBFS
		f_{IN} = 2610 MHz		95		dBFS
		f_{IN} = 3610 MHz		87		dBFS
		f_{IN} = 4910 MHz		90		dBFS

5.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion(2) A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-104		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-104		dBFS
		f_{IN} = 830 MHz, with board trim		-79		dBFS
		f_{IN} = 1760 MHz, with board trim		-102		dBFS
		f_{IN} = 2610 MHz, with board trim		-100		dBFS
		f_{IN} = 3610 MHz, with board trim		-101		dBFS
		f_{IN} = 4910 MHz, with board trim		-99		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-103		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-84		dBFS
		f_{IN} = 381 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 830 MHz		-95		dBFS
		f_{IN} = 1760 MHz		-95		dBFS
		f_{IN} = 2610 MHz		-98		dBFS
		f_{IN} = 3610 MHz		-97		dBFS
		f_{IN} = 4910 MHz		-94		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-104		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-105		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-95		dBFS
		f_{IN} = 830 MHz		-89		dBFS
		f_{IN} = 1760 MHz		-89		dBFS
		f_{IN} = 2610 MHz		-95		dBFS
		f_{IN} = 3610 MHz		-90		dBFS
		f_{IN} = 4910 MHz		-90		dBFS
RX-RX/FB Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-98		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-98		dB
		f_{IN} = 400 MHz		-88		dB
		f_{IN} = 830 MHz		-77		dB
		f_{IN} = 1760 MHz		-71		dB
		f_{IN} = 2610 MHz		-74		dB
		f_{IN} = 3610 MHz		-77		dB
		f_{IN} = 4910 MHz		-65		dB

5.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX-RX Isolation	1TXOUT to 1RXIN 3TXOUT to 2RXIN	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-105		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-101		dB
		f_{IN} = 400 MHz		-99		dB
		f_{IN} = 830 MHz		-86		dB
		f_{IN} = 1760 MHz		-87		dB
		f_{IN} = 2610 MHz		-84		dB
		f_{IN} = 3610 MHz		-82		dB
		f_{IN} = 4910 MHz		-82		dB

(1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
(2) After HD2 trim on specific printed circuit board.
(3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
(4) NF increase 1dB per DSA 1dB above DSA = 3dB

5.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f_{DAC} = f_{VCO}, f_{OUT} = f_{DAC}/4, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO1}	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f_{VCO2}	VCO2 min frequency				8.848	GHz
	VCO2 max frequency		9.216			GHz
f_{VCO3}	VCO3 min frequency				9.8304	GHz
	VCO3 max frequency		10.24			GHz
f_{VCO4}	VCO4 min frequency				11.7965	GHz
	VCO4 max frequency		12.288			GHz
DIV_{DAC}	DAC sample rate divider			1, 2 or 3		
DIV_{RXADC}	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN_{VCO}	Closed Loop Phase Noise F_{PLL} = 11.79848 GHz F_{REF}=491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		–141		dBc/Hz
	Closed Loop Phase Noise F_{PLL}=8.84736 GHz F_{REF}=491.52MHz	600kHz		-114		dBc/Hz
		800kHz		–118		dBc/Hz
		1MHz		–120		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–135		dBc/Hz
		50MHz		–142		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 9.8403 GHz F_{REF}=491.52MHz	600kHz		–113		dBc/Hz
		800kHz		–116		dBc/Hz
		1MHz		–119		dBc/Hz
		1.8MHz		–125		dBc/Hz
		5MHz		–134		dBc/Hz
		50MHz		–140		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 7.86432GHz F_{REF}=491.52MHz	600kHz		–116		dBc/Hz
		800kHz		–119		dBc/Hz
		1MHz		–122		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–136		dBc/Hz
		50MHz		–143		dBc/Hz
F_{rms}	Clock PLL integrated phase error[(1)]	f_{PLL}=11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f_{PLL}=8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f_{PLL}=9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f_{PFD}	PFD frequency		100		500	MHz
PN_{pll_flat}	Normalized PLL flat Noise	f_{VCO} = 11796.48MHz		–226.5		dBc/Hz
F_{REF}	Input Clock frequency		0.1		12	GHz
V_{SS}	Input Clock level		0.6		1.8	Vppdiff

5.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{DAC} = f_{VCO}$, $f_{OUT} = f_{DAC}/4$, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Coupling				AC Coupling Only		
	REFCLK input impedance(2)	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

(1) Single Sideband, not including the reference clock contribution
(2) Refer to S11 data available from TI for impedance vs frequency

5.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs [8:1]SRX+/-						
V_{SRDIFF}	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V_{SRCOM}	SerDes Input Common Mode			400		mV
Z_{SRdiff}	SerDes Internal Differential Termination[1]			100		Ω
F_{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance[2]	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
CML SerDes Outputs [8:1]STX+/-						
V_{STDIFF}	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V_{STCOM}	SerDes Output Common Mode		0.4	0.45	0.55	V
Z_{STdiff}	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V_{IH}	High-Level Input Voltage		0.6×VDD1P8GPIO			V
V_{IL}	Low-Level Input Voltage				0.4×VDD1P8GPIO	V
I_{IH}	High-Level Input Current		–250		250	µA
I_{IL}	Low-Level Input Current		–250		250	µA
C_L	CMOS input capacitance			2		pF
V_{OH}	High-Level Input Voltage		VDD1P8GPIO–0.2			V
V_{OL}	Low-Level Input Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
$F_{SYSREFMAX}$	SYSREF Input Frequency Maximum			40		MHz
$V_{SWINGSRMAX}$	SYSREF Input Swing Maximum			1.8		Vppdiff[3]
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} < 500MHz		0.3		Vppdiff[3]
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} > 500MHz		0.6		Vppdiff[3]
$V_{COMSRMAX}$	SYSREF Input Common Mode Voltage Maximum			0.8		V
$V_{COMSRMIN}$	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z_T	Input termination	differential		100 [1]		Ω
C_L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V_{ICOM}	Input Common Voltage			1.2		V
V_{ID}	Differential Input Voltage swing			450		Vppdiff[3]
Z_T	Input termination	differential		100		Ω
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V_{OCOM}	Output Common Voltage			1.2		V

5.8 Digital Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	Differential Output Voltage swing			500		Vppdiff(3)
Z_T	Internal Termination			100		Ω

(1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
(2) Loss tolerance is bump to bump from STX to SRX
(3) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

5.9 Power Supply Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 500MSPS, RX Output Rate = 500MSPS, f_{DAC} = 9000MSPS interleave mode; f_{ADC} = 3000MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 20Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4T4R - TDD with TX 75%, RX 25% TX Dual Band: 72x Int, TX Rate 125 MSPS RX Dual Band: 24x Dec, RX Rate 125 MSPS f_{DAC} = 9000MSPS, f_{OUT}=f_{IN}= 1.9, 2.6 GHz f_{ADC} = 3000MSPS JESD: 8/10 coding, 20Gbps TX: 2-16-16-1, RX: 2-16-16-1		588		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			439		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			74		mA
I_{VDD1P2}	Group 2: VDD1P2FB + VDD1P2RX + VDD1P2TXCLK + VDD1P2TXENC + VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			1191		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1928		mA
P_{diss}	Power Dissipation			5196		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 4T4R - FDD TX Dual Band: 96x Int, TX Rate 125 MSPS RX Dual Band: RX 24x, RX Rate 125 MSPS f_{DAC} = 12 GSPS, f_{TX} = 1.85 GHz f_{ADC} = 3 GSPS, f_{RX} = 1.75 GHz JESD: 8/10 coding, 20Gbps TX: 2-16-16-1, RX: 2-16-16-1		1146		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			553		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			78		mA
I_{VDD1P2}	Group 2: VDD1P2FB + VDD1P2RX + VDD1P2TXCLK + VDD1P2TXENC + VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			2152		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3217		mA
P_{diss}	Power Dissipation			8757		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4T4R - FDD TX Single Band: 96x Int, TX Rate 125 MSPS RX Single Band: RX 24x, RX Rate 125 MSPS f_{DAC} = 12 GSPS, f_{TX} = 1.85 GHz f_{ADC} = 3 GSPS, f_{RX} = 1.75 GHz JESD: 8/10 coding, 20Gbps TX: 1-8-16-1, RX: 1-8-16-1		1146		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			546		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			78		mA
I_{VDD1P2}	Group 2: VDD1P2FB + VDD1P2RX + VDD1P2TXCLK + VDD1P2TXENC + VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			2144		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2904		mA
P_{diss}	Power Dissipation			8444		mW

5.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 500MSPS, RX Output Rate = 500MSPS, f_{DAC} = 9000MSPS interleave mode; f_{ADC} = 3000MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 20Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 4T4R - FDD TX Single Band: 24x Int, TX Rate 500 MSPS RX Single Band: RX 6x, RX Rate 500 MSPS f_{DAC} = 12 GSPS, f_{TX} = 1.85 GHz f_{ADC} = 3 GSPS, f_{RX} = 1.75 GHz JESD: 8/10 coding, 20Gbps TX: 4-8-4-1, RX: 4-8-4-1		1147		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			700		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			78		mA
I_{VDD1P2}	Group 2: VDD1P2FB + VDD1P2RX + VDD1P2TXCLK + VDD1P2TXENC + VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			2150		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3228		mA
P_{diss}	Power Dissipation			9031		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: same configuration as Mode 4 Sleep Mode. SLEEP pin is pull high.		24		mA
I_{VDD1P8}	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			339		mA
I_{VDD1P8}	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			12		mA
I_{VDD1P2}	Group 2: VDD1P2FB + VDD1P2RX + VDD1P2TXCLK + VDD1P2TXENC + VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			58		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			282		mA
P_{diss}	Power Dissipation			1004		mW

5.10 Timing Requirements

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_{s(SYSREF)}$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{h(SYSREF)}$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_{s(SENB)}$	Setup Time, SENB to Rising Edge of SCLK			15	ns
$t_{h(SENB)}$	Hold Time, SENB after last Rising Edge of SCLK [(1)]			5 + t_{SCLK}	ns
$t_{s(SDIO)}$	Setup Time, SDIO valid to Rising Edge of SCLK			15	ns
$t_{h(SDIO)}$	Hold Time, SDIO valid after Rising Edge of SCLK			5	ns
$t_{(SCLK)\_W}$	Minimum SCLK period: registers write			25	ns
$t_{(SCLK)\_R}$	Minimum SCLK period: registers read			50	ns
$t_{d(data\_out)}$	Minimum Data Output delay after Falling Edge of SCLK			0	ns
	Maximum Data Output delay after Falling Edge of SCLK			15	ns
t_{RESET}	Minimum RESETZ Pulse Width		1		ms

(1) $\overline{\text{SDEN}}$ need to be held one more extra clock cycle with the last SCLK edge

5.11 Switching Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

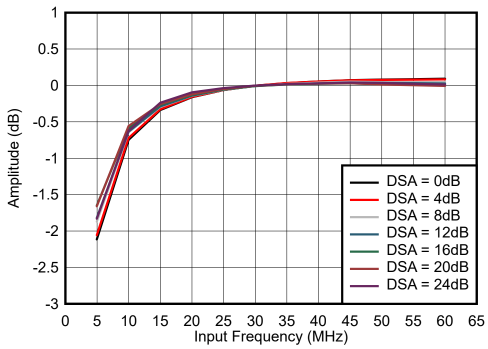
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX Channel Latency						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
t_{JESDTX}	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles(1)
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
RX Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t_{JESDRX}	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles(1)
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=2-8-8-1, 368.64 MSPS, 8x Decimation, Serdes rate = 16.22Gbps (JESD204C)		118		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
FB Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t_{JESDFB}	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles(1)
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

(1) Interface clock cycles is the period of the digital interface clock rate, e.g. 1GSPS = 1ns.

5.12 Typical Characteristics

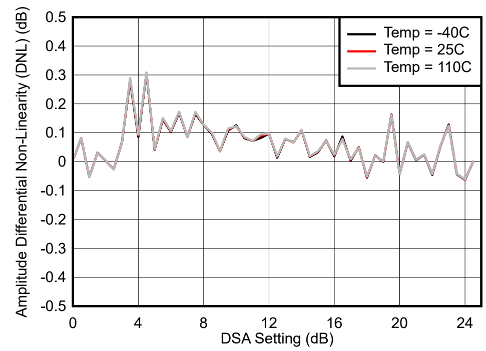
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



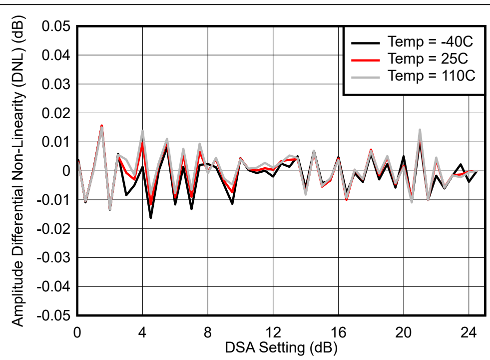
Normalized to 30 MHz

Figure 5-1. RX In-Band Gain Flatness, f_{IN} = 30 MHz



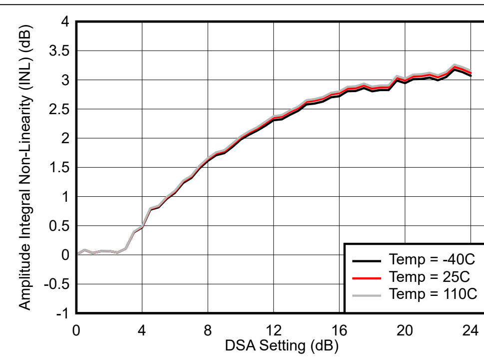
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 5-2. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 5-3. RX Calibrated Differential Amplitude Error vs DSA Setting at 30 MHz

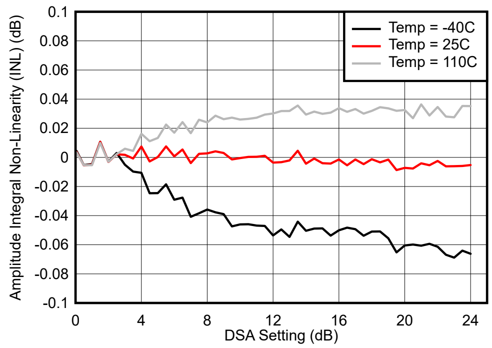


Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 5-4. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 30 MHz

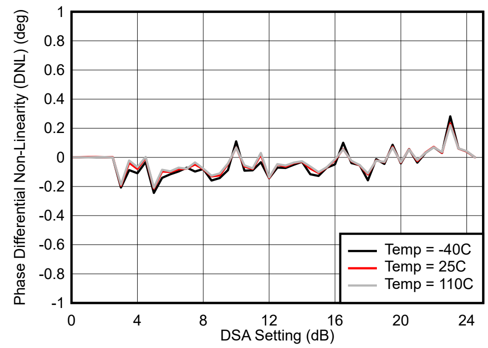
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



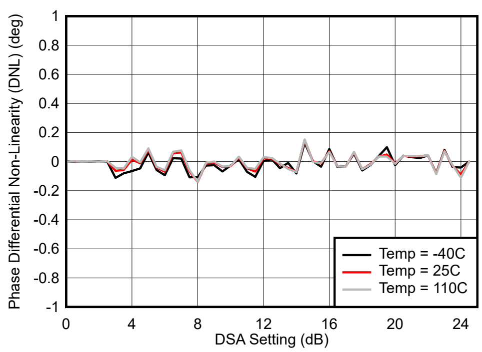
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 5-5. RX Calibrated Integrated Amplitude Error vs DSA Setting at 30 MHz



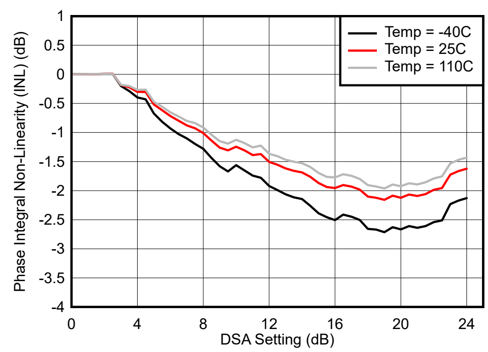
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 5-6. RX Uncalibrated Differential Phase Error vs DSA Setting at 30 MHz



Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 5-7. RX Calibrated Differential Phase Error vs DSA Setting at 30 MHz

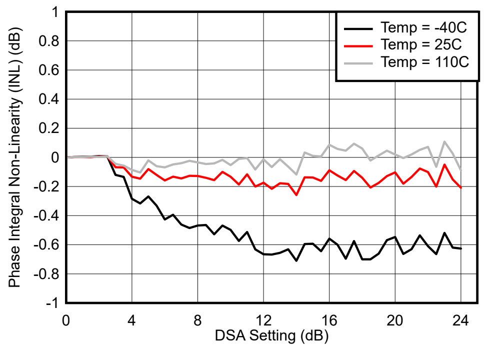


Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-8. RX Uncalibrated Integrated Phase Error vs DSA Setting at 30 MHz

5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

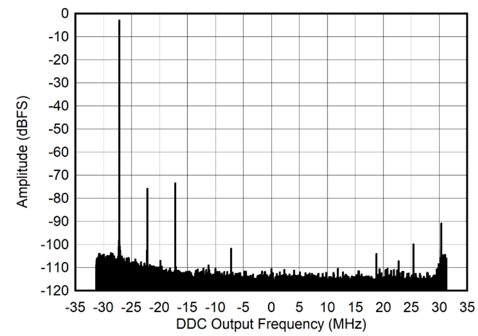
Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



With 0.8 GHz matching

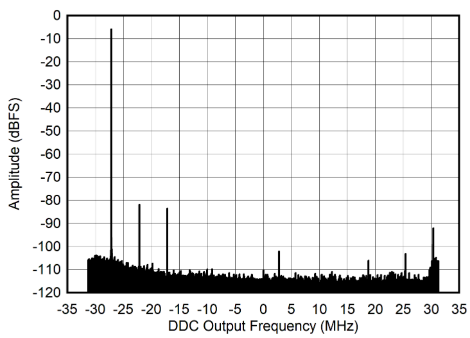
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-9. RX Calibrated Integrated Phase Error vs DSA Setting at 30 MHz



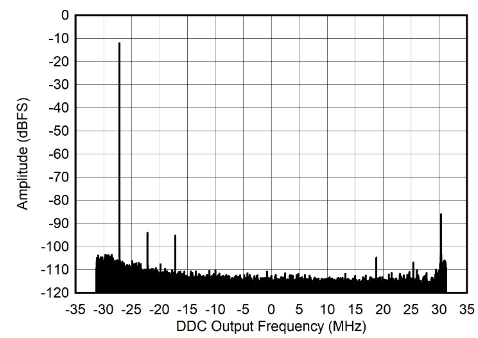
A_{IN} = -3 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-10. RX Output FFT at 5 MHz



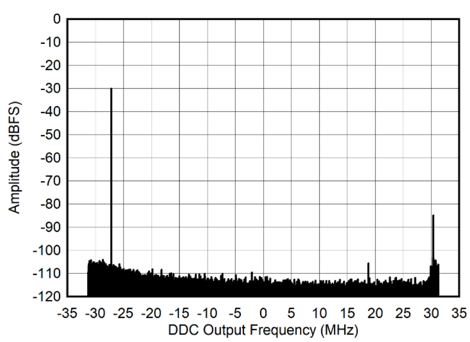
A_{IN} = -6 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32. , Decimate by 24x

Figure 5-11. RX Output FFT at 5 MHz



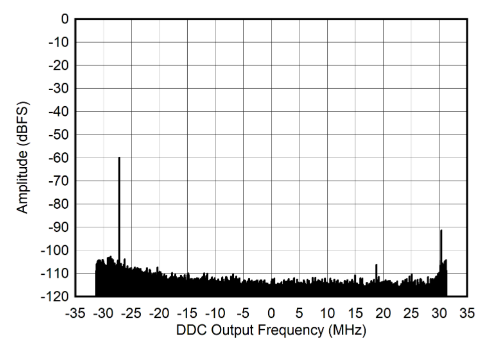
A_{IN} = -12 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-12. RX Output FFT at 5 MHz



A_{IN} = -30 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-13. RX Output FFT at 5 MHz

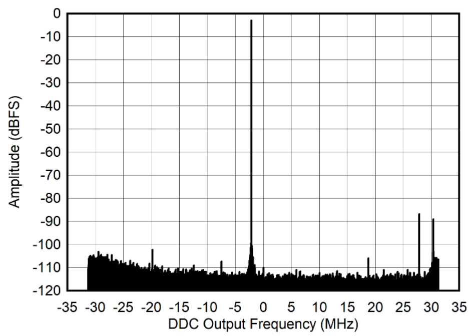


A_{IN} = -60 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-14. RX Output FFT at 5 MHz

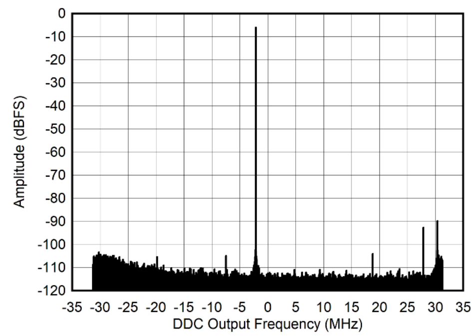
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



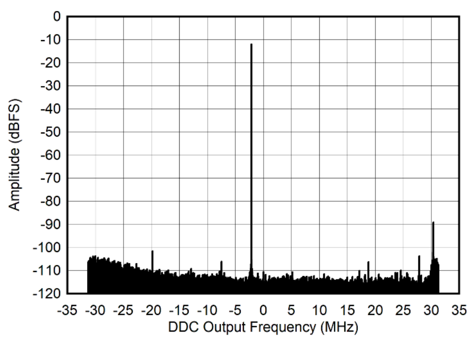
A_{IN} = -3 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-15. RX Output FFT at 30 MHz



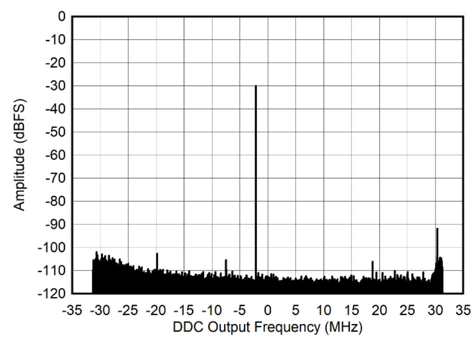
A_{IN} = -6 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-16. RX Output FFT at 30 MHz



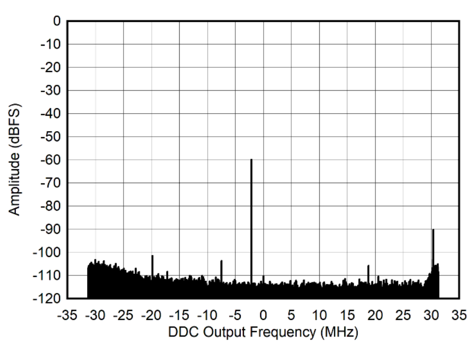
A_{IN} = -12 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-17. RX Output FFT at 30 MHz



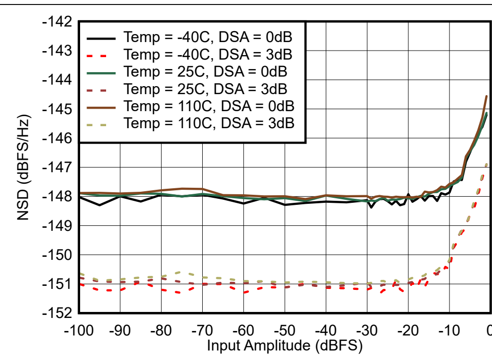
A_{IN} = -30 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-18. RX Output FFT at 30 MHz



A_{IN} = -60 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-19. RX Output FFT at 30 MHz

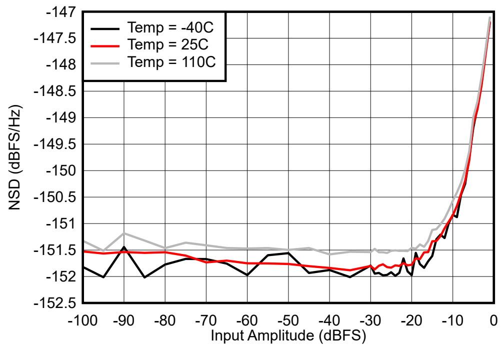


f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-20. NSD vs Input Amplitude at 30 MHz with DSA = 0 and 3dB

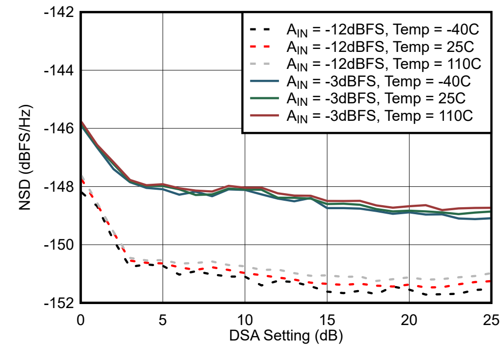
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



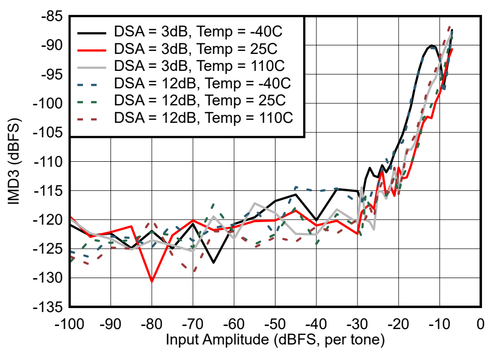
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-21. NSD vs Input Amplitude at 30 MHz with DSA = 12



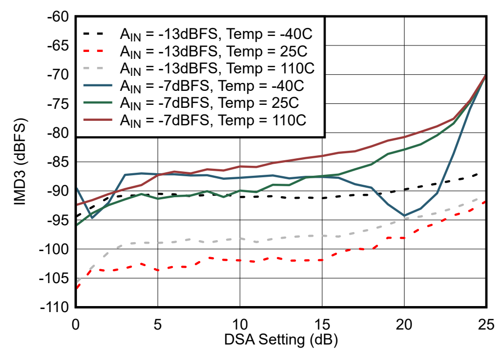
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-22. NSD vs DSA Attenuation at 30 MHz



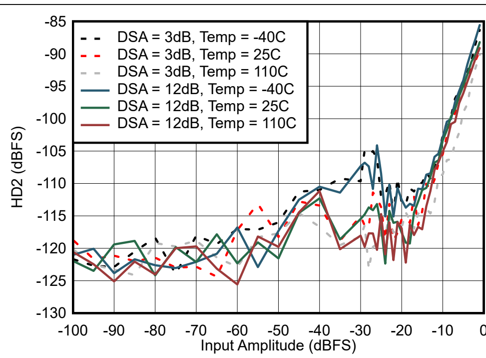
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-23. IMD3 vs Input Amplitude at 30 MHz



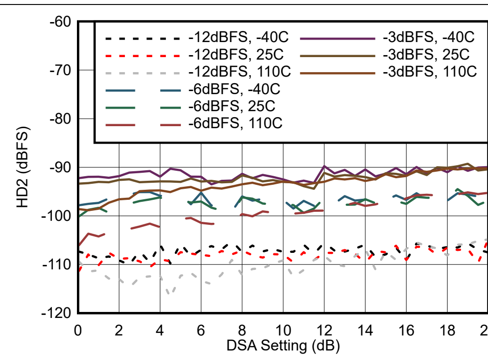
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-24. IMD3 vs DSA Setting at 30 MHz



f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-25. HD2 vs Input Amplitude at 30 MHz

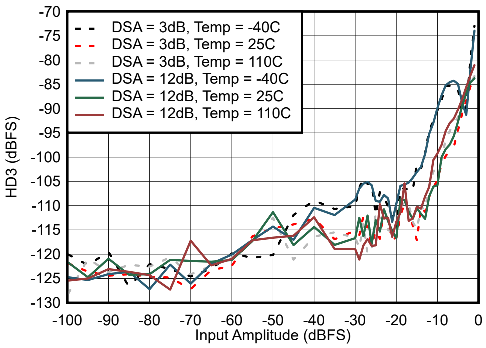


f_{ADC} = 1500 MSPS, f_{NCO} = 32. , Decimate by 24x

Figure 5-26. HD2 vs DSA Setting at 30 MHz

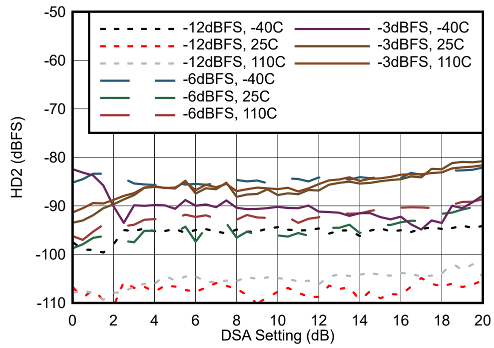
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



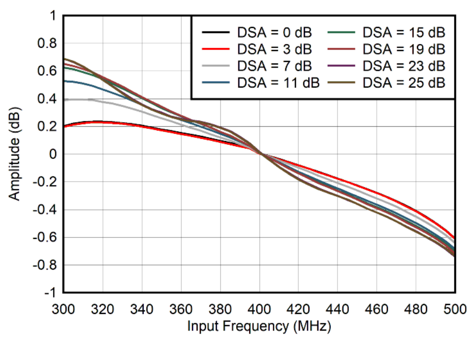
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-27. HD3 vs Input Amplitude at 30 MHz



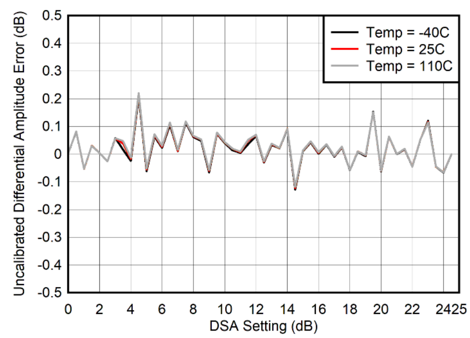
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

Figure 5-28. HD3 vs DSA Setting at 30 MHz



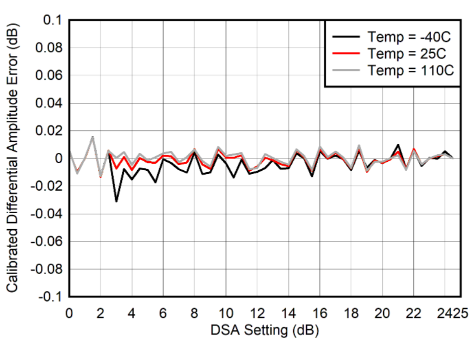
Normalized to 4000 MHz

Figure 5-29. RX In-Band Gain Flatness, f_{IN} = 400 MHz



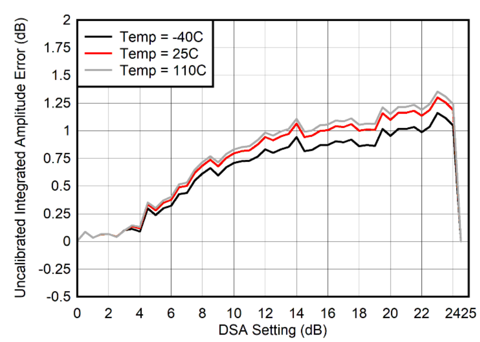
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 5-30. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 5-31. RX Calibrated Differential Amplitude Error vs DSA Setting at 400 MHz

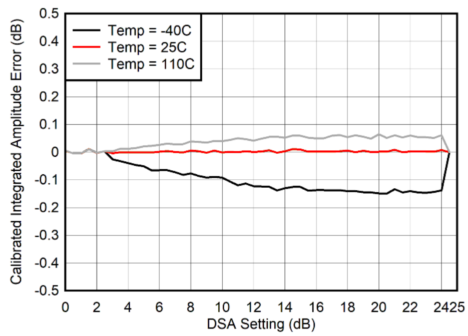


Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 5-32. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 400 MHz

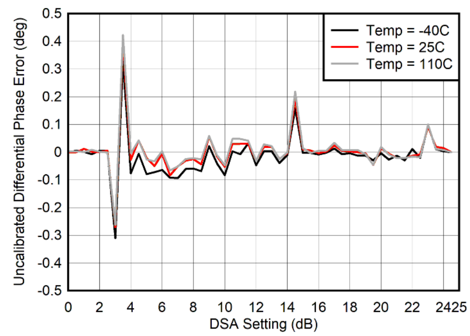
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



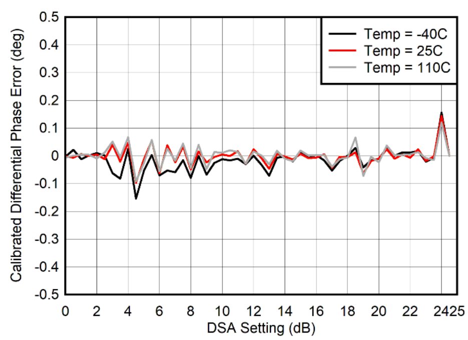
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 5-33. RX Calibrated Integrated Amplitude Error vs DSA Setting at 400 MHz



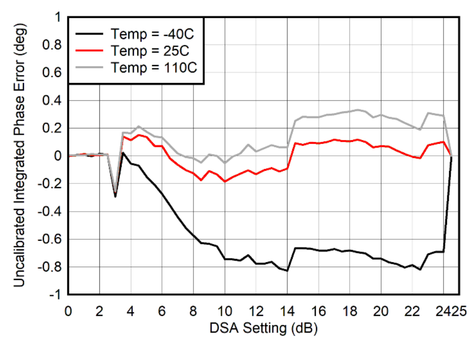
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 5-34. RX Uncalibrated Differential Phase Error vs DSA Setting at 400 MHz



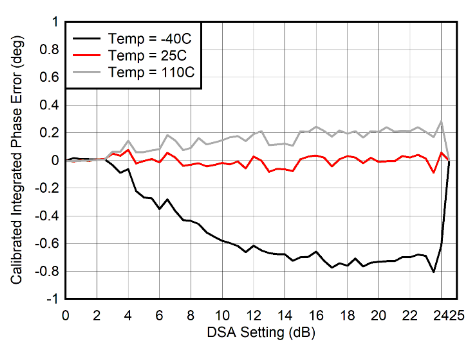
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 5-35. RX Calibrated Differential Phase Error vs DSA Setting at 400 MHz



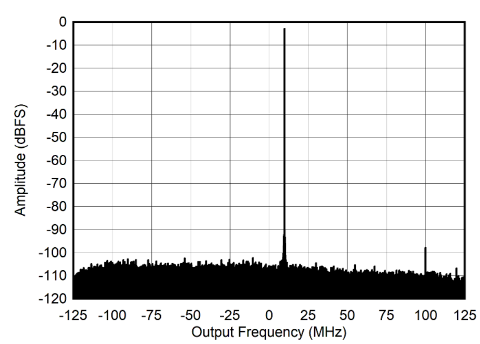
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-36. RX Uncalibrated Integrated Phase Error vs DSA Setting at 400 MHz



Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-37. RX Calibrated Integrated Phase Error vs DSA Setting at 400 MHz

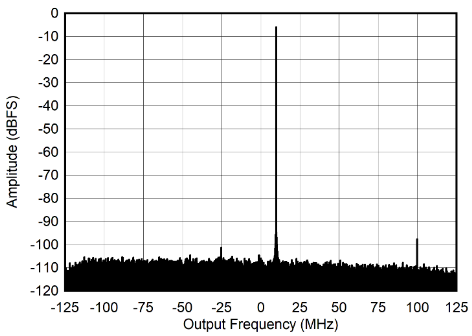


f_{NCO} = 400 MHz

Figure 5-38. RX Output FFT at 405 MHz and -3 dBFS

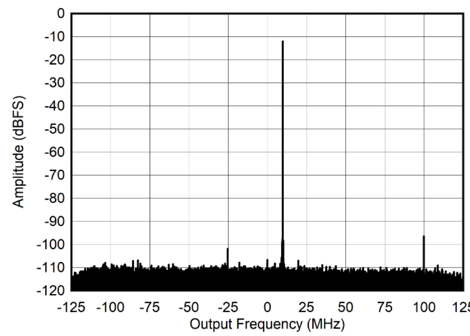
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



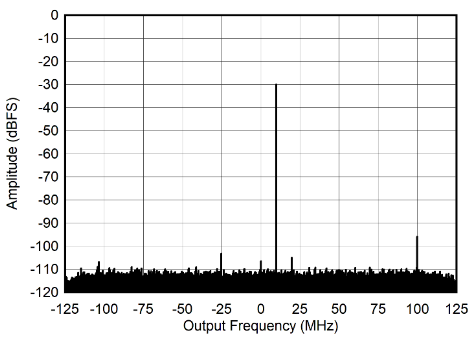
f_{NCO} = 400 MHz

Figure 5-39. RX Output FFT at 405 MHz and -6 dBFS



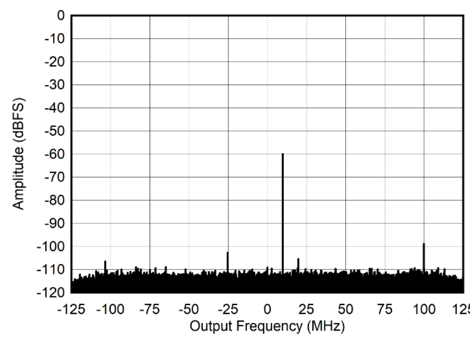
f_{NCO} = 400 MHz

Figure 5-40. RX Output FFT at 405 MHz and -12 dBFS



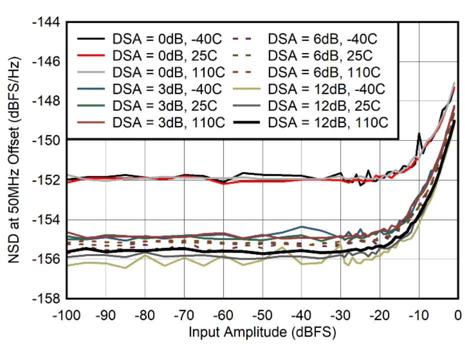
f_{NCO} = 400 MHz

Figure 5-41. RX Output FFT at 405 MHz and -30 dBFS



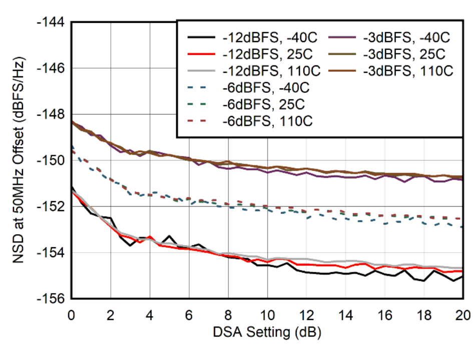
f_{NCO} = 400 MHz

Figure 5-42. RX Output FFT at 405 MHz and -60 dBFS



f_{OFFSET} = 50 MHz

Figure 5-43. NSD vs Input Amplitude at 400 MHz



f_{OFFSET} = 50MHz

Figure 5-44. NSD vs DSA Setting at 400 MHz

5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.

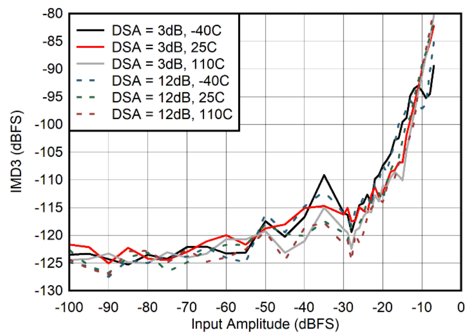


Figure 5-45. IMD3 vs Input Amplitude at 400 MHz

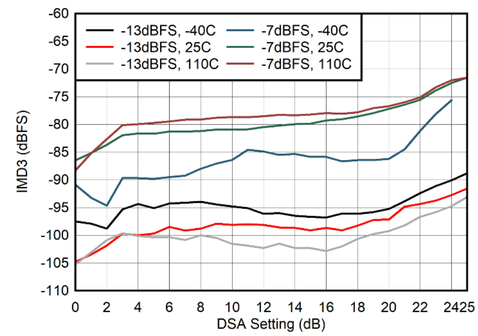


Figure 5-46. IMD3 vs DSA Setting at 400 MHz

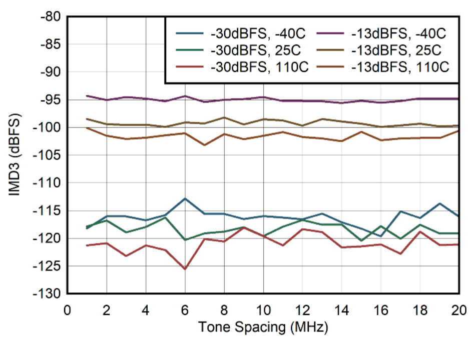


Figure 5-47. IMD3 vs Tone Spacing at 400 MHz

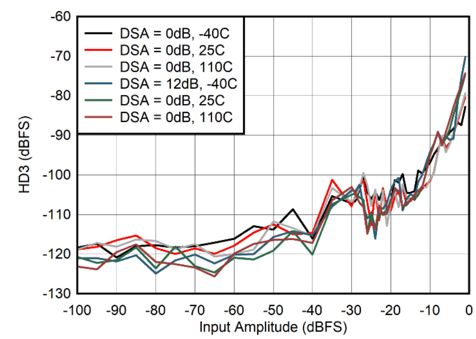


Figure 5-48. HD3 vs Input Amplitude at 400 MHz

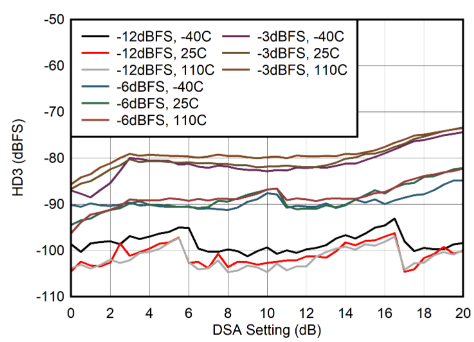
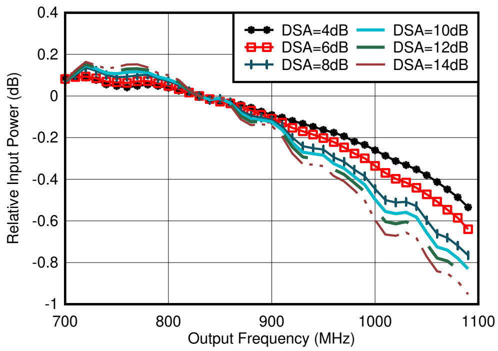


Figure 5-49. HD3 vs DSA Setting at 400 MHz

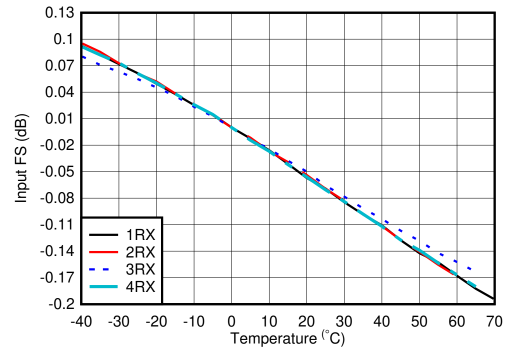
5.12.2 RX Typical Characteristics at 800 MHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



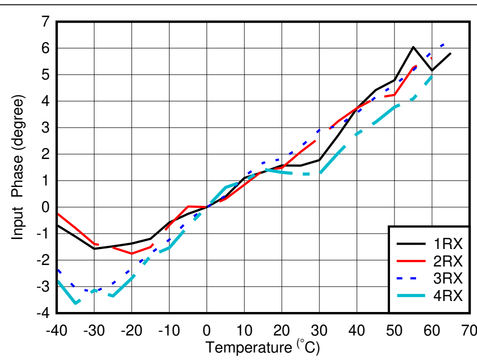
With 0.8 GHz matching, normalized to 830 MHz

Figure 5-50. RX In-Band Gain Flatness for Channel 1RX, f_{IN} = 830 MHz



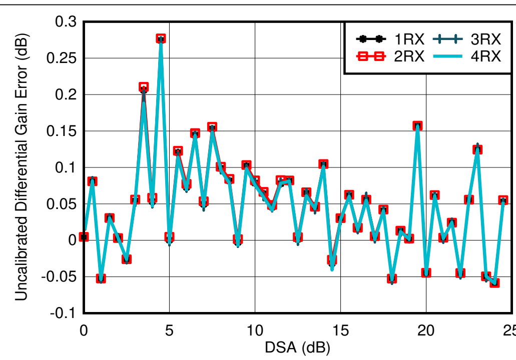
With 0.8 GHz matching, normalized to fullscale at 25°C for each channel

Figure 5-51. RX Input Fullscale vs Temperature and Channel at 800 MHz



With 0.8 GHz matching, normalized to phase at 25°C

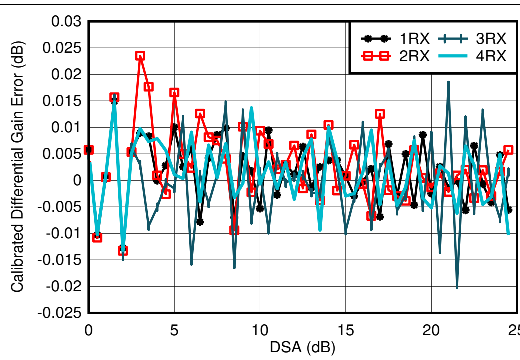
Figure 5-52. RX Input Phase vs Temperature and DSA at f_{OUT} = 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

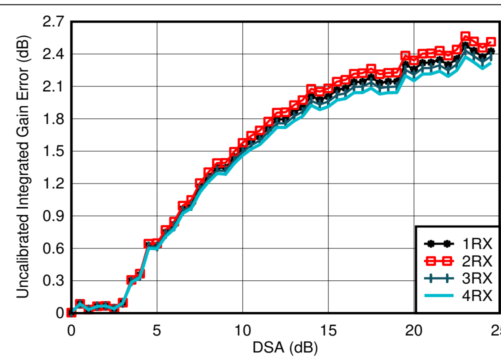
Figure 5-53. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 5-54. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



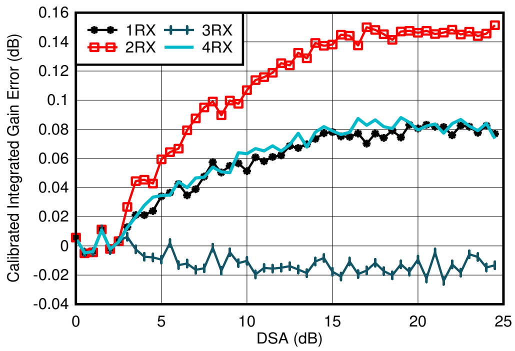
With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 5-55. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz

5.12.2 RX Typical Characteristics at 800 MHz (continued)

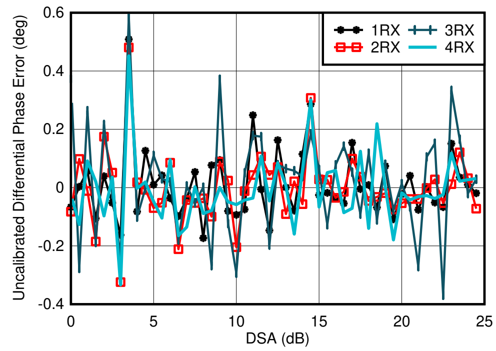
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

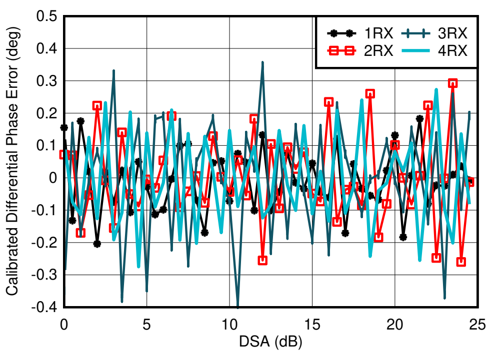
Figure 5-56. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

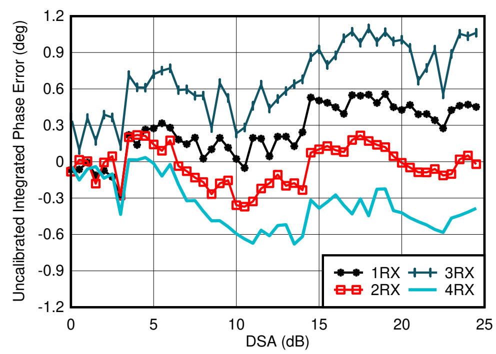
Figure 5-57. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 5-58. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



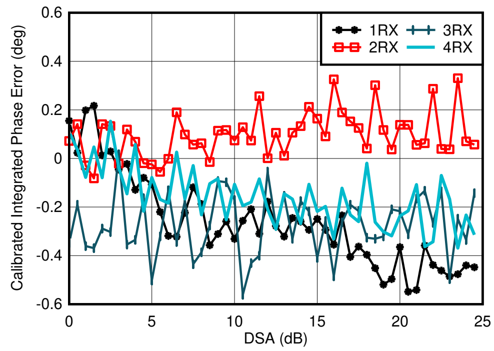
With 0.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-59. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz

5.12.2 RX Typical Characteristics at 800 MHz (continued)

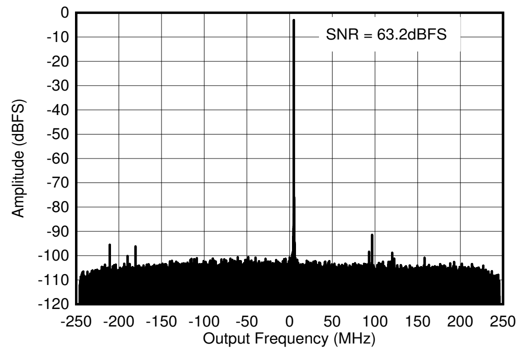
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 0.8 GHz matching

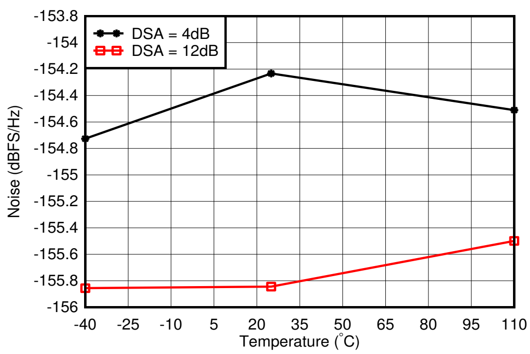
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-60. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



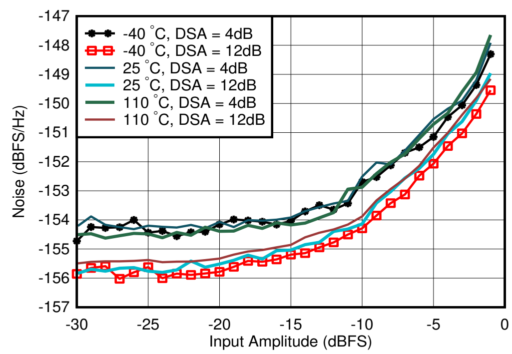
With 0.8 GHz matching, f_{IN} = 840 MHz, A_{IN}= –3 dBFS

Figure 5-61. RX Output FFT at 0.8 GHz



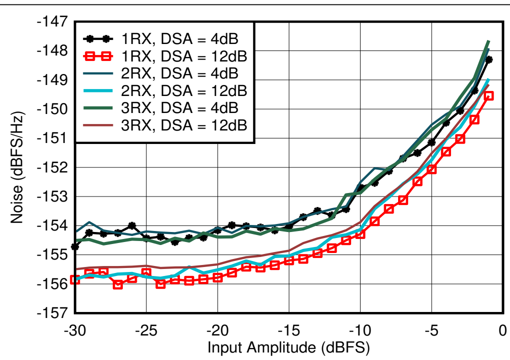
With 0.8 GHz matching, 12.5-MHz offset from tone

Figure 5-62. RX Noise Spectral Density vs Temperature at 0.8 GHz



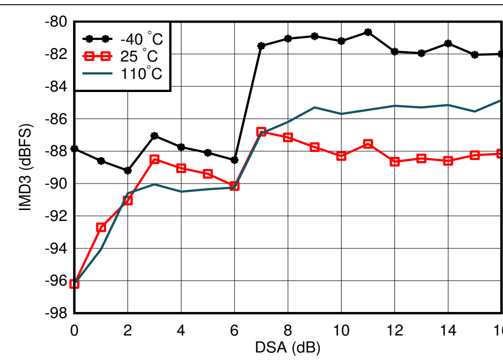
With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 5-63. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz



With 0.8 GHz matching, 12.5-MHz offset from tone

Figure 5-64. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz

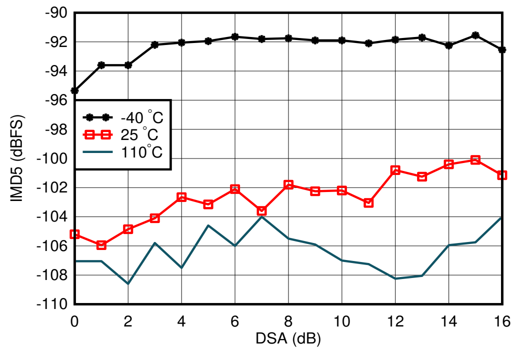


A. With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 5-65. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz

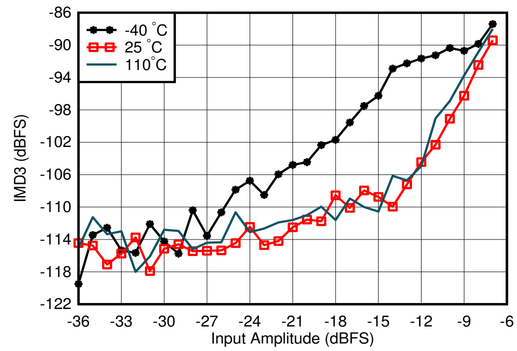
5.12.2 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



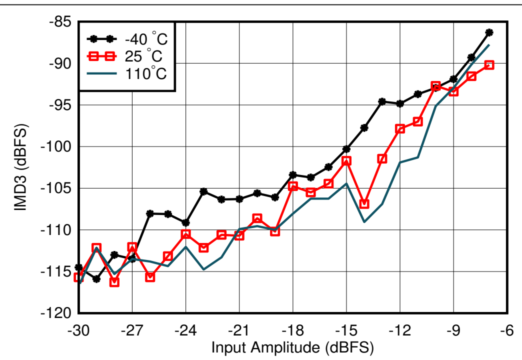
With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 5-66. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz



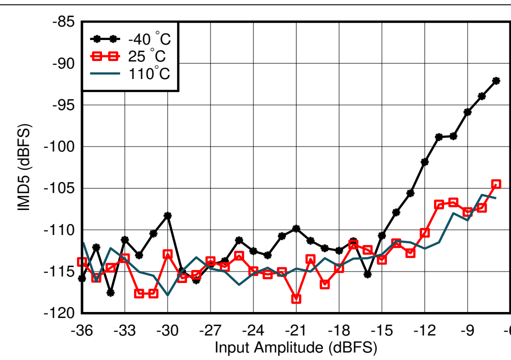
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 5-67. RX IMD3 vs Input Level and Temperature at 0.8 GHz



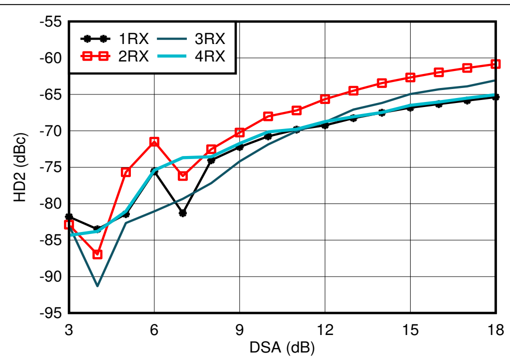
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 5-68. RX IMD3 vs Input Level and Temperature at 0.8 GHz



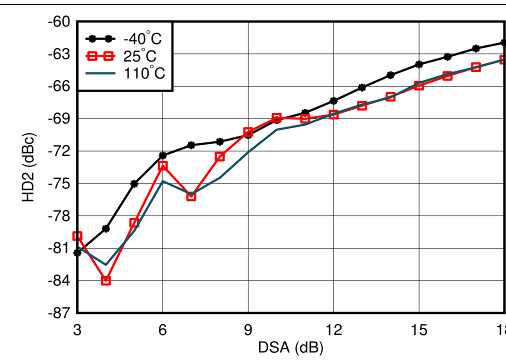
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 5-69. RX IMD5 vs Input Level and Temperature at 0.8 GHz



With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 5-70. RX HD2 vs DSA Setting and Channel at 0.8 GHz

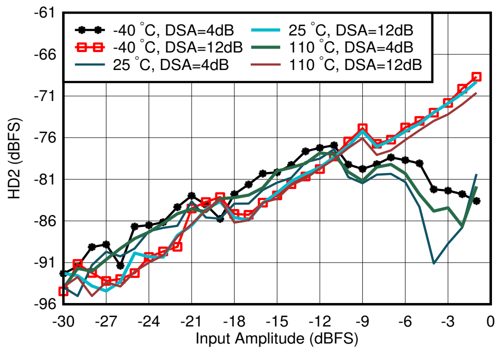


With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 5-71. RX HD2 vs DSA Setting and Temperature at 0.8 GHz

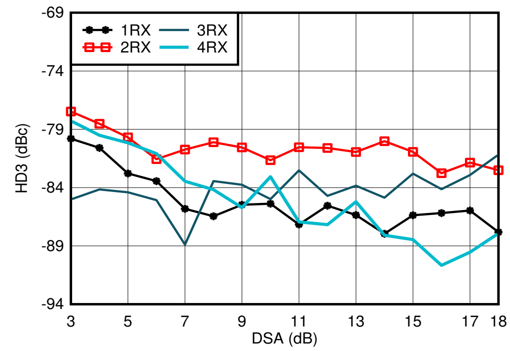
5.12.2 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



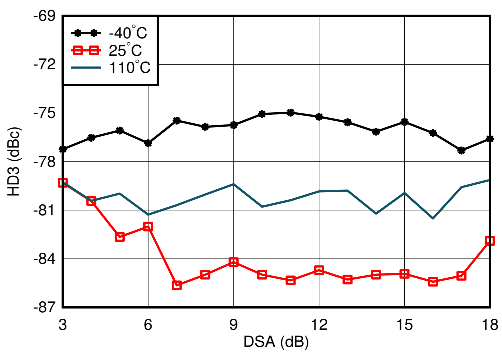
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 5-72. RX HD2 vs Input Level and Temperature at 0.8 GHz



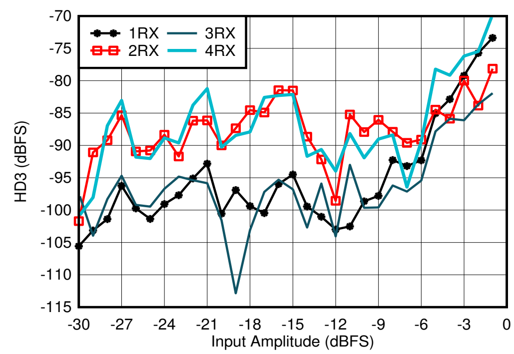
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-73. RX HD3 vs DSA Setting and Channel at 0.8 GHz



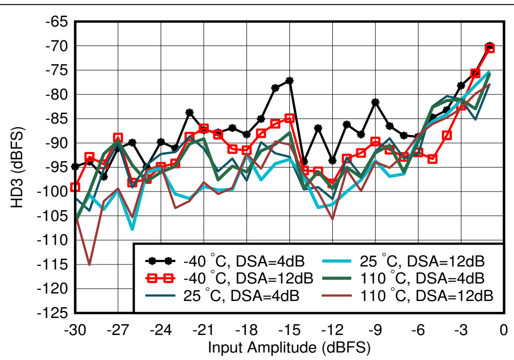
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-74. RX HD3 vs DSA Setting and Temperature at 0.8 GHz



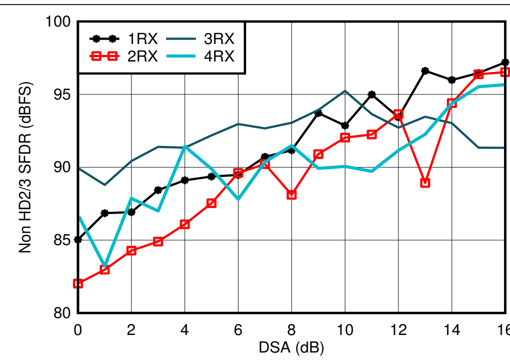
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-75. RX HD3 vs Input Level and Channel at 0.8 GHz



With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-76. RX HD3 vs Input Level and Temperature at 0.8 GHz

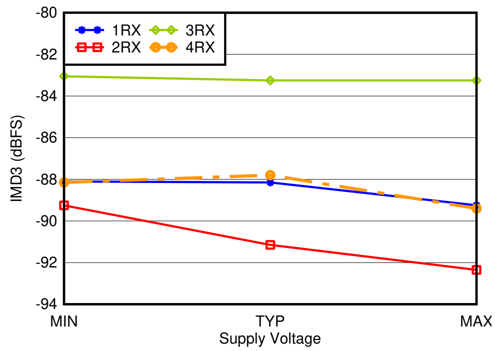


With 0.8 GHz matching

Figure 5-77. RX Non-HD2/3 vs DSA Setting at 0.8 GHz

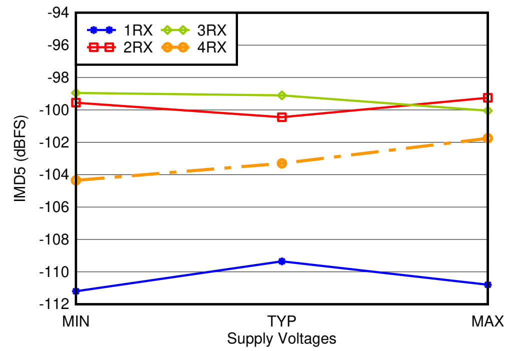
5.12.2 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



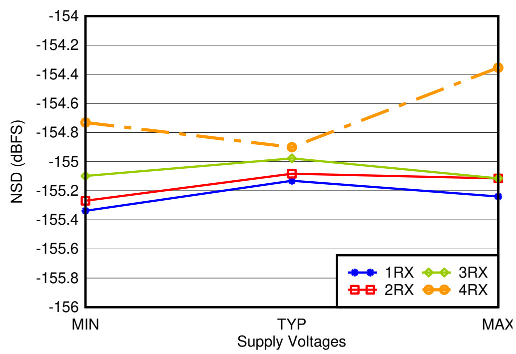
With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-78. RX IMD3 vs Supply and Channel at 0.8 GHz



With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-79. RX IMD5 vs Supply and Channel at 0.8 GHz

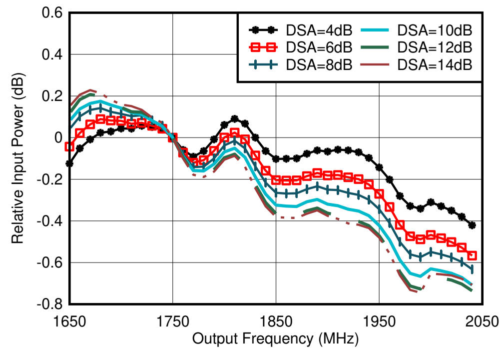


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-80. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

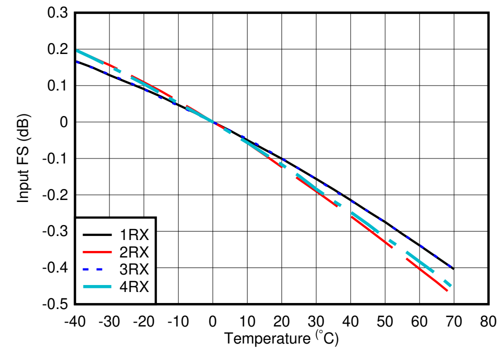
5.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



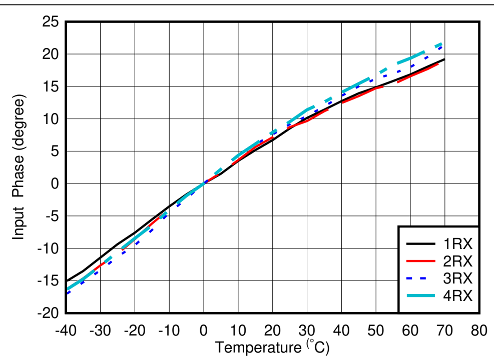
With 1.8 GHz matching, normalized to 1.75 GHz

Figure 5-81. RX In-Band Gain Flatness, f_{IN} = 1750 MHz



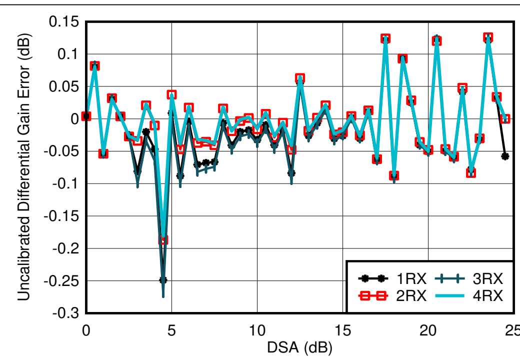
With 1.8 GHz matching, normalized to fullscale at 25°C for each channel

Figure 5-82. RX Input Fullscale vs Temperature and Channel at 1.75 GHz



With 2.6 GHz matching, normalized to phase at 25°C

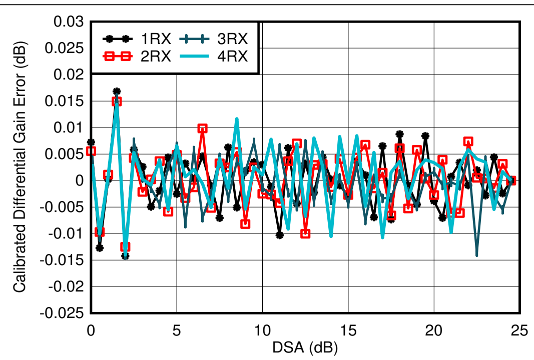
Figure 5-83. RX Input Phase vs Temperature and DSA at f_{IN} = 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

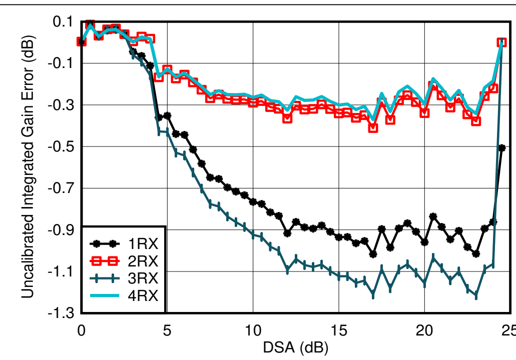
Figure 5-84. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 5-85. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



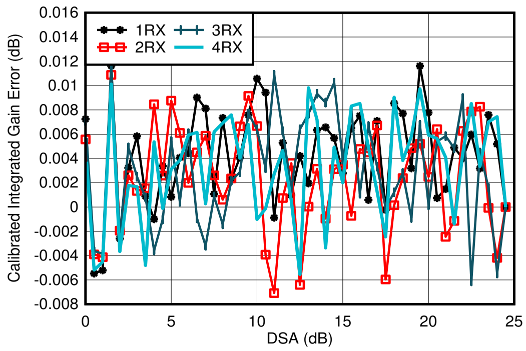
With 1.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 5-86. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz

5.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz (continued)

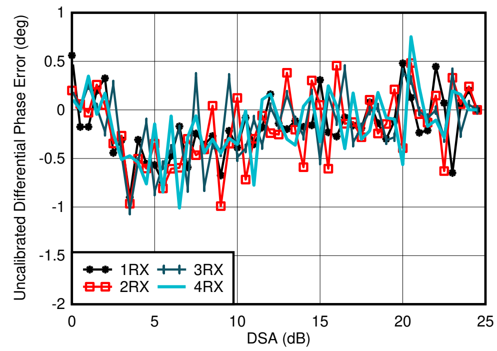
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 1.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

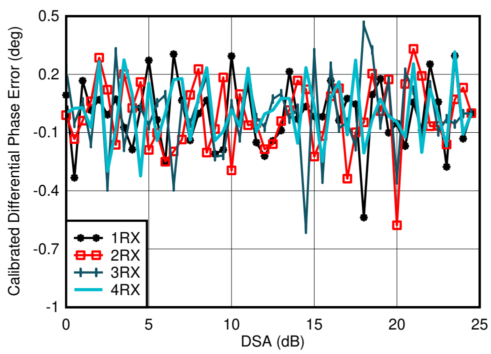
Figure 5-87. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

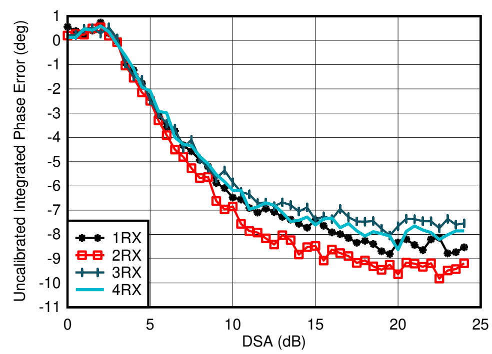
Figure 5-88. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 5-89. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



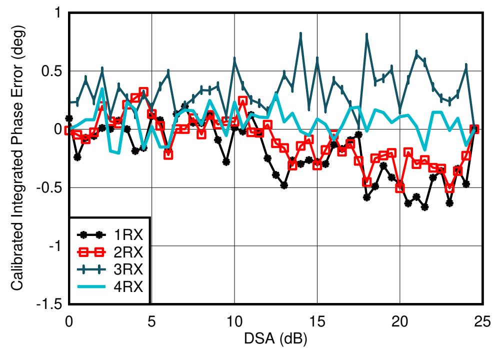
With 1.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-90. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

5.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz (continued)

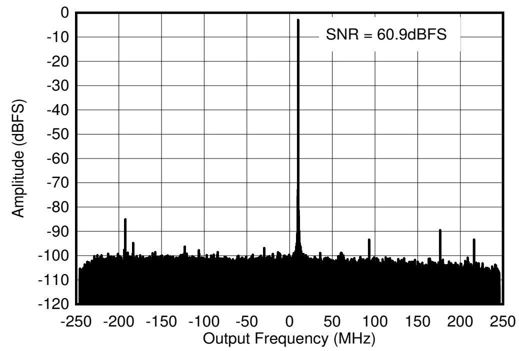
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 1.8 GHz matching

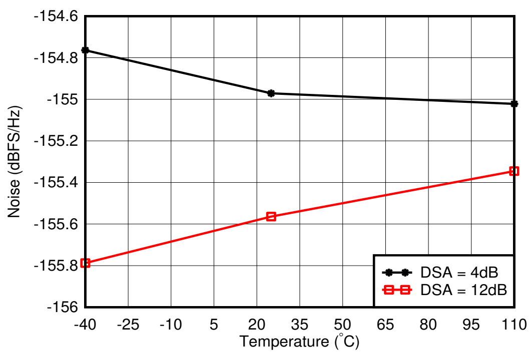
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-91. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



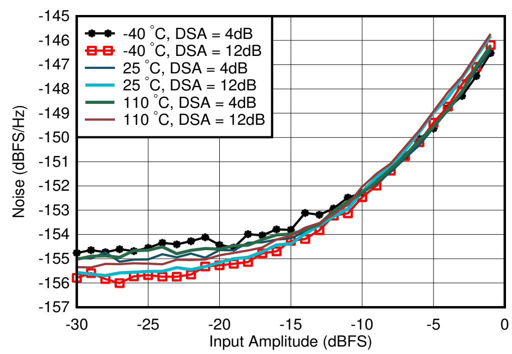
With 1.8 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

Figure 5-92. RX Output FFT at 1.75 GHz



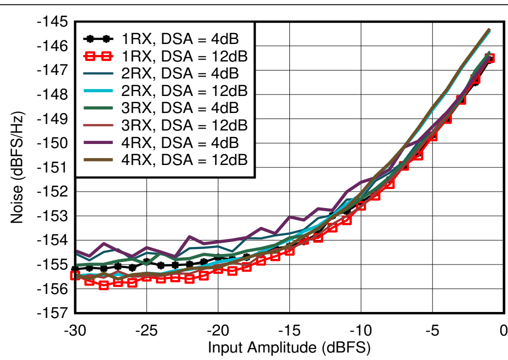
With 1.8 GHz matching, 12.5-MHz offset from tone

Figure 5-93. RX Noise Spectral Density vs Temperature at 1.75 GHz



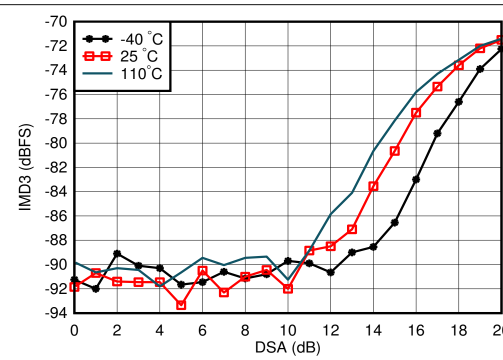
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 5-94. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz



With 1.8 GHz matching, 12.5-MHz offset from tone

Figure 5-95. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz

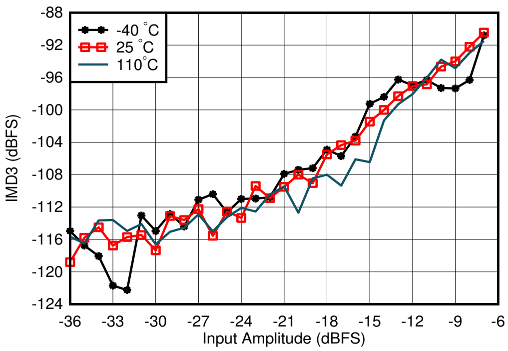


With 1.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 5-96. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz

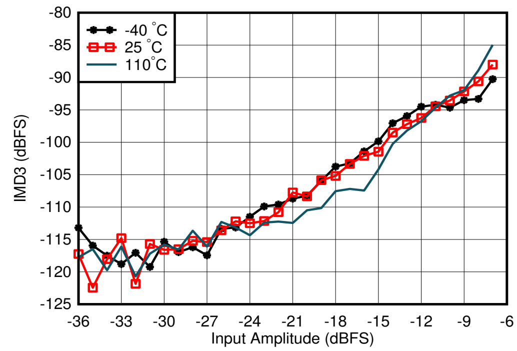
5.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



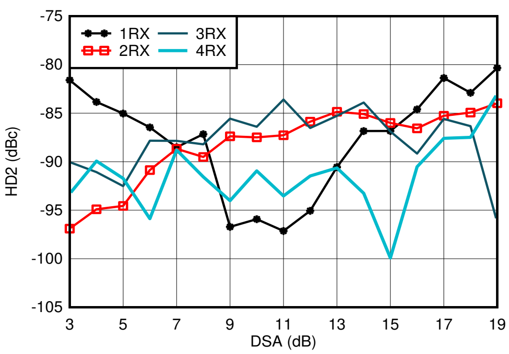
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 5-97. RX IMD3 vs Input Level and Temperature at 1.75 GHz



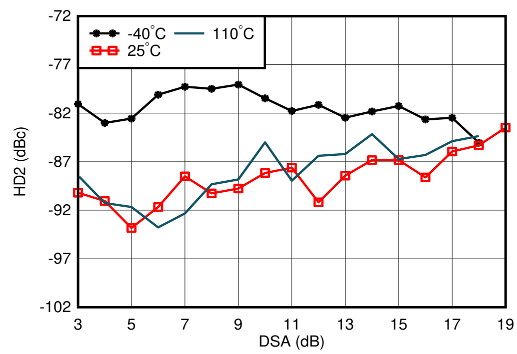
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 5-98. RX IMD3 vs Input Level and Temperature at 1.75 GHz



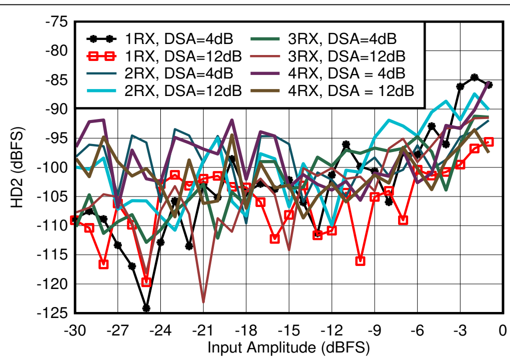
With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 5-99. RX HD2 vs DSA Setting and Channel at 1.9 GHz



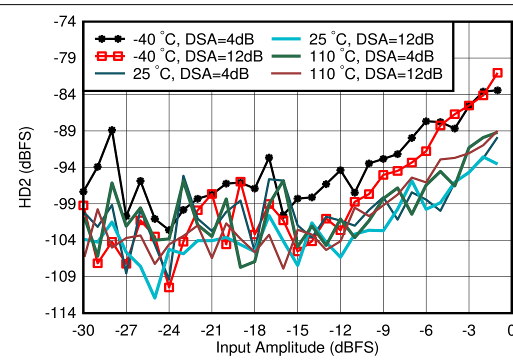
With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 5-100. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 5-101. RX HD2 vs Input Amplitude and Channel at 1.9 GHz

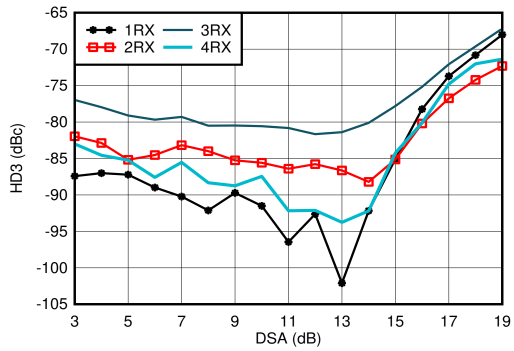


With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 5-102. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz

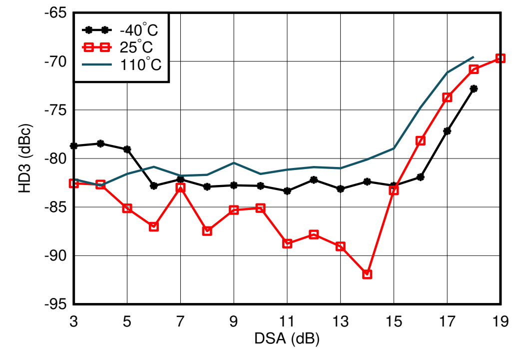
5.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



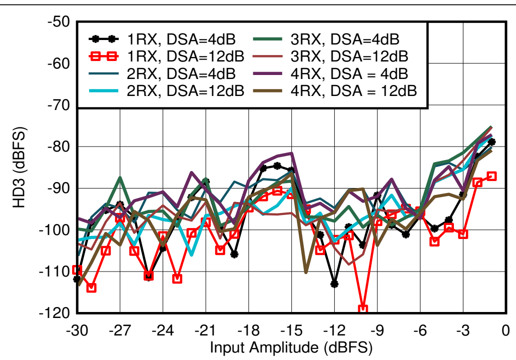
With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

Figure 5-103. RX HD3 vs DSA Setting and Channel at 1.9 GHz



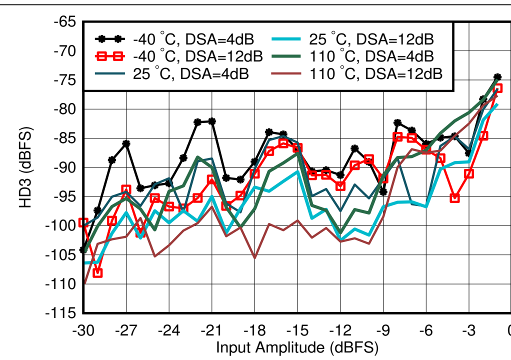
With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

Figure 5-104. RX HD3 vs DSA Setting and Temperature at 1.9 GHz



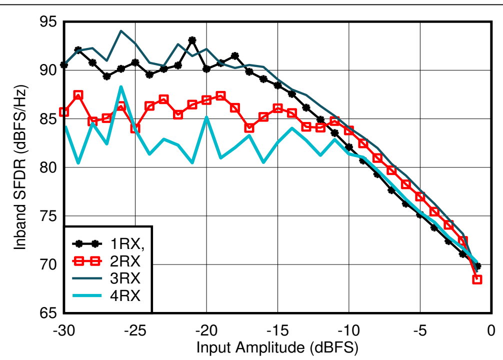
With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

Figure 5-105. RX HD3 vs Input Level and Channel at 1.9 GHz



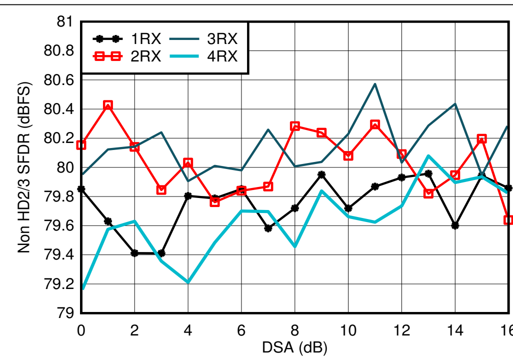
With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

Figure 5-106. RX HD3 vs Input Level and Temperature at 1.9 GHz



With 1.8 GHz matching, decimated by 3

Figure 5-107. RX In-Band SFDR (±400 MHz) vs Input Amplitude at 1.75 GHz

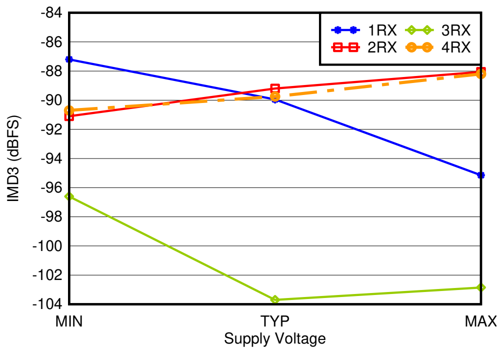


With 1.8 GHz matching

Figure 5-108. RX Non-HD2/3 vs DSA Setting at 1.75 GHz

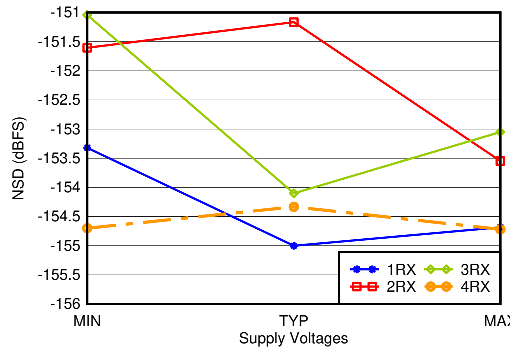
5.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 1.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-109. RX IMD3 vs Supply and Channel at 1.75 GHz

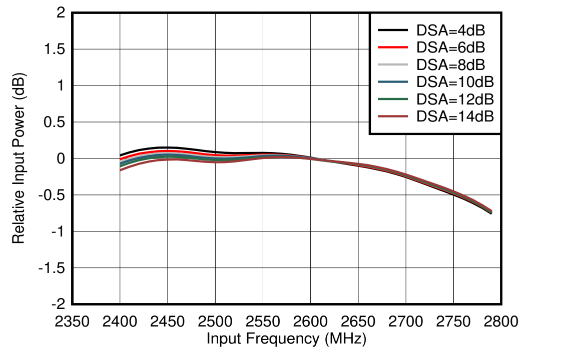


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-110. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

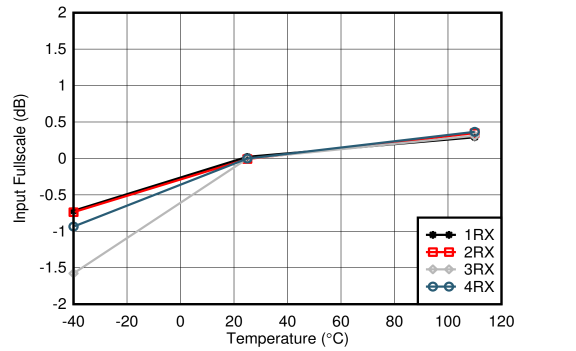
5.12.4 RX Typical Characteristics 2.6 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



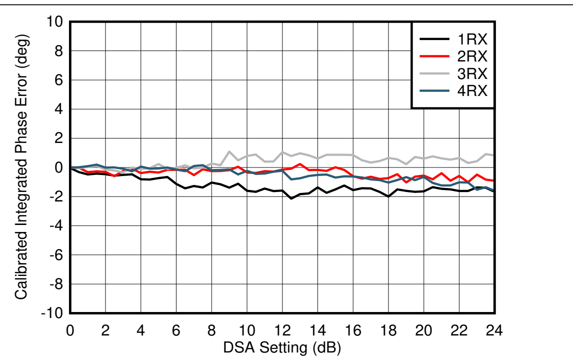
With matching, normalized to power at 2.6 GHz for each DSA setting

Figure 5-111. RX Inband Gain Flatness, f_{IN} = 2600 MHz



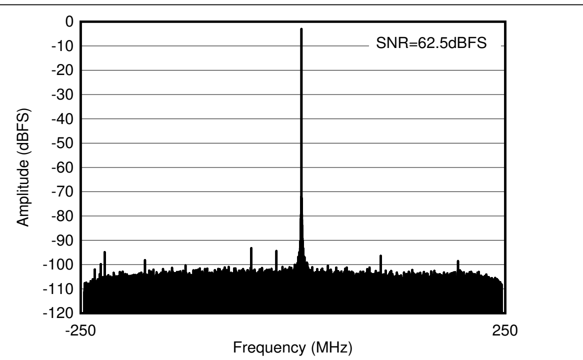
With 2.6 GHz matching, normalized to fullscale at 25°C for each channel

Figure 5-112. RX Input Fullscale vs Temperature and Channel at 2.6 GHz



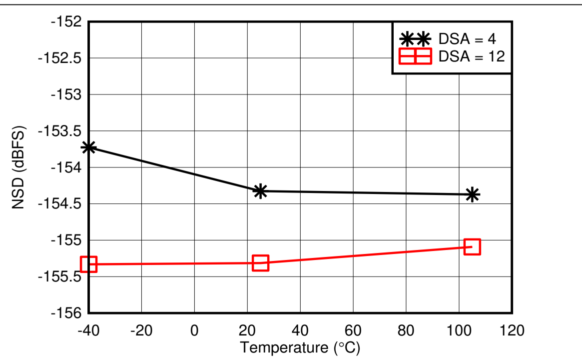
With 2.6 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-113. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



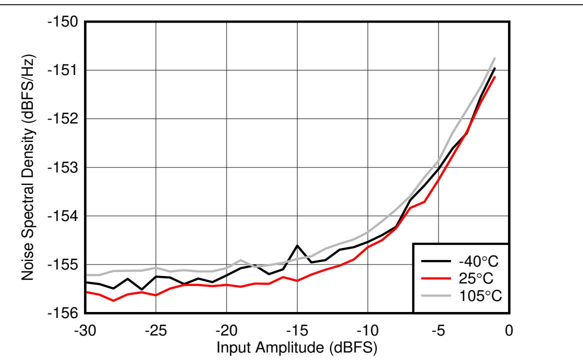
With 2.6 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

Figure 5-114. RX Output FFT at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset from tone

Figure 5-115. RX Noise Spectral Density vs Temperature at 2.6 GHz

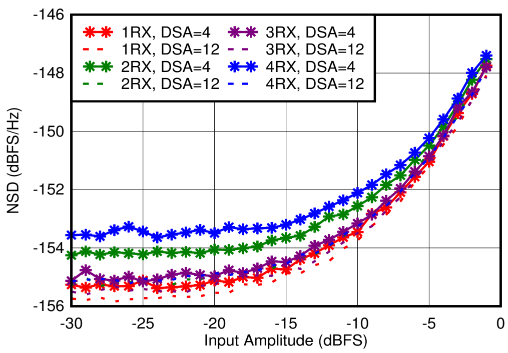


With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 5-116. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

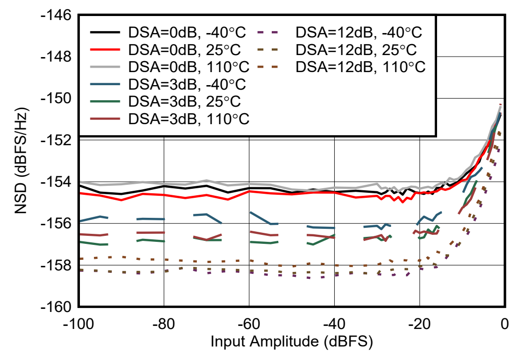
5.12.4 RX Typical Characteristics 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



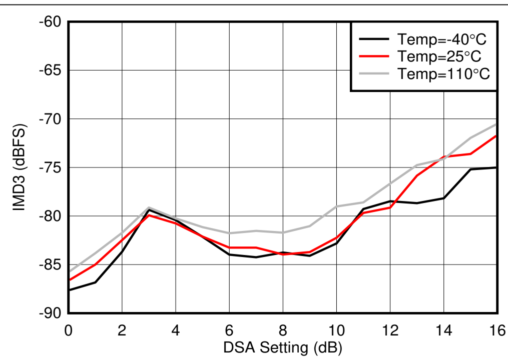
With 2.6 GHz matching, 12.5-MHz offset from tone

Figure 5-117. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz



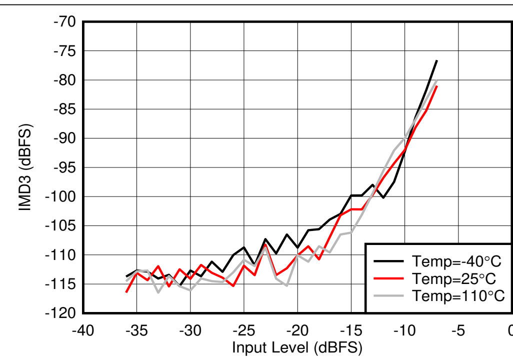
50-MHz offset from tone, external clock mode

Figure 5-118. RX Noise Spectral Density vs Input Amplitude at 2.61 GHz (Ext. Clock)



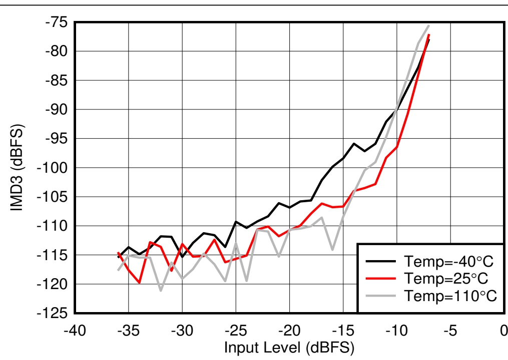
With 2.6 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 5-119. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz



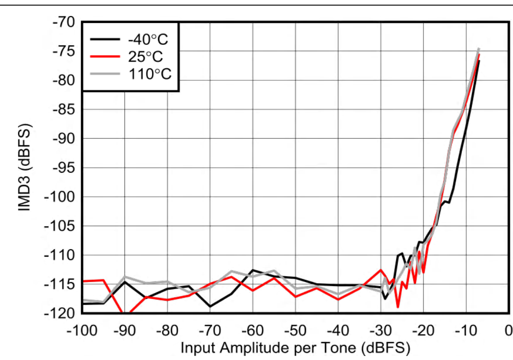
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 5-120. RX IMD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 5-121. RX IMD3 vs Input Level and Temperature at 2.6 GHz

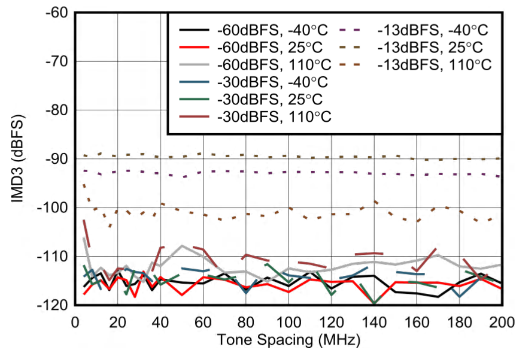


Tone spacing = 50 MHz, External clock mode

Figure 5-122. RX IMD3 vs Input Level at 2.6 GHz (Ext. Clock)

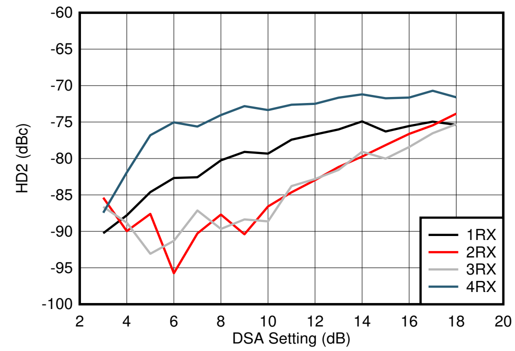
5.12.4 RX Typical Characteristics 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



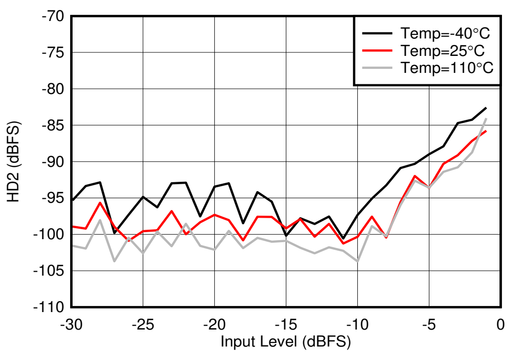
External clock mode

Figure 5-123. RX IMD3 vs Tone Spacing at 2.6 GHz (Ext. Clock)



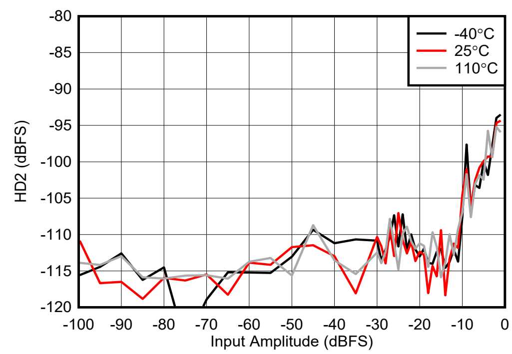
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-124. RX HD2 vs DSA Setting and Channel at 2.6 GHz



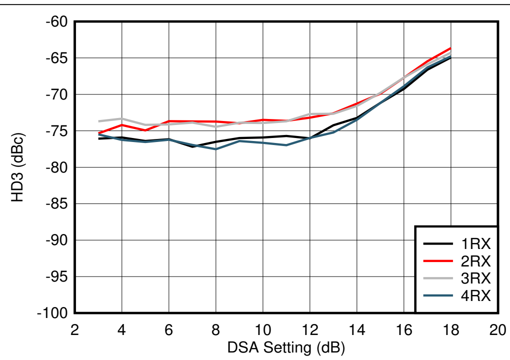
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-125. RX HD2 vs Input Level and Temperature at 2.6 GHz



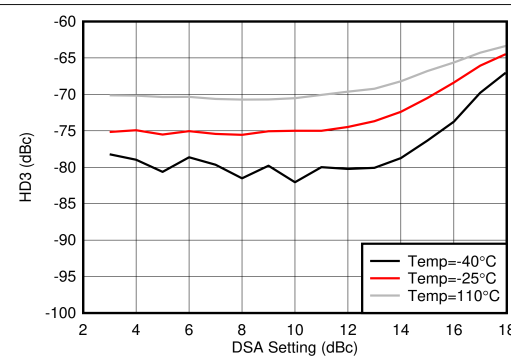
External clock mode

Figure 5-126. RX HD2 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-127. RX HD3 vs DSA Setting and Channel at 2.6 GHz

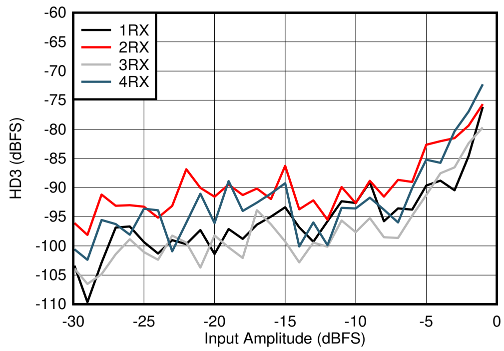


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-128. RX HD3 vs DSA Setting and Temperature at 2.6 GHz

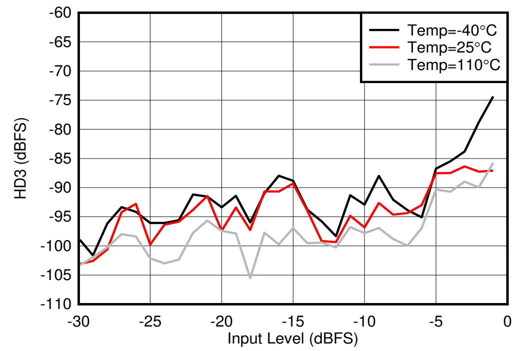
5.12.4 RX Typical Characteristics 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



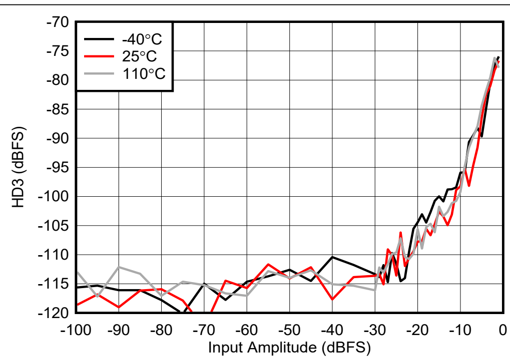
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-129. RX HD3 vs Input Level and Channel at 2.6 GHz



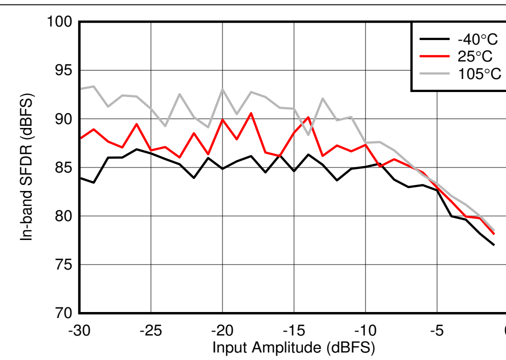
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-130. RX HD3 vs Input Level and Temperature at 2.6 GHz



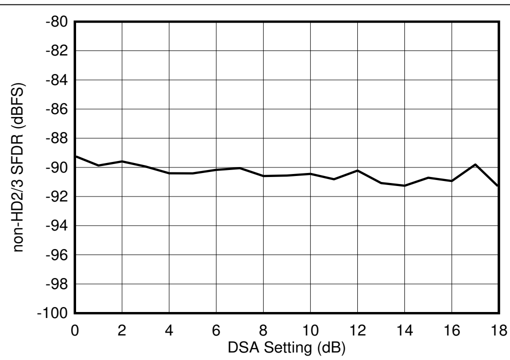
External clock mode

Figure 5-131. RX HD3 vs Input Level and Temperature at 2.6 GHz



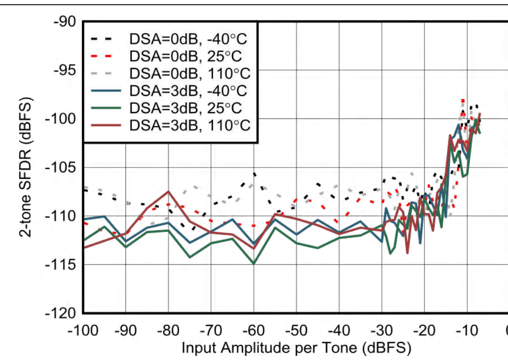
With 2.6 GHz matching, decimate by 4

Figure 5-132. RX In-Band SFDR (±300 MHz) vs Input Amplitude and Temperature at 2.6 GHz



With 2.6 GHz matching

Figure 5-133. RX Non-HD2/3 vs DSA Setting at 2.6 GHz

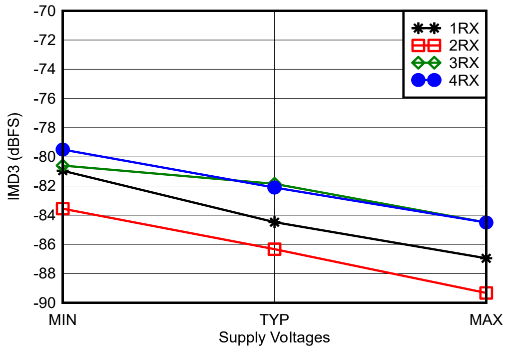


External clock mode, 50MHz tone spacing, excluding 3rd order distortion

Figure 5-134. RX 2-tone SFDR vs Input Amplitude at 2.6 GHz

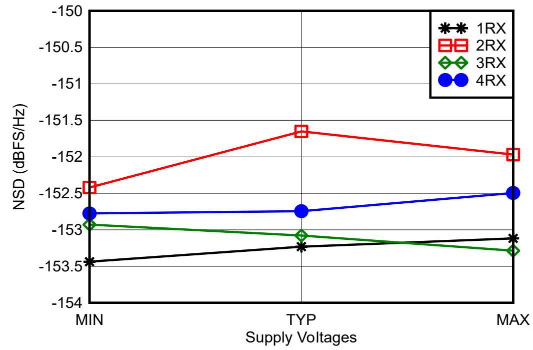
5.12.4 RX Typical Characteristics 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 2.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-135. RX IMD3 vs Supply and Channel at 2.6 GHz

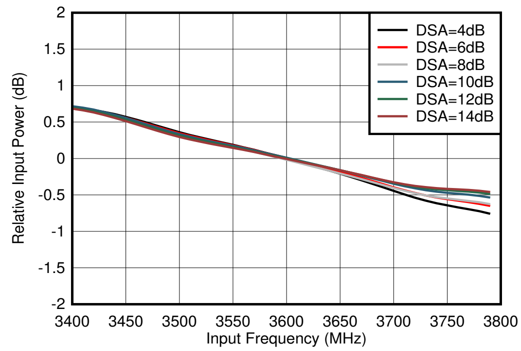


With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-136. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

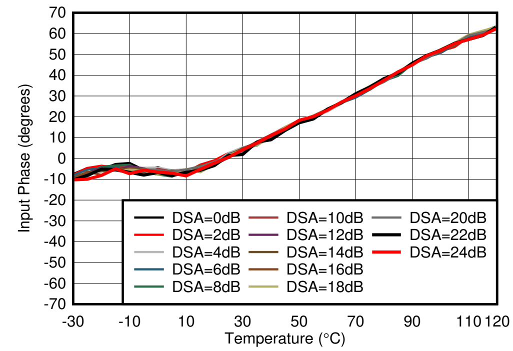
5.12.5 RX Typical Characteristics 3.5 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



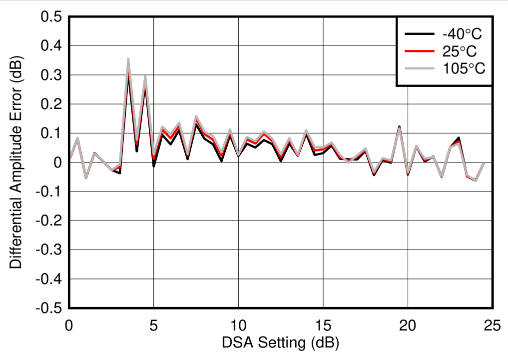
With 3.6 GHz matching, normalized to 3.6 GHz

Figure 5-137. RX In-Band Gain Flatness, f_{IN} = 3600 MHz



With 3.6 GHz matching, normalized to phase at 25°C

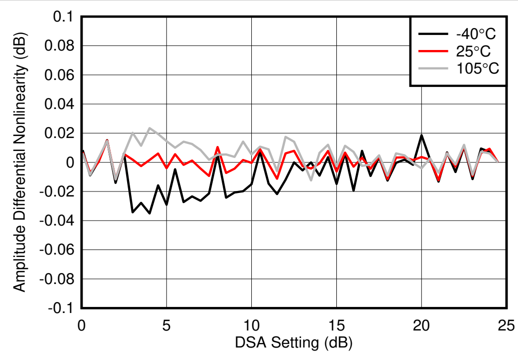
Figure 5-138. RX Input Phase vs Temperature at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

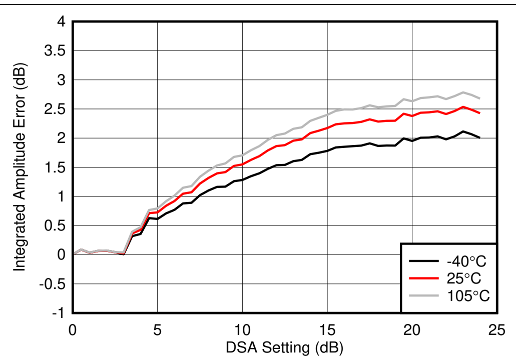
Figure 5-139. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

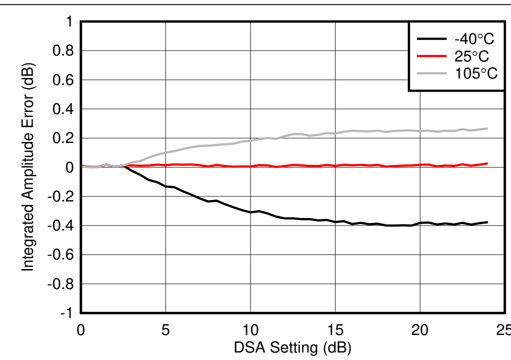
Figure 5-140. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 5-141. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



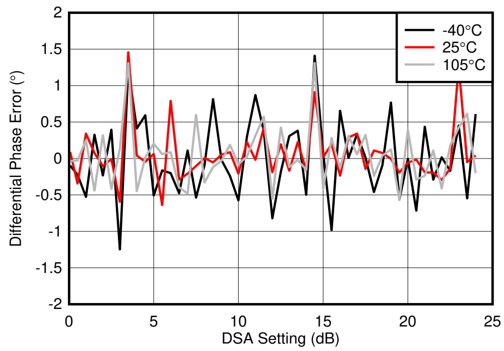
With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 5-142. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz

5.12.5 RX Typical Characteristics 3.5 GHz (continued)

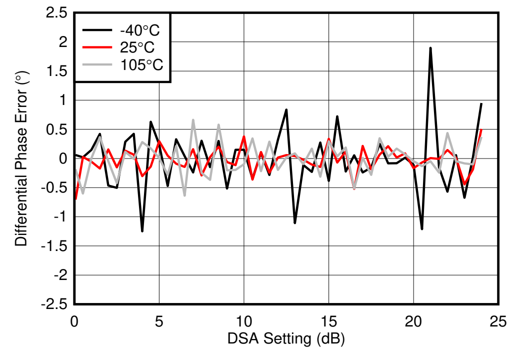
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 3.6 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

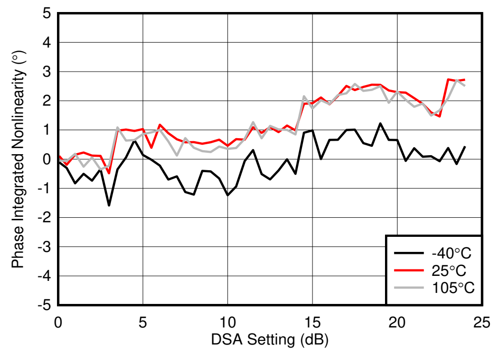
Figure 5-143. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

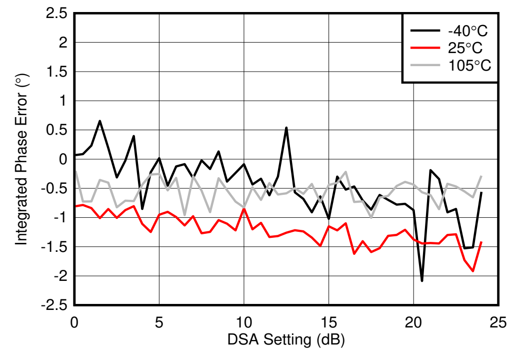
Figure 5-144. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

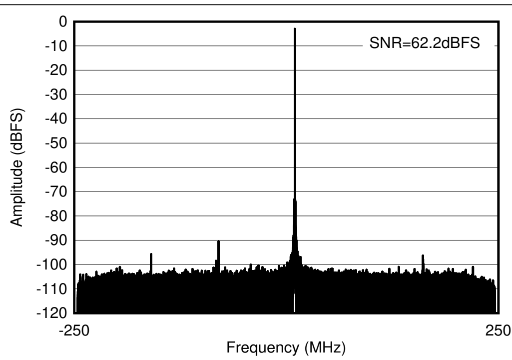
Figure 5-145. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

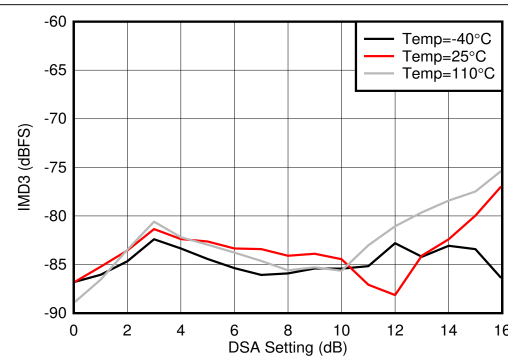
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-146. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching , f_{IN} = 3610 MHz, A_{IN} = –3 dBFS

Figure 5-147. RX Output FFT at 3.6 GHz

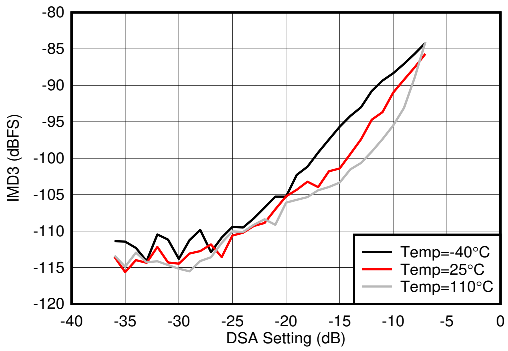


With 3.5 GHz matching, each tone at –7 dBFS, 20-MHz tone spacing

Figure 5-148. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz

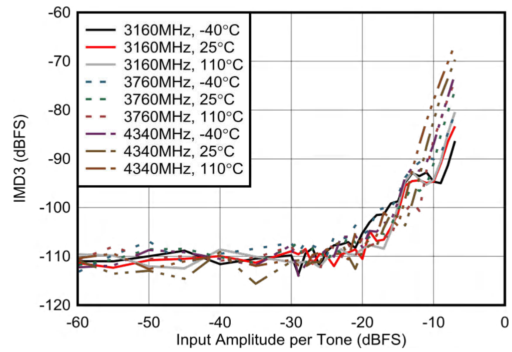
5.12.5 RX Typical Characteristics 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



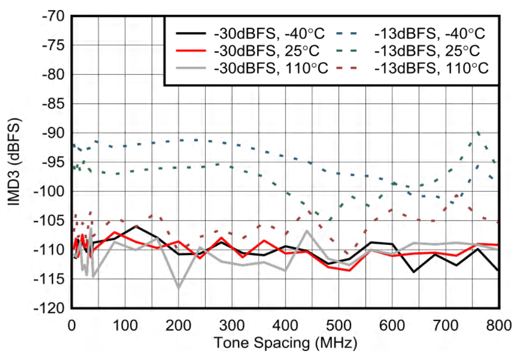
With 3.5 GHz matching, 20-MHz tone spacing

Figure 5-149. RX IMD3 vs Input Level and Temperature at 3.6 GHz



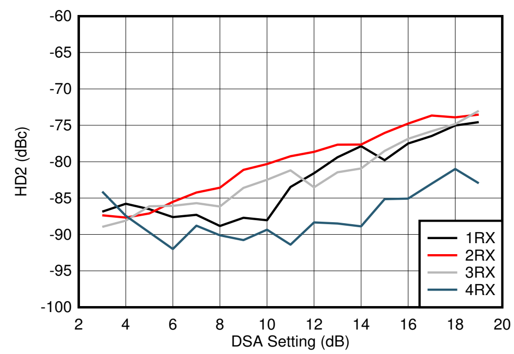
External clock mode, 20-MHz tone spacing, 2x Decimation

Figure 5-150. RX IMD3 vs Input Level



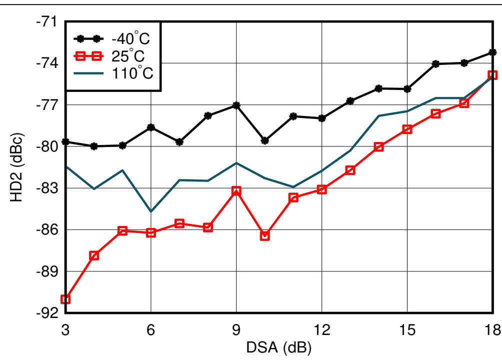
External clock mode, 2x Decimation

Figure 5-151. RX IMD3 vs Tone Spacing at 3.76 GHz



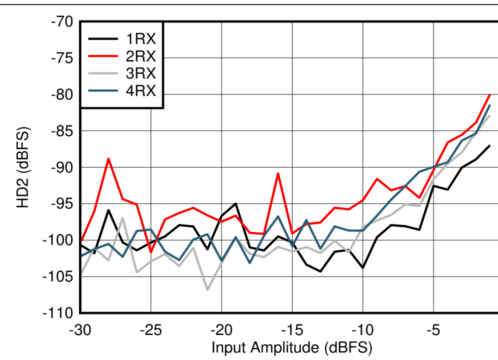
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-152. RX HD2 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-153. RX HD2 vs DSA Setting and Temperature at 3.6 GHz

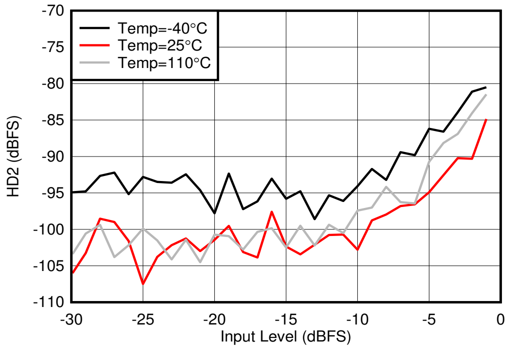


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-154. RX HD2 vs Input Level and Channel at 3.6 GHz

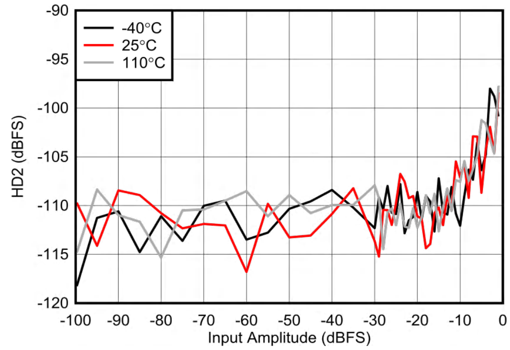
5.12.5 RX Typical Characteristics 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



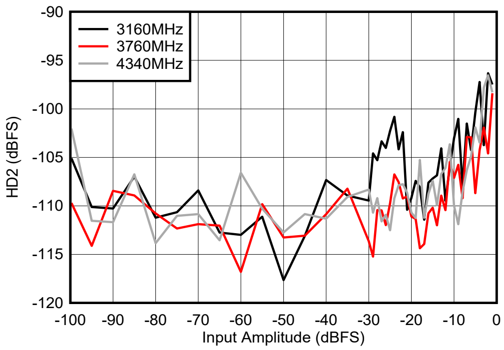
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-155. RX HD2 vs Input Level and Temperature at 3.6 GHz



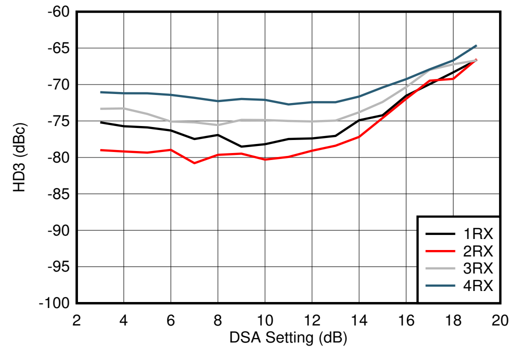
External clock mode, 2x Decimation

Figure 5-156. RX HD2 vs Input Level at 3.76 GHz



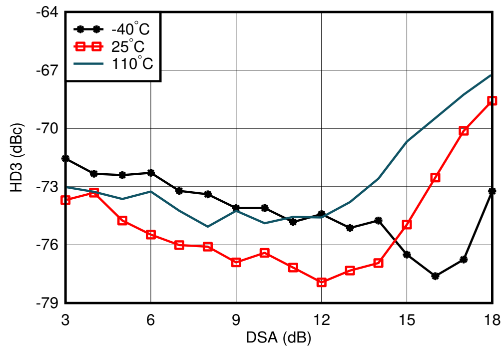
External clock mode, 25°C, 2x Decimation

Figure 5-157. RX HD2 vs Input Level



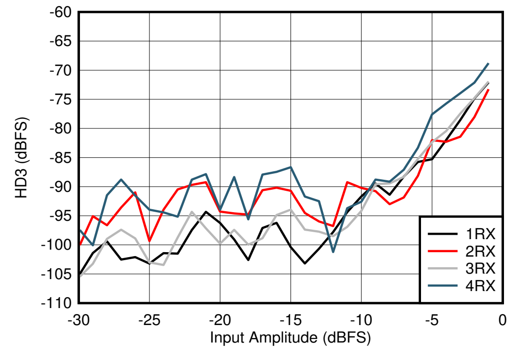
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-158. RX HD3 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-159. RX HD3 vs DSA Setting and Temperature at 3.6 GHz

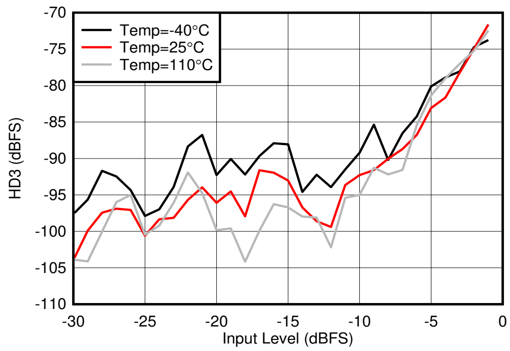


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-160. RX HD3 vs Input Level and Channel at 3.6 GHz

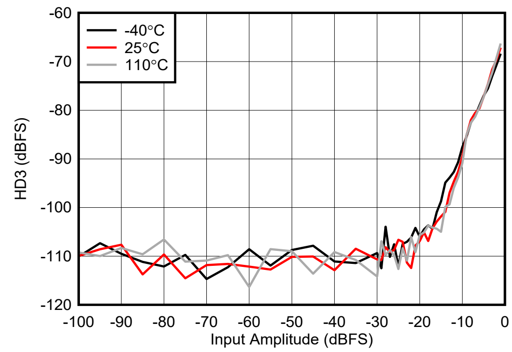
5.12.5 RX Typical Characteristics 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



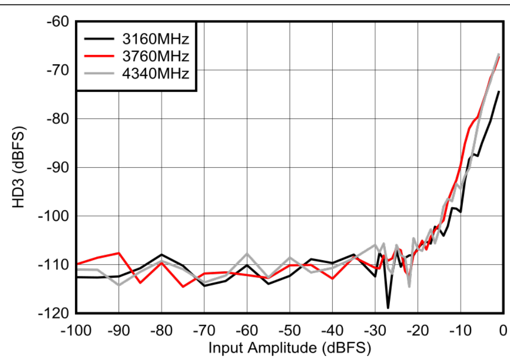
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-161. RX HD3 vs Input Level and Temperature at 3.6 GHz



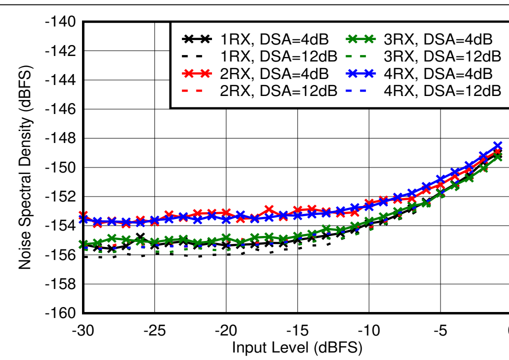
External clock mode, 2x Decimation

Figure 5-162. RX HD3 vs Input Level at 3.76 GHz



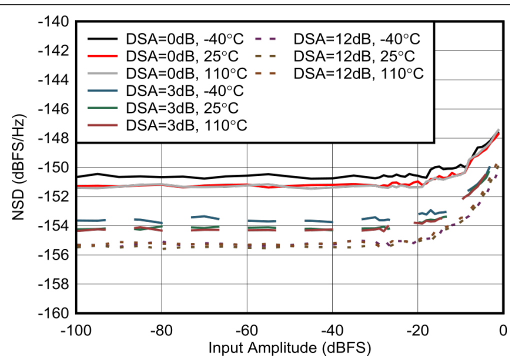
External clock mode, 25°C, 2x Decimation

Figure 5-163. RX HD3 vs Input Level



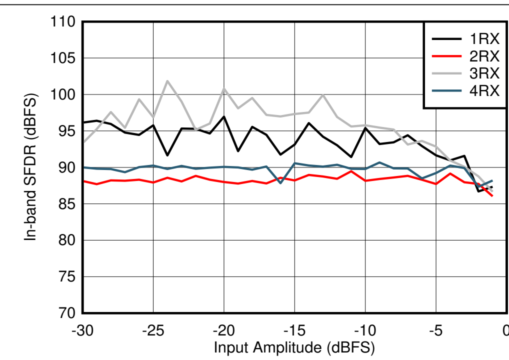
With 3.5 GHz matching, 12.5-MHz offset from tone

Figure 5-164. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



External clock mode, 25°C, 2x Decimation

Figure 5-165. RX Noise Spectral Density vs Input Level at 3.76GHz

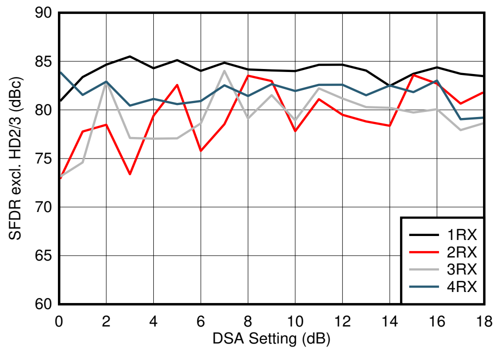


With 3.5 GHz matching

Figure 5-166. RX In-Band SFDR (±200 MHz) vs Input Level and Channel at 3.6 GHz

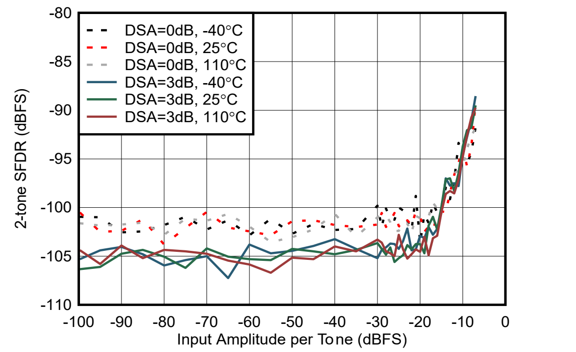
5.12.5 RX Typical Characteristics 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



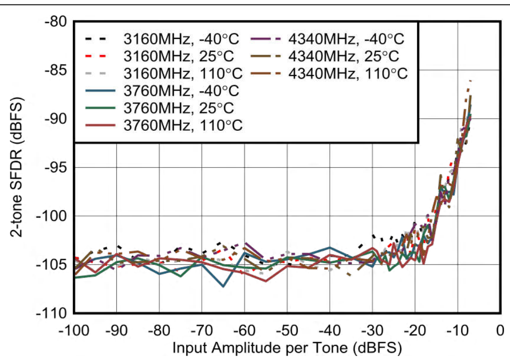
With 3.5 GHz matching

Figure 5-167. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz



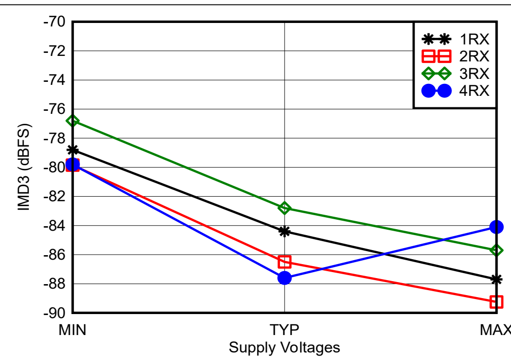
External clock mode, 20MHz tone spacing, excluding 3rd order distortion

Figure 5-168. RX 2-tone SFDR vs Input Amplitude and DSA Setting at 3.7 GHz



External clock mode, 20MHz tone spacing, excluding 3rd order distortion

Figure 5-169. RX 2-tone SFDR vs Input Amplitude and Frequency at 3.7 GHz

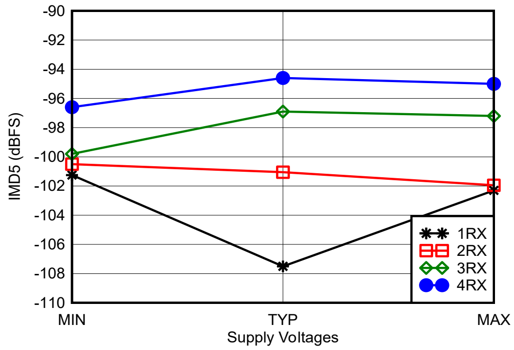


With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-170. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz

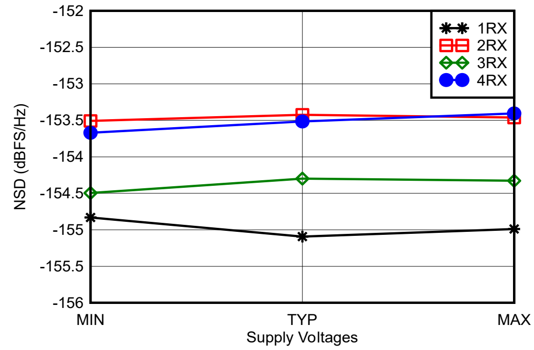
5.12.5 RX Typical Characteristics 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-171. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz

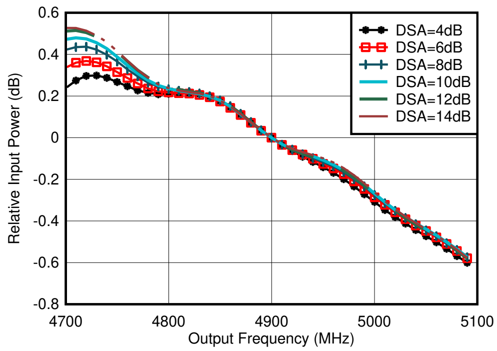


With 3.6 GHz matching, tone at –20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-172. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

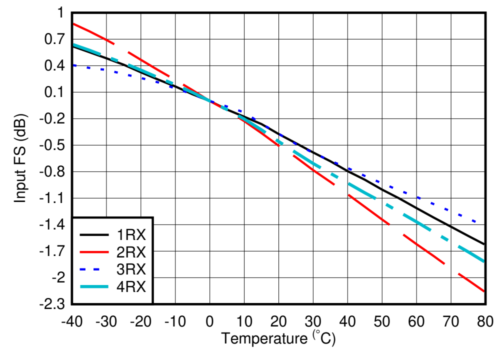
5.12.6 RX Typical Characteristics 4.9 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



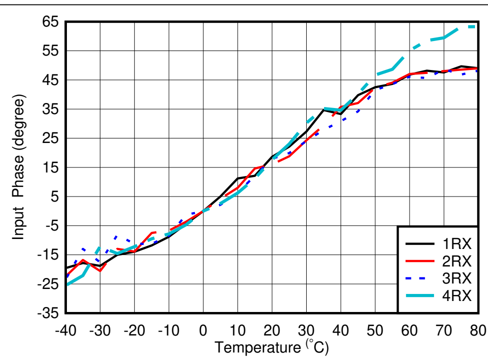
With matching, normalized to power at 4.9GHz for each DSA setting

Figure 5-173. RX Inband Gain Flatness, f_{IN} = 4900 MHz



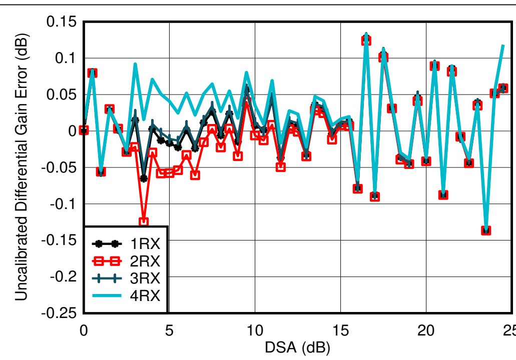
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

Figure 5-174. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at 25°C

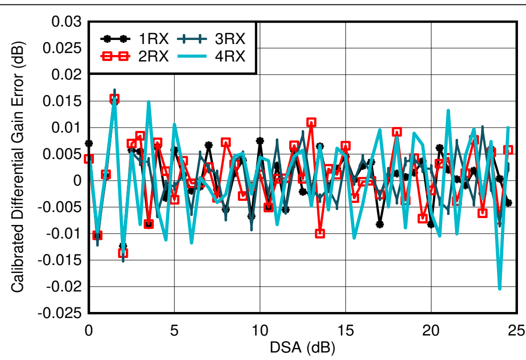
Figure 5-175. RX Input Phase vs Temperature and DSA at f_{OUT} = 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

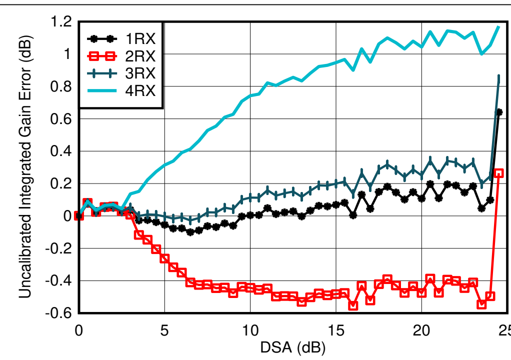
Figure 5-176. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 5-177. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



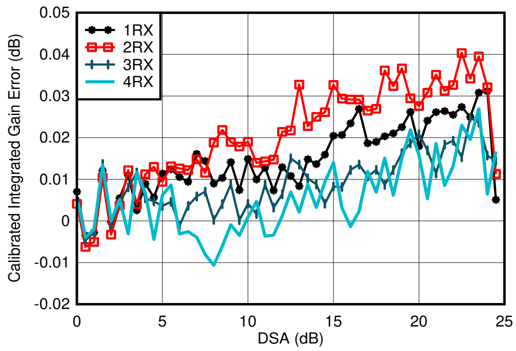
With 4.9 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 5-178. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

5.12.6 RX Typical Characteristics 4.9 GHz (continued)

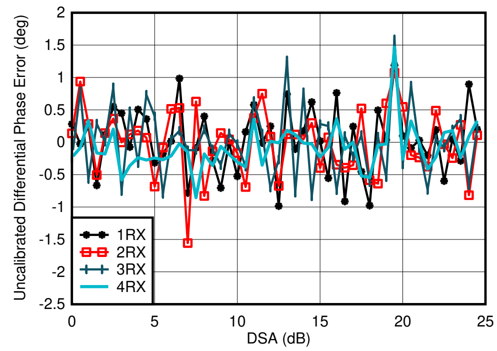
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 4.9 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

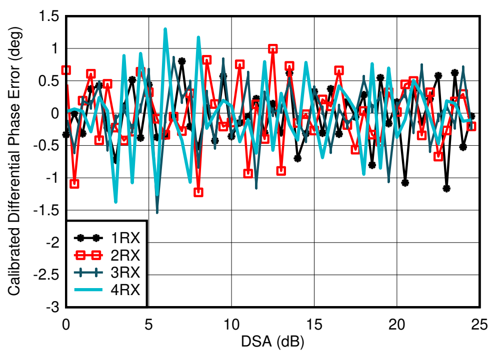
Figure 5-179. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

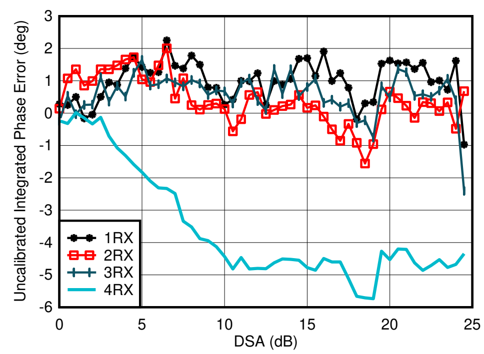
Figure 5-180. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 5-181. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz



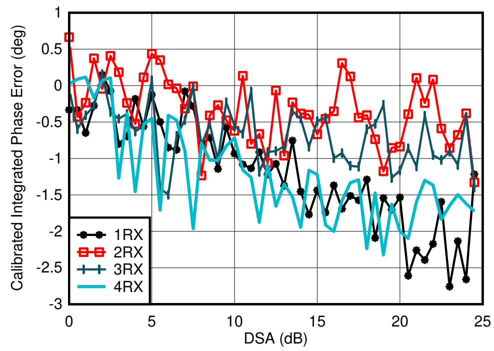
With 4.9 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-182. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz

5.12.6 RX Typical Characteristics 4.9 GHz (continued)

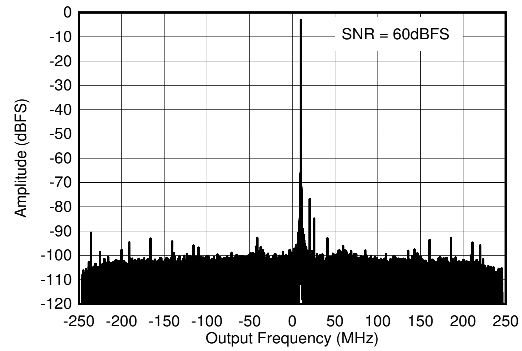
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 4.9 GHz matching

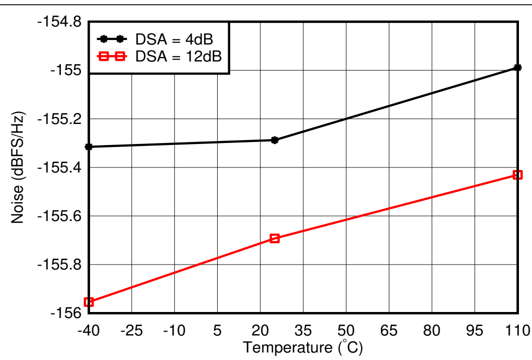
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-183. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



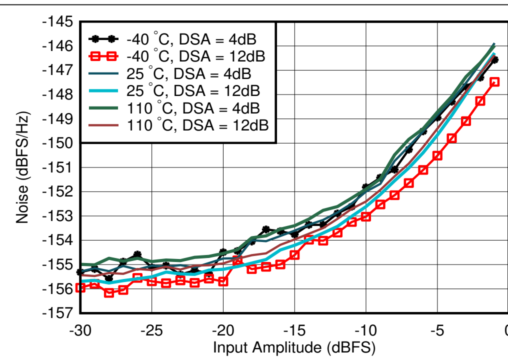
With 4.9 GHz matching, f_{IN} = 4910 MHz, A_{IN}= –3 dBFS

Figure 5-184. RX Output FFT at 4.9 GHz



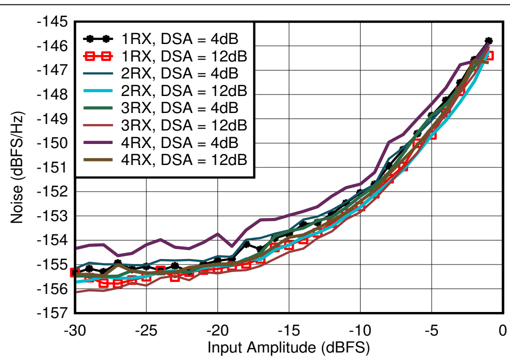
With 4.9 GHz matching, 12.5-MHz offset from tone

Figure 5-185. RX Noise Spectral Density vs Temperature at 4.9 GHz



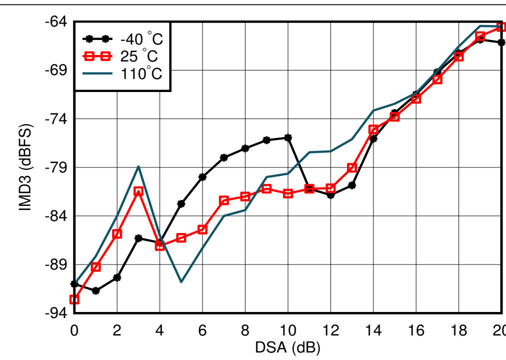
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 5-186. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz



With 4.9 GHz matching, 12.5-MHz offset from tone

Figure 5-187. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz

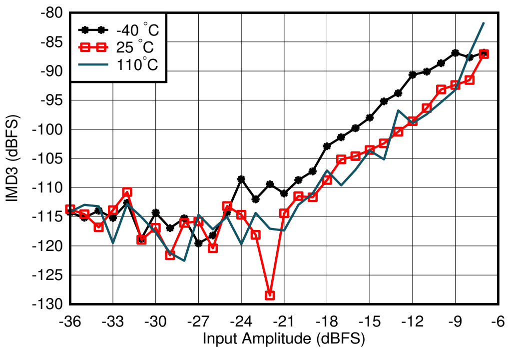


With 4.9 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 5-188. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz

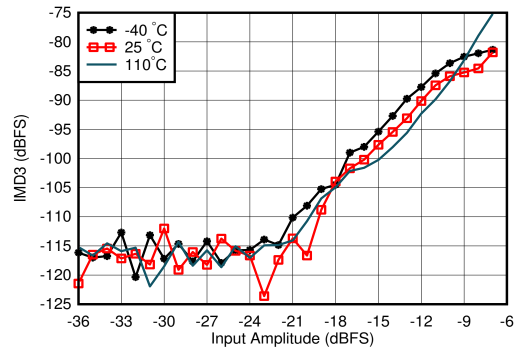
5.12.6 RX Typical Characteristics 4.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



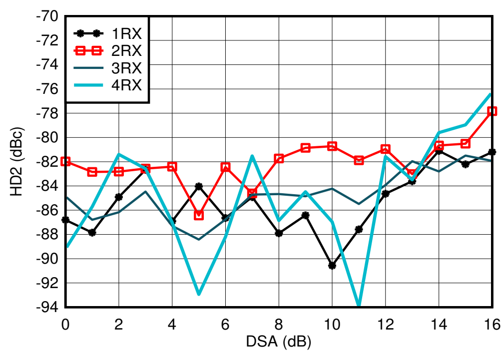
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 5-189. RX IMD3 vs Input Level and Temperature at 4.9 GHz



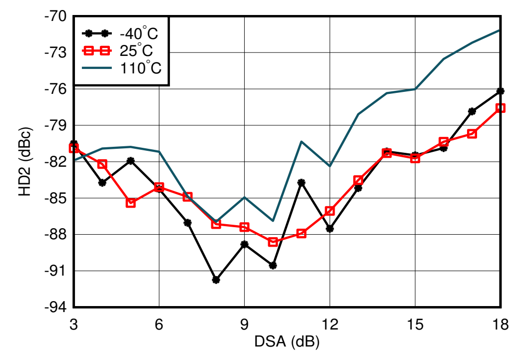
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 5-190. RX IMD3 vs Input Level and Temperature at 4.9 GHz



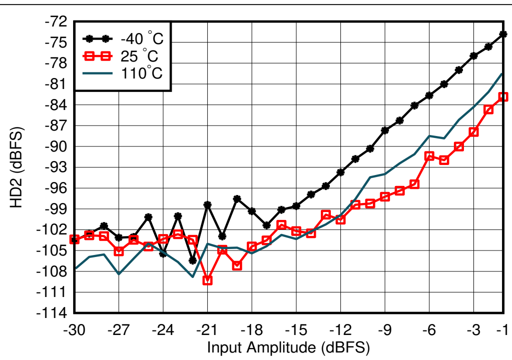
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 5-191. RX HD2 vs DSA Setting and Channel at 4.9 GHz



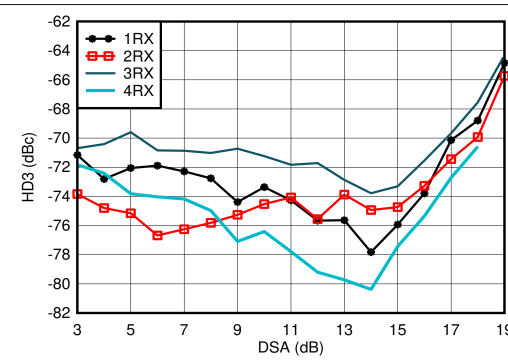
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 5-192. RX HD2 vs DSA and Temperature at 4.9 GHz



With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 5-193. RX HD2 vs Input Level and Temperature at 4.9 GHz

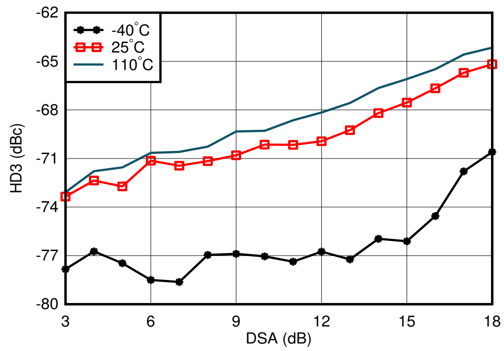


With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-194. RX HD3 vs DSA Setting and Channel at 4.9 GHz

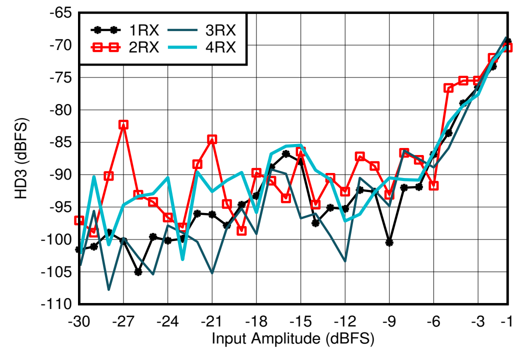
5.12.6 RX Typical Characteristics 4.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



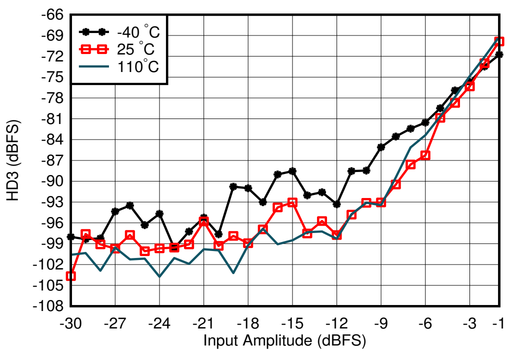
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-195. RX HD3 vs DSA Setting and Temperature at 4.9 GHz



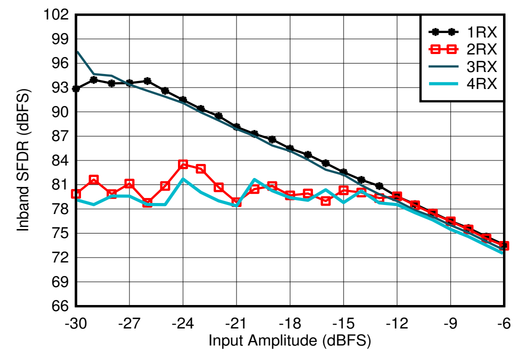
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-196. RX HD3 vs Input Level and Channel at 4.9 GHz



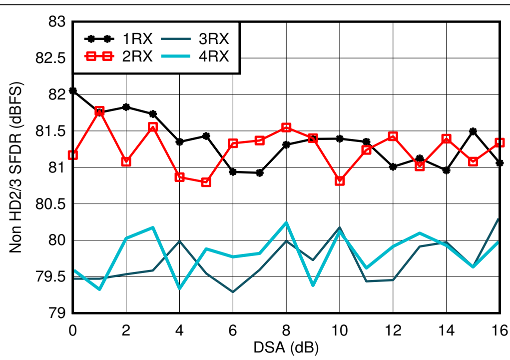
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-197. RX HD3 vs Input Level and Temperature at 4.9 GHz



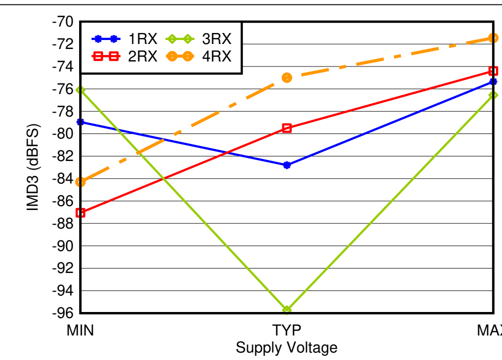
With 4.9 GHz matching, decimate by 3

Figure 5-198. RX In-Band SFDR (±400 MHz) vs Input Amplitude and Channel at 4.9 GHz



With 4.9 GHz matching

Figure 5-199. RX Non-HD2/3 vs DSA Setting at 4.9 GHz

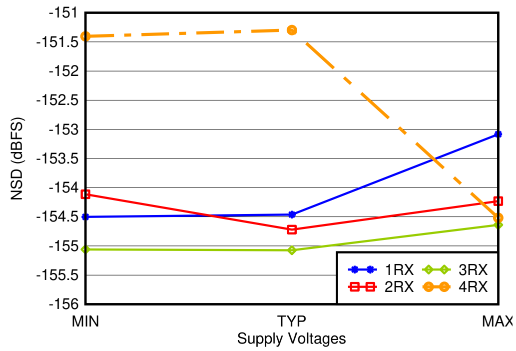


With 4.9 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-200. RX IMD3 vs Supply and Channel at 4.9 GHz

5.12.6 RX Typical Characteristics 4.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.

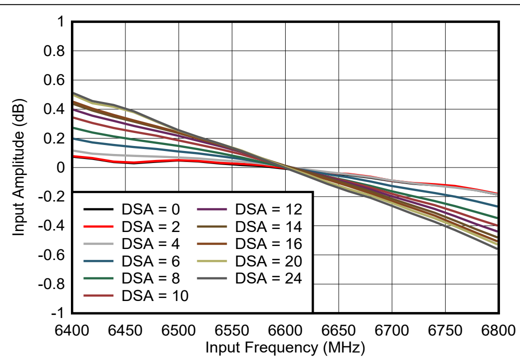


With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-201. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz

5.12.7 RX Typical Characteristics 6.8 GHz

Typical values at T_A = +25°C. Default conditions at 30 MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 500 MSPS (decimate by 6x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



Normalized to 6.6GHz

Figure 5-202. RX In-Band Gain Flatness

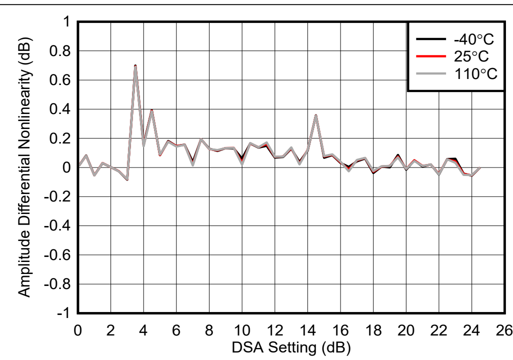
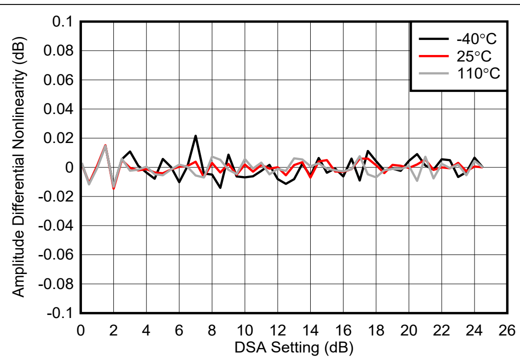


Figure 5-203. RX Uncalibrated Differential Amplitude Error at 6.851 GHz



Calibrated at 25°C, held at -40 and 110°C

Figure 5-204. RX Calibrated Differential Amplitude Error at 6.851 GHz

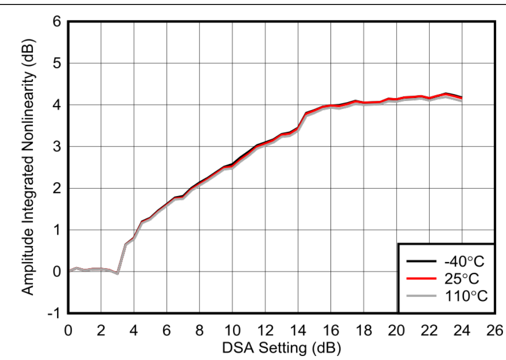
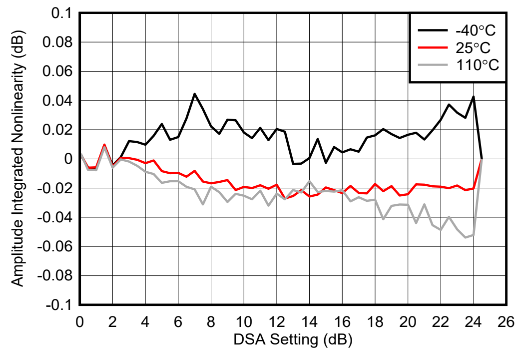


Figure 5-205. RX Uncalibrated Integrated Amplitude Error at 6.851 GHz

5.12.7 RX Typical Characteristics 6.8 GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30 MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 500 MSPS (decimate by 6x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



Calibrated at 25°C, held at -40 and 110°C

Figure 5-206. RX Calibrated Integrated Amplitude Error at 6.851 GHz

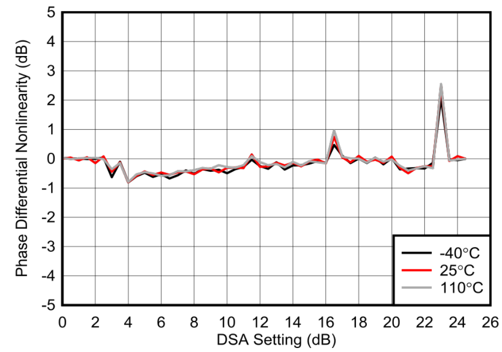
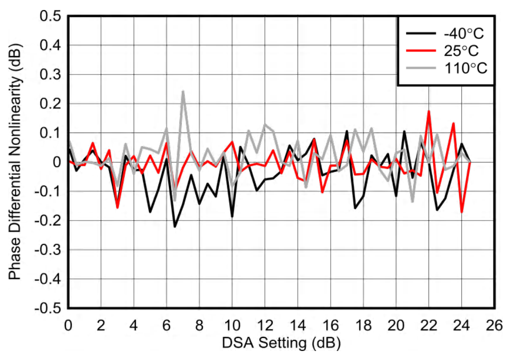


Figure 5-207. RX Uncalibrated Differential Phase Error at 6.851 GHz



Calibrated at 25°C, held at -40 and 110°C

Figure 5-208. RX Calibrated Differential Phase Error at 6.851 GHz

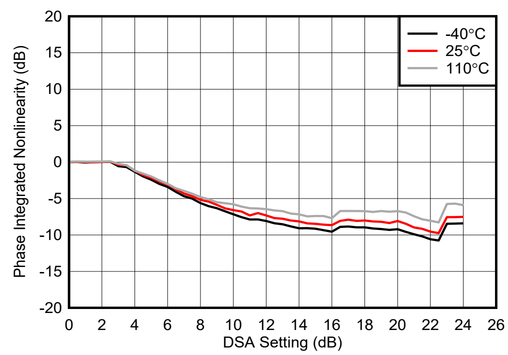
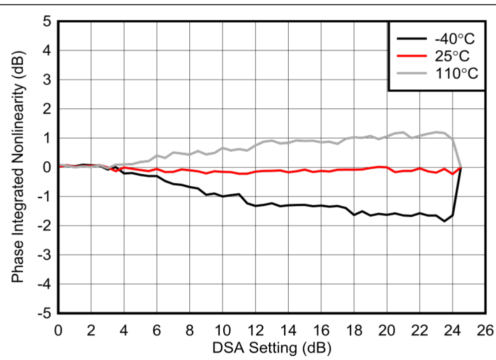
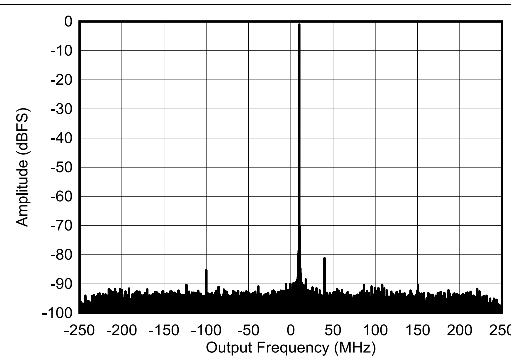


Figure 5-209. RX Uncalibrated Integrated Phase Error at 6.851 GHz



Calibrated at 25°C, held at -40 and 110°C

Figure 5-210. RX Calibrated Integrated Phase Error at 6.851 GHz

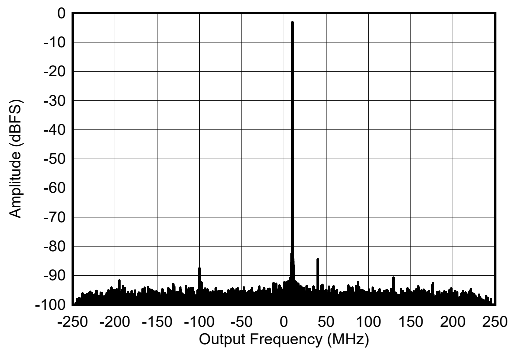


F_{NCO} = 7.1 GHz

Figure 5-211. Single Tone RX Output FFT at 7.11 GHz and -1 dBFS

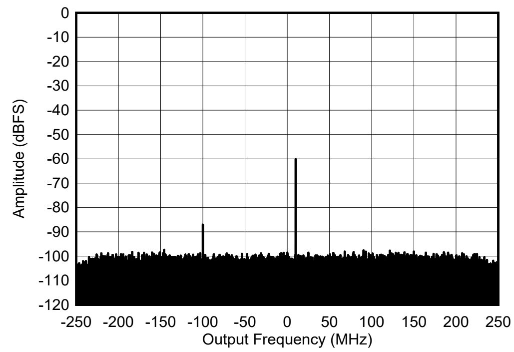
5.12.7 RX Typical Characteristics 6.8 GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30 MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 500 MSPS (decimate by 6x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



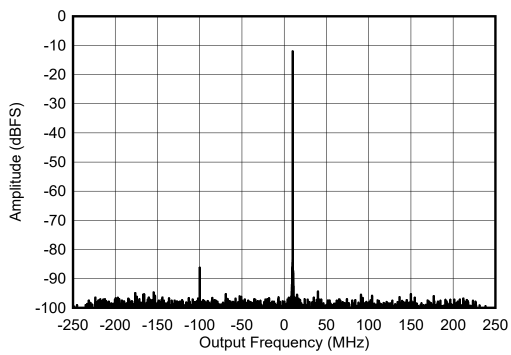
F_{NCO} = 7.1 GHz

Figure 5-212. Single Tone RX Output FFT at 7.11 GHz and -3 dBFS



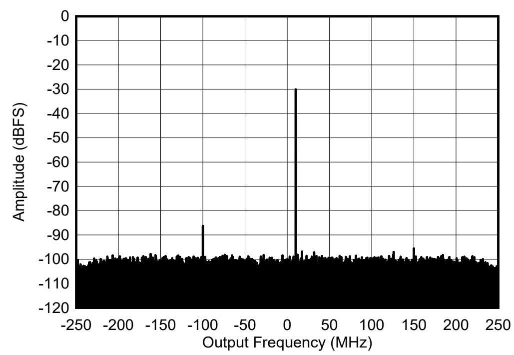
F_{NCO} = 7.1 GHz

Figure 5-213. Single Tone RX Output FFT at 7.11 GHz and -6 dBFS



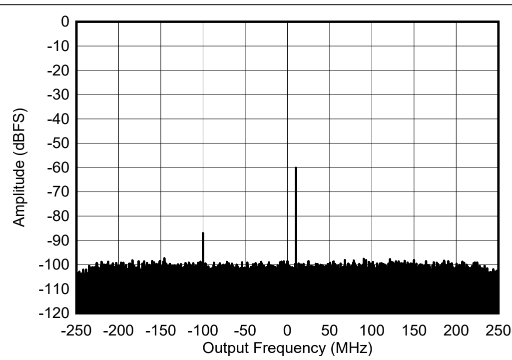
F_{NCO} = 7.1 GHz

Figure 5-214. Single Tone RX Output FFT at 7.11 GHz and -12 dBFS



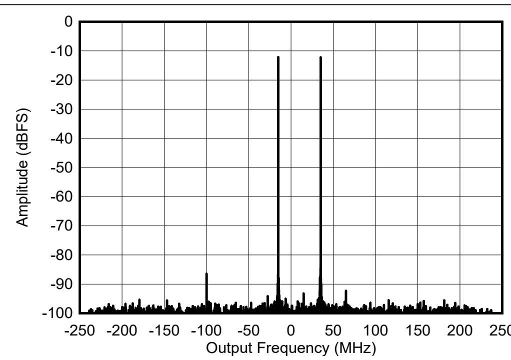
F_{NCO} = 7.1 GHz

Figure 5-215. Single Tone RX Output FFT at 7.11 GHz and -30 dBFS



F_{NCO} = 7.1 GHz

Figure 5-216. Single Tone RX Output FFT at 7.1 GHz and -60 dBFS

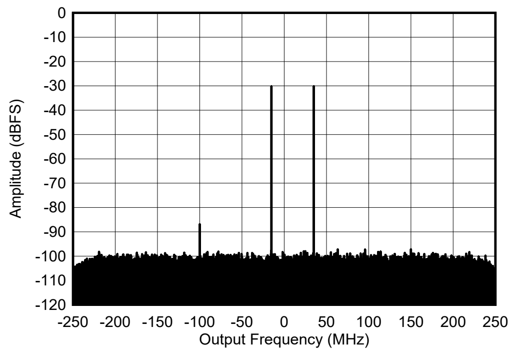


F_{NCO} = 7.1 GHz, 50 MHz Tone Spacing

Figure 5-217. Dual Tone RX Output FFT at 7.1 GHz and -12 dBFS per Tone

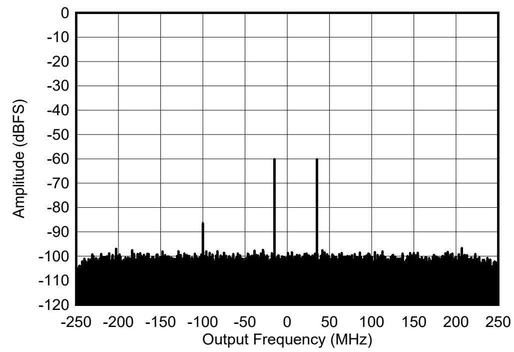
5.12.7 RX Typical Characteristics 6.8 GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30 MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 500 MSPS (decimate by 6x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



F_{NCO} = 7.1 GHz, 50 MHz Tone Spacing

Figure 5-218. Dual Tone RX Output FFT at 7.1 GHz and -30 dBFS per Tone



F_{NCO} = 7.1 GHz, 50 MHz Tone Spacing

Figure 5-219. Dual Tone RX Output FFT at 7.1 GHz and -60 dBFS per Tone

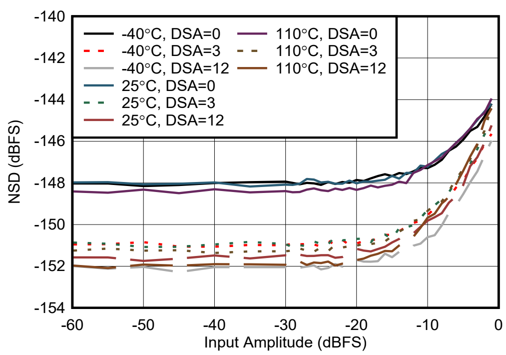
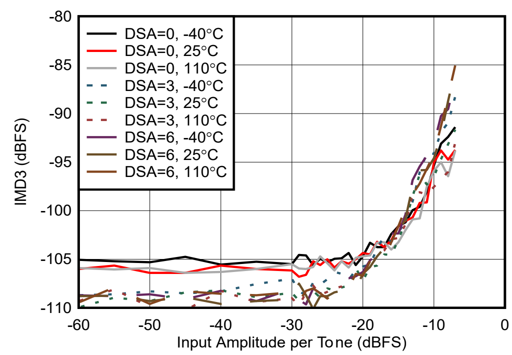
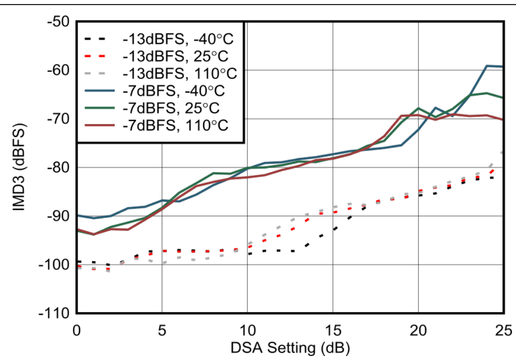


Figure 5-220. RX NSD vs Input Amplitude at 6.851 GHz



100 MHz Tone Spacing

Figure 5-221. RX IMD3 vs Input Amplitude at 6.851 GHz



100 MHz Tone Spacing

Figure 5-222. RX IMD3 vs DSA Setting at 6.851 GHz

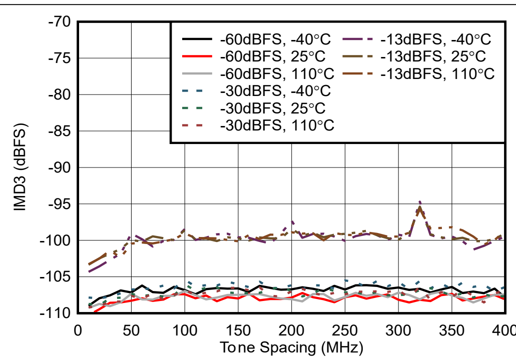


Figure 5-223. RX IMD3 vs Tone Spacing at 6.851 GHz

5.12.7 RX Typical Characteristics 6.8 GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30 MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 500 MSPS (decimate by 6x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.

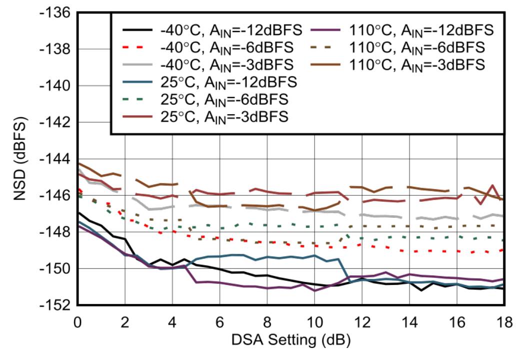


Figure 5-224. RX NSD vs DSA Setting at 6.851 GHz

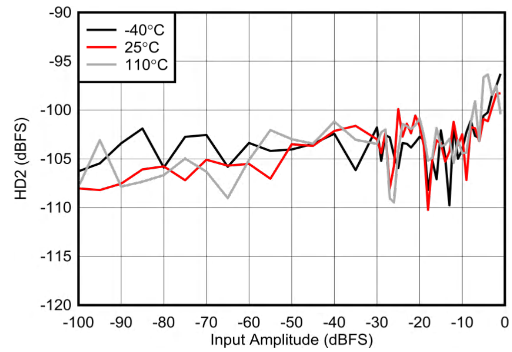
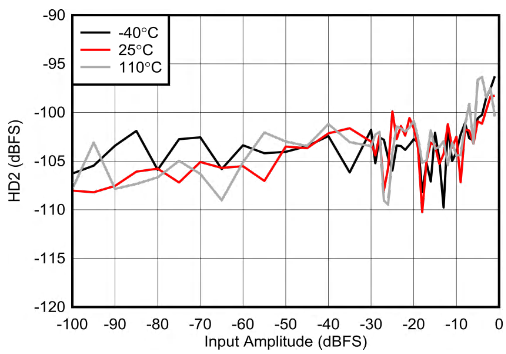
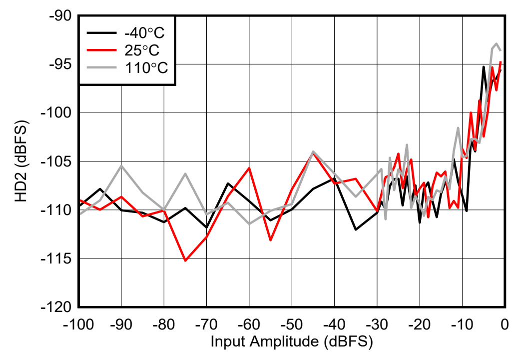


Figure 5-225. RX HD2 vs Input Amplitude at 6.851 GHz



DSA = 0 dB

Figure 5-226. RX HD2 vs Input Amplitude at 6.851 GHz



DSA = 12 dB

Figure 5-227. RX HD2 vs Input Amplitude at 6.851 GHz

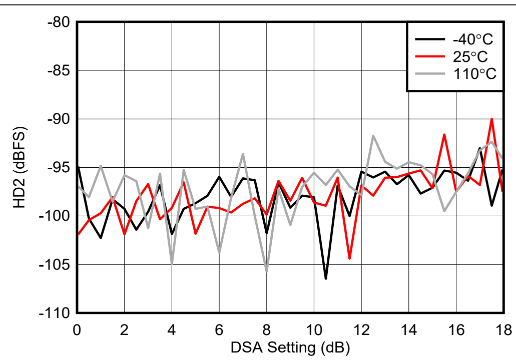


Figure 5-228. RX HD2 vs DSA Setting at 6.851 GHz

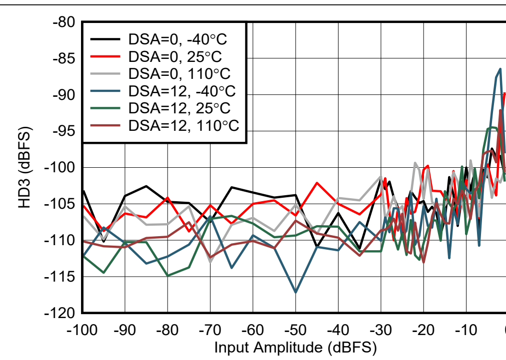


Figure 5-229. RX HD3 vs Input Amplitude at 6.851 GHz

5.12.7 RX Typical Characteristics 6.8 GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30 MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 500 MSPS (decimate by 6x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.

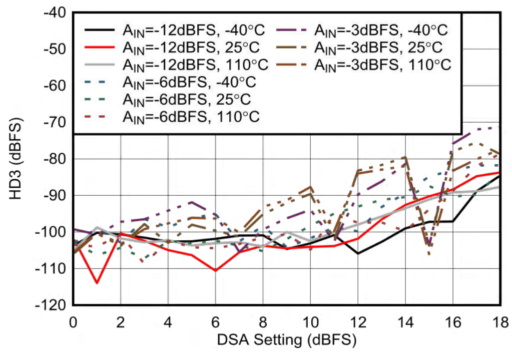
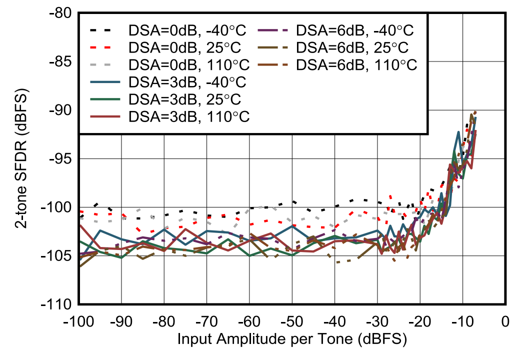


Figure 5-230. RX HD3 vs DSA Setting at 6.851 GHz



100 MHz tone spacing, excluding 3rd order distortion

Figure 5-231. RX 2-tone SFDR vs Input Amplitude at 6.85 GHz

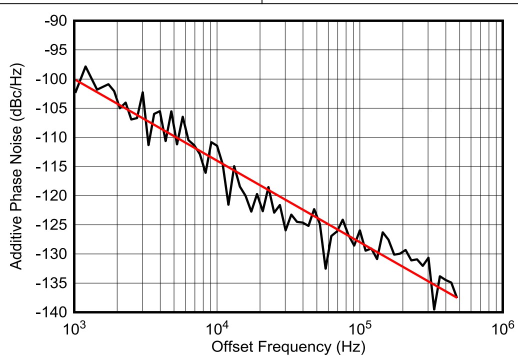
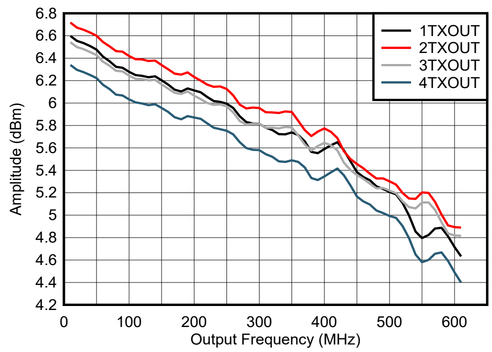


Figure 5-232. RX Additive Phase Noise at 6.85 GHz

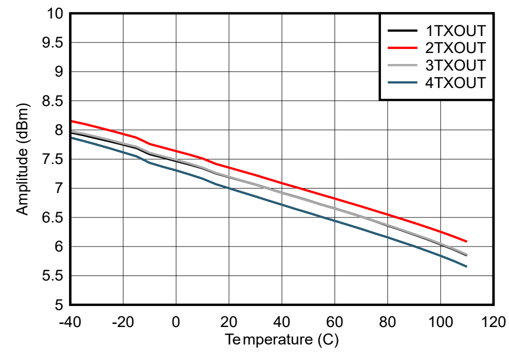
5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



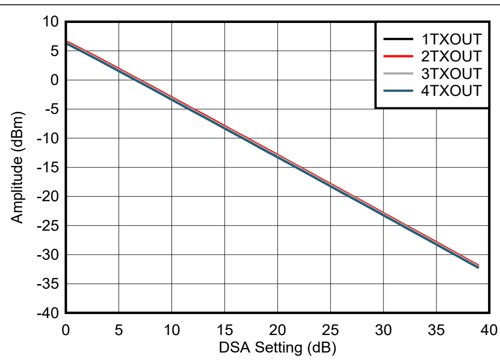
including PCB and cable losses

Figure 5-233. TX Output Fullscale vs Output Frequency: 5 MHz - 600 MHz



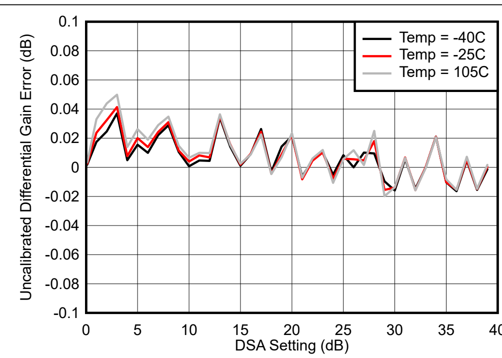
including PCB and cable losses

Figure 5-234. TX Output Fullscale vs Temperature at 30 MHz



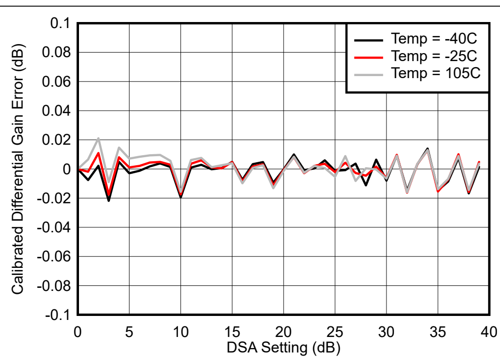
including PCB and cable losses

Figure 5-235. TX Output Fullscale vs DSA Setting at 30 MHz



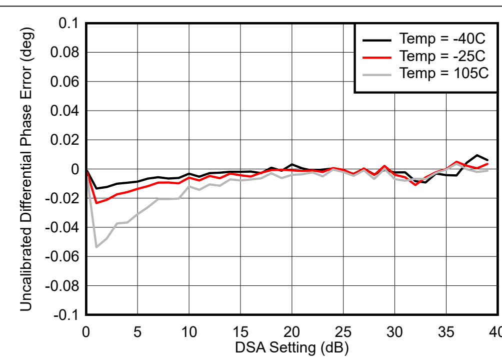
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-236. Uncalibrated TX Differential Gain Error (DNL) at 30 MHz



Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-237. Calibrated TX Differential Gain Error (DNL) at 30MHz

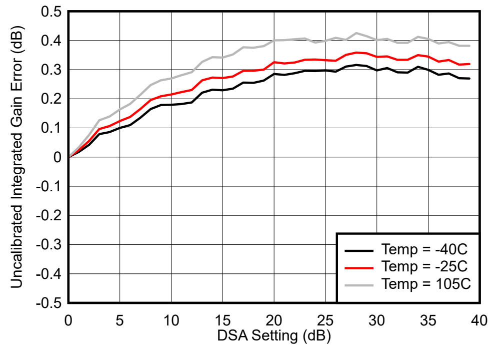


Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-238. Calibrated TX Differential Gain Error (DNL) at 30 MHz

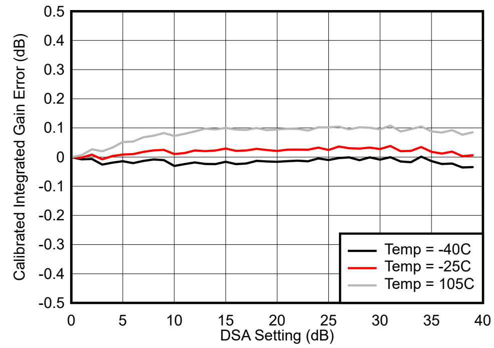
5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



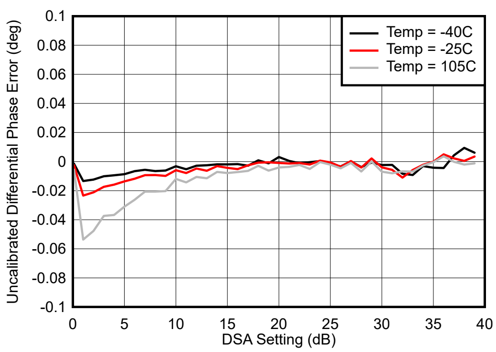
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

Figure 5-239. Uncalibrated TX Integrated Gain Error (INL) at 30 MHz



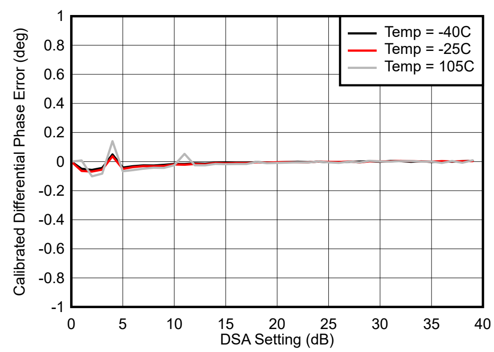
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

Figure 5-240. Calibrated TX Integrated Gain Error (INL) at 30 MHz



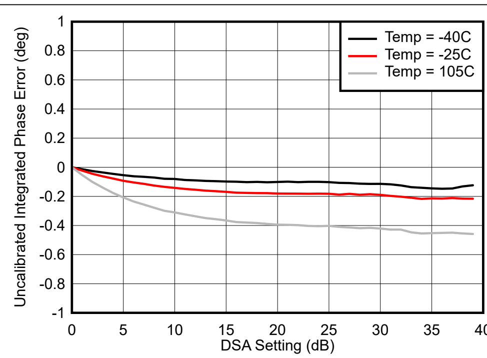
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-241. Uncalibrated TX Differential Phase Error (DNL) at 30 MHz



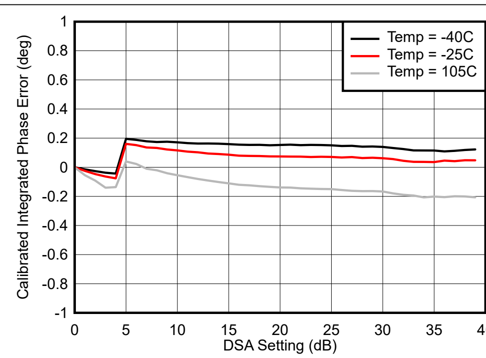
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-242. Calibrated TX Differential Phase Error (DNL) at 30 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

Figure 5-243. Uncalibrated TX Integrated Phase Error (INL) at 30 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

Figure 5-244. Calibrated TX Integrated Phase Error (INL) at 30 MHz

5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

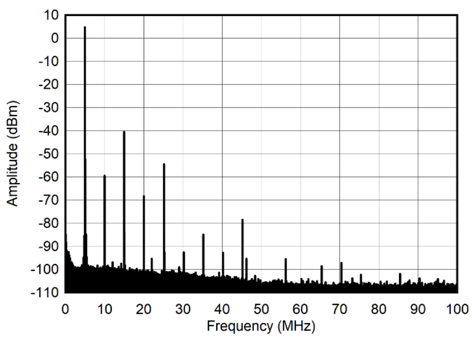


Figure 5-245. Single Tone Spectrum at 5 MHz and -1 dBFS (0 - 100 MHz)

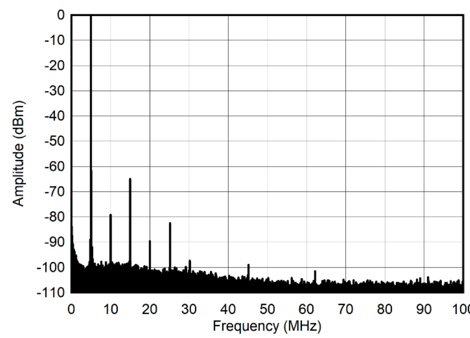


Figure 5-246. Single Tone Spectrum at 5 MHz and -6d BFS (0 - 100 MHz)

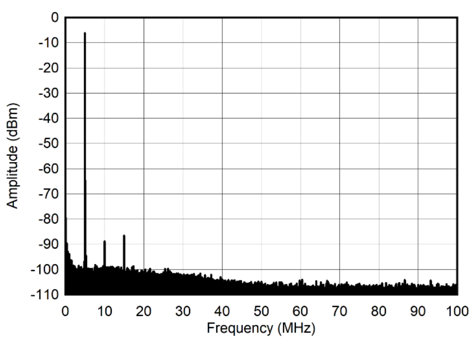


Figure 5-247. Single Tone Spectrum at 5 MHz and -12 dBFS (0 - 100 MHz)

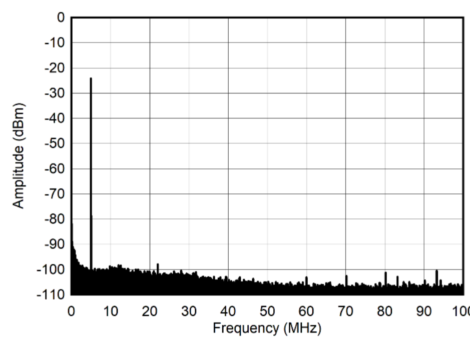


Figure 5-248. Single Tone Spectrum at 5 MHz and -30 dBFS (0 - 100 MHz)

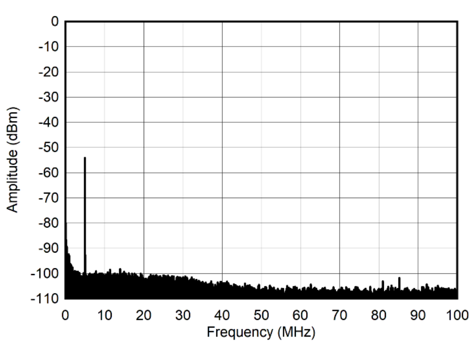


Figure 5-249. Single Tone Spectrum at 5 MHz and -60 dBFS (0 - 100 MHz)

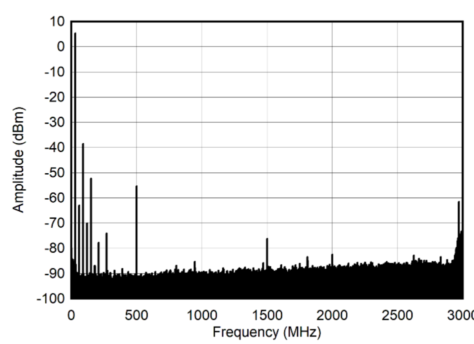


Figure 5-250. Single Tone Spectrum at 30 MHz and -1 dBFS (Nyquist)

5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

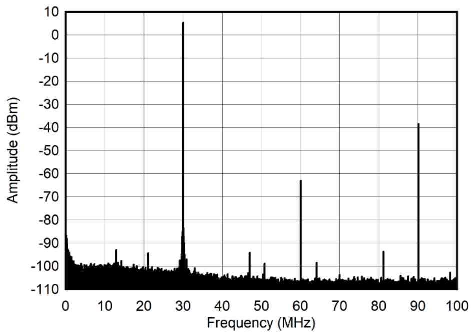


Figure 5-251. Single Tone Spectrum at 30 MHz and -1 dBFS (0 - 100 MHz)

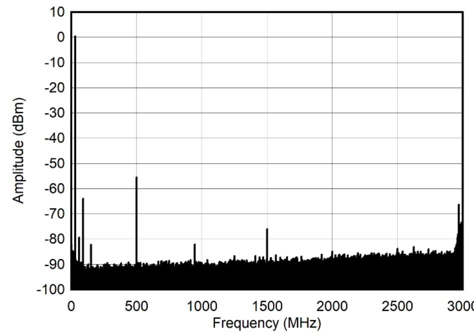


Figure 5-252. Single Tone Spectrum at 30 MHz and -6 dBFS (Nyquist)

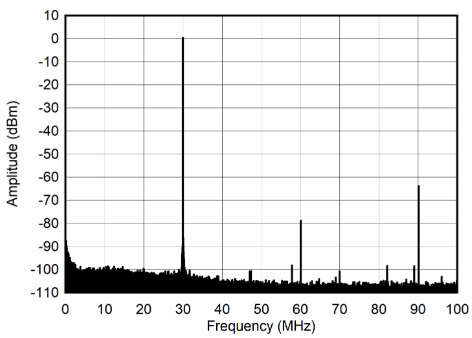


Figure 5-253. Single Tone Spectrum at 30 MHz and -6 dBFS (0 - 100 MHz)

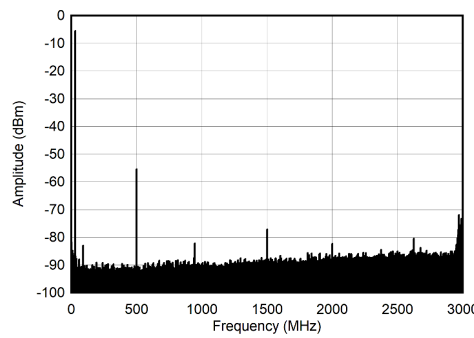


Figure 5-254. Single Tone Spectrum at 30 MHz and -12 dBFS (Nyquist)

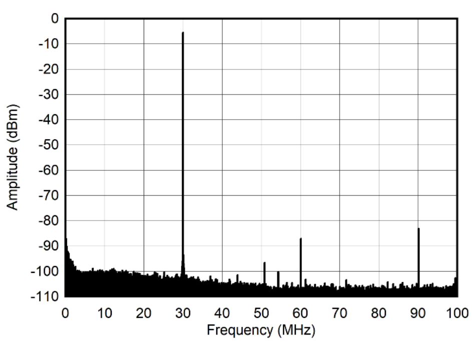


Figure 5-255. Single Tone Spectrum at 30 MHz and -12 dBFS (0 - 100 MHz)

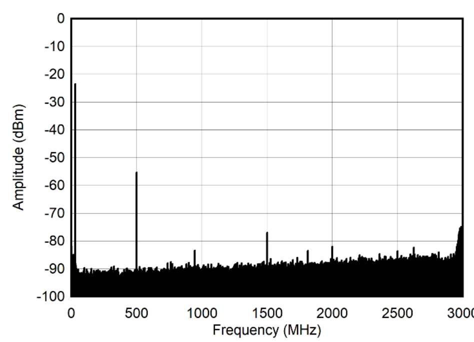


Figure 5-256. Single Tone Spectrum at 30 MHz and -30 dBFS (Nyquist)

5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

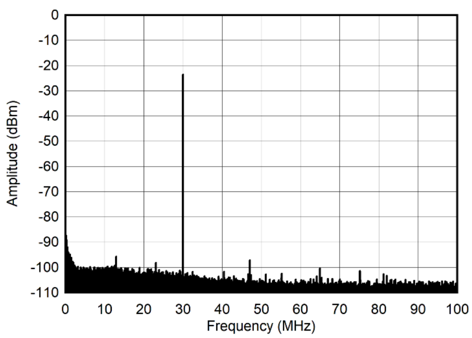


Figure 5-257. Single Tone Spectrum at 30 MHz and -30 dBFS (0 - 100 MHz)

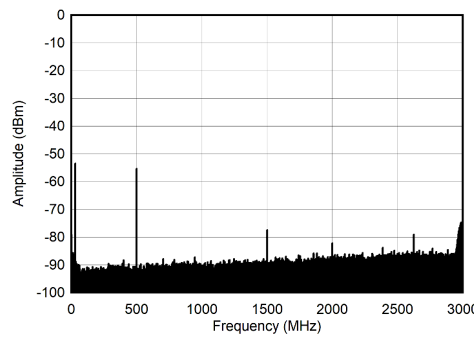


Figure 5-258. Single Tone Spectrum at 30 MHz and -60 dBFS (Nyquist)

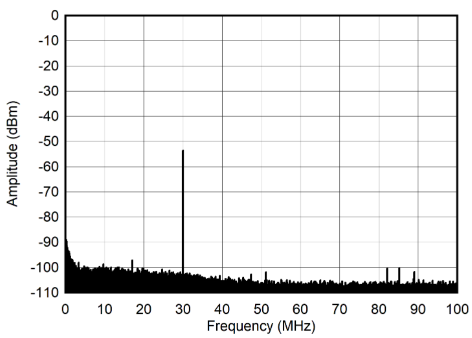


Figure 5-259. Single Tone Spectrum at 30 MHz and -60 dBFS (0 - 100 MHz)

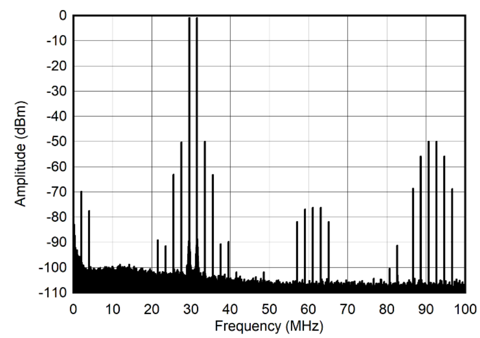


Figure 5-260. Dual Tone Spectrum at 30 MHz and -7 dBFS (0 - 100 MHz)

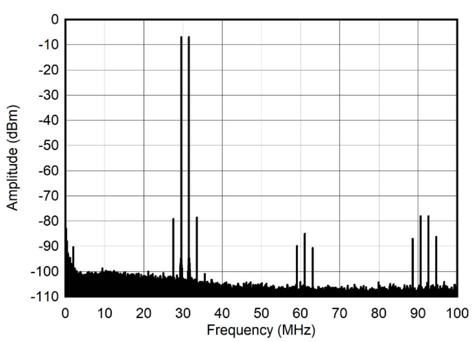


Figure 5-261. Dual Tone Spectrum at 30 MHz and -13 dBFS (0 - 100 MHz)

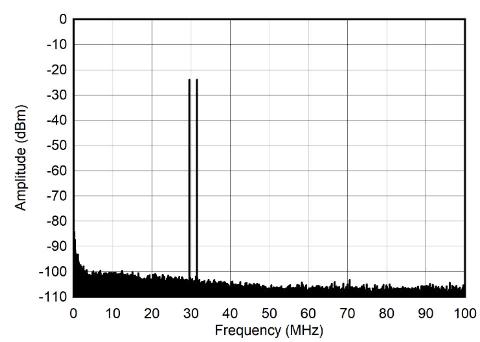


Figure 5-262. Dual Tone Spectrum at 30 MHz and -30 dBFS (0 - 100 MHz)

5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

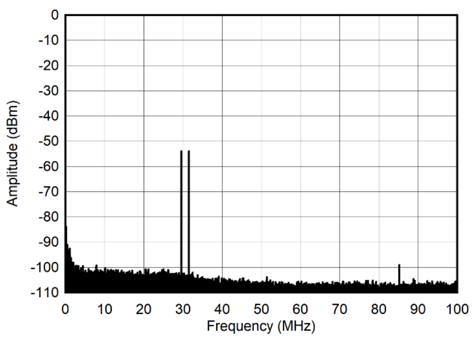
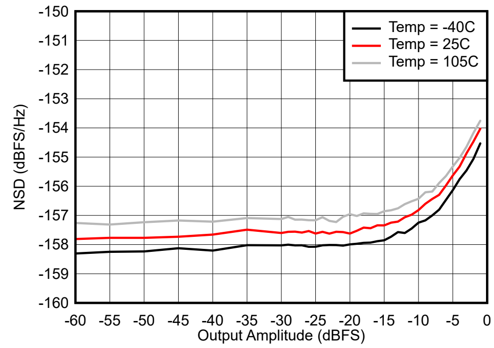
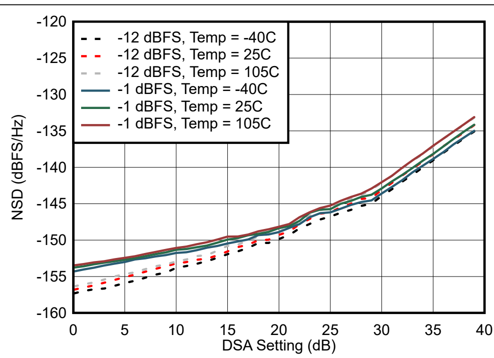


Figure 5-263. Dual Tone Spectrum at 30 MHz and -60d BFS (0 - 100 MHz)



measured at +50 MHz offset

Figure 5-264. Noise Spectral Density vs Digital Amplitude at 30 MHz



measured at +50 MHz offset

Figure 5-265. Noise Spectral Density vs DSA Setting at 30 MHz

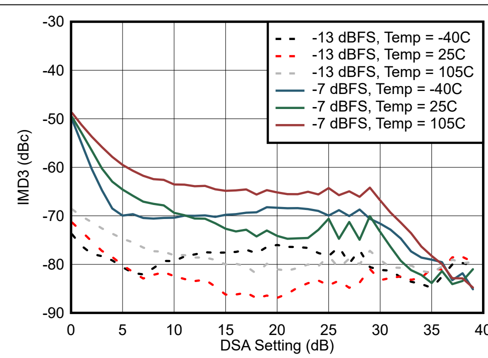


Figure 5-266. IMD3 vs DSA Setting at 30 MHz

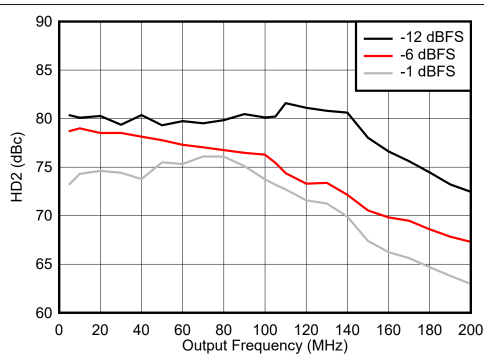


Figure 5-267. HD2 vs Frequency 0 - 200 MHz

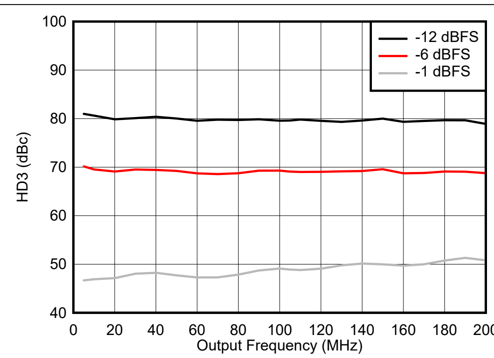
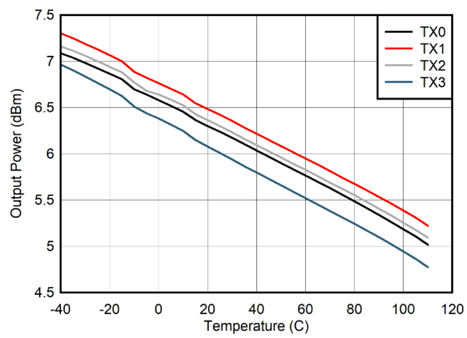


Figure 5-268. HD3 vs Frequency 0 - 200 MHz

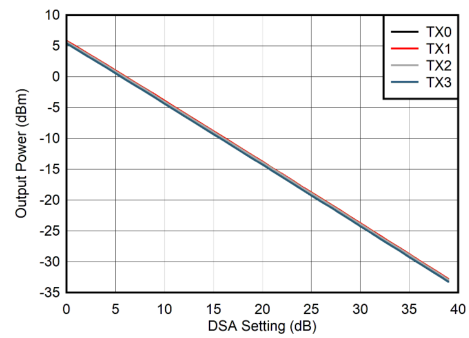
5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



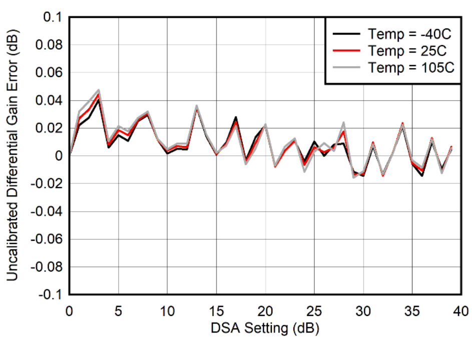
including PCB and cable losses

Figure 5-269. TX Output Fullscale vs Temperature at 400 MHz



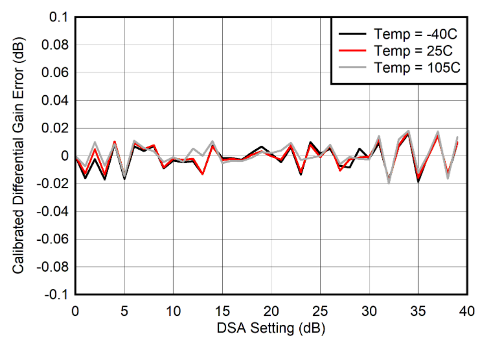
including PCB and cable losses

Figure 5-270. TX Output Fullscale vs DSA Setting at 400 MHz



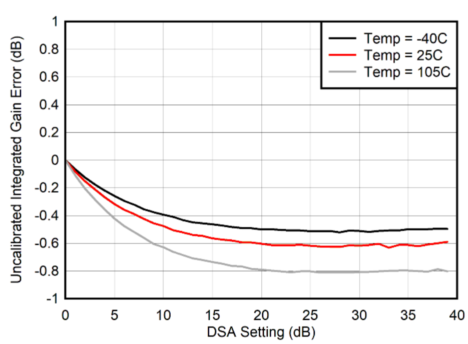
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-271. Uncalibrated TX Differential Gain Error (DNL) at 400 MHz



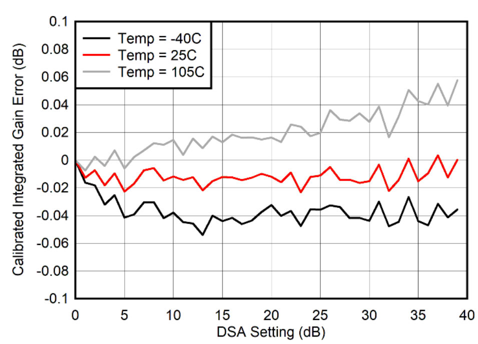
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-272. Calibrated TX Differential Gain Error (DNL) at 400 MHz



Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

Figure 5-273. Uncalibrated TX Integrated Gain Error (INL) at 400 MHz

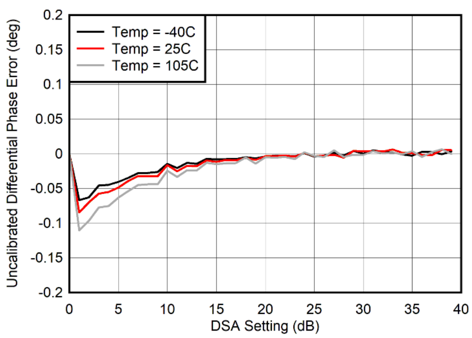


Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

Figure 5-274. Calibrated TX Integrated Gain Error (INL) at 400 MHz

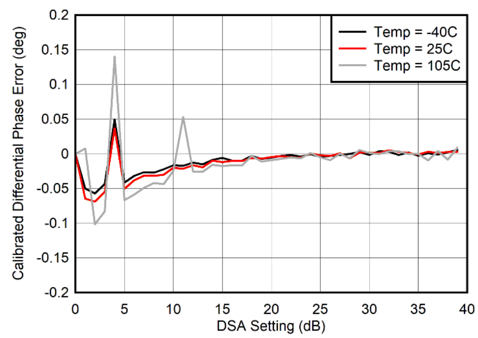
5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



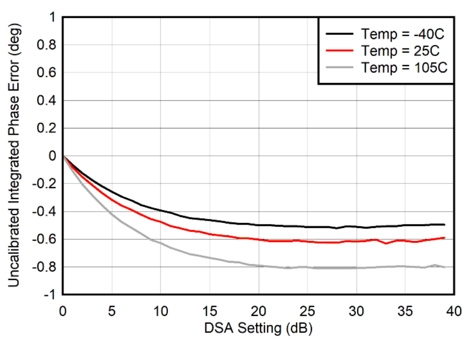
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-275. Uncalibrated TX Differential Phase Error (DNL) at 400 MHz



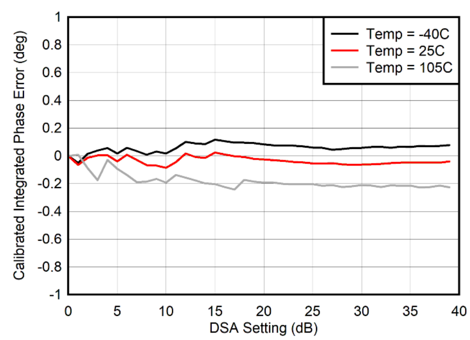
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-276. Calibrated TX Differential Phase Error (DNL) at 400 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

Figure 5-277. Uncalibrated TX Integrated Phase Error (INL) at 400 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

Figure 5-278. Calibrated TX Integrated Phase Error (INL) at 400 MHz

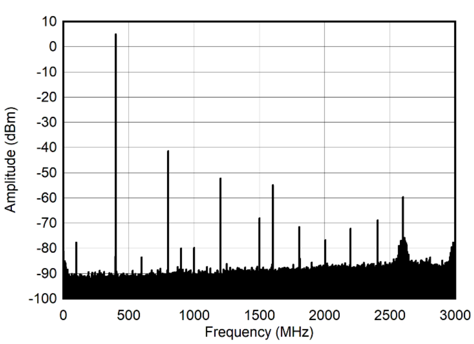


Figure 5-279. Single Tone Spectrum at 400 MHz and -1 dBFS (Nyquist)

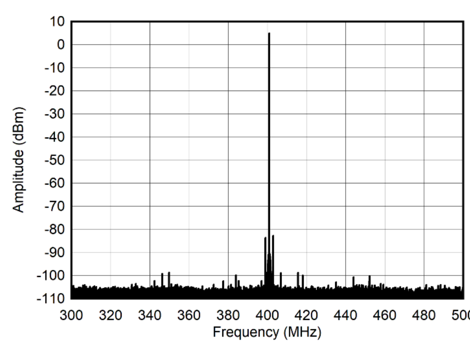


Figure 5-280. Single Tone Spectrum at 400 MHz and -1 dBFS (±100MHz)

5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1^{st} Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

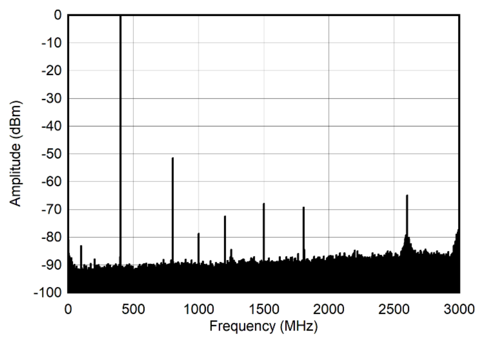


Figure 5-281. Single Tone Spectrum at 400 MHz and -6 dBFS (Nyquist)

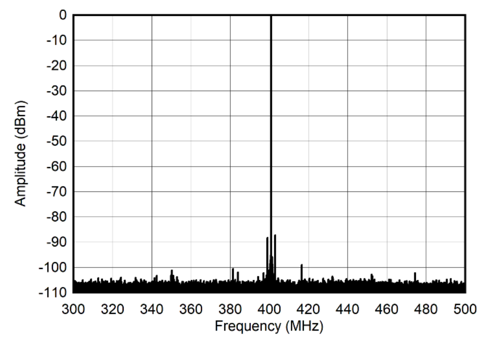


Figure 5-282. Single Tone Spectrum at 400 MHz and -6 dBFS (±100MHz)

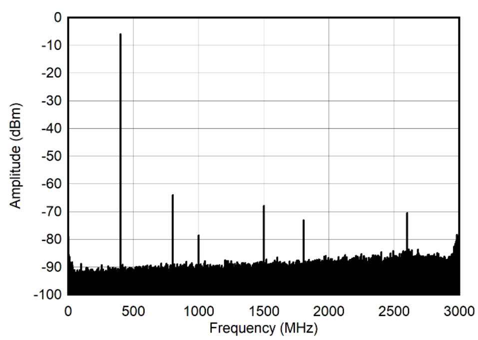


Figure 5-283. Single Tone Spectrum at 400 MHz and -12 dBFS (Nyquist)

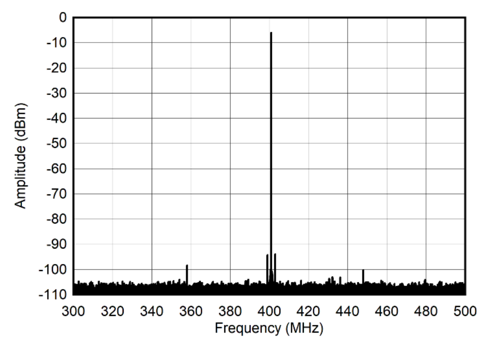


Figure 5-284. Single Tone Spectrum at 400 MHz and -12 dBFS (±100MHz)

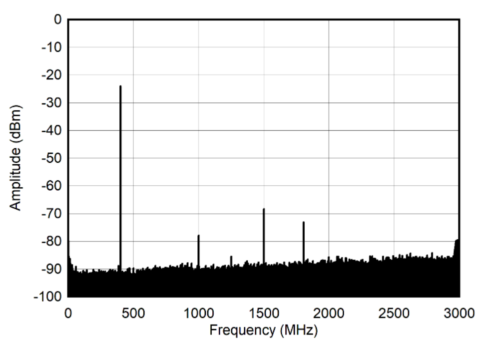


Figure 5-285. Single Tone Spectrum at 400 MHz and -30 dBFS (Nyquist)

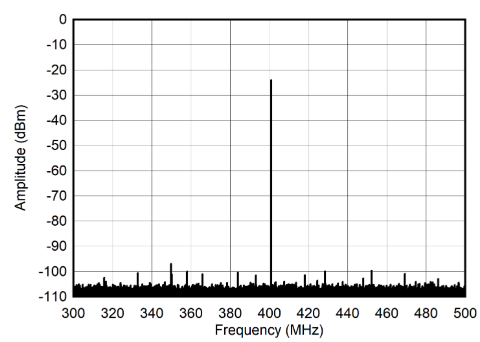


Figure 5-286. Single Tone Spectrum at 400 MHz and -30 dBFS (±100MHz)

5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1^{st} Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

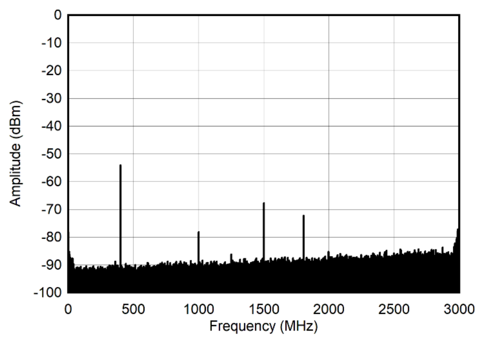


Figure 5-287. Single Tone Spectrum at 400 MHz and -60 dBFS (Nyquist)

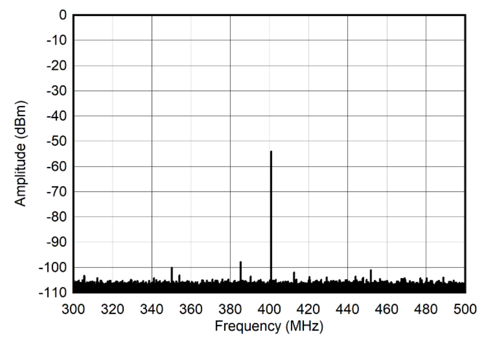
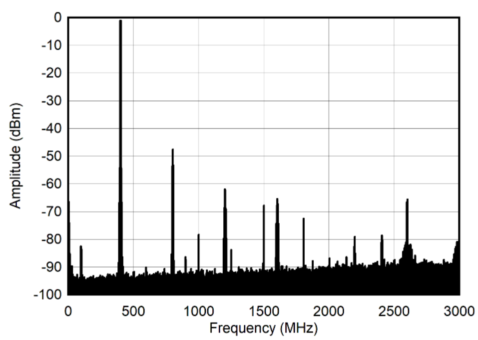
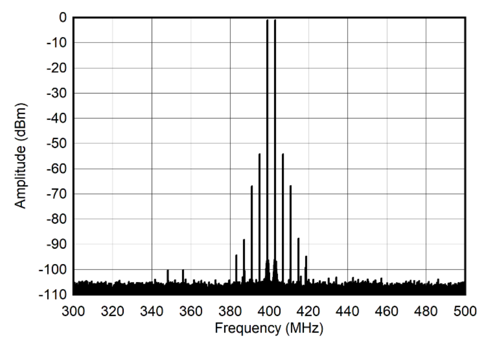


Figure 5-288. Single Tone Spectrum at 400 MHz and -60 dBFS (±100MHz)



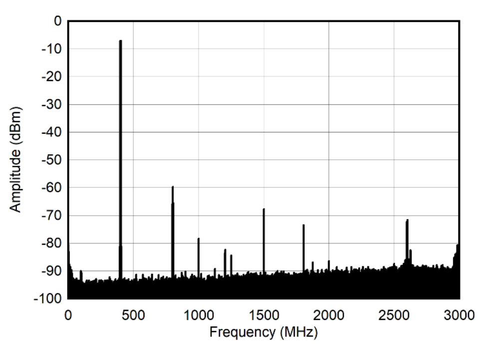
Tone Spacing = 4 MHz

Figure 5-289. Dual Tone Spectrum at 400 MHz and -7 dBFS (Nyquist)



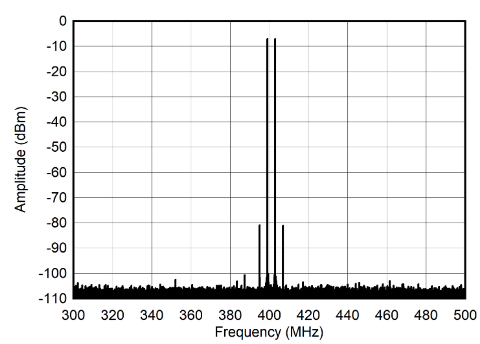
Tone Spacing = 4 MHz

Figure 5-290. Dual Tone Spectrum at 400 MHz and -7 dBFS (±100MHz)



Tone Spacing = 4 MHz

Figure 5-291. Dual Tone Spectrum at 400 MHz and -13 dBFS (Nyquist)

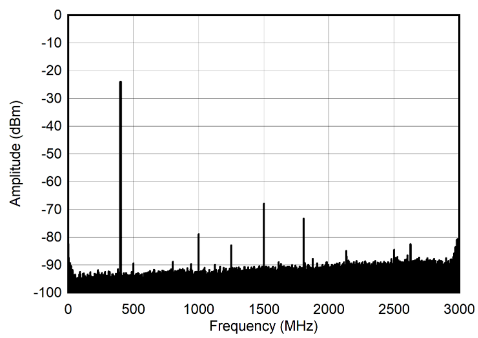


Tone Spacing = 4 MHz

Figure 5-292. Dual Tone Spectrum at 400 MHz and -13 dBFS (±100 MHz)

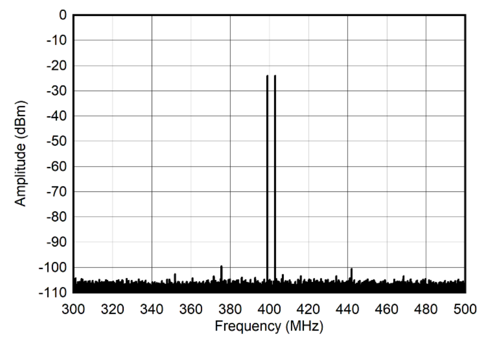
5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1[st] Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



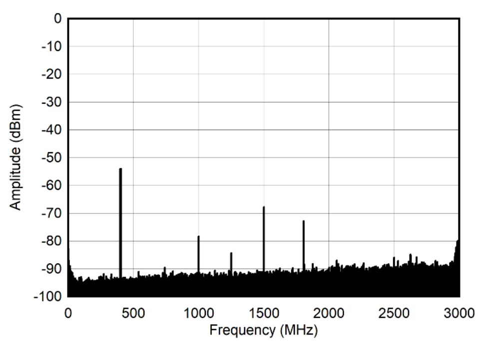
Tone Spacing = 4 MHz

Figure 5-293. Dual Tone Spectrum at 400 MHz and -30 dBFS (Nyquist)



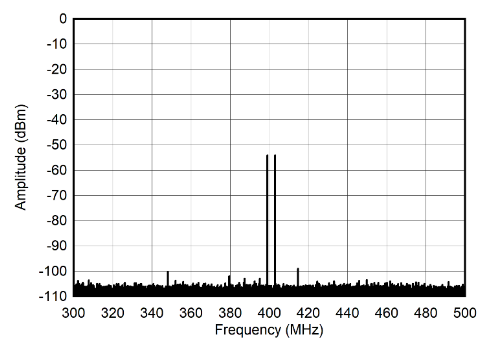
Tone Spacing = 4 MHz

Figure 5-294. Dual Tone Spectrum at 400 MHz and -30 dBFS (±100MHz)



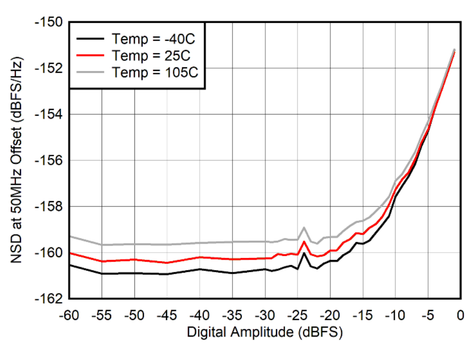
Tone Spacing = 4 MHz

Figure 5-295. Dual Tone Spectrum at 400 MHz and -60 dBFS (Nyquist)



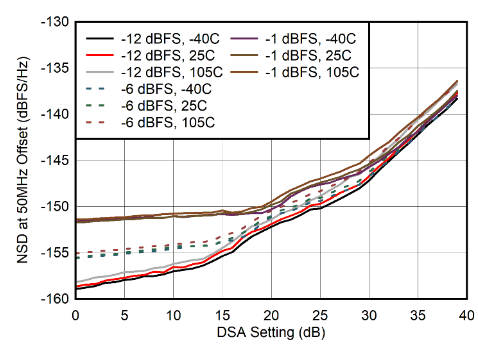
Tone Spacing = 4 MHz

Figure 5-296. Dual Tone Spectrum at 400 MHz and -60 dBFS (±100MHz)



measured at 50 MHz offset

Figure 5-297. Noise Spectral Density vs Digital Amplitude at 400 MHz

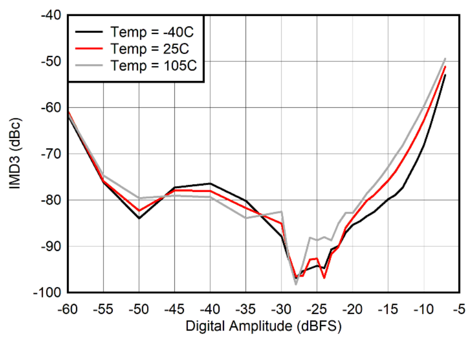


measured at 50 MHz offset

Figure 5-298. Noise Spectral Density vs DSA Setting at 400 MHz

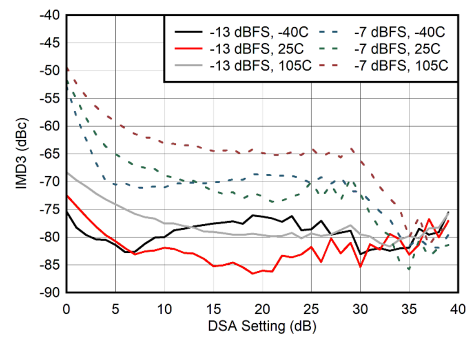
5.12.8 TX Typical Characteristics at 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



Tone Spacing = 4 MHz

Figure 5-299. IMD3 vs Digital Amplitude at 400 MHz



Tone Spacing = 4 MHz

Figure 5-300. IMD3 vs DSA Setting at 400 MHz

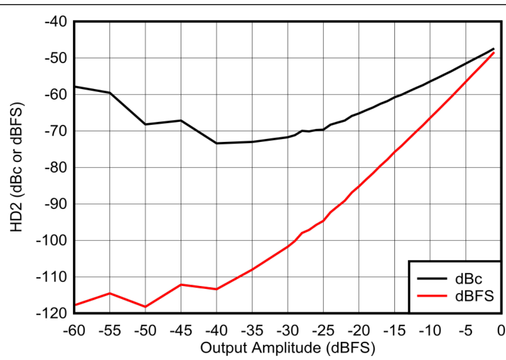


Figure 5-301. HD2 vs Amplitude at 400 MHz

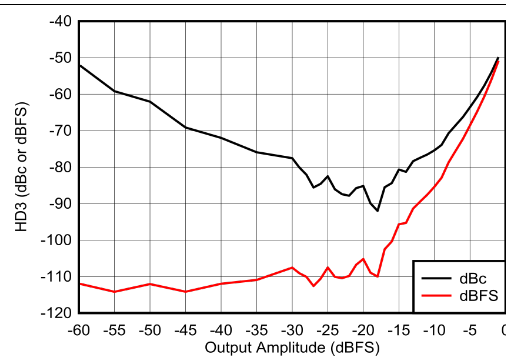
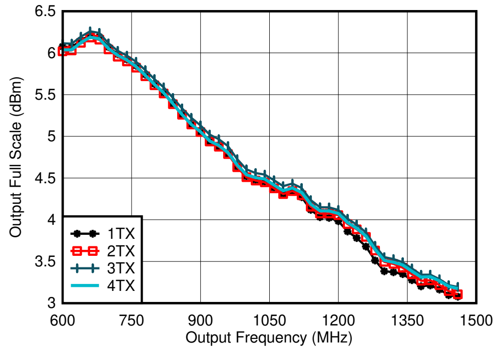


Figure 5-302. HD3 vs Amplitude at 400 MHz

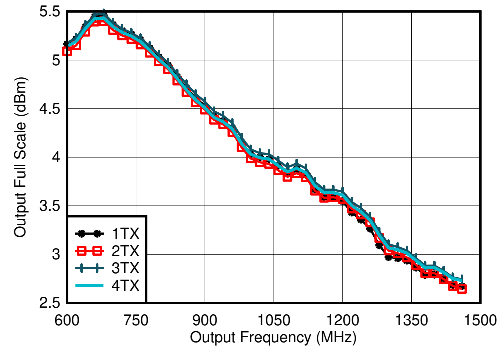
5.12.9 TX Typical Characteristics at 800 MHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



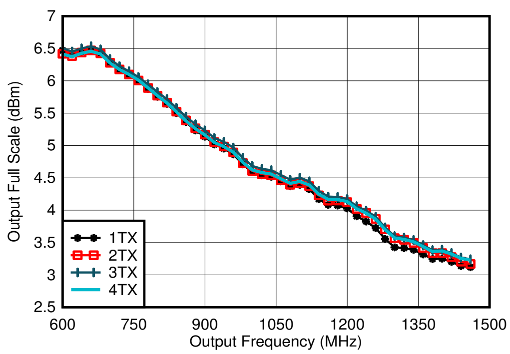
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

Figure 5-303. TX Full Scale vs RF Frequency and Channel at 5898.24 MSPS, Straight Mode



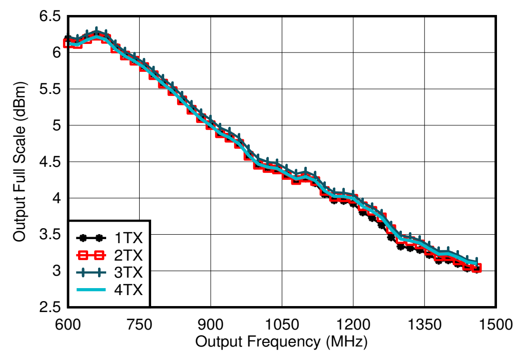
Including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

Figure 5-304. TX Full Scale vs RF Frequency and Channel at 8847.36 MSPS, Straight Mode



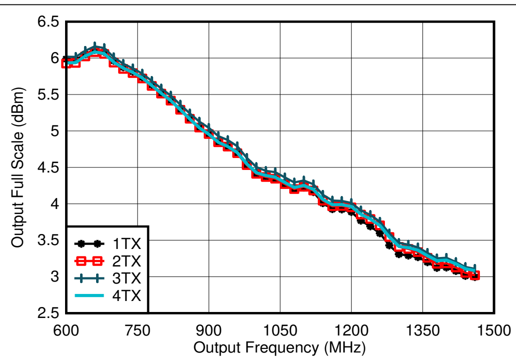
Including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

Figure 5-305. TX Full Scale vs RF Frequency and Channel at 5898.24 MSPS, Interleave Mode



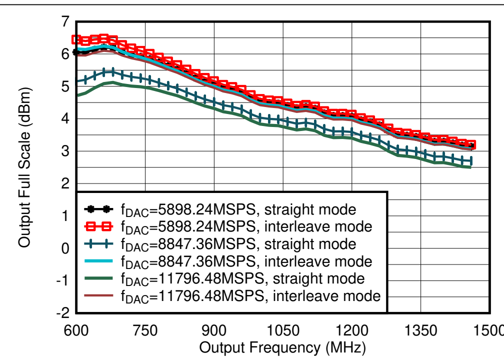
Including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

Figure 5-306. TX Full Scale vs RF Frequency and Channel at 8847.36 MSPS, Interleave Mode



Including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

Figure 5-307. TX Full Scale vs RF Frequency and Channel at 11796.48 MSPS, Interleave Mode

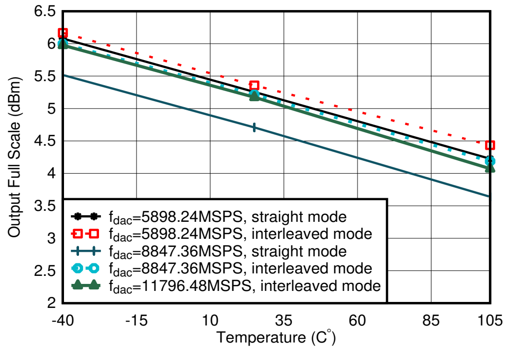


including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

Figure 5-308. TX Output Fullscale vs Output Frequency

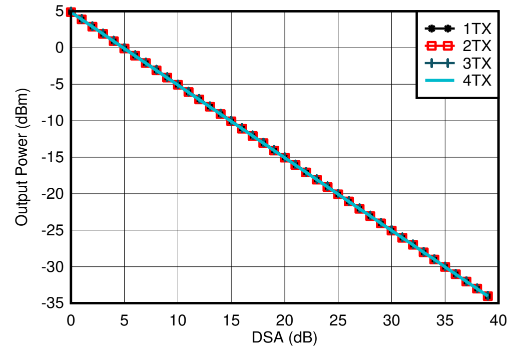
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



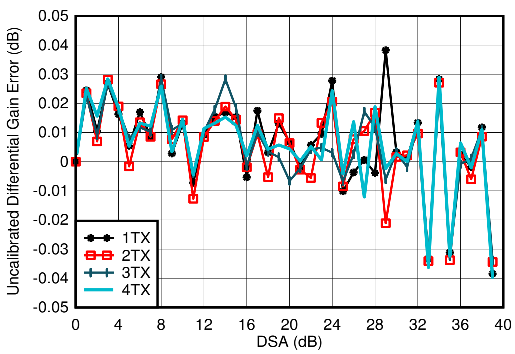
including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

Figure 5-309. TX Output Fullscale vs Temperature



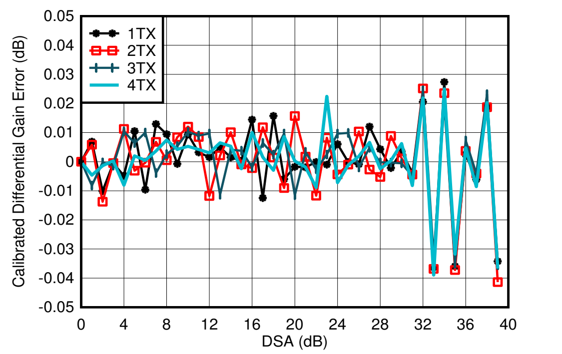
f_{DAC} = 11796.48 MSPS, interleave mode, A_{out} = -0.5 dFBS, matching 0.8 GHz

Figure 5-310. TX Output Power vs DSA Setting and Channel at 0.85 GHz



f_{DAC}=5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-311. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz

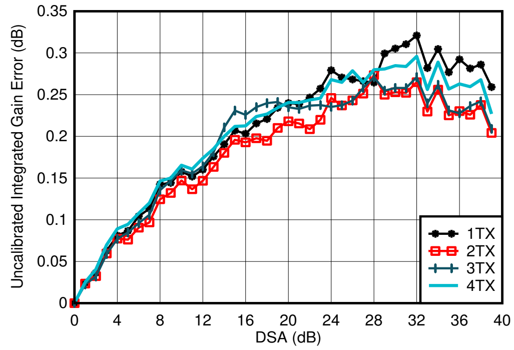


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-312. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz

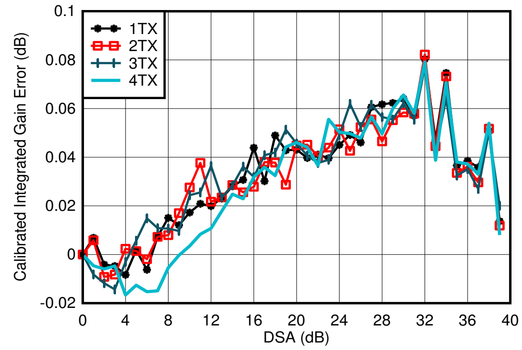
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



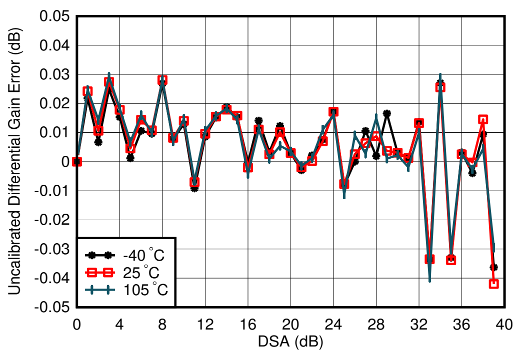
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Settings

Figure 5-313. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



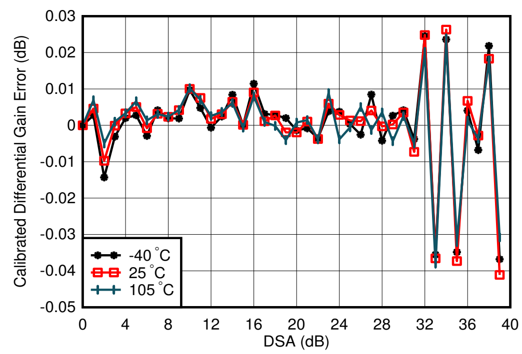
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

Figure 5-314. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-315. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz

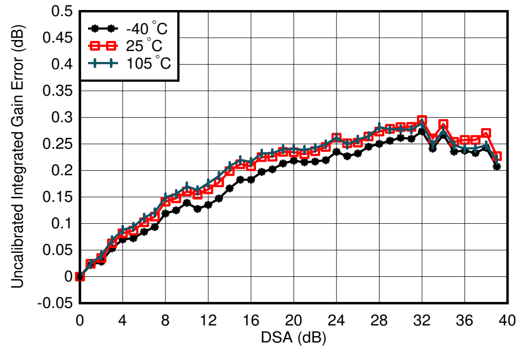


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-316. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz

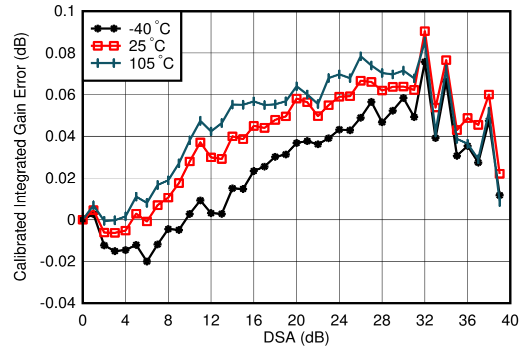
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



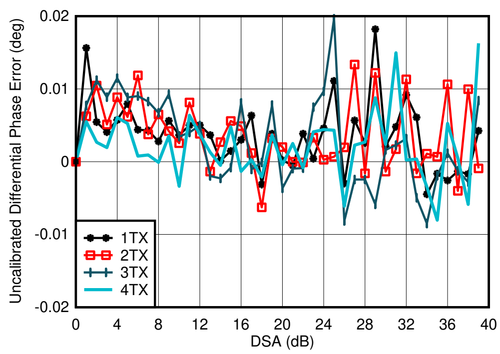
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

Figure 5-317. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz



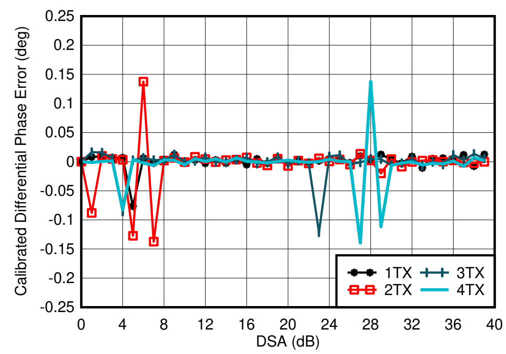
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

Figure 5-318. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-319. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz

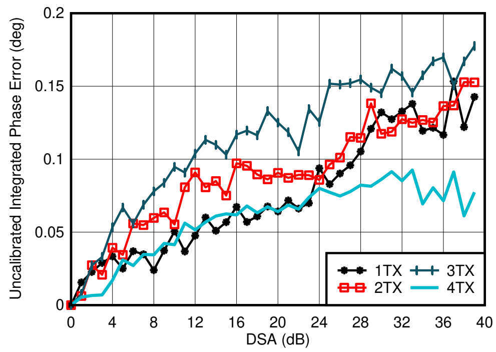


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

Figure 5-320. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz

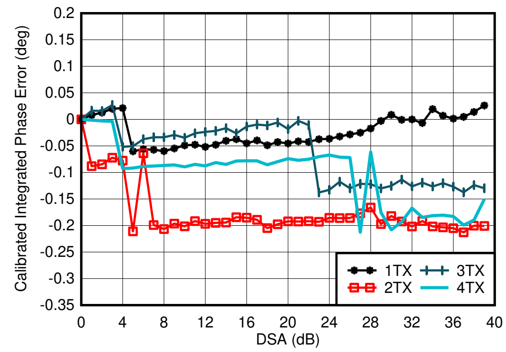
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



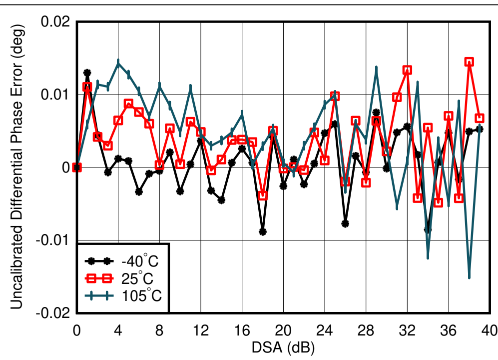
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 5-321. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz



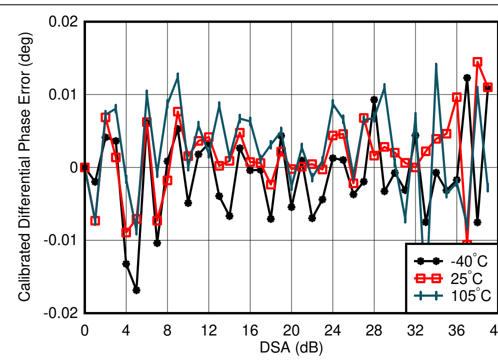
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 5-322. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

Figure 5-323. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz

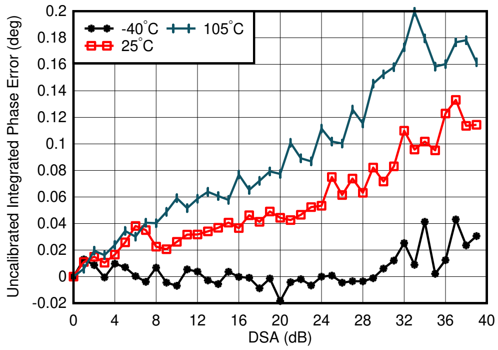


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

Figure 5-324. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz

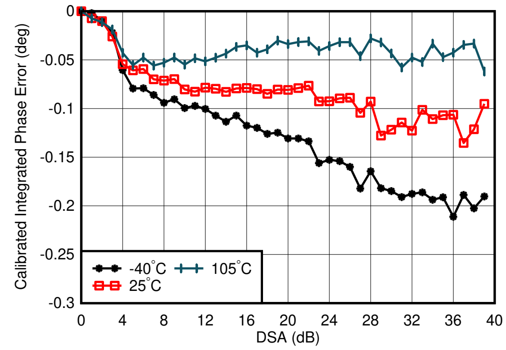
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



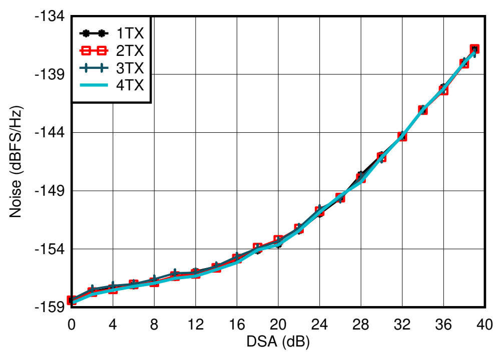
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 5-325. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



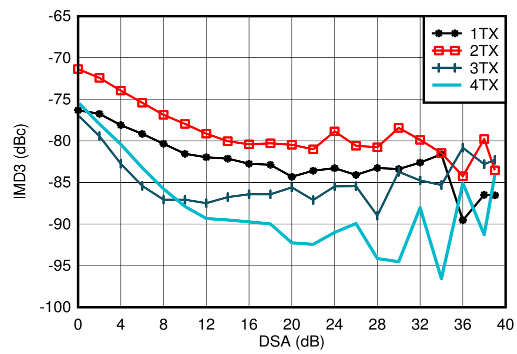
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 5-326. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



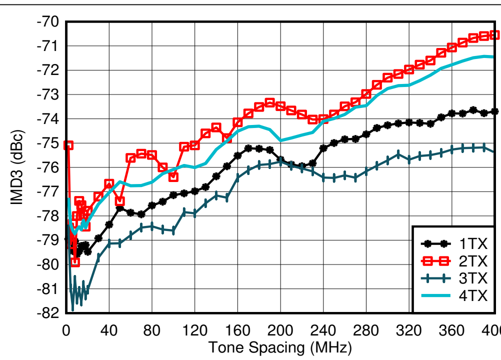
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz, P_{OUT} = –13 dBFS

Figure 5-327. TX Output Noise vs Channel and Attenuation at 0.85 GHz



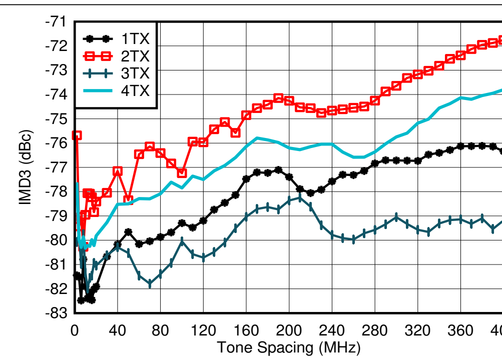
f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

Figure 5-328. TX IMD3 vs DSA Setting at 0.85 GHz



f_{DAC} = 5898.24 MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

Figure 5-329. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz

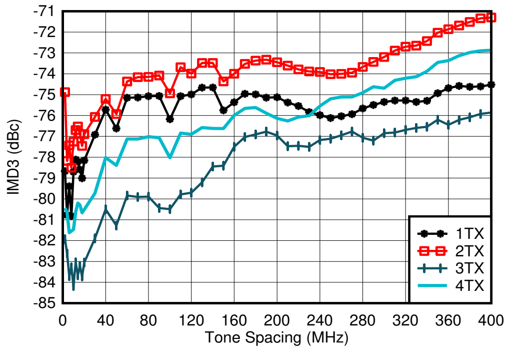


f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

Figure 5-330. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz

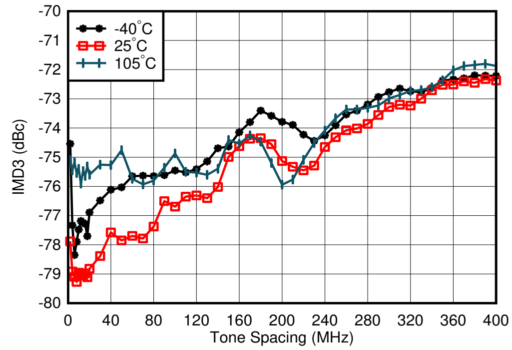
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



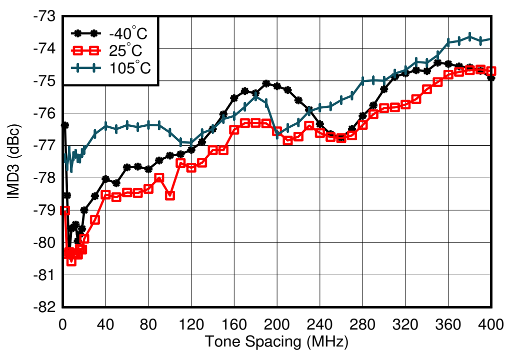
f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

Figure 5-331. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



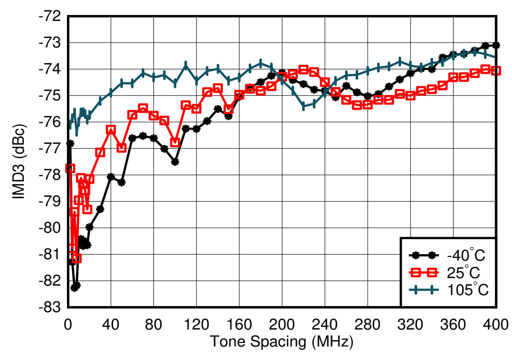
f_{DAC} = 5898.24 MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

Figure 5-332. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



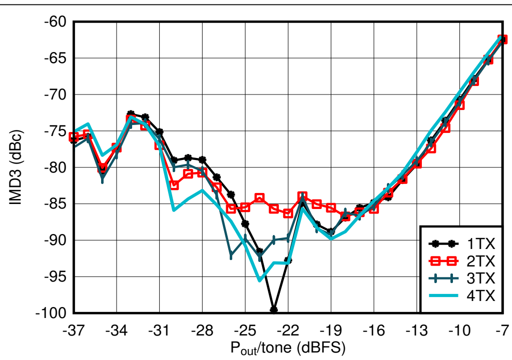
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

Figure 5-333. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



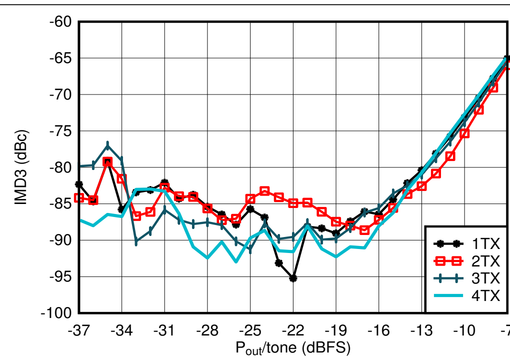
f_{DAC} = 11796.48 MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

Figure 5-334. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



f_{DAC} = 5898.24 MSPS, straight mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

Figure 5-335. TX IMD3 vs Digital Level at 0.85 GHz

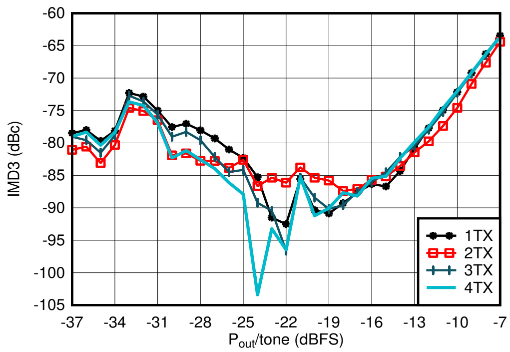


f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

Figure 5-336. TX IMD3 vs Digital Level at 0.85 GHz

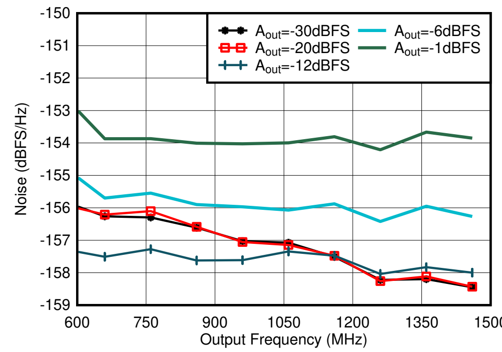
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



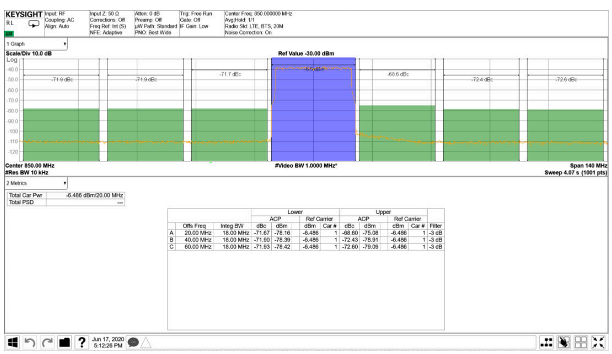
f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

Figure 5-337. TX IMD3 vs Digital Level at 0.85 GHz



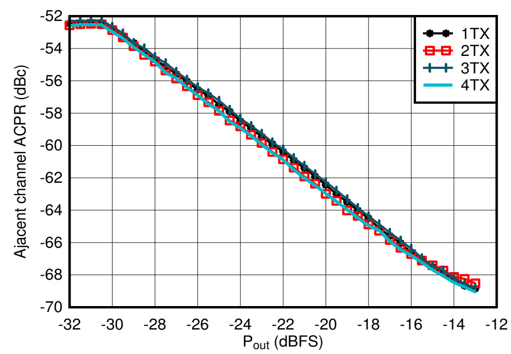
Matching at 0.8 GHz, Single tone, f_{DAC} = 11.79648 GSPS, interleave mode, 40-MHz offset, DSA = 0dB

Figure 5-338. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz



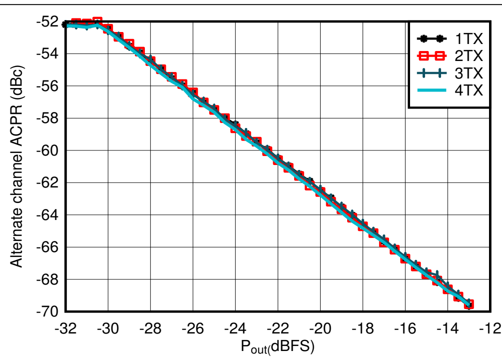
TM1.1, P_{OUT_RMS} = –13 dBFS

Figure 5-339. TX 20-MHz LTE Output Spectrum at 0.85 GHz



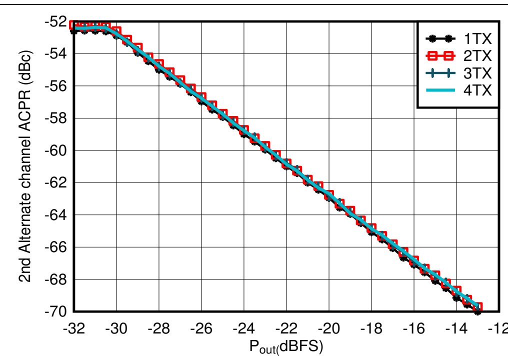
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-340. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz



Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-341. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz

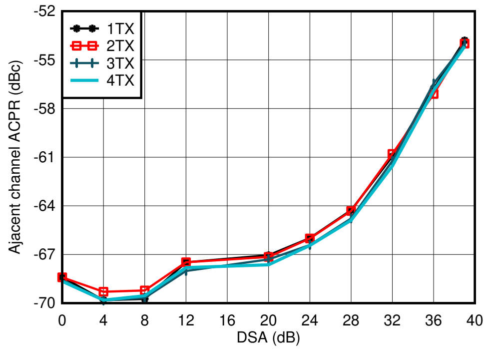


Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-342. TX 20-MHz LTE alt2-ACPR vs Digital Level at 0.85 GHz

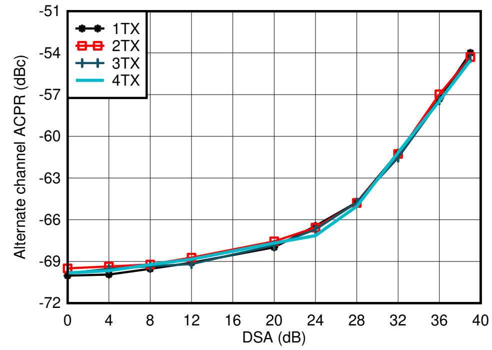
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



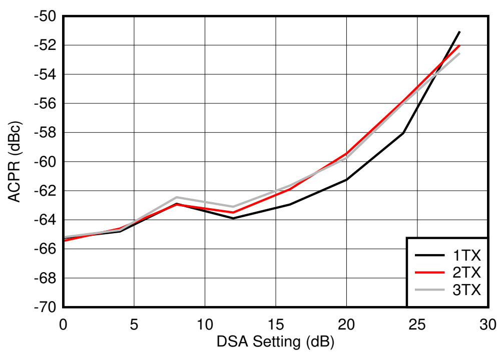
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-343. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz



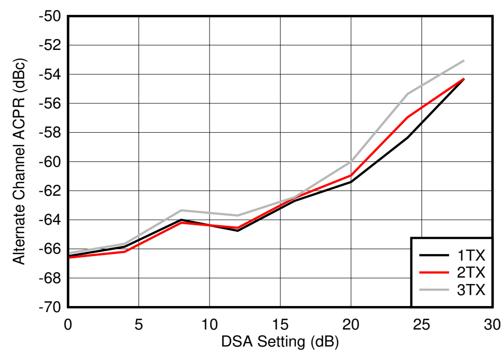
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-344. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz



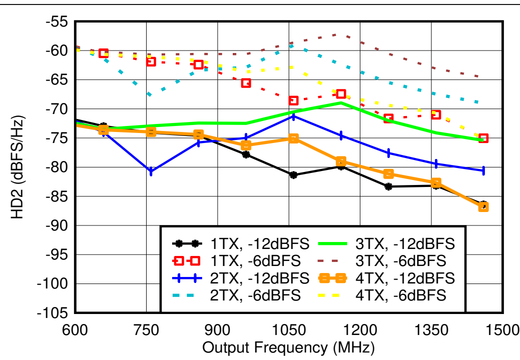
Matching at 0.8 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 5-345. TX 100-MHz NR ACPR vs DSA at 0.85 GHz



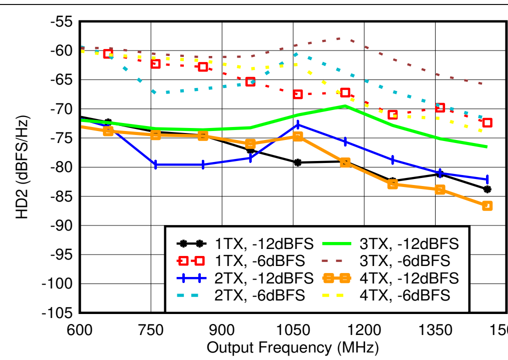
Matching at 0.8 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 5-346. TX 100-MHz NR alt-ACPR vs DSA at 0.85 GHz



Matching at 0.8 GHz, f_{DAC} = 5898.24GSPS, straight mode

Figure 5-347. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz

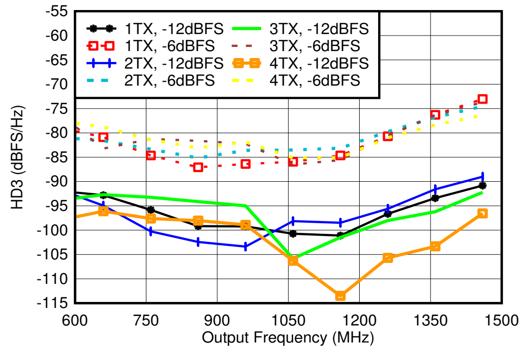


Matching at 0.8 GHz, f_{DAC} = 8847.36 GSPS, straight mode

Figure 5-348. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz

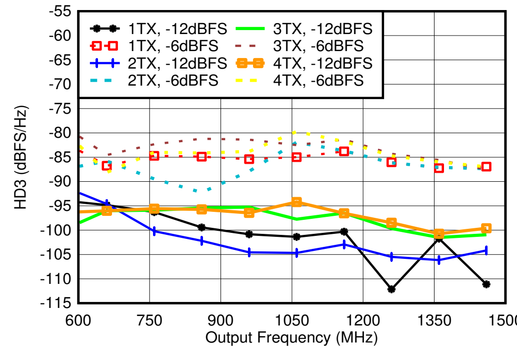
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



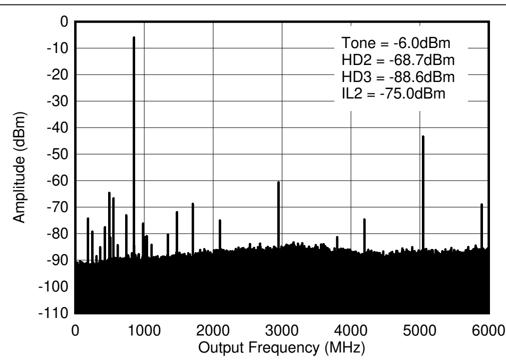
Matching at 0.8 GHz, f_{DAC} = 5898.24 MSPS, straight mode, normalized to output power at harmonic frequency

Figure 5-349. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



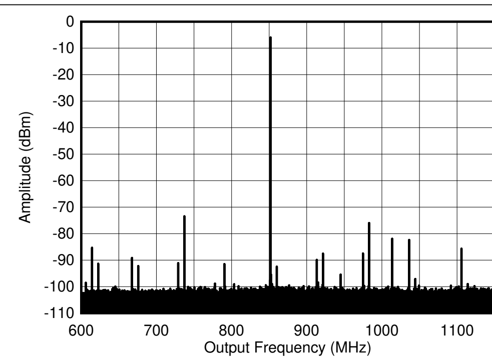
Matching at 0.8 GHz, f_{DAC} = 8847.36 MSPS, straight mode, normalized to output power at harmonic frequency

Figure 5-350. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



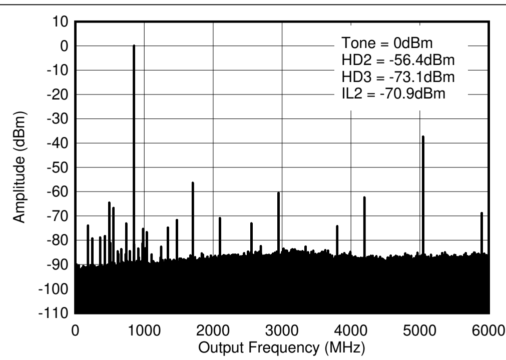
f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 5-351. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



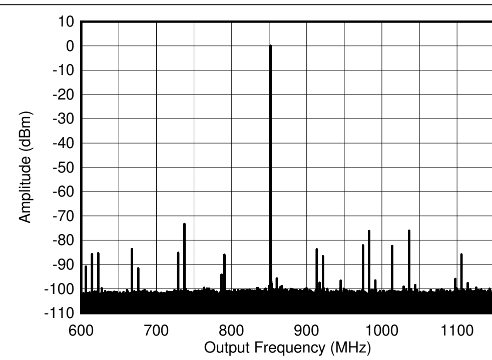
f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

Figure 5-352. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 5-353. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})

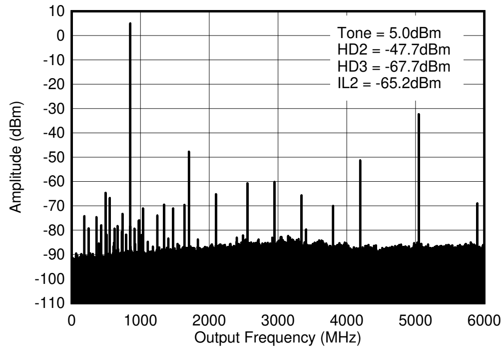


f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

Figure 5-354. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

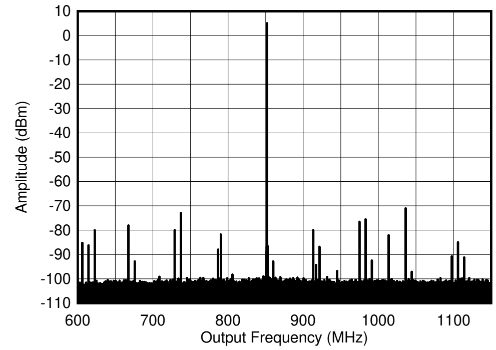
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



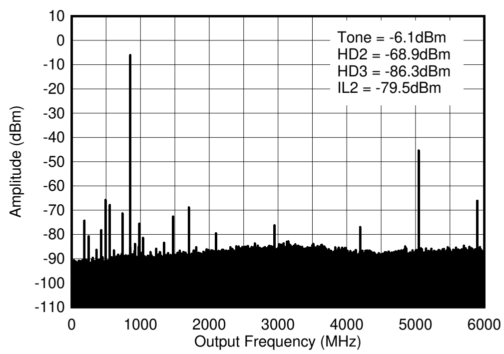
f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 5-355. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



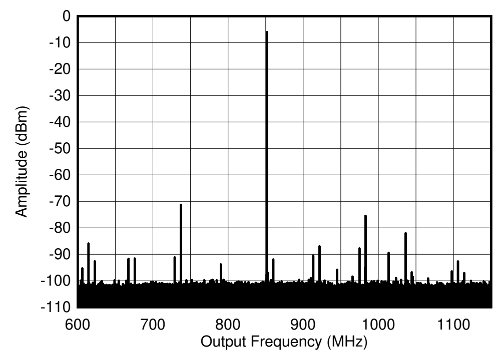
f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

Figure 5-356. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



f_{DAC} = 5898.24 MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 5-357. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})

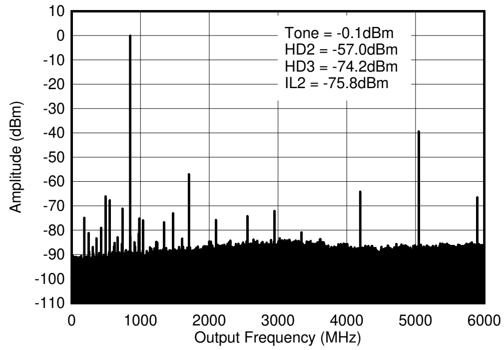


f_{DAC} = 5898.24 MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

Figure 5-358. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

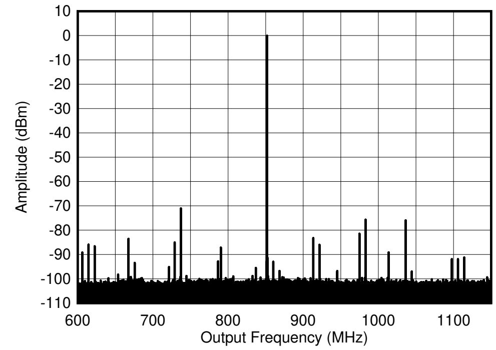
5.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



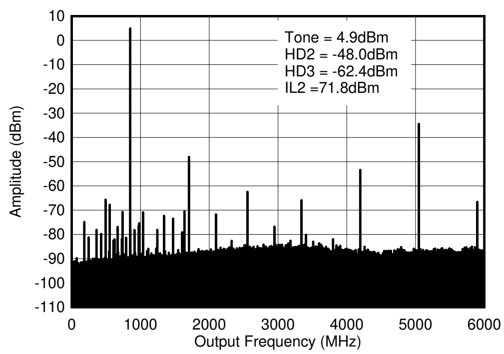
f_{DAC} = 5898.24 MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 5-359. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



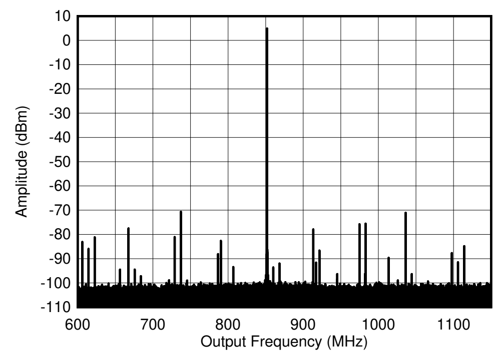
f_{DAC} = 5898.24 MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

Figure 5-360. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



f_{DAC} = 5898.24 MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 5-361. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})

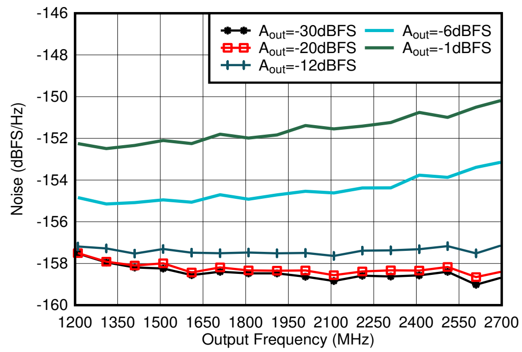


f_{DAC} = 5898.24 MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

Figure 5-362. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

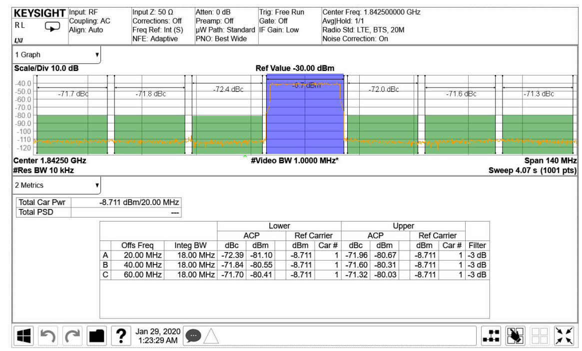
5.12.10 TX Typical Characteristics at 1.8 GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



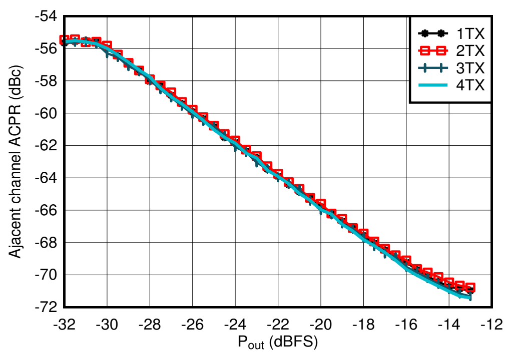
Matching at 1.8 GHz, Single tone, f_{DAC} = 11.79648 GSPS, interleave mode, 40-MHz offset

Figure 5-363. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz



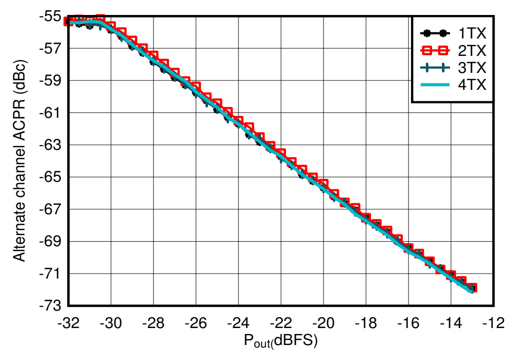
TM1.1, P_{OUT_RMS} = –13 dBFS

Figure 5-364. TX 20-MHz LTE Output Spectrum at 1.8425 GHz



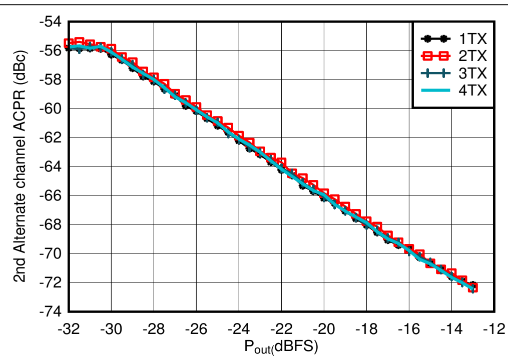
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-365. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz



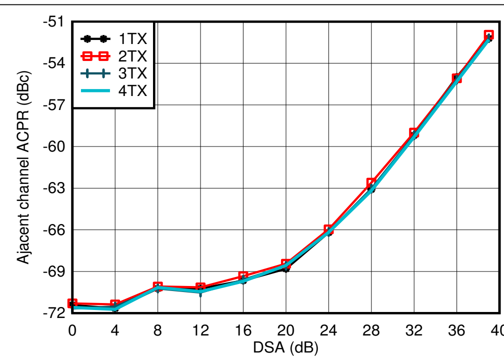
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-366. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-367. TX 20-MHz LTE alt2-ACPR vs Digital Level at 1.8425 GHz

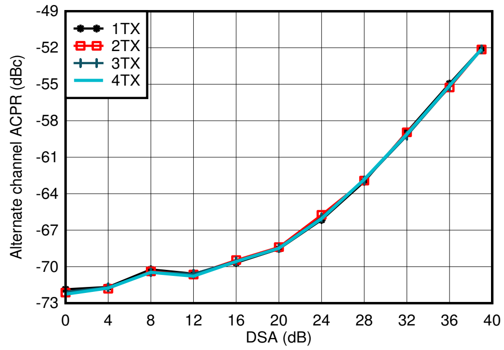


Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-368. TX 20-MHz LTE ACPR vs DSA at 1.8 GHz

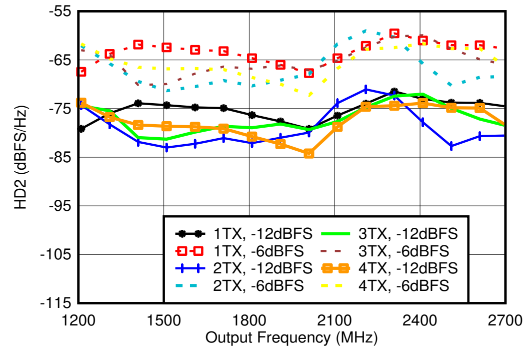
5.12.10 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



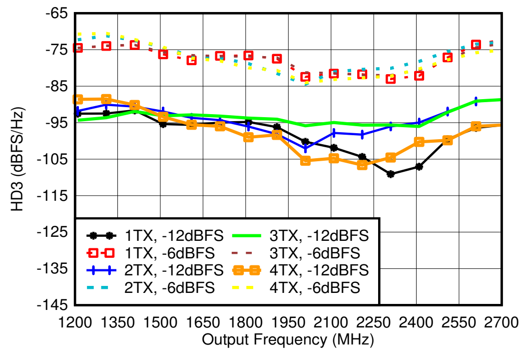
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-369. TX 20-MHz LTE alt-ACPR vs DSA at 1.8 GHz



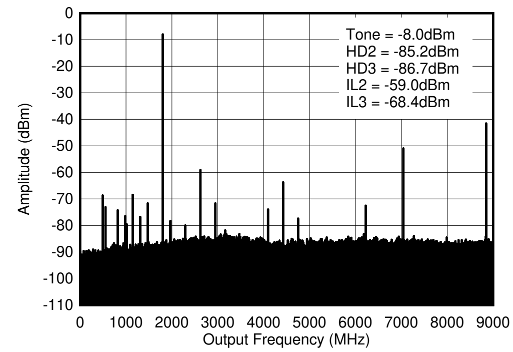
Matching at 1.8 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 5-370. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz



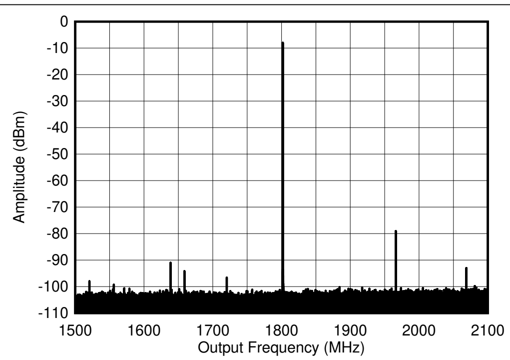
Matching at 1.8 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 5-371. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz



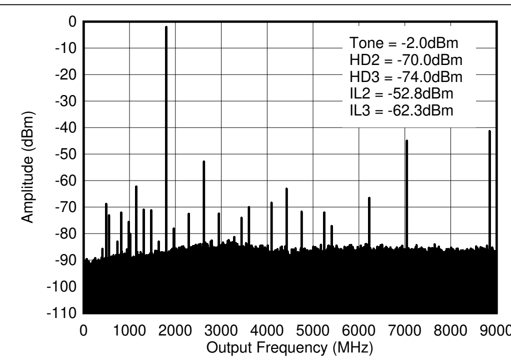
f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 5-372. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

Figure 5-373. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)

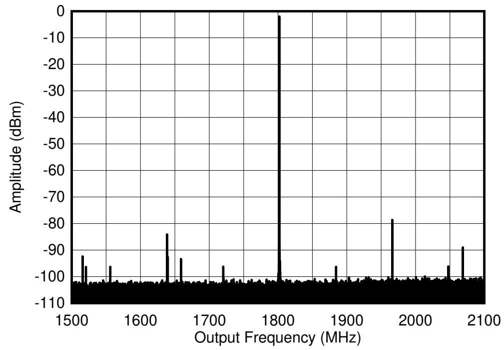


f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 5-374. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

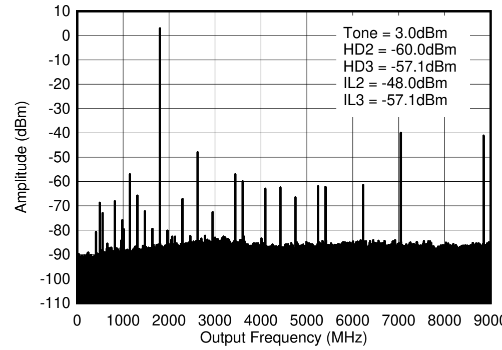
5.12.10 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



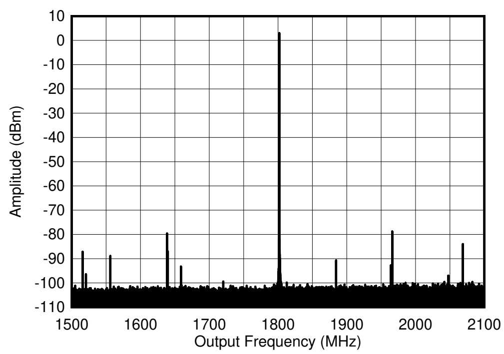
f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

Figure 5-375. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



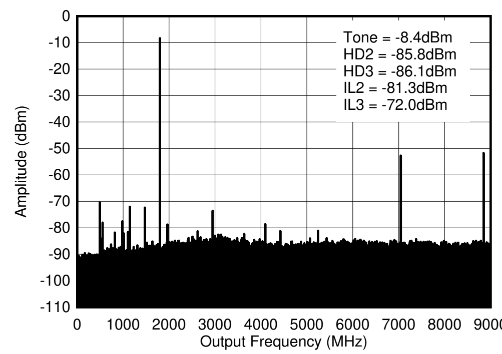
f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 5-376. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

Figure 5-377. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)

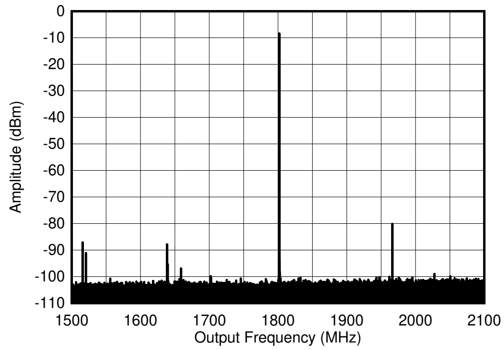


f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 5-378. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

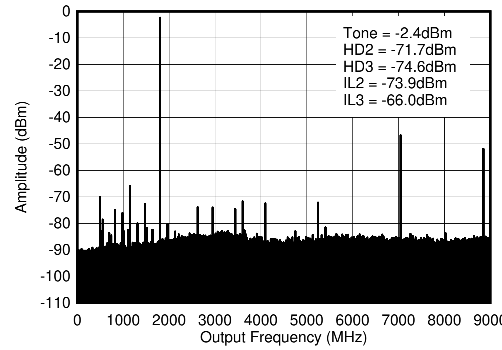
5.12.10 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



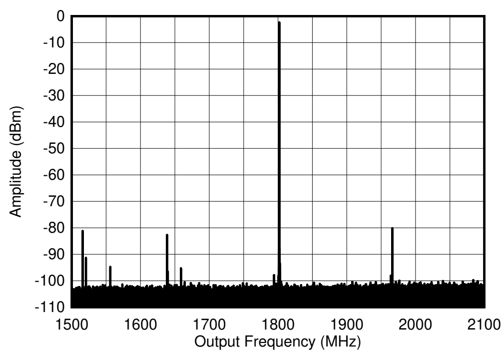
f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

Figure 5-379. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



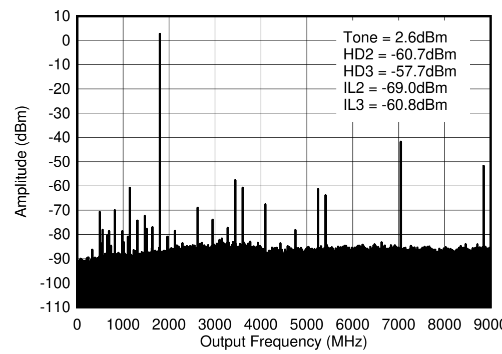
f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 5-380. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



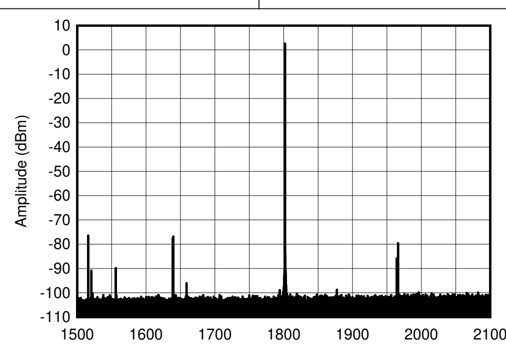
f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

Figure 5-381. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 5-382. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

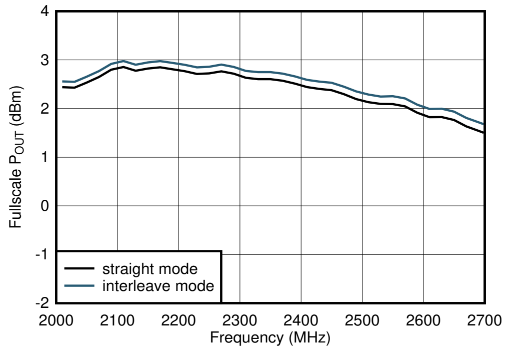


f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

Figure 5-383. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)

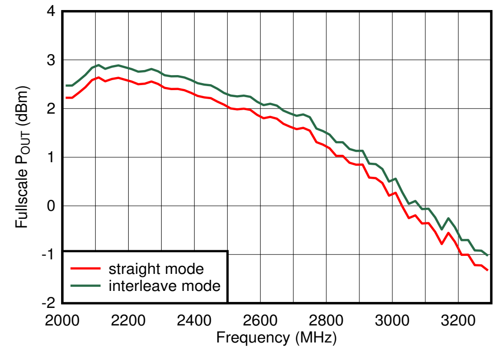
5.12.11 TX Typical Characteristics at 2.6 GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



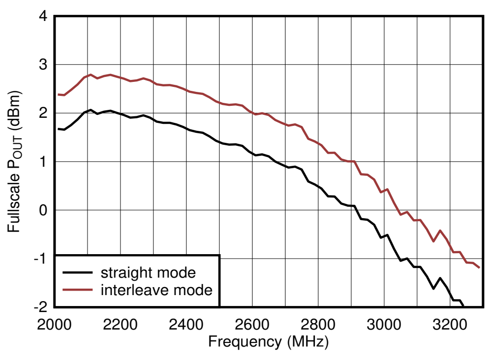
Including PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 2.6 GHz matching

Figure 5-384. TX Full Scale vs RF Frequency at 5898.24 MSPS



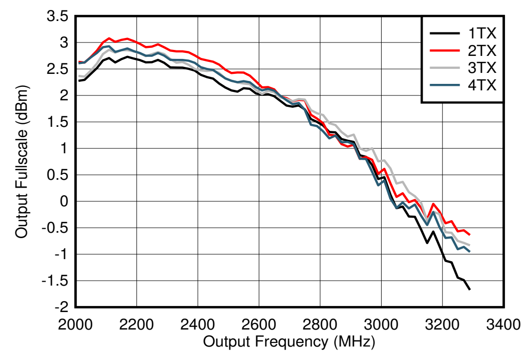
Including PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 2.6 GHz matching

Figure 5-385. TX Full Scale vs RF Frequency at 8847.36 MSPS



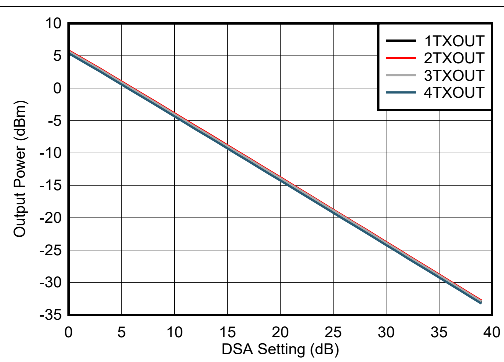
Including PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 2.6 GHz matching

Figure 5-386. TX Full Scale vs RF Frequency at 11796.48 MSPS



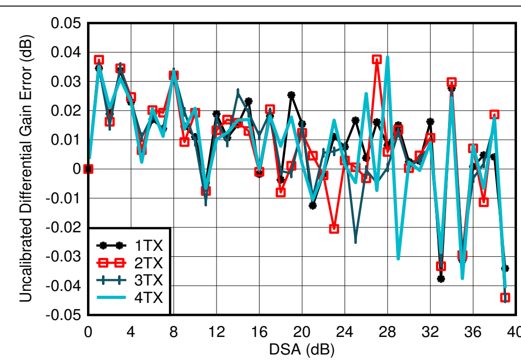
f_{DAC} = 8847.36 MSPS, interleave mode, including PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 2.6 GHz matching

Figure 5-387. TX Output Fullscale vs Output Frequency and Channel



f_{DAC} = 8847.36 MSPS, A_{out} = -0.5 dBFS, matching 2.6 GHz

Figure 5-388. TX Output Power vs DSA Setting and Channel at 2.6 GHz

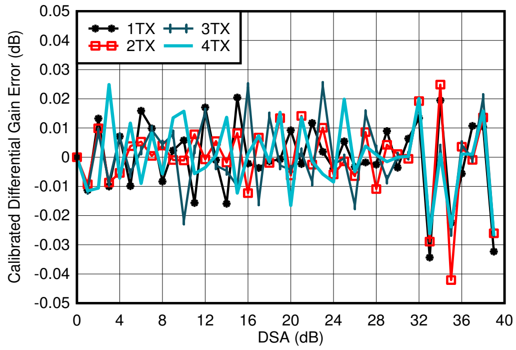


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-389. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz

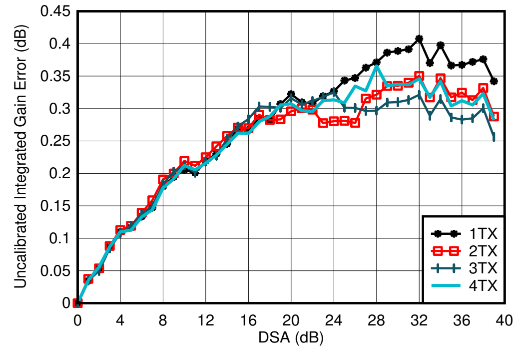
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



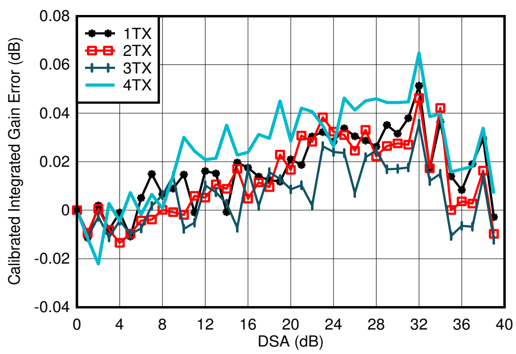
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-390. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



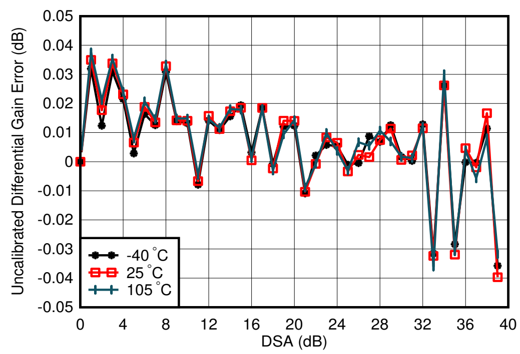
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 5-391. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 5-392. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz

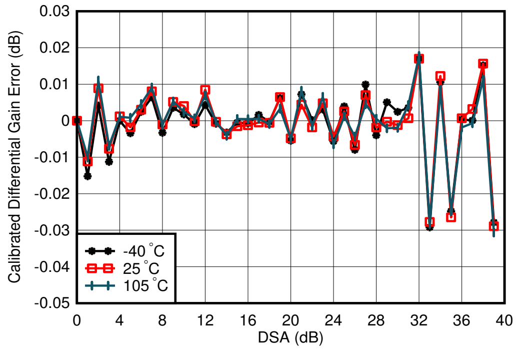


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-393. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz

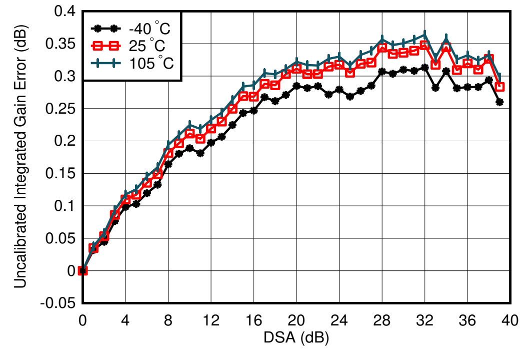
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



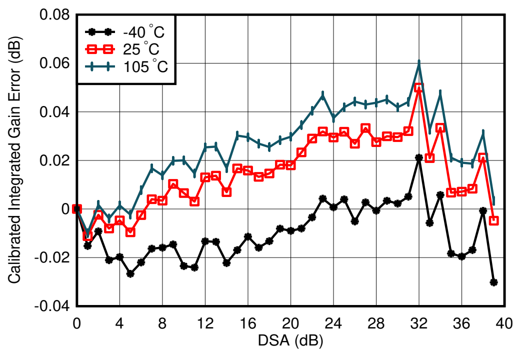
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-394. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



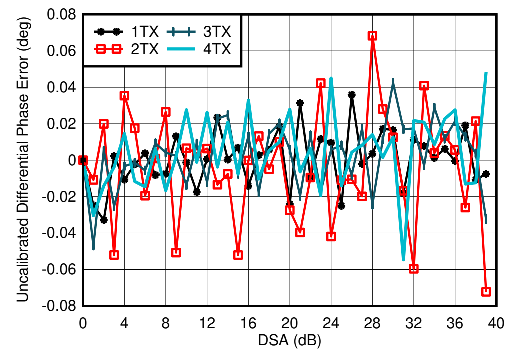
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 5-395. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 5-396. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

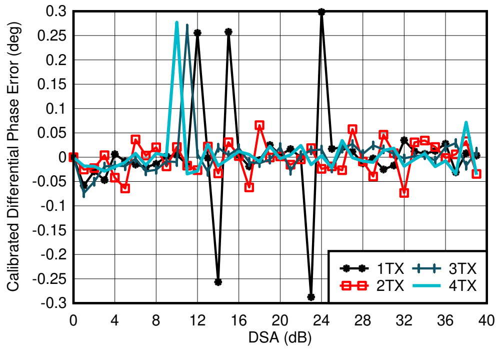


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-397. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz

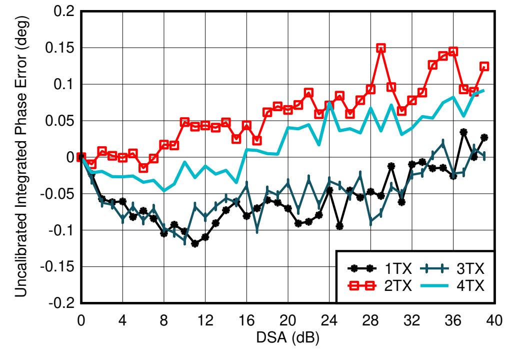
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



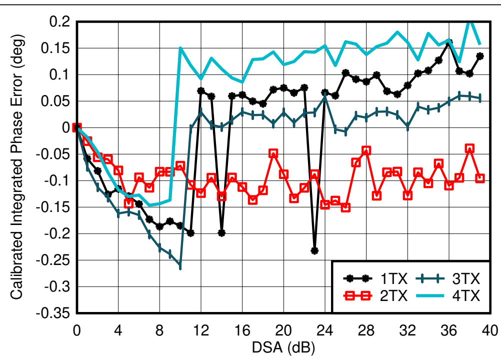
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

Figure 5-398. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



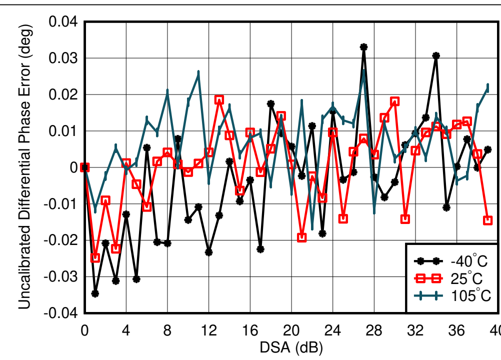
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-399. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-400. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

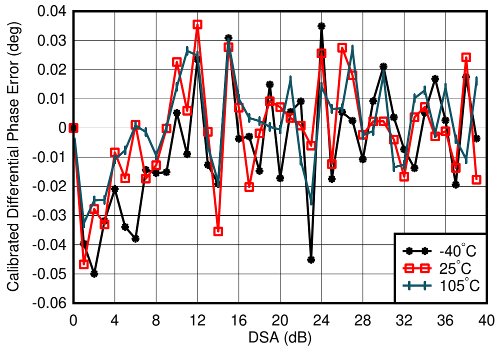


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-401. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz

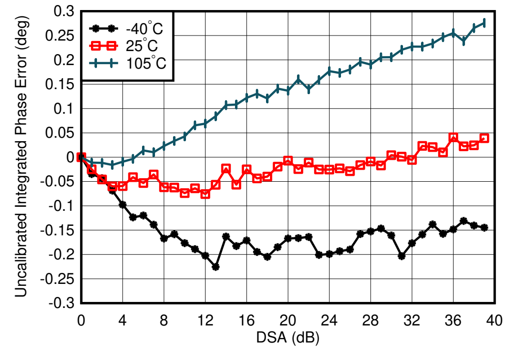
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1^{st} Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



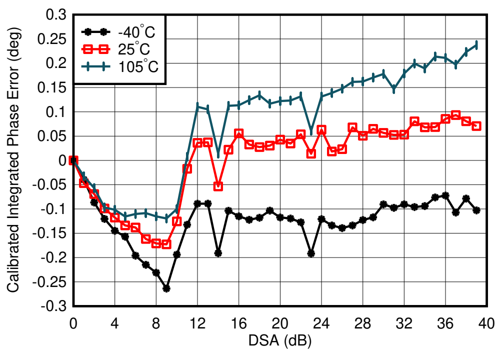
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-402. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



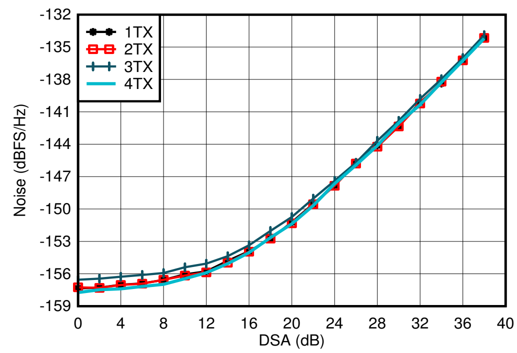
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the medium variation over DSA setting at 25°C Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-403. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-404. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz

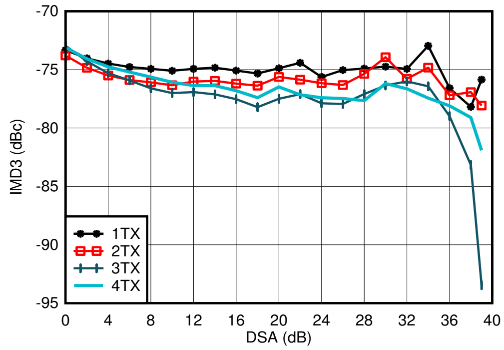


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, P_{OUT} = –13 dBFS

Figure 5-405. TX Output Noise vs Channel and Attenuation at 2.6 GHz

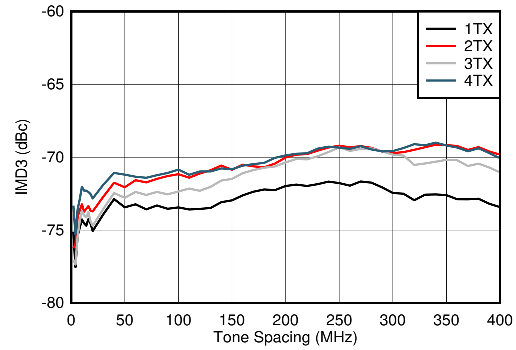
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



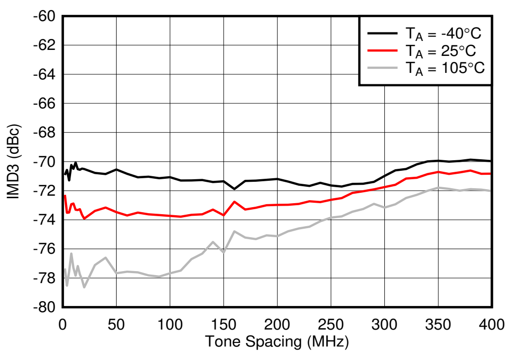
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

Figure 5-406. TX IMD3 vs DSA Setting at 2.6 GHz



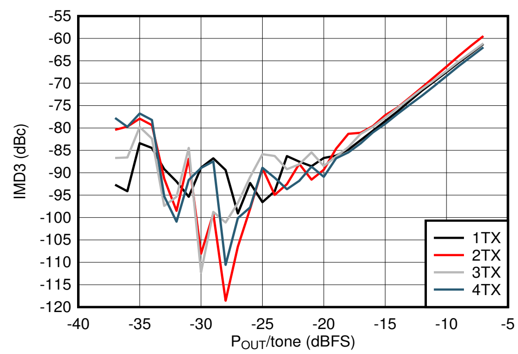
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

Figure 5-407. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz



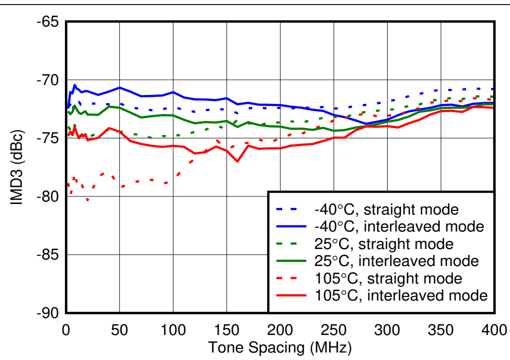
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone, worst channel.

Figure 5-408. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz



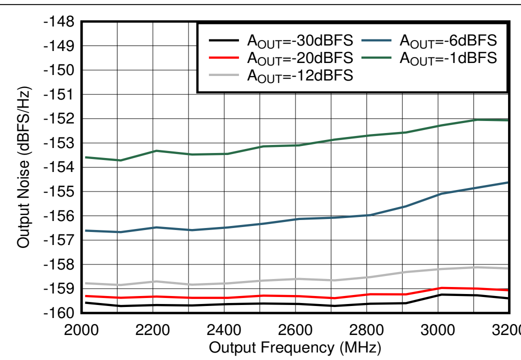
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, $f_{SPACING}$ = 20 MHz, matching at 2.6 GHz

Figure 5-409. TX IMD3 vs Digital Level at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

Figure 5-410. TX IMD3 vs Tone Spacing and Temperature

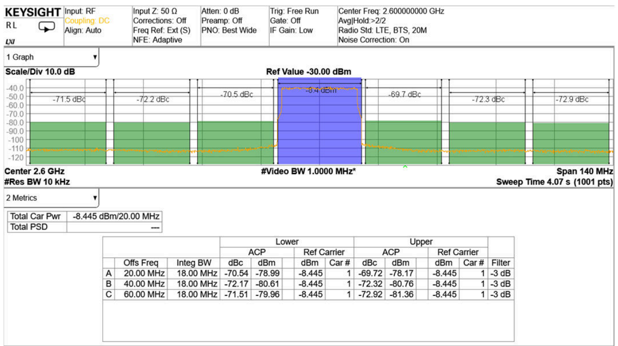


Matching at 2.6 GHz, Single tone, f_{DAC} = 11.79648 GSPS, interleave mode, 40-MHz offset

Figure 5-411. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz

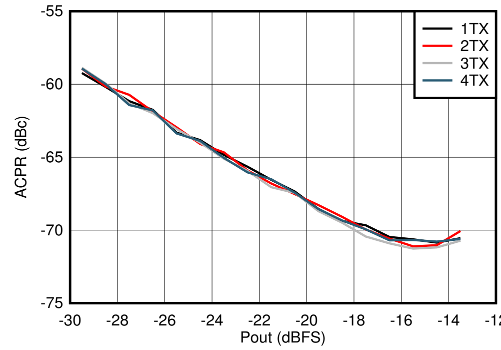
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



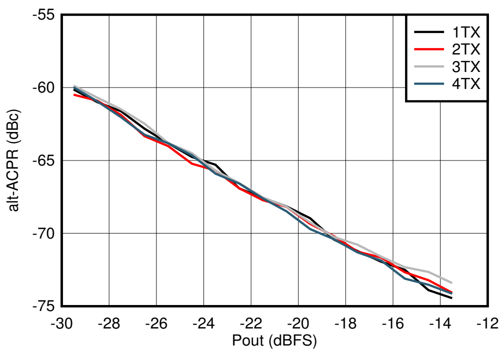
TM1.1, P_{OUT_RMS} = –13 dBFS

Figure 5-412. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)



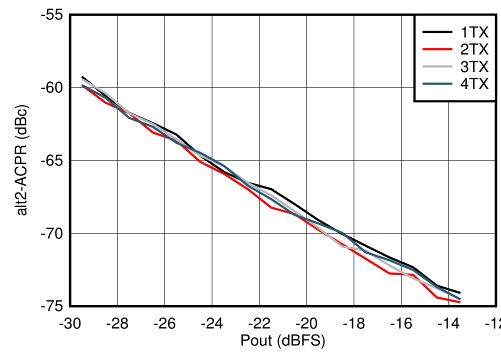
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-413. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz



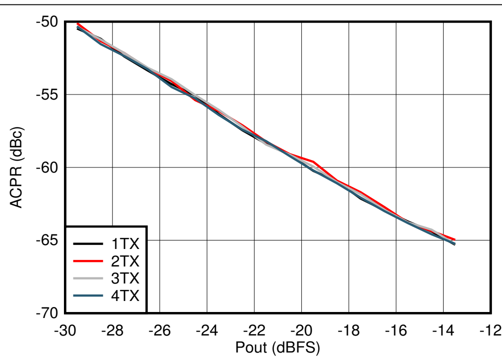
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-414. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz



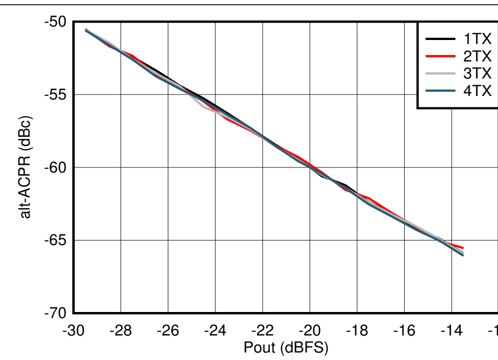
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-415. TX 20-MHz LTE alt2-ACPR vs Digital Level at 2.6 GHz



Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 5-416. TX 100-MHz NR ACPR vs Digital Level at 2.6 GHz

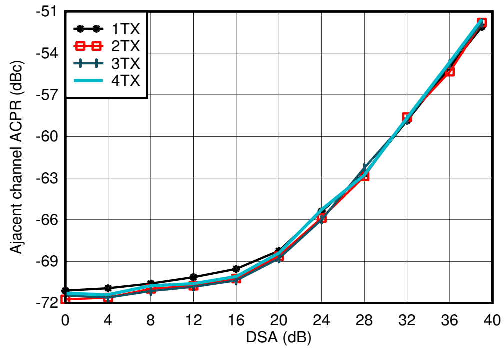


Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 5-417. TX 100-MHz NR alt-ACPR vs Digital Level at 2.6 GHz

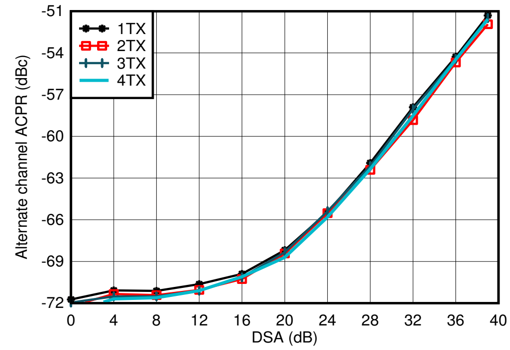
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



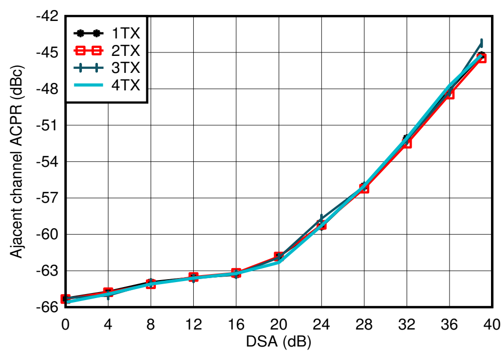
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-418. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz



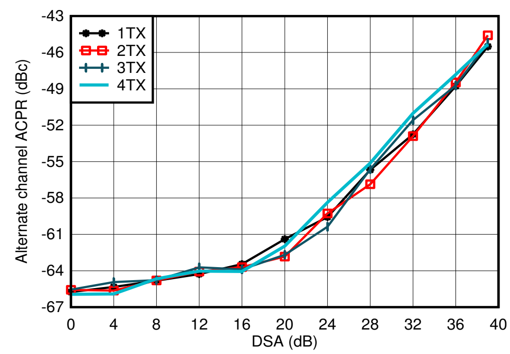
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-419. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz



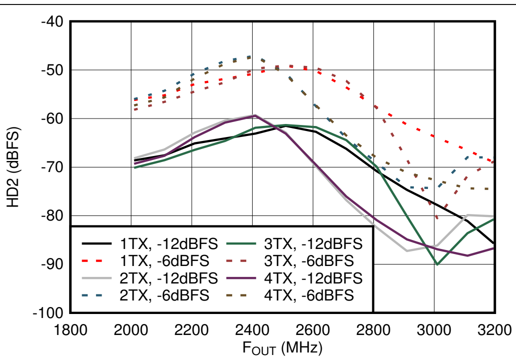
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 5-420. TX 100-MHz NR ACPR vs DSA at 2.6 GHz



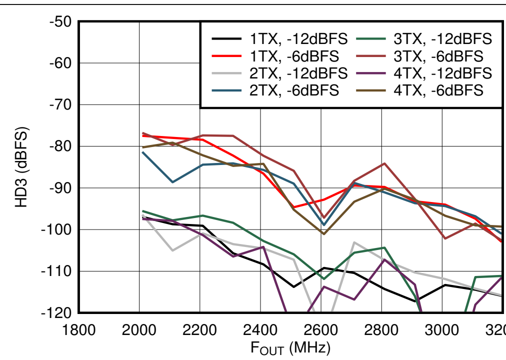
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 5-421. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz



Matching at 2.6 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 5-422. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz

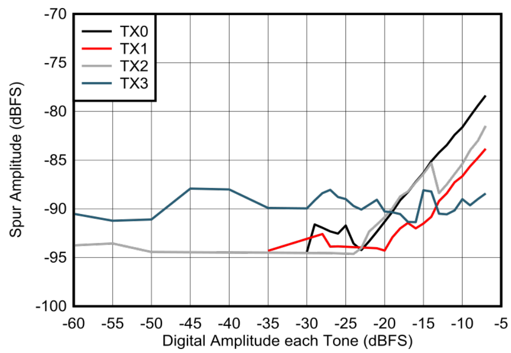


Matching at 2.6 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 5-423. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz

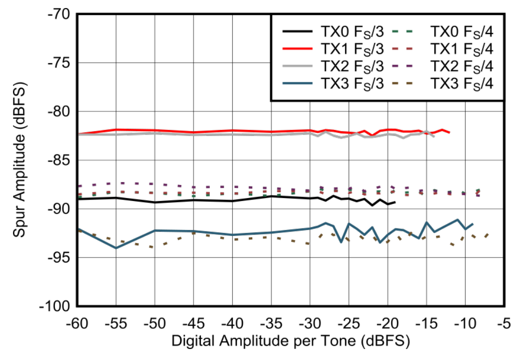
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



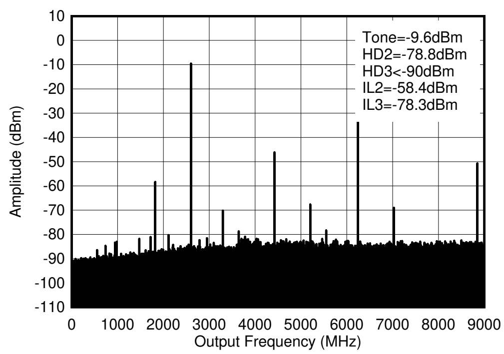
Inband = 2600 MHz ± 600 MHz, f_{DAC} = 12 GSPS, not including F_S/3 and F_S/4, external clock mode, non-interleave mode

Figure 5-424. Two Tone Inband SFDR vs Digital Amplitude at 2.6 GHz



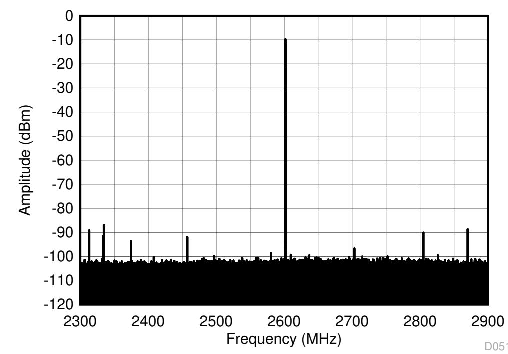
Inband = 2600 MHz ± 600 MHz, f_{DAC} = 12 GSPS, external clock mode, non-interleave mode

Figure 5-425. Two Tone Inband Fixed Spurs vs Digital Amplitude at 2.6 GHz



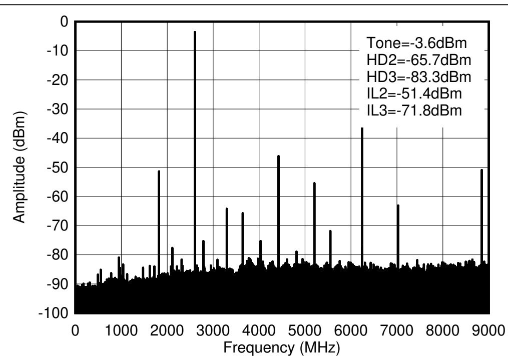
f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 5-426. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



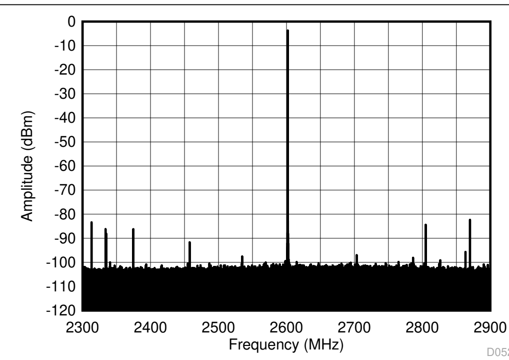
f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

Figure 5-427. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 5-428. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})

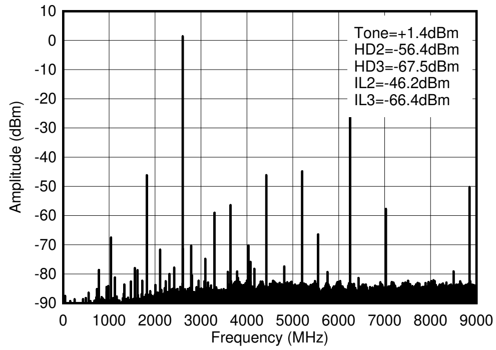


f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

Figure 5-429. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)

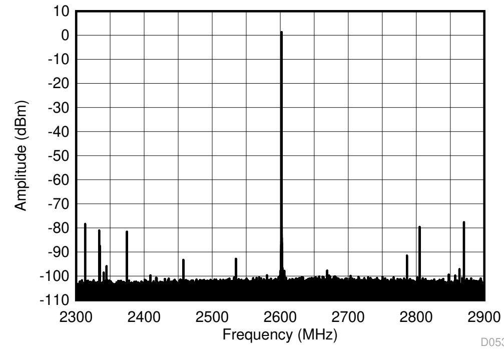
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



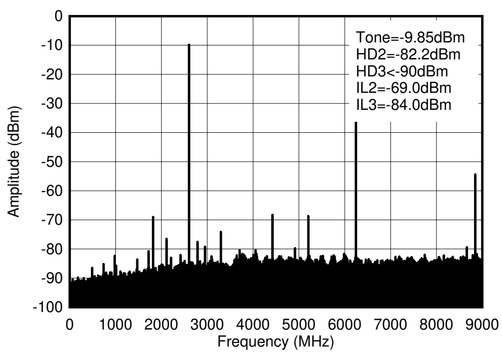
f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 5-430. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



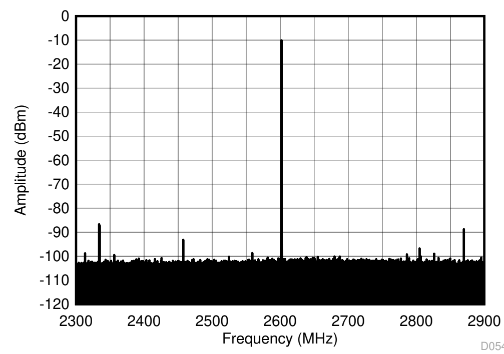
f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

Figure 5-431. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

Figure 5-432. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})

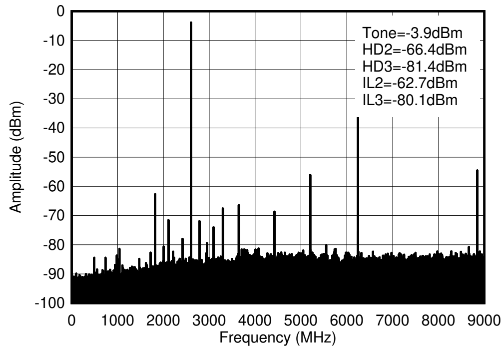


f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

Figure 5-433. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)

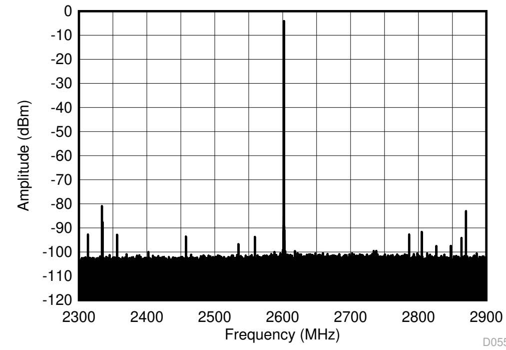
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



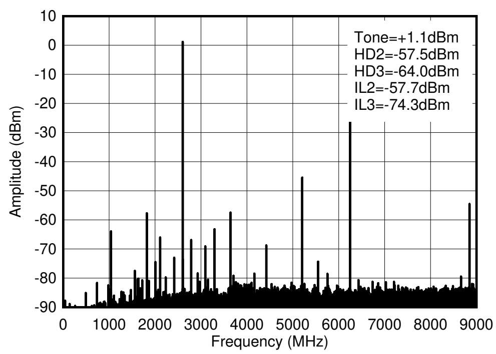
f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 5-434. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



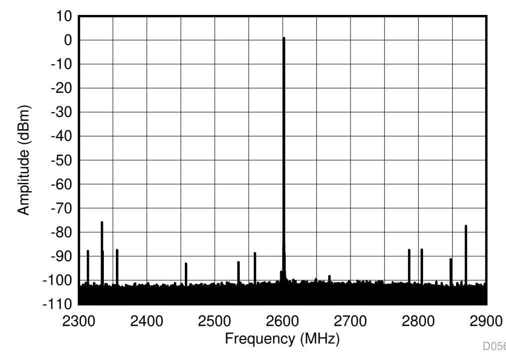
f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

Figure 5-435. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



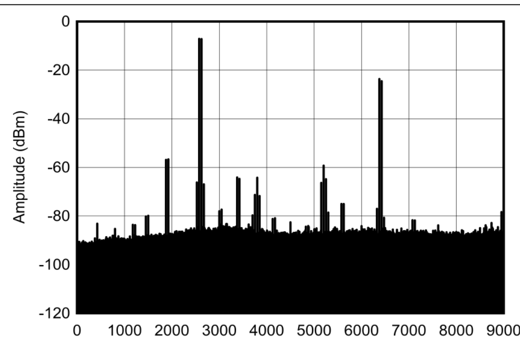
f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 5-436. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



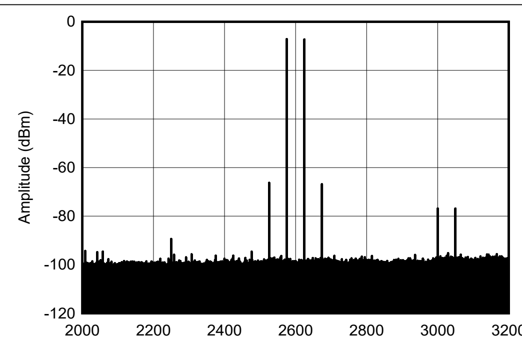
f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

Figure 5-437. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

Figure 5-438. TX Dual Tone Output Spectrum at 2.6 GHz, -7 dBFS each (0 - $_{DAC}$)

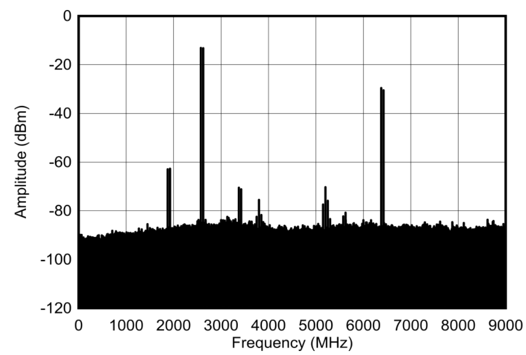


f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

Figure 5-439. TX Dual Tone Output Spectrum at 2.6 GHz, -7 dBFS each (±600 MHz)

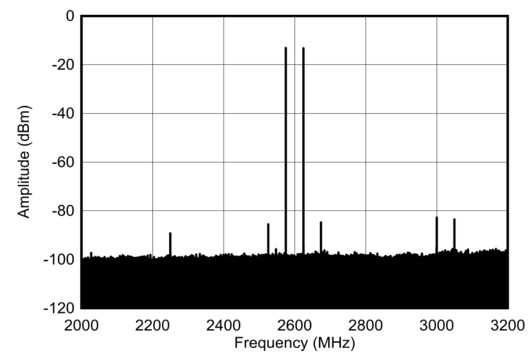
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



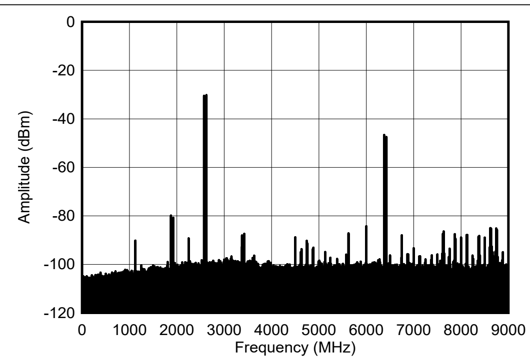
f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

Figure 5-440. TX Dual Tone Output Spectrum at 2.6 GHz, -13 dBFS each (0 - $_{DAC}$)



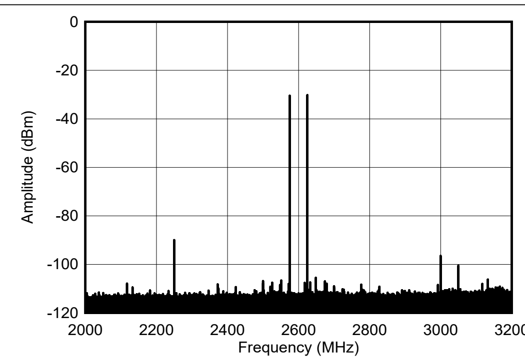
f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

Figure 5-441. TX Dual Tone Output Spectrum at 2.6 GHz, -13dBFS each (±600 MHz)



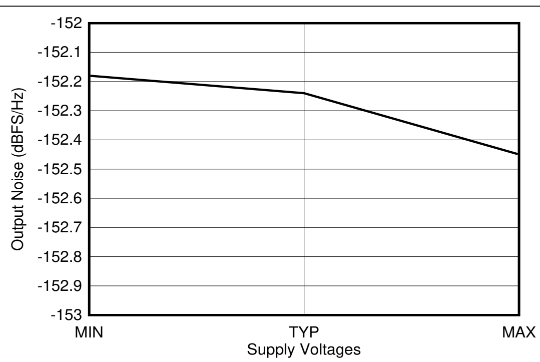
f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

Figure 5-442. TX Dual Tone Output Spectrum at 2.6 GHz, -30 dBFS each (0 - $_{DAC}$)



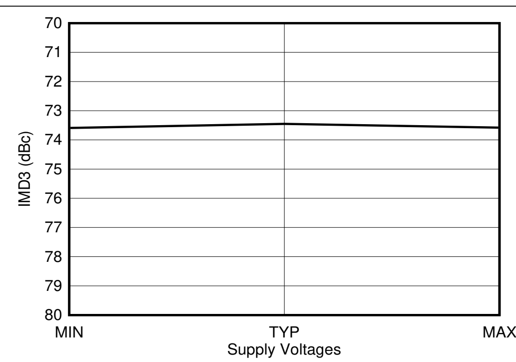
f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

Figure 5-443. TX Dual Tone Output Spectrum at 2.6 GHz, -30 dBFS each (±600 MHz)



f_{DAC} = 11796.48 MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = –1 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

Figure 5-444. TX Output Noise vs Supply Voltage at 2.6 GHz

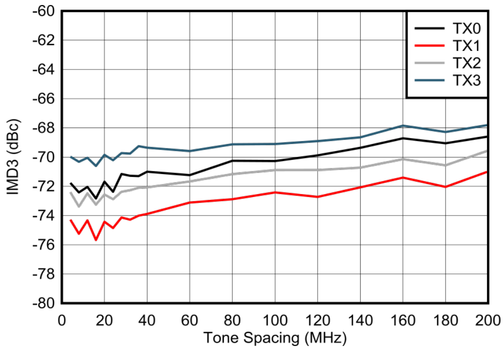


f_{DAC} = 11796.48 MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = –13 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

Figure 5-445. TX IMD3 vs Supply Voltage at 2.6 GHz

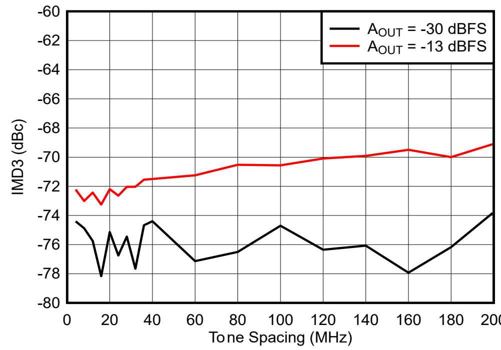
5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



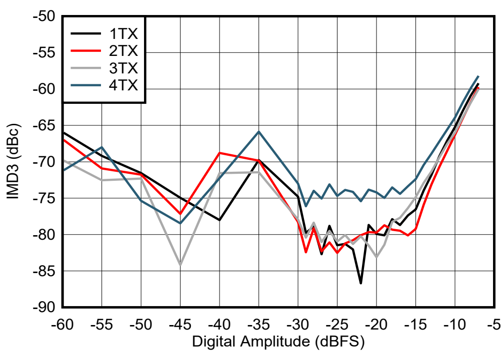
f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode

Figure 5-446. IMD3 vs Tone Spacing and Channel at 2.6 GHz



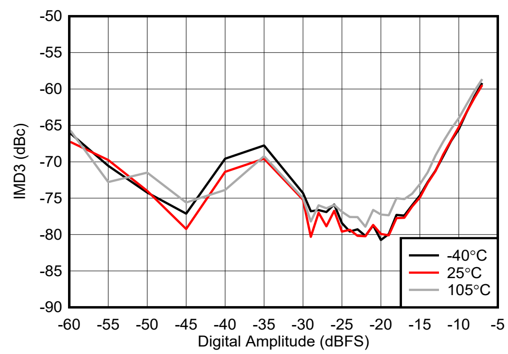
f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode

Figure 5-447. IMD3 vs Tone Spacing and Amplitude at 2.6 GHz



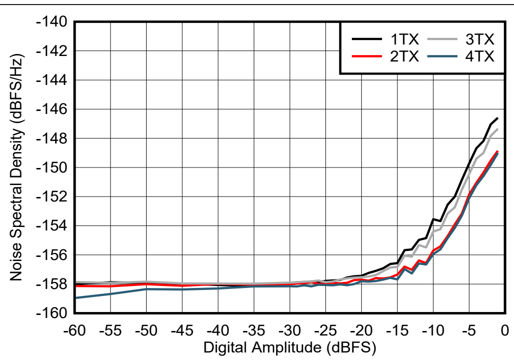
f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode

Figure 5-448. IMD3 vs Digital Amplitude and Channel at 2.6 GHz



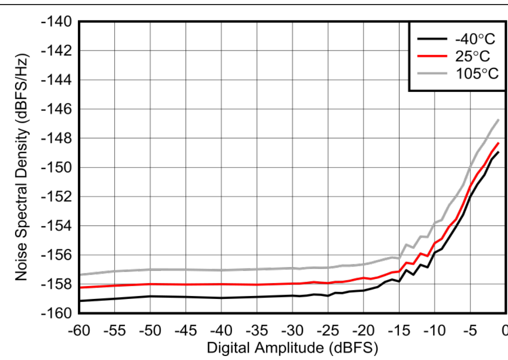
f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode

Figure 5-449. IMD3 vs Digital Amplitude and Temperature at 2.6 GHz



f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode, 50MHz offset

Figure 5-450. NSD vs Digital Amplitude and Channel at 2.6 GHz

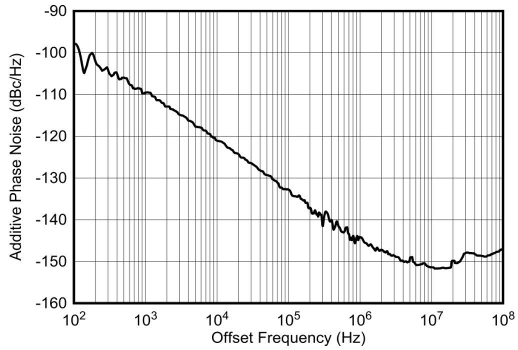


f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode, 50MHz offset

Figure 5-451. NSD vs Digital Amplitude and Temperature at 2.6 GHz

5.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

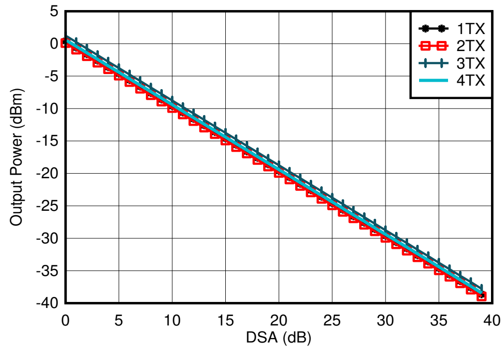


f_{DAC} = f_{CLK} = 9000 MSPS, non-interleave mode

Figure 5-452. External Clock Additive Phase Noise at 2.6 GHz

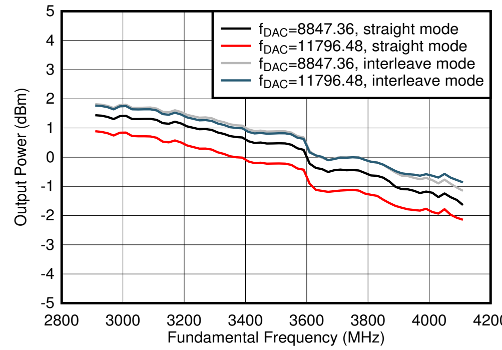
5.12.12 TX Typical Characteristics at 3.5 GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



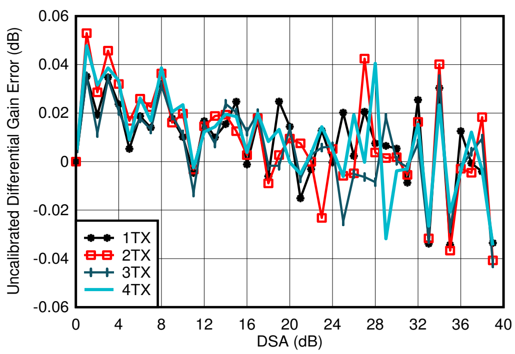
A_{out} = -0.5 dFBS, 3.5 GHz Matching, included PCB and cable losses

Figure 5-453. TX Output Power vs DSA Setting at 3.5 GHz



A_{out} = -0.5 dFBS, 3.5 GHz Matching, included PCB and cable losses

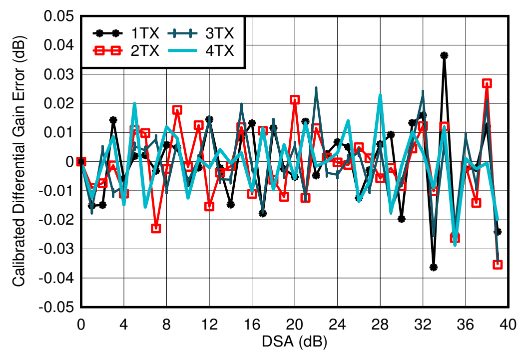
Figure 5-454. TX Output Power vs Frequency



3.5 GHz Matching, included PCB and cable losses

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

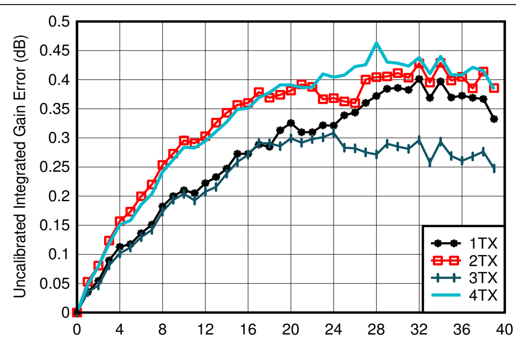
Figure 5-455. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

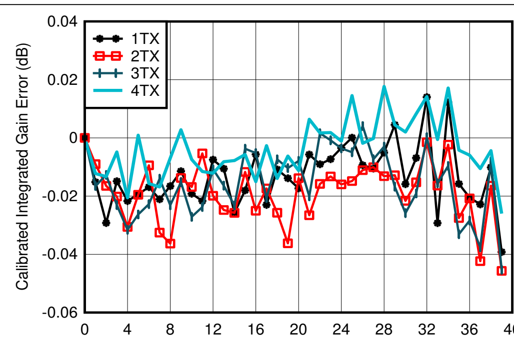
Figure 5-456. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 5-457. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz



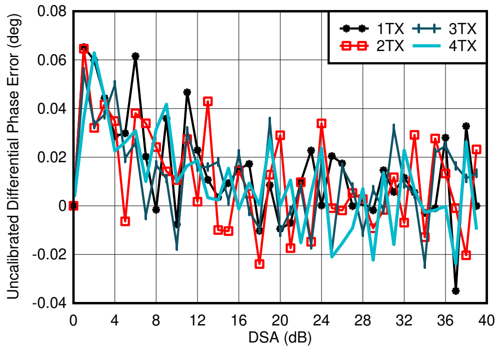
3.5 GHz Matching, included PCB and cable losses

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 5-458. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

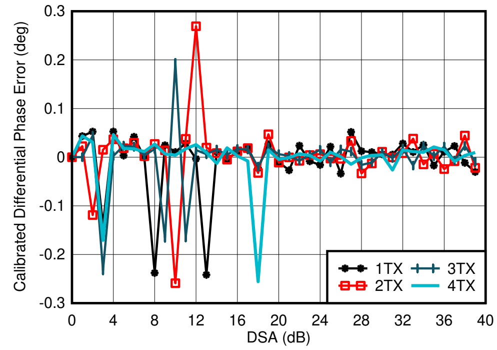
5.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



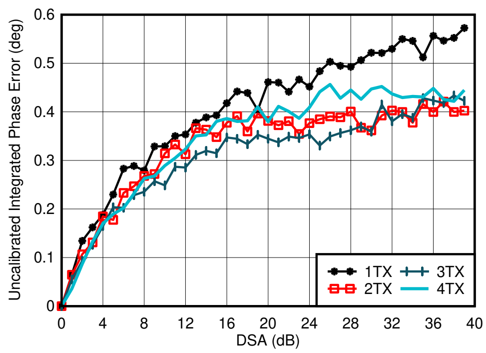
3.5 GHz Matching, included PCB and cable losses
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-459. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



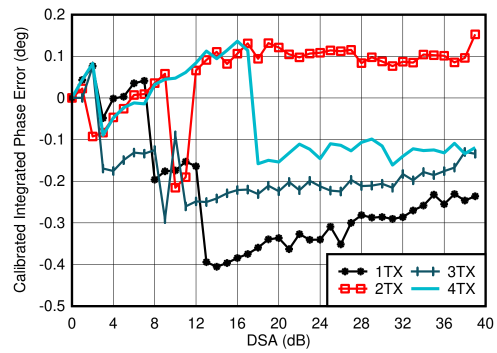
3.5 GHz Matching, included PCB and cable losses
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting). Phase DNL spike may occur at any DSA setting.

Figure 5-460. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-461. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz

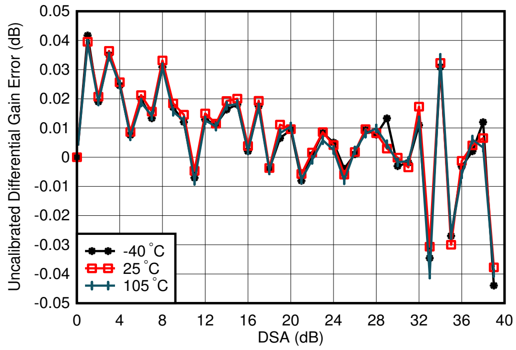


3.5 GHz Matching, included PCB and cable losses
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-462. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz

5.12.12 TX Typical Characteristics at 3.5 GHz (continued)

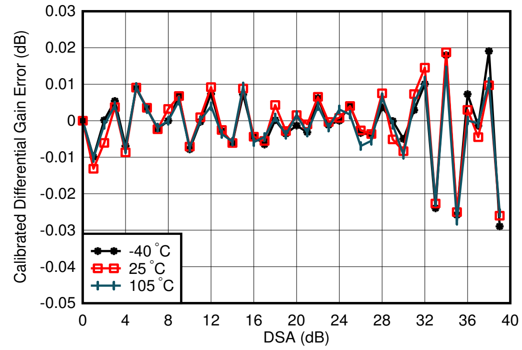
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



3.5 GHz Matching, 1TX

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

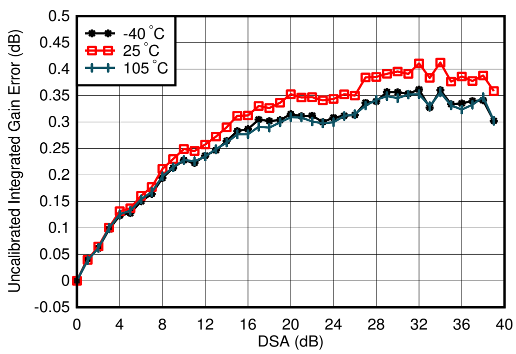
Figure 5-463. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

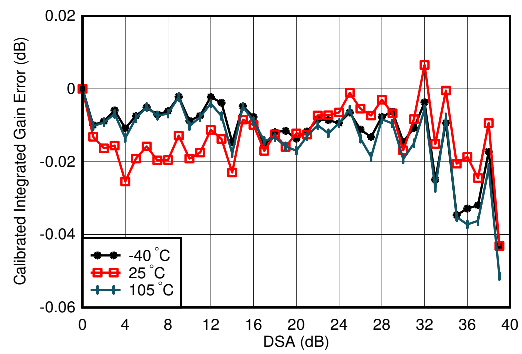
Figure 5-464. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-465. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



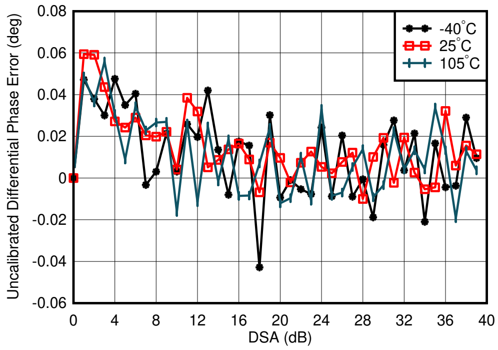
3.5 GHz Matching, 1TX, Calibrated at 25°C

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-466. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz

5.12.12 TX Typical Characteristics at 3.5 GHz (continued)

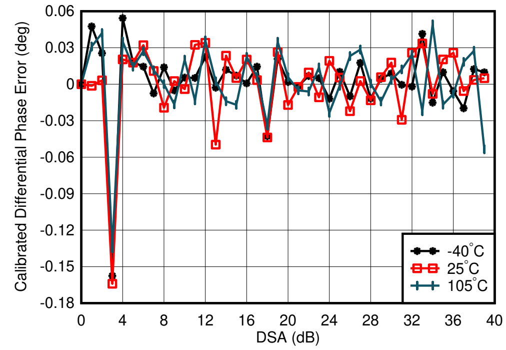
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



3.5 GHz Matching, 1TX

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

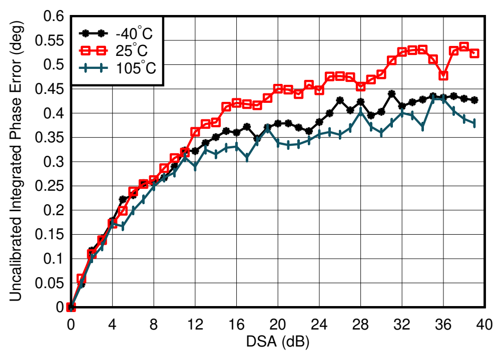
Figure 5-467. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

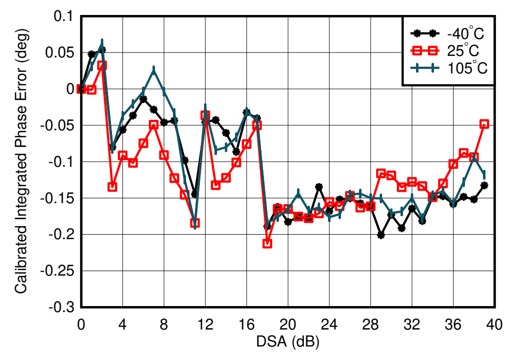
Figure 5-468. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting=0)

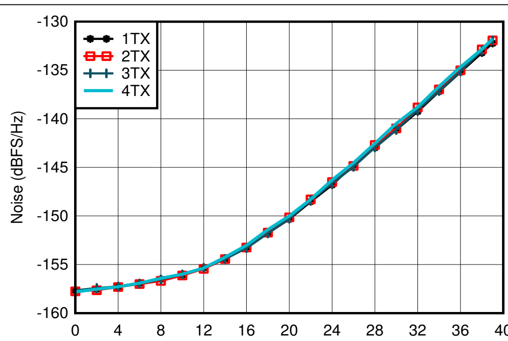
Figure 5-469. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

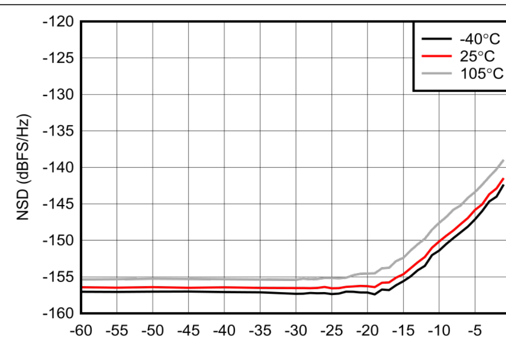
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-470. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



A. f_{DAC}=11796.48 MSPS, interleave mode, matching at 3.5 GHz, A_{out} = –13 dBFS.

Figure 5-471. TX NSD vs DSA Setting at 3.5 GHz

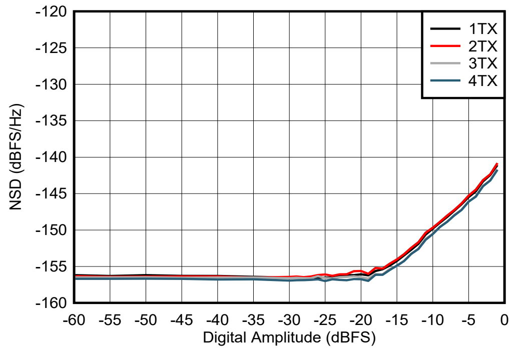


A. f_{DAC} = 12 MSPS, external clock mode, non-interleave mode

Figure 5-472. TX NSD vs Digital Amplitude and Temperature at 3.75 GHz

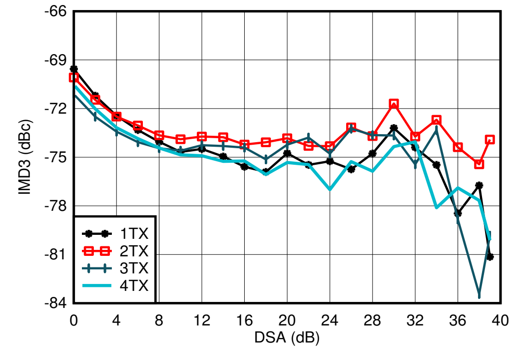
5.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



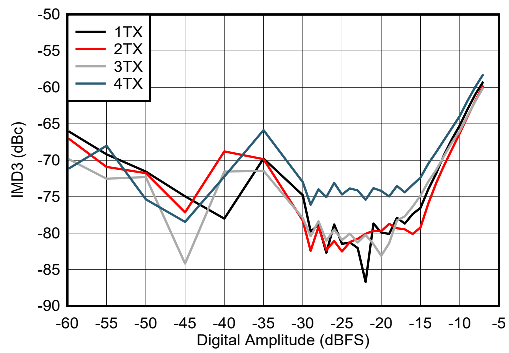
A. f_{DAC} = 12 MSPS, external clock mode, non-interleave mode

Figure 5-473. TX NSD vs Digital Amplitude and Channel at 3.75 GHz



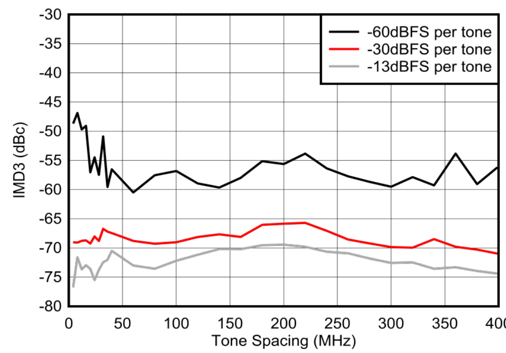
20-MHz tone spacing, 3.5 GHz Matching, –13 dBFS each tone, included PCB and cable losses

Figure 5-474. TX IMD3 vs DSA Setting at 3.5 GHz



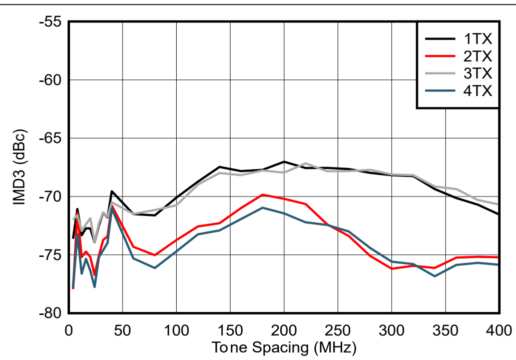
20-MHz tone spacing, 3.5 GHz Matching

Figure 5-475. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz



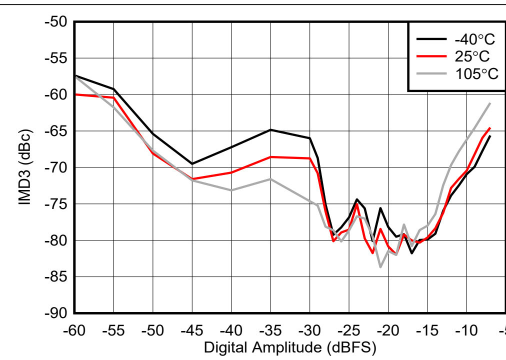
50-MHz tone spacing, external clock mode, non-interleave mode

Figure 5-476. TX IMD3 vs Tone Spacing and Amplitude at 3.75 GHz



External clock mode, non-interleave mode

Figure 5-477. TX IMD3 vs Tone Spacing and Channel at 3.75 GHz

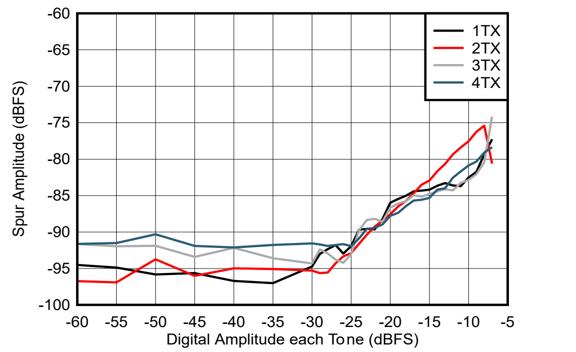


50-MHz tone spacing, external clock mode, non-interleave mode

Figure 5-478. TX IMD3 vs Digital Amplitude and Temperature at 3.75 GHz

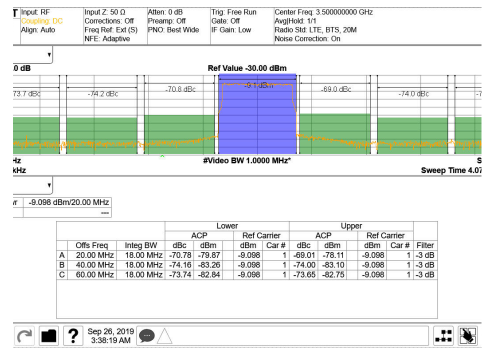
5.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



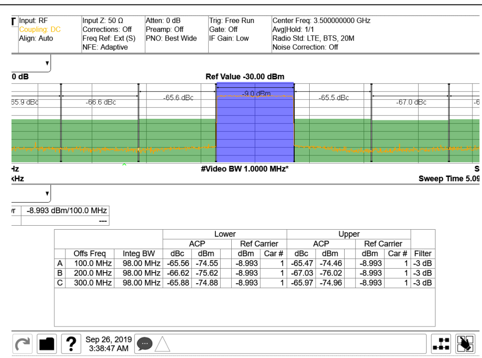
Inband = 3.75 GHz ± 600 MHz, f_{DAC} = 9 GSPS, external clock mode, non-interleave mode.

Figure 5-479. Two Tone Inband SFDR vs Digital Amplitude at 3.75 GHz



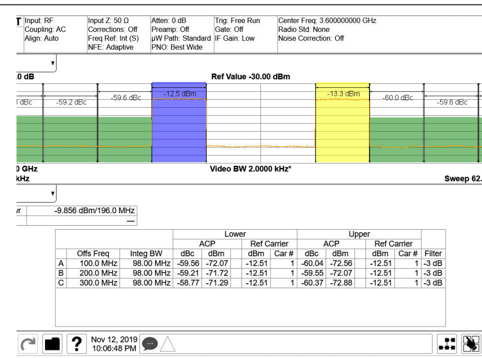
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 5-480. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)



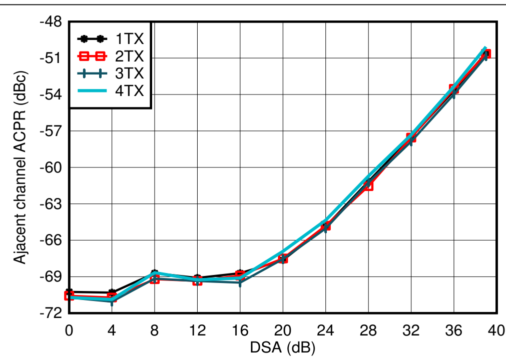
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 5-481. TX 100-MHz NR Output Spectrum at 3.5 GHz (Band 42)



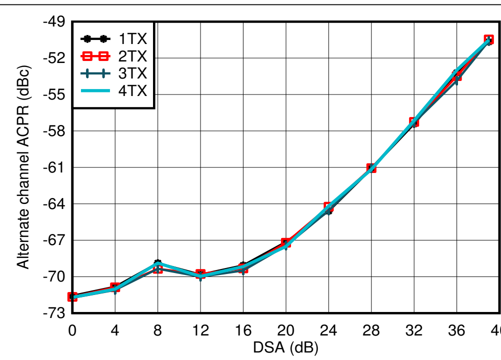
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 5-482. TX 2 carrier 100-MHz NR Output Spectrum at 3.45 GHz and 3.75 GHz



3.5 GHz Matching, single carrier 20-MHz BW NR TM1.1 LTE

Figure 5-483. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz

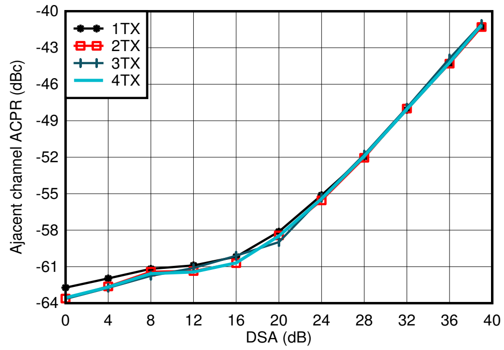


3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 5-484. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz

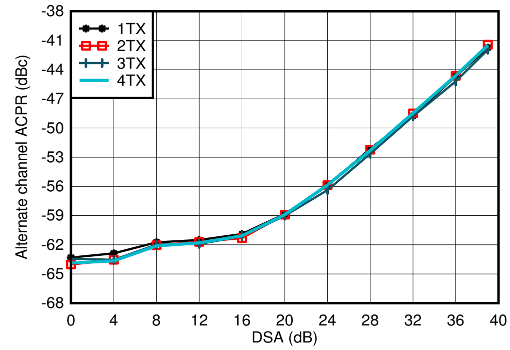
5.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



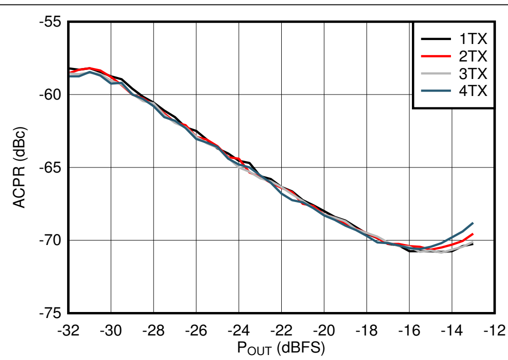
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 5-485. TX 100-MHz NR ACPR vs DSA Setting at 3.5 GHz



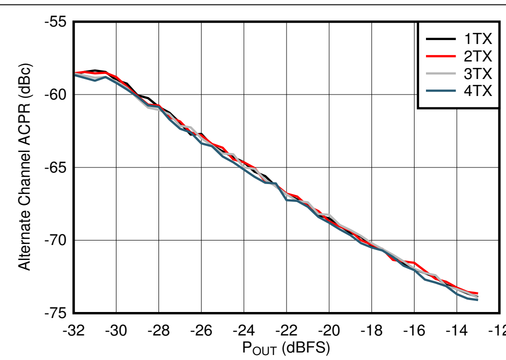
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 5-486. TX 100-MHz NR alt-ACPR vs DSA Setting at 3.5 GHz



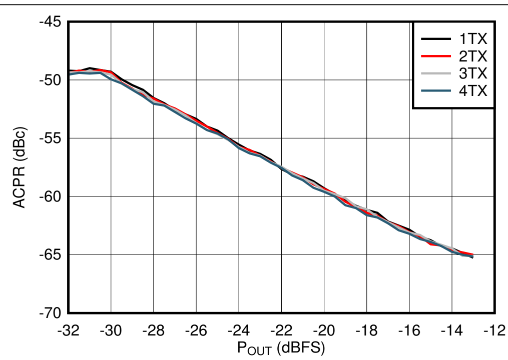
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 5-487. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz



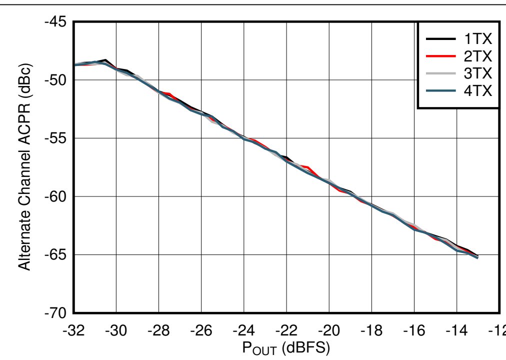
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 5-488. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz



3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 5-489. TX 100-MHz NR ACPR vs Digital Level at 3.5 GHz

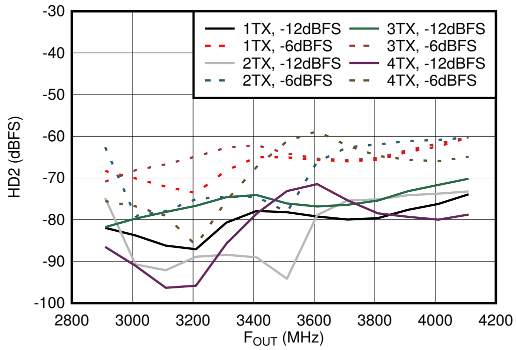


3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 5-490. TX 100-MHz NR alt-ACPR vs Digital Level at 3.5 GHz

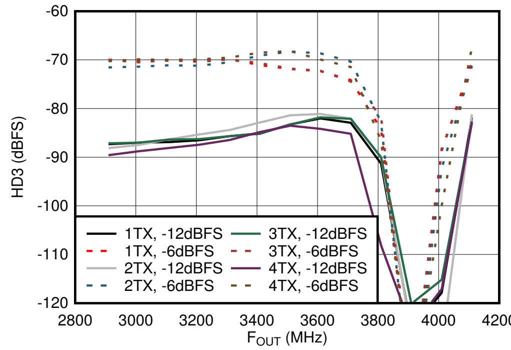
5.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



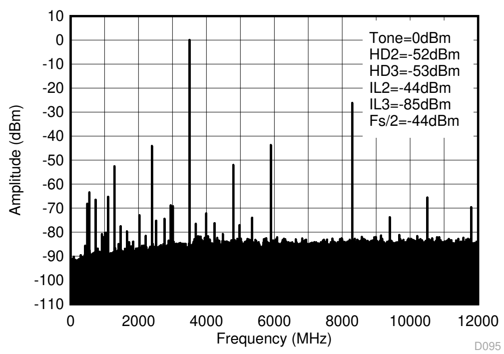
Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 5-491. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz



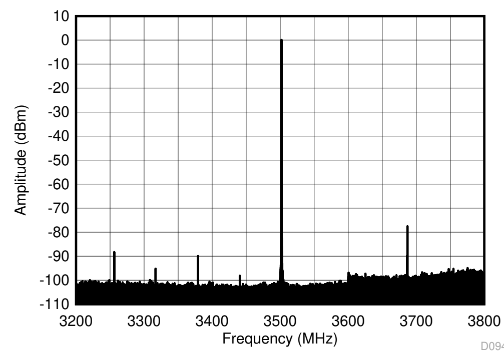
Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

Figure 5-492. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz



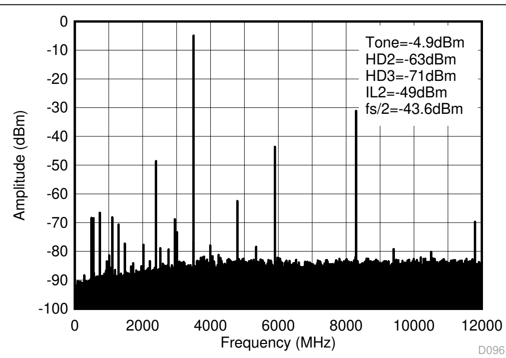
Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

Figure 5-493. TX Single Tone (–1 dBFS) Output Spectrum at 3.5 GHz (0 - f_{DAC})



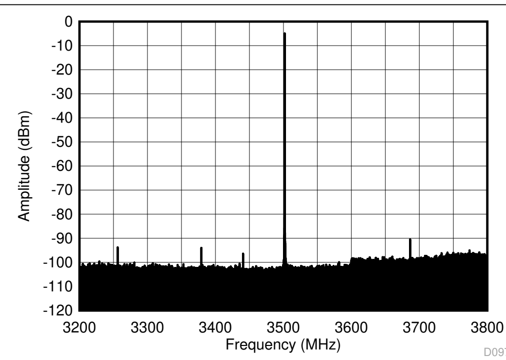
Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

Figure 5-494. TX Single Tone (–1 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)



Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

Figure 5-495. TX Single Tone (–6 dBFS) Output Spectrum at 3.5 GHz (0-f_{DAC})

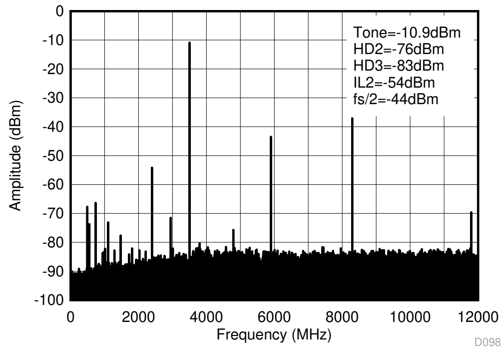


Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

Figure 5-496. TX Single Tone (–6 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)

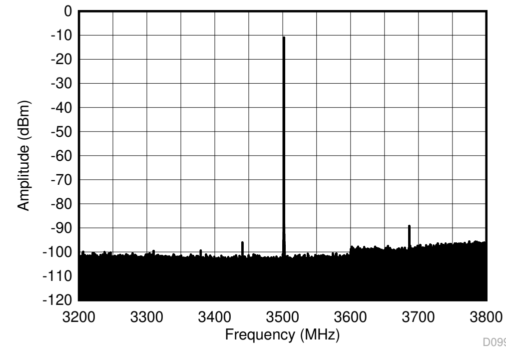
5.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



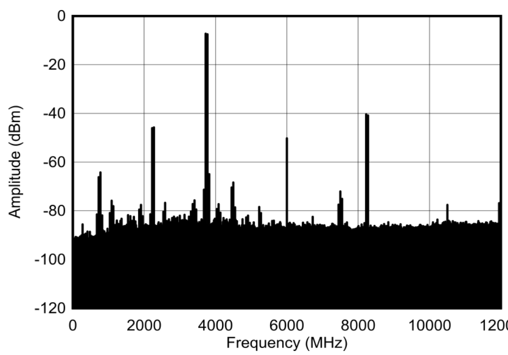
Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

Figure 5-497. TX Single Tone (–12 dBFS) Output Spectrum at 3.5 GHz (0-f_{DAC})



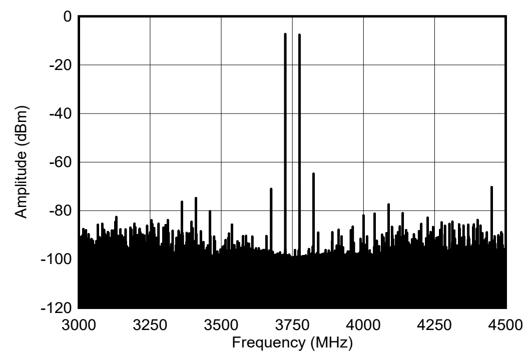
Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

Figure 5-498. TX Single Tone (–12 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)



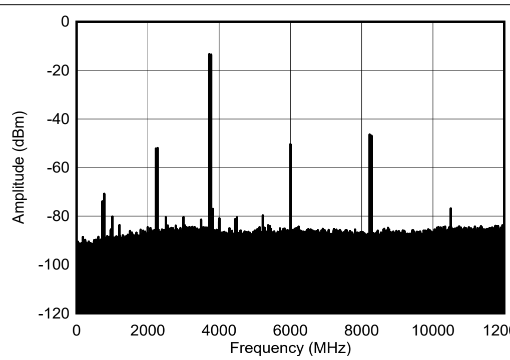
Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

Figure 5-499. TX Dual Tone Output Spectrum at 3.75 GHz, -7 dBFS each (0 - f_{DAC})



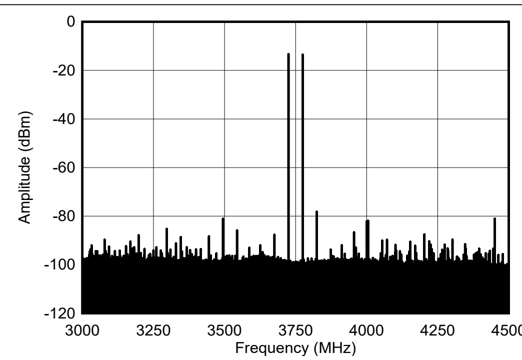
Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

Figure 5-500. TX Dual Tone Output Spectrum at 3.75 GHz, -7 dBFS each (±600 MHz)



Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

Figure 5-501. TX Dual Tone Output Spectrum at 3.75 GHz, -13 dBFS each (0 - f_{DAC})

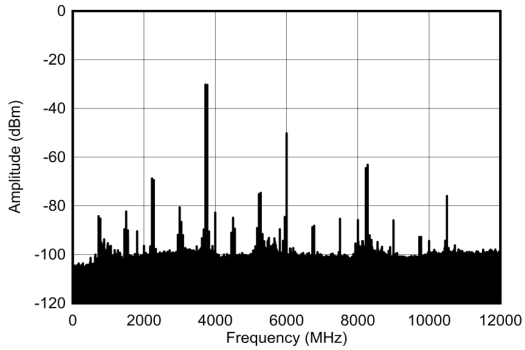


Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

Figure 5-502. TX Dual Tone Output Spectrum at 3.75 GHz, -13 dBFS each (±600 MHz)

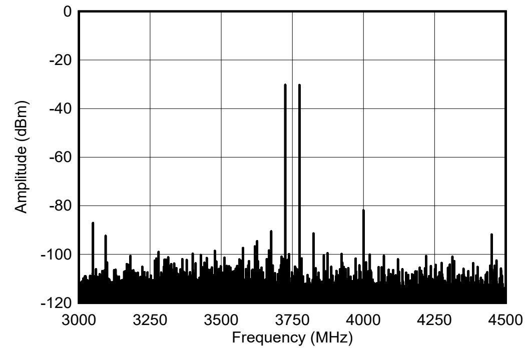
5.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1^{st} Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



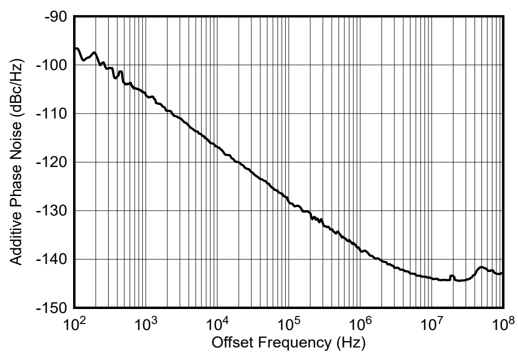
Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

Figure 5-503. TX Dual Tone Output Spectrum at 3.75 GHz, -30 dBFS each (0 - f_{DAC})



Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

Figure 5-504. TX Dual Tone Output Spectrum at 3.75 GHz, -30 dBFS each (±600 MHz)

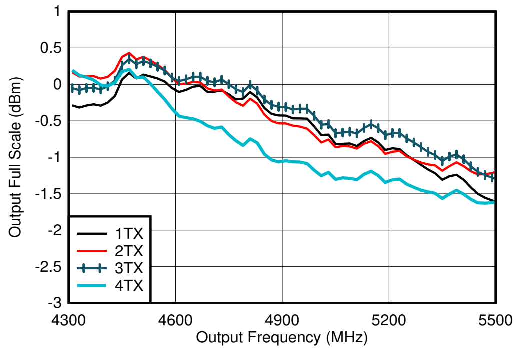


f_{DAC} = f_{CLK} = 12 GSPS, non-interleave mode.

Figure 5-505. External Clock Additive Phase Noise at 3.7 GHz

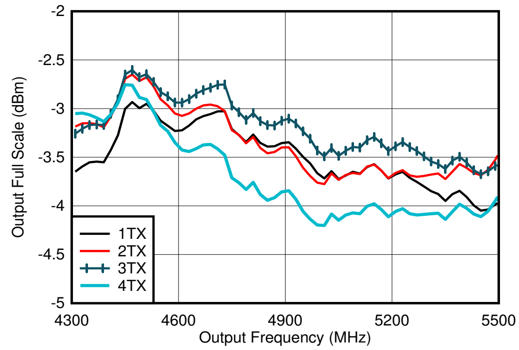
5.12.13 TX Typical Characteristics at 4.9 GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



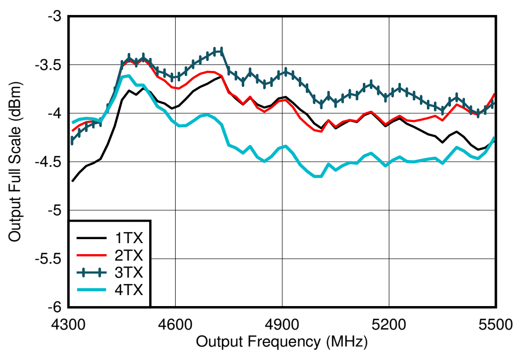
Excluding PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 4.9 GHz matching

Figure 5-506. TX Full Scale vs RF Frequency and Channel at 11796.48 MSPS



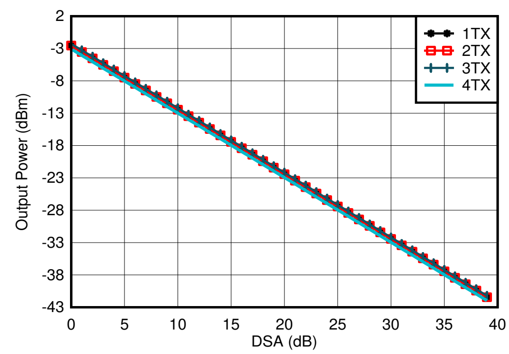
Excluding PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 4.9 GHz matching

Figure 5-507. TX Full Scale vs RF Frequency and Channel at 5898.24M SPS, Mix Mode, 2nd Nyquist Zone



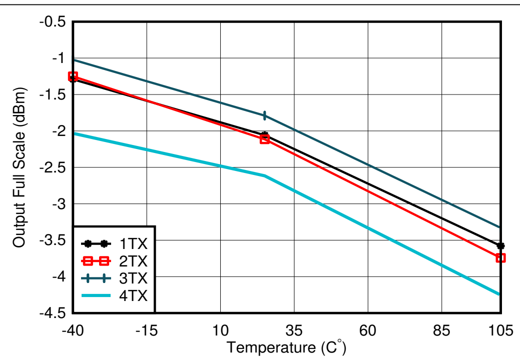
Excluding PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 4.9 GHz matching

Figure 5-508. TX Full Scale vs RF Frequency and Channel at 8847.36 MSPS, Mix Mode, 2nd Nyquist Zone



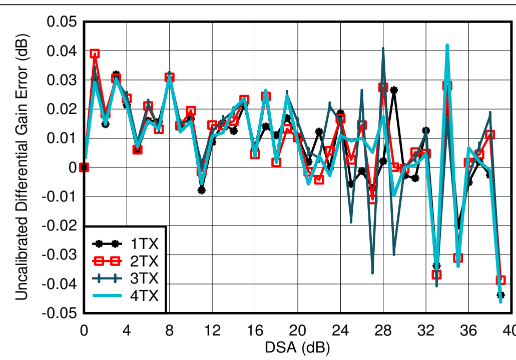
f_{DAC} = 11796.48 MSPS, A_{out} = -0.5 dBFS, matching 4.9 GHz

Figure 5-509. TX Output Power vs DSA Setting and Channel at 4.9 GHz



A_{out} = -0.5 dBFS, 4.9 GHz Matching, PCB and cable losses included.

Figure 5-510. TX Full Scale Output Power vs Temperature and Channel at 4.9 GHz

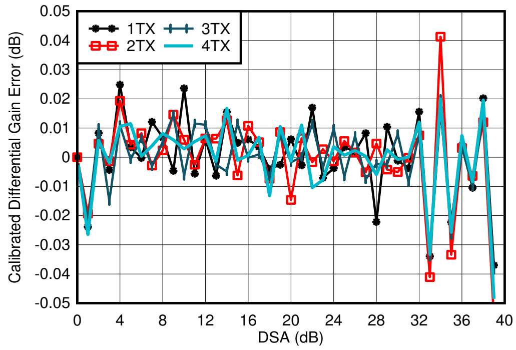


f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-511. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz

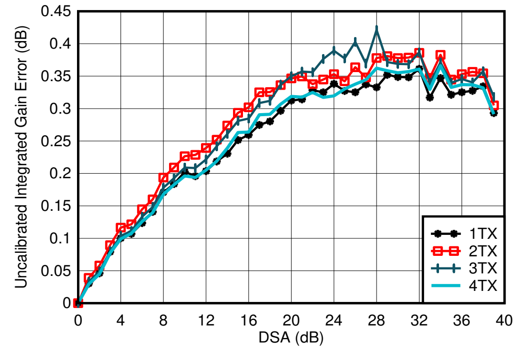
5.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



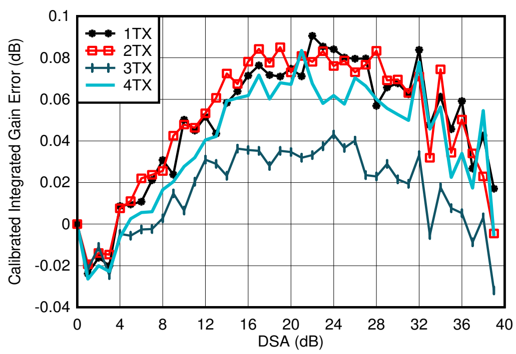
f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-512. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz



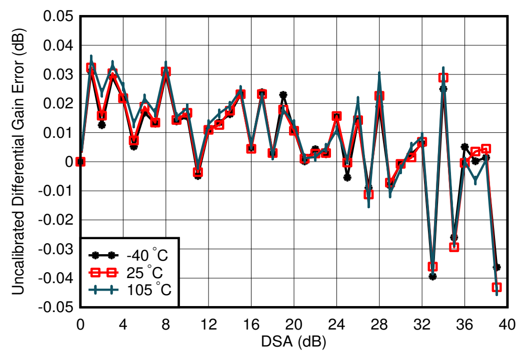
f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 5-513. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 5-514. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz

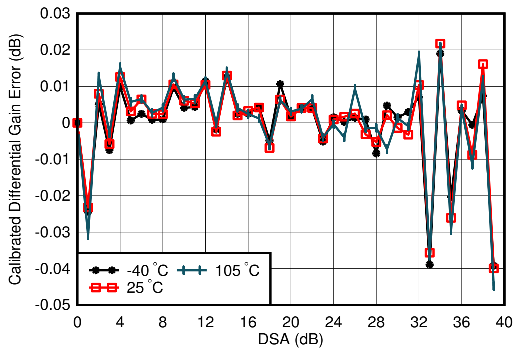


f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 5-515. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz

5.12.13 TX Typical Characteristics at 4.9 GHz (continued)

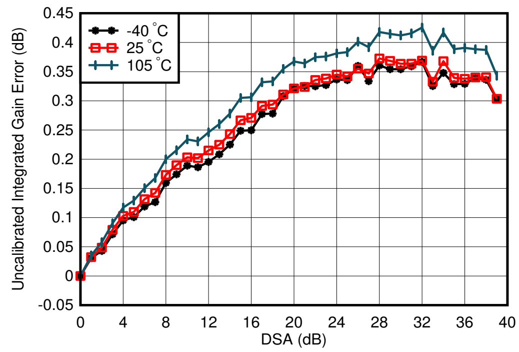
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

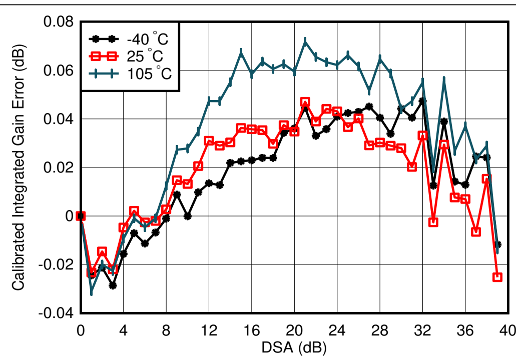
Figure 5-516. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

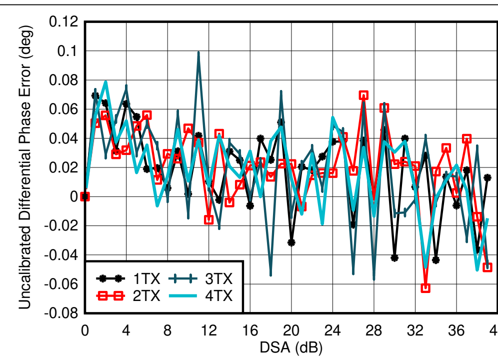
Figure 5-517. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 5-518. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



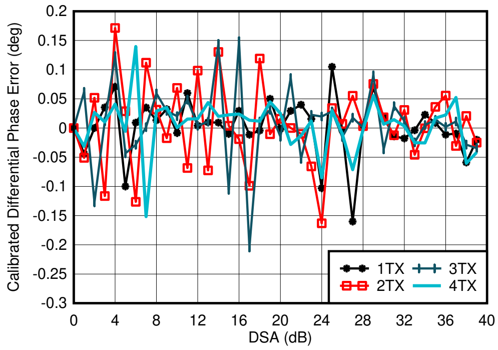
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-519. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

5.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

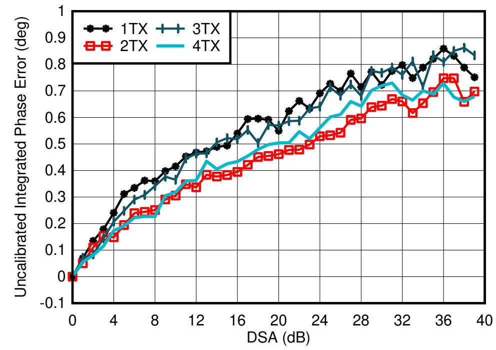


f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Phase DNL spike may occur at any DSA setting.

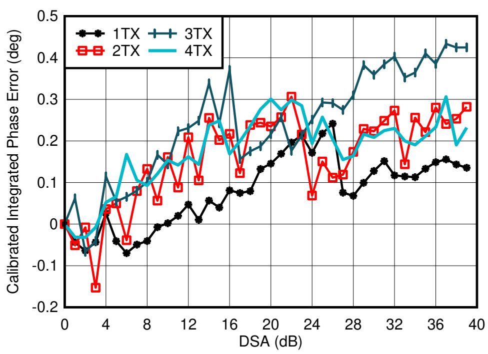
Figure 5-520. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

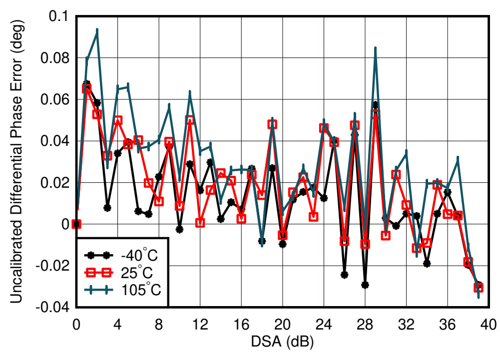
Figure 5-521. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-522. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



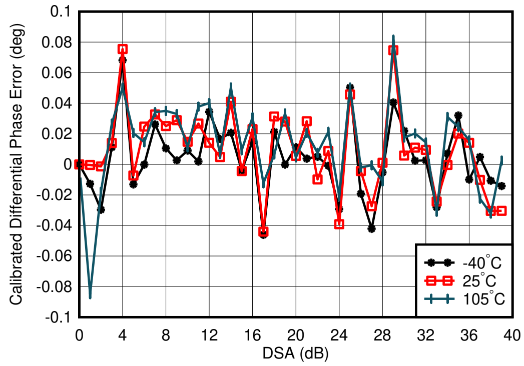
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 5-523. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz

5.12.13 TX Typical Characteristics at 4.9 GHz (continued)

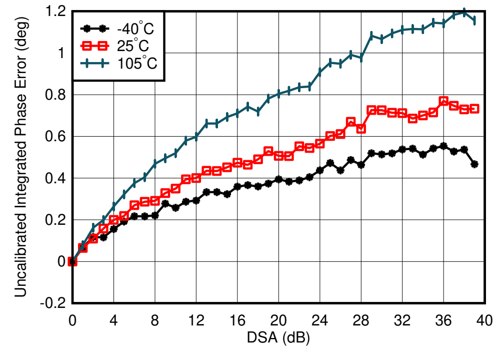
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

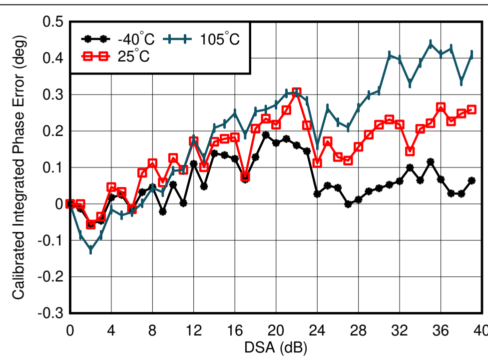
Figure 5-524. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

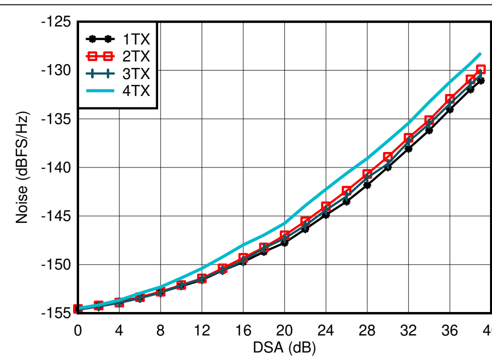
Figure 5-525. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-526. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz

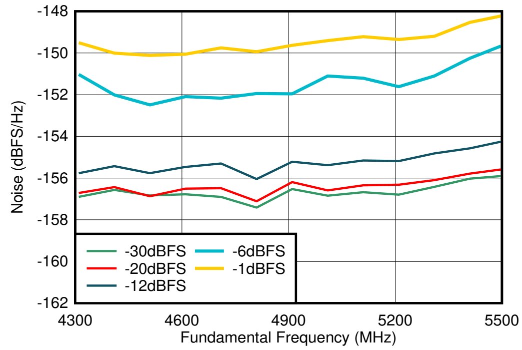


f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, P_{OUT} = –13 dBFS

Figure 5-527. TX Output Noise vs Channel and Attenuation at 4.9 GHz

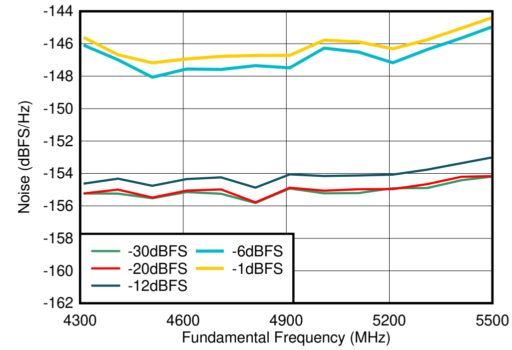
5.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



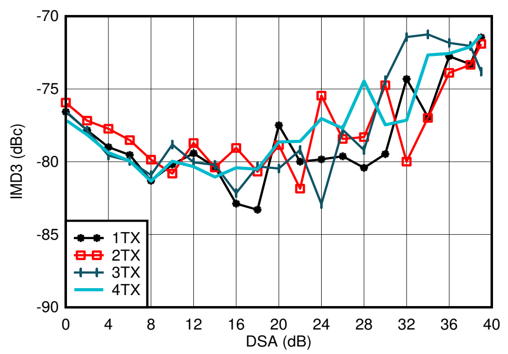
f_{DAC}=11796.48 MSPS, interleave mode, matching at 4.9 GHz, A_{out} = –13 dBFS.

Figure 5-528. TX NSD vs Output Frequency and Digital Amplitude at 4.9 GHz (DSA = 0 dB)



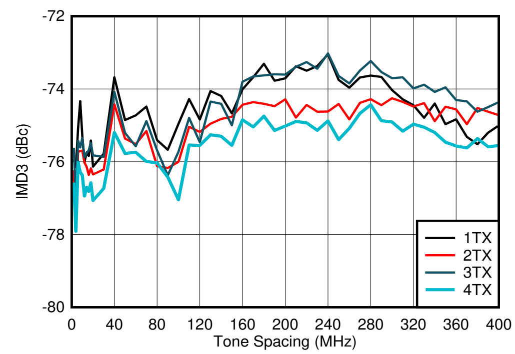
f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz, A_{out} = –13 dBFS.

Figure 5-529. TX NSD vs Output Frequency and Digital Amplitude at 4.9 GHz (DSA = 6 dB)



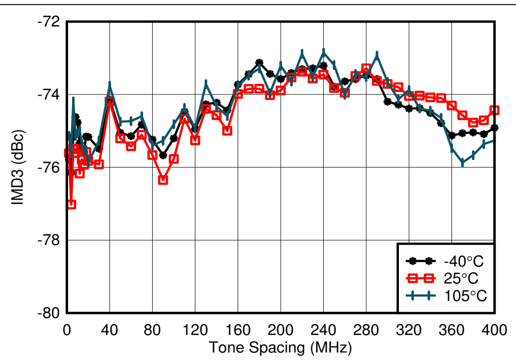
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9 GHz, -13 dBFS each tone

Figure 5-530. TX IMD3 vs DSA Setting at 4.9 GHz



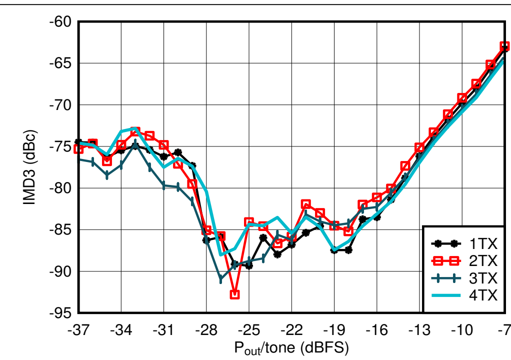
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9 GHz, –13 dBFS each tone

Figure 5-531. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9 GHz, –13 dBFS each tone, worst channel

Figure 5-532. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz

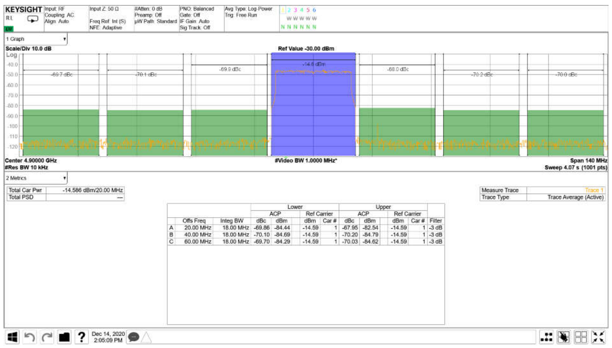


f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9 GHz, $f_{SPACING}$ = 20 MHz

Figure 5-533. TX IMD3 vs Digital Level at 4.9 GHz

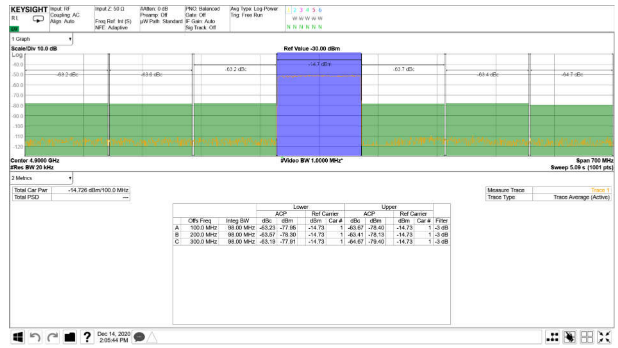
5.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



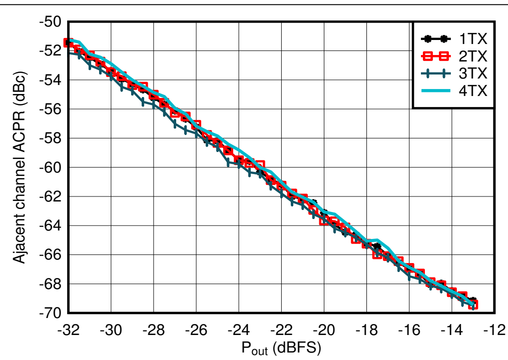
TM1.1, P_{OUT_RMS} = –13 dBFS

Figure 5-534. TX 20-MHz LTE Output Spectrum at 4.9 GHz



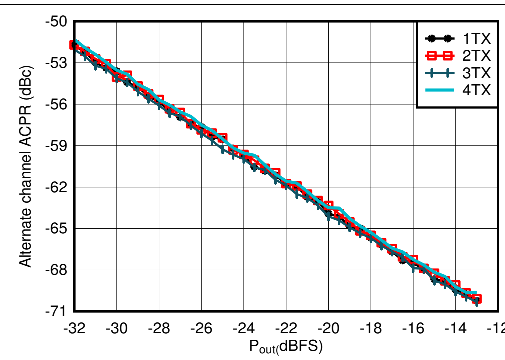
TM1.1, P_{OUT_RMS} = –13 dBFS

Figure 5-535. TX 100-MHz NR Output Spectrum at 4.9 GHz



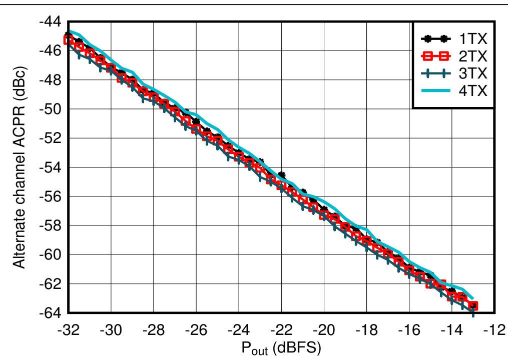
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-536. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz



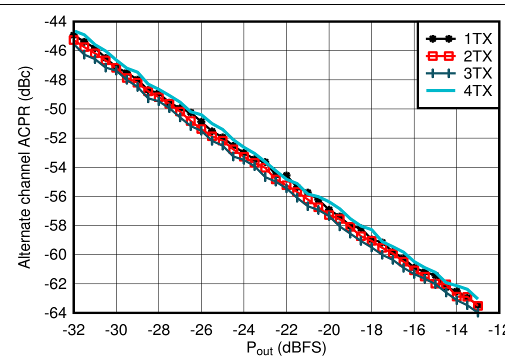
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-537. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 5-538. TX 100-MHz NR ACPR vs Digital Level at 4.9 GHz

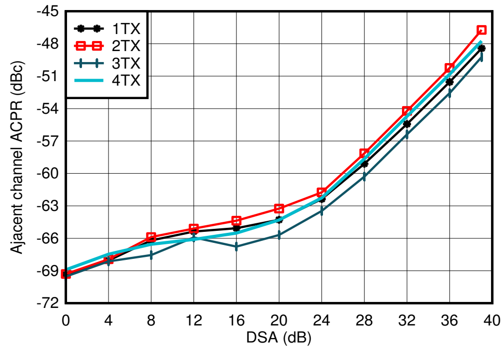


Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 5-539. TX 100-MHz NR alt-ACPR vs Digital Level at 4.9 GHz

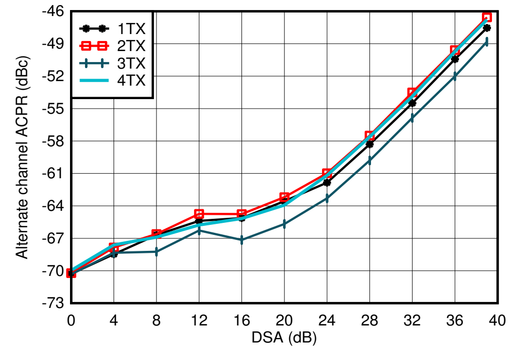
5.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



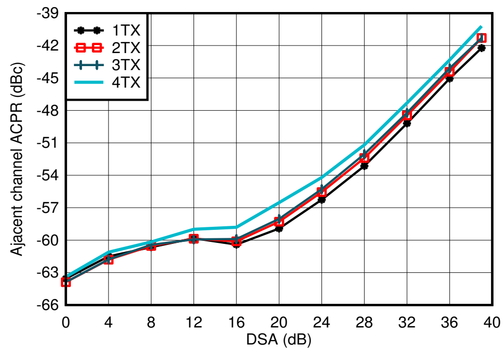
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-540. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz



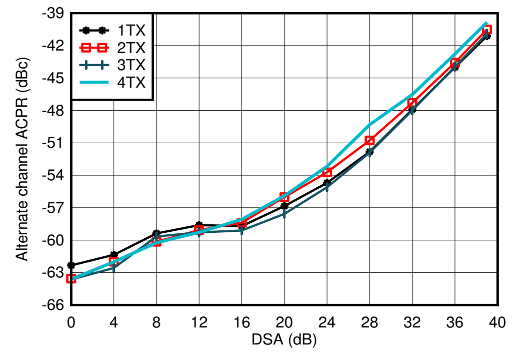
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-541. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz



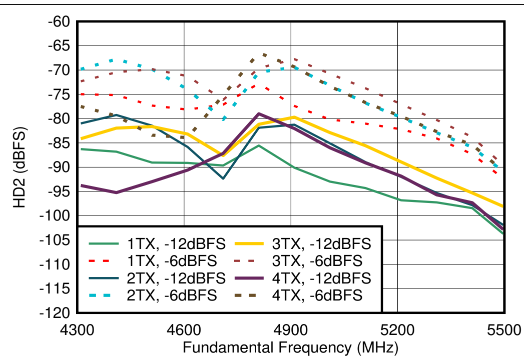
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 5-542. TX 100-MHz NR ACPR vs DSA at 4.9 GHz



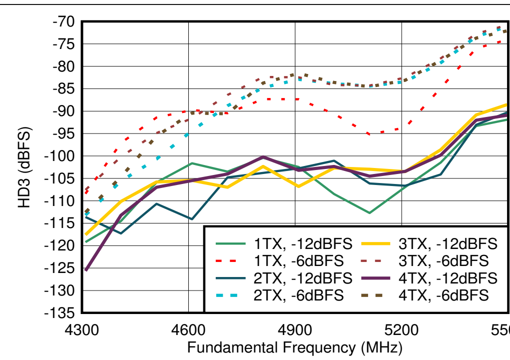
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 5-543. TX 100-MHz NR alt-ACPR vs DSA at 4.9 GHz



Matching at 4.9 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 5-544. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz

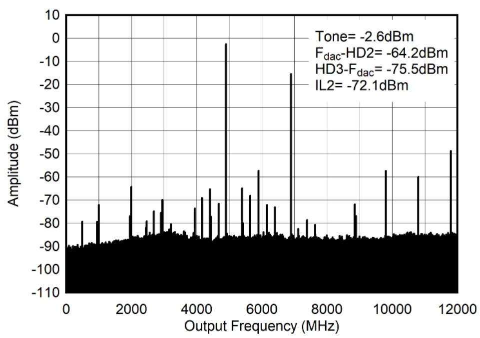


Matching at 4.9 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 5-545. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz

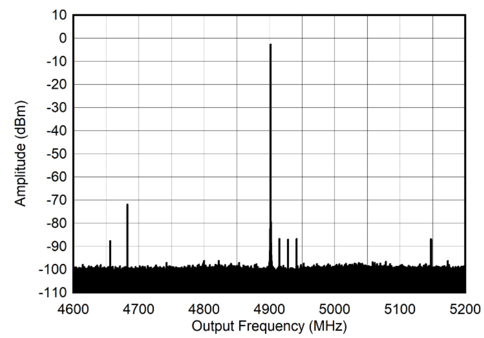
5.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



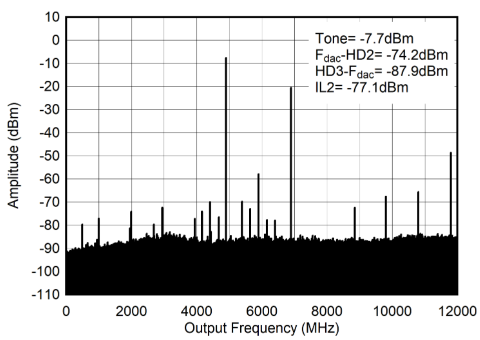
f_{DAC} = 11796.48 MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 5-546. TX Single Tone (–1 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})



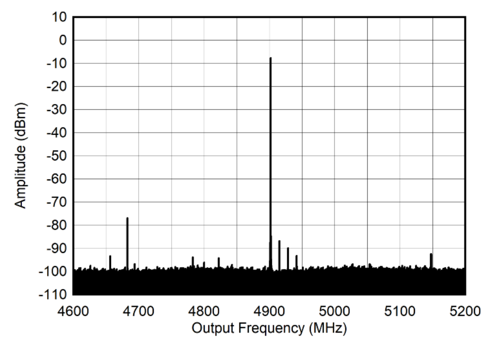
f_{DAC} = 11796.48 MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

Figure 5-547. TX Single Tone (–1 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)



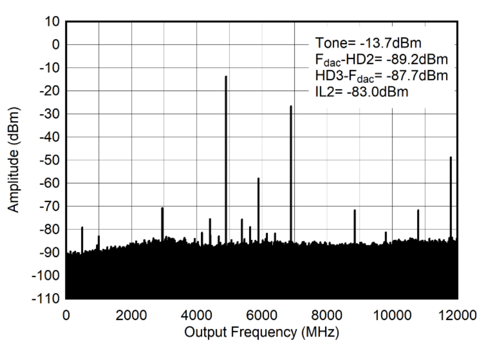
f_{DAC} = 11796.48 MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 5-548. TX Single Tone (–6 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})



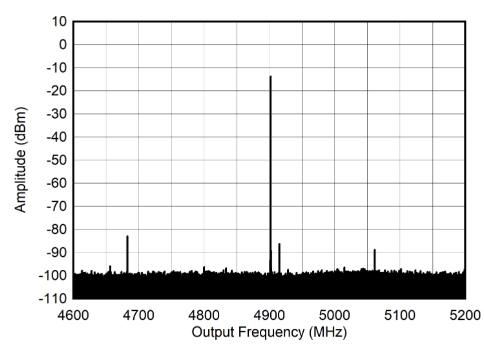
f_{DAC} = 11796.48 MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

Figure 5-549. TX Single Tone (–6 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)



f_{DAC} = 11796.48 MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 5-550. TX Single Tone (–12 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})

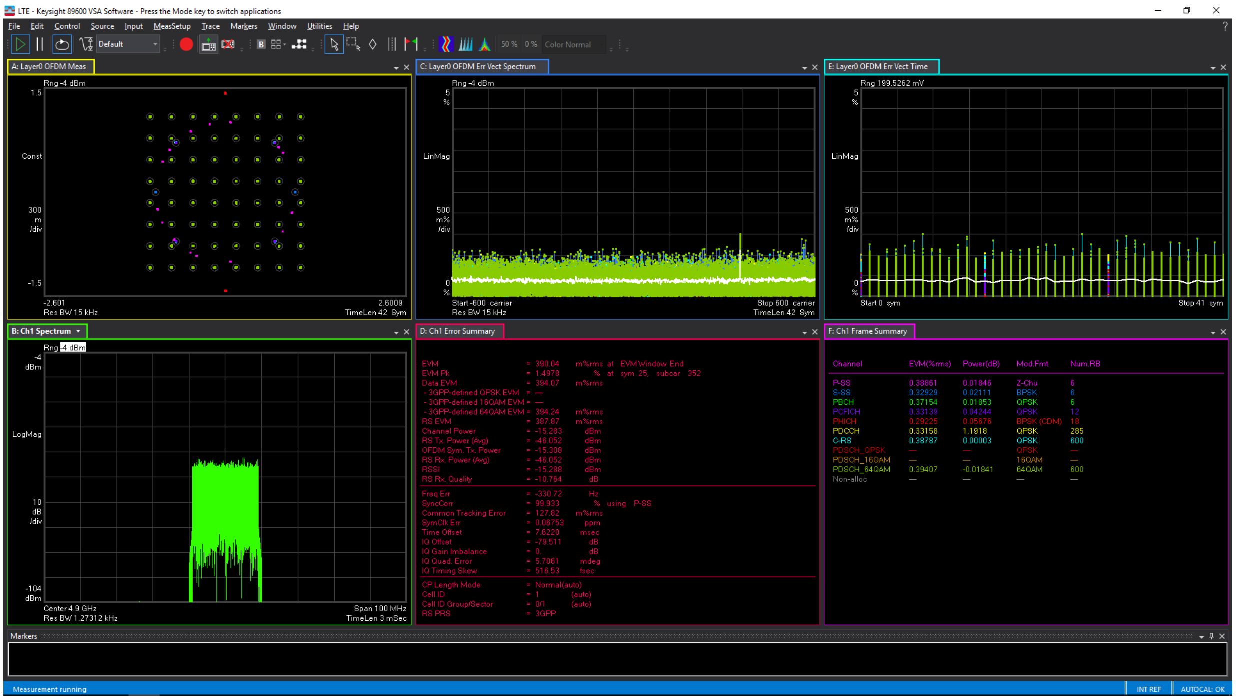


f_{DAC} = 11796.48 MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

Figure 5-551. TX Single Tone (–12 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)

5.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

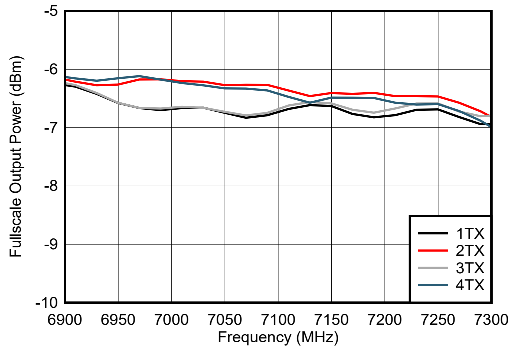


TM1.1, P_{OUT_RMS} = –13 dBFS

Figure 5-552. TX 20-MHz LTE Error Vector Magnitude at 4.9 GHz

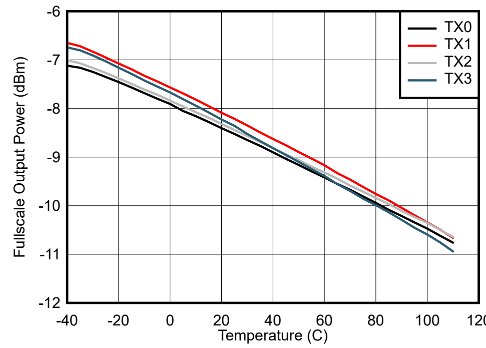
5.12.14 TX Typical Characteristics at 7.1 GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



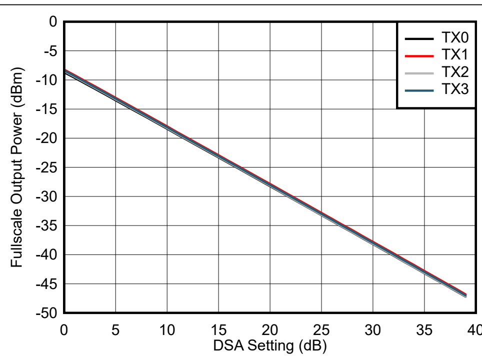
Excluding PCB and cable losses

Figure 5-553. TX Full Scale vs RF Frequency and Channel



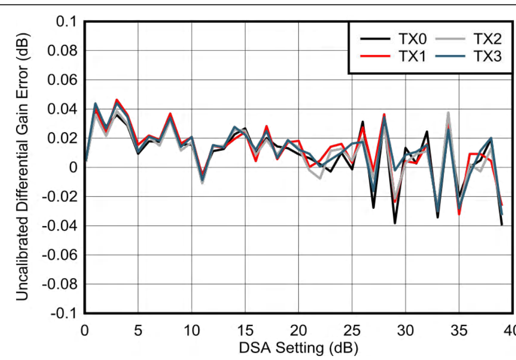
Excluding PCB and cable losses

Figure 5-554. TX Full Scale vs Temperature and Channel at 7.1 GHz



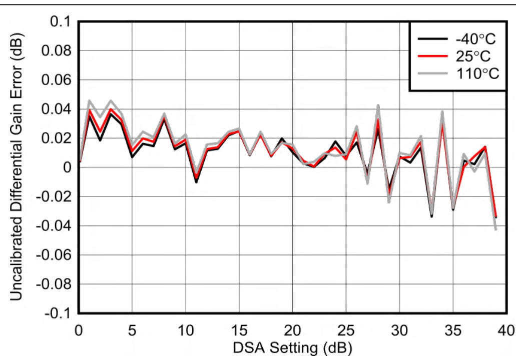
Excluding PCB and cable losses

Figure 5-555. TX Full Scale vs DSA Setting and Channel at 7.1 GHz



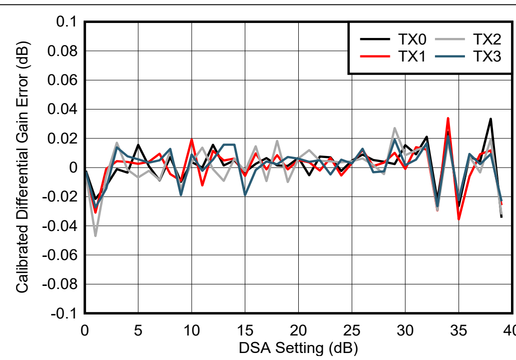
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

Figure 5-556. Uncalibrated Differential Gain Error vs Channel at 7.1 GHz



Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

Figure 5-557. Uncalibrated Differential Gain Error vs Temperature at 7.1 GHz

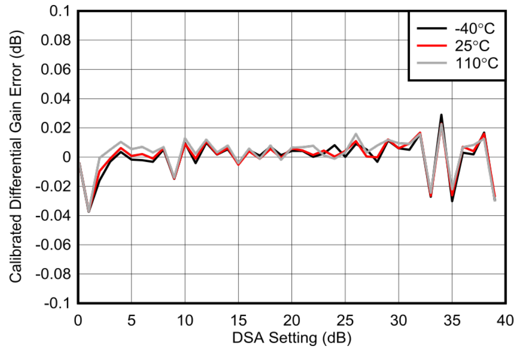


Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

Figure 5-558. Calibrated Differential Gain Error vs Channel at 7.1 GHz

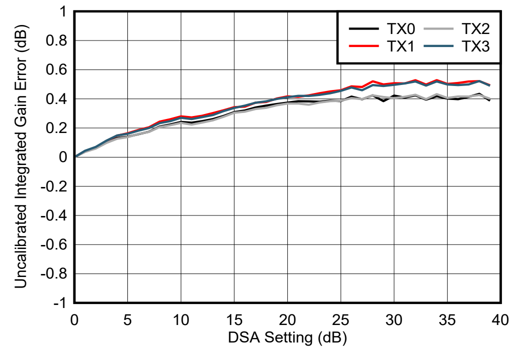
5.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



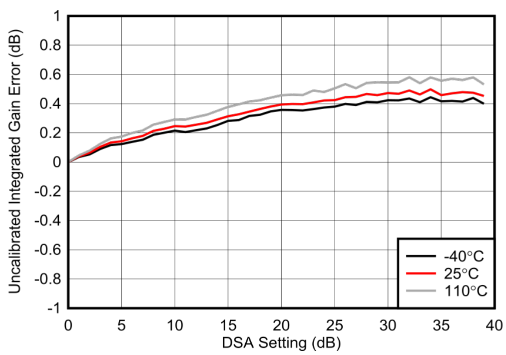
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

Figure 5-559. Calibrated Differential Gain Error vs Temperature at 7.1 GHz



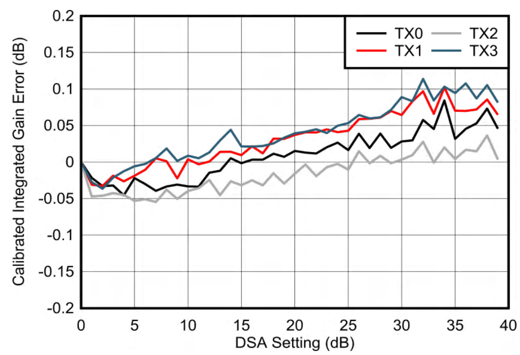
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

Figure 5-560. Uncalibrated Integrated Gain Error vs Channel at 7.1 GHz



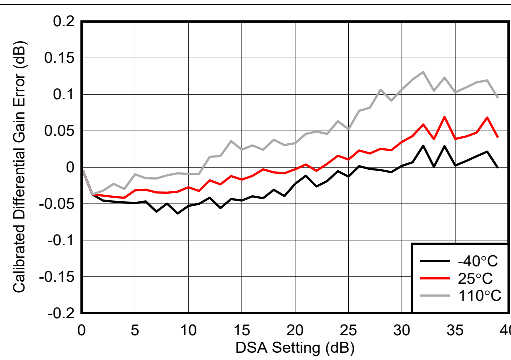
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

Figure 5-561. Uncalibrated Integrated Gain Error vs Temperature at 7.1 GHz



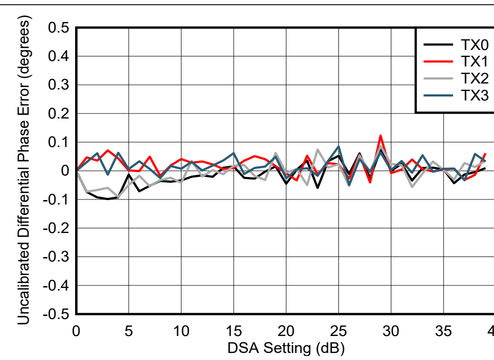
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

Figure 5-562. Calibrated Integrated Gain Error vs Channel at 7.1 GHz



Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

Figure 5-563. Calibrated Integrated Gain Error vs Temperature at 7.1 GHz

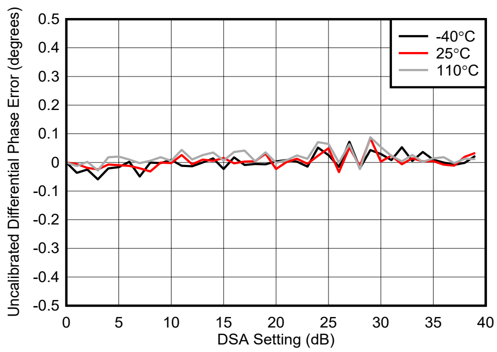


Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

Figure 5-564. Uncalibrated Differential Phase Error vs Channel at 7.1 GHz

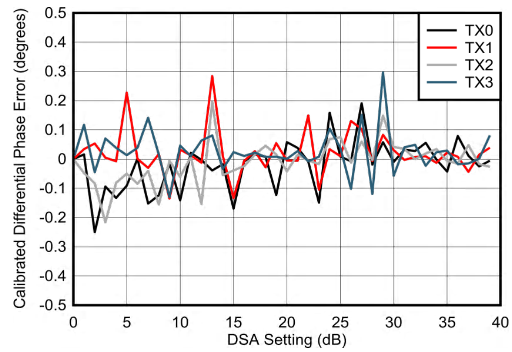
5.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



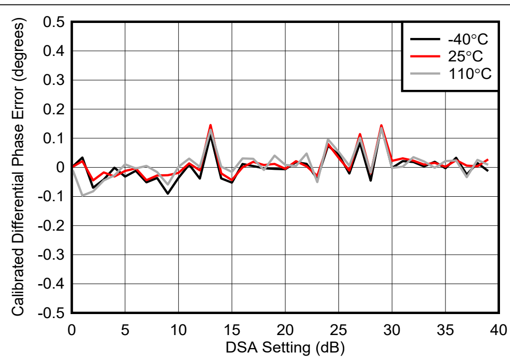
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

Figure 5-565. Uncalibrated Differential Phase Error vs Temperature at 7.1 GHz



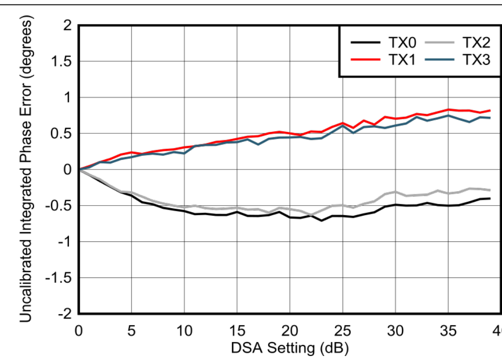
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

Figure 5-566. Calibrated Differential Phase Error vs Channel at 7.1 GHz



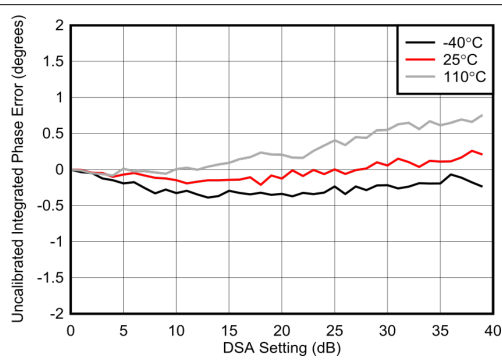
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

Figure 5-567. Calibrated Differential Phase Error vs Temperature at 7.1 GHz



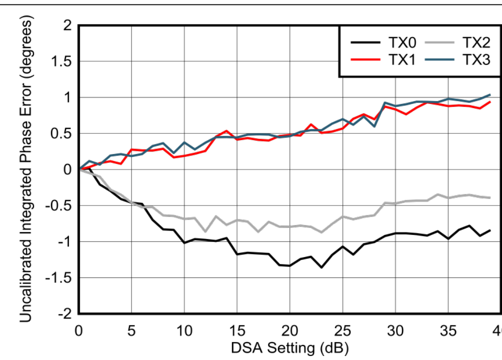
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-568. Uncalibrated Integrated Phase Error vs Channel at 7.1 GHz



Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-569. Uncalibrated Integrated Phase Error vs Temperature at 7.1 GHz

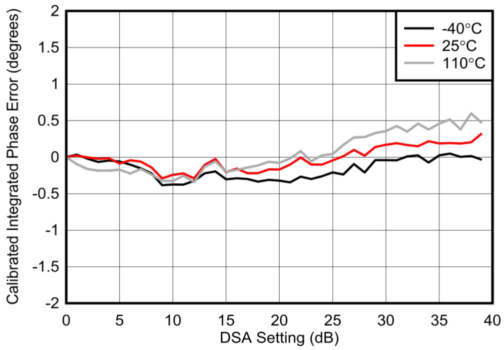


Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-570. Calibrated Integrated Phase Error vs Channel at 7.1 GHz

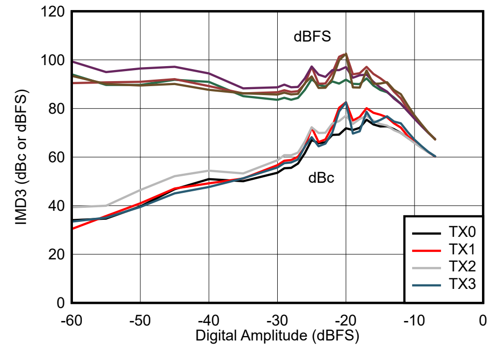
5.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



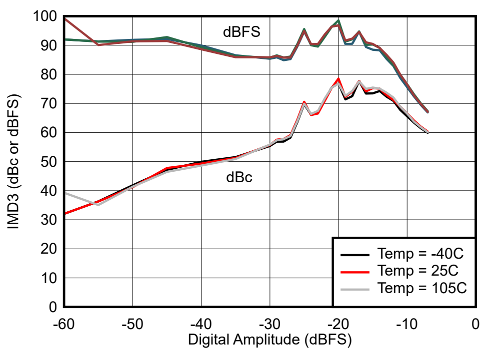
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 5-571. Calibrated Integrated Phase Error vs Temperature at 7.1 GHz



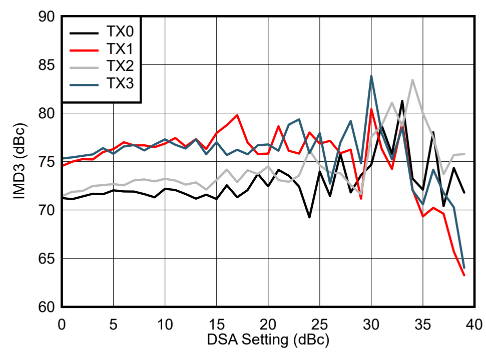
Tone spacing = 50 MHz

Figure 5-572. IMD3 vs Digital Amplitude and Channel at 7.1 GHz



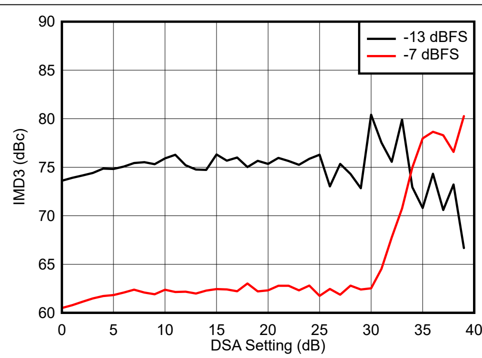
Tone spacing = 50 MHz

Figure 5-573. IMD3 vs Digital Amplitude and Temperature at 7.1 GHz



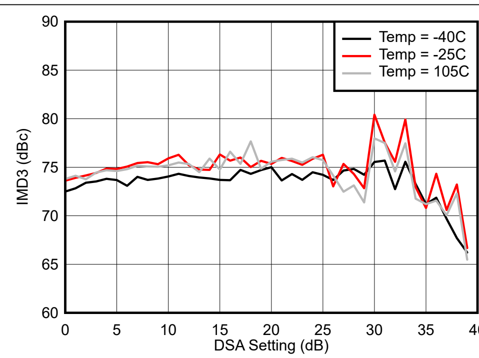
Tone spacing = 50 MHz

Figure 5-574. IMD3 vs DSA Setting and Channel at 7.1 GHz



Tone spacing = 5 0MHz

Figure 5-575. IMD3 vs DSA Setting and Digital Amplitude at 7.1 GHz



Tone spacing = 50 MHz

Figure 5-576. IMD3 vs DSA Setting and Temperature at 7.1 GHz

5.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.

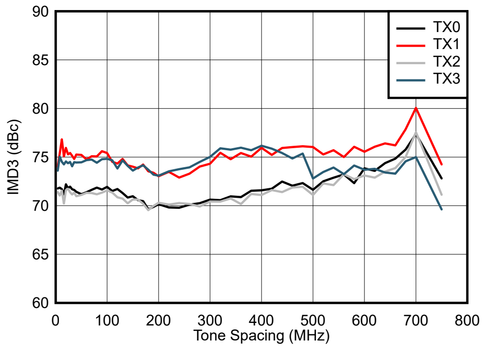


Figure 5-577. IMD3 vs Tone Spacing and Channel at 7.1 GHz

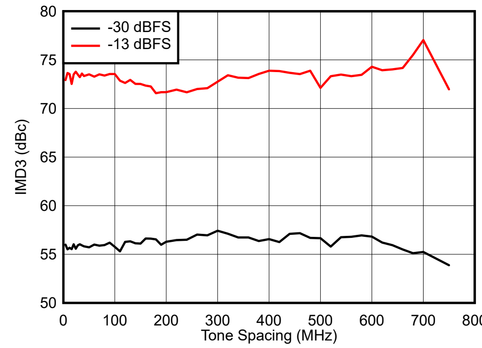


Figure 5-578. IMD3 vs Tone Spacing and Digital Amplitude at 7.1 GHz

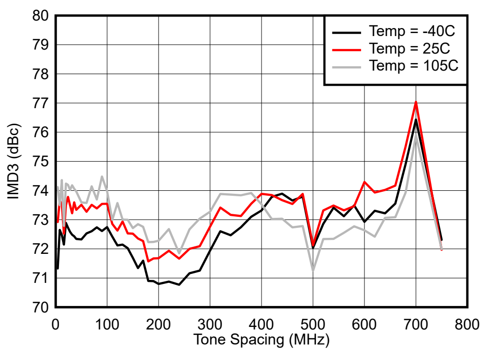
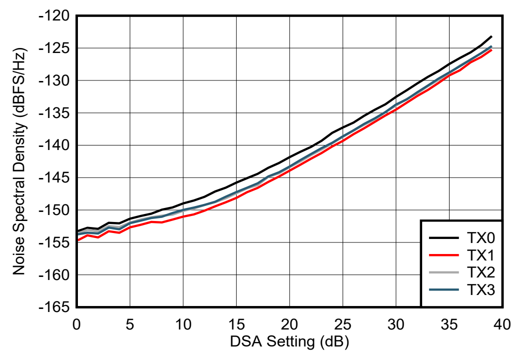
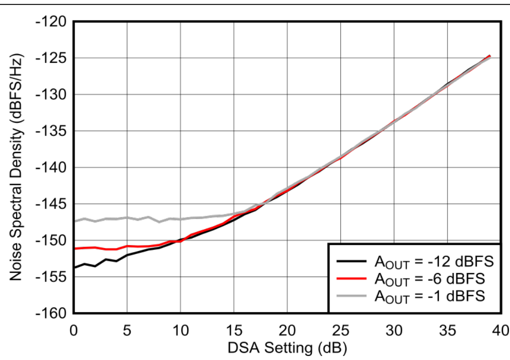


Figure 5-579. IMD3 vs Tone Spacing and Temperature at 7.1 GHz



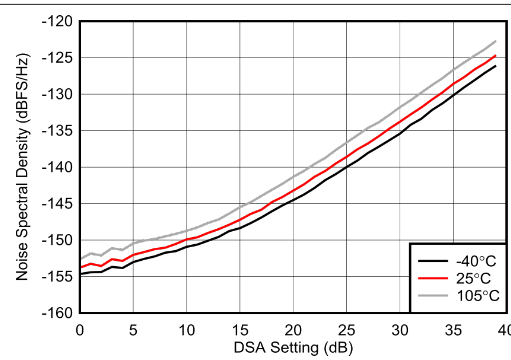
Tone at -12 dBFS, 50 MHz offset from tone

Figure 5-580. NSD vs DSA Setting and Channel at 7.1 GHz



50 MHz offset from tone

Figure 5-581. NSD vs DSA Setting and Amplitude at 7.1 GHz

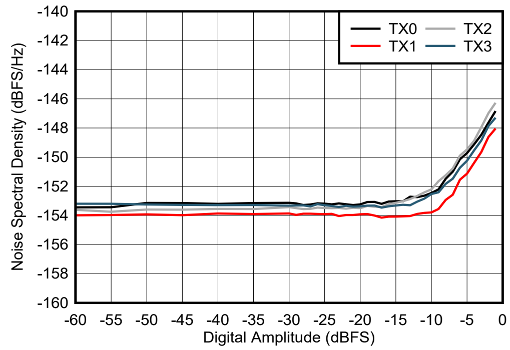


Tone at -12 dBFS, 50 MHz offset from tone

Figure 5-582. NSD vs DSA Setting and Temperature at 7.1 GHz

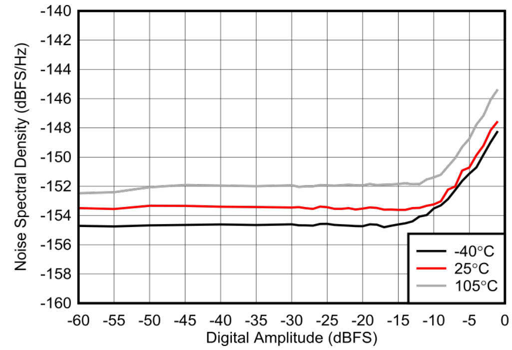
5.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



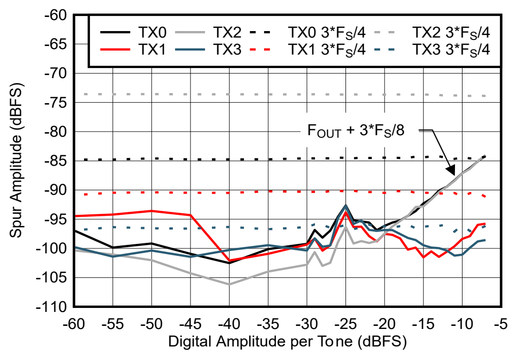
50MHz offset from tone

Figure 5-583. NSD vs Digital Amplitude and Channel at 7.1 GHz



50MHz offset from tone

Figure 5-584. NSD vs Digital Amplitude and Temperature at 7.1 GHz



Inband = 7100 MHz ± 600 MHz, excluding IMD3 components, 3 x F_S/4 spur not included and shown separately

Figure 5-585. Two Tone Inband SFDR vs Digital Amplitude at 7.1 GHz

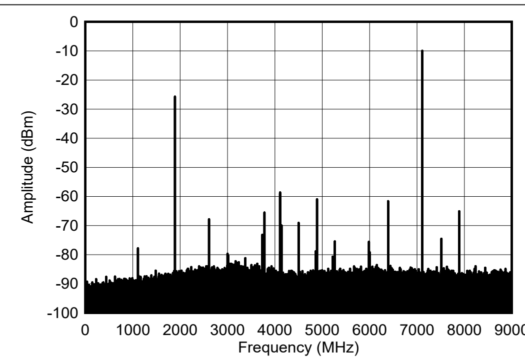


Figure 5-586. Single Tone Output Spectrum at 7.1 GHz, -1 dBFS ($0 - F_{DAC}$)

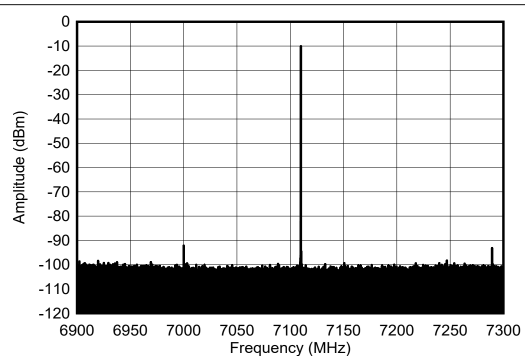


Figure 5-587. Single Tone Output Spectrum at 7.1 GHz, -1 dBFS (Inband)

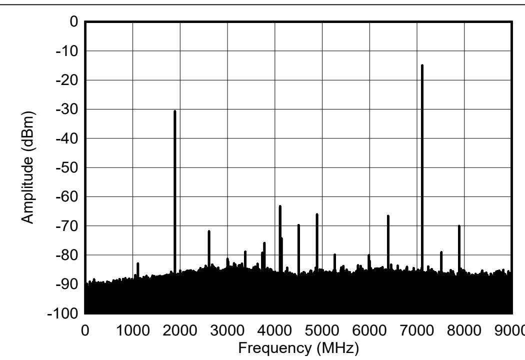


Figure 5-588. Single Tone Output Spectrum at 7.1 GHz, -6 dBFS ($0 - F_{DAC}$)

5.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.

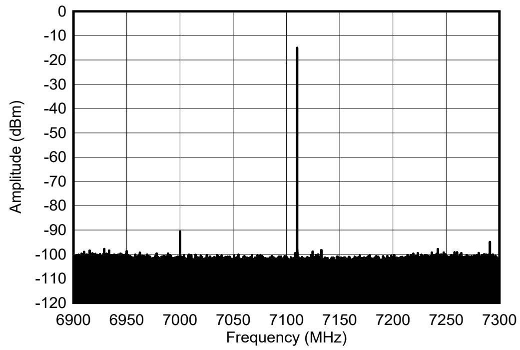


Figure 5-589. Single Tone Output Spectrum at 7.1 GHz, -6 dBFS (Inband)

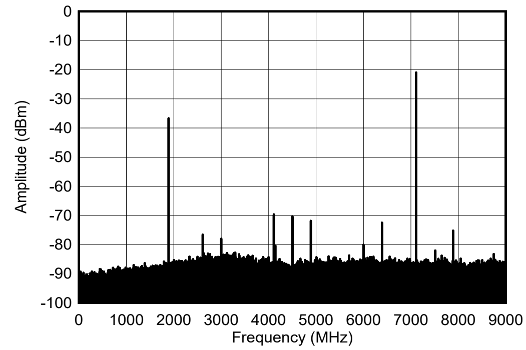


Figure 5-590. Single Tone Output Spectrum at 7.1 GHz, -12 dBFS (0 - F_{DAC})

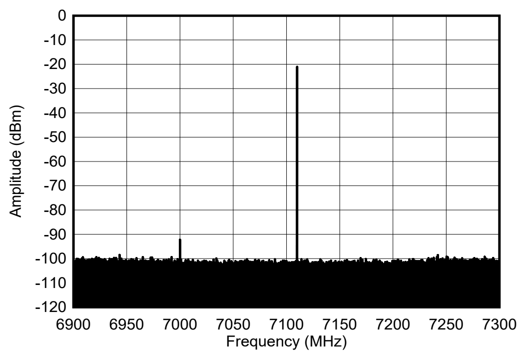
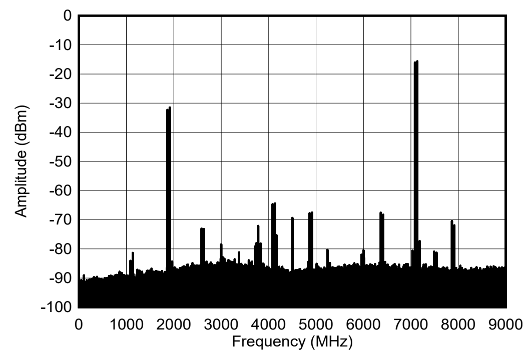
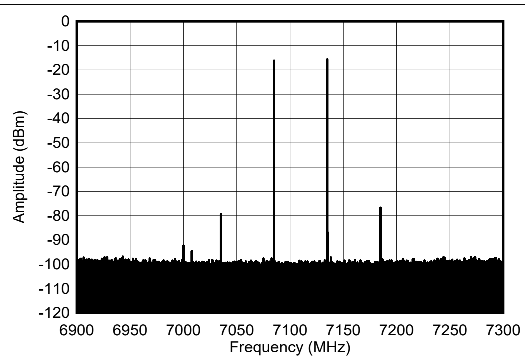


Figure 5-591. Single Tone Output Spectrum at 7.1 GHz, -12 dBFS (Inband)



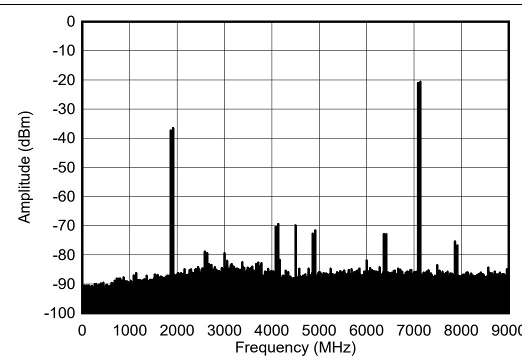
50MHz Tone Spacing

Figure 5-592. Two Tone Output Spectrum at 7.1 GHz, -7 dBFS each (0 - F_{DAC})



50MHz Tone Spacing

Figure 5-593. Two Tone Output Spectrum at 7.1 GHz, -7 dBFS each (Inband)

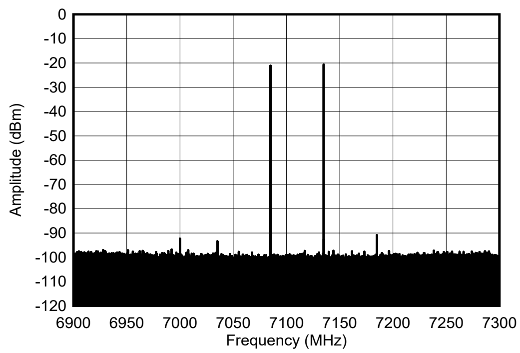


50 MHz Tone Spacing

Figure 5-594. Two Tone Output Spectrum at 7.1 GHz, -12 dBFS each (0 - F_{DAC})

5.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



50MHz Tone Spacing

Figure 5-595. Two Tone Output Spectrum at 7.1 GHz, -12 dBFS each (Inband)

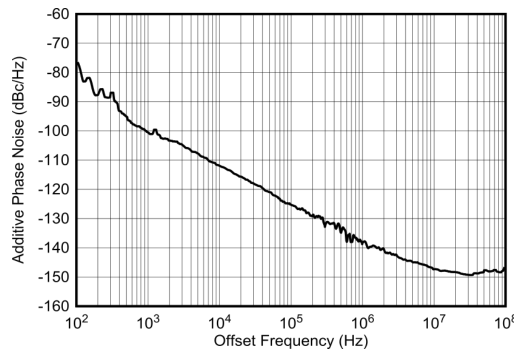
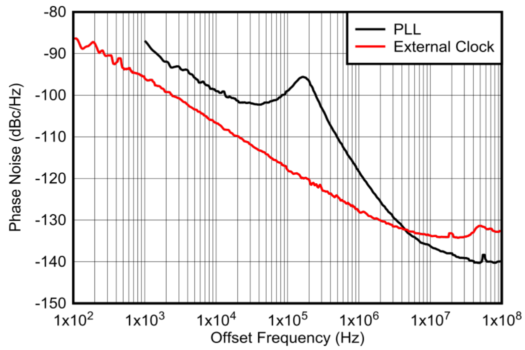


Figure 5-596. External Clock Additive Phase Noise at 7.1 GHz

5.12.15 PLL and Clock Typical Characteristics



measured at TX output, normalized to 12 GHz by 20 x log10(12 GHz/F_{OUT})

Figure 5-597. Phase Noise vs Offset Frequency for PLL and External Clock at 12 GHz

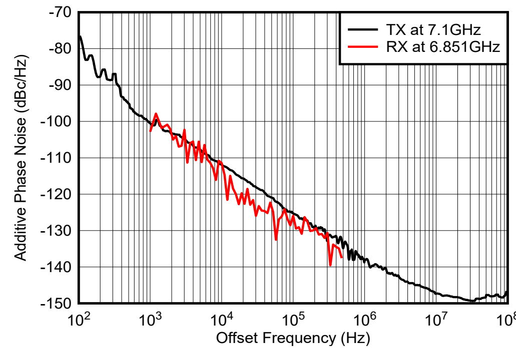
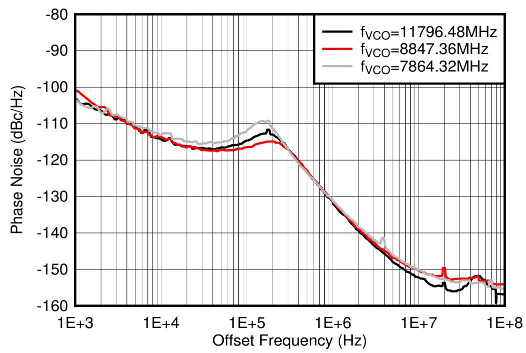
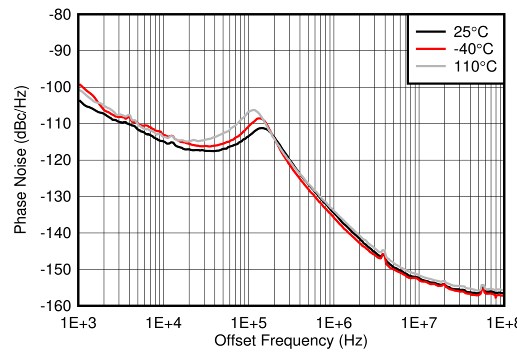


Figure 5-598. TX vs RX Additive Phase Noise at 7G Hz



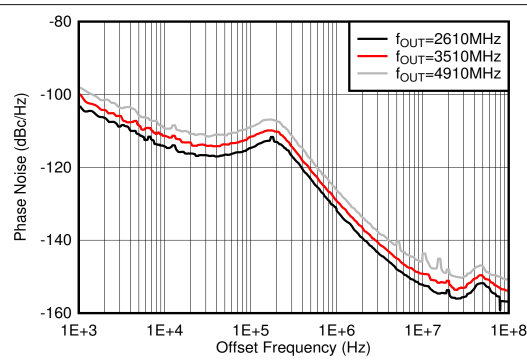
PLL enabled, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-599. Phase Noise vs Offset Frequency and f_{VCO} at f_{OUT} = 2610 MHz



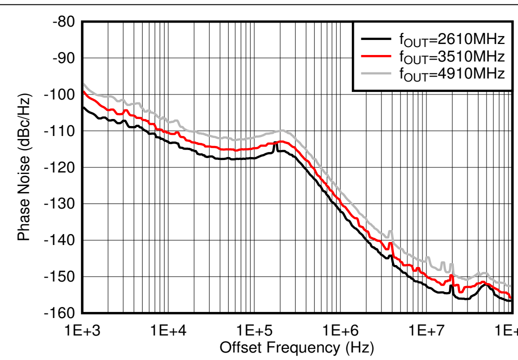
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-600. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



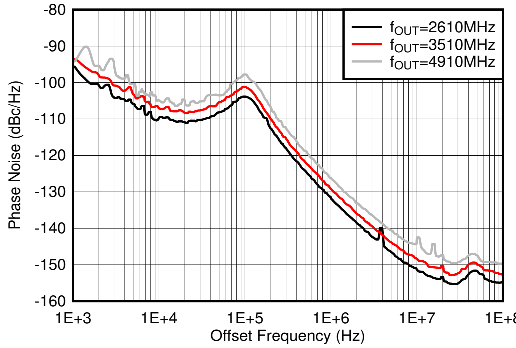
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-601. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



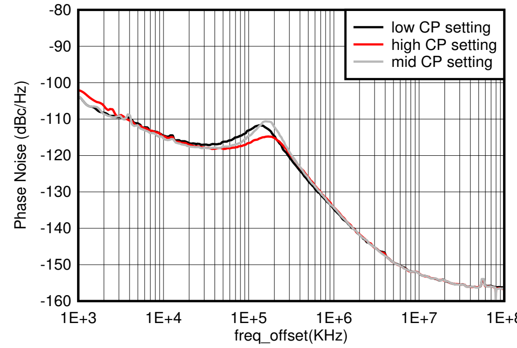
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-602. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



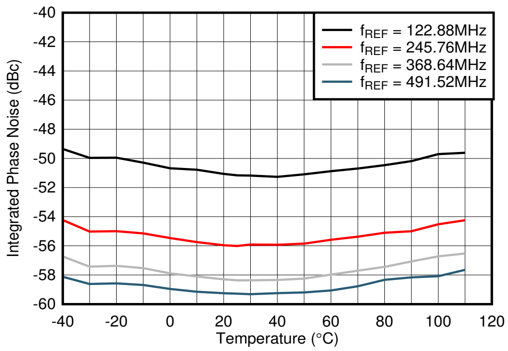
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-603. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



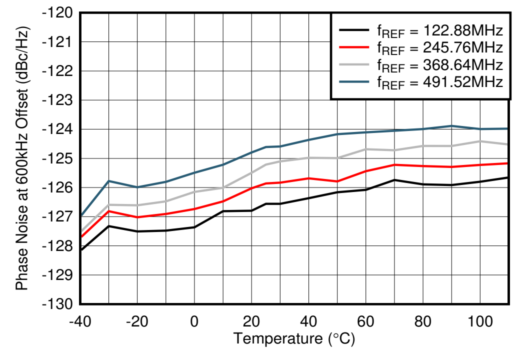
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-604. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at f_{OUT} = 2.6 GHz



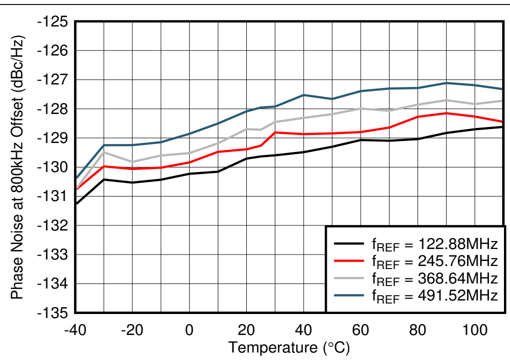
PLL enabled, f_{VCO} = 11796.48 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

Figure 5-605. Integrated Phase Noise for 12-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



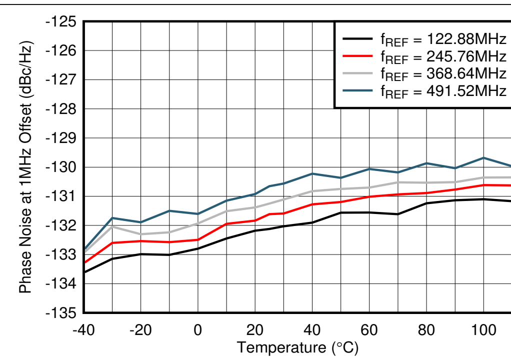
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 5-606. Phase Noise for 12-GHz VCO at 600 kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



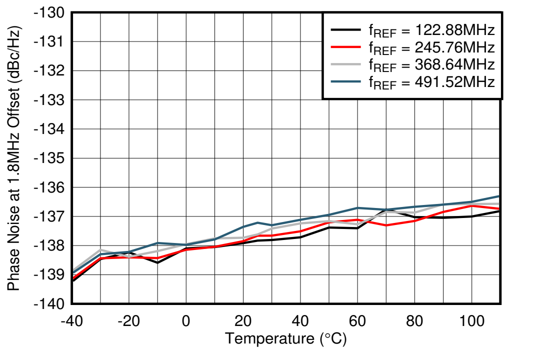
A. PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 5-607. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



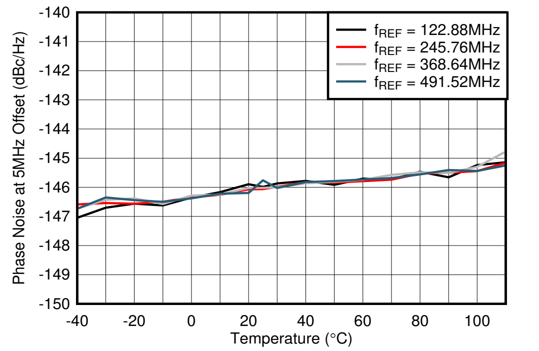
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 5-608. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



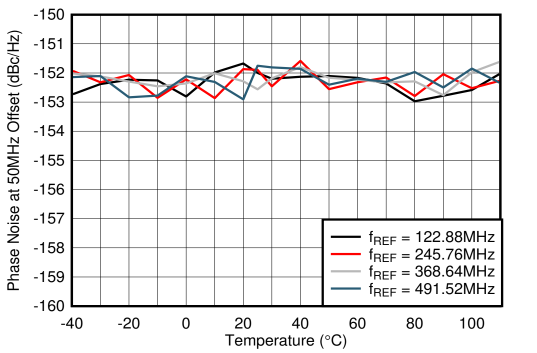
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 5-609. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



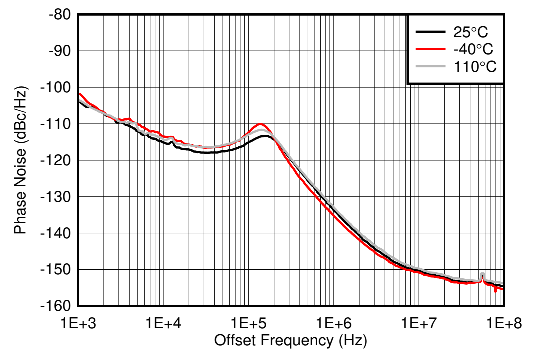
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 5-610. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



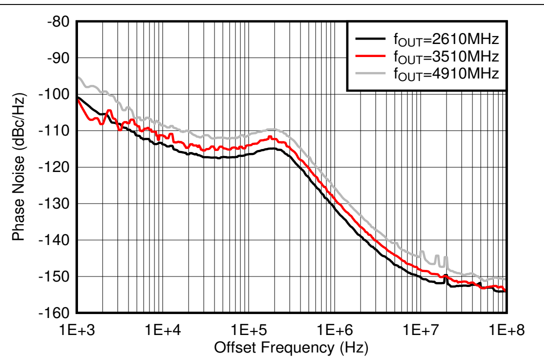
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 5-611. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



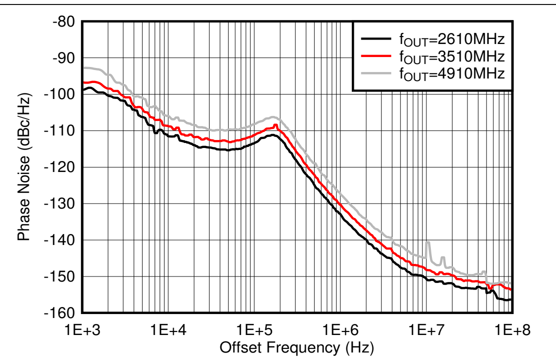
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-612. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



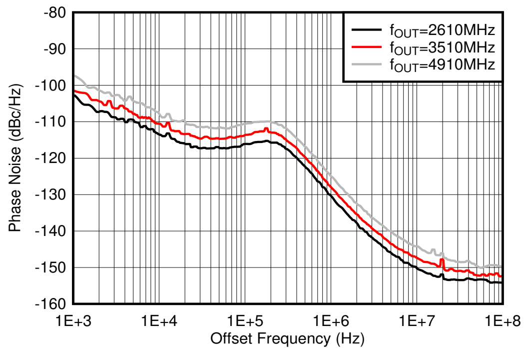
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-613. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



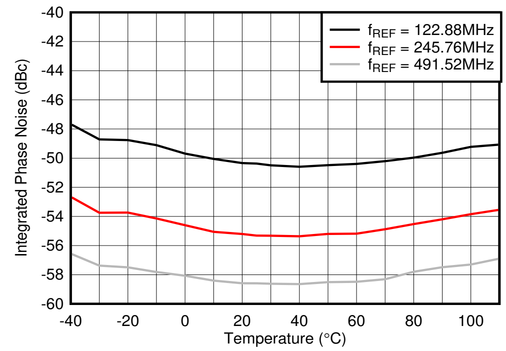
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-614. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



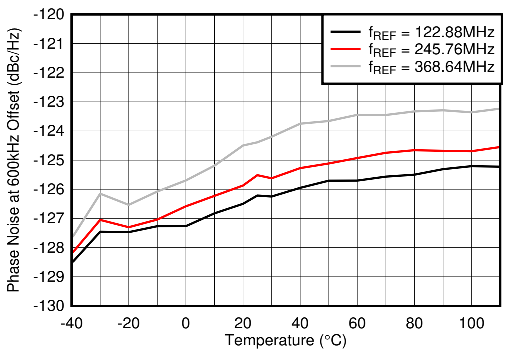
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-615. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



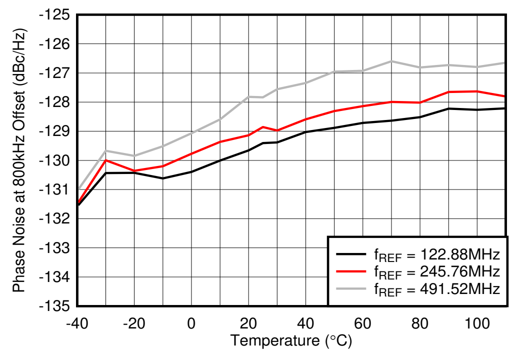
PLL enabled, f_{VCO} = 9830.4 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

Figure 5-616. Integrated Phase Noise for 10-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



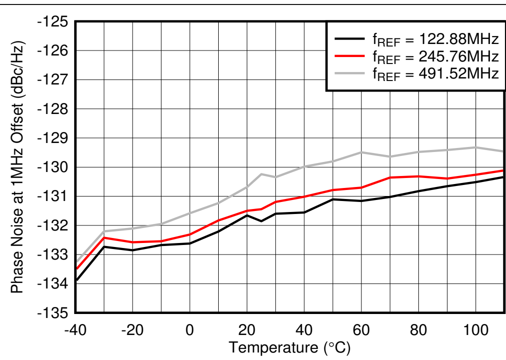
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 5-617. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



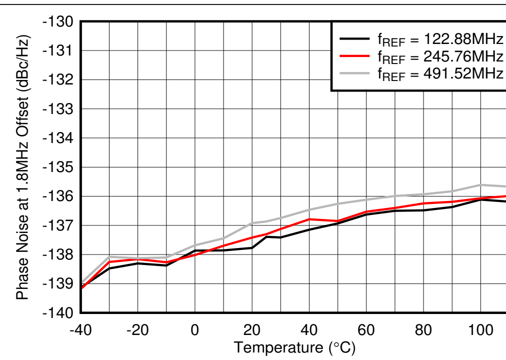
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 5-618. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



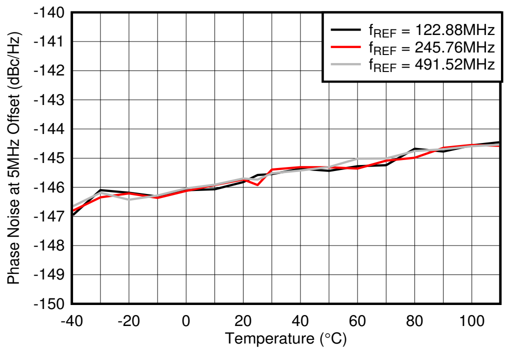
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 5-619. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



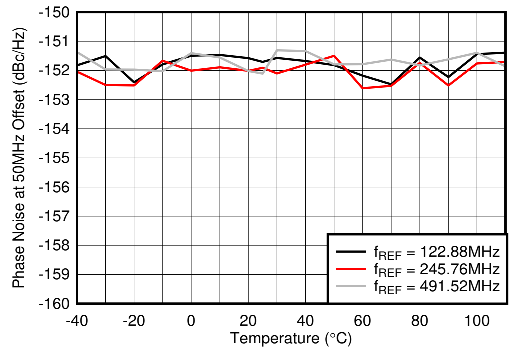
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 5-620. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



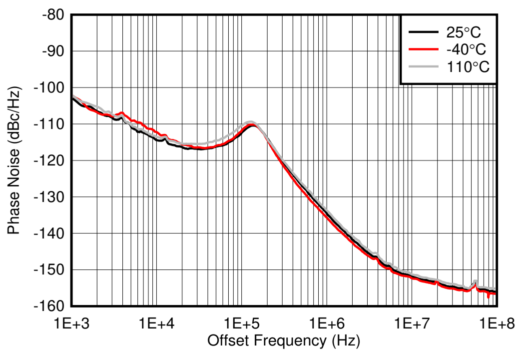
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 5-621. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



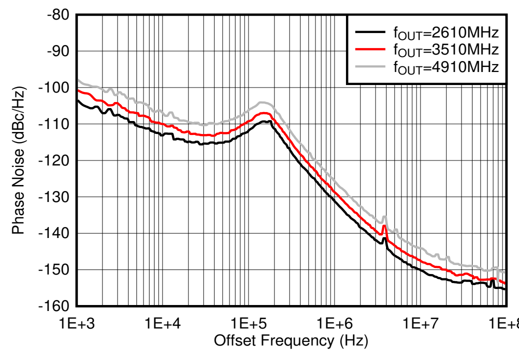
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 5-622. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



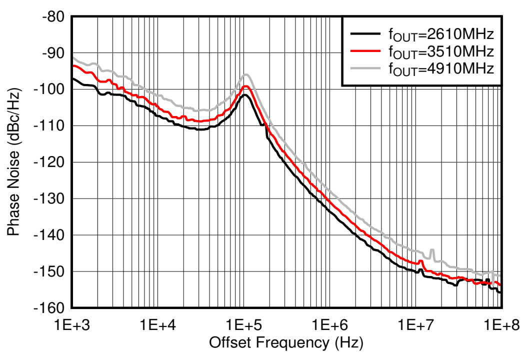
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-623. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



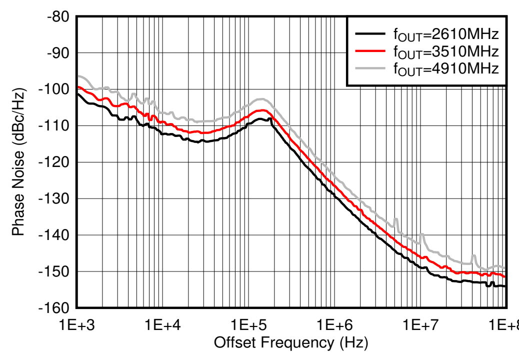
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-624. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



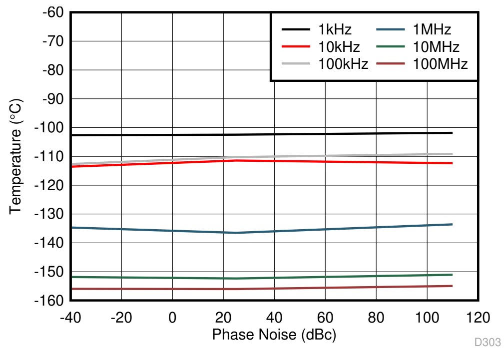
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-625. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



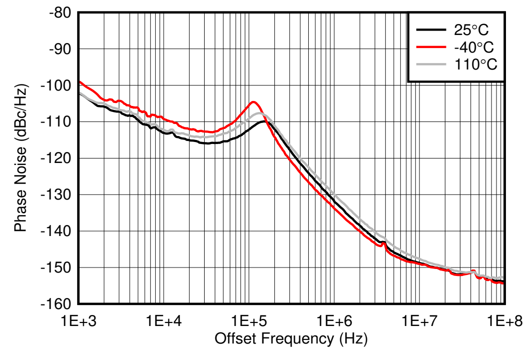
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-626. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52 MSPS, minimum LPF BW, measured at 2TXOUT

Figure 5-627. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 7864.32 MHz, f_{REF} = 491.52 MSPS, measured at 2TXOUT

Figure 5-628. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 14, 2023 to May 1, 2025 (from Revision A (June 2023) to Revision B (May 2025)) — **Page**

- RX Input Max Power moved from RF ADC Electrical Characteristics to Absolute Maximum Ratings............. 11

Changes from April 20, 2023 to June 13, 2023 (from Revision * (April 2023) to Revision A (June 2023)) — **Page**

- Added note 2 to the *Package Information* table... 1
- Deleted *TX Clock Dither Enabled* from all TX Typical Characteristics description...80
- Changed 1st Nyquist zone output to 2nd Nyquist zone output.. 142

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE7901IABJ	Active	Production	FCBGA (ABJ) | 400	90 | JEDEC TRAY (5+1)	Yes	SNAGCU | SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7901I
AFE7901IABJ.B	Active	Production	FCBGA (ABJ) | 400	1 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 85	
AFE7901IALK	Active	Production	FCBGA (ALK) | 400	90 | JEDEC TRAY (5+1)	No	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7901 SNPB
AFE7901IALK.B	Active	Production	FCBGA (ALK) | 400	90 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

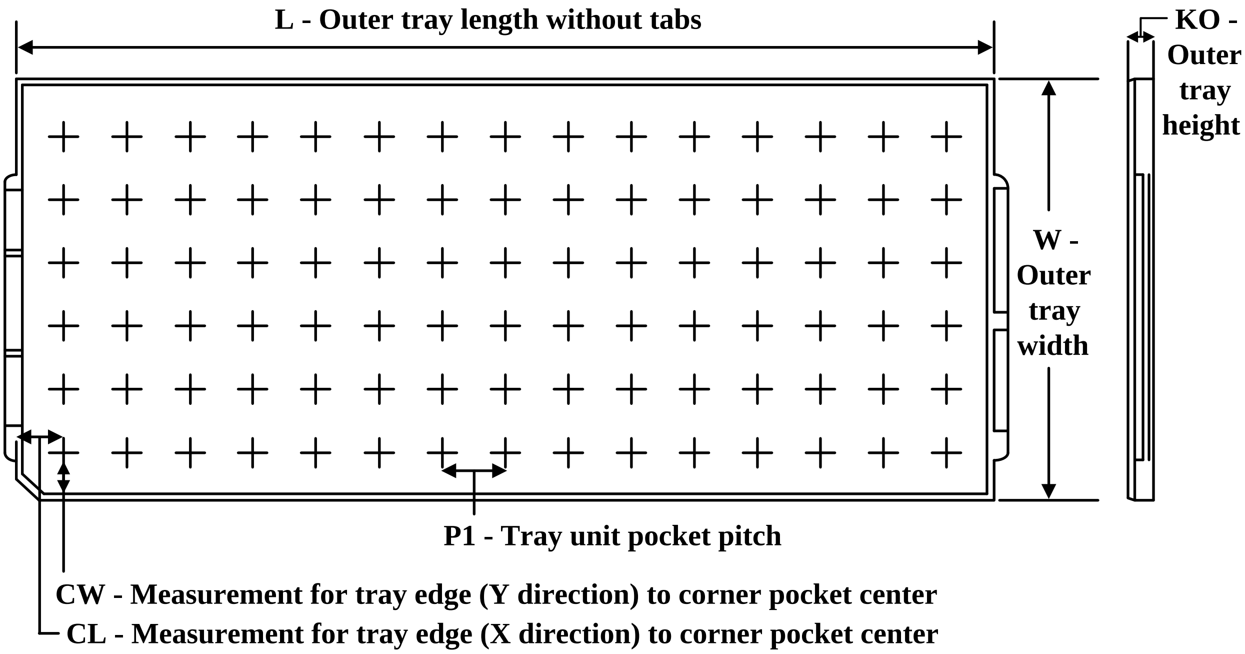
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

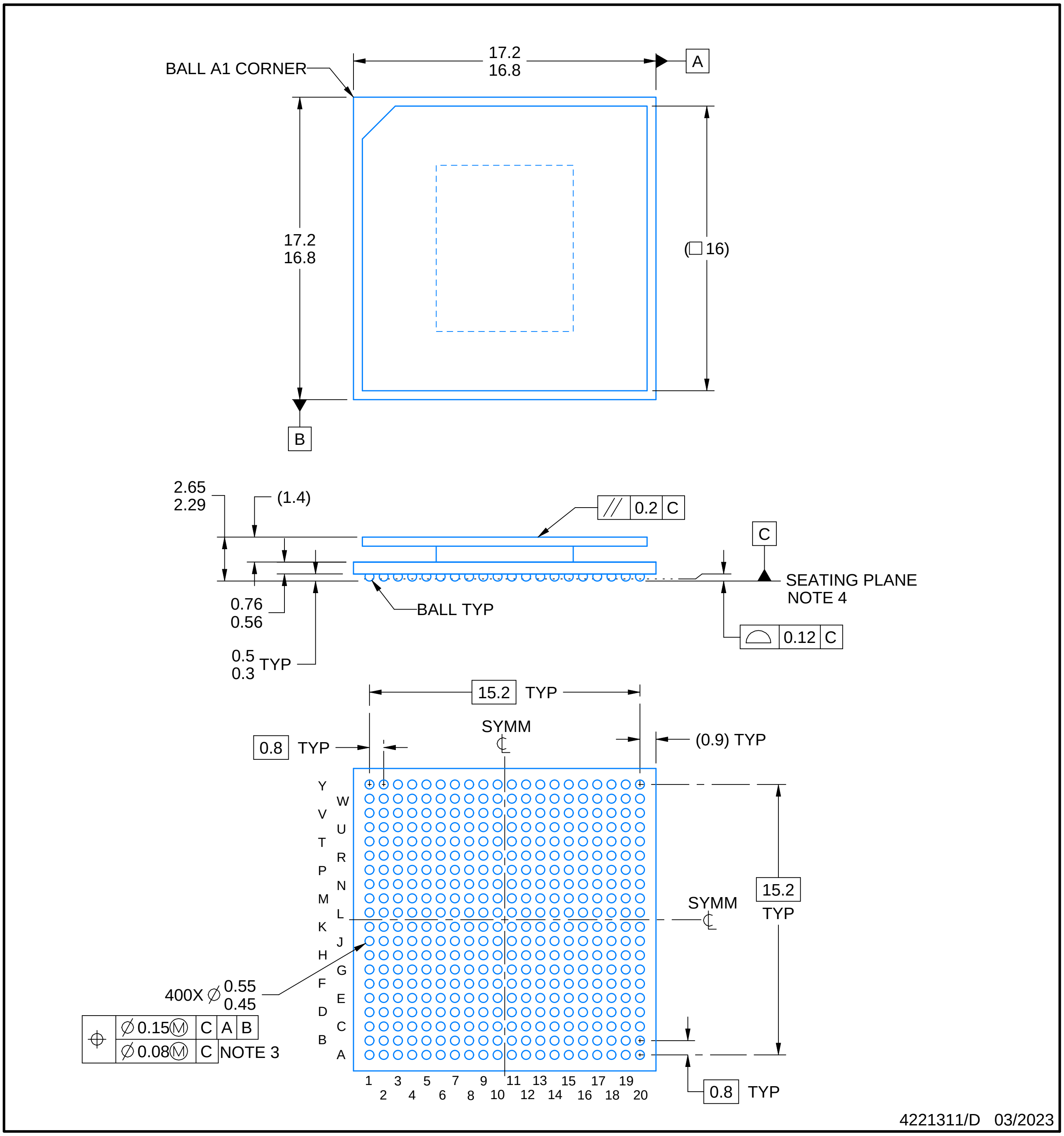
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

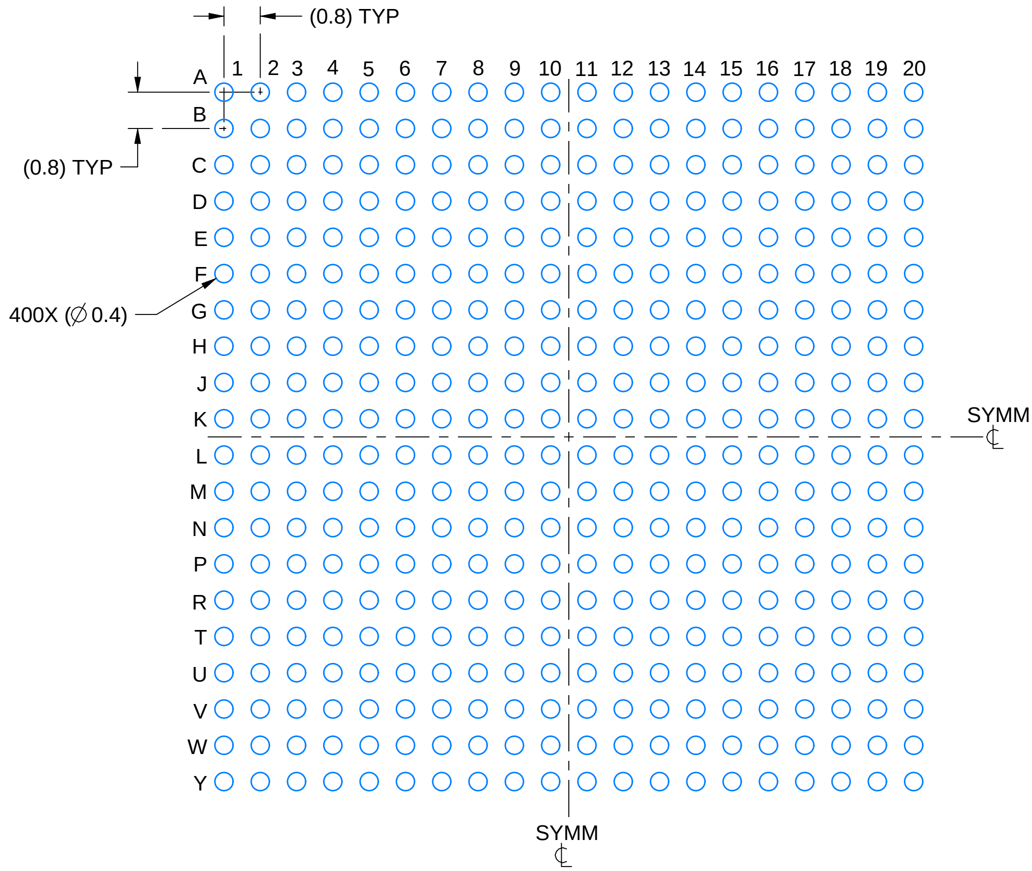
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE7901IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7901IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7901IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7901IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2

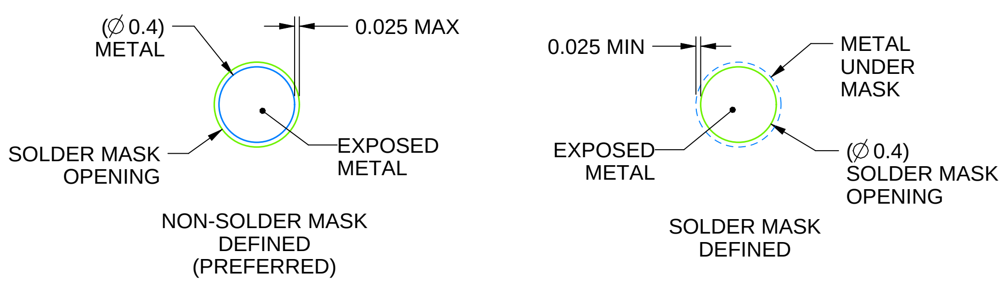


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

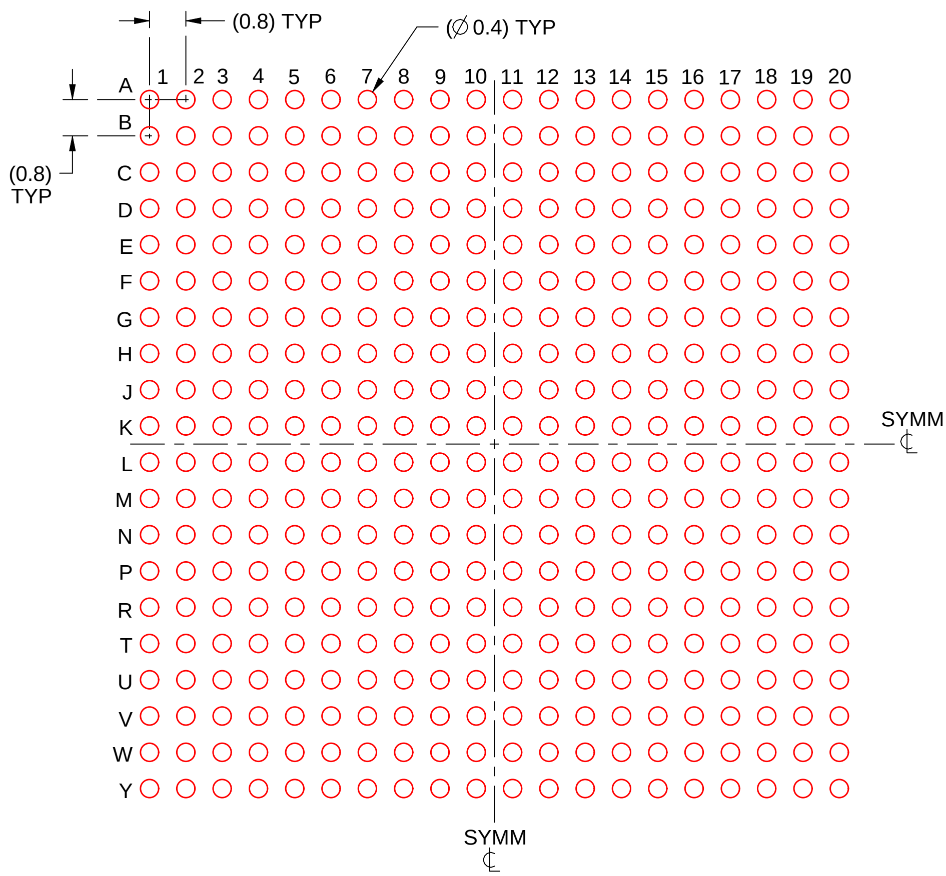


SOLDER MASK DETAILS
NOT TO SCALE

4221311/D 03/2023

NOTES: (continued)

6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

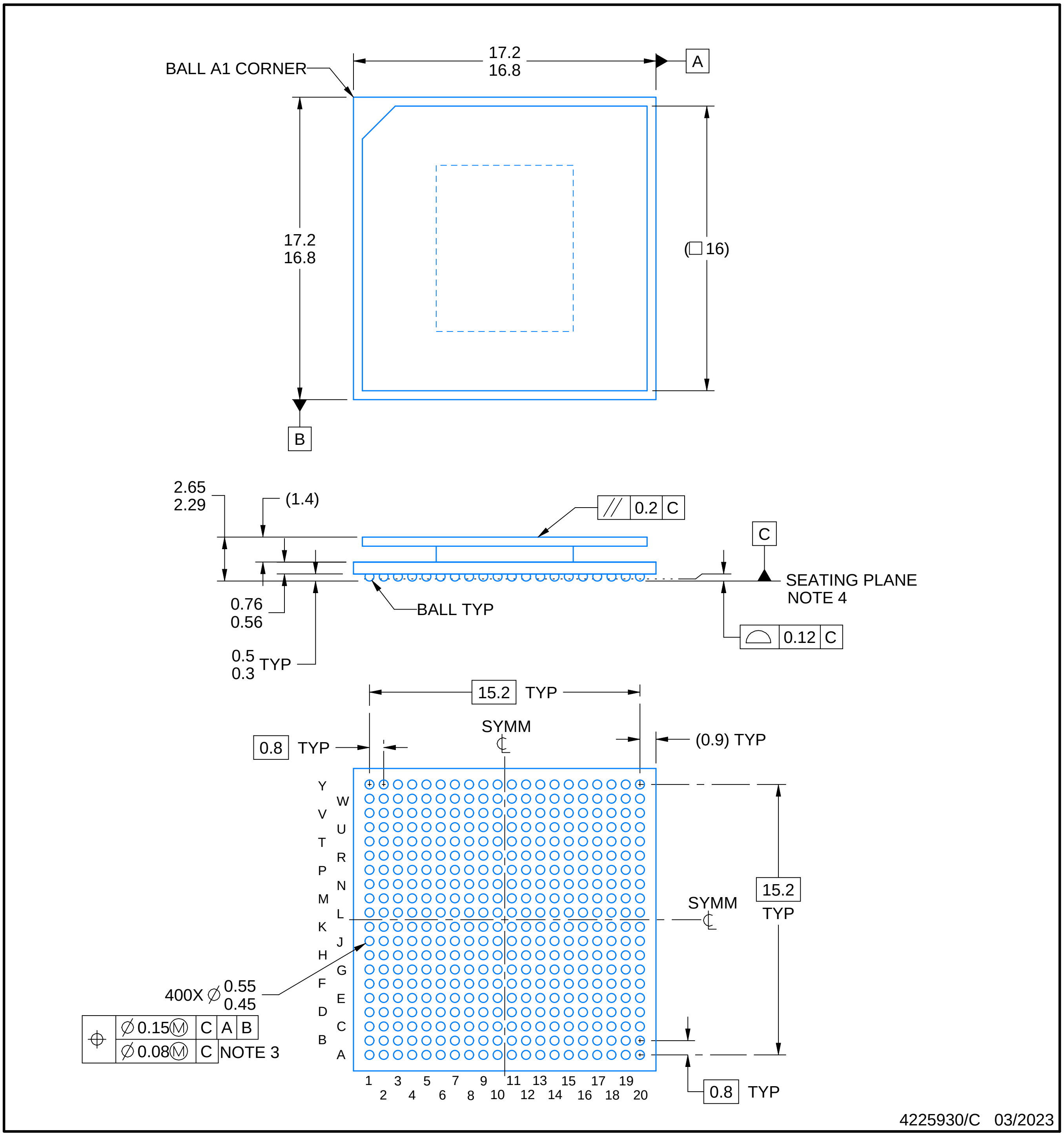


SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4221311/D 03/2023

NOTES: (continued)

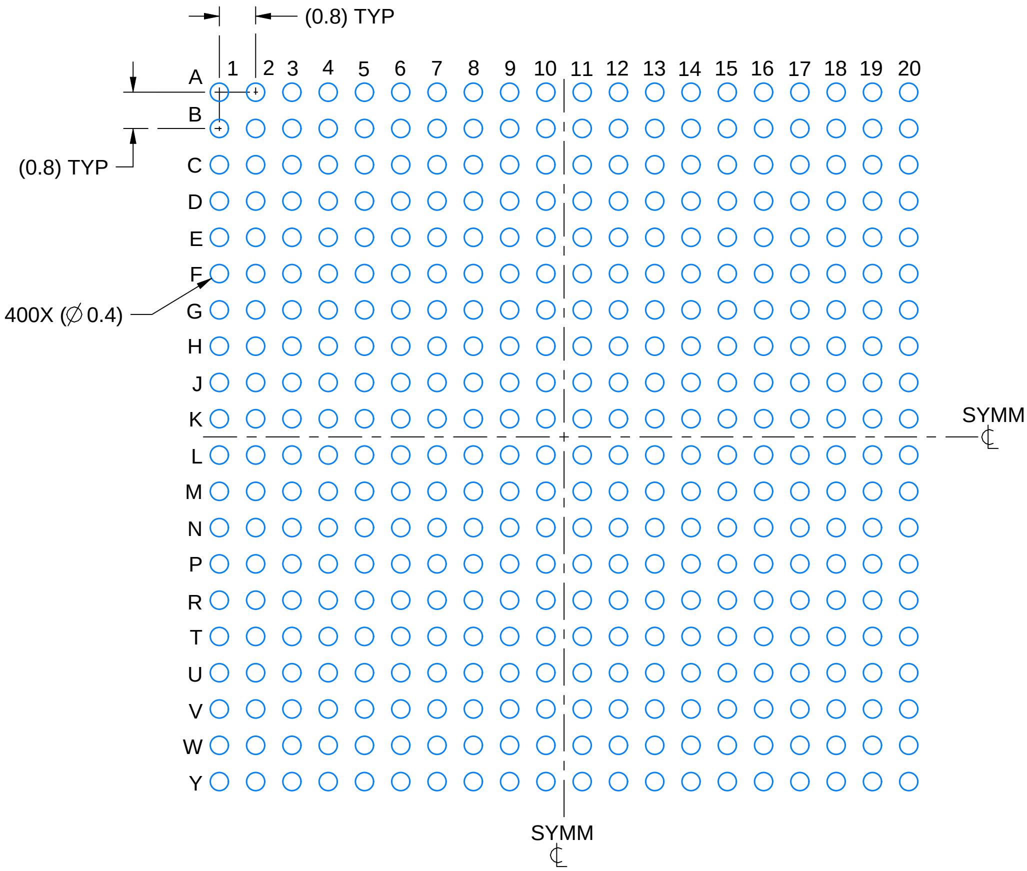
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



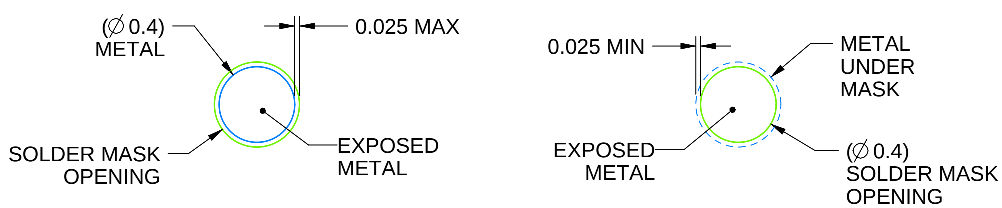
4225930/C 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON-SOLDER MASK DEFINED (PREFERRED)

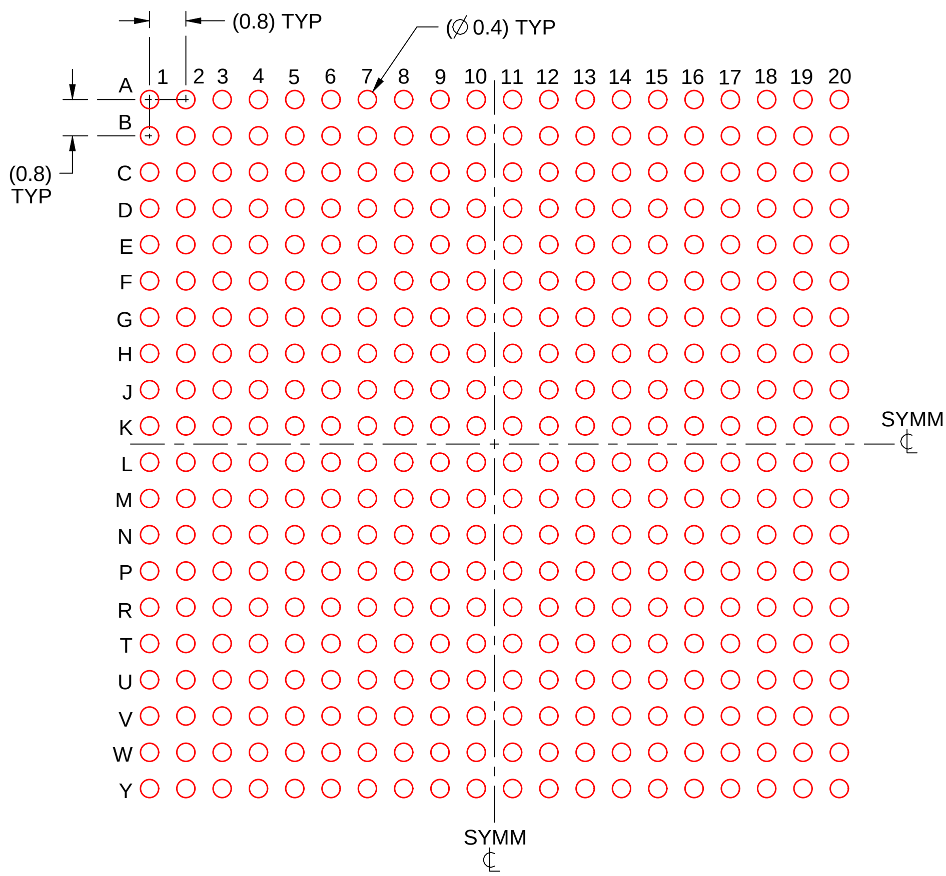
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

7. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.