AFE58JD18 16-Channel, Ultrasound AFE with 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, Passive CW Mixer, I/Q Demodulator, and LVDS, JESD204B Outputs

1 Features

- 16-Channel, Complete Analog Front-End (AFE):
  - LNA, VCAT, PGA, LPF, ADC, and CW Mixer
- LNA with Programmable Gain:
  - Gain: 24 dB, 18 dB, and 12 dB
  - Linear Input Range: 0.25 V_{PP}, 0.5 V_{PP}, and 1 V_{PP}
  - Input-Referred Noise: 0.63 nV/√Hz, 0.7 nV/√Hz, and 0.9 nV/√Hz
  - Programmable Active Termination
- Voltage-Controlled Attenuator (VCAT): 40 dB
- Programmable Gain Amplifier (PGA): 24 dB and 30 dB
- Total Signal Chain Gain: 54 dB (max)
- 3rd-Order, Linear-Phase LPF:
  - 10 MHz, 15 MHz, 20 MHz, 30 MHz, 35 MHz, and 50 MHz
- Analog-to-Digital Converter (ADC):
  - 14-Bit ADC: 75-dBFS SNR at 65 MSPS
  - 12-Bit ADC: 72-dBFS SNR at 80 MSPS
- LVDS Interface Maximum Speed of 1 Gbps
- Noise and Power Optimizations (Full-Channel):
  - 140 mW/Ch at 0.75 nV/√Hz, 65 MSPS
  - 91.5 mW/Ch at 1.1 nV/√Hz, 40 MSPS
  - 80 mW/Ch at CW Mode
- Excellent Device-to-Device Gain Matching:
  - ±0.5 dB (typical) and ±1.1 dB (max)
- Low Harmonic Distortion
- Fast and Consistent Overload Recovery
- Passive Mixer for CWD:
  - Low Close-In Phase Noise: –156 dBc/Hz at 1 kHz Off 2.5-MHz Carrier
  - Phase Resolution: λ / 16
  - Supports 16X, 8X, 4X, and 1X CW Clocks
  - CWD High-Pass Filter Rejects Undesired Low-Frequency Signals < 1 kHz
- Digital Features:
  - Digital I/Q Demodulator after ADC:
    - Fractional Decimation Filter M = 1 to 63 with 0.25X Increment Step
    - Data Throughput Reduction After Decimation
    - On-Chip RAM with 32 Preset Profiles
- 5-Gbps JESD Interface:
  - JESD204B Subclass 0, 1, and 2
  - 2, 4, or 8 Channels per JESD Lane
- Small Package: 15-mm × 15-mm NFBGA-289

2 Applications

- Medical Ultrasound Imaging
- Nondestructive Evaluation Equipment
- Sonar Imaging Equipment

3 Description

The AFE58JD18 is a highly-integrated, analog front-end (AFE) solutions specifically designed for ultrasound systems where high performance and small size are required.

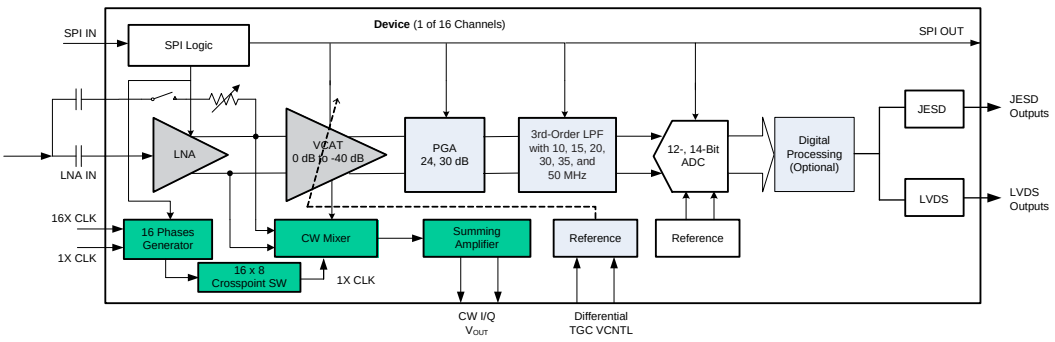
To request a full datasheet or other design resources: request AFE58JD18

Device Information(1)

PART NUMBER	OUTPUT INTERFACE	DIGITAL I/Q DEMODULATOR
AFE58JD18	LVDS and JESD	Supported

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2015) to Revision A	Page
• Added link to request full data sheet	1

5 Description (continued)

The AFE58JD18 has a total of 16 channels, with each channel consisting of a voltage-controlled amplifier (VCA), a simultaneous sampling 14-bit and 12-bit analog-to-digital converter (ADC), and a continuous wave (CW) mixer. The VCA includes a low-noise amplifier (LNA), a voltage-controlled attenuator (VCAT), a programmable gain amplifier (PGA), and a low-pass filter (LPF). LNA gain is programmable and supports 250-mV_{PP} to 1-V_{PP} input signals and programmable active termination. The ultra-low noise VCAT provides an attenuation control range of 40 dB and improves overall low-gain SNR, which benefits harmonic and near-field imaging. The PGA provides gain options of 24 dB and 30 dB. In front of the ADC, an LPF can be configured at 10 MHz, 15 MHz, 20 MHz, 30 MHz, 35 MHz, or 50 MHz to support ultrasound applications with different frequencies.

The AFE58JD18 also integrates a low-power passive mixer and a low-noise summing amplifier to create an on-chip CWD beamformer. 16 selectable phase delays can be applied to each analog input signal. Furthermore, a unique third- and fifth-order harmonic suppression filter is implemented to enhance CW sensitivity

The high-performance, 14-bit ADC achieves 75-dBFS SNR. This ADC ensures excellent SNR at low-chain gain. The device can operate at maximum speeds of 65 MSPS and 80 MSPS, providing a 14-bit and a 12-bit output, respectively.

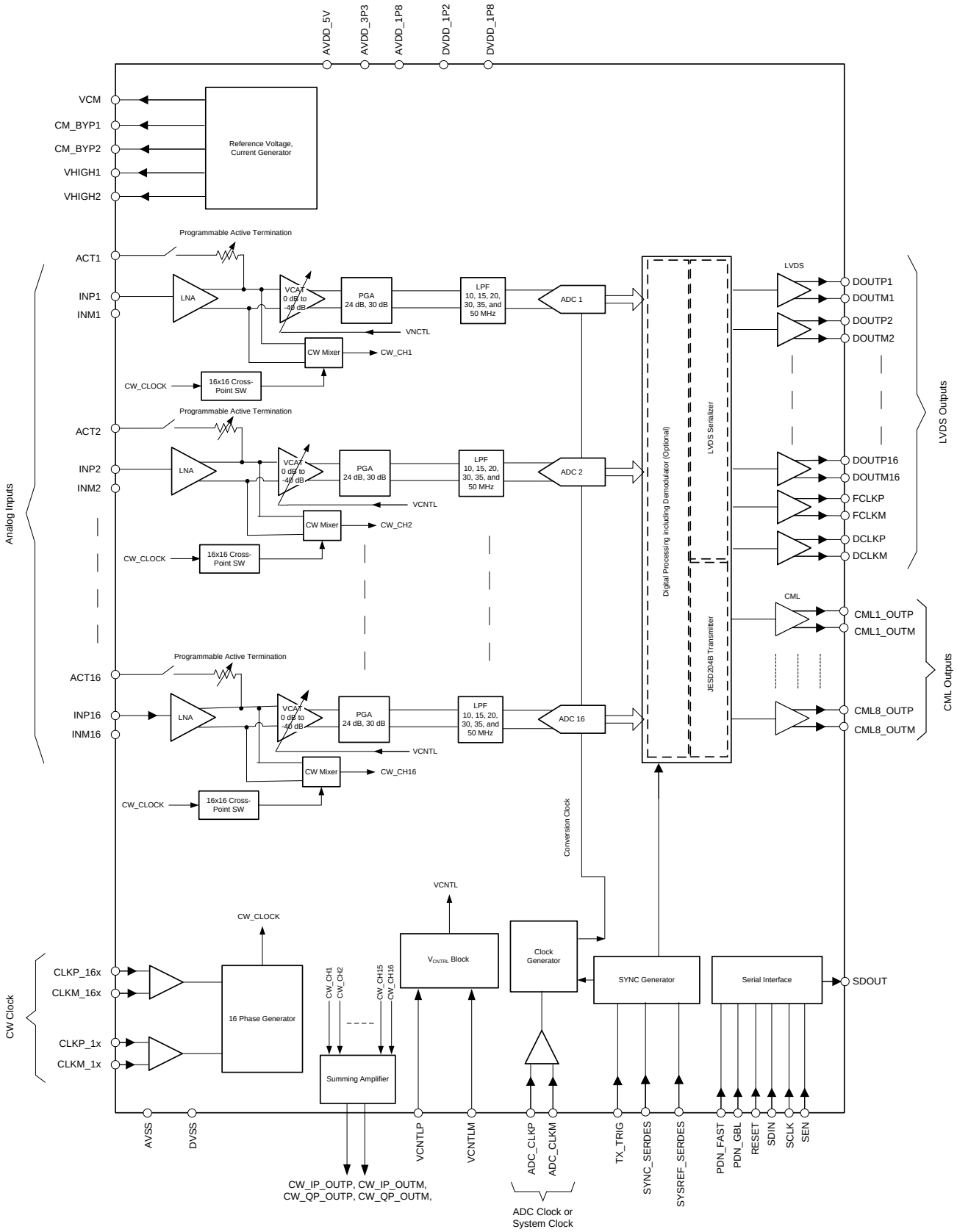
The ADC low-voltage differential signaling (LVDS) outputs enable a flexible system integration that is desirable for miniaturized systems.

The AFE58JD18 additionally includes an optional digital demodulator and JESD204B data packing blocks after the 12- or 14-bit ADC. The digital in-phase and quadrature (I/Q) demodulator with programmable fractional decimation filters accelerates computationally-intensive algorithms at low power. A JESD204B interface that runs up to 5 Gbps further reduces the circuit board routing challenges in high-channel count systems.

The AFE58JD18 also allows various power and noise combinations to be selected to optimize system performance. Therefore, the AFE58JD18 is a suitable ultrasound AFE solution for both high-end and portable systems.

The AFE58JD18 is available in a 15-mm × 15-mm NFBGA-289 package (ZBV package, S-PBGA-N289) and is specified for operation from –40°C to 85°C. The device pinout is also similar to the AFE5816 device family.

6 Functional Block Diagram



7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

AFE5816 Data Sheet, SBAS688

MicroStar BGA Packaging Reference Guide, SSYZ015

Clocking High-Speed Data Converters, SLYT075

Design for a Wideband Differential Transimpedance DAC Output, SBAA150

TI Active Filter Design Tool, WEBENCH® Filter Designer

CDCM7005 Data Sheet, SCAS793

CDCE72010 Data Sheet, SCAS858

TLV5626 Data Sheet, SLAS236

DAC7821 Data Sheet, SBAS365

THS413x Data Sheet, SLOS318

OPA1632 Data Sheet, SBOS286

LMK048x Data Sheet, SNAS489

OPA2211 Data Sheet, SBOS377

ADS8413 Data Sheet, SLAS490

ADS8472 Data Sheet, SLAS514

ADS8881 Data Sheet, SBAS547

SN74AUP1T04 Data Sheet, SCES800

UCC28250 Data Sheet,SLUSA29

ISO7240 Data Sheet, SLLS868

7.2 Trademarks

All trademarks are the property of their respective owners.

7.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

7.4 Export Control Notice

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7.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

8.1 Tray Information

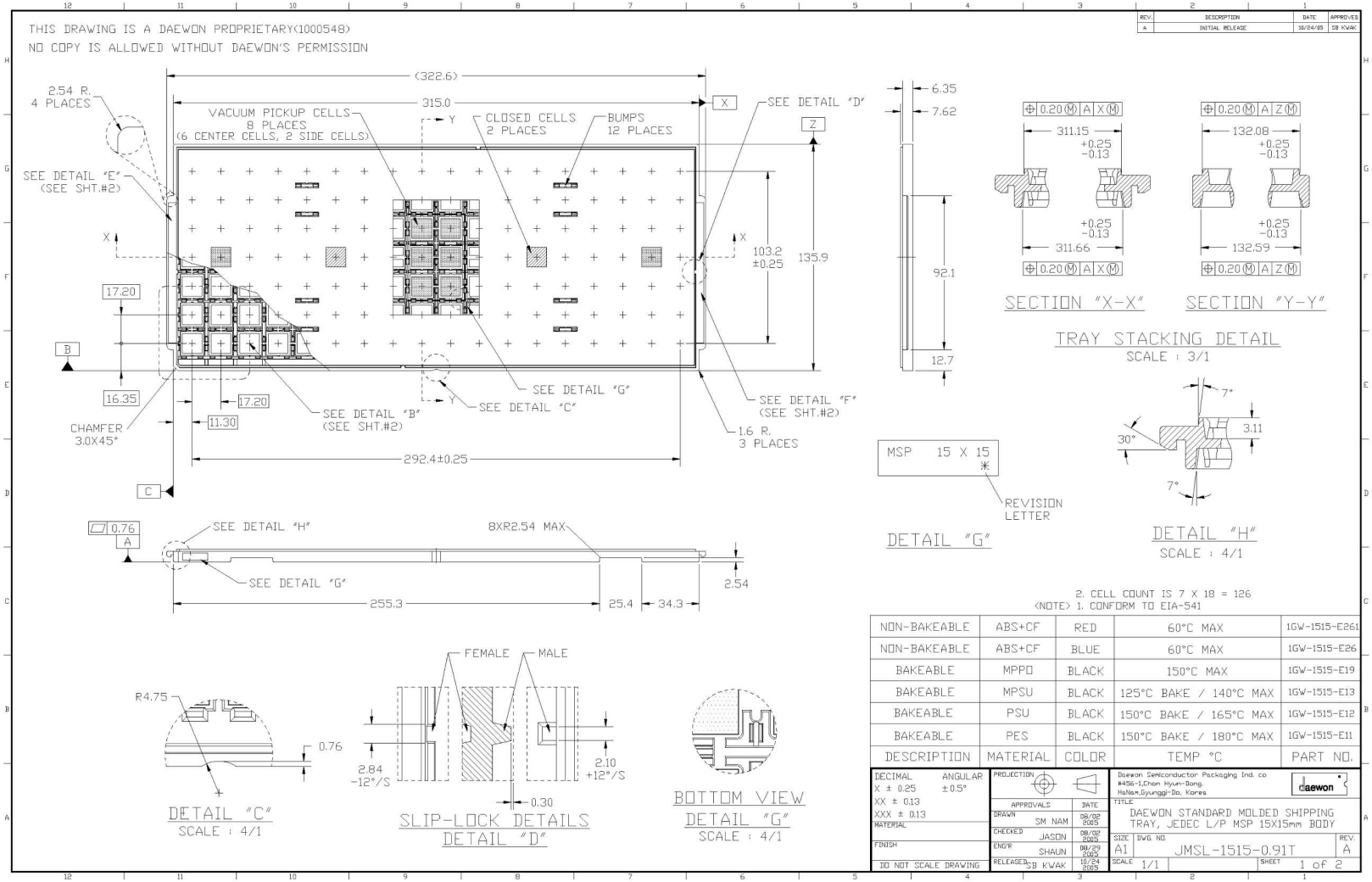


Figure 1. Tray Diagram, Section 1

Tray Information (continued)

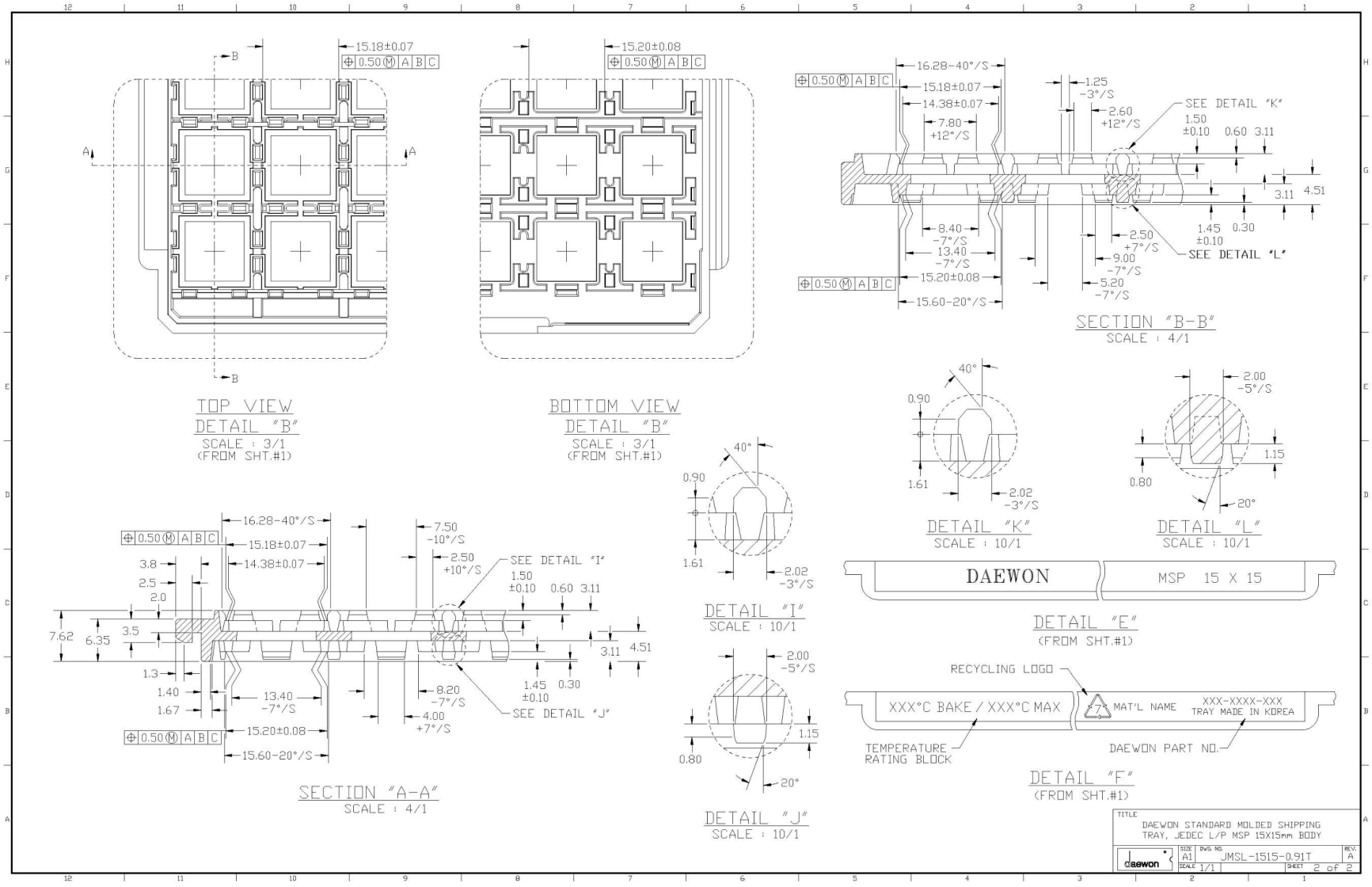


Figure 2. Tray Diagram, Section 2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE58JD18ZBV	Active	Production	NFBGA (ZBV) | 289	126 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE58JD18
AFE58JD18ZBV.A	Active	Production	NFBGA (ZBV) | 289	126 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE58JD18
AFE58JD18ZBV.B	Active	Production	NFBGA (ZBV) | 289	126 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE58JD18

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

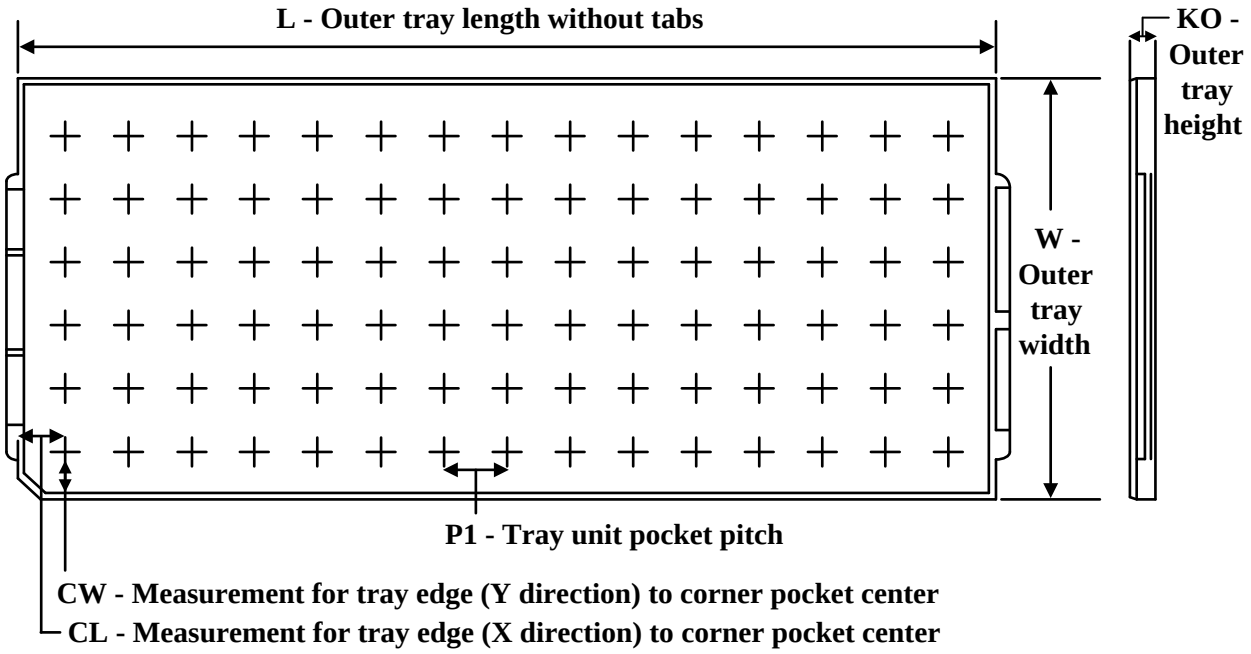
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY

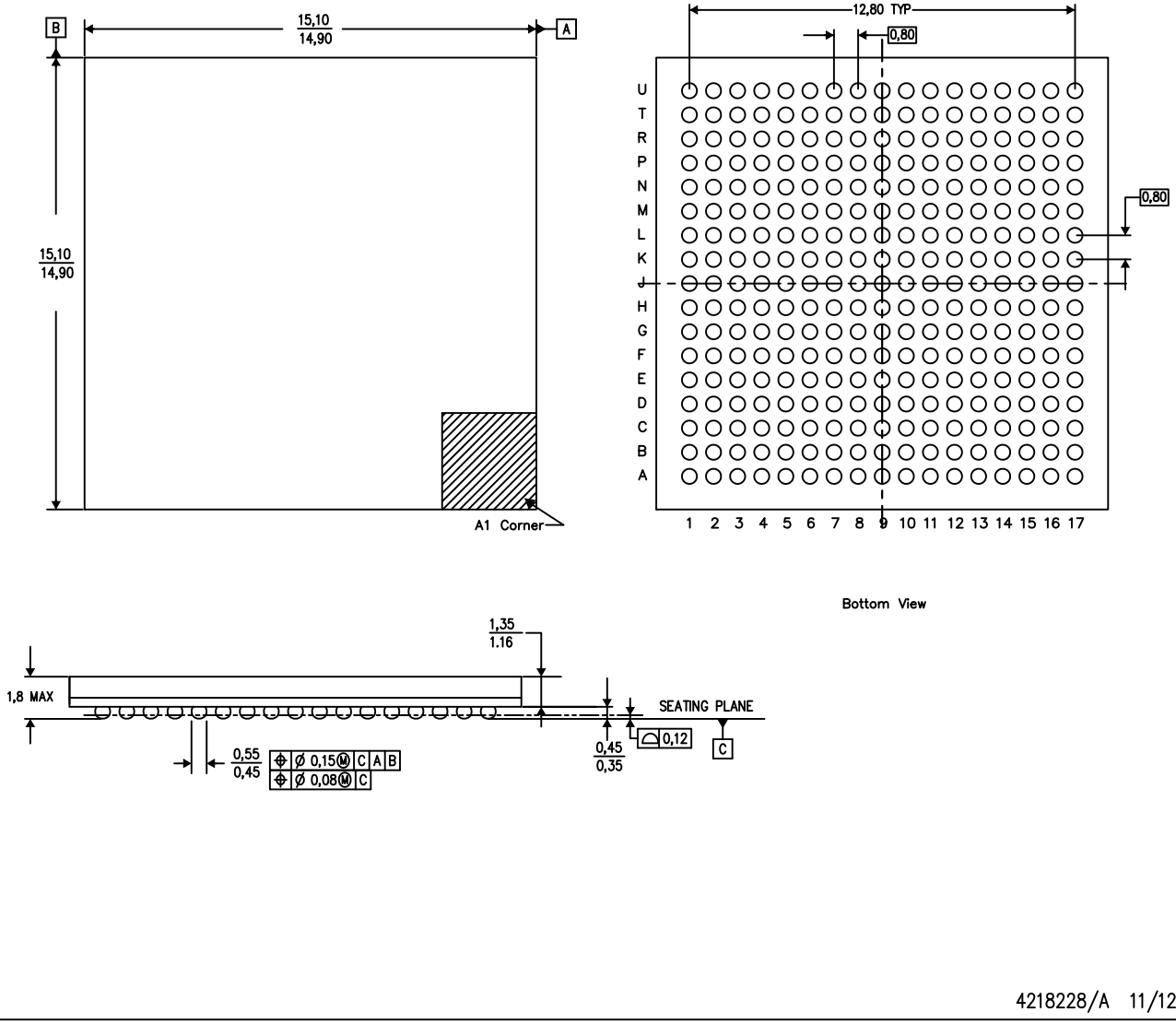


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE58JD18ZBV	ZBV	NFBGA	289	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35
AFE58JD18ZBV.A	ZBV	NFBGA	289	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35
AFE58JD18ZBV.B	ZBV	NFBGA	289	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35

ZBV (S–PBGA–N289) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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