AFEx39xx 12-Bit, 10-Bit, and 8-Bit Smart Analog Front Ends for TEC Control Using Voltage and PWM Output

1 Features

- Integrated proportional-integral (PI) control
  - Standalone operation from nonvolatile memory (NVM)
  - Programmable proportional and integral gain
  - Comparator input for output clamping
  - Programmable min, max, and common-mode values for output
  - Programmable loop-phase inversion
- AFE639D2
  - I^2C controller for external digital temperature sensor interface
  - 12-bit DAC output: 4-LSB DNL, 1-LSB DNL
- AFE539A4
  - 10-bit ADC input: 2-LSB INL, 1-LSB DNL
  - 10-bit DAC output: 1-LSB INL and DNL
- AFE439A2
  - 8-bit ADC input: 1-LSB INL and DNL
  - 7-bit duty-cycle PWM output
- Programmable comparator for fault management
- High impedance output on DAC channel when VDD is off
- Automatically detects I^2C or SPI
  - 1.62-V V_{IH} with V_{DD} = 5.5 V
- VREF/MODE pin selects between programming and standalone modes
- User-programmable NVM
- Internal, external, or power supply as reference
- Wide operating range
  - Power supply: 1.8 V to 5.5 V
  - Temperature range: –40˚C to +125˚C
- Tiny package: 16-pin WQFN (3 mm × 3 mm)

2 Applications

- Laser
- Chemistry and gas analyzer
- Mechanically scanning LIDAR
- Robot sensing module
- Mobile robot sensing module
- Seeker front end

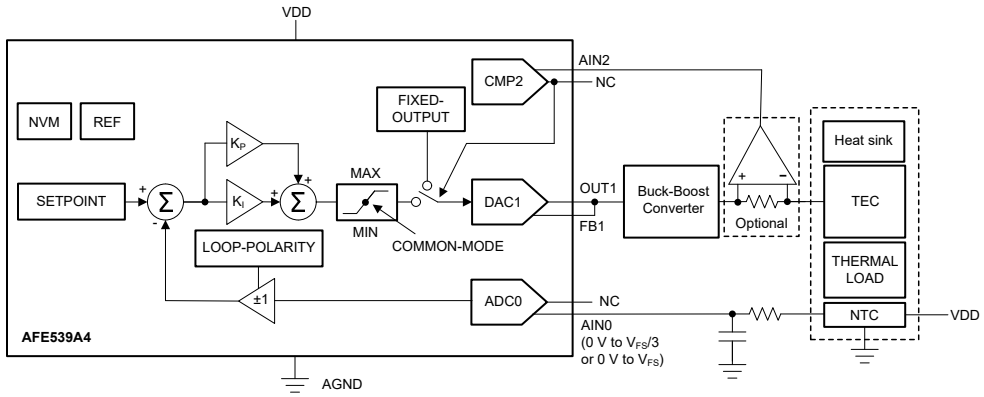
3 Description

The 8-bit AFE439A2, 10-bit AFE539A4, and 12-bit AFE639D2 (AFEx39xx) are smart analog front ends (AFE) for thermoelectric cooling (TEC) control using voltage or PWM output. The AFE639D2 supports an I^2C controller interface to interface with external digital temperature sensors. The AFE639D2 and AFE539A4 support voltage output and AFE439A2 supports PWM output. The AFEx39xx support a comparator channel for fault management. These devices also support Hi-Z power-down mode and Hi-Z output on the DAC channel during power off. These devices have an integrated state machine that is preprogrammed as a proportional-integral (PI) controller. The AFEx39xx are an excellent choice for TEC control, temperature control, and dynamic headroom control applications. The AFEx39xx integrate advanced features, internal reference, and NVM that enable this smart AFE for *processor-less* applications and design reuse.

Device Information

PART NUMBER	RESOLUTION	PACKAGE(1)
AFE439A2	8-bit	WQFN (16)
AFE539A4	10-bit	
AFE639D2	12-bit	

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Thermoelectric Cooling (TEC) Control Using the AFE539A4

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2021) to Revision A (June 2023)	Page
• Changed device data sheet status from advanced information (preview) to production data (active)	1

5 Pin Configuration and Functions

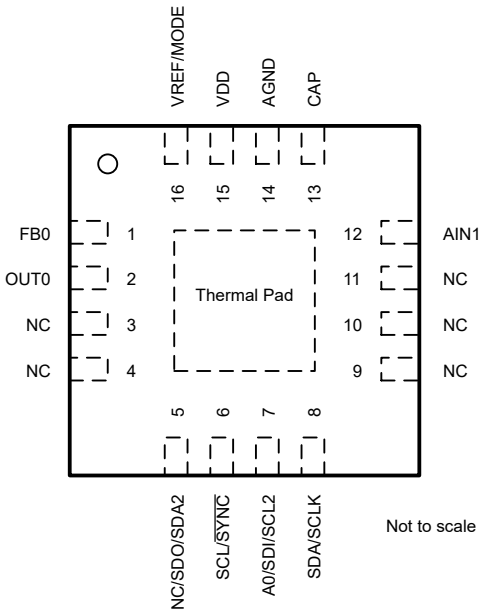


Figure 5-1. AFE639D2: RTE Package, 16-pin WQFN (Top View)

Table 5-1. Pin Functions: AFE639D2

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	FB0	Input	Voltage feedback input for DAC channel 0. Connect this pin to OUT0 for closed-loop amplifier output.
2	OUT0	Output	Analog output for DAC channel 0.
3	NC	—	Not connected.
4	NC	—	Not connected.
5	NC/SDO/ SDA2	Input/Output	*Target mode*: This pin can be configured as SDO or left unconnected. For SDO function, connect this pin to the IO voltage with an external pullup resistor. *Controller mode*: Bidirectional I^2C serial data bus.
6	SCL/$\overline{\text{SYNC}}$	Input	*Target mode*: I^2C serial interface clock or SPI chip select input. Connect this pin to the IO voltage using an external pullup resistor.
7	A0/SDI/SCL2	Input/Output	*Target mode*: Address configuration input in I^2C target mode or serial data input for SPI. In A0 function, connect this pin to VDD, AGND, SDA, or SCL for address configuration. In SDI function, this pin does not need termination. *Controller mode*: I^2C serial interface clock output.
8	SDA/SCLK	Input/Output	*Target mode*: Bidirectional I^2C serial data bus or SPI clock input. Connect this pin to the IO voltage using an external pullup resistor.
9	NC	—	Not connected.
10	NC	—	Not connected.
11	NC	—	Not connected.
12	AIN1	Input	Analog input for comparator.
13	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 µF) between CAP and AGND.
14	AGND	Ground	Ground reference point for all circuitry on the device.
15	VDD	Power	Supply voltage: 1.8 V to 5.5 V.
16	VREF/MODE	Input	External reference or interface mode select input. Connect a capacitor (approximately 0.1 µF) between VREF/MODE and AGND. Use a pullup resistor to VDD when the external reference is not used. In case an external reference is used or when in interface select mode, make sure the reference ramps up after VDD. In interface select mode: Pull this pin low to enable I^2C target or SPI communication. Pull this pin high to enable I^2C controller mode.
—	Thermal Pad	Ground	Connect the thermal pad to AGND.

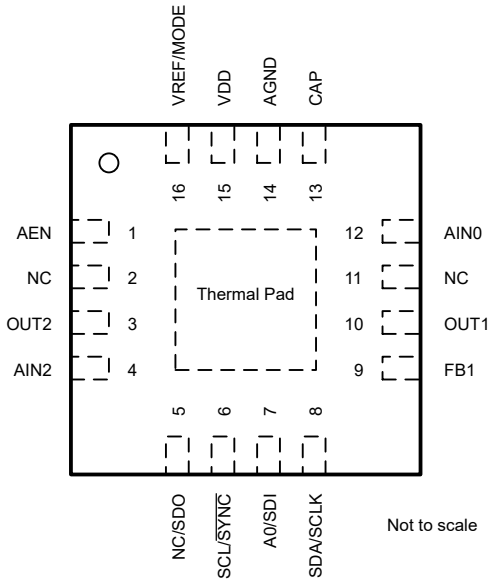


Figure 5-2. AFE539A4: RTE Package, 16-pin WQFN (Top View)

Table 5-2. Pin Functions: AFE539A4

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AEN	Input	ADC hardware enable pin. Connect this pin to VDD with a pullup resistor.
2	NC	—	Not connected.
3	NC	—	Not connected.
4	AIN2	Input	Analog input to the comparator. When unused, pull this pin to VDD or AGND.
5	NC/SDO	Output	This pin can be configured as SDO or left unconnected. For SDO function, connect this pin to the IO voltage with an external pullup resistor.
6	SCL/$\overline{\text{SYNC}}$	Input	I^2C serial interface clock or SPI chip select input. Connect this pin to the IO voltage using an external pullup resistor.
7	A0/SDI	Input	Address configuration input for I^2C or serial data input for SPI. In A0 function, connect this pin to VDD, AGND, SDA, or SCL for address configuration. In SDI function, this pin does not need termination.
8	SDA/SCLK	Input/Output	Bidirectional I^2C serial data bus or SPI clock input. Connect this pin to the IO voltage using an external pullup resistor.
9	FB1	Input	Voltage feedback input for DAC channel 1. Connect this pin to OUT1 for closed-loop amplifier output.
10	OUT1	Output	Analog output for DAC channel 1.
11	NC	—	Not connected.
12	AIN0	Input	Analog input for ADC channel 0.
13	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 µF) between CAP and AGND.
14	AGND	Ground	Ground reference point for all circuitry on the device.
15	VDD	Power	Supply voltage: 1.8 V to 5.5 V
16	VREF/MODE	Input	External reference or interface mode select input. Connect a capacitor (approximately 0.1 µF) between VREF and AGND. Use a pullup resistor to VDD when the external reference is not used. In case an external reference is used or when in interface select mode, make sure the reference ramps up after VDD. In interface select mode: Pull this pin low to enable I^2C/SPI communication. Pull this pin high to enable standalone mode.
—	Thermal Pad	Ground	Connect the thermal pad to AGND.

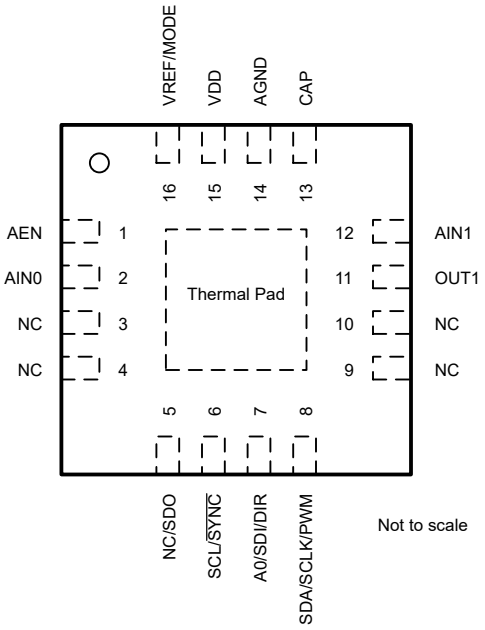


Figure 5-3. AFE439A2: RTE Package, 16-pin WQFN (Top View)

Table 5-3. Pin Functions: AFE439A2

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AEN	Input	ADC hardware enable pin. Connect this pin to VDD with a pullup resistor.
2	AIN0	Input	Analog input for ADC channel 0.
3	NC	—	Not connected.
4	NC	—	Not connected.
5	NC/SDO	Output	This pin can be configured as SDO or left unconnected. For SDO function, connect this pin to the IO voltage with an external pullup resistor.
6	SCL/$\overline{\text{SYNC}}$	Input	I^2C serial interface clock or SPI chip select input. Connect this pin to the IO voltage using an external pullup resistor.
7	A0/SDI/DIR	Input	*Programming mode*: Address configuration input for I^2C or serial data input for SPI. In A0 function, connect this pin to VDD, AGND, SDA, or SCL for address configuration. In SDI function, this pin does not need termination. *Standalone mode*: Direction output.
8	SDA/ SCLK/PWM	Input/Output	*Programming mode*: Bidirectional I^2C serial data bus or SPI clock input. Connect this pin to the IO voltage using an external pullup resistor. *Standalone mode*: PWM output.
9	NC	—	Not connected.
10	NC	—	Not connected.
11	NC	—	Not connected.
12	AIN1	Input	Analog input for comparator. When unused, pull this pin to VDD or AGND.
13	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 µF) between CAP and AGND.
14	AGND	Ground	Ground reference point for all circuitry on the device.
15	VDD	Power	Supply voltage: 1.8 V to 5.5 V
16	VREF/MODE	Input	External reference or interface mode select input. Connect a capacitor (approximately 0.1 µF) between VREF and AGND. Use a pullup resistor to VDD when the external reference is not used. In case an external reference is used or when in interface select mode, make sure the reference ramps up after VDD. In interface select mode: Pull this pin low to enable I^2C/SPI communication. Pull this pin high to enable standalone mode.
—	Thermal Pad	Ground	Connect the thermal pad to AGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage, V_{DD} to AGND	–0.3	6	V
	Digital inputs to AGND	–0.3	V_{DD} + 0.3	V
	V_{FBX} to AGND	–0.3	V_{DD} + 0.3	V
	V_{OUTX} or A_{INX} to AGND	–0.3	V_{DD} + 0.3	V
V_{REF}	External reference, V_{REF} to AGND	–0.3	V_{DD} + 0.3	V
	Current into any pin except the OUTx, VDD, and AGND pins	–10	10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage to ground (AGND)	1.7		5.5	V
V_{REF}	External reference to ground (AGND)	1.7		V_{DD}	V
V_{IH}	Digital input high voltage, 1.7 V < V_{DD} ≤ 5.5 V	1.62			V
V_{IL}	Digital input low voltage			0.4	V
C_{CAP}	External capacitor on CAP pin	0.5		15	µF
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		AFE439A2, AFE539A4, AFE639D2 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report.*

6.5 Electrical Characteristics: Voltage Output

all minimum/maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	AFE639D2	12			Bits
		AFE539A4	10			
INL	Integral nonlinearity(1)	AFE639D2	–4		4	LSB
		AFE539A4	–1		1	
DNL	Differential nonlinearity(1)		–1		1	LSB
	Zero-code error(2)	Code 0d into DAC, external reference, V_{DD} = 5.5 V		6	12	mV
		Code 0d into DAC, internal V_{REF}, gain = 4 ×, V_{DD} = 5.5 V		6	15	
	Zero-code error temperature coefficient(2)			±10		µV/°C
	Offset error(2)	1.7 V ≤ V_{DD} < 2.7 V, V_{FB} pin shorted to V_{OUT}, DAC code: 32d for 12-bit resolution, 8d for 10-bit resolution	–0.75	0.3	0.75	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, V_{FB} pin shorted to V_{OUT}, DAC code: 32d for 12-bit resolution, 8d for 10-bit resolution	–0.5	0.25	0.5	
	Offset-error temperature coefficient(2)	V_{FB} pin shorted to V_{OUT}, DAC code: 32d for 12-bit resolution, 8d for 10-bit resolution		±0.0003		%FSR/°C
	Gain error(2)	Between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution	–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient(2)	Between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution		±0.0008		%FSR/°C
	Full-scale error(2)	1.7 V ≤ V_{DD} < 2.7 V, DAC at full-scale	–1		1	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, DAC at full-scale	–0.5		0.5	
	Full-scale-error temperature coefficient(2)	DAC at full-scale		±0.0008		%FSR/°C
OUTPUT						
	Output voltage	Reference tied to V_{DD}	0		V_{DD}	V
C_L	Capacitive load(3)	R_L = infinite, phase margin = 30°			200	pF
		Phase margin = 30°			1000	
	Short-circuit current	V_{DD} = 1.7 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		15		mA
		V_{DD} = 2.7 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		50		
		V_{DD} = 5.5 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		60		
	Output-voltage headroom(3)	To V_{DD}, DAC output unloaded, internal reference = 1.21 V), V_{DD} ≥ 1.21 V × gain + 0.2 V	0.2			V
		To V_{DD} and to AGND, DAC output unloaded, external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD}	0.8			%FSR
		To V_{DD} and to AGND, I_{LOAD} = 10 mA at V_{DD} = 5.5 V, I_{LOAD} = 3 mA at V_{DD} = 2.7 V, I_{LOAD} = 1 mA at V_{DD} = 1.8 V, external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD}	10			
Z_O	V_{FB} dc output impedance(4)	DAC output enabled, internal reference (gain = 1.5 × or 2 ×) or external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD}	400	500	600	kΩ
		DAC output enabled, internal V_{REF}, gain = 3 × or 4 ×	325	400	485	

6.5 Electrical Characteristics: Voltage Output (continued)

all minimum/maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio (dc)	Internal V_{REF}, gain = 2 ×, DAC at midscale, V_{DD} = 5 V ±10%		0.25		mV/V
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		20		µs
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V, internal V_{REF}, gain = 4 ×		25		
	Slew rate	V_{DD} = 5.5 V		0.3		V/µs
	Power-on glitch magnitude	At start-up, DAC output disabled		75		mV
		At start-up, DAC output disabled, R_L = 100 kΩ		200		
	Output-enable glitch magnitude	DAC output disabled to enabled, DAC registers at zero scale, R_L = 100 kΩ		250		mV
V_n	Output noise voltage (peak to peak)	f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		50		μV_{PP}
		Internal V_{REF}, gain = 4 ×, f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		90		
	Output noise density	f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.35		$\mu V/\sqrt{Hz}$
		Internal V_{REF}, gain = 4 ×, f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.9		
	Power supply rejection ratio (ac)(4)	Internal V_{REF}, gain = 4 ×, 200-mV 50-Hz or 60-Hz sine wave superimposed on power supply voltage, DAC at midscale		–68		dB
	Code change glitch impulse	±1-LSB change around midscale (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1-LSB change around midscale (including feedthrough)		15		mV

(1) Measured with DAC output unloaded. For external reference and internal reference V_{DD} ≥ 1.21 × gain + 0.2 V, between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution.
(2) Measured with DAC output unloaded.
(3) Specified by design and characterization, not production tested.
(4) Specified with 200-mV headroom with respect to reference value when internal reference is used.

6.6 Electrical Characteristics: Comparator Mode

all minimum/maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, reference tied to VDD, gain = 1 ×, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Offset error(1) (2)	1.7 V ≤ V_{DD} ≤ 5.5 V; DAC at midscale, comparator input at Hi-Z, and DAC operating with external reference.	–5	0	5	mV
	Offset error time drift(1)	V_{DD} = 5.5 V, external reference, T_A = 125°C, AIN in Hi-Z mode, DAC at full scale and V_{AIN} at 0 V or DAC at zero scale and V_{AIN} at 1.84 V, drift specified for 10 years of continuous operation		4		mV
OUTPUT						
	Input voltage	V_{REF} connected to V_{DD}, AIN resistor network connected to ground	0		V_{DD}	V
		V_{REF} connected to V_{DD}, AIN resistor network disconnected from ground	0		V_{DD} (1/3 – 1/100)	
V_{OL}	Logic low output voltage	I_{LOAD} = 100 µA, output in open-drain mode		0.1		V
DYNAMIC PERFORMANCE						
t_{resp}	Output response time	DAC at midscale with 10-bit resolution, AIN input at Hi-Z, and transition step at AIN node is (V_{DAC} – 2 LSB) to (V_{DAC} + 2 LSB), transition time measured between 10% and 90% of output, output current of 100 µA, comparator output configured in push-pull mode, load capacitor at DAC output is 25 pF		10		µs

(1) Specified by design and characterization, not production tested.
(2) This specification does not include the total unadjusted error (TUE) of the DAC.

6.7 Electrical Characteristics: ADC Input

all minimum/maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, reference tied to VDD, gain = 1 ×, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution	AFE539A4	10			Bits
		AFE439A2	8			
INL	Integral nonlinearity(1) (2)		–2		2	LSB
DNL	Differential nonlinearity(1) (2)		–1		1	LSB
	Offset error(1) (2) (3)	1.7 V ≤ V_{DD} < 2.7 V	–5	0	5	mV
		2.7 V ≤ V_{DD} ≤ 5.5 V	–5	0	5	
	Gain error(1) (2) (3)		–1		1	%FSR
	Input voltage	External V_{REF} = V_{DD}, analog input attenuation is 1	0		V_{DD}	V
	Data rate(2)	ADC averaging setting is 4 samples	1406		2008	SPS
	Sampling capacitor			10		pF

(1) For external reference and internal reference V_{DD} ≥ 1.21 × gain + 0.2 V, between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution.
(2) Specified by design and characterization, not production tested.
(3) Measured at analog input at mid-scale, Hi-Z input configuration, and with external reference.

6.8 Electrical Characteristics: General

all minimum/maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, reference tied to VDD, gain = 1 ×, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE						
	Initial accuracy	T_A = 25°C for all measurements	1.1979	1.212	1.224	V
	Reference output temperature coefficient(1) (2)				50	ppm/°C
EXTERNAL REFERENCE						
	External reference input range		1.7		V_{DD}	V
	V_{REF} input impedance(1) (3)			192		kΩ-ch
EEPROM						
	Endurance(1)	–40°C ≤ T_A ≤ +85°C		20000		Cycles
		T_A = 125°C		1000		
	Data retention(1)			50		Years
	EEPROM programming write cycle time(1)				200	ms
	Device boot-up time(1)	Time taken from power valid (V_{DD} ≥ 1.7 V) to output valid state (output state as programmed in EEPROM), 0.5-µF capacitor on the CAP pin		5		ms
DIGITAL INPUTS						
	Digital feedthrough	Voltage output mode, DAC output static at midscale, fast mode plus, SCL toggling		20		nV-s
	Pin capacitance	Per pin		10		pF
POWER						
I_{DD}	Current flowing into VDD	Sleep mode, internal reference powered down, external reference at 5.5 V			28	µA
	Current flowing into VDD(1)	Sleep mode, internal reference enabled, additional current through internal reference		10		
		All channels enabled, internal reference enabled, additional current through internal reference per channel		12.5		µA-ch
		Normal operation, state machine enabled, AFE439A2		1.05		mA
		Normal operation, state machine enabled, AFE539A4		1.4		
		Normal operation, state machine enabled, AFE639D2		1.04		
HIGH-IMPEDANCE OUTPUT						
I_{LEAK}	Current flowing into V_{OUTX} and V_{FBX}	DAC in Hi-Z output mode, 1.7 V ≤ V_{DD} ≤ 5.5 V		10		nA
		V_{DD} = 0 V, V_{OUT} ≤ 1.5 V, decoupling capacitor between V_{DD} and AGND = 0.1 µF		200		
		V_{DD} = 0 V, 1.5 V < V_{OUT} ≤ 5.5 V, decoupling capacitor between V_{DD} and AGND = 0.1 µF		500		
		100 kΩ between V_{DD} and AGND, V_{OUT} ≤ 1.25 V, series resistance of 10 kΩ at OUT pin		±2		µA

(1) Specified by design and characterization, not production tested.
(2) Measured at –40°C and +125°C and calculated the slope.
(3) Impedances for the DAC, comparator, or ADC channels are connected in parallel.

6.9 Timing Requirements: I²C Standard Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			100	kHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			3.45	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			3.45	µs

6.10 Timing Requirements: I²C Fast Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			400	kHz
t_{BUF}	Bus free time between stop and start conditions	1.3			µs
t_{HDSTA}	Hold time after repeated start	0.6			µs
t_{SUSTA}	Repeated start setup time	0.6			µs
t_{SUSTO}	Stop condition setup time	0.6			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.9	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.9	µs

6.11 Timing Requirements: I²C Fast Mode Plus

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			µs
t_{HDSTA}	Hold time after repeated start	0.26			µs
t_{SUSTA}	Repeated start setup time	0.26			µs
t_{SUSTO}	Stop condition setup time	0.26			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			µs
t_{HIGH}	SCL clock high period	0.26			µs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.45	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.45	µs

6.12 Timing Requirements: SPI Write Operation

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			50	MHz
$t_{SCLKHIGH}$	SCLK high time	9			ns
$t_{SCLKLOW}$	SCLK low time	9			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	18			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	10			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	50			ns
$t_{DACWAIT}$	Sequential update wait time (time between subsequent $\overline{SYNC}$ rising edges) for same channel	2			µs

6.13 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 0)

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 0

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			1.25	MHz
$t_{SCLKHIGH}$	SCLK high time	350			ns
$t_{SCLKLOW}$	SCLK low time	350			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	400			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	400			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	1			µs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ≤ 5 mA, C_L = 20 pF			300	ns

6.14 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 1)

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 1

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			2.5	MHz
$t_{SCLKHIGH}$	SCLK high time	175			ns
$t_{SCLKLOW}$	SCLK low time	175			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	300			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	300			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	1			µs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ≤ 5 mA, C_L = 20 pF			300	ns

6.15 Timing Requirements: PWM Output

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{PWMOUT}	PWM frequency(1)	0.218		48.828	kHz
t_{PWMOHI}	PWM high time	1			µs
t_{PWMOLO}	PWM low time	1			µs
$t_{PWMODTY}$	PWM duty cycle	0		100	%

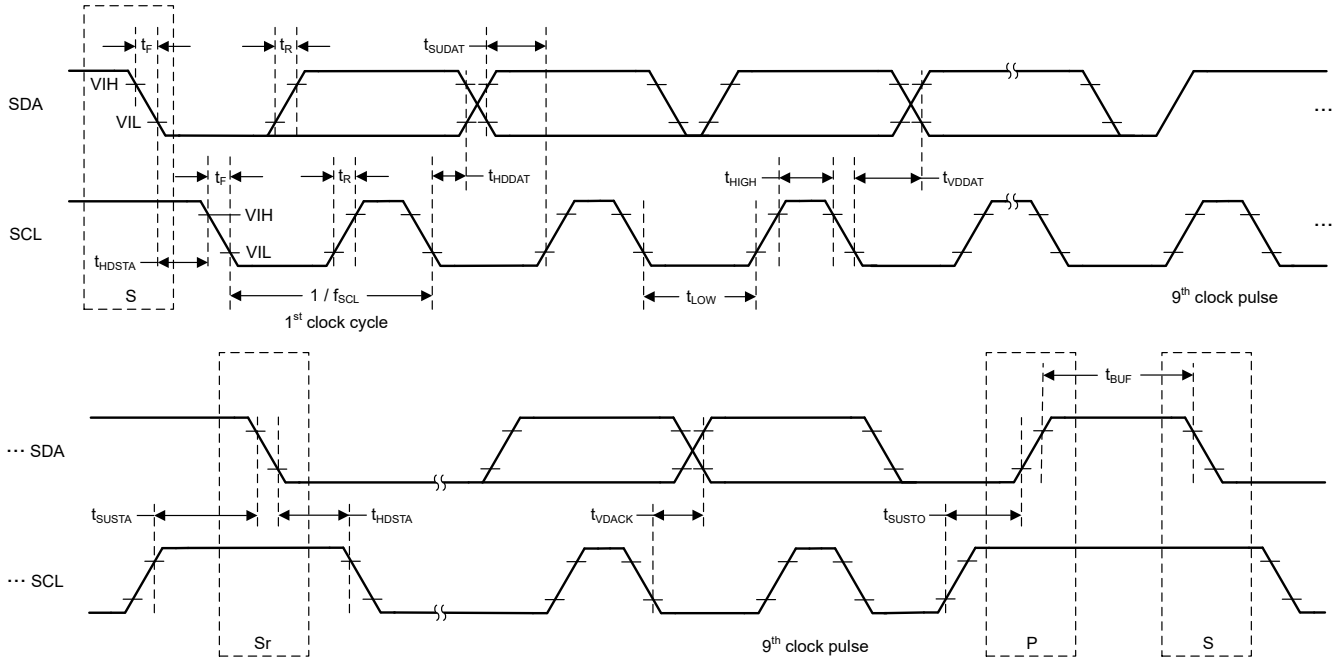
(1) The frequency range does not account for the internal oscillator frequency error.

6.16 Timing Requirements: I²C Controller

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			100	kHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns

6.17 Timing Diagrams



S: Start bit, **Sr**: Repeated start bit, **P**: Stop bit

Figure 6-1. I²C Timing Diagram

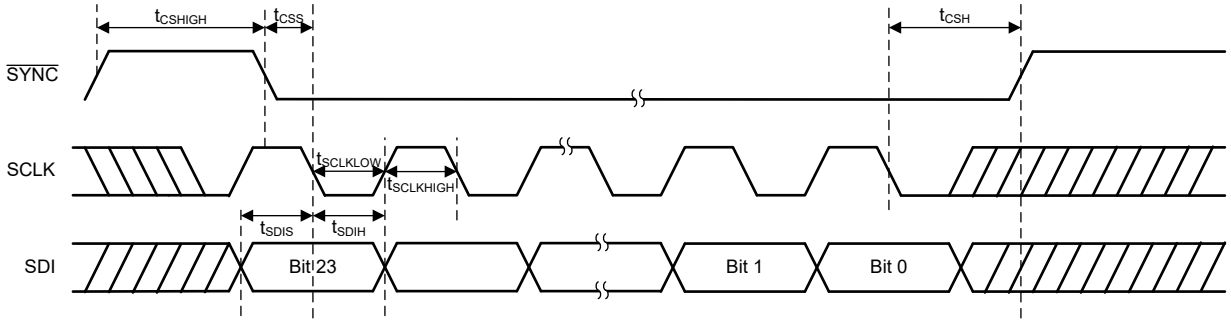


Figure 6-2. SPI Write Timing Diagram

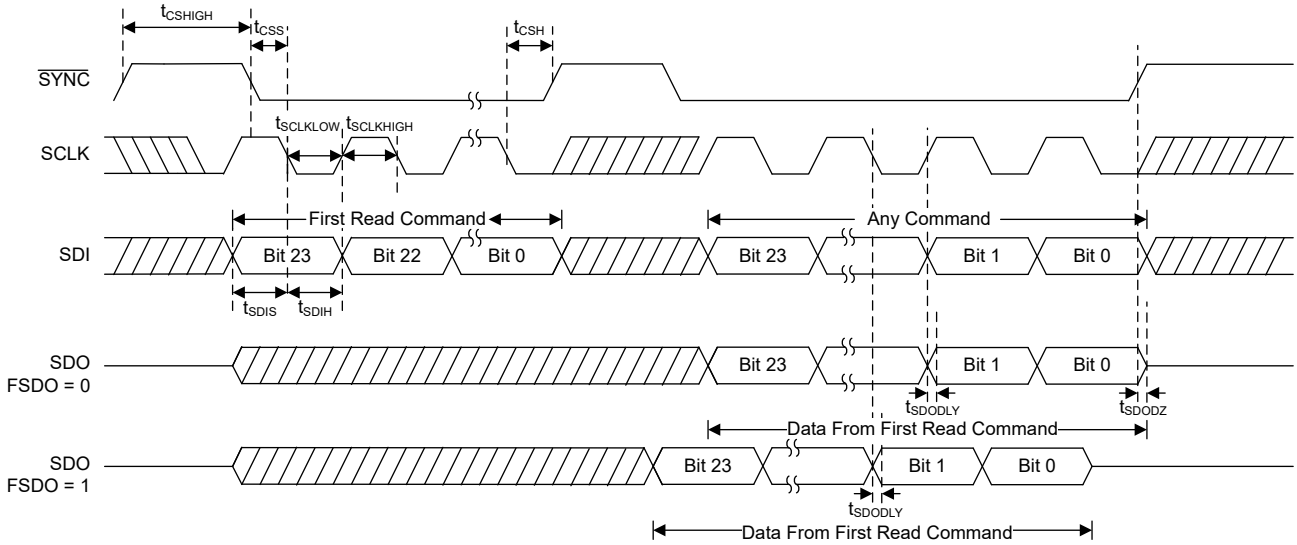


Figure 6-3. SPI Read Timing Diagram

6.18 Typical Characteristics: Voltage Output

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

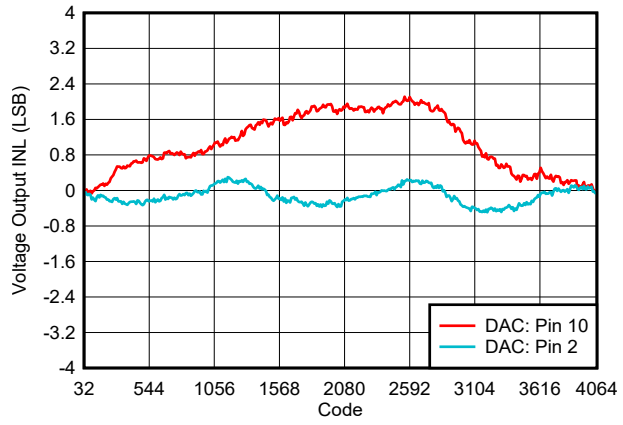


Figure 6-4. Voltage Output INL vs Digital Input Code

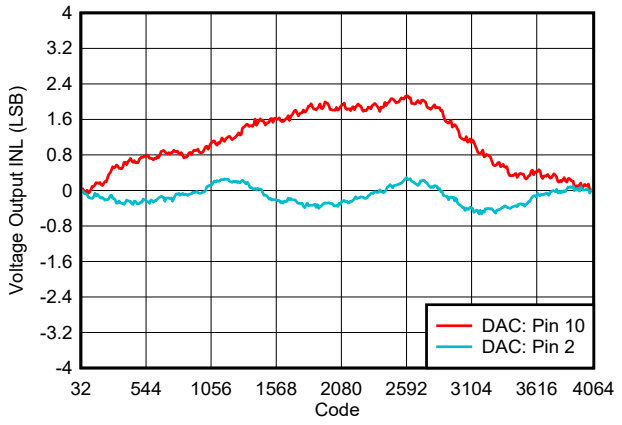


Figure 6-5. Voltage Output INL vs Digital Input Code

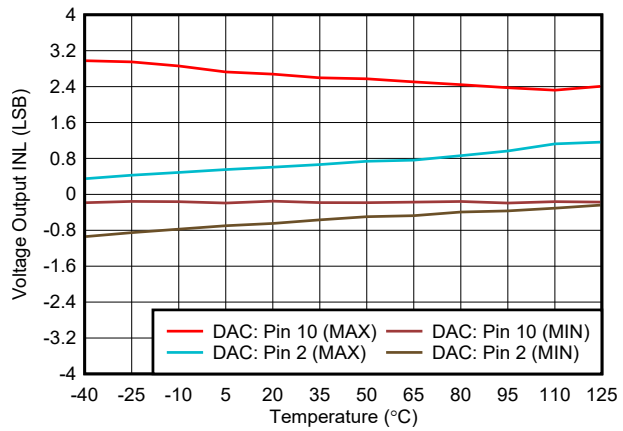


Figure 6-6. Voltage Output INL vs Temperature

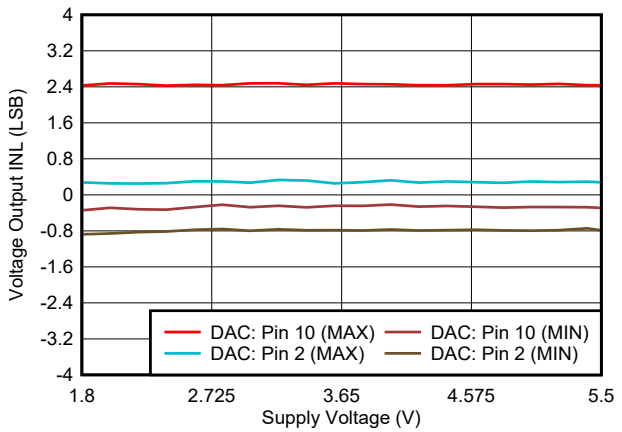


Figure 6-7. Voltage Output INL vs Supply Voltage

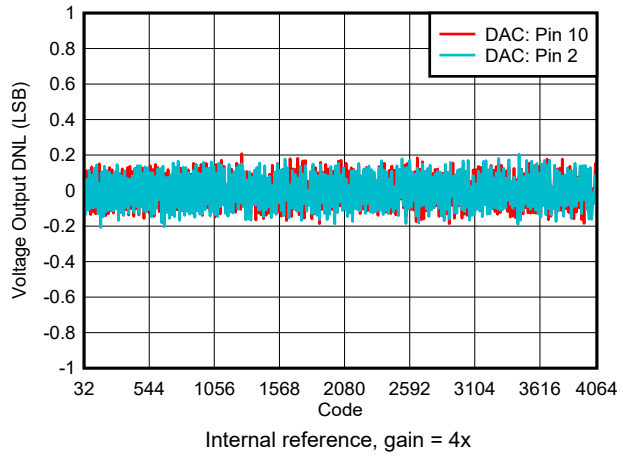


Figure 6-8. Voltage Output DNL vs Digital Input Code

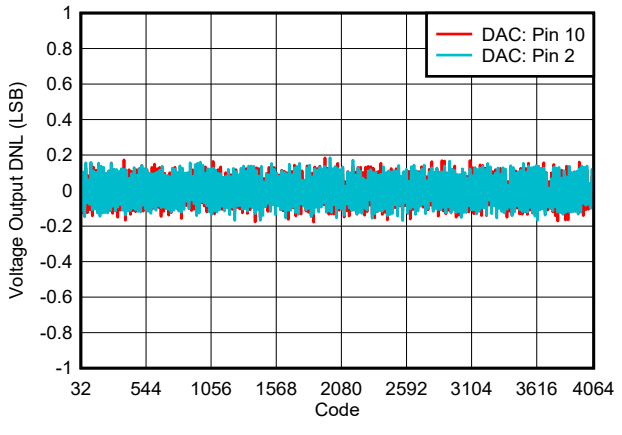


Figure 6-9. Voltage Output DNL vs Digital Input Code

6.18 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

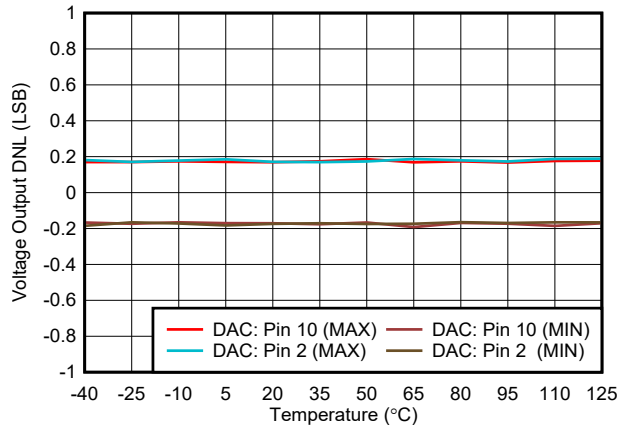


Figure 6-10. Voltage Output DNL vs Temperature

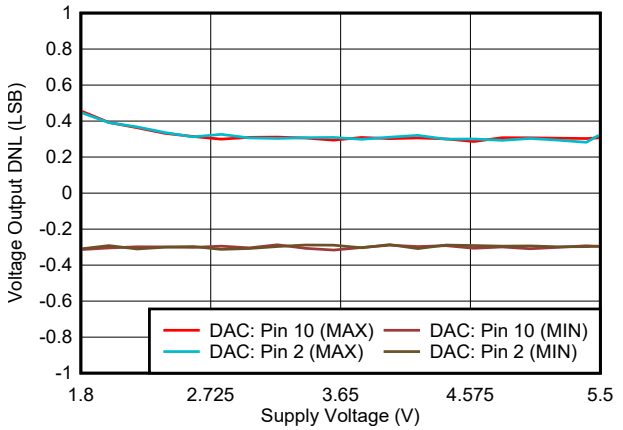


Figure 6-11. Voltage Output DNL vs Supply Voltage

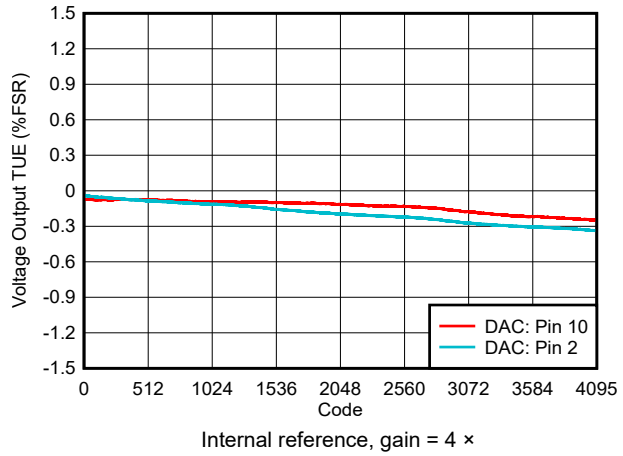


Figure 6-12. Voltage Output TUE vs Digital Input Code

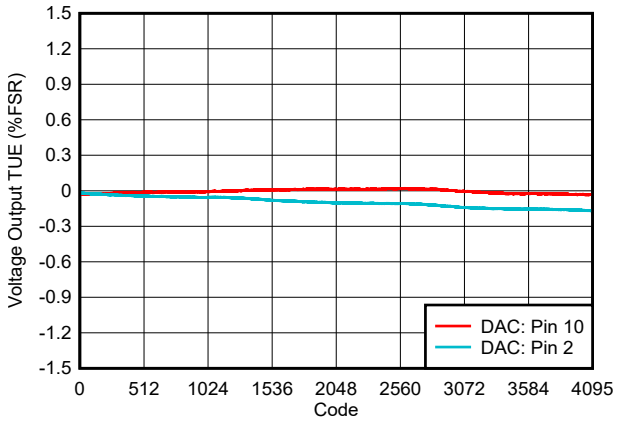


Figure 6-13. Voltage Output TUE vs Digital Input Code

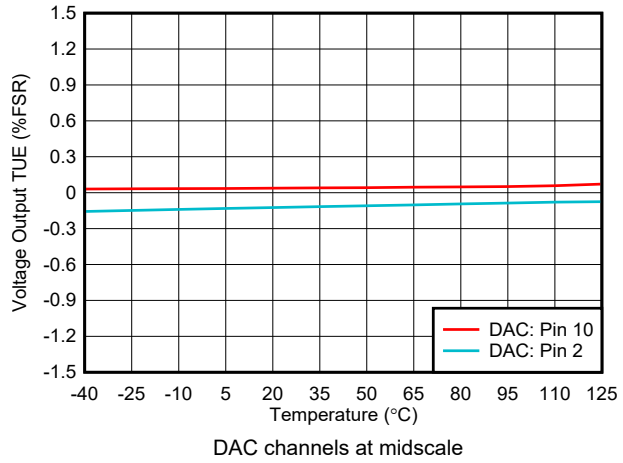


Figure 6-14. Voltage Output TUE vs Temperature

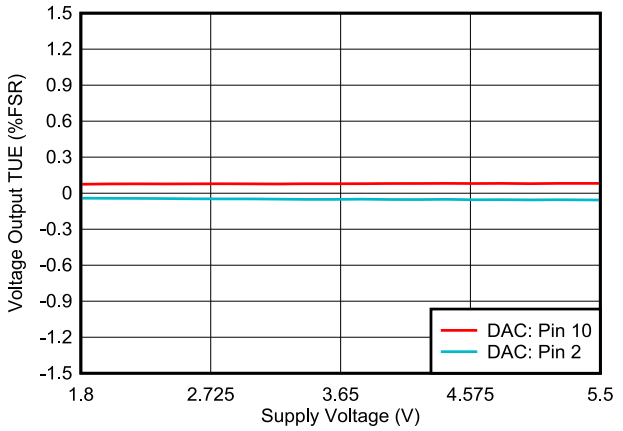


Figure 6-15. Voltage Output TUE vs Supply Voltage

6.18 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

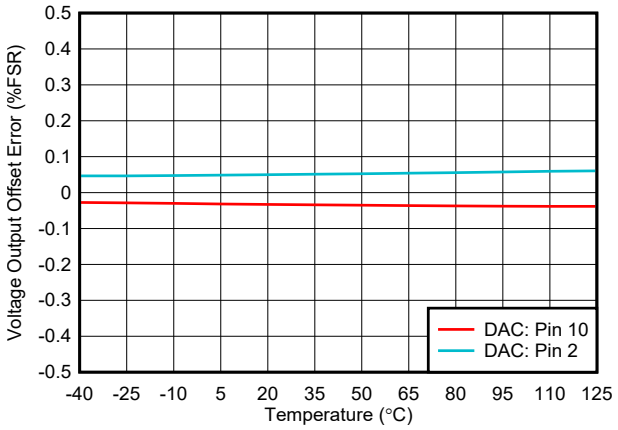


Figure 6-16. Voltage Output Offset Error vs Temperature

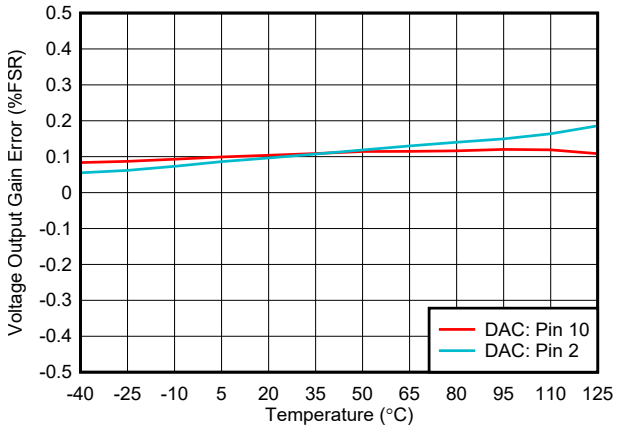
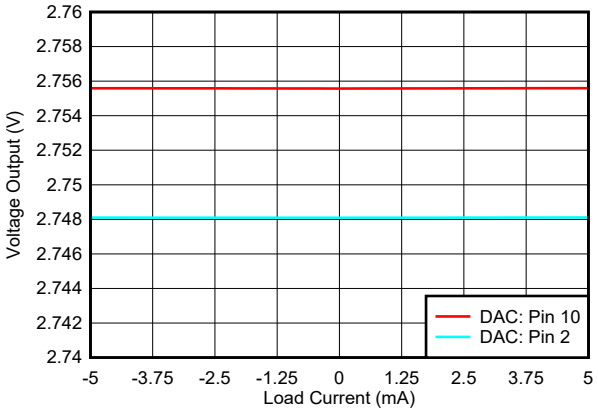


Figure 6-17. Voltage Output Gain Error vs Temperature



DAC channels at midscale

Figure 6-18. Voltage Output vs Load Current

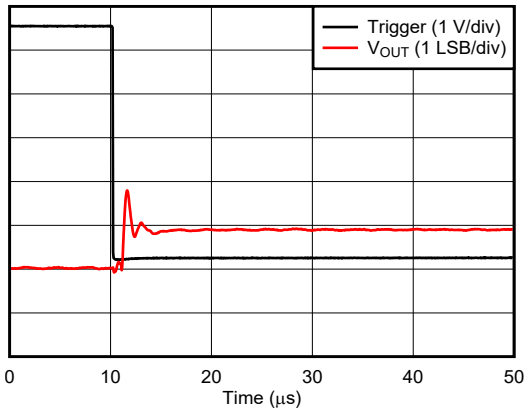


Figure 6-19. Voltage Output Code-to-Code Glitch - Rising Edge

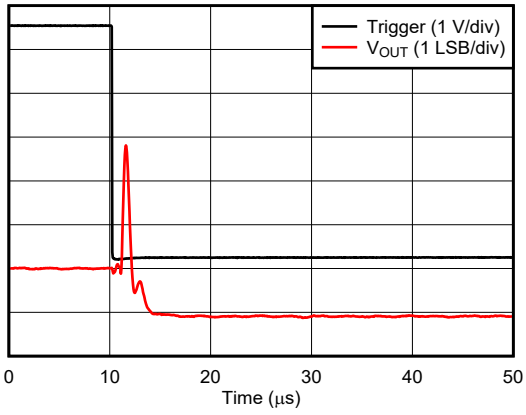
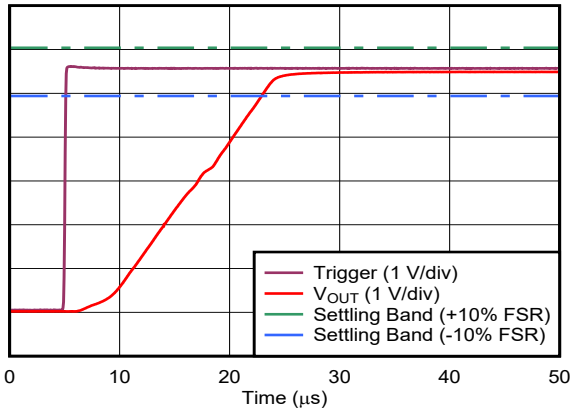


Figure 6-20. Voltage Output Code-to-Code Glitch - Falling Edge

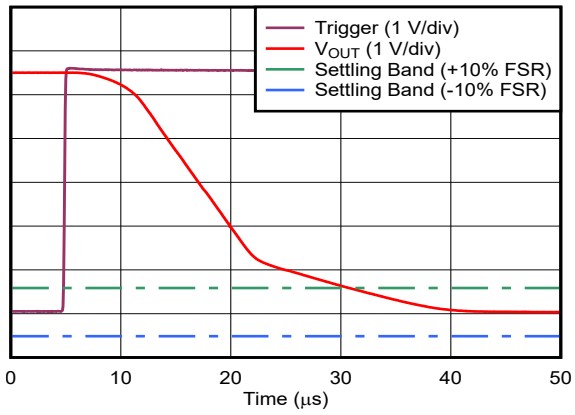


Zero scale to full scale swing

Figure 6-21. Voltage Output Setting Time - Rising Edge

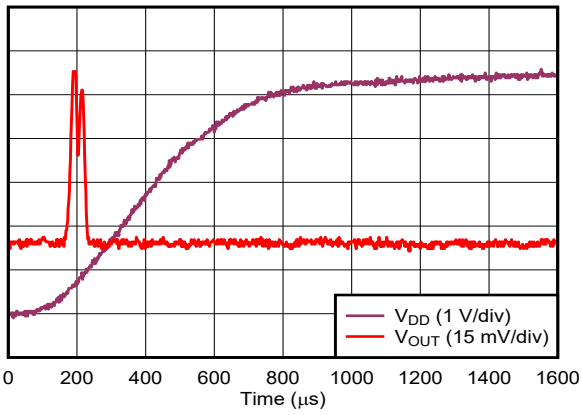
6.18 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



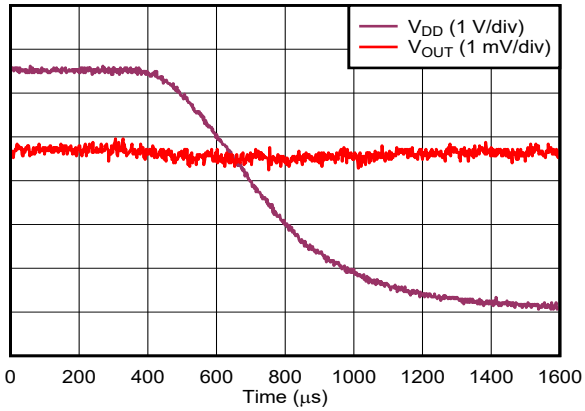
Full scale to zero scale swing

Figure 6-22. Voltage Output Setting Time - Falling Edge



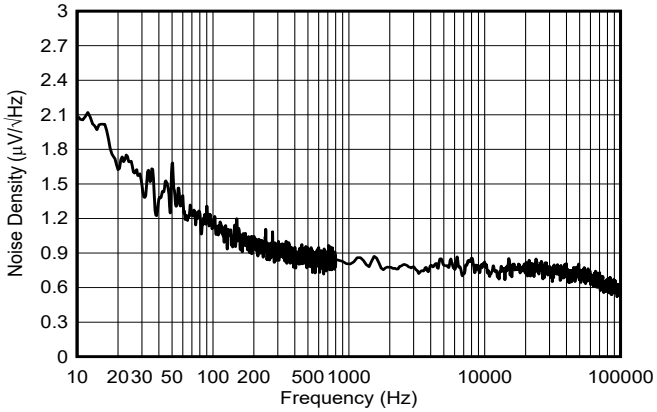
DAC in Hi-Z power-down mode

Figure 6-23. Voltage Output Power-On Glitch



DAC at zero scale

Figure 6-24. Voltage Output Power-Off Glitch



Internal reference, gain = 4 ×

Figure 6-25. Voltage Output Noise Density

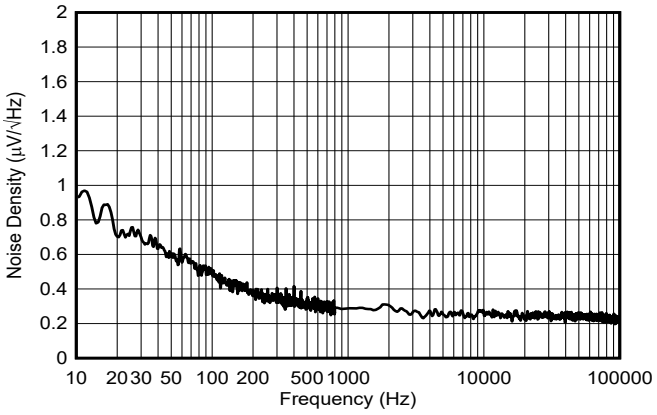
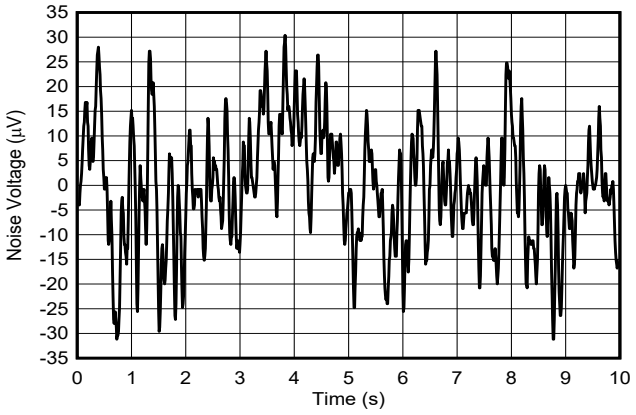


Figure 6-26. Voltage Output Noise Density

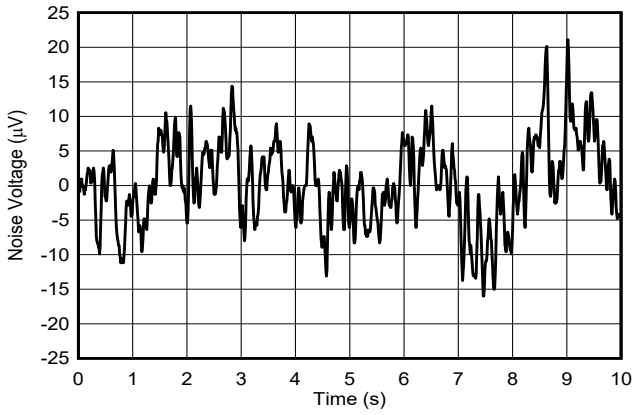


Internal reference, gain = 4 ×, f = 0.1 Hz to 10 Hz

Figure 6-27. Voltage Output Flicker Noise

6.18 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



f = 0.1 Hz to 10 Hz

Figure 6-28. Voltage Output Flicker Noise

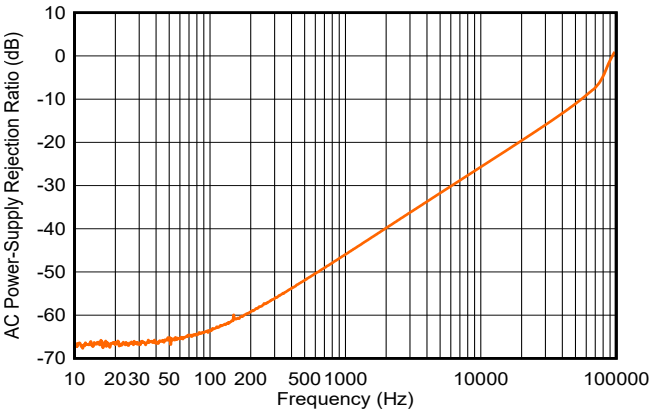


Figure 6-29. Voltage Output AC PSRR vs Frequency

6.19 Typical Characteristics: ADC

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 10-bit resolution, and Hi-Z input (unless otherwise noted)

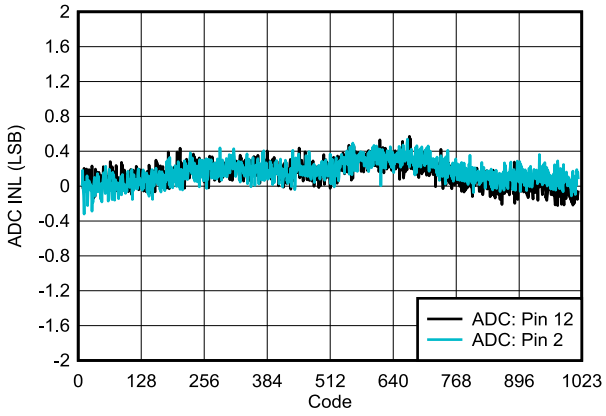


Figure 6-30. ADC INL vs Digital Output Code

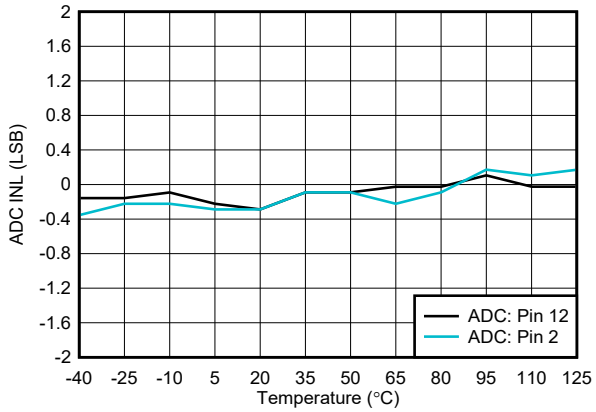


Figure 6-31. ADC INL vs Temperature

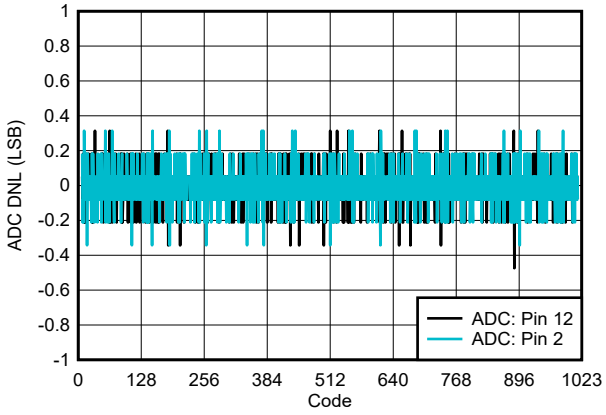


Figure 6-32. ADC DNL vs Digital Output Code

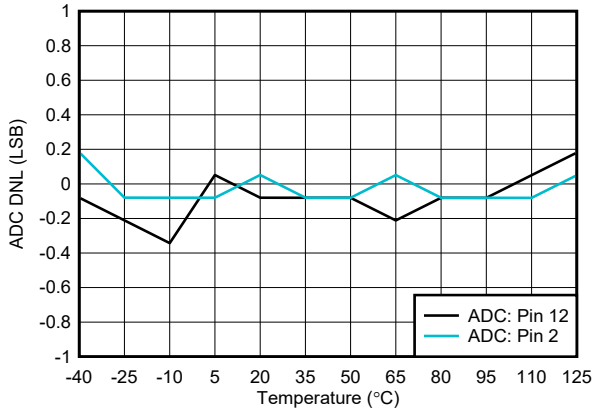


Figure 6-33. ADC DNL vs Temperature

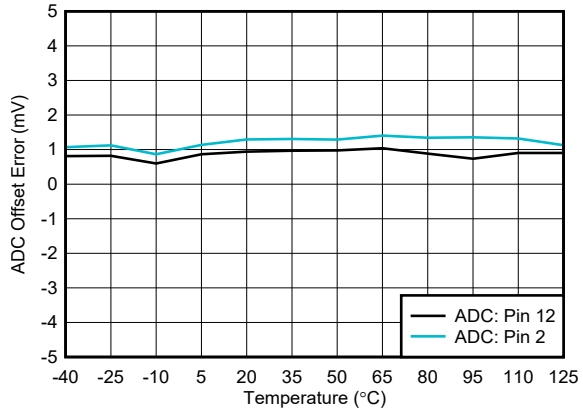


Figure 6-34. ADC Offset Error vs Temperature

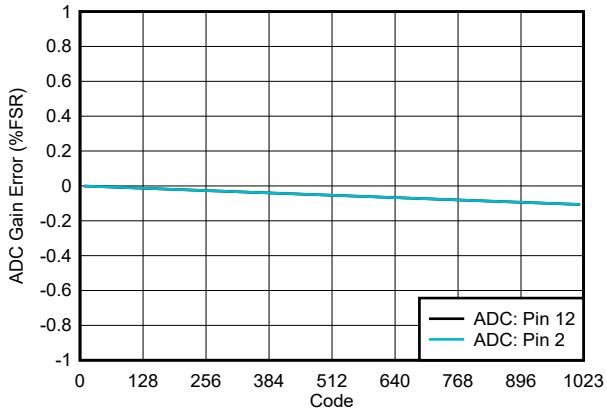


Figure 6-35. ADC Gain Error vs Digital Output Code

6.19 Typical Characteristics: ADC (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 10-bit resolution, and Hi-Z input (unless otherwise noted)

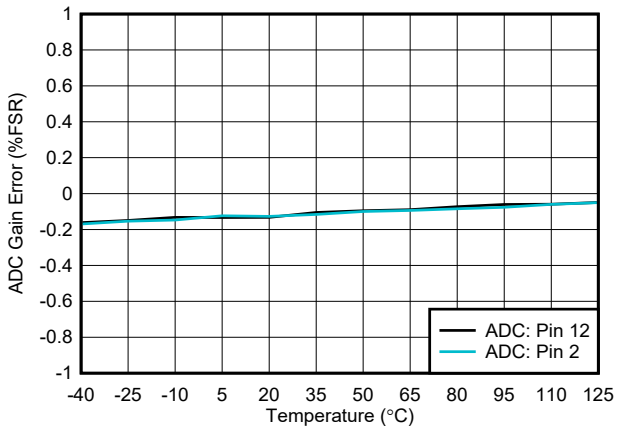


Figure 6-36. ADC Gain Error vs Temperature

6.20 Typical Characteristics: Comparator

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, AINx pin in Hi-Z mode, and DAC outputs unloaded (unless otherwise noted)

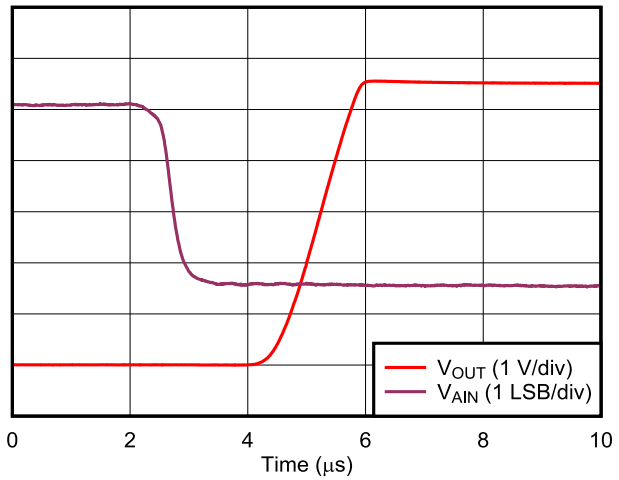


Figure 6-37. Comparator Response Time: Low-to-High Transition

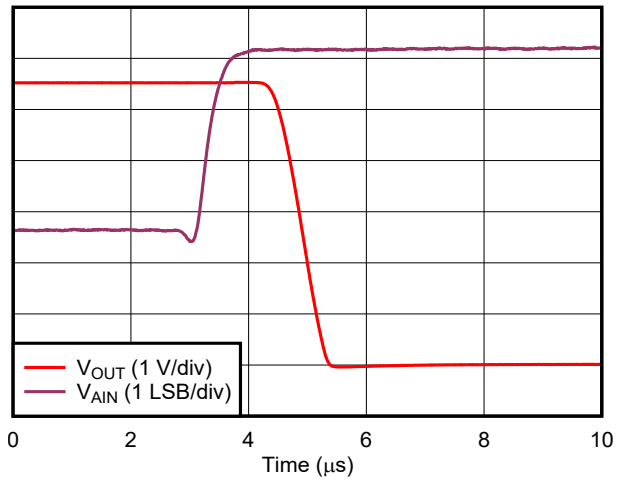


Figure 6-38. Comparator Response Time: High-to-Low Transition

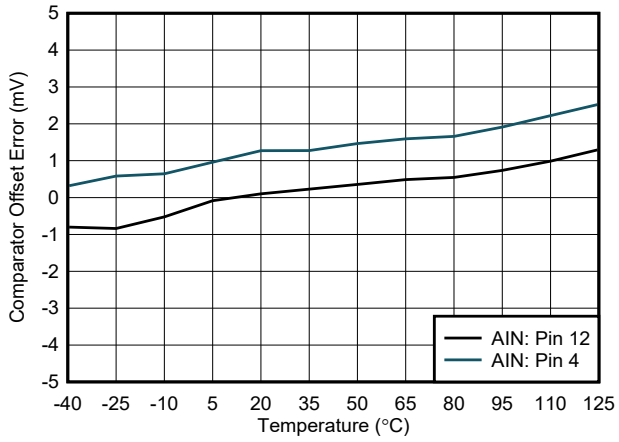
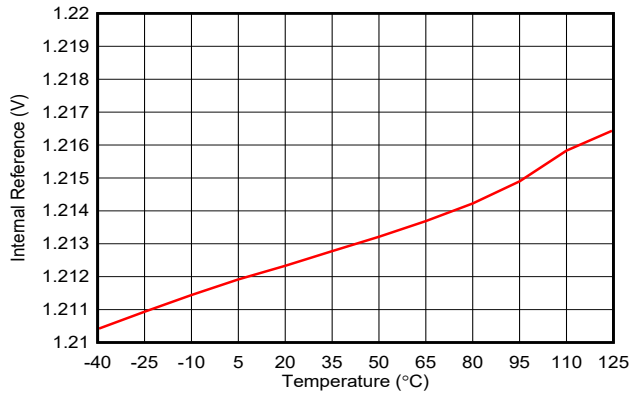


Figure 6-39. Comparator Offset Error vs Temperature

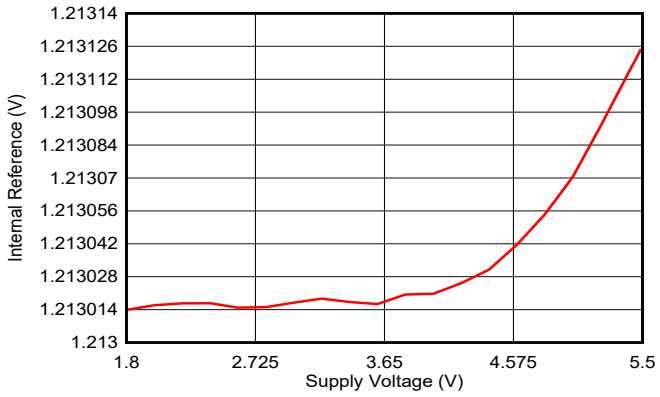
6.21 Typical Characteristics: General

at T_A = 25°C, V_{DD} = 5.5 V, and DAC outputs unloaded (unless otherwise noted)



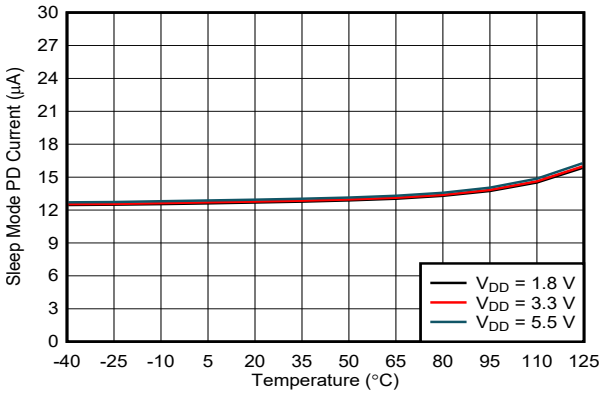
Internal reference

Figure 6-40. Internal Reference vs Temperature



Internal reference

Figure 6-41. Internal Reference vs Supply Voltage



Sleep mode, internal reference disabled

Figure 6-42. Power-Down Current vs Temperature

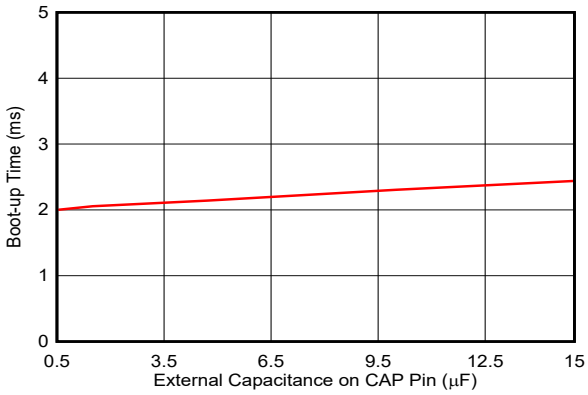


Figure 6-43. Boot-up Time vs Capacitance on CAP pin

7 Detailed Description

7.1 Overview

The 8-bit AFE439A2, 10-bit AFE539A4, and 12-bit AFE639D2 devices (AFEx39xx) are smart analog front ends (AFE) for thermoelectric cooling (TEC) control using voltage or PWM output. These devices support a programmable comparator input for fault management. Table 7-1 provides the key functions these devices support.

Table 7-1. Function List

DEVICE	ADC	DAC	PWM	COMPARATOR	I^2C CONTROLLER	PI CONTROL
AFE439A2	8-bit	No	7-bit	8-bit	No	Yes
AFE539A4	10-bit	10-bit	No	10-bit	No	Yes
AFE639D2	Interfaces to external ADC	12-bit	No	12-bit	Yes	Yes

The AFEx39xx provide a pre-programmed state machine that functions as a proportional-integral (PI) controller. These devices contain nonvolatile memory (NVM), an internal reference, and automatically detect I^2C and SPI. The AFEx39xx has a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The AFEx39xx operates with either an internal reference, external reference, or power supply as the reference.

The AFEx39xx supports I^2C standard mode (100Kbps), fast mode (400Kbps), and fast mode plus (1Mbps). The I^2C interface can be configured with four device addresses using the A0 pin. The SPI mode supports a three-wire interface by default, with up to 25-MHz SCLK input. The NC/SDO input can be configured as SDO in the NVM for SPI read capability. The AFEx39xx is designed for closed-loop control applications, such as TEC control, car seat heating control, medical in-vitro diagnostics devices, blood gas analyzers, and thermal cyclers.

The AFE639D2 includes an I^2C controller interface to interface with external digital temperature sensors. Use the VREF/MODE pin to select between the target mode and the controller mode.

7.2 Functional Block Diagrams

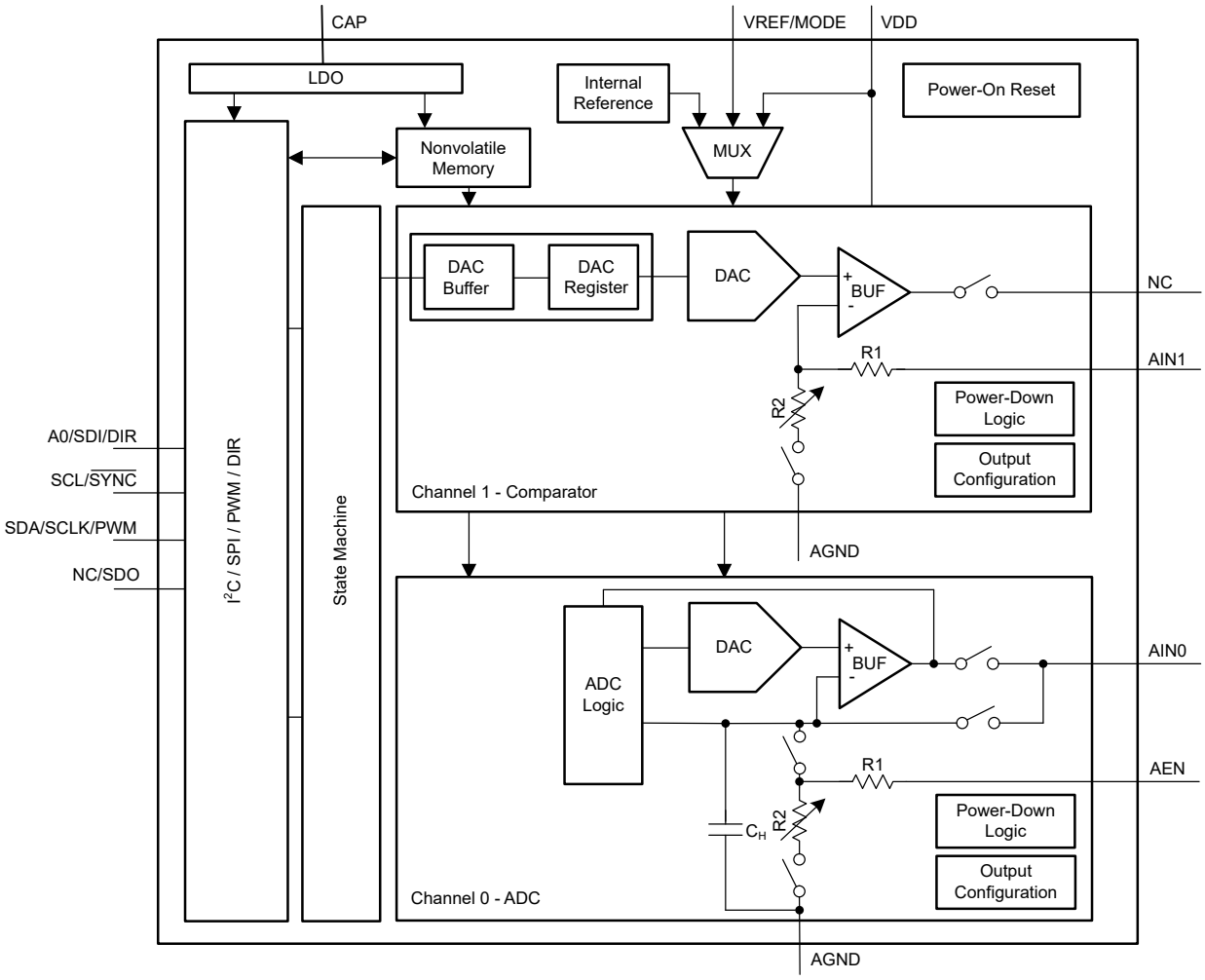


Figure 7-1. Functional Block Diagram: AFE439A2

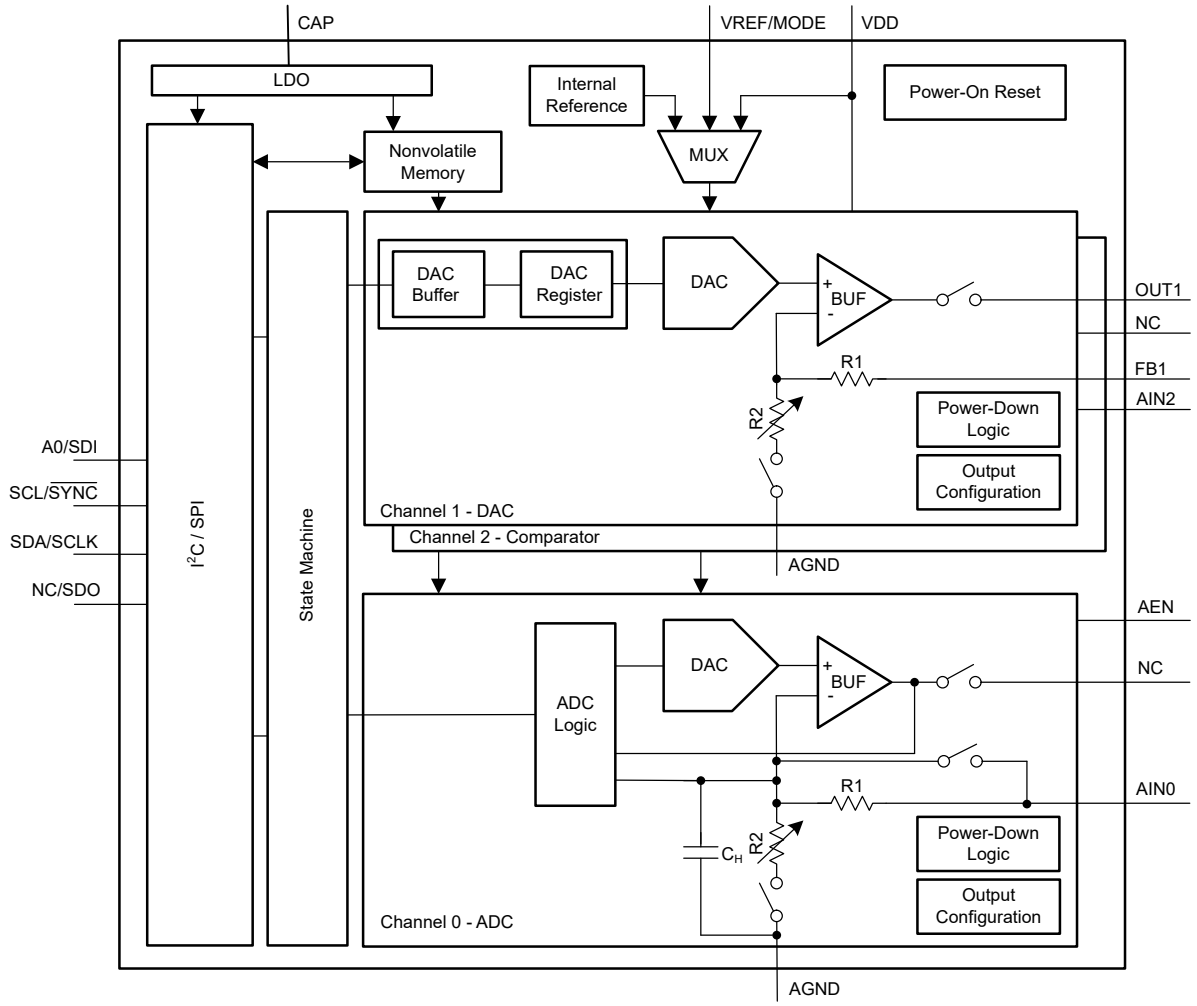


Figure 7-2. Functional Block Diagram: AFE539A4

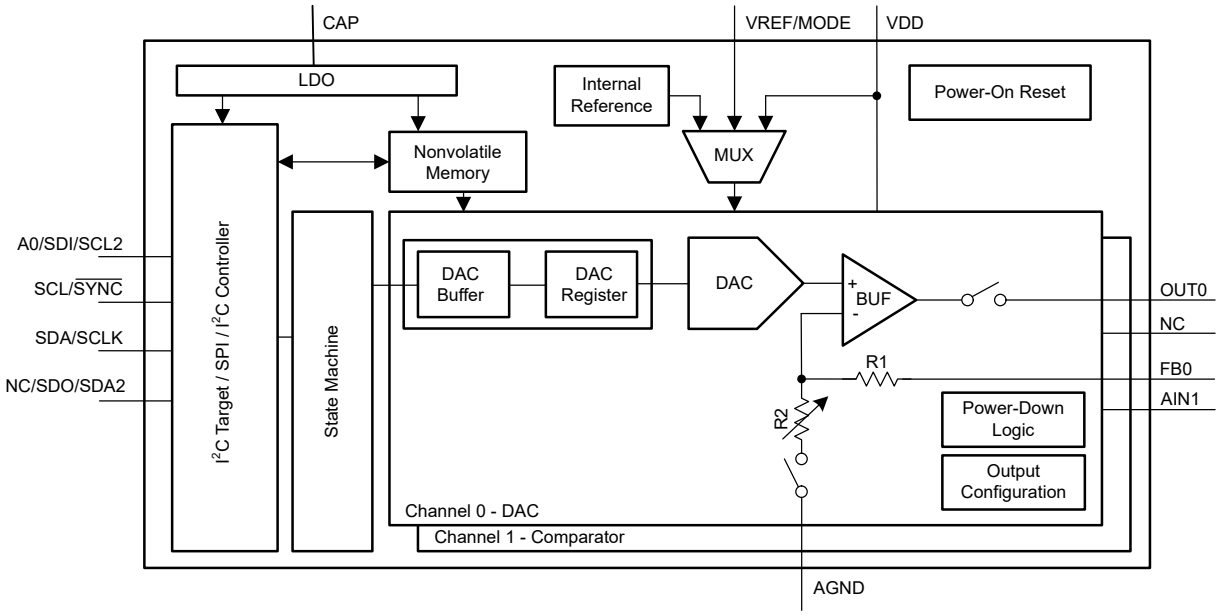


Figure 7-3. Functional Block Diagram: AFE639D2

7.3 Feature Description

7.3.1 Smart Analog Front End (AFE) Architecture

AFE639D2 consists of a 12-bit digital-to-analog converter (DAC) with string architecture, followed by a voltage-output amplifier. Similarly, AFE539A4 consists of a 10-bit DAC. Figure 7-3 and Figure 7-2 show the DAC architecture within the block diagram, which operates from a 1.8-V to 5.5-V power supply.

AFE439A2 supports 7-bit duty-cycle pulse-width modulation (PWM) output on the SDA/SCLK/PWM pin. Pull the VREF/MODE pin high to enable the PWM function. AFE439A2 also supports a DIR output to provide bidirectional control of TEC elements.

The AFEx39xx have an internal voltage reference of 1.21 V. There is an option to select an external reference on the VREF/MODE pin or use the power supply as a reference. These devices use one of these three reference options.

The AFEx39xx support an independent programmable comparator for fault management. The architecture supports inversion of the comparator output using register settings. The comparator outputs can be push-pull or open-drain. The comparator outputs are accessible internally by the device to force the PI controller output to a predefined value in case of a fault.

The AFE439A2 and AFE539A4 feature an ADC to sense the input for the PI controller. AFE639D2 provides an I^2C controller interface to interface to external digital temperature sensors.

The AFEx39xx feature a programmable state machine supporting arithmetic, logic, and timing operations, as shown in Figure 7-4. This state machine has been pre-programmed as a proportional-integral (PI) controller allowing the user to program the coefficients and input-output parameters. The details of the PI controller are discussed in Section 7.4.6. The user configurations are stored in the NVM and the state machine can be operated in standalone mode without interfacing to a processor (*processor-less* operation)

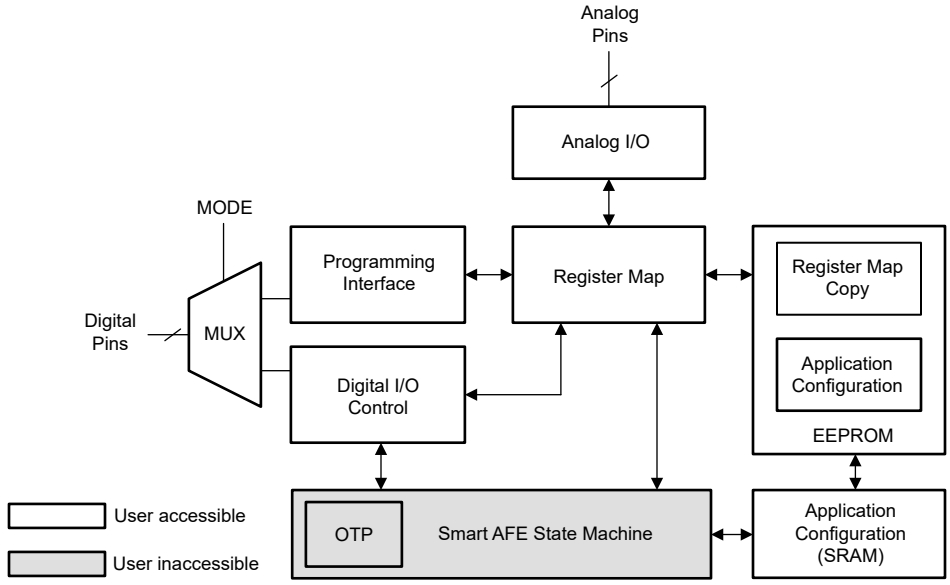


Figure 7-4. Smart AFE Architecture

7.3.2 Programming Interface

The AFEx39xx have four digital IO pins that include I^2C and SPI when the VREF/MODE pin is held low. These devices automatically detect I^2C and SPI protocols at the first successful communication after power on, and then connect to the detected interface. After an interface protocol is connected, any change in the protocol is ignored. The I^2C interface uses the A0 pin to select from among four address options. The SPI is a three-wire interface by default. No readback capability is available in the three-wire SPI mode. The NC/SDO pin can be configured as the SDO function in the register map and then programmed into the NVM. With the NC/SDO pin acting as SDO, the SPI works as a four-wire interface. The SPI readback mode is slower than the write mode. The programming interface pins are:

- For I^2C: SCL, SDA, A0
- For SPI: SCLK, SDI, $\overline{\text{SYNC}}$, NC/SDO

All the digital pins are open-drain when used as outputs. Therefore, all the output pins must be pulled up to the desired IO voltage using external registers.

7.3.3 Nonvolatile Memory (NVM)

The AFEx39xx contain nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain the set values in the absence of a power supply. All the register bits, shown in the highlighted gray cells in Table 7-23, can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register; this bit automatically resets. The NVM-BUSY bit in the GENERAL-STATUS register is set to 1 by the device when an NVM write or reload operation is ongoing. During this time, the device blocks all read and write operations to the device. The NVM-BUSY bit is set to 0 after the write or reload operation is complete; at this point, all read and write operations to the device are allowed. The default value for all the registers in the AFEx39xx is loaded from NVM as soon as a POR event is issued.

The AFEx39xx also reloads the registers with the current values stored in the NVM using the NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 for the device to start an NVM reload operation. After completion, the device automatically resets this bit to 0. During the NVM-RELOAD operation, the NVM-BUSY bit is set to 1.

7.3.3.1 NVM Cyclic Redundancy Check (CRC)

The AFEx39xx implements a cyclic redundancy check (CRC) feature for the NVM to make sure that the data stored in the NVM is uncorrupted. There are two types of CRC alarm bits implemented in the AFEx39xx:

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

The NVM-CRC-FAIL-USER bit indicates the status of user-programmable NVM bits, and the NVM-CRC-FAIL-INT bit indicates the status of internal NVM bits. The CRC feature is implemented by storing a 16-bit CRC (CRC-16-CCITT) along with the NVM data each time the NVM program operation (write or reload) is performed and during the device boot up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM-CRC-FAIL-USER and NVM-CRC-FAIL-INT in the GENERAL-STATUS register) report any errors after the data are read from the device NVM. The alarm bits are set only at boot up.

7.3.3.1.1 NVM-CRC-FAIL-USER Bit

A logic 1 on NVM-CRC-FAIL-USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the device are initialized with factory reset values, and any registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see *External Reset*) command, or cycle power to the device. A software reset or power-cycle also reloads the user-programmable NVM bits. In case the failure persists, reprogram the NVM.

7.3.3.1.2 NVM-CRC-FAIL-INT Bit

A logic 1 on NVM-CRC-FAIL-INT bit indicates that the internal NVM data are corrupt. During this condition, all registers in the device are initialized with factory reset values, and any registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset (see *External Reset*) command or cycle power to the device. A permanent failure in the NVM makes the device unusable.

7.3.4 Power-On Reset (POR)

The AFEx39xx family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a POR (boot-up) delay. The default value for all the registers in the AFEx39xx is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels, as indicated in Figure 7-5, to make sure that the internal capacitors discharge and reset the device at power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65 V, a POR does not occur.

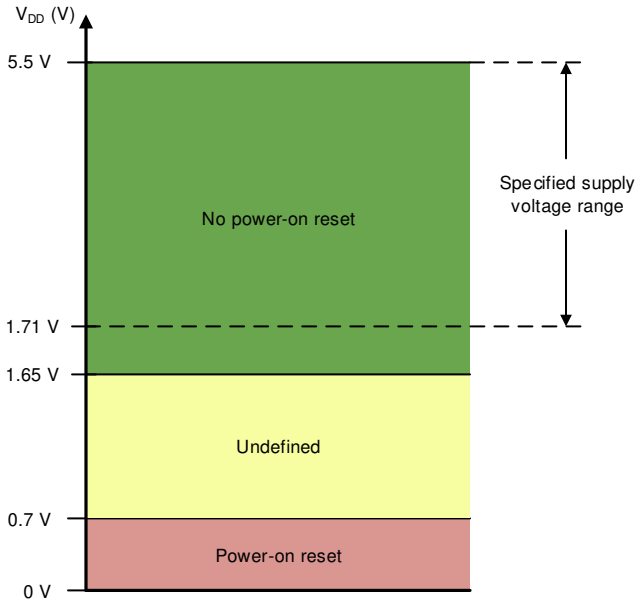


Figure 7-5. Threshold Levels for V_{DD} POR Circuit

7.3.5 External Reset

An external reset to the device can be triggered through the register map. To initiate a device software reset event, write the reserved code 1010b to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event.

7.3.6 Register-Map Lock

The AFEx39xx implement a register-map lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. However, the software reset function through the COMMON-TRIGGER register is not blocked when using I^2C interface. To bypass the DEV-LOCK setting, write 0101b to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

7.4 Device Functional Modes

7.4.1 Voltage-Output Mode

The voltage-output mode for the DAC channel can be entered by selecting the power-up option in the VOUT-PDN-x fields in the COMMON-CONFIG register. Short the OUTx and FBx pins of respective channels externally for closed-loop amplifier output. An open FBx pin saturates the amplifier output. To achieve the desired voltage output, select the correct reference option and select the amplifier gain for the required output range for the respective channels.

7.4.2 Voltage Reference and DAC Transfer Function

There are three voltage reference options possible with the AFEx39xx: internal reference, external reference, and the power supply as reference, as shown in Figure 7-6. The DAC and ADC transfer functions in the voltage input/output and comparator modes change based on the voltage reference selection.

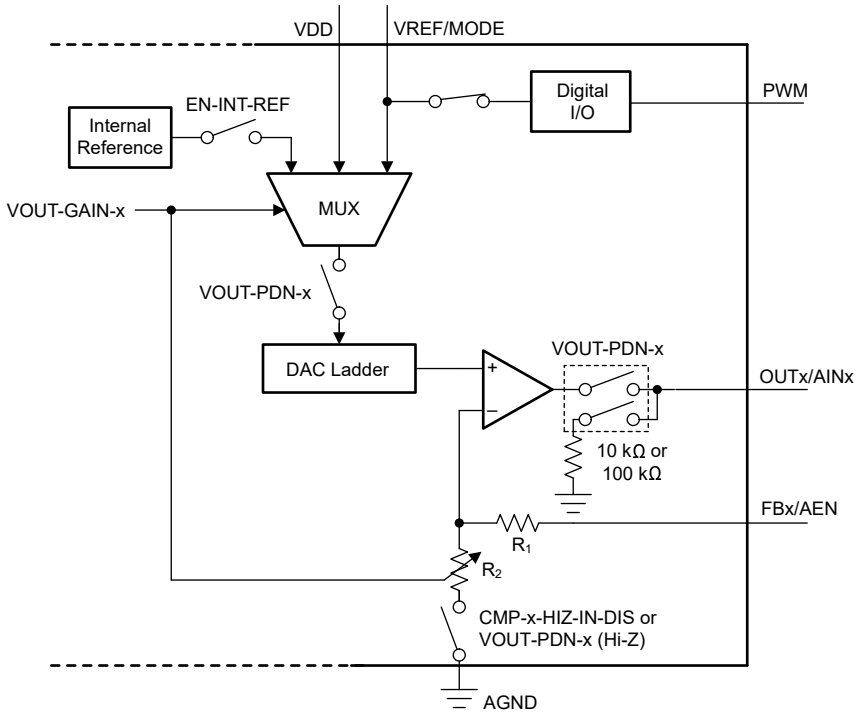


Figure 7-6. Voltage Reference Selection and Power-Down Logic

7.4.2.1 Power-Supply as Reference

By default, the AFEx39xx operate with the power-supply pin (VDD) as a reference. Equation 1 shows DAC transfer function when the power-supply pin is used as reference. The gain at the output stage is always 1 ×.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{DD} \quad (1)$$

where:

- N is the resolution in bits, 8 bits for AFE439A2,10 bits for AFE539A4, and 12 bits for AFE639D2.
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{DD} is used as the DAC reference voltage.

7.4.2.2 Internal Reference

The AFEx39xx contain an internal reference that is disabled by default. To enable the internal reference, write 1 to bit EN-INT-REF in the COMMON-CONFIG register. The internal reference generates a fixed 1.21-V voltage (typical). Use the VOUT-GAIN-x field in the DAC-x-VOUT-CMP-CONFIG register to achieve gains of 1.5 ×, 2 ×, 3 ×, or 4 × for the DAC output voltage (V_{OUT}). Equation 2 shows DAC transfer function using the internal reference.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \times GAIN \quad (2)$$

where:

- N is the resolution in bits, 8 bits for AFE439A2,10 bits for AFE539A4, and 12 bits for AFE639D2.
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the internal reference voltage = 1.21 V.
- GAIN = 1.5 ×, 2 ×, 3 ×, or 4 ×, based on VOUT-GAIN-x bits.

7.4.2.3 External Reference

The AFEx39xx provide an external reference input. Select the external reference option by configuring the VOUT-GAIN-x field in the DAC-x-VOUT-CMP-CONFIG register appropriately. The external reference can be between 1.8 V and VDD. Equation 3 shows DAC transfer function when the external reference is used.

Note

The external reference must be less than VDD in both transient and steady-state conditions. Therefore, the external reference must ramp up after VDD and ramp down before VDD.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \quad (3)$$

where:

- N is the resolution in bits, 8 bits for AFE439A2,10 bits for AFE539A4, and 12 bits for AFE639D2.
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the external reference voltage.

7.4.3 Comparator Mode

A DAC channel is configured as programmable comparator by making the output amplifier open loop. To enter the comparator mode for a channel, write 1 to the CMP-x-EN bit in the respective DAC-x-VOUT-CMP-CONFIG register. The comparator output can be configured as push-pull or open-drain using the CMP-x-OD-EN bit. To invert the comparator output, write 1 to the CMP-x-INV-EN bit. The AINx pin has a finite impedance. By default, the AINx pin is in the high-impedance mode. To disable high-impedance on the AINx pin, write 1 to the CMP-x-HIZ-IN-DIS bit.

Note

Table 7-2 provides the comparator input range limits. Any higher input voltage is clipped.

7.4.4 Analog-to-Digital Converter (ADC) Mode

AFE439A2 and AFE539A4 support integrated ADC. The ADC is controlled by the state-machine in these devices. The transfer function of the ADC is given in Equation 4.

$$\text{ADC\_DATA} = \left(\text{INTEGER}\right)\left(\frac{V_{IN}}{V_{FS}}\right) \times 2^{N} \tag{4}$$

where

- ADC_DATA is the output of the ADC available to the state machine and is limited to (2^N–1).
- V_{IN} is the input voltage at the AINx pin.
- α is the attenuation factor at the ADC input.
- V_{FS} is the full-scale input voltage as provided in Table 7-2.
- N is the number of ADC bits, that is 8 bits for AFE439A2 and 10 bits for AFE539A4.
- (INTEGER) denotes integer division.

Table 7-2. Full Scale Analog Input (V_{FS})

REFERENCE (VREF)	GAIN	V_{FS} (Hi-Z INPUT MODE)	V_{FS} (FINITE IMPEDANCE INPUT MODE)
Power supply	1 ×	VDD / 3	VDD
External	1 ×	VREF / 3	VREF
Internal	1.5 ×	(VREF × GAIN) / 3	VREF × GAIN
	2 ×	(VREF × GAIN) / 3	VREF × GAIN
	3 ×	(VREF × GAIN) / 6	(VREF × GAIN) / 2
	4 ×	(VREF × GAIN) / 6	(VREF × GAIN) / 2

7.4.5 Pulse-Width Modulation (PWM)

The AFE439A2 provides a 7-bit duty-cycle PWM output on the SDA/SCLK/PWM pin. Pull the VREF/MODE pin high to enable PWM functionality. Table 7-3 lists all the possible PWM frequency configurations.

Table 7-3. PWM Frequency Configuration

SRAM REGISTER	PWM-FREQUENCY	PWM FREQUENCY (kHz)	DUTY CYCLE (%) FOR CODE 1	DUTY CYCLE (%) FOR CODE 126
PWM-FREQUENCY (0x21[4:0])(1)	0	Invalid	N/A	N/A
	1	48.828	4.88	95.12
	2	24.414	2.44	97.56
	3	16.276	1.63	98.37
	4	12.207	1.22	98.44
	5	8.138	0.81	98.44
	6	6.104	0.78	98.44
	7	3.052	0.78	98.44
	8	2.035	0.78	98.44
	9	1.526	0.78	98.44
	10	1.221	0.78	98.44
	11	1.017	0.78	98.44
	12	0.872	0.78	98.44
	13	0.763	0.78	98.44
	14	0.678	0.78	98.44
	15	0.610	0.78	98.44
	16	0.555	0.78	98.44
	17	0.509	0.78	98.44
	18	0.470	0.78	98.44
	19	0.436	0.78	98.44
	20	0.407	0.78	98.44
	21	0.381	0.78	98.44
	22	0.359	0.78	98.44
	23	0.339	0.78	98.44
	24	0.321	0.78	98.44
	25	0.305	0.78	98.44
	26	0.291	0.78	98.44
	27	0.277	0.78	98.44
	28	0.265	0.78	98.44
	29	0.254	0.78	98.44
	30	0.244	0.78	98.44
	31	0.218	0.78	98.44

(1) The PWM-FREQUENCY shares SRAM location with MIN-OUTPUT (0x21[15:9]). Therefore, both these parameters must be written together.

The duty cycle of the PWM is proportional to the 7-bit code, 0d to 126d. As Table 7-4 shows, the code 127d corresponds to 100% duty cycle. The duty cycle 99.22% (127d/128d) is skipped to achieve 100% duty cycle using a 7-bit code. The PWM duty-cycle setting is done by the state machine and is not exposed to the user.

Table 7-4. PWM Duty Cycle Setting

CODE	DUTY-CYCLE	DESCRIPTION
0	0%	Always 0
1	0.78%	Minimum linear duty cycle
x	(x/128)%	*x* is the code between 2d and 125d, both included.
126	98.44%	Maximum linear duty cycle
127	100%	Always 1. The duty cycle 99.22% (127d/128d) is skipped.

7.4.6 Proportional-Integral (PI) Control

7.4.6.1 AFE439A2 PI Control

The AFE439A2 provides a preprogrammed PI controller state machine, as shown in Figure 7-7. ADC channel 0 is used as the input and SDA/SCLK/PWM pin is used as the output. DAC channel 1 is used as a comparator that is used to set the output of PWM output to a value specified by the FIXED-OUTPUT field. Table 7-5 lists all the input/output pin names and functions.

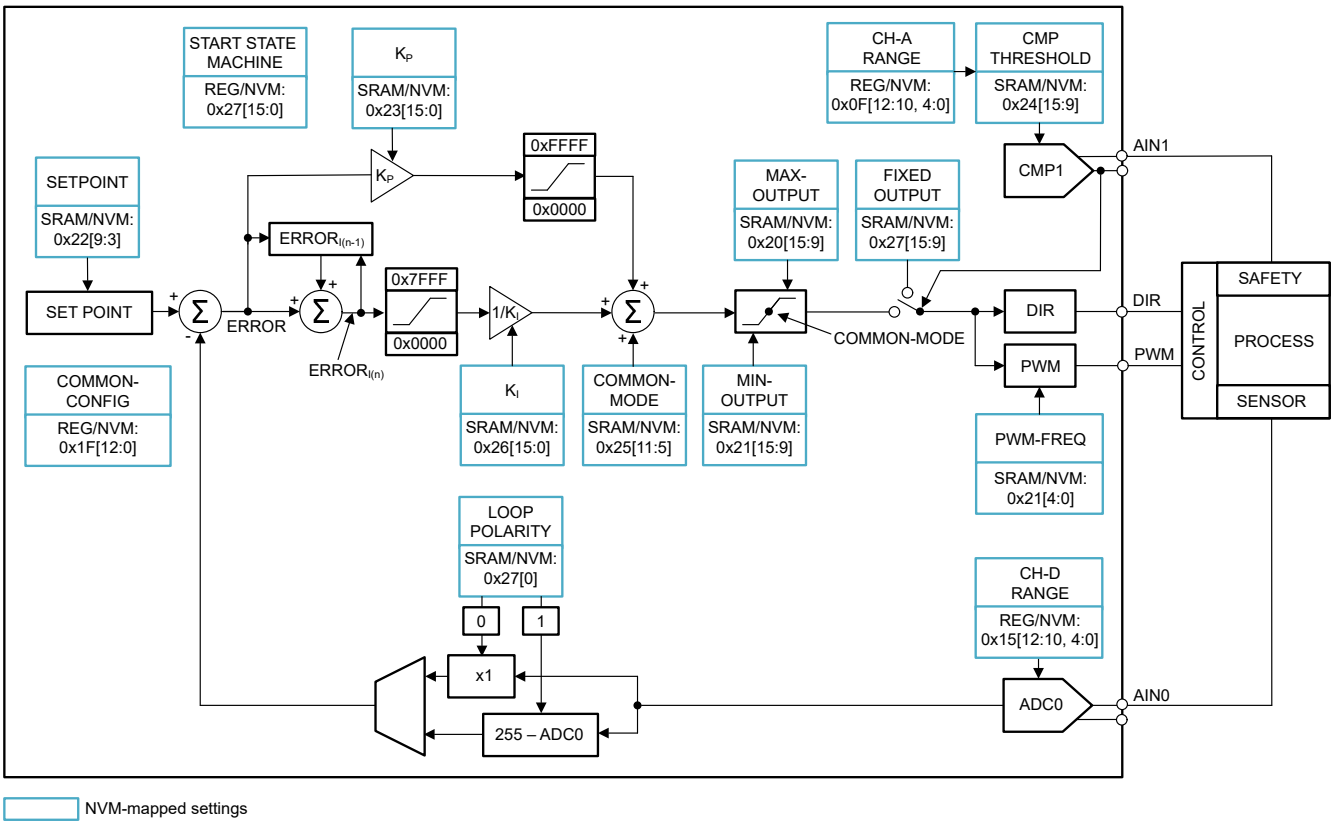


Figure 7-7. PI Controller Architecture of AFE439A2

Table 7-5. PI Controller Pin Definition of AFE439A2

PIN	FUNCTION	RANGE
AIN0	ADC0 input	Hi-Z: 0 V to V_{FS} / 3
AEN	Not used for PI control—connect to VDD using a pullup resistor	Not applicable
AIN1	DAC1 comparator input— connect to AGND if unused for fixed output clamping	See Section 7.4.3
SDA/SCLK/PWM	PWM output—connect to VDD or VIO using a pullup resistor	0 V to VDD or VIO
A0/SDI/DIR	Direction output—connect to VDD or VIO using a pullup resistor	0 V to VDD or VIO

The PI controller provides many configuration parameters. The following Table 7-6list describes the function of each configuration parameter:

Table 7-6. PI Controller Parameters of AFE439A2: Description

REGISTER FIELD NAME	STATIC ADDRESS
SETPOINT	The 8-bit set point to which the ADC input is compared to by the PI controller. The unit of this value is the same as the value at the ADC input. The PI controller minimizes the error between the set point and the sensed ADC data.
K_P	This 16-bit parameter is used as the proportional gain. K_P is multiplied with the instantaneous error. A higher K_P enables the loop to correct the error faster. However, if the external process has a fast response time, a higher K_P can cause system instability.
K_I	This 16-bit parameter is used as inverse integral gain. K_I is inverted and multiplied to the accumulated error. This parameter is important to help minimize the steady-state error under different ambient conditions of the process. A higher K_I means a weaker response to the steady-state error. A smaller K_I can effectively correct the steady-state error, but can also lead to bigger oscillations. The integral function is disabled when $K_I = 0$.
MAX-OUTPUT	This 7-bit value limits the maximum value of the PI controller output.
MIN-OUTPUT	This 7-bit value limits the minimum value of the PI controller output.
COMMON-MODE	This 7-bit value is present at the PI output when the proportional and integral outputs are zero. This parameter is important to help achieve a uniform response for all set points with fixed K_P and K_I settings. COMMON-MODE represents the nominal output to achieve a given set point. Therefore, for best results, use empirically measured COMMON-MODE values for every set point.
LOOP-POLARITY	This 1-bit parameter provides the option to invert the phase of the PI-controller loop. This function is useful when the loop external to the device has an additional phase inversion.
FIXED-OUTPUT	This 8-bit parameter is used to take the output to this predefined value based on the output of comparator channel 2. This function is useful in failure scenarios.
CMP-THRESHOLD	This 8-bit parameter is used to set the threshold for comparator.

Note

An SRAM location is accessed using the SRAM-ADDR and SRAM-DATA registers. Do not access the SRAM registers when the state machine is running. The state machine can be stopped by writing to the STATE-MACHINE-CONFIG0 register. The parameters in Table 7-7 are mapped to NVM. As the digital pins in are mapped to PWM when the VREF/MODE pin is high, the PI controller parameters cannot be read during run time.

Table 7-7. PI Controller Parameters of AFE439A2: Values

REGISTER FIELD NAME	SRAM ADDRESS	STATIC ADDRESS LOCATION	DEFAULT VALUE (16-BIT ALIGNED)
SETPOINT	0x22[9:3]	SRAM	0x0200
K_P	0x23[15:0]	SRAM	0x0032
K_I	0x26[15:0]	SRAM	0x0000
MAX-OUTPUT	0x20[15:9]	SRAM	0x7E00
MIN-OUTPUT	0x21[15:9]	SRAM	0x0000
COMMON-MODE	0x25[11:5]	SRAM	0x0000
LOOP-POLARITY	0x27[0]	SRAM	0x0000
FIXED-OUTPUT	0x27[15:9]	SRAM	0x8000
CMP-THRESHOLD	0x24[15:9]	SRAM	0x8000

Table 7-8 shows the default device configuration.

Table 7-8. Device Configuration for AFE439A2

REGISTER NAME	ADDRESS	DEFAULT VALUE
COMMON-CONFIG	0x1F	0x13F9
DAC-A-VOUT-CMP-CONFIG	0x03	0x0405
DAC-D-VOUT-CMP-CONFIG	0x15	0x0401
STATE-MACHINE-CONFIG0	0x27	0x0003

Follow these steps to configure and operate the PI controller:

1. Stop the state machine by writing 0004h to the STATE-MACHINE-CONFIG0 register.
2. Connect the ADC input, comparator input, and DAC output as shown in Figure 7-7.
3. Pull the VREF/MODE pin low enable programming mode.
4. Write 0 to the START-FUNCTION bit in the COMMON-PWM-TRIG resistor to disable PWM.
5. Write to the COMMON-CONFIG register to enable all the DAC channels.
6. Write to the DAC-x-VOUT-CMP-CONFIG register for respective channels to select the voltage reference and output range for each channel. Configure channels A and D as comparators.
7. Calculate the PWM output range and configure MIN-OUTPUT and MAX-OUTPUT accordingly.

Note

The PWM-FREQUENCY (0x21[4:0]) shares SRAM location with MIN-OUTPUT (0x21[15:9]). Therefore, both these parameters must be written together.

8. Program the PWM frequency as per Table 7-3 together with MIN-OUTPUT.
9. Program the configuration parameters LOOP-POLARITY, CMP-THRESHOLD, and FIXED-OUTPUT as appropriate for the system.
10. Program the initial values of K_P and K_I.
11. Maintain a table to SETPOINT versus COMMON-MODE in the host processor and program these values as required by the system.
12. Configure the STATE-MACHINE-CONFIG0 register to start the state machine.
13. Tune the K_P and K_I iteratively to achieve the best transient and steady-state response.
14. Store the values in the NVM by writing to the NVM-PROG bit in the COMMON-TRIGGER register.
15. Pull the VREF/MODE pin high to enable PWM output.

7.4.6.2 AFE539A4 PI Control

The AFE539A4 provides a preprogrammed PI controller state machine. Figure 7-8 shows the PI controller architecture. ADC channel 0 is used as the input and DAC channel 1 is used as the output. DAC channel 2 is used as a comparator that is used to set the output of DAC channel 1 to a value specified by the FIXED-OUTPUT field. Table 7-9 lists all the input/output pin names and functions.

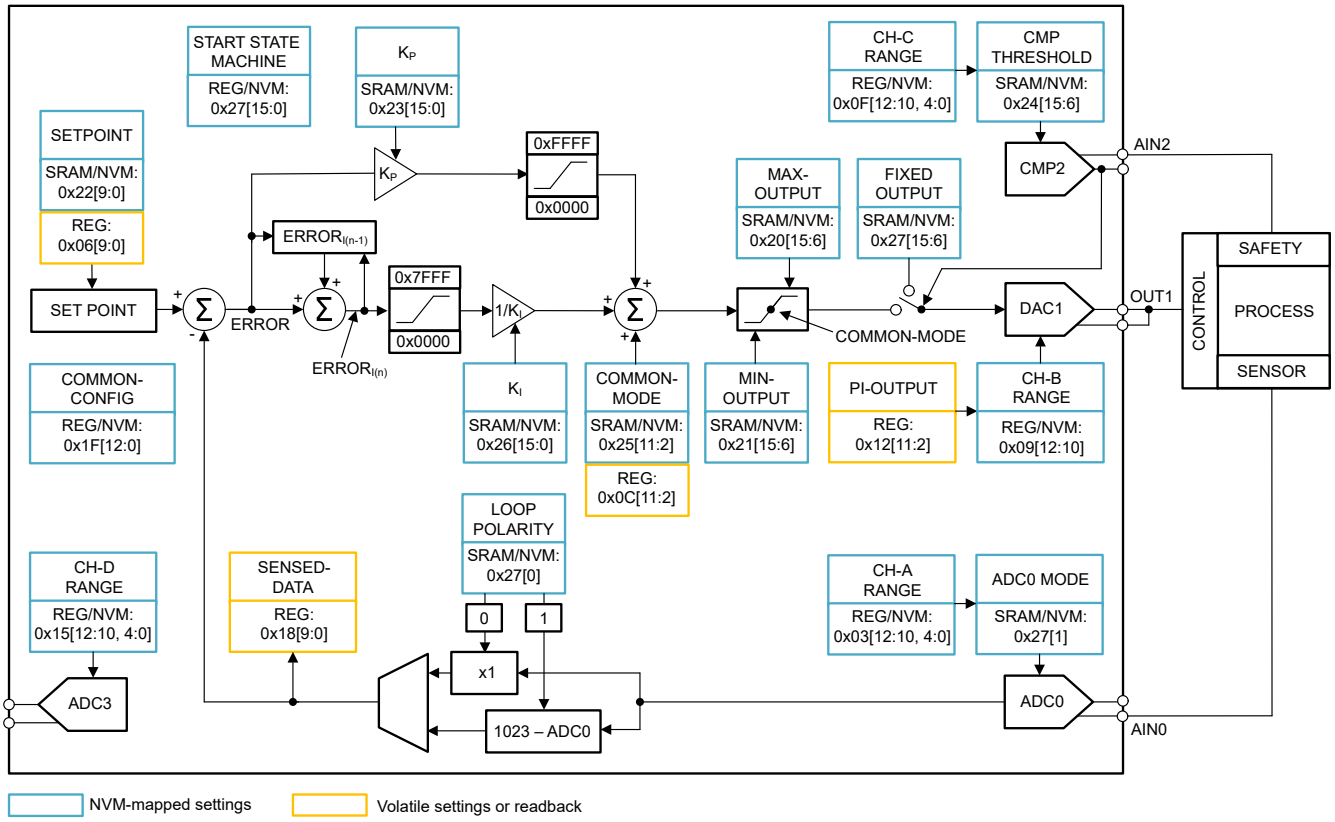


Figure 7-8. PI Controller Architecture

Table 7-9. PI Controller Pin Definition

PIN	FUNCTION	RANGE
AIN0	ADC0 input	Hi-Z: 0 V to V_{FS} / 3 Finite impedance: 0 V to V_{FS}
FB1	Voltage-feedback input for DAC1—connect this pin to OUT1	Not applicable
OUT1	DAC1 voltage output	0 V to V_{FS}
AIN2	DAC2 comparator input— connect to AGND if unused for fixed output clamping	See Section 7.4.3
AEN	Not used for PI control—connect to VDD using a pullup resistor	Not applicable

The PI controller provides many configuration parameters. Table 7-10 describes the function of each configuration parameter:

Table 7-10. PI Controller Parameters for AFE539A4: Description

REGISTER FIELD NAME	STATIC ADDRESS
SETPOINT	The 10-bit set point to which the ADC input is compared by the PI controller. The unit of this value is the same as the value at the ADC input. The PI controller minimizes the error between the set point and the sensed ADC data.
K_P	This 16-bit parameter is used as the proportional gain. K_P is multiplied with the instantaneous error. A higher K_P enables the loop to correct the error faster. However, if the external process has a fast response time, a higher K_P can cause system instability.
K_I	This 16-bit parameter is used as inverse integral gain. K_I is inverted and multiplied to the accumulated error. This parameter is important to help minimize the steady-state error under different ambient conditions of the process. A higher K_I means a weaker response to the steady-state error. A smaller K_I can effectively correct the steady-state error, but can also lead to bigger oscillations. The integral function is disabled when K_I = 0.
MAX-OUTPUT	This 10-bit value limits the maximum value of the PI controller output.
MIN-OUTPUT	This 10-bit value limits the minimum value of the PI controller output.
COMMON-MODE	This 10-bit value is present at the PI output when the proportional and integral outputs are zero. This parameter is very important to help achieve a uniform response for all set points with fixed K_P and K_I settings. COMMON-MODE represents the nominal output to achieve a given set point. Therefore, for best results, use empirically measured COMMON-MODE values for every set point.
LOOP-POLARITY	This 1-bit parameter provides the option to invert the phase of the PI-controller loop. This function is useful when the loop external to the device has an additional phase inversion.
FIXED-OUTPUT	This 10-bit parameter is used to take the output to this predefined value based on the output of comparator. This function is useful in failure scenarios.
ADC-MODE	This 1-bit parameter is used to select between Hi-Z or finite-impedance mode for ADC. ADC-MODE = 0 corresponds to Hi-Z input; ADC-MODE = 1 corresponds to finite-impedance input.
CMP-THRESHOLD	This 10-bit parameter is used to set the threshold for comparator.

Note

An SRAM location is accessed using the SRAM-ADDR and SRAM-DATA registers. Do not access the SRAM registers when the state machine is running. The state machine can be stopped by writing to the STATE-MACHINE-CONFIG0 register. The critical parameters that must be updated in run-time can be accessed using the dynamic locations as listed in Table 7-11. The static (SRAM) locations in Table 7-11 are mapped to NVM. The dynamic locations are not mapped to the NVM. Set all the unassigned bits in the static SRAM locations to 0.

Table 7-11. PI Controller Parameters for AFE539A4: Values

REGISTER FIELD NAME	STATIC ADDRESS	STATIC ADDRESS LOCATION	DEFAULT VALUE (16-BIT ALIGNED)	DYNAMIC ADDRESS	DYNAMIC ADDRESS LOCATION
SETPOINT	0x22[9:0]	SRAM	0x0200	0x06[9:0]	Register
K_P	0x23[15:0]	SRAM	0x0064	N/A	N/A
K_I	0x26[15:0]	SRAM	0x0000	N/A	N/A
MAX-OUTPUT	0x20[15:6]	SRAM	0xFFF0	N/A	N/A
MIN-OUTPUT	0x21[15:6]	SRAM	0x0000	N/A	N/A
COMMON-MODE	0x25[11:2]	SRAM	0x02FF	0x0C[11:2]	Register
LOOP-POLARITY	0x27[0]	SRAM	0x0000	N/A	N/A
FIXED-OUTPUT	0x27[15:6]	SRAM	0x0000	N/A	N/A
ADC-MODE	0x27[1]	SRAM	0x0000	N/A	N/A
CMP-THRESHOLD	0x24[15:6]	SRAM	0x8000	N/A	N/A

Table 7-12 shows the default device configuration.

Table 7-12. Device Configuration for AFE539A4

REGISTER NAME	ADDRESS	DEFAULT VALUE
COMMON-CONFIG	0x1F	0x1249
DAC-A-VOUT-CMP-CONFIG	0x03	0x0401
DAC-B-VOUT-CMP-CONFIG	0x09	0x0400
DAC-C-VOUT-CMP-CONFIG	0x0F	0x0405
DAC-D-VOUT-CMP-CONFIG	0x15	0x0401
STATE-MACHINE-CONFIG0	0x27	0x0003

Follow these steps to configure and operate the PI controller:

1. Stop the state machine by writing 0004h to the STATE-MACHINE-CONFIG0 register.
2. Connect the ADC input, comparator input, and DAC output as shown in Figure 7-8.
3. Write to the COMMON-CONFIG register to enable all the channels.
4. Write to the DAC-x-VOUT-CMP-CONFIG register for respective channels to select the voltage reference and output range for each channel. Configure channels A, C, and D as comparators.
5. Calculate the voltage output range for DAC1 and configure MIN-OUTPUT and MAX-OUTPUT accordingly.
6. Program the configuration parameters LOOP-POLARITY, ADC-MODE, CMP-THRESHOLD, and FIXED-OUTPUT as appropriate for the system.
7. Program the initial values of K_P and K_I.
8. Maintain a table to SETPOINT versus COMMON-MODE in the host processor and program these values as required by the system.
9. Configure the STATE-MACHINE-CONFIG0 register to start the state machine.
10. Tune the K_P and K_I iteratively to achieve the best transient and steady-state response.
11. Store the values in the NVM by writing to the NVM-PROG bit in the COMMON-TRIGGER register.

7.4.6.3 AFE639D2 PI Control

The AFE639D2 provides a preprogrammed PI controller state machine, as shown in Figure 7-9. An external digital temperature sensor is used as the input and DAC channel 0 is used as the output. DAC channel 1 is used as a comparator that is used to set the output of DAC channel 0 to a value specified by the FIXED-OUTPUT field. Table 7-13 lists all the input/output pin names and functions.

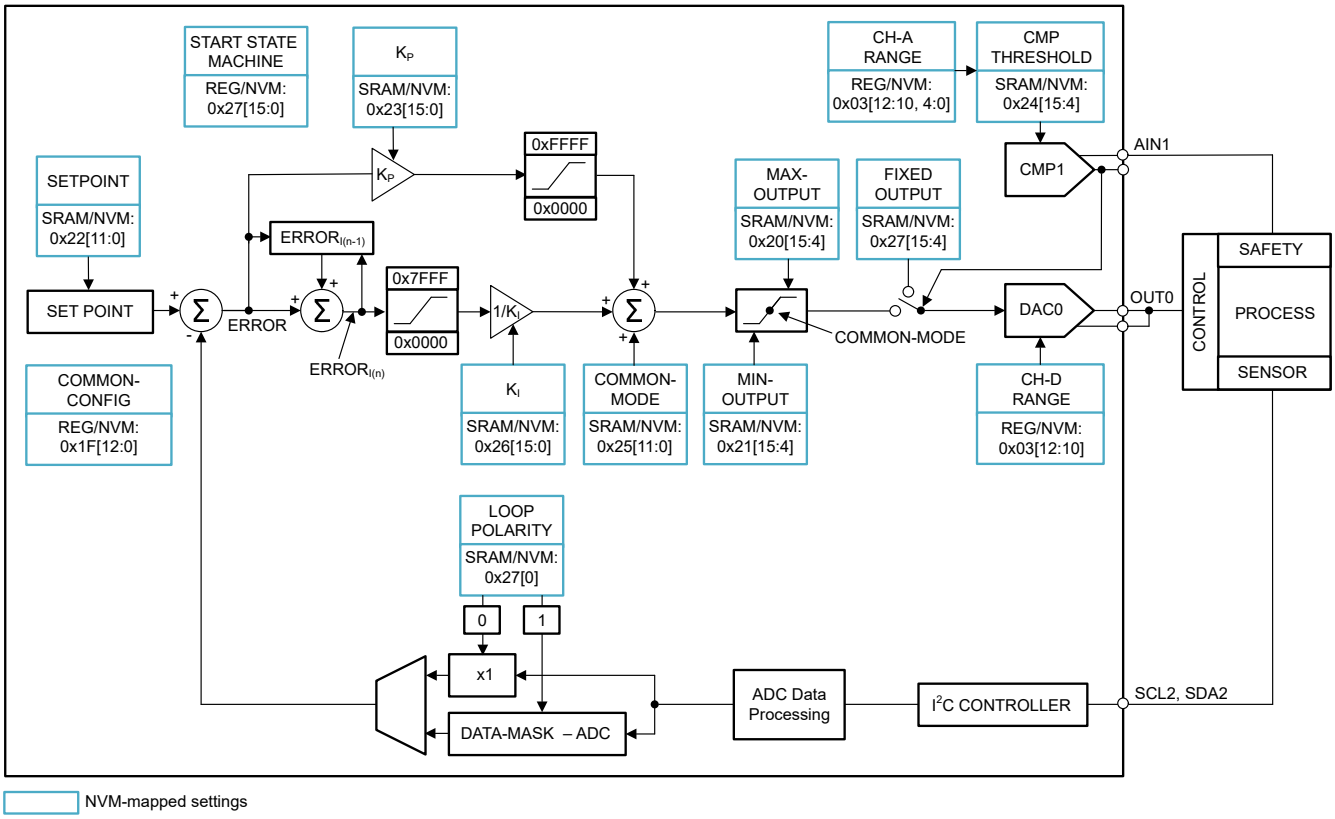


Figure 7-9. PI Controller Architecture of AFE639D2

Table 7-13. PI Controller Pin Definition of AFE639D2

PIN	FUNCTION	RANGE
FB0	Voltage-feedback input for DAC0—connect this pin to OUT0.	Not applicable
OUT0	DAC0 voltage output.	0 V to V_{FS}
AIN1	DAC1 comparator input— connect to AGND if unused for fixed output clamping.	See Section 7.4.3
A0/SDI/SCL2	I^2C controller clock output.	Not applicable
NC/SDO/SDA2	Bidirectional I^2C controller data input/output.	Not applicable

The PI controller provides many configuration parameters. The following list describes the function of each configuration parameter:

Table 7-14. PI Controller Parameters of AFE639D2: Description

PARAMETER	DESCRIPTION
SETPOINT	The 12-bit set point to which the ADC input is compared by the PI controller. The unit of this value is the same as the value at the external ADC input. The PI controller minimizes the error between the set point and the sensed ADC data.
K_P	This 16-bit parameter is used as the proportional gain. K_P is multiplied with the instantaneous error. A higher K_P enables the loop to correct the error faster. However, if the external process has a fast response time, a higher K_P can cause system instability.
K_I	This 16-bit parameter is used as inverse integral gain. K_I is inverted and multiplied to the accumulated error. This parameter is important to help minimize the steady-state error under different ambient conditions of the process. A higher K_I means a weaker response to the steady-state error. A smaller K_I can effectively correct the steady-state error, but can also lead to bigger oscillations. The integral function is disabled when $K_I = 0$.
MAX-OUTPUT	This 12-bit value limits the maximum value of the PI controller output.
MIN-OUTPUT	This 12-bit value limits the minimum value of the PI controller output.
COMMON-MODE	This 12-bit value is present at the PI output when the proportional and integral outputs are zero. This parameter is very important to help achieve a uniform response for all set points with fixed K_P and K_I settings. COMMON-MODE represents the nominal output to achieve a given set point. Therefore, for best results, use empirically measured COMMON-MODE values for every set point.
LOOP-POLARITY	This 1-bit parameter provides the option to invert the phase of the PI-controller loop. This function is useful when the loop external to the device has an additional phase inversion.
FIXED-OUTPUT	This 12-bit parameter is used to take the output to this predefined value based on the output of comparator. This function is useful in failure scenarios.
CMP-THRESHOLD	This 12-bit parameter is used to set the threshold for comparator.
PERIPHERAL-ADDR	The 7-bit I^2C target address of the external temperature sensor or ADC.
DATA-REG-ADDR	The 8-bit address of the temperature or ADC data register.
CONFIG-REG-ADDR	The 8-bit address of the configuration register.
CONFIG-DATA	The 16-bit configuration data for the external temperature sensor or ADC.
ADC-DATA-SHIFT	The number of bits by which the ADC data needs to be shifted to align the data to 16-bit MSB.
SHIFT-DIR	The direction of the ADC data shift. 0 refers to left shift. 1 refers to right shift.
DATA-MASK	The mask that needs to be applied on the data when LOOP-POLARITY is set to 1. The DATA-MASK value must be 0xFFFF right shifted by (16-bits − ADC data length). For a 12-bit ADC, the DATA-MASK must be 0x0FFF.
TWOS-FLAG	1: 16-bit data is in 2's compliment, 0: Data is not 16-bit.

Note

1. An SRAM location is accessed using the SRAM-ADDR and SRAM-DATA registers. Do not access the SRAM registers when the state machine is running. The state machine can be stopped by writing to the STATE-MACHINE-CONFIG0 register. The static (SRAM) locations in Table 7-15 are mapped to NVM.
2. The read or write to the I^2C target channel is not available when the I^2C controller is active (VREF/MODE pin is high).
3. The external I^2C peripheral is configured whenever the state machine is restarted. The VREF/MODE pin must remain high during this time.

Table 7-15. PI Controller Parameters of AFE639D2: Values

REGISTER FIELD NAME	STATIC ADDRESS	STATIC ADDRESS LOCATION	DEFAULT VALUE (16-BIT ALIGNED)
SETPOINT	0x23[15:4]	SRAM	0x0200
K_P	0x24[15:0]	SRAM	0x0064
K_I	0x27[15:0]	SRAM	0x0001
MAX-OUTPUT	0x21[15:4]	SRAM	0x7FC0
MIN-OUTPUT	0x22[15:4]	SRAM	0x0000
COMMON-MODE	0x26[11:0]	SRAM	0x8000
LOOP-POLARITY	0x28[0]	SRAM	0x0000
FIXED-OUTPUT	0x28[15:4]	SRAM	0x8000
CMP-THRESHOLD	0x25[15:4]	SRAM	0x8000
PERIPHERAL-ADDR	0x29[14:8]	Register	0xC800
DATA-REG-ADDR	0x29[7:0]	SRAM	0x0000
CONFIG-REG-ADDR	0x2A[7:0]	SRAM	0x0001
CONFIG-DATA	0x2B[15:0]	SRAM	0x0220
ADC-DATA-SHIFT	0x2C[0]	SRAM	0x0000
SHIFT-DIR	0x2D[0]	SRAM	0x0001
DATA-MASK	0x2E[15:0]	SRAM	0xFFFF
TWOS-FLAG	0x2F[0]	SRAM	0x0001

Table 7-16. Device Configuration for AFE639D2

REGISTER NAME	ADDRESS	DEFAULT VALUE
COMMON-CONFIG	0x1F	0x13F9
DAC-A-VOUT-CMP-CONFIG	0x03	0x0401
DAC-D-VOUT-CMP-CONFIG	0x15	0x0400
STATE-MACHINE-CONFIG0	0x27	0x0003

Table 7-16 shows the default device configuration. Follow these steps to configure and operate the PI controller:

1. Stop the state machine by writing 0004h to the STATE-MACHINE-CONFIG0 register.
2. Connect the external temperature sensor or ADC input, comparator input, and DAC output as shown in Figure 7-9.
3. Pull the VREF/MODE pin low to enable programming mode.
4. Write to the COMMON-CONFIG register to enable all the DAC channels.
5. Write to the DAC-x-VOUT-CMP-CONFIG register for respective channels to select the voltage reference and output range for each channel. Configure channel D as a comparator.
6. Calculate the voltage output range for DAC0 and configure MIN-OUTPUT and MAX-OUTPUT accordingly.
7. Program the configuration parameters LOOP-POLARITY, CMP-THRESHOLD, and FIXED-OUTPUT as appropriate for the system.
8. Configure the I^2C peripheral parameters based on the selected peripheral device.
9. Program the initial values of K_P and K_I.
10. Maintain a table to SETPOINT versus COMMON-MODE in the host processor and program these values as required by the system.
11. Configure the STATE-MACHINE-CONFIG0 register to start the state machine.
12. Tune the K_P and K_I iteratively to achieve the best transient and steady-state response.
13. Store the values in the NVM by writing to the NVM-PROG bit in the COMMON-TRIGGER register.
14. Pull the VREF/MODE pin high immediately to enable the I^2C controller configure the peripheral device.

7.5 Programming

7.5.1 SPI Programming Mode

An SPI access cycle for AFEx39xx is initiated by asserting the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. The SPI frame for AFEx39xx is 24 bits long. Therefore, the $\overline{\text{SYNC}}$ pin must stay low for at least 24 SCLK falling edges. The access cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. By default, the SDO pin is not enabled (three-wire SPI). In the three-wire SPI mode, if the access cycle contains more than the minimum clock edges, only the first 24 bits are used by the device. When $\overline{\text{SYNC}}$ is high, the SCLK and SDI signals are blocked, and SDO becomes Hi-Z to allow data readback from other devices connected on the bus.

Table 7-17 and Figure 7-10 describe the format for the 24-bit SPI access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 7-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

Table 7-17. SPI Read/Write Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Identifies the communication as a read or write command to the address register: R/$\overline{\text{W}}$ = 0 sets a write operation. R/$\overline{\text{W}}$ = 1 sets a read operation
22-16	A[6:0]	Register address: specifies the register to be accessed during the read or write operation
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are *don't care* values.

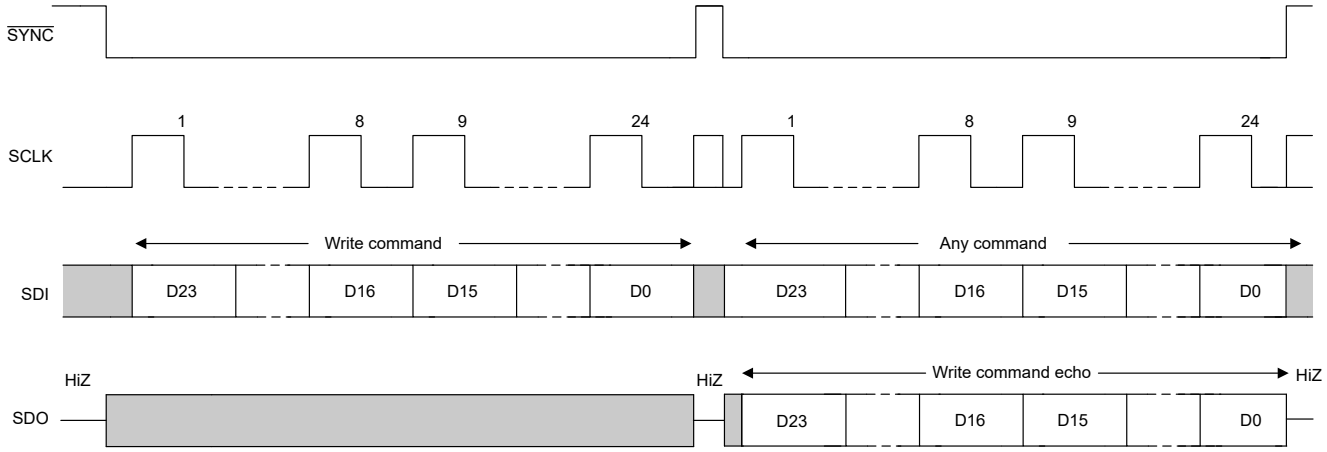


Figure 7-10. SPI Write Cycle

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit in the INTERFACE-CONFIG register. This configuration is called four-wire SPI. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. The output data format is shown in Table 7-18 and Figure 7-11. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit, as shown in Figure 6-3.

Table 7-18. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Echo R/$\overline{\text{W}}$ from previous access cycle
22-16	A[6:0]	Echo register address from previous access cycle
15-0	DI[15:0]	Readback data requested on previous access cycle

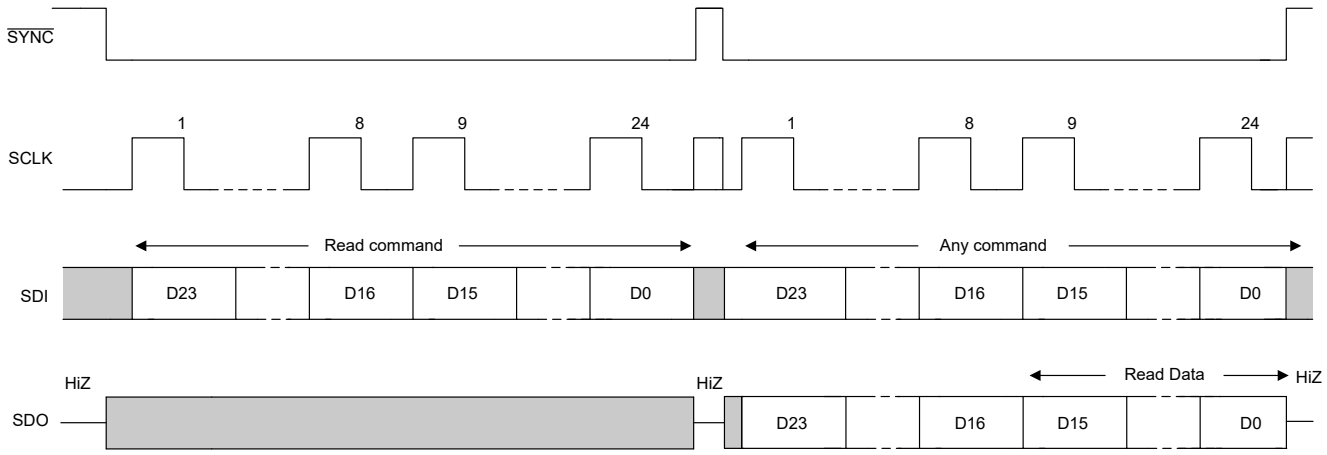


Figure 7-11. SPI Read Cycle

The daisy-chain operation is also enabled with the SDO pin. In daisy-chain mode, multiple devices are connected in a *chain* with the SDO pin of one device is connected to SDI pin of the following device, as shown in Figure 7-12. The SPI host drives the SDI pin of the first device in the chain. The SDO pin of the last device in the chain is connected to the POCI pin of the SPI host. In four-wire SPI mode, if the access cycle contains multiples of 24 clock edges, only the last 24 bits are used by the device first device in the chain. If the access cycle contains clock edges that are not in multiples of 24, the SPI packet is ignored by the device. Figure 7-13 describes the packet format for the daisy-chain write cycle.

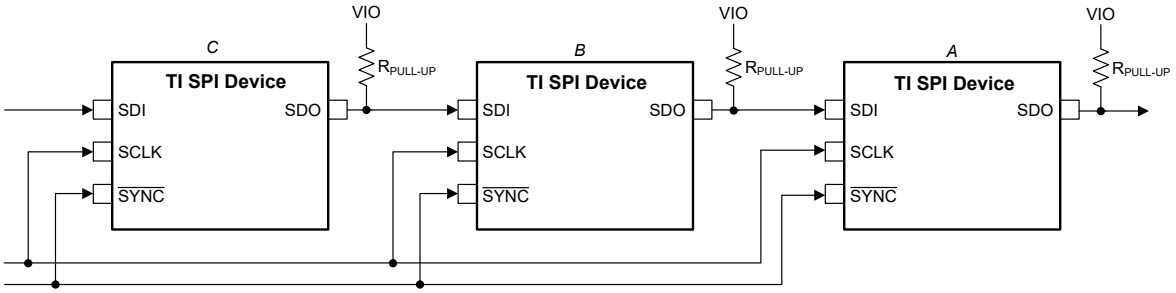


Figure 7-12. SPI Daisy-Chain Connection

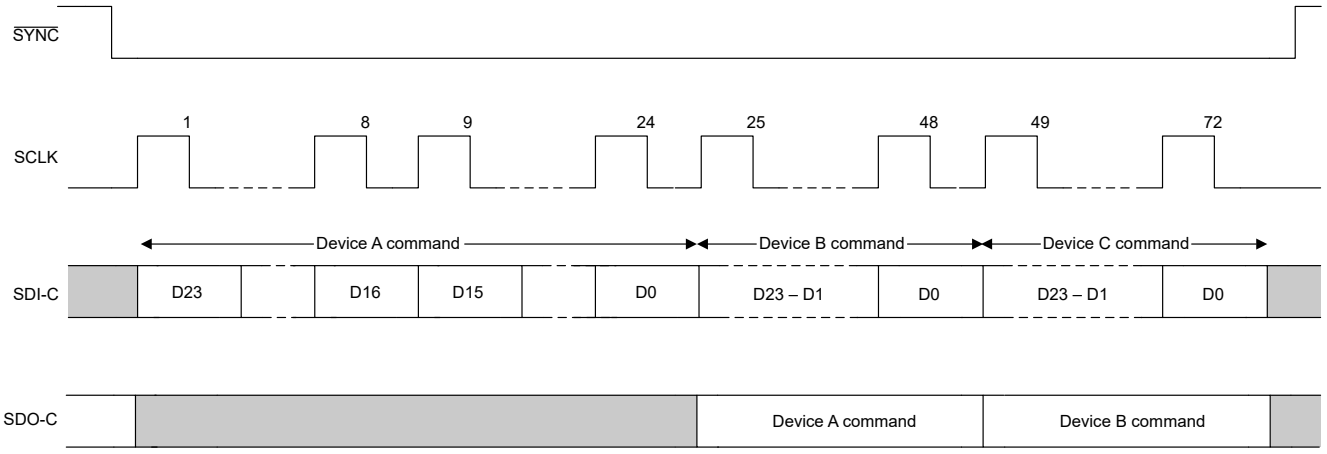


Figure 7-13. SPI Daisy-Chain Write Cycle

7.5.2 I²C Programming Mode

The AFEx39xx devices have a 2-wire serial interface (SCL and SDA), and one address pin (A0), as shown in the pin diagram in the *Pin Configuration and Functions* section. The I²C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through the open drain I/O pins, SDA and SCL.

The I²C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller generates the SCL signal. The controller also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller on an I²C bus is typically a microcontroller or digital signal processor (DSP). The AFEx39xx family operates as a target on the I²C bus. A target acknowledges controller commands, and upon controller control, receives or transmits data.

Typically, the AFEx39xx family operates as a target receiver. A controller writes to the AFEx39xx, a target receiver. However, if a controller requires the AFEx39xx internal register data, the AFEx39xx operate as a target transmitter. In this case, the controller reads from the AFEx39xx. According to I²C terminology, read and write refer to the controller.

The AFEx39xx family supports the following data transfer modes:

- Standard mode (100Kbps)
- Fast mode (400Kbps)
- Fast mode plus (1.0Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current is 3 mA; similar to the case of standard and fast modes. The AFEx39xx family supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle, as shown in Figure 7-14.

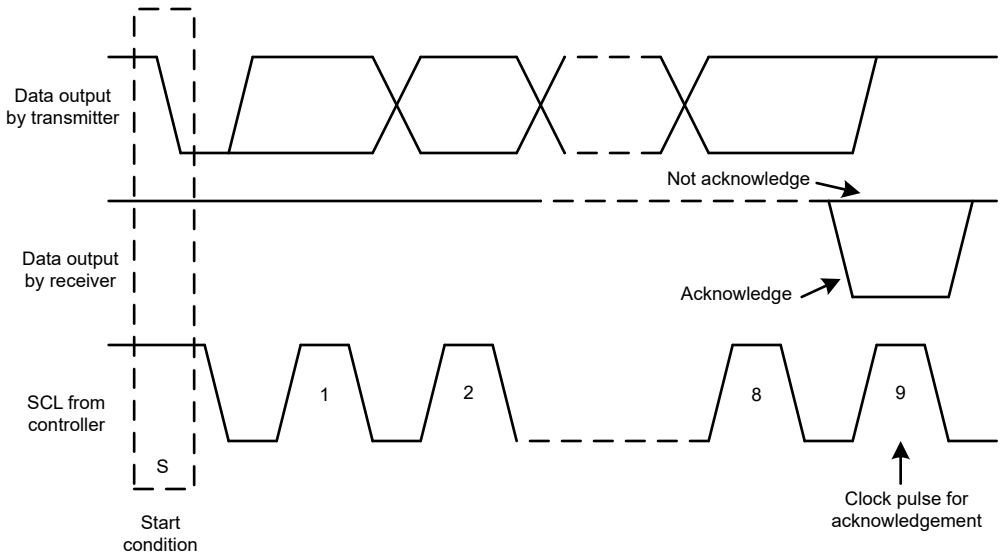


Figure 7-14. Acknowledge and Not Acknowledge on the I²C Bus

7.5.2.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The controller initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 7-15. All I^2C-compatible devices recognize a start condition.
2. The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/$\overline{W}$) on the SDA line. During all transmissions, the controller makes sure that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in Figure 7-16. All devices recognize the address sent by the controller and compare the address to the respective internal fixed address. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle, as shown in Figure 7-14. When the controller detects this acknowledge, the communication link with a target has been established.
3. The controller generates further SCL cycles to transmit (R/$\overline{W}$ bit 0) or receive (R/$\overline{W}$ bit 1) data to the target. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the controller or by the target, depending on which is the receiver. The 9-bit valid data sequences consists of eight data bits and one acknowledge-bit, and can continue as long as necessary.
4. To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high, as shown in Figure 7-15. This action releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all target devices then wait for a start condition followed by a matching address.

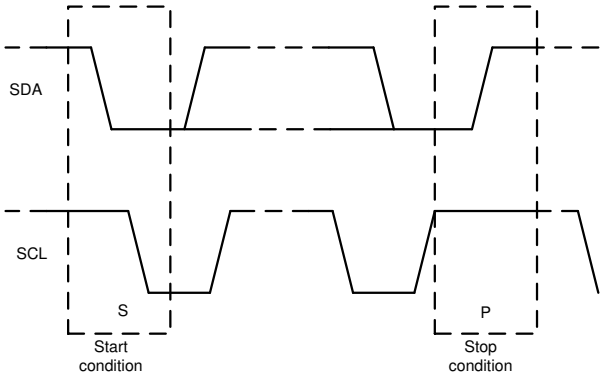


Figure 7-15. Start and Stop Conditions

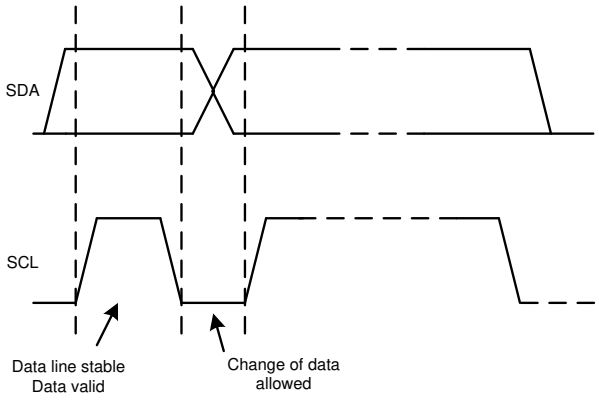


Figure 7-16. Bit Transfer on the I^2C Bus

7.5.2.2 I²C Update Sequence

For a single update, the AFEx39xx require a start condition, a valid I²C address byte, a command byte, and two data bytes, as listed in Table 7-19.

Table 7-19. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte Section 7.5.2.2.1				Command byte Section 7.5.2.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the AFEx39xx acknowledge the byte by pulling the SDA line low during the high period of a single clock pulse, as shown in Figure 7-17. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I²C address byte selects the AFEx39xx.

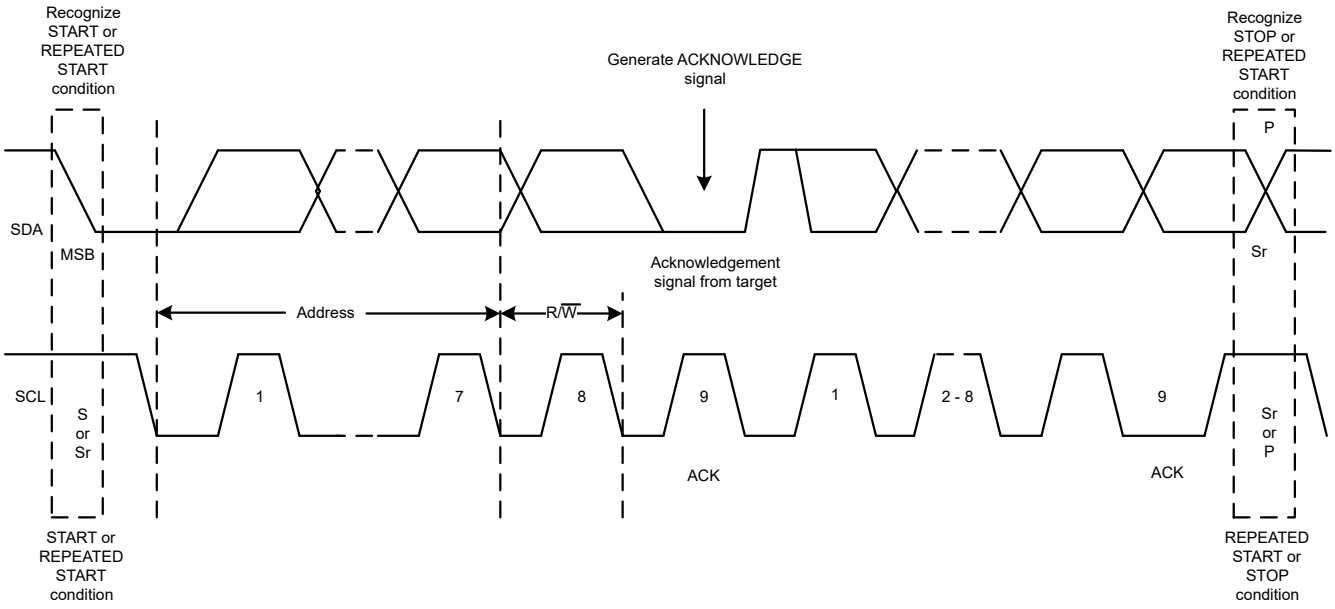


Figure 7-17. I²C Bus Protocol

The command byte sets the operating mode of the selected AFEx39xx device. For a data update to occur when the operating mode is selected by this byte, the AFEx39xx device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The AFEx39xx device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 10 kSPS. Using fast mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 25 kSPS. When a stop condition is received, the AFEx39xx device releases the I²C bus and awaits a new start condition.

7.5.2.2.1 Address Byte

The address byte, as shown in Table 7-20, is the first byte received from the controller device following the start condition. The first four bits (MSBs) of the address are factory preset to 1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to Table 7-21.

Table 7-20. Address Byte

COMMENT	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/$\overline{W}$
General address	1	0	0	1	See Table 7-21 (target address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

Table 7-21. Address Format

TARGET ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

The AFEx39xx supports broadcast addressing, which is used for synchronously updating or powering down multiple AFEx39xx devices. When the broadcast address is used, the AFEx39xx responds regardless of the address pin state. Broadcast is supported only in write mode.

7.5.2.2.2 Command Byte

Table 7-24 lists the command byte in the ADDRESS column.

7.5.2.3 I²C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a target address and the R/$\overline{W}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the target address and the R/$\overline{W}$ bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The controller must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

The broadcast address cannot be used for reading.

Table 7-22. Read Sequence

S	MSB	…	R/$\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/$\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	ADDRESS BYTE Section 7.5.2.2.1				COMMAND BYTE Section 7.5.2.2.2				Sr	ADDRESS BYTE Section 7.5.2.2.1				MSDB				LSDB			
From Controller				Target	From Controller			Target	From Controller				Target	From Target			Controller	From Target			Controller

7.6 Register Maps

Table 7-23. Register Map

REGISTER	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
NOP	NOP															
DAC-X-VOUT-CMP-CONFIG	X			VOUT-GAIN-x			X							CMP-x-HIZ-IN-DIS	CMP-x-INV-EN	CMP-x-EN
COMMON-CONFIG	RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	VOUT-PDN-D		RESERVED	VOUT-PDN-C		RESERVED	VOUT-PDN-B		RESERVED	VOUT-PDN-A		RESERVED
COMMON-TRIGGER	DEV-UNLOCK				RESET				RESERVED						NVM-PROG	NVM-RELOAD
COMMON-PWM-TRIG	RESERVED															START-FUNCTION
GENERAL-STATUS	NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	RESERVED					NVM-BUSY	DEVICE-ID						VERSION-ID	
INTERFACE-CONFIG	X			TIMEOUT-EN	X			RESERVED	X					FSDO-EN	X	SDO-EN
STATE-MACHINE-CONFIG0	RESERVED													SM-ABORT	SM-START	SM-EN
STATE-MACHINE-CONFIG-1	RESERVED	PERIPHERAL-ADDR							X							
SRAM-CONFIG	X								SRAM-ADDR							
SRAM-DATA	SRAM-DATA															

Note: Shaded cells indicate the register bits or fields that are stored in NVM.

Note: X = Don't care.

Table 7-24. Register Names

I²C OR SPI ADDRESS (COMMAND BYTE)	REGISTER NAME	SECTION
00h	NOP	Section 7.6.1
03h	DAC-A-VOUT-CMP-CONFIG	Section 7.6.2
09h	DAC-B-VOUT-CMP-CONFIG	Section 7.6.2
0Fh	DAC-C-VOUT-CMP-CONFIG	Section 7.6.2
15h	DAC-D-VOUT-CMP-CONFIG	Section 7.6.2
1Fh	COMMON-CONFIG	Section 7.6.3
20h	COMMON-TRIGGER	Section 7.6.4
21h	COMMON-PWM-TRIG	Section 7.6.5
22h	GENERAL-STATUS	Section 7.6.6
26h	INTERFACE-CONFIG	Section 7.6.7
27h	STATE-MACHINE-CONFIG0	Section 7.6.8
29h	STATE-MACHINE-CONFIG1	Section 7.6.9
2Bh	SRAM-CONFIG	Section 7.6.10
2Ch	SRAM-DATA	Section 7.6.11

7.6.1 NOP Register (address = 00h) [reset = 0000h]

Figure 7-18. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R/W-0h															

Table 7-25. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	R/W	0000h	No operation

7.6.2 DAC-x-VOUT-CMP-CONFIG Register (address = 03h, 09h, 0Fh, 15h)

Note

A corresponds to the data converter channel on pins (11, 12). B corresponds to the channel on pins (9, 10). C corresponds to the channel on pins (3, 4). D corresponds to the channel on pins (1, 2).

Figure 7-19. DAC-x-VOUT-CMP-CONFIG Register (x= A, B, C, D)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			VOUT-GAIN-x			X							CMP-x-HIZ-IN-DIS	CMP-x-INV-EN	CMP-x-EN
X-0h			R/W-0h			X-0h							R/W-0h	R/W-0h	R/W-0h

Table 7-26. DAC-x-VOUT-CMP-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12-10	VOUT-GAIN-x	R/W	0h	000: Gain = 1 ×, external reference on VREF/MODE pin 001: Gain = 1 ×, VDD as reference 010: Gain = 1.5 ×, internal reference 011: Gain = 2 ×, internal reference 100: Gain = 3 ×, internal reference 101: Gain = 4 ×, internal reference Others: Invalid
9-3	X	X	0h	Don't care
2	CMP-x-HIZ-IN-DIS	R/W	0	0: AINx input has high-impedance. Input voltage range is limited. 1: AINx input is connected to resistor divider and has finite impedance. Input voltage range is same as full-scale.
1	CMP-x-INV-EN	R/W	0	0: Don't invert the comparator output 1: Invert the comparator output
0	CMP-x-EN	R/W	0	0: Disable comparator mode 1: Enable comparator mode. Current-output must be in power-down. Voltage-output mode must be enabled.

7.6.3 COMMON-CONFIG Register (address = 1Fh)

Note

A corresponds to the data converter channel on pins (11, 12). B corresponds to the channel on pins (9, 10). C corresponds to the channel on pins (3, 4). D corresponds to the channel on pins (1, 2).

Figure 7-20. COMMON-CONFIG Register

15	14	13	12	11 10	9	8 7	6	5 4	3	2 1	0
RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	VOUT-PDN-D	RESERVED	VOUT-PDN-C	RESERVED	VOUT-PDN-B	RESERVED	VOUT-PDN-A	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W	R/W-1b	R/W	R/W-1b	R/W	R/W-1b	R/W	R/W-1b

Table 7-27. COMMON-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0	Always write 0.
14	DEV-LOCK	R/W	0	0: Device not locked. 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	RESERVED	R/W	0	Always write 0.
12	EN-INT-REF	R/W	0	0: Disable internal reference. 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11-10, 8-7, 5-4, 2-1	VOUT-PDN-x	R/W	--	00: Power-up VOUT-x 01: Power-down VOUT-x with 10 kΩ to AGND 10: Power-down VOUT-x with 100 kΩ to AGND 11: Power-down VOUT-x with Hi-Z to AGND
9, 6, 3, 0	RESERVED	R/W	1	Always write 1.

7.6.4 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

Figure 7-21. COMMON-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV-UNLOCK				RESET				RESERVED						NVM-PROG	NVM-RELOAD
R/W-0h				R/W-0h				R/W-0h						R/W-0h	R/W-0h

Table 7-28. COMMON-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DEV-UNLOCK	R/W	0000	0101: Device unlocking password. To unlock device, write this unlock password first, followed by a write 0 to the DEV-LOCK bit in the COMMON-CONFIG register. Others: Don't care
11-8	RESET	W	0000	1010: POR reset triggered. This bit self-resets. Others: Don't care
7-2	RESERVED	R/W	0	Always write 00h.
1	NVM-PROG	R/W	0	0: NVM write not triggered 1: NVM write triggered. This bit self-resets.
0	NVM-RELOAD	R/W	0	0: NVM reload not triggered 1: Reload data from NVM to register map. This bit self-resets.

7.6.5 COMMON-PWM-TRIG Register (address = 21h) [reset = 0000h]

Figure 7-22. COMMON-PWM-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															START-FUNCTION
R/W-0000h															R/W-0h

Table 7-29. COMMON-PWM-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	W	0	Always write 0000h.
0	START-FUNCTION	R/W	0	0: Stop PWM generation on AFE439A2. 1: Invalid. The state machine write to this bit automatically.

7.6.6 GENERAL-STATUS Register (address = 22h) [reset = 00h, DEVICE-ID, VERSION-ID]

Figure 7-23. GENERAL-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X					NVM-BUSY	DEVICE-ID						VERSION-ID	
R-0h	R-0h	X-0h					X-0h	R						R-0h	

Table 7-30. GENERAL-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0	0: No CRC error in OTP 1: Indicates a failure in OTP loading. A software reset or power-cycle can bring the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0	0: No CRC error in NVM loading 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get original state. A software reset brings the device out of this temporary error condition.
13	X	R	0	Don't care
8	NVM-BUSY	R	0	0: NVM is available for read and write. 1: NVM is not available for read or write.
7-2	DEVICE-ID	R	AFE639D2: 0Dh AFE539A4: 0Ch AFE439A2: 0Eh	Device identifier.
1-0	VERSION-ID	R	00	Version identifier.

7.6.7 INTERFACE-CONFIG Register (address = 26h) [reset = 0000h]

Figure 7-24. INTERFACE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			TIMEOUT-EN	X									FSDO-EN	X	SDO-EN
X-0h			R/W-0h	X-0h									R/W-0h	X-0h	R/W-0h

Table 7-31. INTERFACE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care.
12	TIMEOUT-EN	R/W	0	0: I²C timeout disabled. 1: I²C timeout enabled.
11-3	X	X	0h	Don't care.
2	FSDO-EN	R/W	0	0: Fast SDO disabled. 1: Fast SDO enabled.
1	X	X	0	Don't care.
0	SDO-EN	R/W	0	0: SDO disabled. 1: SDO enabled.

7.6.8 STATE-MACHINE-CONFIG0 Register (address = 27h) [reset = 0003h]

Figure 7-25. STATE-MACHINE-CONFIG0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SM-ABORT	SM-START	SM-EN
R/W-0h													R/W-0h	R/W-1h	R/W-1h

Table 7-32. STATE-MACHINE-CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R/W	0000h	Always write 0.
2	SM-ABORT	R/W	0	0: State machine not aborted. 1: State machine aborted.
1	SM-START	R/W	1	0: State machine stopped. 1: State machine started. The state machine must be enabled using the SM-EN bit.
0	SM-EN	R/W	1	0: State machine disabled. 1: State machine enabled.

7.6.9 STATE-MACHINE-CONFIG1 Register (address = 29h) [reset = C800h]

Figure 7-26. STATE-MACHINE-CONFIG1 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	PERIPHERAL-ADDR							X							
R/W-1	R/W-48h							X-0h							

Table 7-33. STATE-MACHINE-CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	1	Always write 1.
14-8	PERIPHERAL-ADDR	R/W	48h	7-bit peripheral for I²C controller on AFE639D2.
7-0	X	R/W	0	Don't care

7.6.10 SRAM-CONFIG Register (address = 2Bh) [reset = 0000h]

Figure 7-27. SRAM-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								SRAM-ADDR							
X-00h								R/W-00h							

Table 7-34. SRAM-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X	X	00h	Don't care
7-0	SRAM-ADDR	R/W	00h	8-bit SRAM address. Writing to this register field configures the SRAM address to be accessed next. This address automatically increments after a write to the SRAM.

7.6.11 SRAM-DATA Register (address = 2Ch) [reset = 0000h]

Figure 7-28. SRAM-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM-DATA															
R/W-0000h															

Table 7-35. SRAM-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SRAM-DATA	R/W	0000h	16-bit SRAM data. Data are written to or read from the address configured in the SRAM-CONFIG register.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Follow these guidelines for best performance of the AFEx39xx:

- For voltage output, short the OUTx and FBx pins.
- Connect AEN to VDD using a pullup resistor in the ADC mode.
- The external reference must not exceed VDD, either during transient or steady-state conditions.
- For the best Hi-Z output performance when VDD is off, use a pullup resistor on the VREF/MODE pin to VDD. In case the VDD remains floating during the off condition, place a 100-kΩ resistor to AGND for proper detection of the VDD off condition.
- All the digital outputs are open drain; use external pullup resistors on these pins.
- The interface protocol is detected at power on, and the device locks to the protocol as long as VDD is on.
- When allocating the I^2C addresses in the system in I^2C mode, consider the broadcast address as well.
- I^2C timeout can be enabled for robustness.
- SPI mode is three-wire by default.
- Configure the NC/SDO pin as SDO in the NVM for SPI readback capability.
- The SPI clock speed in readback mode is slower than that in write mode.
- The I^2C controller can only be used for specific external devices that comply with the specified register format.
- The target I^2C readback functionality when the I^2C controller is enabled (VREF/MODE is high). Make the VREF/MODE pin low to enable read and write functionality on the I^2C target interface.

8.2 Typical Application

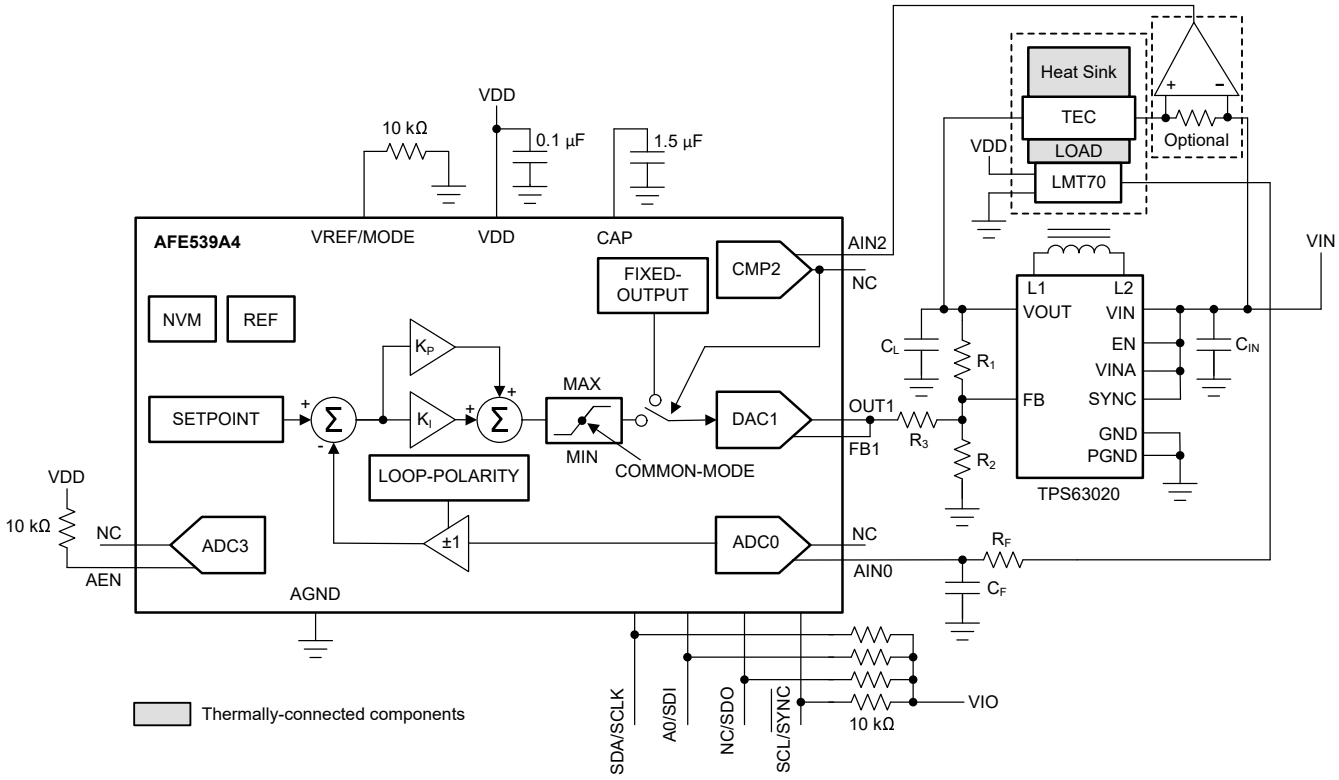


Figure 8-1. TEC Control

A thermoelectric cooling (TEC) circuit is used in many applications, such as laser diode cooling, medical blood analysis and thermal-cycling, central-processing unit (CPU) cooling, portable refrigeration, automotive seat heating, and more. A TEC element is controlled by controlling the voltage across the TEC element using a PI controller. This application example extends the circuit explained in the *Low-Power TEC Driver* application report. Figure 8-1 shows the complete circuit diagram.

8.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
Measured temperature range	–55ºC to +150ºC
AFE output-voltage range	0 V to 1.8 V
Temperature set point	30ºC
Steady-state error	< ±0.5ºC

8.2.2 Detailed Design Procedure

This design example uses the TPS63020, a buck-boost converter, and connects the TEC element between the VIN and VOUT nodes to create bidirectional voltage control of the TEC element. The control voltage to the TPS63020 must be between 0 V and 1.8 V to achieve the full range of TEC current. As shown in Figure 8-1, the temperature is measured using the LMT70, a high-precision, analog temperature sensor. The LMT70 provides a voltage output between 1.38 V and 300 mV for the temperature range of –55ºC to +125ºC. Therefore, configure the PI controller output (DAC1) with the internal reference and a gain of 1.5 ×. Similarly, configure ADC0 to be in Hi-Z input mode (ADC-MODE = 0), with the internal reference, and 4 × gain. This configuration sets ADC0 at a full-scale input (V_{FS}) range of (1.21 V × 4) / 3 = 1.613 V. With 10-bit resolution, 1 LSB of ADC0 code corresponds to (1.613 V / 1024) = 1.58 mV. The response slope of the LMT70 at 30ºC is 5.194 mV/ºC. Therefore, 1 LSB of the ADC0 corresponds to (1.58 / 5.194) = 0.3ºC.

The voltage output of the LMT70 corresponding to the temperature set point of 30ºC is 943.227 mV. Using Equation 4, calculate the SETPOINT input as 598d (0x256). For negative feedback, use an odd number of phase inversions in the feedback loop. The DAC1 output to the TPS63020 output has one phase inversion; the TPS63020 decreases when the DAC1 output increases. The TPS63020 output and the TEC cold-side temperature have the second phase inversion; the TEC cold-side temperature decreases when the TPS63020 output increases. The TEC cold-side and the LMT70 have the third phase inversion; when the TEC cold-side temperature decreases, the LMT70 output voltage increases. The external loop of the AFEx39xx has an odd number of phase inversions; therefore, make sure that the internal PI control loop has no phase inversion. To prevent the phase inversion, configure LOOP-POLARITY = 1. Choose the values of R_F and C_F in Figure 8-1 based on the noise level present in the sensing circuit.

When the output of the comparator is low, the PI controller output enters safe mode. Therefore, the current sense amplifier and the comparator setting must be configured to trigger fallback mode at the desired TEC current limit.

Follow the procedure described in Section 7.4.6.2 to configure the parameters listed in Table 8-2.

Table 8-2. PI Controller Parameters

REGISTER FIELD NAME	STATIC ADDRESS	STATIC ADDRESS LOCATION	CONFIGURED VALUE (16-BIT)	DYNAMIC ADDRESS	DYNAMIC ADDRESS LOCATION
SETPOINT	0x22[9:0]	SRAM	0x0256	0x06[9:0]	Register
K_P	0x23[15:0]	SRAM	0x0FA0	N/A	N/A
K_I	0x26[15:0]	SRAM	0x0001	N/A	N/A
MAX-OUTPUT	0x20[15:6]	SRAM	0xFFC0	N/A	N/A
MIN-OUTPUT	0x21[15:6]	SRAM	0x0000	N/A	N/A
COMMON-MODE	0x25[11:2]	SRAM	0x7FC0	0x0C[11:2]	Register
LOOP-POLARITY	0x27[0]	SRAM	0x0001	N/A	N/A
FIXED-OUTPUT	0x27[15:6]	SRAM	0x0000	N/A	N/A
ADC-MODE	0x27[1]	SRAM	0x0002	N/A	N/A
CMP-THRESHOLD	0x24[15:6]	SRAM	0x7FC0	N/A	N/A

8.2.3 Application Curves

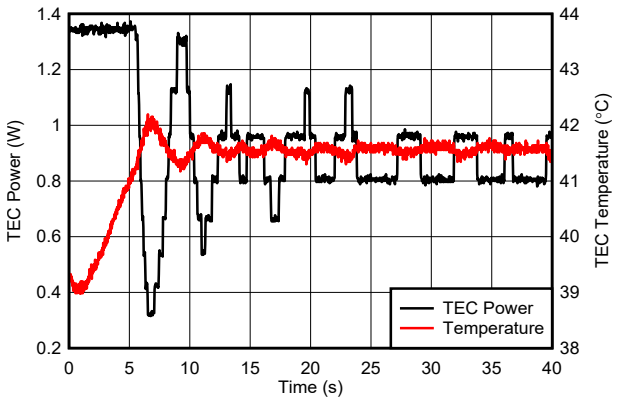


Figure 8-2. TEC Power and TEC Temperature vs Time

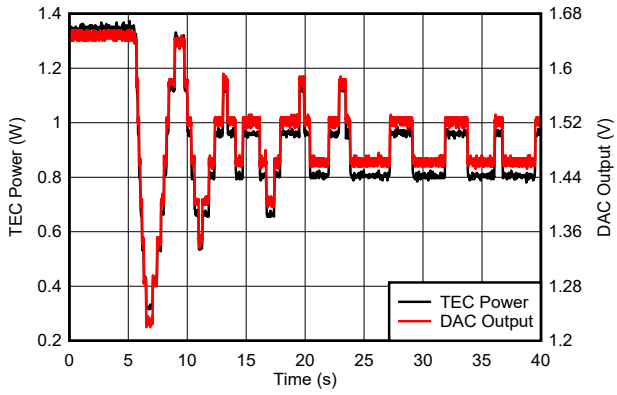


Figure 8-3. TEC Power and DAC Output vs Time

8.3 Power Supply Recommendations

The AFEx39xx family of devices does not require specific power-supply sequencing. These devices require a single power supply, V_{DD}. However, make sure the external voltage reference is applied after VDD. Use a 0.1-µF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value approximately 1.5 µF for the CAP pin.

8.4 Layout

8.4.1 Layout Guidelines

The AFEx39xx pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

8.4.2 Layout Example

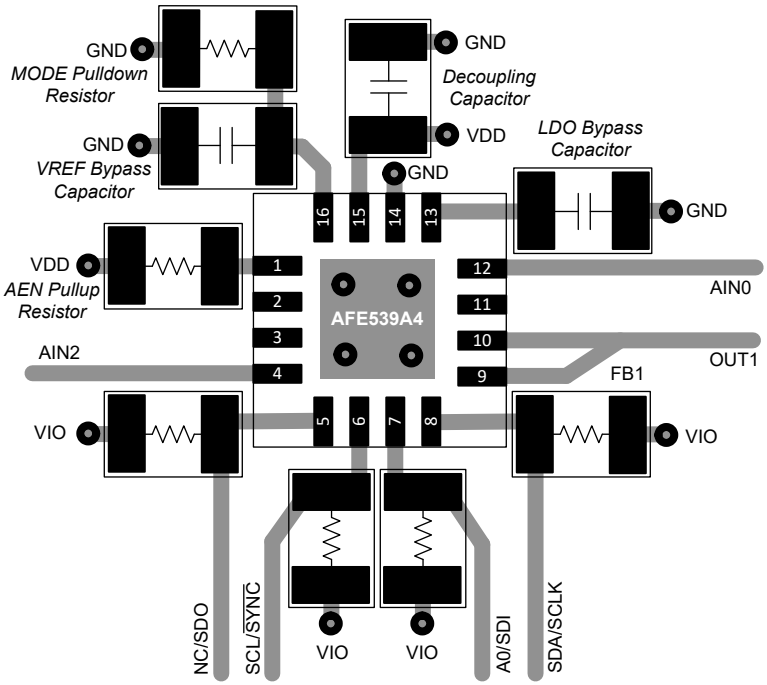


Figure 8-4. Layout Example

Note: The ground and power planes have been omitted for clarity. Connect the thermal pad to ground.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

The following documentation is available: *AFE539A4 Evaluation Module* user's guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE439A2RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A49A2
AFE539A4RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A59A4
AFE639D2RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A69D2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

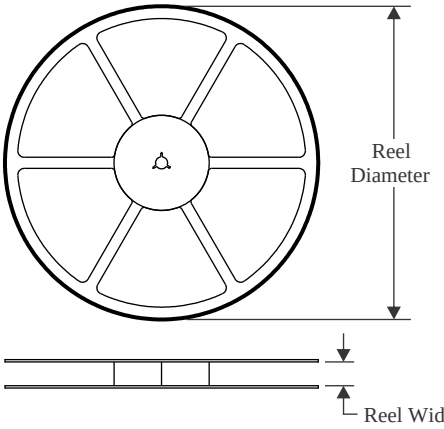
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

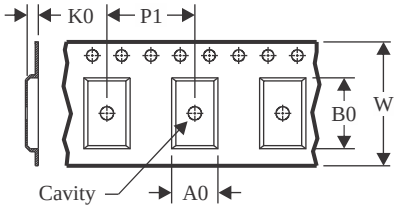
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

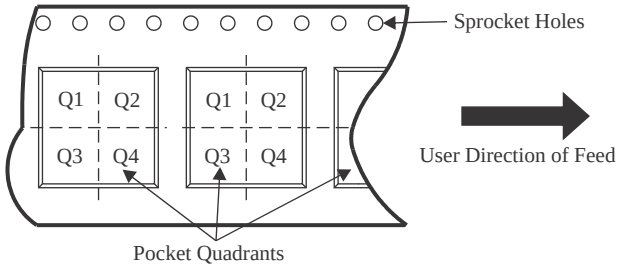


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

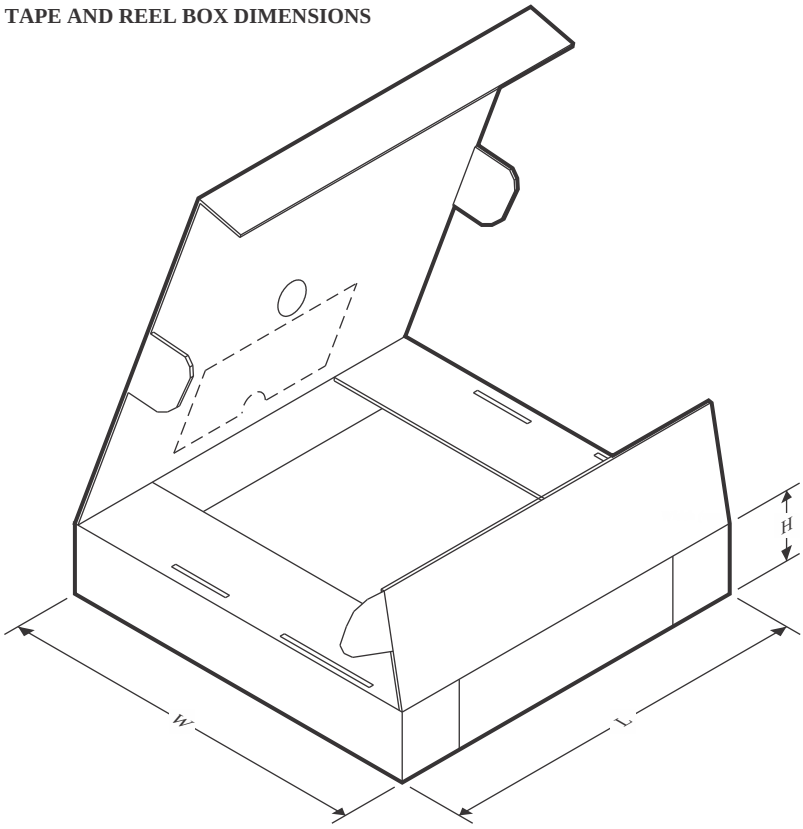
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE439A2RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
AFE539A4RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
AFE639D2RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE439A2RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
AFE539A4RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
AFE639D2RTER	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

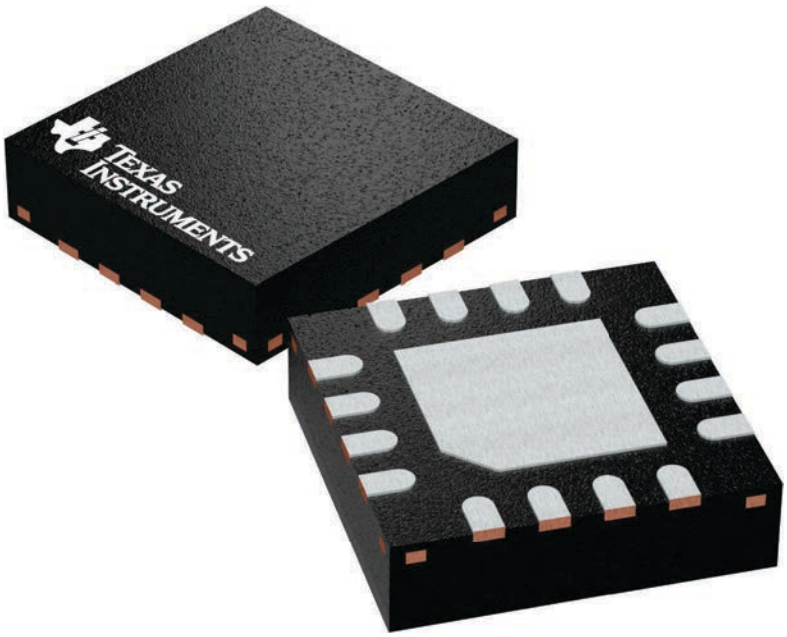
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

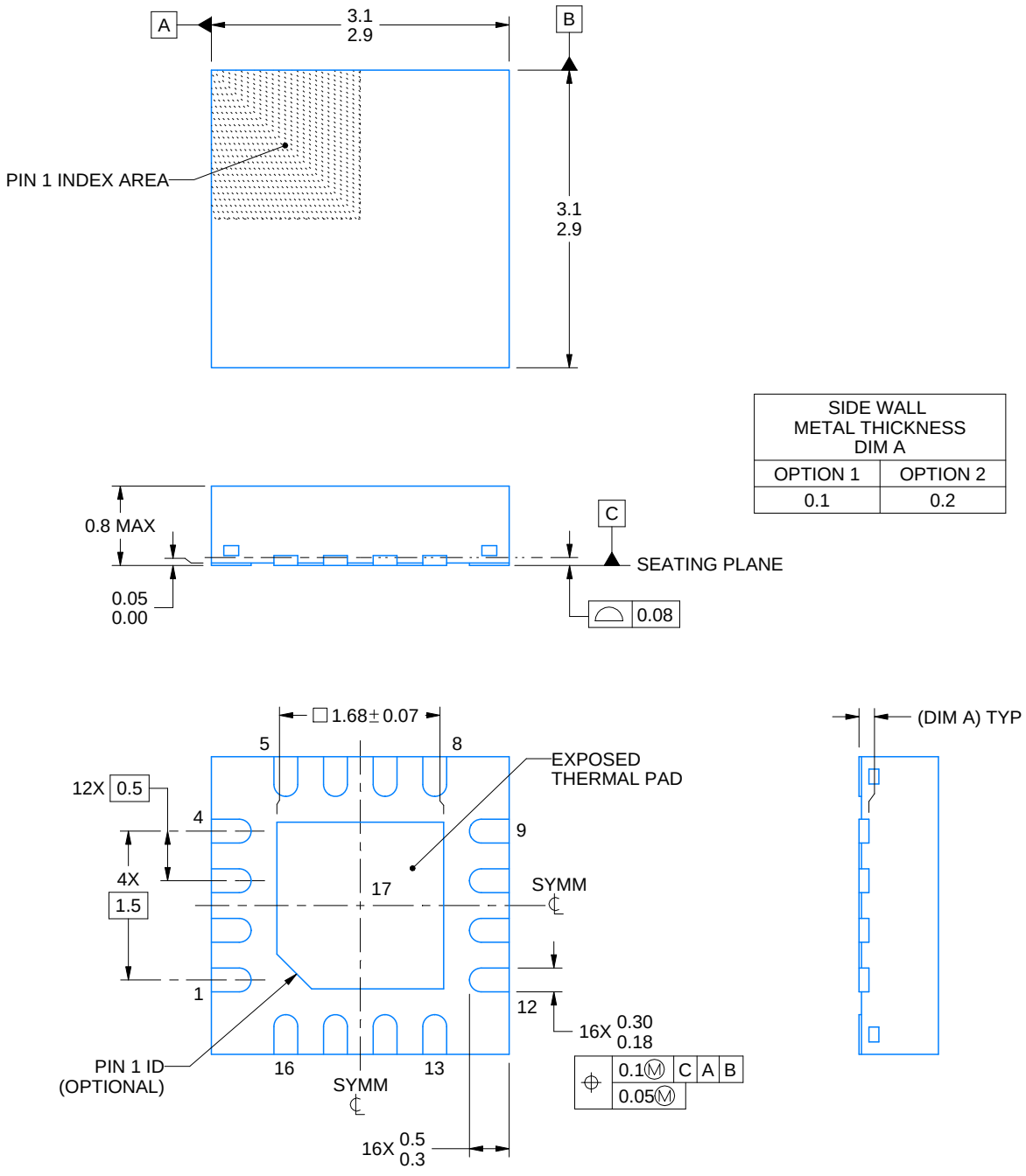


RTE0016C

PACKAGE OUTLINE

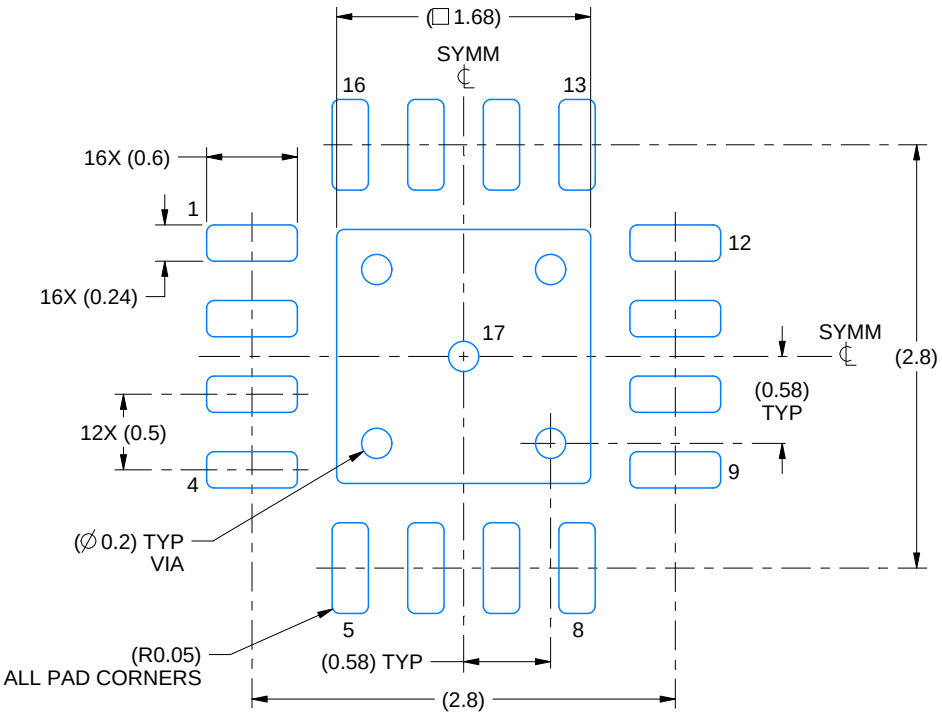
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

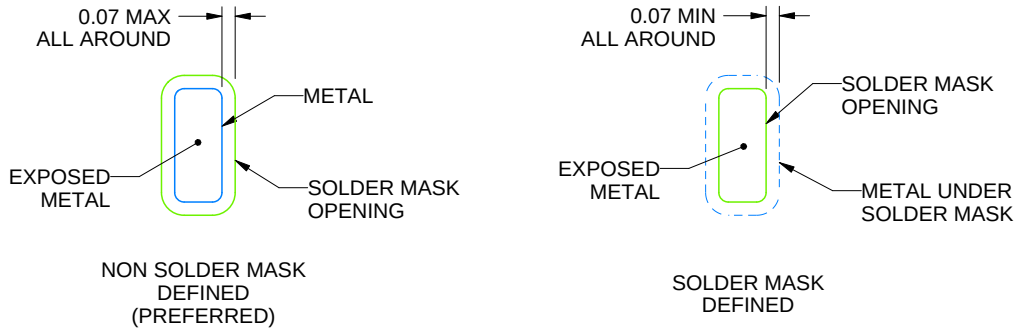


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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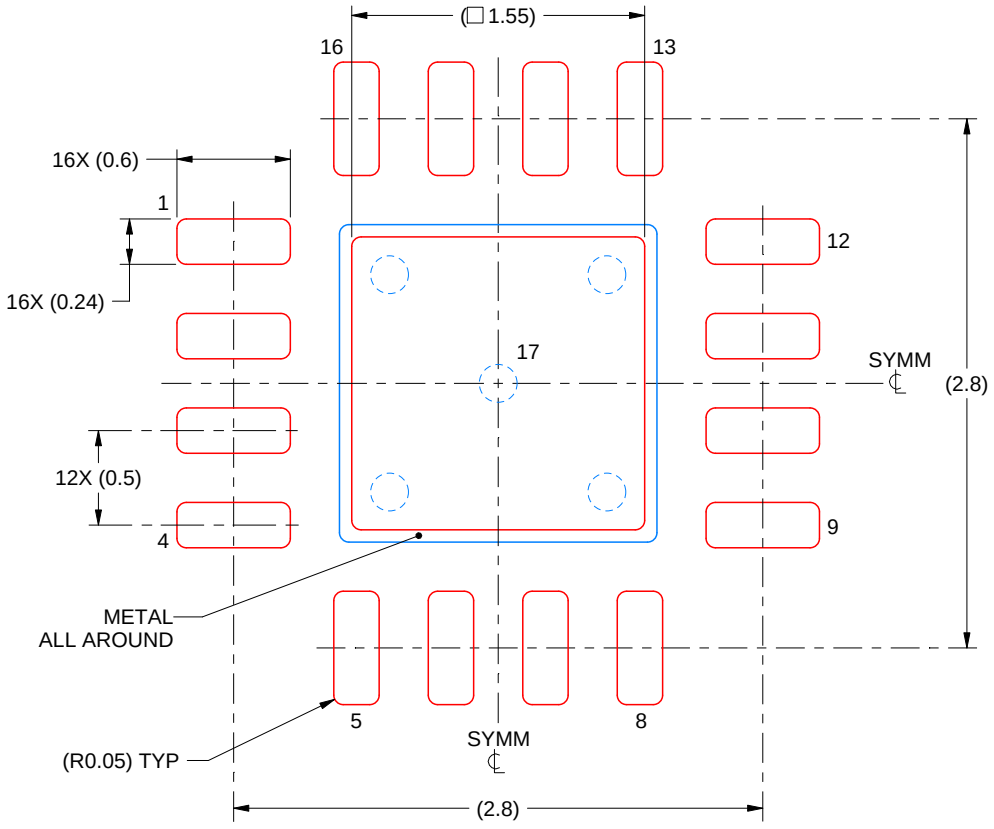
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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