

# AFEx32A3W 10-Bit and 8-Bit, Three-Channel, Voltage-Output, Current-Output, and ADC-Input, Smart AFE With I<sup>2</sup>C or SPI

## 1 Features

- Current-source DAC:
  - 1LSB DNL
  - Two ranges: 300mA and 220mA
  - 770mV headroom
- Dual voltage-output DACs:
  - 1LSB DNL
  - Gains of 1 ×, 1.5 ×, 2 ×, 3 ×, and 4 ×
- ADC input on channel 1
- Programmable comparator mode on channel 1
- High-impedance output when VDD is off
- High-impedance and resistive pulldown power-down modes
- 50MHz SPI-compatible interface
- Automatically detects I<sup>2</sup>C or SPI
  - 1.62V V<sub>IH</sub> with V<sub>DD</sub> = 5.5V
- General-purpose input/output (GPIO) configurable as multiple functions
- Predefined waveform generation: sine, cosine, triangular, sawtooth
- User-programmable nonvolatile memory (NVM)
- Internal or power-supply as reference
- Wide operating range:
  - Power supply: 3V to 5.5V
  - Temperature: –40°C to +125°C

## 2 Applications

- [Optical module](#)
- [Laser](#)

## 3 Description

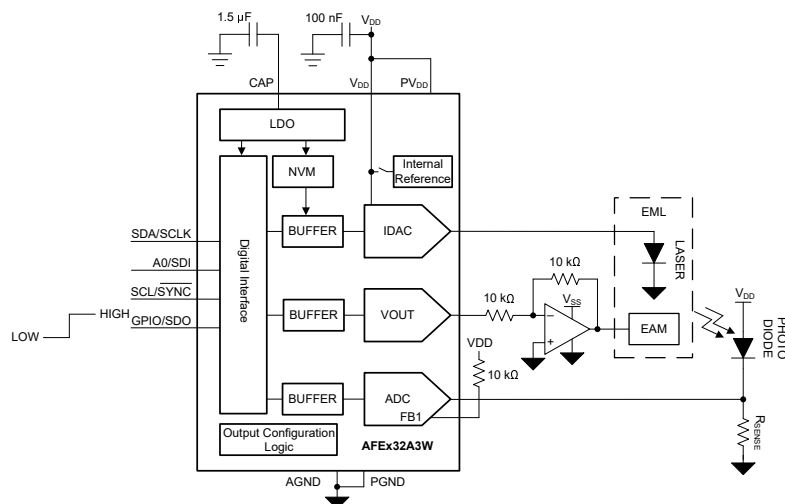
The 10-bit AFE532A3W and 8-bit AFE432A3W (AFEx32A3W) are 3-channel, buffered voltage-output, current-output, and ADC-input, smart analog front ends (AFEs). The AFEx32A3W support a current source used for linear control of laser diodes and miniature motors. These devices support Hi-Z power-down mode and Hi-Z output during power-off conditions for voltage output. Channel 1 is configurable as an ADC, voltage-output DAC, or comparator. The voltage-output DACs provide a force-sense option for use as a programmable comparator and current sink. The multifunction GPIO, function generation, and programmable nonvolatile memory (NVM) enable these smart AFEs for *processor-less* applications and design reuse. These devices automatically detect SPI or I<sup>2</sup>C interfaces and contain an internal reference.

The AFEx32A3W feature set combined with the tiny package and low power make these smart AFEs an excellent choice for laser diode power control and electro-absorption modulated laser (EML) control in passive optical network (PON), and other industrial laser applications.

### Device Information

PART NUMBER	RESOLUTION	PACKAGE <sup>(1)</sup>
AFE532A3W	10-bit	YBH (DSBGA, 16)
AFE432A3W	8-bit	

(1) For more information see [Section 11](#).



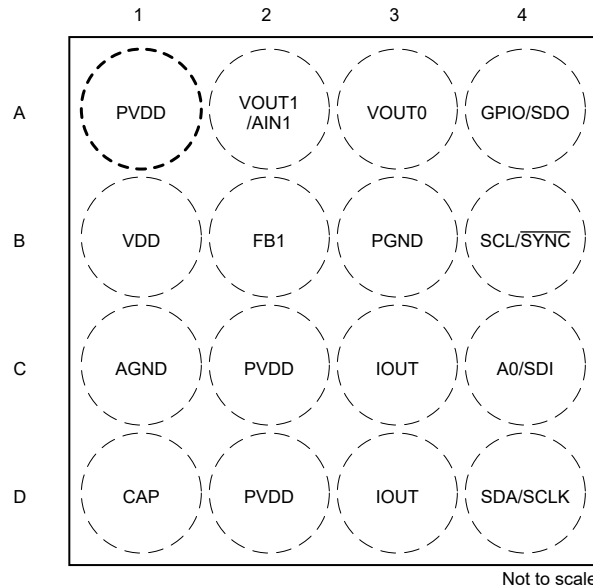
**Electro-Absorption Modulated Laser (EML) Control Using the AFEx32A3W**



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## 4 Pin Configuration and Functions



**Figure 4-1. YBH (16-pin DSBGA) Package, Top View**

**Table 4-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	PVDD	Power	Power supply for the current source. Connect this pin to VDD with low trace impedance
A2	VOUT1/AIN1	Input/Output	Voltage output or analog input on DAC channel 1.
A3	VOUT0	Output	Voltage output on DAC channel 0.
A4	GPIO/SDO	Input/Output	General-purpose input/output configurable as LDAC, PD, PROTECT, RESET, SDO, and STATUS. For STATUS and SDO, connect the pin to the I/O voltage with an external pullup resistor. If unused, connect the GPIO pin to VDD or AGND using an external resistor. This pin can ramp up before VDD.
B1	VDD	Power	Supply voltage.
B2	FB1	Input	Voltage feedback pin for channel 1. In voltage-output mode, connect to VOUT1/AIN1 for closed-loop amplifier output. In ADC-input mode, pull up this pin to VDD using a resistor. Use this pin as analog input in comparator mode.
B3	PGND	Ground	Ground return path for the current source. Connect this pin to AGND.
B4	SCL/SYNC	Output	I <sup>2</sup> C serial interface clock or SPI chip select input. This pin must be connected to the I/O voltage using an external pullup resistor. This pin can ramp up before VDD.
C1	AGND	Ground	Ground reference point for all circuitry on the device.
C2	PVDD	Power	Power supply for the current source. Connect this pin to VDD.
C3	IOU	Output	Current output on channel 2.
C4	A0/SDI	Input	Address configuration pin for I <sup>2</sup> C or serial data input for SPI. For A0, connect this pin to VDD, AGND, SDA, or SCL for address configuration (see the <i>Address Byte</i> section). For SDI, this pin need not be pulled up or pulled down. This pin can ramp up before VDD.
D1	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 $\mu$ F) between CAP and AGND.
D2	PVDD	Power	Power supply for the current source. Connect this pin to VDD.
D3	IOU	Output	Current output on channel 2.
D4	SDA/SCLK	Input/Output	Bidirectional I <sup>2</sup> C serial data bus or SPI clock input. This pin must be connected to the I/O voltage using an external pullup resistor in the I <sup>2</sup> C mode. This pin can ramp up before VDD.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage, V <sub>DD</sub> to AGND	-0.3	6	V
PV <sub>DD</sub>	Supply voltage, PV <sub>DD</sub> to V <sub>DD</sub>	-0.3	0.3	V
	Digital inputs to AGND	-0.3	V <sub>DD</sub> + 0.3	V
	V <sub>FB1</sub> to AGND	-0.3	V <sub>DD</sub> + 0.3	V
	V <sub>OUTX</sub> to AGND	-0.3	V <sub>DD</sub> + 0.3	V
	I <sub>OUT</sub> to AGND	-0.3	V <sub>DD</sub> + 0.3	V
	Current into any pin except the I <sub>OUT</sub> , V <sub>OUTx</sub> , V <sub>DD</sub> , PV <sub>DD</sub> , PGND, and AGND pins	-10	10	mA
T <sub>J</sub>	Junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Positive supply voltage to ground (AGND), resistive or diode load	3		5.5	V
	Positive supply voltage to ground (AGND), inductive load	3		4.5	
PV <sub>DD</sub>	Positive supply voltage to ground (PGND)		V <sub>DD</sub>		V
V <sub>IH</sub>	Digital input high voltage, 3 V < V <sub>DD</sub> ≤ 5.5 V	1.62			V
V <sub>IL</sub>	Digital input low voltage			0.4	V
C <sub>CAP</sub>	External capacitor on CAP pin	0.5		15	μF
T <sub>A</sub>	Ambient temperature	-40		125	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		AFE532A3W, AFE432A3W		UNIT
		YBH (DSBGA)		
		16 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	81.2		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.3		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	20.3		°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2		°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	20.3		°C/W

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 5.5 Electrical Characteristics: Voltage Output

all minimum and maximum specifications at  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  and typical specifications at  $T_A = 25^{\circ}\text{C}$ ,  $3\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ ,  $V_{\text{DD}}$  as reference, gain = 1 ×, voltage-output DAC pin (VOUTx) loaded with resistive load ( $R_L = 5\text{ k}\Omega$  to AGND) and capacitive load ( $C_L = 200\text{ pF}$  to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC PERFORMANCE</b>						
	Resolution	AFE532A3W	10			Bits
		AFE432A3W	8			
INL	Integral nonlinearity <sup>(1)</sup>	AFE532A3W	-1.25		1.25	LSB
		AFE432A3W	-1		1	
DNL	Differential nonlinearity <sup>(1)</sup>		-1		1	LSB
	Zero-code error <sup>(2)</sup>	Code 0d into DAC, $V_{\text{DD}} = 5.5\text{ V}$		6	12	mV
		Code 0d into DAC, internal $V_{\text{REF}}$ , gain = 4 ×, $V_{\text{DD}} = 5.5\text{ V}$		6	15	
	Zero-code-error temperature coefficient <sup>(2)</sup>			±10		$\mu\text{V}/^{\circ}\text{C}$
	Offset error <sup>(2)</sup>	$3\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ , $V_{\text{FB}}$ pin shorted to $V_{\text{OUT}}$ , DAC code: 8d for 10-bit resolution, 2d for 8-bit resolution	-0.5	0.25	0.5	%FSR
	Offset-error temperature coefficient <sup>(2)</sup>	$V_{\text{FB}}$ pin shorted to $V_{\text{OUT}}$ , DAC code: 8d for 10-bit resolution, 2d for 8-bit resolution		±0.0003		%FSR/ $^{\circ}\text{C}$
	Gain error <sup>(2)</sup>	Between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution	-0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient <sup>(2)</sup>	Between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution		±0.0008		%FSR/ $^{\circ}\text{C}$
	Full-scale error <sup>(2)</sup>	$3\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ , DAC at full scale	-0.5		0.5	%FSR
	Full-scale-error temperature coefficient <sup>(2)</sup>	DAC at full scale		±0.0008		%FSR/ $^{\circ}\text{C}$
<b>OUTPUT</b>						
	Output voltage		0		$V_{\text{DD}}$	V
$C_L$	Capacitive load <sup>(3)</sup>	$R_L = \text{infinite}$ , phase margin = $30^{\circ}$			200	pF
		Phase margin = $30^{\circ}$			1000	
	Short-circuit current	$V_{\text{DD}} = 3\text{ V}$ , full-scale output shorted to AGND or zero-scale output shorted to $V_{\text{DD}}$		50		mA
		$V_{\text{DD}} = 5.5\text{ V}$ , full-scale output shorted to AGND or zero-scale output shorted to $V_{\text{DD}}$		60		
	Output-voltage headroom <sup>(3)</sup>	To $V_{\text{DD}}$ , DAC output unloaded, internal reference = 1.21 V, $V_{\text{DD}} \geq 1.21\text{ V} \times \text{gain} + 0.2\text{ V}$	0.2			V
		To $V_{\text{DD}}$ and to AGND, DAC output unloaded	0.8			
		To $V_{\text{DD}}$ and to AGND, $I_{\text{LOAD}} = 10\text{ mA}$ at $V_{\text{DD}} = 5.5\text{ V}$ , $I_{\text{LOAD}} = 3\text{ mA}$ at $V_{\text{DD}} = 3\text{ V}$	10			
$Z_O$	$V_{\text{FB}}$ dc output impedance <sup>(4)</sup>	DAC output enabled, internal reference (gain = 1.5 × or 2 ×) or $V_{\text{DD}}$ as reference (gain = 1 ×)	400	500	600	k $\Omega$
		DAC output enabled, internal $V_{\text{REF}}$ , gain = 3 × or 4 ×	325	400	485	
	Power-supply rejection ratio (dc)	Internal $V_{\text{REF}}$ , gain = 2 ×, DAC at midscale, $V_{\text{DD}} = 5\text{ V} \pm 10\%$		0.25		mV/V

## 5.5 Electrical Characteristics: Voltage Output (continued)

all minimum and maximum specifications at  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  and typical specifications at  $T_A = 25^{\circ}\text{C}$ ,  $3\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ ,  $V_{\text{DD}}$  as reference, gain = 1  $\times$ , voltage-output DAC pin (VOUTx) loaded with resistive load ( $R_L = 5\text{ k}\Omega$  to AGND) and capacitive load ( $C_L = 200\text{ pF}$  to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DYNAMIC PERFORMANCE</b>						
$t_{\text{sett}}$	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, $V_{\text{DD}} = 5.5\text{ V}$		20		$\mu\text{s}$
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, $V_{\text{DD}} = 5.5\text{ V}$ , internal $V_{\text{REF}}$ , gain = 4 $\times$		25		
	Slew rate	$V_{\text{DD}} = 5.5\text{ V}$		0.3		V/ $\mu\text{s}$
	Power-on glitch magnitude	At start-up, DAC output disabled		75		mV
		At start-up, DAC output disabled, $R_L = 100\text{ k}\Omega$		200		
	Output-enable glitch magnitude	DAC output disabled to enabled, DAC registers at zero scale, $R_L = 100\text{ k}\Omega$		250		mV
$V_n$	Output noise voltage (peak-to-peak)	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$ , DAC at midscale, $V_{\text{DD}} = 5.5\text{ V}$		50		$\mu\text{V}_{\text{PP}}$
		Internal $V_{\text{REF}}$ , gain = 4 $\times$ , $f = 0.1\text{ Hz}$ to $10\text{ Hz}$ , DAC at midscale, $V_{\text{DD}} = 5.5\text{ V}$		90		
	Output noise density	$f = 1\text{ kHz}$ , DAC at midscale, $V_{\text{DD}} = 5.5\text{ V}$		0.35		$\mu\text{V}/\sqrt{\text{Hz}}$
		Internal $V_{\text{REF}}$ , gain = 4 $\times$ , $f = 1\text{ kHz}$ , DAC at midscale, $V_{\text{DD}} = 5.5\text{ V}$		0.9		
	Power-supply rejection ratio (ac) <sup>(4)</sup>	Internal $V_{\text{REF}}$ , gain = 4 $\times$ , 200-mV 50-Hz or 60-Hz sine wave superimposed on power supply voltage, DAC at midscale		-68		dB
	Code-change glitch impulse	$\pm 1$ -LSB change around midscale, including feedthrough		10		nV-s
	Code-change glitch impulse magnitude	$\pm 1$ -LSB change around midscale, including feedthrough		15		mV
<b>POWER</b>						
$I_{\text{DD}}$	Current flowing into VDD <sup>(2) (5)</sup>	Normal operation, DACs at full scale, digital pins static		150		$\mu\text{A}/\text{ch}$

- (1) Measured with DAC output unloaded. For internal reference  $V_{\text{DD}} \geq 1.21 \times \text{gain} + 0.2\text{ V}$ , between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution.
- (2) Measured with DAC output unloaded.
- (3) Specified by design and characterization, not production tested.
- (4) Specified with 200-mV headroom with respect to reference value when internal reference is used.
- (5) The total power consumption is calculated by  $I_{\text{DD}} \times (\text{total number of channels powered on}) + (\text{sleep-mode current})$ .

## 5.6 Electrical Characteristics: Current Output

all minimum and maximum specifications at  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  and typical specifications at  $T_A = 25^{\circ}\text{C}$ ,  $3\text{ V} \leq V_{DD} \leq 4.5\text{ V}$ , and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC PERFORMANCE</b>						
	Resolution	AFE532A3W	10			Bits
		AFE432A3W	8			
INL	Integral nonlinearity	At minimum output-voltage headroom, AFE532A3W	-1.25	1.25		LSB
		At minimum output-voltage headroom, AFE432A3W	-1	1		
DNL	Differential nonlinearity		-1	1		LSB
	Offset error		6			mA
	Gain error		16.6			%FSR
<b>OUTPUT</b>						
	Output range <sup>(1)</sup>	IOUT-GAIN = 000b	300			mA
		IOUT-GAIN = 001b	220			
	Output voltage headroom <sup>(2)</sup>	Sourcing current at 300 mA	770	1500		mV
		Sourcing current at 100 mA	300	1500		
	Power-down leakage at output	DAC channel disabled, voltage across the internal pulldown resistor	3			mV
	Power supply rejection ratio (dc)	DAC at midscale, $V_{DD}$ changed from 3.5 V to 4.5 V	0.5			LSB/V

## 5.6 Electrical Characteristics: Current Output (continued)

all minimum and maximum specifications at  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  and typical specifications at  $T_A = 25^{\circ}\text{C}$ ,  $3\text{ V} \leq V_{\text{DD}} \leq 4.5\text{ V}$ , and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DYNAMIC PERFORMANCE</b>						
$t_{\text{sett}}$	Output current settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 1 LSB, $V_{\text{DD}} = 3\text{ V}$ , diode load		60		$\mu\text{s}$
		1/8 to 3/8 scale and 3/8 to 1/8 scale settling to 1 LSB, $V_{\text{DD}} = 4\text{ V}$ , inductive load, $C_L = 470\text{ nF}$		260		
Overshoot		DAC code changed from 1/4 scale to 3/4 scale, diode load		0.7		%
		DAC powered down, full-scale current programmed as MARGIN-HIGH with slew rate setting 32-LSB and 4- $\mu\text{s}$ step, the DAC is powered up, and then the margin start is commanded immediately, diode load		1		
		DAC powered down, midscale current programmed as MARGIN-HIGH with slew rate setting 32-LSB and 4- $\mu\text{s}$ step, the DAC is powered up, and then the margin start is commanded immediately, inductive load		1		
		DAC at zero scale, full-scale current programmed as MARGIN-HIGH with slew rate setting 32-LSB and 4- $\mu\text{s}$ step, and then the margin start is commanded, diode load		1		
		DAC at zero scale, midscale current programmed as MARGIN-HIGH with slew rate setting 32-LSB and 4- $\mu\text{s}$ step, and then the margin start is commanded, inductive load, $C_L = 470\text{ nF}$		1		
		DAC at full scale, zero-scale current programmed as MARGIN-LOW with slew rate setting 32-LSB and 4- $\mu\text{s}$ step, and then the margin start is commanded, diode load		-1		
		DAC at midscale, zero-scale current programmed as MARGIN-LOW with slew rate setting 32-LSB and 4- $\mu\text{s}$ step, and then the margin start is commanded, inductive load, $C_L = 470\text{ nF}$		-1		
$V_n$	Output noise current (peak to peak)	0.1 Hz to 10 Hz, DAC at 1/4 scale, inductive load, $C_L = 470\text{ nF}$		50		$\mu\text{A}_{\text{PP}}$
	Output noise density	$f = 1\text{ kHz}$ , DAC at 1/4 scale, inductive load, $C_L = 470\text{ nF}$		159		$\text{nA}/\sqrt{\text{Hz}}$
	Power-supply rejection ratio (ac)	200-mV 50-Hz or 60-Hz sine wave superimposed on power-supply voltage, DAC at 1/4 scale, inductive load, $C_L = 470\text{ nF}$		1.7		LSB/V
<b>POWER</b>						
$I_{\text{DD}}$	Current flowing into VDD <sup>(3)</sup>	Normal operation, DAC at midscale		172		$\mu\text{A}$

- (1) Use the device in the minimum current range to meet the electrical specifications.
- (2) These devices do not have automatic thermal shutdown. The external circuitry must maintain the junction temperature within the specified limits.
- (3) The current flowing into  $V_{\text{DD}}$  does not account for the load current sourced or sunk on the IOUT pins.



## 5.7 Electrical Characteristics: Comparator Mode

all minimum and maximum specifications at  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  and typical specifications at  $T_A = 25^{\circ}\text{C}$ ,  $3\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ ,  $V_{\text{DD}}$  reference, gain = 1 ×, voltage-output DAC output pin (VOUTx) loaded with resistive load ( $R_L = 5\text{ k}\Omega$  to AGND) and capacitive load ( $C_L = 200\text{ pF}$  to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC PERFORMANCE</b>						
	Offset error <sup>(1) (2)</sup>	$3\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ ; DAC at midscale, comparator input at Hi-Z	-6	0	6	mV
	Offset error time drift <sup>(1)</sup>	$V_{\text{DD}} = 5.5\text{ V}$ , $T_A = 125^{\circ}\text{C}$ , FB1 in Hi-Z mode, DAC at full scale and $V_{\text{FB}}$ at 0 V or DAC at zero scale and $V_{\text{FB}}$ at 1.84 V, drift specified for 10 years of continuous operation		4		mV
<b>OUTPUT</b>						
	Input voltage	$V_{\text{FB1}}$ resistor network connected to ground	0		$V_{\text{DD}}$	V
		$V_{\text{FB1}}$ resistor network disconnected from ground	0		$V_{\text{DD}} \times (1/3 - 1/100)$	
$V_{\text{OL}}$	Logic low output voltage	$I_{\text{LOAD}} = 100\text{ }\mu\text{A}$ , output in open-drain mode		0.1		V
<b>DYNAMIC PERFORMANCE</b>						
$t_{\text{resp}}$	Output response time	DAC at midscale with 10-bit resolution, FB1 input at Hi-Z, and transition step at FB1 node is $(V_{\text{DAC}} - 2\text{ LSB})$ to $(V_{\text{DAC}} + 2\text{ LSB})$ , transition time measured between 10% and 90% of output, output current of 100 $\mu\text{A}$ , comparator output configured in push-pull mode, load capacitor at DAC output is 25 pF		10		$\mu\text{s}$

- (1) Specified by design and characterization, not production tested.  
(2) This specification does not include the total unadjusted error (TUE) of the DAC.

## 5.8 Electrical Characteristics: ADC Input

all minimum and maximum specifications at  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  and typical specifications at  $T_A = 25^{\circ}\text{C}$ ,  $3\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ ,  $V_{\text{DD}}$  as reference, gain = 1 ×, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC PERFORMANCE</b>						
	Resolution		10			Bits
INL	Integral nonlinearity <sup>(1)</sup>		-2		2	LSB
DNL	Differential nonlinearity <sup>(1)</sup>		-1		1	LSB
	Offset error <sup>(1) (2)</sup>		-5	0	5	mV
	Gain error <sup>(1) (2)</sup>		-1		1	%FSR
<b>INPUT</b>						
	Input voltage range		0		$V_{\text{DD}} / 3$	V
<b>DYNAMIC PERFORMANCE</b>						
	Data rate <sup>(1)</sup>	ADC averaging setting is 4 samples	1406		2008	SPS
	Sampling capacitor			10		pF

- (1) Specified by design and characterization, not production tested.  
(2) Measured at DAC at mid-scale, comparator input at Hi-Z.

## 5.9 Electrical Characteristics: General

all minimum and maximum specifications at  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  and typical specifications at  $T_A = 25^{\circ}\text{C}$ ,  $3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{DD}$  as reference, gain = 1 ×, voltage-output DAC output pin (VOUTx) loaded with resistive load ( $R_L = 5\text{ k}\Omega$  to AGND) in voltage-output mode and capacitive load ( $C_L = 200\text{ pF}$  to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INTERNAL REFERENCE</b>						
	Initial accuracy		1.1979	1.212	1.224	V
	Reference-output temperature coefficient <sup>(1) (2)</sup>				73	ppm/°C
<b>EEPROM</b>						
	Endurance <sup>(1)</sup>	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		20000		Cycles
		$T_A = 125^{\circ}\text{C}$		1000		
	Data retention <sup>(1)</sup>			50		Years
	EEPROM programming write cycle time <sup>(1)</sup>				200	ms
	Device boot-up time <sup>(1)</sup>	Time taken from power valid ( $V_{DD} \geq 3\text{ V}$ ) to output valid state (output state as programmed in EEPROM), 0.5- $\mu\text{F}$ capacitor on the CAP pin		5		ms
<b>DIGITAL INPUTS</b>						
	Digital feedthrough	Voltage output mode, DAC output static at midscale, fast mode plus, SCL toggling		20		nV-s
	Pin capacitance	Per pin		10		pF
<b>POWER-DOWN MODE</b>						
$I_{DD}$	Current flowing into VDD	DAC in sleep mode, internal reference powered down			28	$\mu\text{A}$
$I_{DD}$	Current flowing into VDD <sup>(1)</sup>	DAC in sleep mode, internal reference enabled, additional current through internal reference		10		$\mu\text{A}$
		DAC channels enabled, internal reference enabled, additional current through internal reference per DAC channel in voltage-output mode		12.5		
<b>HIGH-IMPEDANCE OUTPUT</b>						
$I_{LEAK}$	Current flowing into V <sub>OUT</sub> and V <sub>FB</sub>	DAC in Hi-Z output mode, $3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		10		nA
		$V_{DD} = 0\text{ V}$ , $V_{OUT} \leq 1.5\text{ V}$ , decoupling capacitor between $V_{DD}$ and AGND = 0.1 $\mu\text{F}$		200		
		$V_{DD} = 0\text{ V}$ , $1.5\text{ V} < V_{OUT} \leq 5.5\text{ V}$ , decoupling capacitor between $V_{DD}$ and AGND = 0.1 $\mu\text{F}$		500		
		100 k $\Omega$ between $V_{DD}$ and AGND, $V_{OUT} \leq 1.25\text{ V}$ , series resistance of 10 k $\Omega$ at OUT pin		$\pm 2$		$\mu\text{A}$

(1) Specified by design and characterization, not production tested.

(2) Measured at  $-40^{\circ}\text{C}$  and  $+125^{\circ}\text{C}$  and calculated the slope.

### 5.10 Timing Requirements: I<sup>2</sup>C Standard Mode

all input signals are timed from VIL to 70% of V<sub>pull-up</sub>, 3 V ≤ V<sub>DD</sub> ≤ 5.5 V, –40°C ≤ T<sub>A</sub> ≤ +125°C, and 1.7 V ≤ V<sub>pull-up</sub> ≤ V<sub>DD</sub>

		MIN	NOM	MAX	UNIT
f <sub>SCL</sub>	SCL frequency			100	kHz
t <sub>BUF</sub>	Bus free time between stop and start conditions	4.7			μs
t <sub>HDSTA</sub>	Hold time after repeated start	4			μs
t <sub>SUSTA</sub>	Repeated start setup time	4.7			μs
t <sub>SUSTO</sub>	Stop condition setup time	4			μs
t <sub>HDDAT</sub>	Data hold time	0			ns
t <sub>SUDAT</sub>	Data setup time	250			ns
t <sub>LOW</sub>	SCL clock low period	4700			ns
t <sub>HIGH</sub>	SCL clock high period	4000			ns
t <sub>F</sub>	Clock and data fall time			300	ns
t <sub>R</sub>	Clock and data rise time			1000	ns
t <sub>VDDAT</sub>	Data valid time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			3.45	μs
t <sub>VDAACK</sub>	Data valid acknowledge time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			3.45	μs

### 5.11 Timing Requirements: I<sup>2</sup>C Fast Mode

all input signals are timed from VIL to 70% of V<sub>pull-up</sub>, 3 V ≤ V<sub>DD</sub> ≤ 5.5 V, –40°C ≤ T<sub>A</sub> ≤ +125°C, and 1.7 V ≤ V<sub>pull-up</sub> ≤ V<sub>DD</sub>

		MIN	NOM	MAX	UNIT
f <sub>SCL</sub>	SCL frequency			400	kHz
t <sub>BUF</sub>	Bus free time between stop and start conditions	1.3			μs
t <sub>HDSTA</sub>	Hold time after repeated start	0.6			μs
t <sub>SUSTA</sub>	Repeated start setup time	0.6			μs
t <sub>SUSTO</sub>	Stop condition setup time	0.6			μs
t <sub>HDDAT</sub>	Data hold time	0			ns
t <sub>SUDAT</sub>	Data setup time	100			ns
t <sub>LOW</sub>	SCL clock low period	1300			ns
t <sub>HIGH</sub>	SCL clock high period	600			ns
t <sub>F</sub>	Clock and data fall time			300	ns
t <sub>R</sub>	Clock and data rise time			300	ns
t <sub>VDDAT</sub>	Data valid time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			0.9	μs
t <sub>VDAACK</sub>	Data valid acknowledge time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			0.9	μs

### 5.12 Timing Requirements: I<sup>2</sup>C Fast-Mode Plus

all input signals are timed from VIL to 70% of V<sub>pull-up</sub>, 3 V ≤ V<sub>DD</sub> ≤ 5.5 V, –40°C ≤ T<sub>A</sub> ≤ +125°C, and 1.7 V ≤ V<sub>pull-up</sub> ≤ V<sub>DD</sub>

		MIN	NOM	MAX	UNIT
f <sub>SCL</sub>	SCL frequency			1	MHz
t <sub>BUF</sub>	Bus free time between stop and start conditions	0.5			μs
t <sub>HDSTA</sub>	Hold time after repeated start	0.26			μs
t <sub>SUSTA</sub>	Repeated start setup time	0.26			μs
t <sub>SUSTO</sub>	Stop condition setup time	0.26			μs
t <sub>HDDAT</sub>	Data hold time	0			ns
t <sub>SUDAT</sub>	Data setup time	50			ns
t <sub>LOW</sub>	SCL clock low period	0.5			μs
t <sub>HIGH</sub>	SCL clock high period	0.26			μs
t <sub>F</sub>	Clock and data fall time			120	ns
t <sub>R</sub>	Clock and data rise time			120	ns
t <sub>VDDAT</sub>	Data valid time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			0.45	μs
t <sub>VDAACK</sub>	Data valid acknowledge time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			0.45	μs

### 5.13 Timing Requirements: SPI Write Operation

all input signals are specified with  $t_r = t_f = 1 \text{ V/ns}$  (10% to 90% of  $V_{IO}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ ,  $1.7 \text{ V} \leq V_{IO} \leq 5.5 \text{ V}$ ,  $3 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

		MIN	NOM	MAX	UNIT
$f_{\text{SCLK}}$	Serial clock frequency			50	MHz
$t_{\text{SCLKHIGH}}$	SCLK high time	9			ns
$t_{\text{SCLKLOW}}$	SCLK low time	9			ns
$t_{\text{SDIS}}$	SDI setup time	8			ns
$t_{\text{SDIH}}$	SDI hold time	8			ns
$t_{\text{CSS}}$	$\overline{\text{CS}}$ to SCLK falling edge setup time	18			ns
$t_{\text{CSH}}$	SCLK falling edge to $\overline{\text{CS}}$ rising edge	10			ns
$t_{\text{CSHIGH}}$	$\overline{\text{CS}}$ high time	50			ns
$t_{\text{DACWAIT}}$	Sequential DAC update wait time (time between subsequent LDAC falling edges) for same channel	2			$\mu\text{s}$
$t_{\text{BCASTWAIT}}$	Broadcast DAC update wait time (time between subsequent LDAC falling edges)	2			$\mu\text{s}$

### 5.14 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 0)

all input signals are specified with  $t_r = t_f = 1 \text{ V/ns}$  (10% to 90% of  $V_{IO}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ ,  $1.7 \text{ V} \leq V_{IO} \leq 5.5 \text{ V}$ ,  $3 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , and  $\text{FSDO} = 0$

		MIN	NOM	MAX	UNIT
$f_{\text{SCLK}}$	Serial clock frequency			1.25	MHz
$t_{\text{SCLKHIGH}}$	SCLK high time	350			ns
$t_{\text{SCLKLOW}}$	SCLK low time	350			ns
$t_{\text{SDIS}}$	SDI setup time	8			ns
$t_{\text{SDIH}}$	SDI hold time	8			ns
$t_{\text{CSS}}$	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	400			ns
$t_{\text{CSH}}$	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	400			ns
$t_{\text{CSHIGH}}$	$\overline{\text{SYNC}}$ high time	1			$\mu\text{s}$
$t_{\text{SDODLY}}$	SCLK rising edge to SDO falling edge, $I_{OL} \leq 5 \text{ mA}$ , $C_L = 20 \text{ pF}$ .			300	ns

### 5.15 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 1)

all input signals are specified with  $t_r = t_f = 1 \text{ V/ns}$  (10% to 90% of  $V_{IO}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ ,  $1.7 \text{ V} \leq V_{IO} \leq 5.5 \text{ V}$ ,  $3 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , and  $\text{FSDO} = 1$

		MIN	NOM	MAX	UNIT
$f_{\text{SCLK}}$	Serial clock frequency			2.5	MHz
$t_{\text{SCLKHIGH}}$	SCLK high time	175			ns
$t_{\text{SCLKLOW}}$	SCLK low time	175			ns
$t_{\text{SDIS}}$	SDI setup time	8			ns
$t_{\text{SDIH}}$	SDI hold time	8			ns
$t_{\text{CSS}}$	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	300			ns
$t_{\text{CSH}}$	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	300			ns
$t_{\text{CSHIGH}}$	$\overline{\text{SYNC}}$ high time	1			$\mu\text{s}$
$t_{\text{SDODLY}}$	SCLK rising edge to SDO falling edge, $I_{OL} \leq 5 \text{ mA}$ , $C_L = 20 \text{ pF}$ .			300	ns

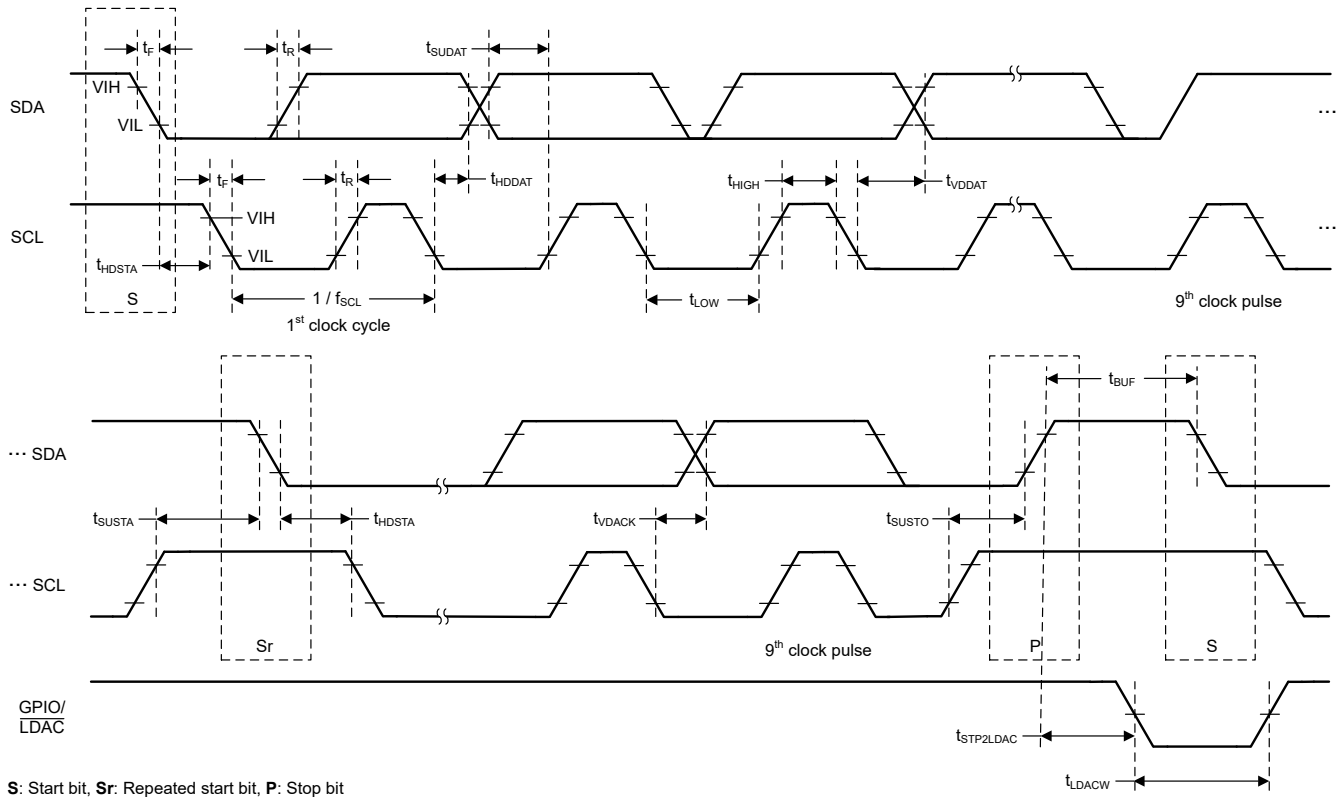
### 5.16 Timing Requirements: GPIO

all input signals are specified with  $t_r = t_f = 1 \text{ V/ns}$  (10% to 90% of  $V_{IO}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ ,  $1.7 \text{ V} \leq V_{IO} \leq 5.5 \text{ V}$ ,  $3 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

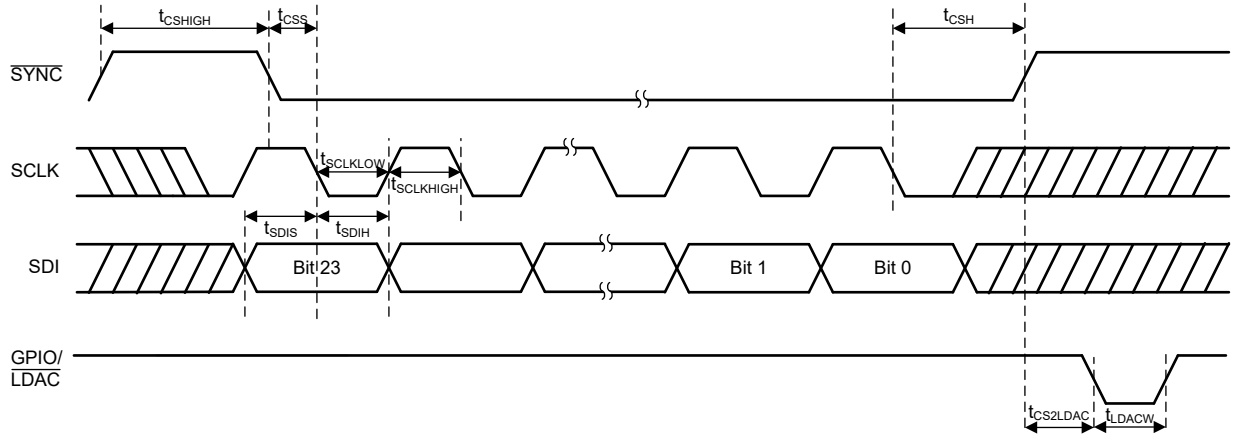
		MIN	NOM	MAX	UNIT
$t_{GPIHIGH}$	GPI high time	2			$\mu\text{s}$
$t_{GPILOW}$	GPI low time	2			$\mu\text{s}$
$t_{GPAWGD}$	$\overline{\text{LDAC}}$ falling edge to DAC update delay <sup>(1)</sup>			2	$\mu\text{s}$
$t_{CS2LDAC}$	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	1			$\mu\text{s}$
$t_{STP2LDAC}$	I <sup>2</sup> C stop bit rising edge to $\overline{\text{LDAC}}$ falling edge	1			$\mu\text{s}$
$t_{LDACW}$	$\overline{\text{LDAC}}$ low time	2			$\mu\text{s}$

(1) The GPIOs can be configured as a channel-specific or global  $\overline{\text{LDAC}}$  function.

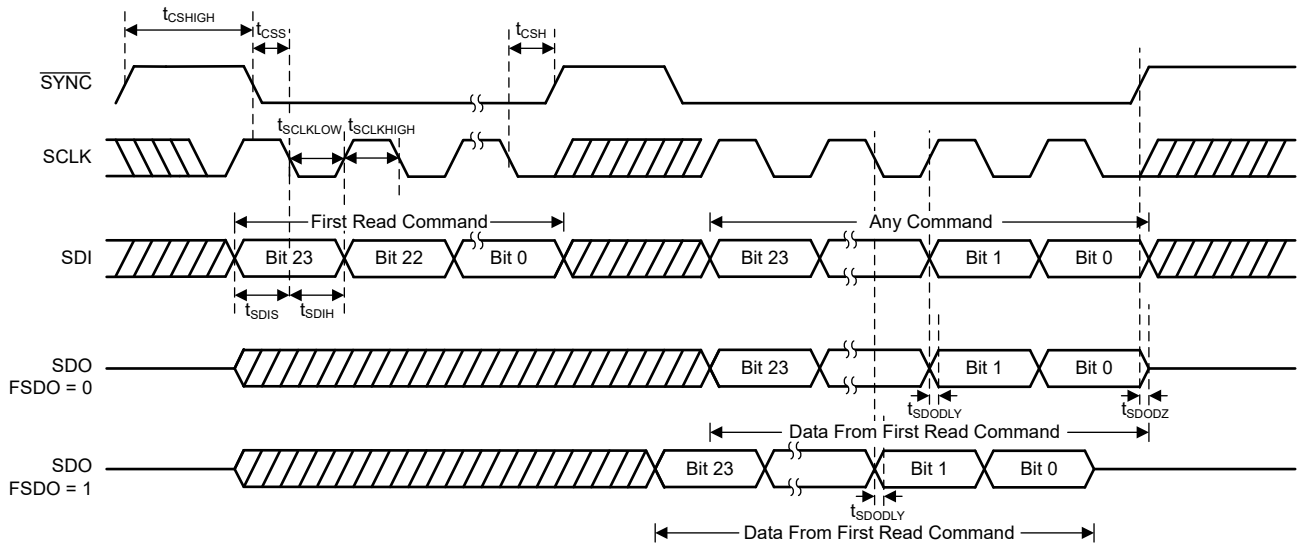
### 5.17 Timing Diagrams



**Figure 5-1. I<sup>2</sup>C Timing Diagram**



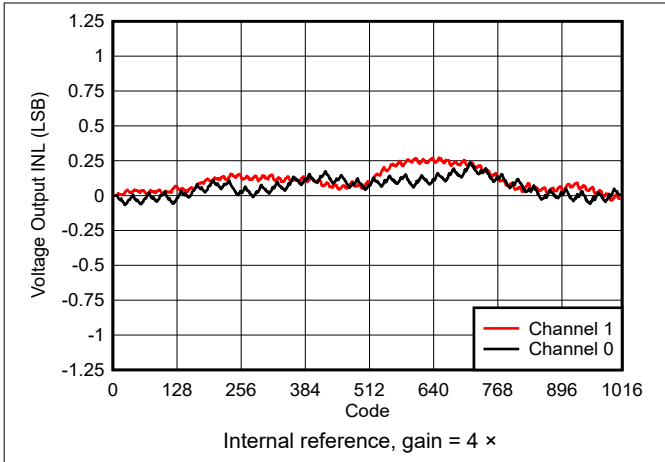
**Figure 5-2. SPI Write Timing Diagram**



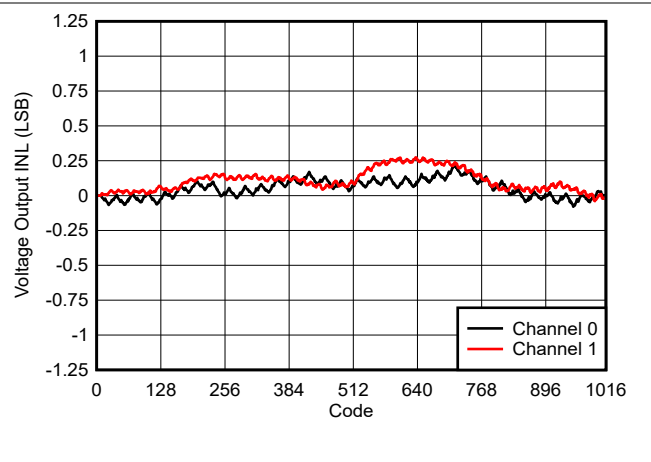
**Figure 5-3. SPI Read Timing Diagram**

### 5.18 Typical Characteristics: Voltage Output

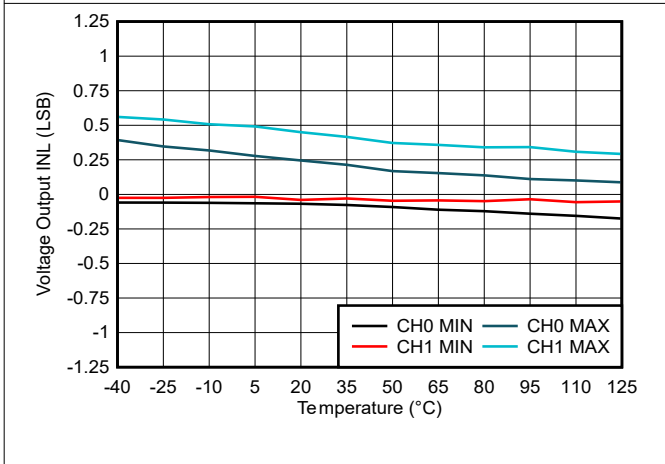
at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ ,  $V_{DD}$  as reference, gain = 1 ×, 10-bit resolution, and DAC outputs unloaded (unless otherwise noted)



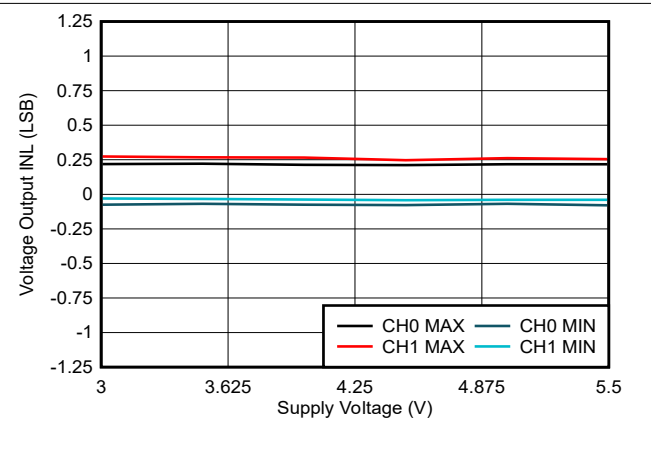
**Figure 5-4. Voltage Output INL vs Digital Input Code**



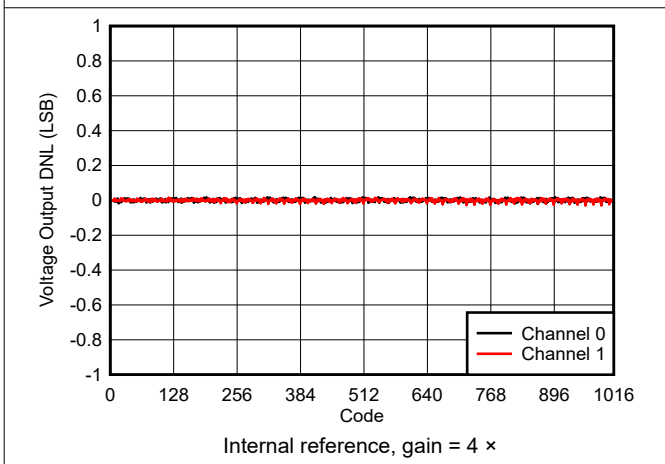
**Figure 5-5. Voltage Output INL vs Digital Input Code**



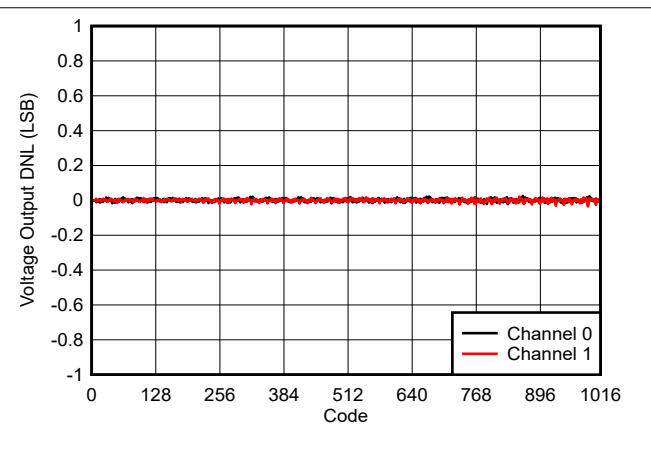
**Figure 5-6. Voltage Output INL vs Temperature**



**Figure 5-7. Voltage Output INL vs Supply Voltage**



**Figure 5-8. Voltage Output DNL vs Digital Input Code**



**Figure 5-9. Voltage Output DNL vs Digital Input Code**

### 5.18 Typical Characteristics: Voltage Output (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ ,  $V_{DD}$  as reference, gain = 1 ×, 10-bit resolution, and DAC outputs unloaded (unless otherwise noted)

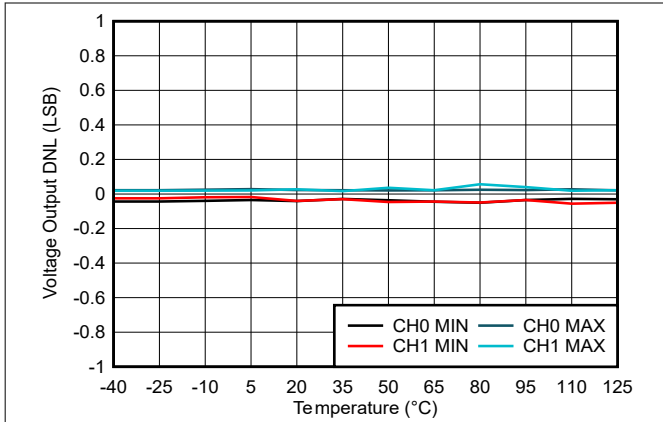


Figure 5-10. Voltage Output DNL vs Temperature

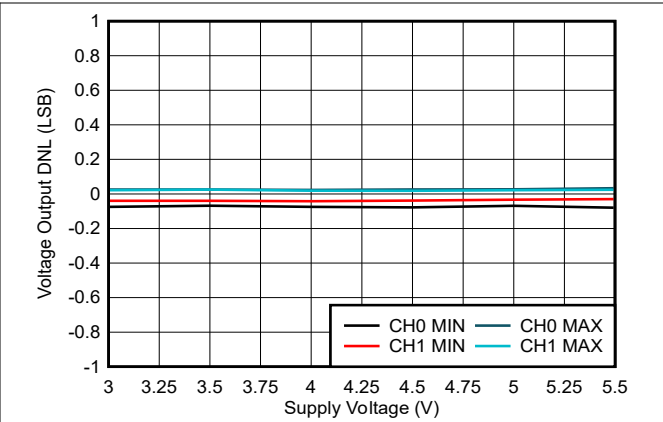


Figure 5-11. Voltage Output DNL vs Supply Voltage

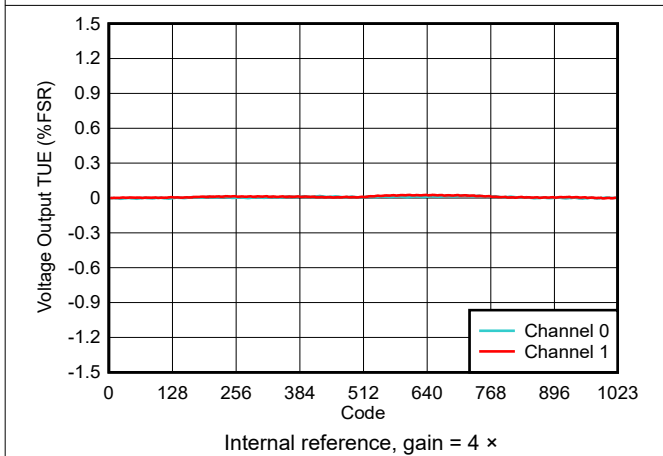


Figure 5-12. Voltage Output TUE vs Digital Input Code

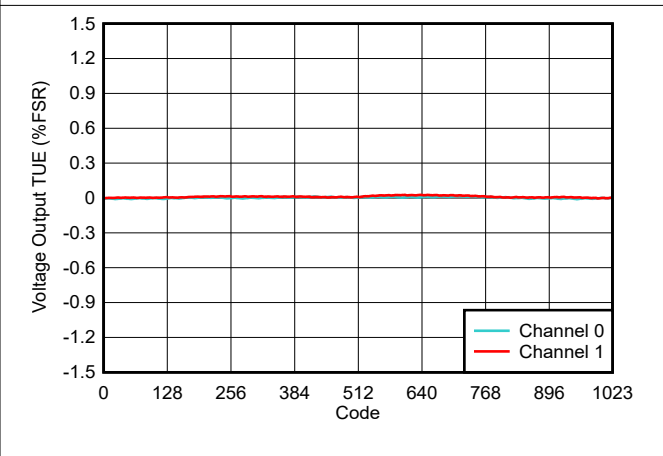


Figure 5-13. Voltage Output TUE vs Digital Input Code

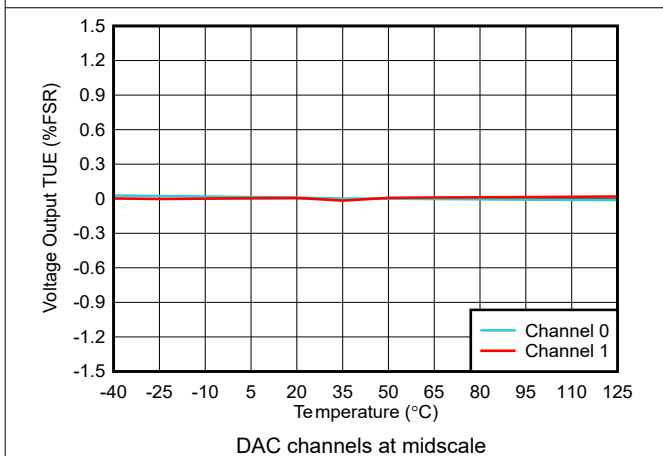


Figure 5-14. Voltage Output TUE vs Temperature

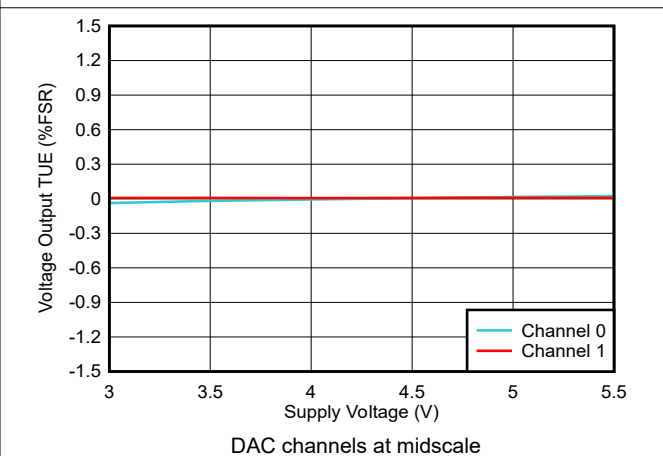


Figure 5-15. Voltage Output TUE vs Supply Voltage



### 5.18 Typical Characteristics: Voltage Output (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ ,  $V_{DD}$  as reference, gain = 1  $\times$ , 10-bit resolution, and DAC outputs unloaded (unless otherwise noted)

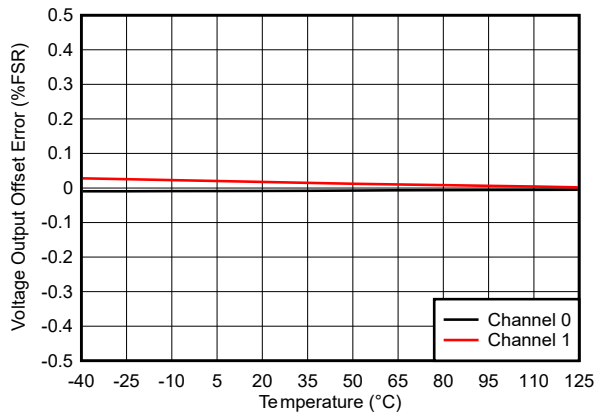


Figure 5-16. Voltage Output Offset Error vs Temperature

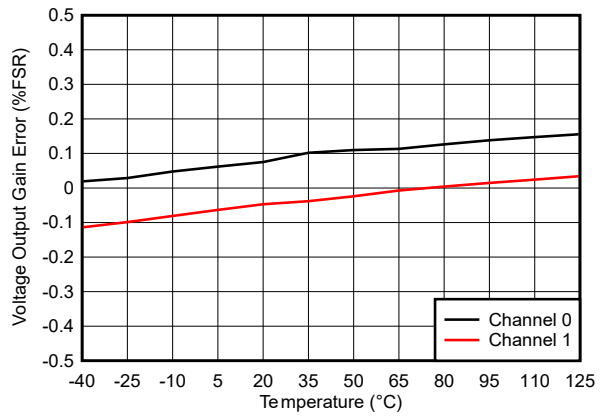


Figure 5-17. Voltage Output Gain Error vs Temperature

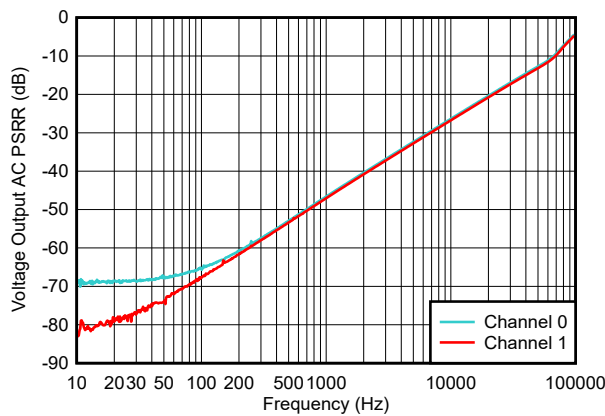


Figure 5-18. Voltage Output AC PSRR vs Frequency

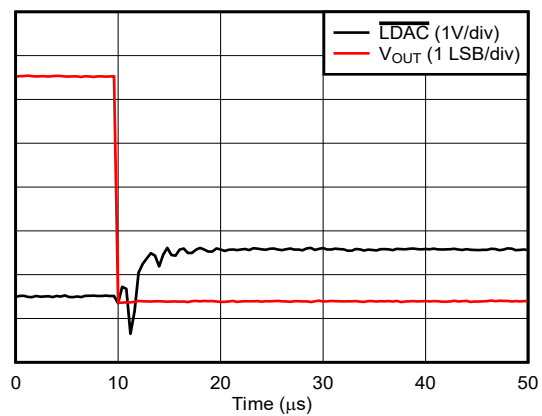


Figure 5-19. Voltage Output Code-to-Code Glitch: Rising Edge

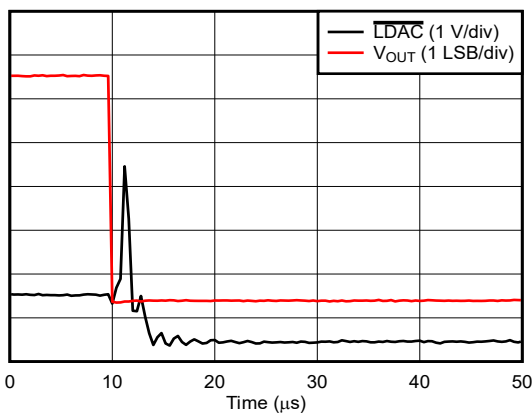


Figure 5-20. Voltage Output Code-to-Code Glitch: Falling Edge

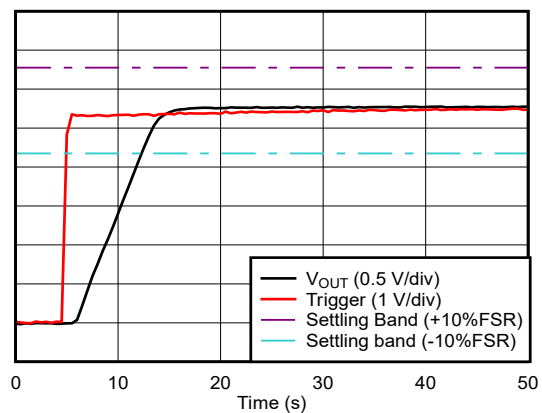
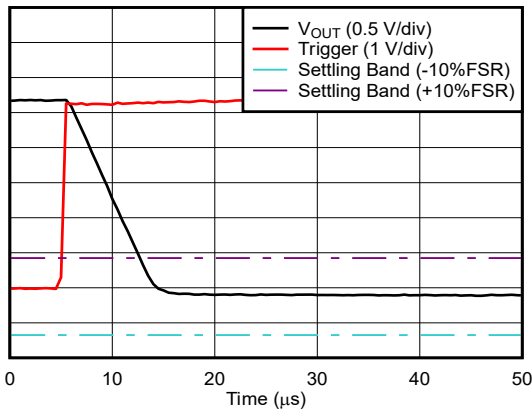


Figure 5-21. Voltage Output Setting Time: Rising Edge

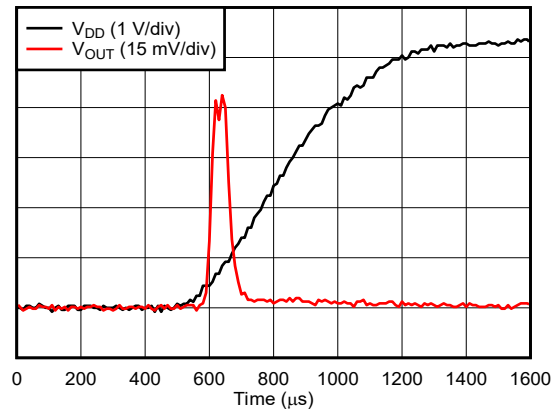
### 5.18 Typical Characteristics: Voltage Output (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ ,  $V_{DD}$  as reference, gain = 1  $\times$ , 10-bit resolution, and DAC outputs unloaded (unless otherwise noted)



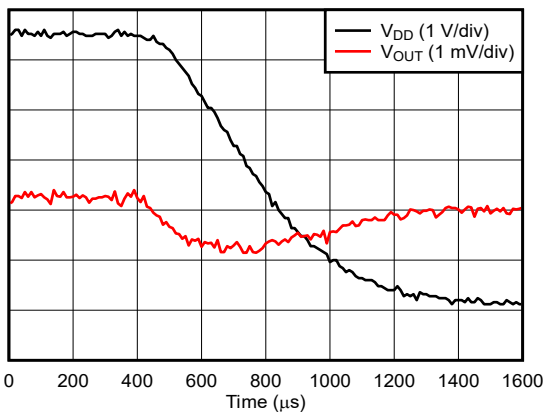
Full scale to zero scale swing

Figure 5-22. Voltage Output Setting Time: Falling Edge



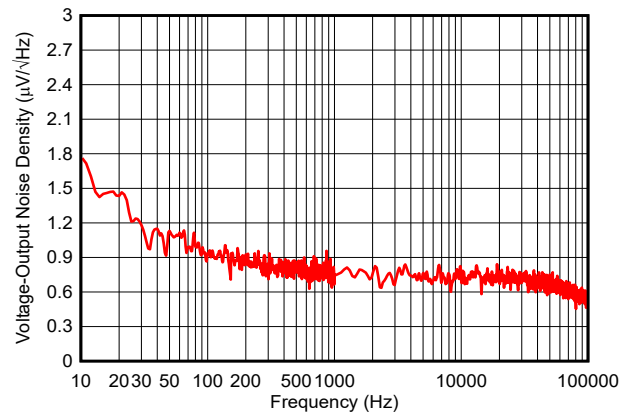
DAC in Hi-Z power-down mode

Figure 5-23. Voltage Output Power-On Glitch



DAC at zero scale

Figure 5-24. Voltage Output Power-Off Glitch



Internal reference, gain = 4  $\times$

Figure 5-25. Voltage Output Noise Density

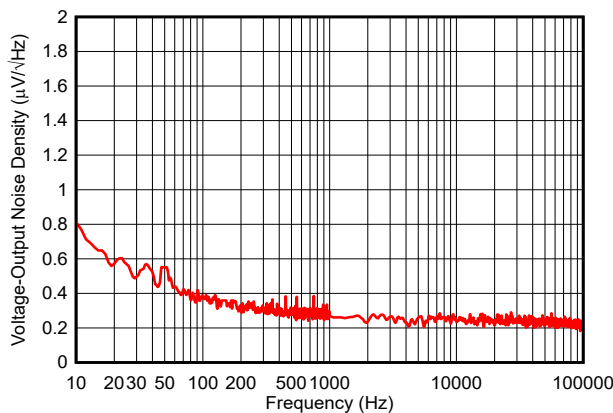
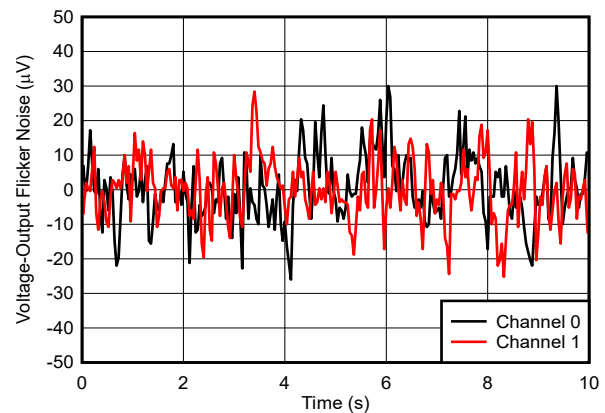


Figure 5-26. Voltage Output Noise Density

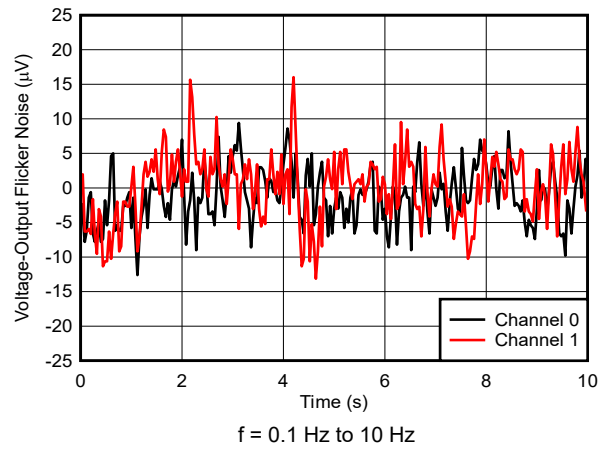


Internal reference, gain = 4  $\times$ ,  $f = 0.1\text{ Hz to }10\text{ Hz}$

Figure 5-27. Voltage Output Flicker Noise

### 5.18 Typical Characteristics: Voltage Output (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , VDD as reference, gain = 1 ×, 10-bit resolution, and DAC outputs unloaded (unless otherwise noted)



**Figure 5-28. Voltage Output Flicker Noise**

### 5.19 Typical Characteristics: Current Output

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ ,  $I_{OUT-GAIN} = 2/3$ , diode load (unless otherwise noted)

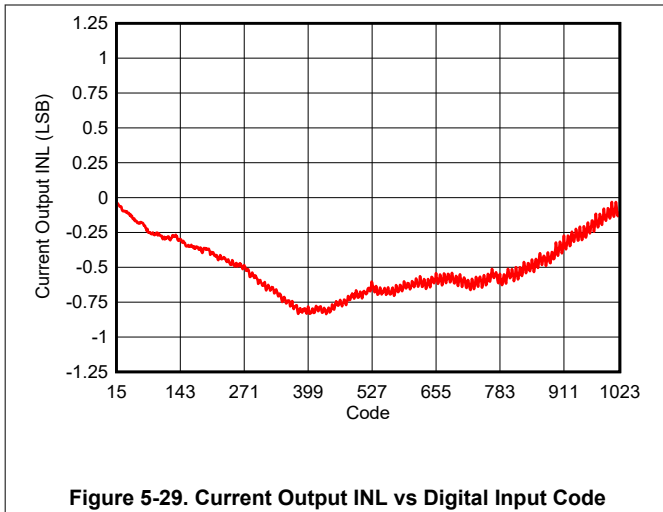


Figure 5-29. Current Output INL vs Digital Input Code

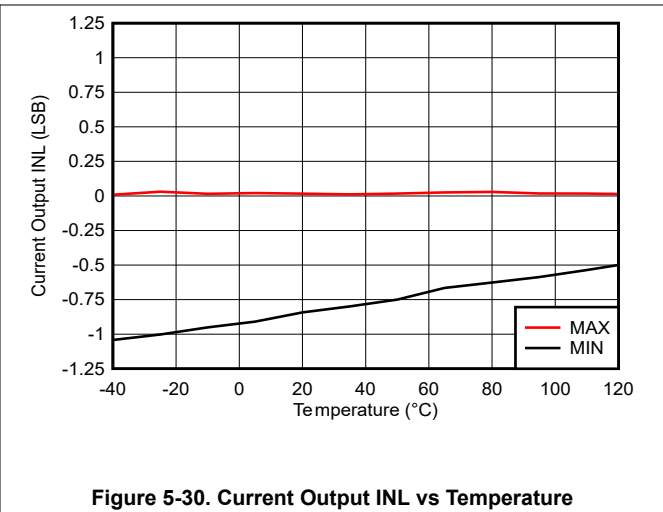


Figure 5-30. Current Output INL vs Temperature

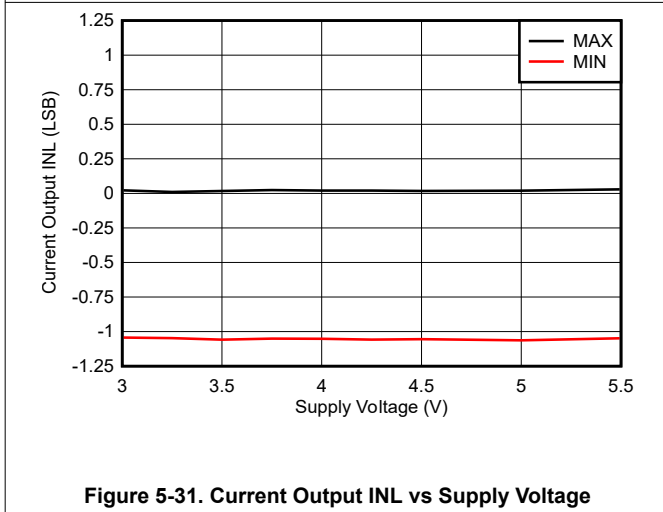


Figure 5-31. Current Output INL vs Supply Voltage

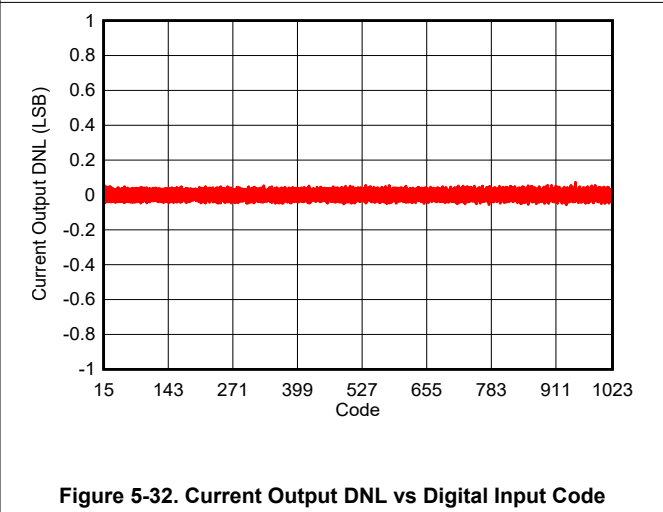


Figure 5-32. Current Output DNL vs Digital Input Code

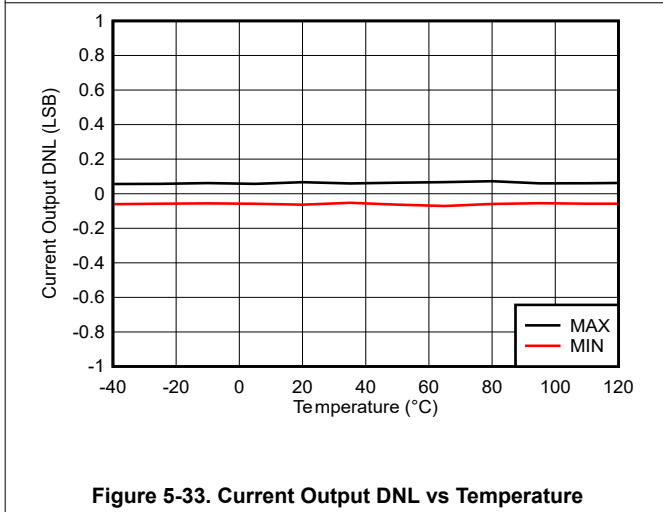


Figure 5-33. Current Output DNL vs Temperature

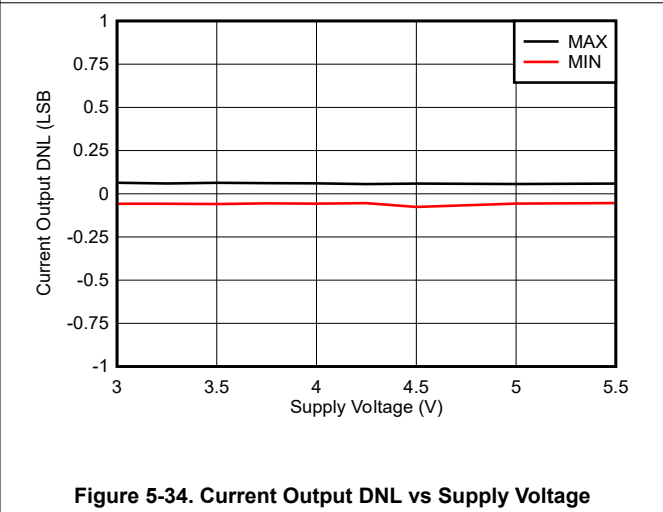


Figure 5-34. Current Output DNL vs Supply Voltage

### 5.19 Typical Characteristics: Current Output (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ ,  $I_{OUT-GAIN} = 2/3$ , diode load (unless otherwise noted)

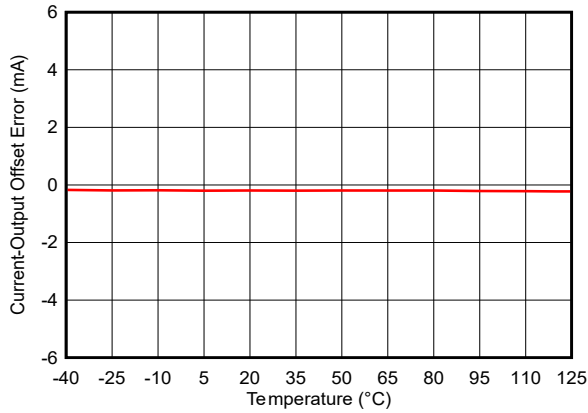


Figure 5-35. Current Output Offset Error vs Temperature

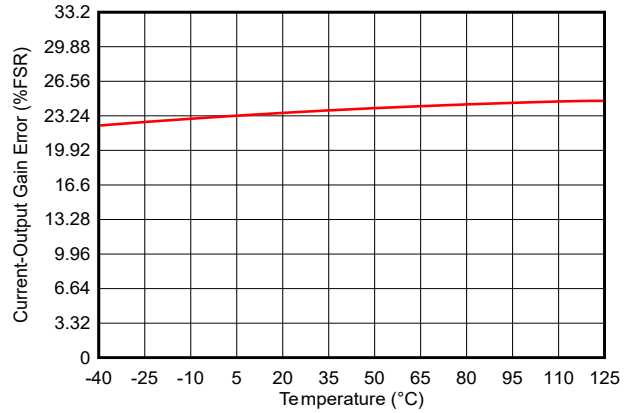


Figure 5-36. Current Output Gain Error vs Temperature

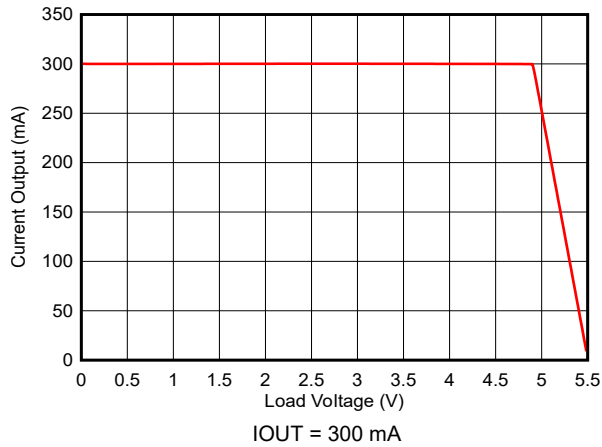


Figure 5-37. Current Output vs Load Voltage

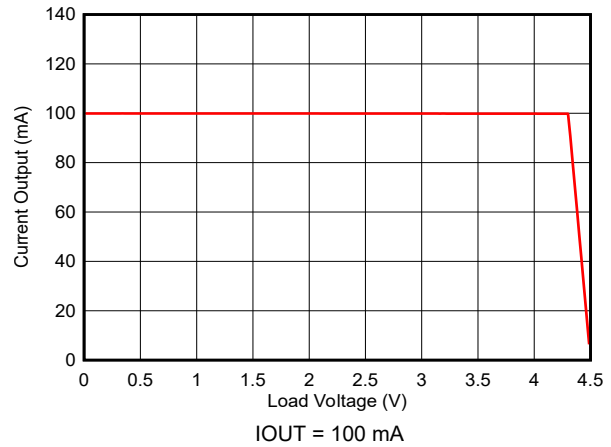


Figure 5-38. Current Output vs Load Voltage

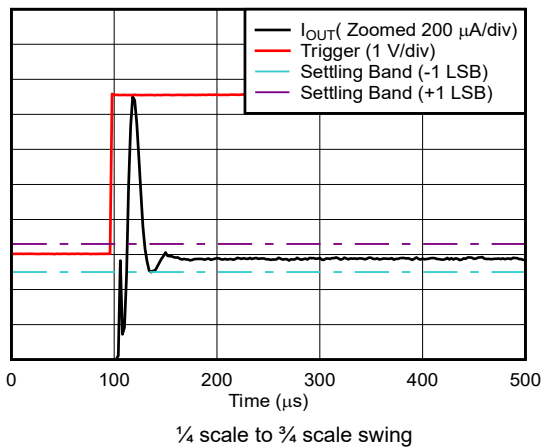


Figure 5-39. Current Output Setting Time, Rising Edge

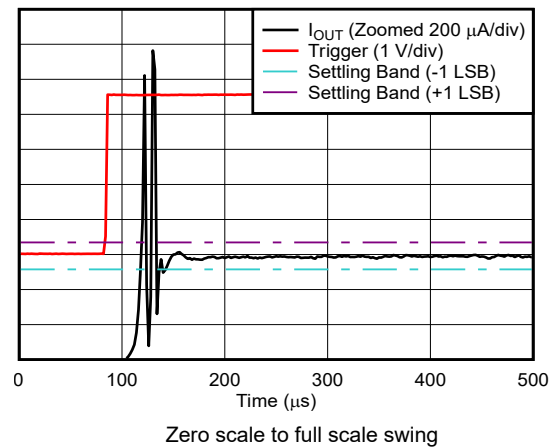


Figure 5-40. Current Output Setting Time, Rising Edge

### 5.19 Typical Characteristics: Current Output (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ ,  $I_{OUT-GAIN} = 2/3$ , diode load (unless otherwise noted)

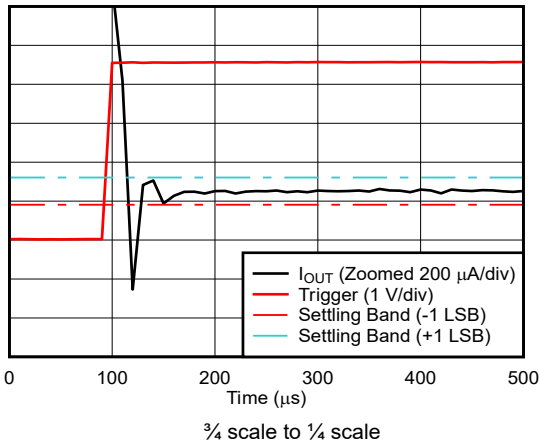


Figure 5-41. Current Output Setting Time, Falling Edge

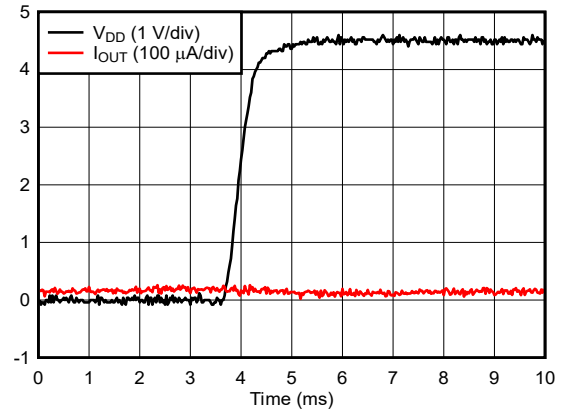


Figure 5-42. Current Output Power-On Glitch

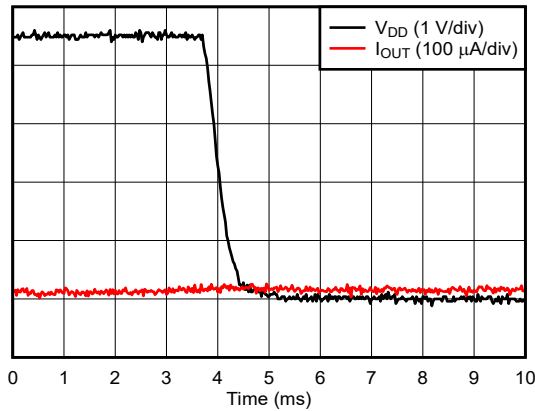


Figure 5-43. Current Output Power-Off Glitch

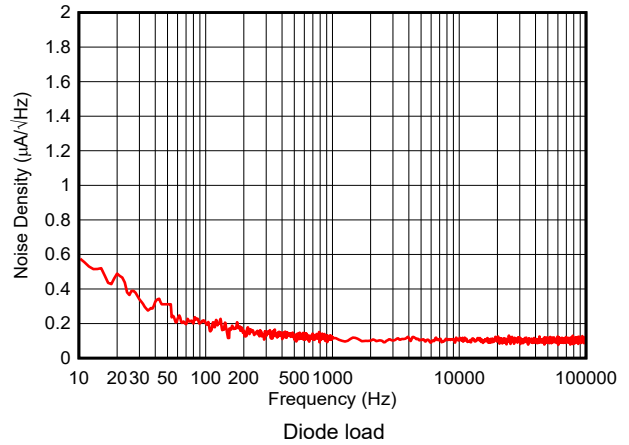


Figure 5-44. Current Output Noise Density

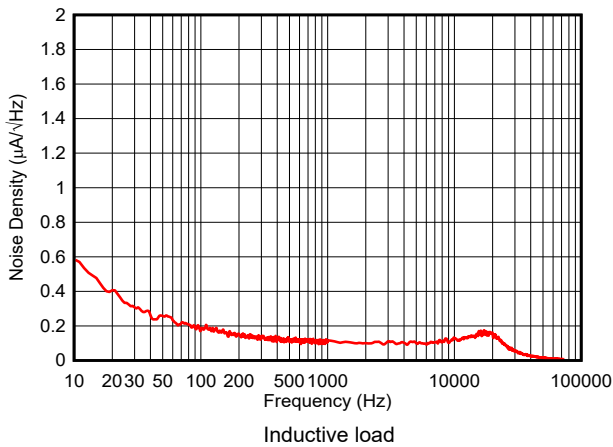


Figure 5-45. Current Output Noise Density

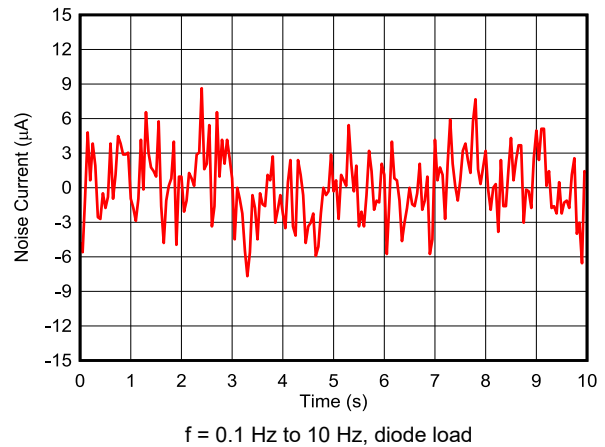
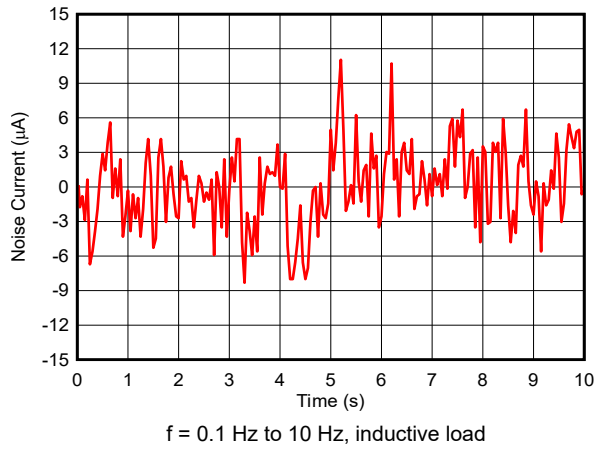


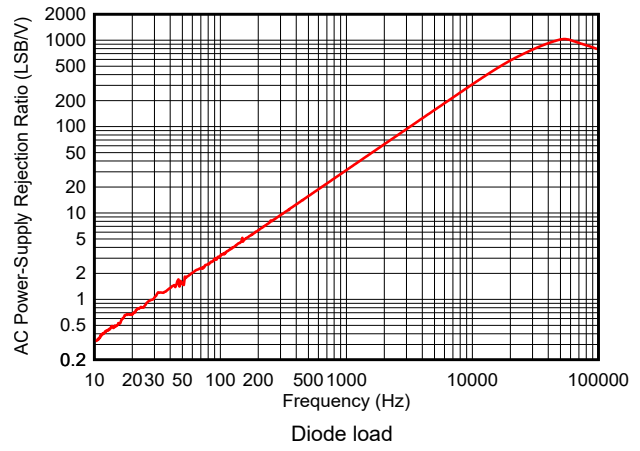
Figure 5-46. Current Output Flicker Noise

### 5.19 Typical Characteristics: Current Output (continued)

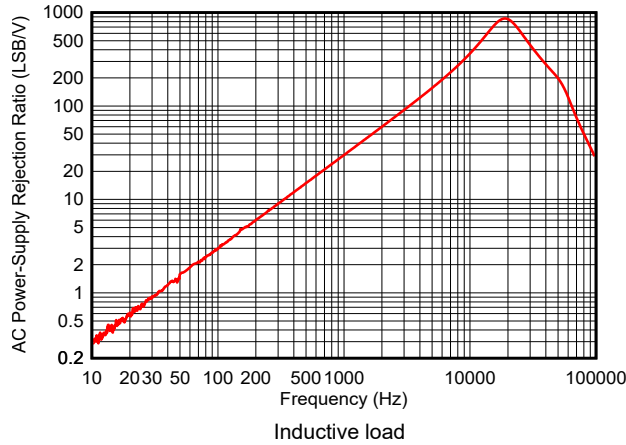
at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ ,  $I_{OUT-GAIN} = 2/3$ , diode load (unless otherwise noted)



**Figure 5-47. Current Output Flicker Noise**



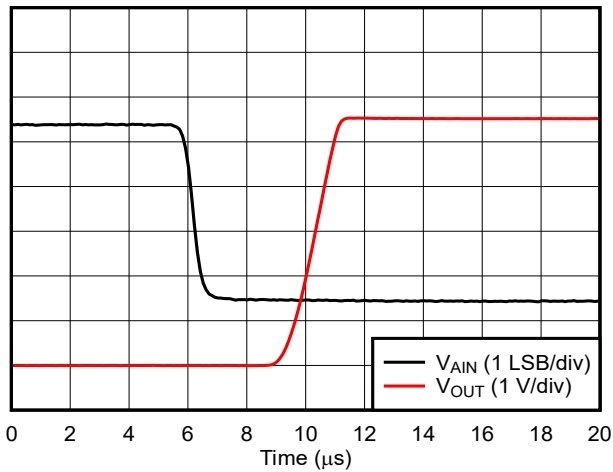
**Figure 5-48. Current Output AC PSRR vs Frequency**  
Diode load



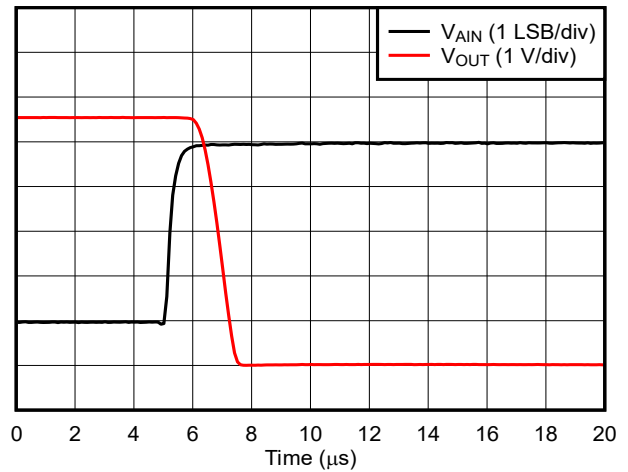
**Figure 5-49. Current Output AC PSRR vs Frequency**  
Inductive load

## 5.20 Typical Characteristics: Comparator

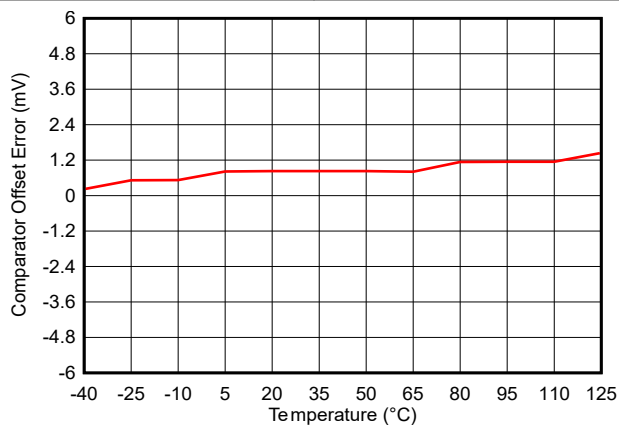
at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ ,  $V_{DD}$  as reference, gain = 1  $\times$ , 10-bit resolution, FB1 pin in Hi-Z mode, and DAC outputs unloaded (unless otherwise noted)



**Figure 5-50. Comparator Response Time: Low-to-High Transition**



**Figure 5-51. Comparator Response Time: High-to-Low Transition**

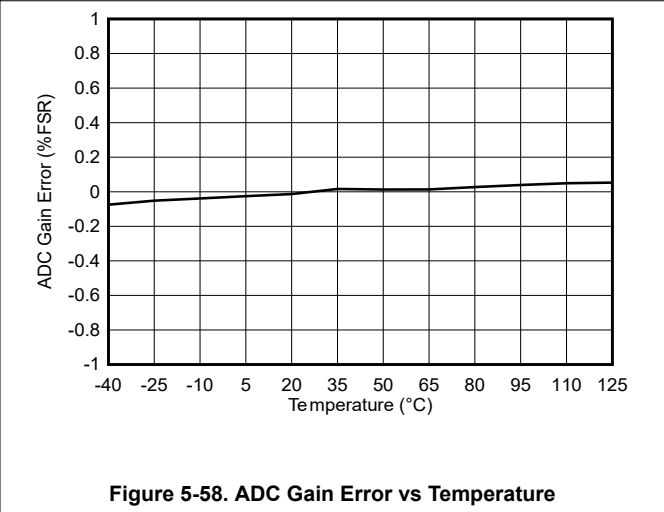
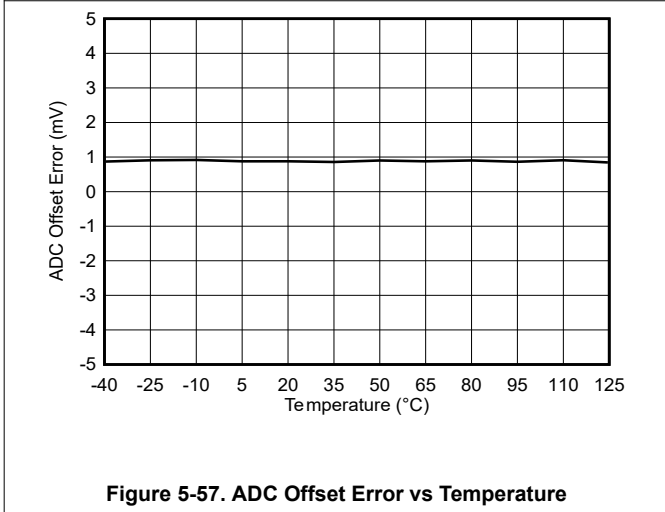
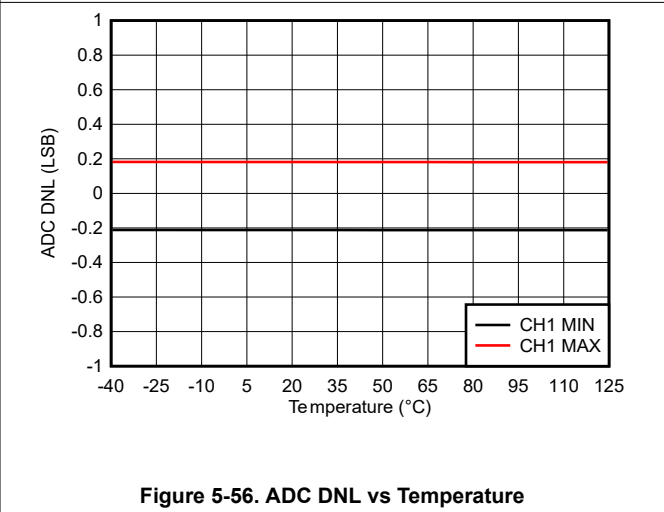
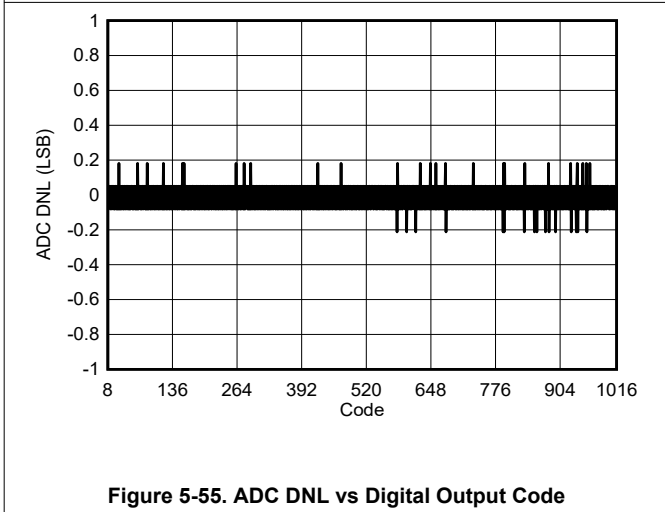
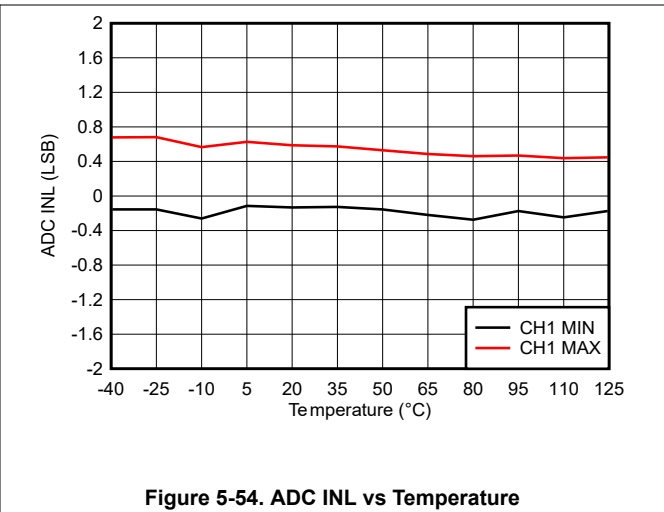
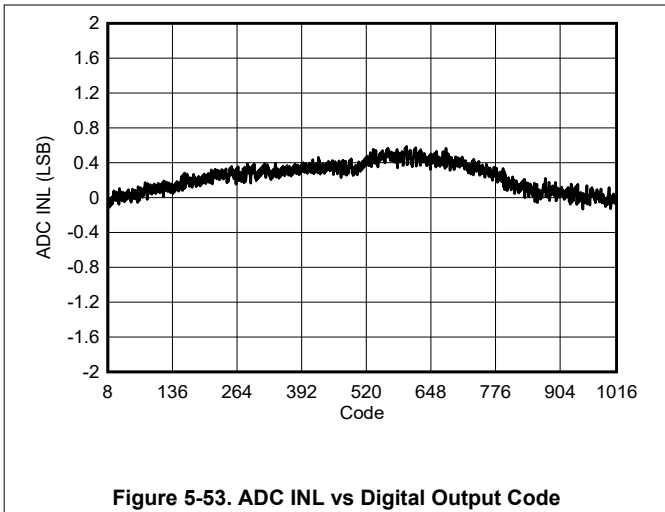


**Figure 5-52. Comparator Offset Error vs Temperature**



### 5.21 Typical Characteristics: ADC

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ ,  $V_{DD}$  as reference, gain = 1  $\times$ , 10-bit resolution, and Hi-Z input (unless otherwise noted)



## 5.22 Typical Characteristics: General

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , and DAC outputs unloaded (unless otherwise noted)

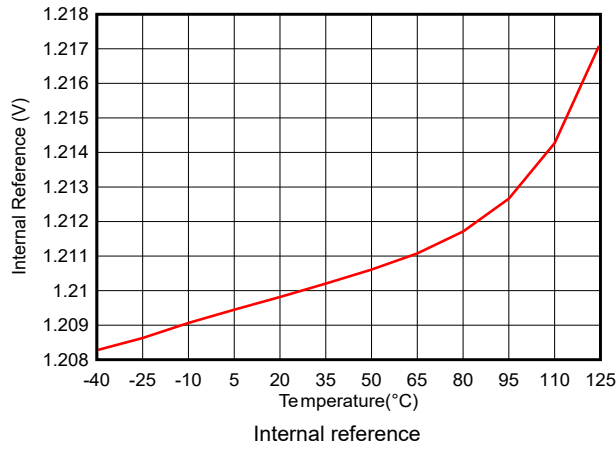


Figure 5-59. Internal Reference vs Temperature

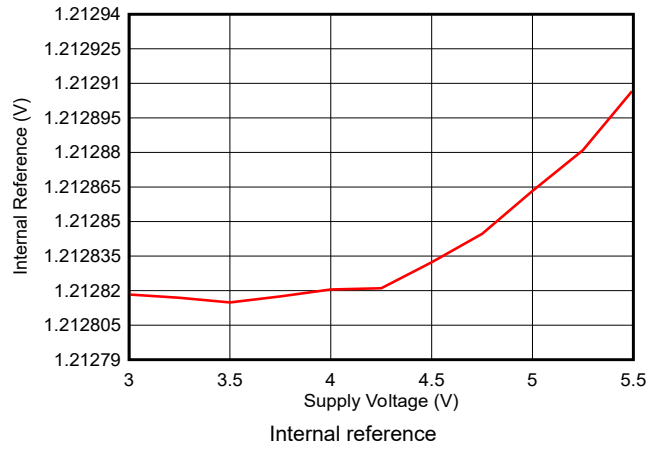


Figure 5-60. Internal Reference vs Supply Voltage

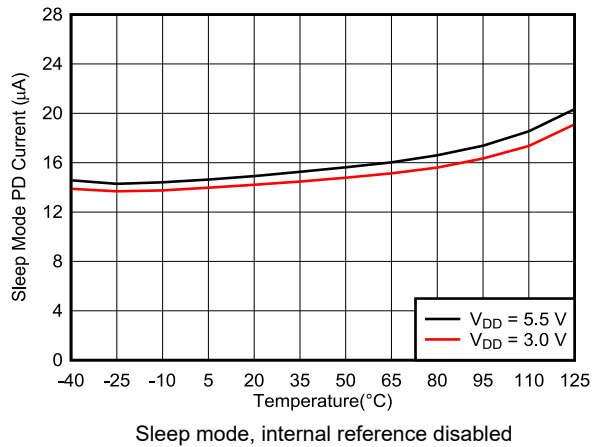


Figure 5-61. Power-Down Current vs Temperature

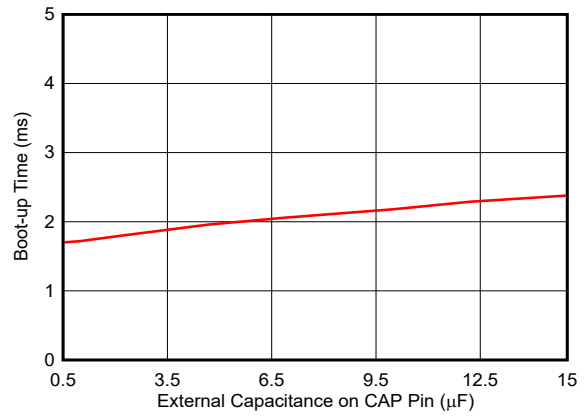


Figure 5-62. Boot-Up Time vs Capacitance on CAP pin

## 6 Detailed Description

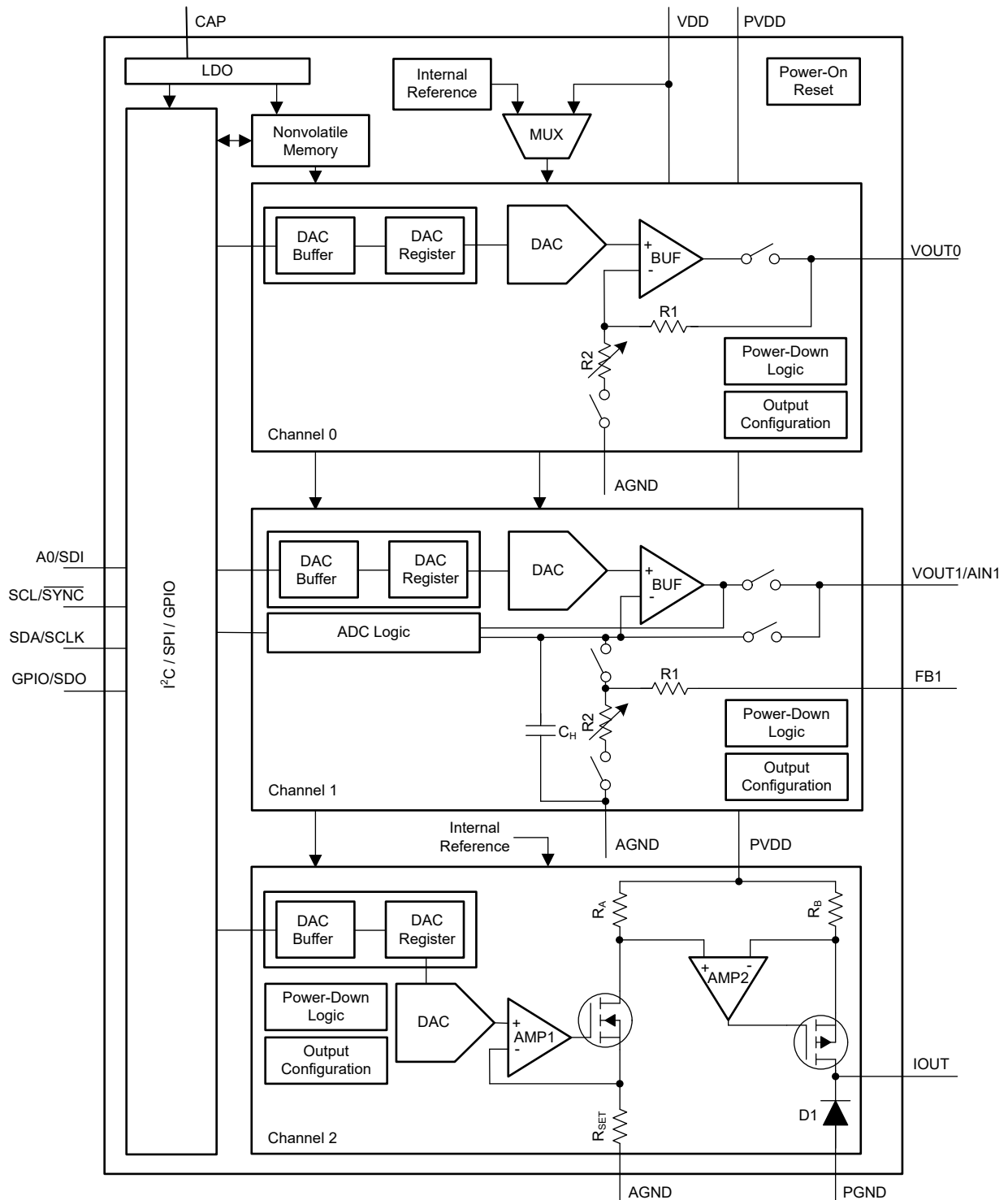
### 6.1 Overview

The 10-bit AFE532A3W and the 8-bit AFE432A3W (AFEx32A3W) are a three-channel buffered voltage-output, current-output, and ADC-input smart AFEs. The DAC channel 2 acts as a current source. The DAC channel 1 is configurable as voltage output, comparator input, or ADC input. The DAC outputs are changed to Hi-Z when VDD is off; a feature useful in voltage-margining applications. This smart AFE contains NVM, an internal reference, automatically detectable I<sup>2</sup>C or SPI, force-sense output, and a general-purpose input. This device supports Hi-Z power-down modes by default, which can be configured to 10 k $\Omega$ -GND or 100 k $\Omega$ -GND for voltage-output channels using the NVM. The AFEx32A3W has a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The AFEx32A3W operates with either an internal reference or with a power supply as the reference.

The AFEx32A3W supports I<sup>2</sup>C standard mode (100kbps), fast mode (400kbps), and fast-mode plus (1Mbps). The I<sup>2</sup>C interface can be configured with four target addresses using the A0 pin. SPI mode supports a 3-wire interface by default with up to 50-MHz SCLK input. The GPIO/SDO input can be configured as SDO in the NVM for SPI read capability. The GPIO/SDO input can alternatively be configurable as  $\overline{\text{LDAC}}$ ,  $\overline{\text{PD}}$ ,  $\overline{\text{STATUS}}$ ,  $\overline{\text{FAULT-DUMP}}$ ,  $\overline{\text{RESET}}$ , and  $\overline{\text{PROTECT}}$  functions.

The AFEx32A3W also includes digital slew rate control, and supports standard waveform generation such as *sine*, *cosine*, *triangular*, and *sawtooth* waveforms. This device can generate pulse-width modulation (PWM) output with the combination of the triangular or sawtooth waveform and the FB1 pin. The force-sense outputs of channel 1 can be used as a programmable comparator. The comparator mode allows programmable hysteresis, latching comparator, window comparator, and fault-dump to the NVM. These features enable the AFEx32A3W to go beyond the limitations of a conventional DAC that depends on a processor to function. As a result of *processor-less* operation and the *smart* feature set, the AFEx32A3W is called a smart AFE.

## 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Smart Analog Front End (AFE) Architecture

The voltage-output DAC channels of the AFE<sub>x</sub>32A3W devices consist of a string architecture with a voltage-output amplifier, as well as an external feedback pin on channel 1. [Section 6.2](#) shows the DAC architecture within the block diagram that operates from a 3-V to 5.5-V power supply. The DAC has an internal voltage reference of 1.21 V. Optionally, use the power supply as a reference. The voltage-output mode supports multiple programmable output ranges.

The AFE<sub>x</sub>32A3W devices support Hi-Z output when VDD is off, maintaining very low leakage current at the output pins with up to 1.25 V of forced voltage. The DAC output pin also starts up in high-impedance mode by default, making these devices an excellent choice for voltage margining and scaling applications. To change the power-up mode to 10 k $\Omega$ -GND or 100 k $\Omega$ -GND, program the corresponding DAC-PDN-x field in the COMMON-CONFIG register and load these bits in the device NVM.

The AFE<sub>x</sub>32A3W devices support comparator mode on channel 1. The FB1 pin acts as an input for the comparator. The DAC architecture supports inversion of the comparator output using register settings. The comparator outputs can be push-pull or open-drain. The comparator mode supports programmable hysteresis using the *margin-high* and *margin-low* register fields, latching comparator, and window comparator. The comparator outputs are accessible internally by the device.

The AFE<sub>x</sub>32A3W supports an ADC input on channel 1. Pull the FB1 to VDD in this mode and use the VOUT1/AIN1 pin as the analog input. The channel must be configured as a comparator to enable the ADC mode. Channel 0 functions as a closed-loop buffered voltage-output DAC.

Channel 2 functions as a current source with a minimum 770-mV headroom at 300-mA output. Make sure the junction temperature of the device is kept within the recommended limit while using the current output.

The AFE<sub>x</sub>32A3W devices include a *smart* feature set to enable *processor-less* operation and high integration. The NVM enables a predictable start-up. In the absence of a processor or when the processor or software fails, the GPIO triggers the DAC output without the SPI or I<sup>2</sup>C interface. The integrated functions and the FB1 pin enable PWM output for control applications.

### 6.3.2 Digital Input/Output

The AFE432A3W have four digital I/O pins that include I<sup>2</sup>C, SPI, and GPIO interfaces. These devices automatically detect I<sup>2</sup>C and SPI protocols at the first successful communication after power-on, and then connect to the detected interface. After an interface protocol is connected, any change in the protocol is ignored. The I<sup>2</sup>C interface uses the A0 pin to select from among four address options. The SPI interface is a three-wire interface by default. No readback capability is available in this mode. The GPIO/SDO pin can be configured in the register map and then programmed in to the NVM as the SDO function. The SPI readback mode is slower than the write mode. The programming interface pins are:

- I<sup>2</sup>C: SCL, SDA, A0
- SPI: SCLK, SDI,  $\overline{\text{SYNC}}$ , SDO/GPIO

The GPIO/SDO can be configured as multiple functions other than SDO. These are  $\overline{\text{LDAC}}$ ,  $\overline{\text{PD}}$ ,  $\overline{\text{STATUS}}$ ,  $\overline{\text{PROTECT}}$ ,  $\overline{\text{FAULT-DUMP}}$ , and  $\overline{\text{RESET}}$ . All the digital pins are open-drain when used as outputs. Therefore, all the output pins must be pulled up to the desired I/O voltage using external resistors.

### 6.3.3 Nonvolatile Memory (NVM)

The AFE432A3W contain NVM bits. These memory bits are user programmable and erasable, and retain the set values in the absence of a power supply. All the register bits, shown in the highlighted gray cells in [Section 7](#), can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register. The NVM-PROG is an autoresetting bit. The default values for all the registers in the AFE432A3W are loaded from NVM as soon as a POR event is issued.

The AFE432A3W also implement NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 and the device starts an NVM-reload operation. After completion, the device autoresets the NVM-RELOAD bit to 0. During the NVM write or reload operation, all read/write operations to the device are blocked. The *Electrical Characteristics: General* section provides the timing specification for the NVM write cycle. The processor must wait for the specified duration before resuming any read or write operation on the SPI or I<sup>2</sup>C interface.

## 6.4 Device Functional Modes

### 6.4.1 Voltage-Output Mode

The voltage-output mode for each DAC channel 0 and DAC channel 1 can be entered by selecting the power-up option in the DAC-PDN-0 and DAC-PDN-1 fields, respectively in the COMMON-CONFIG register. Short the VOUT1/AIN1 and FB1 pins of channel 1 externally for closed-loop amplifier output. An open FB1 pin saturates the amplifier output on channel 1. To achieve the desired voltage output, select the correct reference option, select the amplifier gain for the required output range, and program the DAC code in the DAC-0-DATA and DAC-1-DATA registers, respectively for channel 0 and channel 1.

#### 6.4.1.1 Voltage Reference and DAC Transfer Function

Figure 6-1 shows that there are two voltage reference options possible with the AFEx32A3W: internal reference and the power supply as reference. The DAC transfer function in the voltage-output and comparator modes changes based on the voltage reference selection.

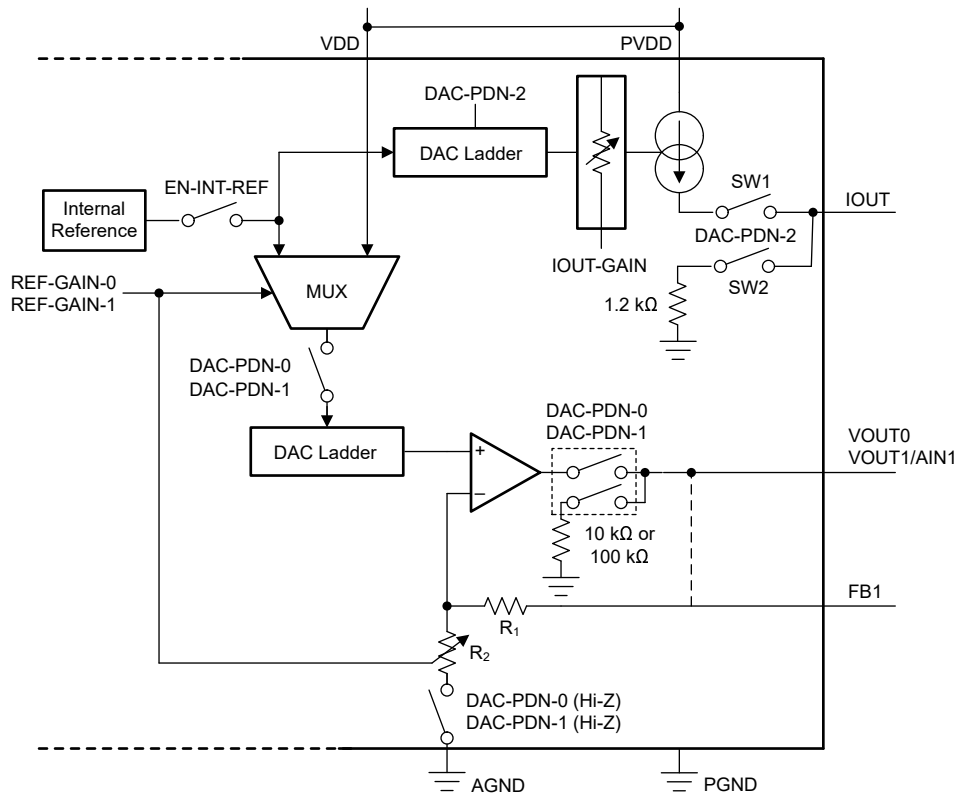


Figure 6-1. Voltage Reference Selection and Power-Down Logic

#### 6.4.1.1.1 Internal Reference

The AFE<sub>x</sub>32A3W contains an internal reference that is disabled by default. To enable the internal reference, write 1 to bit EN-INT-REF in the COMMON-CONFIG register. The internal reference generates a fixed 1.21-V voltage (typical). On channel 0, use the REF-GAIN-0 bit in the DAC-0-GAIN-CONFIG register to achieve gains of 1.5 ×, 2 ×, 3 ×, or 4 × for the DAC output voltage ( $V_{OUT}$ ). Similarly on channel 1, use the REF-GAIN-1 bit in the DAC-1-GAIN-CMP-CONFIG register. Equation 1 shows the DAC transfer function using the internal reference, in Volts.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \times GAIN \quad (1)$$

where:

- N is the resolution in bits, 10 for AFE532A3W and 8 for AFE432A3W .
- DAC\_DATA is the decimal equivalent of the binary code that is loaded to the DAC-x-DATA bit in the DAC-x-DATA register. DAC\_DATA ranges from 0 to  $2^N - 1$ .
- $V_{REF}$  is the internal reference voltage = 1.21 V (typical).
- GAIN = 1.5 ×, 2 ×, 3 ×, or 4 ×, based on REF-GAIN-x bits.

#### 6.4.1.1.2 Power-Supply as Reference

The AFE<sub>x</sub>32A3W can operate with the power-supply pin (VDD) as a reference. Equation 2 shows DAC transfer function in Volts, when the power-supply pin is used as reference. The gain at the output stage is always 1 ×.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{DD} \quad (2)$$

where:

- N is the resolution in bits, 10 for AFE532A3W and 8 for AFE432A3W .
- DAC\_DATA is the decimal equivalent of the binary code that is loaded to the DAC-x-DATA bit in the DAC-x-DATA register.
- DAC\_DATA ranges from 0 to  $2^N - 1$ .
- $V_{DD}$  is used as the DAC reference voltage.

#### 6.4.2 Current-Output Mode

To enable current output on DAC channel 2 (IOUT), write 00b to DAC-PDN-2 bits in the COMMON-CONFIG register. Select the desired current-output range by writing to the IOUT-GAIN bits in the DAC-2-GAIN-CONFIG register. The transfer function of the output current is shown in Equation 3, in Amperes.

$$I_{OUT} = \frac{DAC\_DATA}{2^N} \times GAIN \times K \quad (3)$$

where:

- N is the resolution in bits, 10 for AFE532A3W and 8 for AFE432A3W .
- DAC\_DATA is the decimal equivalent of the binary code that is loaded to the DAC-2-DATA bit as specified in the DAC-2-DATA register.
- GAIN is the value of the IOUT-GAIN setting as specified in the DAC-2-GAIN-CONFIG register.
- K is the transfer function constant, 0.5241 (typical).



### 6.4.3 Comparator Mode

DAC channel 1 can be configured as programmable comparator in the voltage-output mode. To enter the comparator mode for channel 1, write 1 to the CMP-1-EN bit in DAC-1-GAIN-CMP-CONFIG register. The comparator output can be configured as push-pull or open-drain using the CMP-1-OD-EN bit. To enable the comparator output on the output pin, write 1 to the CMP-1-OUT-EN bit. To invert the comparator output, write 1 to the CMP-1-INV-EN bit. The FB1 pin has a finite impedance. By default, the FB1 pin is in the high-impedance mode. To disable high-impedance on the FB1 pin, write 1 to the CMP-1-HIZ-IN-DIS bit. Table 6-1 shows the comparator output at the pin for different bit settings. The output of the comparator is indicated by the CMP-FLAG-1 bit in the CMP-STATUS register.

#### Note

In the Hi-Z input mode, the comparator input range is limited to:

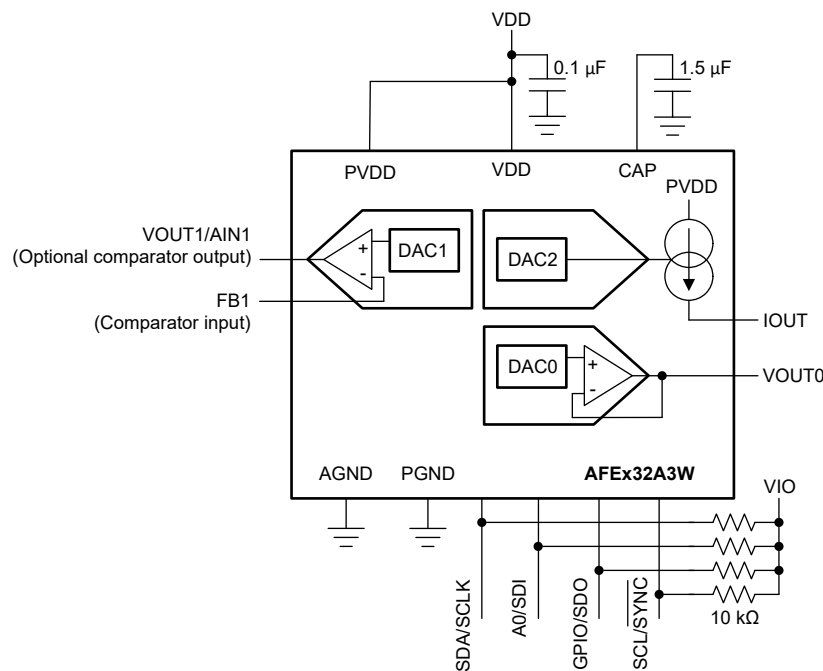
- For GAIN = 1 ×, 1.5 ×, or 2 ×:  $V_{FB1} \leq (V_{REF} \times GAIN) / 3$
- For GAIN = 3 ×, or 4 ×:  $V_{FB1} \leq (V_{REF} \times GAIN) / 6$

Any higher input voltage is clipped.

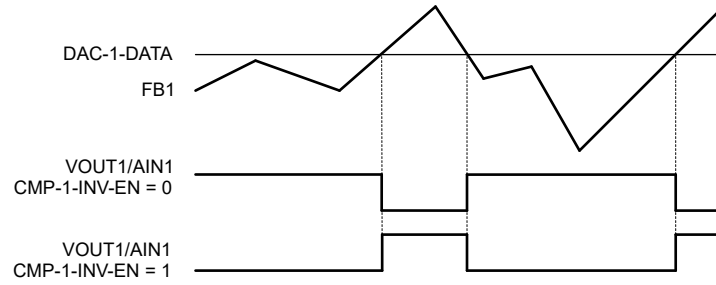
**Table 6-1. Comparator Output Configuration**

CMP-1-EN	CMP-1-OUT-EN	CMP-1-OD-EN	CMP-1-INV-EN	CMPX-OUT PIN
0	X	X	X	Comparator not enabled
1	0	X	X	No output
1	1	0	0	Push-pull output
1	1	0	1	Push-pull and inverted output
1	1	1	0	Open-drain output
1	1	1	1	Open-drain and inverted output

Figure 6-2 shows the interface circuit when DAC channel 1 is configured as a comparator. The programmable comparator operation is as shown in Figure 6-3. The comparator can be configured in no-hysteresis, with-hysteresis, and window-comparator modes using the CMP-1-MODE bit in the respective DAC-1-CMP-MODE-CONFIG register, as shown in Table 6-2.



**Figure 6-2. Comparator Interface**



**Figure 6-3. Programmable Comparator Operation**

**Table 6-2. Comparator Mode Selection**

CMP-1-MODE BIT FIELD	COMPARATOR CONFIGURATION
00	Normal comparator mode. No hysteresis or window operation.
01	Hysteresis comparator mode. DAC-1-MARGIN-HIGH and DAC-1-MARGIN-LOW registers set the hysteresis.
10	Window comparator mode. DAC-1-MARGIN-HIGH and DAC-1-MARGIN-LOW registers set the window bounds.
11	Invalid setting

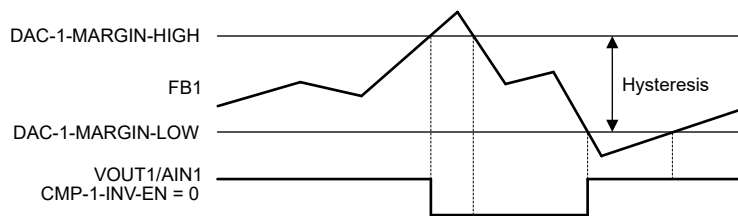
### 6.4.3.1 Programmable Hysteresis Comparator

Table 6-2 shows that comparator mode provides hysteresis when the CMP-1-MODE bit is set to 01b. Figure 6-4 shows that the hysteresis is provided by the DAC-1-MARGIN-HIGH and DAC-1-MARGIN-LOW registers.

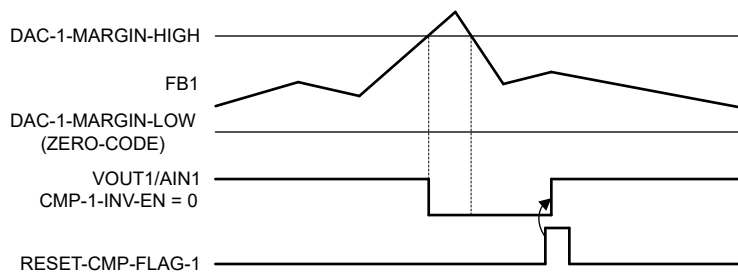
When the DAC-1-MARGIN-HIGH is set to full-code or the DAC-1-MARGIN-LOW is set to zero-code, the comparator works as a latching comparator that is, the output is latched after the threshold is crossed. The latched output can be reset by writing to the corresponding RESET-CMP-FLAG-1 bit in the COMMON-DAC-TRIG register. Figure 6-5 shows the behavior of a latching comparator with active low output, and Figure 6-6 shows the behavior of a latching comparator with active high output.

#### Note

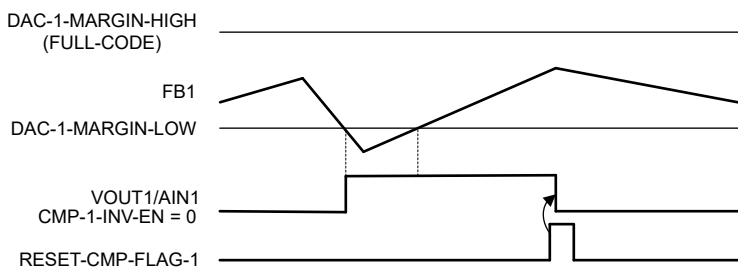
The value of the DAC-1-MARGIN-HIGH register must be greater than the value of the DAC-1-MARGIN-LOW register. The comparator output in the hysteresis mode can only be noninverting; that is, the CMP-1-INV-EN bit in the DAC-1-GAIN-CMP-CONFIG register must be set to 0. For the reset to take effect in latching mode, the input voltage must be within DAC-1-MARGIN-HIGH and DAC-1-MARGIN-LOW.



**Figure 6-4. Programmable Hysteresis Without Latching Output**



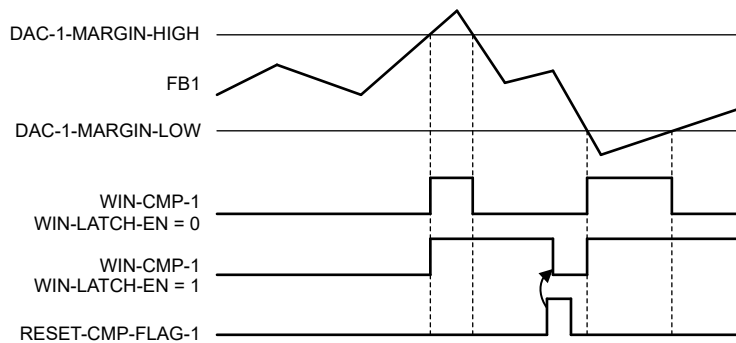
**Figure 6-5. Latching Comparator With Active Low Output**



**Figure 6-6. Latching Comparator With Active High Output**

### 6.4.3.2 Programmable Window Comparator

Window comparator mode on channel 1 is enabled by setting the CMP-1-MODE bit to 10b (see also [Table 6-2](#)). [Figure 6-7](#) shows that the window bounds are set by the DAC-1-MARGIN-HIGH and the DAC-1-MARGIN-LOW registers. The output of the window comparator is indicated by the WIN-CMP-1 bit in the CMP-STATUS register. The comparator output (WIN-CMP-1) can be latched by writing 1 to the WIN-LATCH-EN bit in the COMMON-CONFIG register. After being latched, the comparator output can be reset using the corresponding RESET-CMP-FLAG-1 bit in the COMMON-DAC-TRIG register. For the reset to take effect, the input must be within the window bounds.



**Figure 6-7. Window Comparator Operation**

A single comparator is used per channel to check both the *margin-high* and *margin-low* limits of the window. Therefore, the window comparator function has a finite response time (see also *Electrical Characteristics: Comparator Mode* section). The static behavior of the WIN-CMP-1 bit is not reflected at the output pins. Set the CMP-1-OUT-EN bit to 0. The WIN-CMP-1 bit must be read digitally using the communication interface. This bit can also be mapped to the GPIO/SDO pin (see also [Table 6-10](#)).

#### Note

- The value of the DAC-1-MARGIN-HIGH register must be greater than that of the DAC-1-MARGIN-LOW register.
- Set the SLEW-RATE-1 bit to 0000b (no-slew) and LOG-SLEW-EN-1 bit to 0b in the DAC-1-FUNC-CONFIG register to get the best response time from the window comparator.
- The CMP-1-OUT-EN bit in the DAC-1-GAIN-CMP-CONFIG register can be set to 0b to eliminate undesired toggling of the VOUT1/AIN1 pin.

### 6.4.4 Analog-to-Digital Converter (ADC) Mode

AFE432A3W support integrated ADC on channel 1. Connect FB1 to VDD using a pullup resistor. Channel 1 must be configured as a comparator. The transfer function of the ADC is given in Equation 4.

$$\text{ADC\_DATA} = \left( \text{INTEGER} \right) \left( \frac{V_{\text{IN}}}{V_{\text{FS}}} \right) \times 2^N \tag{4}$$

where

- ADC\_DATA is the output of the ADC-DATA register.
- V<sub>IN</sub> is the input voltage at the VOUT1/AIN1 pin.
- V<sub>FS</sub> is the full-scale input voltage as provided in Table 6-3.
- N is the number of ADC bits, 10.
- (INTEGER) denotes integer division.

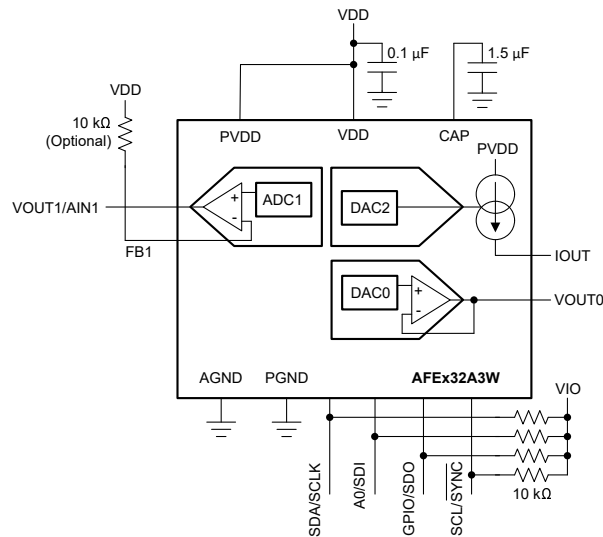
**Table 6-3. Full Scale Analog Input (V<sub>FS</sub>)**

REFERENCE (VREF)	GAIN	V <sub>FS</sub>
Power supply	1 ×	VDD/3
Internal	1.5 ×	(VREF × GAIN)/3
	2 ×	(VREF × GAIN)/3
	3 ×	(VREF × GAIN)/6
	4 ×	(VREF × GAIN)/6

Follow these steps to configure and read data from ADC on channel 1:

1. Configure the gain using the REF-GAIN-1 bits in the DAC-1-GAIN-CMP-CONFIG register.
2. Configure DAC channel 1 as comparator by writing 1 to the CMP-1-EN bit in the DAC-1-GAIN-CMP-CONFIG register.
3. Enable the ADC (ADC-EN bit) and select the number of averages (ADC-AVG) in the ADC-CONFIG-TRIG register.
4. Start the ADC conversion by writing 1 to the TRIG-ADC bit in the ADC-CONFIG-TRIG register.
5. Read the ADC data using the ADC-DATA register. The data is valid when the ADC-DRDY bit is 1. Repeat steps 4 and 5 for every ADC readback.

Figure 6-8 shows the interface example for the ADC on channel 1.



**Figure 6-8. ADC Interface**

### 6.4.5 Fault-Dump Mode

The AFEx32A3W provides a feature to save a few registers into the NVM when the FAULT-DUMP bit is triggered or when the GPIO mapped to fault-dump is triggered (see also [Table 6-9](#)). This feature is useful in system-level fault management to capture the state of the device or system just before a fault is triggered, and to allow diagnosis after the fault has occurred. The registers saved when fault-dump is triggered, are:

- CMP-STATUS[7:0]
- DAC-0-DATA[15:8]
- DAC-1-DATA[15:8]
- DAC-2-DATA[15:8]
- ADC-DATA [15:0]

---

#### Note

When the fault-dump cycle is in progress, any change in the data can corrupt the final outcome. Make sure the comparator and the DAC codes are stable during the NVM write cycle.

---

[Table 6-4](#) shows the storage format of the registers in the NVM.

**Table 6-4. Fault-Dump NVM Storage Format**

NVM ROWS	B31-B24	B23-B16	B15-B8	B7-B0
Row1	CMP-STATUS[7:0]	ADC-DATA[15:0]		Don't care
Row2	DAC-2-DATA[15:8]	Don't care	DAC-0-DATA[15:8]	DAC-1-DATA[15:8]

The data captured in the NVM after the fault dump can be read in a specific sequence:

1. Set the EE-READ-ADDR bit to 0b in the COMMON-CONFIG register, to select row1 of the NVM.
2. Trigger the read of the selected NVM row by writing 1 to the READ-ONE-TRIG in the COMMON-TRIGGER register; this bit autoresets. This action copies that data from the selected NVM row to SRAM addresses 0x9D (LSB 16 bits from the NVM) and 0x9E (MSB 16 bits from the NVM).
3. To read the SRAM data:
  - a. Write 0x009D to the SRAM-CONFIG register.
  - b. Read the data from the SRAM-DATA register to get the LSB 16 bits.
  - c. Write 0x009E to the SRAM-CONFIG register.
  - d. Read the data from the SRAM-DATA register again to get the MSB bits.
4. Set the EE-READ-ADDR bit to 1b in the COMMON-CONFIG register, to select row2 of the NVM. Repeat steps 2 and 3.

## 6.4.6 Application-Specific Modes

This section provides the details of application-specific functional modes available in the AFEx32A3W.

### 6.4.6.1 Voltage Margining and Scaling

Voltage margining or scaling is a primary application for the AFEx32A3W. This section provides specific features available for this application such as Hi-Z output, slew-rate control, and  $\overline{\text{PROTECT}}$  input.

#### 6.4.6.1.1 High-Impedance Output and $\overline{\text{PROTECT}}$ Input

All the DAC output channels remain in a Hi-Z when VDD is off. Figure 6-9 shows a simplified schematic of the AFEx32A3W used in a voltage-margining application. Almost all linear regulators and DC/DC converters have a feedback voltage of  $\leq 1.25$  V. The low-leakage currents at the outputs are maintained for  $V_{\text{FB}}$  of  $\leq 1.25$  V. Thus, for all practical purposes, the DAC outputs appear as Hi-Z when VDD of the DAC is off in voltage margining and scaling applications. This feature allows for seamless integration of the AFEx32A3W into a system without any need for additional power-supply sequencing for the DAC.

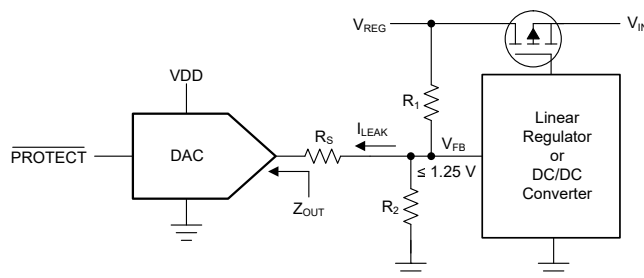


Figure 6-9. High-Impedance (Hi-Z) Output and  $\overline{\text{PROTECT}}$  Input

The DAC channels power down to Hi-Z at boot up. The outputs can power up with a preprogrammed code that corresponds to the nominal output of the DC/DC converter or the linear regulator. This feature allows for smooth power up and power down of the DAC without impacting the feedback loop of the DC/DC converter or the linear regulator.

Table 6-9 shows how the GPIO/SDO pin of the AFEx32A3W can be configured as a  $\overline{\text{PROTECT}}$  function.  $\overline{\text{PROTECT}}$  takes the DAC outputs to a predictable state with a slewed or direct transition. This function is useful in systems where a fault condition (such as a brownout), a subsystem failure, or a software crash requires that the DAC outputs reach a predefined state without the involvement of a processor. The detected event can be fed to the GPIO/SDO pin that is configured as the  $\overline{\text{PROTECT}}$  input. The  $\overline{\text{PROTECT}}$  function can also be triggered using the PROTECT bit in the COMMON-TRIGGER register. Table 6-5 shows how to configure the behavior of the  $\overline{\text{PROTECT}}$  function in the PROTECT-CONFIG field in the DEVICE-MODE-CONFIG register.

#### Note

- After the  $\overline{\text{PROTECT}}$  function is triggered, the write functionality is disabled on the communication interface until the function is completed.
- The PROTECT-FLAG bit in the CMP-STATUS register is set to 1 when the  $\overline{\text{PROTECT}}$  function is triggered. This bit can be polled by reading the CMP-STATUS register. After the  $\overline{\text{PROTECT}}$  function is complete, a read command on the CMP-STATUS register resets the PROTECT-FLAG bit.

Table 6-5.  $\overline{\text{PROTECT}}$  Function Configuration

PROTECT-CONFIG FIELD	FUNCTION
00	Switch to Hi-Z power-down (no slew).
01	Switch to DAC code stored in NVM (no slew) and then switch to Hi-Z power-down.
10	Slew to margin-low code and then switch to Hi-Z power-down.
11	Slew to margin-high code and then switch to Hi-Z power-down.

#### 6.4.6.1.2 Programmable Slew-Rate Control

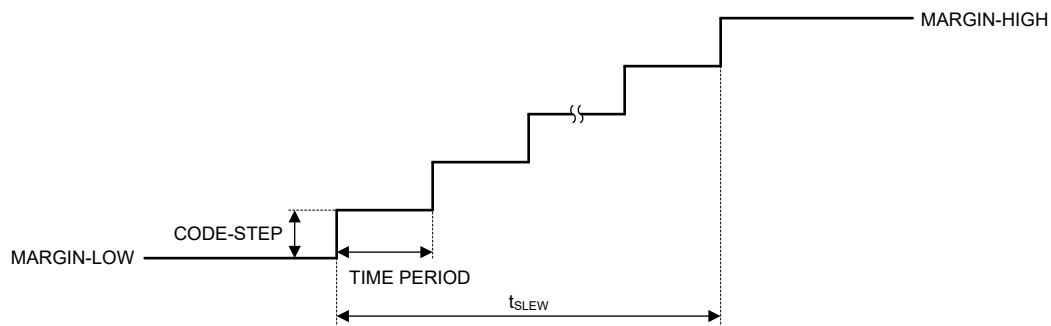
When the DAC data registers are written, the voltage ( $V_{OUTX}$ ) or current ( $I_{OUT}$ ) on DAC output immediately transitions to the new code following the slew rate and settling time specified in the *Electrical Characteristics*.

The slew rate control feature allows the user to control the rate at which the output voltage ( $V_{OUT}$ ) changes. When this feature is enabled (using the SLEW-RATE-x[3:0] bits), the DAC output changes from the current code to the code in the DAC-x-MARGIN-HIGH or DAC-x-MARGIN-LOW registers (when margin high or low commands are issued to the DAC) using the step size and time-period per step set in CODE-STEP-x and SLEW-RATE-x bits in the DAC-x-FUNC-CONFIG register:

- SLEW-RATE-x defines the time-period per step at which the digital slew updates.
- CODE-STEP-x defines the number of LSBs by which the output value changes at each update, for the corresponding channels.

Table 6-6 and Table 6-7 show different settings available for CODE-STEP-x and SLEW-RATE-x. With the default slew rate control setting of no-slew, the output changes immediately at a rate limited by the output drive circuitry and the attached load.

When the slew rate control feature is used, the output changes happen at the programmed slew rate. Figure 6-10 shows that this configuration results in a staircase formation at the output. Do not write to CODE-STEP-x, SLEW-RATE-x, or DAC-x-DATA during the output slew operation. Equation 5 provides the equation for the calculating the slew time ( $t_{SLEW}$ ).



**Figure 6-10. Programmable Slew-Rate Control**

$$t_{SLEW} = SLEW\_RATE \times CEILING\left(\frac{MARGIN\_HIGH - MARGIN\_LOW}{CODE\_STEP} + 1\right) \quad (5)$$

where:

- SLEW\_RATE is the SLEW-RATE-x setting specified in Table 6-7.
- CODE\_STEP is the CODE-STEP-x setting specified in Table 6-6.
- MARGIN\_HIGH is the decimal value of the DAC-x-MARGIN-HIGH bits in the DAC-x-MARGIN-HIGH register.
- MARGIN\_LOW is the decimal value of the DAC-x-MARGIN-LOW bits in the DAC-x-MARGIN-LOW register.



**Table 6-6. Code Step**

REGISTER	CODE-STEP-x[2]	CODE-STEP-x[1]	CODE-STEP-x[0]	CODE STEP SIZE
DAC-x-FUNC-CONFIG	0	0	0	1 LSB (default)
	0	0	1	2 LSB
	0	1	0	3 LSB
	0	1	1	4 LSB
	1	0	0	6 LSB
	1	0	1	8 LSB
	1	1	0	16 LSB
	1	1	1	32 LSB

**Table 6-7. Slew Rate**

REGISTER	SLEW-RATE-x[3]	SLEW-RATE-x[2]	SLEW-RATE-x[1]	SLEW-RATE-x[0]	TIME PERIOD (PER STEP)
DAC-x-FUNC-CONFIG	0	0	0	0	No slew (default)
	0	0	0	1	4 $\mu$ s
	0	0	1	0	8 $\mu$ s
	0	0	1	1	12 $\mu$ s
	0	1	0	0	18 $\mu$ s
	0	1	0	1	27 $\mu$ s
	0	1	1	0	40.5 $\mu$ s
	0	1	1	1	60.75 $\mu$ s
	1	0	0	0	91.13 $\mu$ s
	1	0	0	1	136.69 $\mu$ s
	1	0	1	0	239.2 $\mu$ s
	1	0	1	1	418.61 $\mu$ s
	1	1	0	0	732.56 $\mu$ s
	1	1	0	1	1281.98 $\mu$ s
	1	1	1	0	2563.96 $\mu$ s
1	1	1	1	5127.92 $\mu$ s	

### 6.4.6.2 Function Generation

The AFE<sub>x</sub>32A3W implement a continuous function or waveform generation feature. These devices can generate a triangular wave, sawtooth wave, and sine wave independently for every channel.

#### 6.4.6.2.1 Triangular Waveform Generation

Figure 6-11 shows that the triangular waveform uses the DAC-x-MARGIN-LOW (FUNCTION-MIN) and DAC-x-MARGIN-HIGH (FUNCTION-MAX) registers for minimum and maximum levels, respectively. The frequency of the waveform depends on the min and max levels, CODE-STEP and SLEW-RATE settings as shown in Equation 6. An external RC load with a time-constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The CODE-STEP-x and SLEW-RATE-x settings are available in the DAC-x-FUNC-CONFIG register. Writing 0b000 to the FUNC-CONFIG-x bit field in the DAC-x-FUNC-CONFIG register selects triangular waveform.

$$f_{\text{TRIANGLE}} = \frac{1}{2 \times \text{TIME\_STEP} \times \text{CEILING}\left(\frac{\text{FUNCTION\_MAX} - \text{FUNCTION\_MIN}}{\text{CODE\_STEP}}\right)} \quad (6)$$

where

- TIME\_STEP is the SLEW-RATE-x setting specified in Table 6-7.
- CODE\_STEP is the CODE-STEP-x setting specified in Table 6-6.
- FUNCTION\_MAX is the decimal value of DAC-x-MARGIN-HIGH bits in the DAC-x-MARGIN-HIGH register.
- FUNCTION\_MIN is the decimal value of the DAC-x-MARGIN-LOW bits in the DAC-x-MARGIN-LOW register.

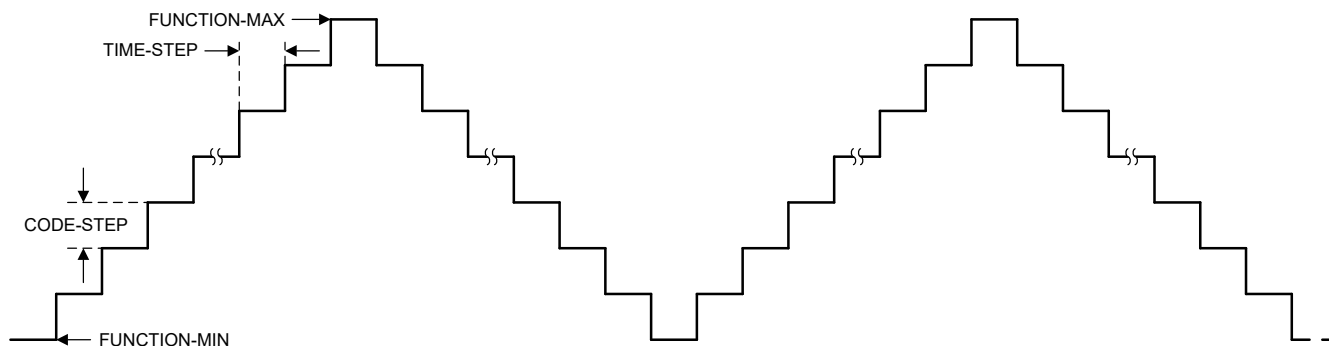


Figure 6-11. Triangle Waveform

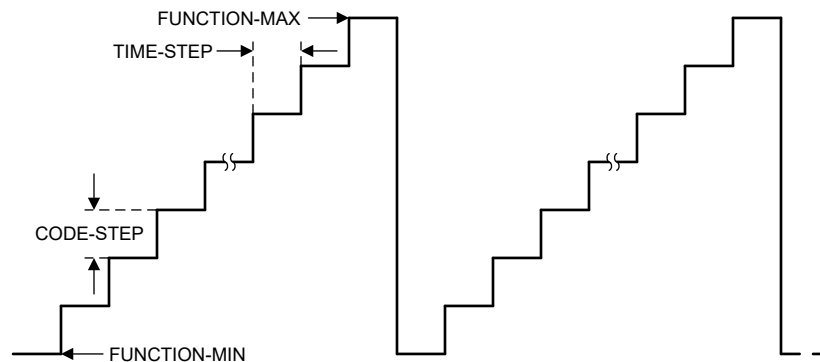
#### 6.4.6.2.2 Sawtooth Waveform Generation

Figure 6-12 shows the sawtooth and the inverse sawtooth waveforms use the DAC-x-MARGIN-LOW (FUNCTION-MIN) and DAC-x-MARGIN-HIGH (FUNCTION-MAX) registers for minimum and maximum levels, respectively. The frequency of the waveform depends on the min and max levels, CODE-STEP and SLEW-RATE settings as shown in Equation 7. An external RC load with a time constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The CODE-STEP-x and SLEW-RATE-x settings are available in the DAC-x-FUNC-CONFIG register. Write 0b001 to the FUNC-CONFIG-x bit field in the DAC-x-FUNC-CONFIG register to select sawtooth waveform, and write 0b010 to select inverse sawtooth waveform.

$$f_{\text{SAWTOOTH}} = \frac{1}{\text{TIME\_STEP} \times \text{CEILING}\left(\frac{\text{FUNCTION\_MAX} - \text{FUNCTION\_MIN}}{\text{CODE\_STEP}} + 1\right)} \quad (7)$$

where

- TIME\_STEP is the SLEW-RATE-x setting specified in Table 6-7.
- CODE\_STEP is the CODE-STEP-x setting specified in Table 6-6.
- FUNCTION\_MAX is the decimal value of the DAC-x-MARGIN-HIGH bits in the DAC-x-MARGIN-HIGH register.
- FUNCTION\_MIN is the decimal value of the DAC-x-MARGIN-LOW bits in the DAC-x-MARGIN-LOW register.



**Figure 6-12. Sawtooth Waveform**

### 6.4.6.2.3 Sine Waveform Generation

The sine wave function uses 24 preprogrammed points per cycle. The frequency of the sine wave depends on the SLEW-RATE settings as shown in Equation 8:

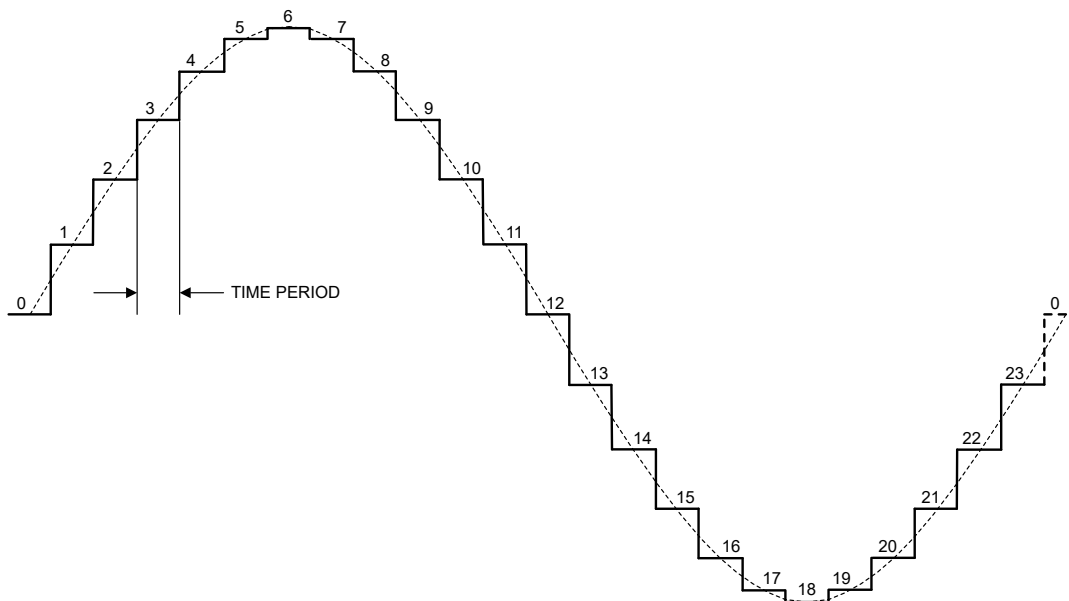
$$f_{\text{SINE\_WAVE}} = \frac{1}{24 \times \text{SLEW\_RATE}} \quad (8)$$

where SLEW\_RATE is the SLEW-RATE-x setting as specified in Table 6-7.

An external RC load with a time constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The SLEW-RATE-x setting is available in the DAC-x-FUNC-CONFIG register. Writing 0b100 to the FUNC-CONFIG-x bit field in the DAC-x-FUNC-CONFIG register selects sine wave. The codes for the sine wave are fixed. Use the gain settings at the output amplifier for changing the full-scale output using the internal reference option. The gain settings are accessible through the DAC-GAIN-0, DAC-GAIN-1, and IOUT-GAIN bits in the DAC-0-GAIN-CONFIG, DAC-1-GAIN-CMP-CONFIG, and DAC-2-GAIN-CONFIG registers, respectively. Table 6-8 shows the list of hard-coded discrete points for the sine wave with 12-bit resolution and Figure 6-13 shows the pictorial representation of the sine wave. There are four phase settings available for the sine wave that are selected using the PHASE-SEL-x bit in the DAC-x-FUNC-CONFIG register.

**Table 6-8. Sine Wave Data Points**

SEQUENCE	12-BIT VALUE	SEQUENCE	12-BIT VALUE
0 (0° phase start)	0x800	12	0x800
1	0x9A8	13	0x658
2	0xB33	14	0x4CD
3	0xC87	15	0x379
4	0xD8B	16 (240° phase start)	0x275
5	0xE2F	17	0x1D1
6 (90° phase start)	0xE66	18	0x19A
7	0xE2F	19	0x1D1
8 (120° phase start)	0xD8B	20	0x275
9	0xC87	21	0x379
10	0xB33	22	0x4CD
11	0x9A8	23	0x658



**Figure 6-13. Sine Wave Generation**

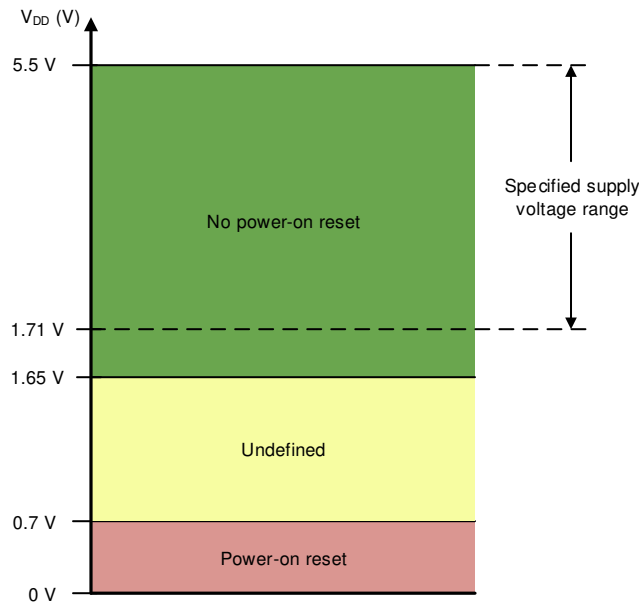
## 6.4.7 Device Reset and Fault Management

This section provides the details of power-on-reset (POR), software reset, and other diagnostics and fault-management features of AFE32A3W.

### 6.4.7.1 Power-On Reset (POR)

The AFE32A3W family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the  $V_{DD}$  supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a POR (boot-up) delay. The default value for all the registers in the AFE32A3W is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. Figure 6-14 indicates that the POR circuit requires specific  $V_{DD}$  levels to make sure that the internal capacitors discharge and reset the device at power up. To make sure that a POR occurs,  $V_{DD}$  must be less than 0.7 V for at least 1 ms. When  $V_{DD}$  drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When  $V_{DD}$  remains greater than 1.65 V, a POR does not occur.



**Figure 6-14. Threshold Levels for  $V_{DD}$  POR Circuit**

### 6.4.7.2 External Reset

An external reset to the device can be triggered through the GPIO/SDO pin or through the register map. To initiate a device software reset event, write the reserved code 1010b to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event. Table 6-9 shows how the GPIO/SDO pin can be configured as a  $\overline{\text{RESET}}$  pin. This configuration must be programmed into the NVM so that the setting is not cleared after the device reset. The  $\overline{\text{RESET}}$  input must be a low pulse. The device starts the boot-up sequence after the falling edge of the  $\overline{\text{RESET}}$  input. The rising edge of the  $\overline{\text{RESET}}$  input does not have any effect.

### 6.4.7.3 Register-Map Lock

The AFE32A3W implement a register-map lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. However, the software reset function through the COMMON-TRIGGER register is not blocked when using the I<sup>2</sup>C interface. To bypass the DEV-LOCK setting, write 0101b to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

#### 6.4.7.4 NVM Cyclic Redundancy Check (CRC)

The AFEx32A3W implement a cyclic redundancy check (CRC) feature for the NVM to make sure that the data stored in the NVM is uncorrupted. There are two types of CRC alarm bits implemented in AFEx32A3W:

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

The NVM-CRC-FAIL-USER bit indicates the status of user-programmable NVM bits, and the NVM-CRC-FAIL-INT bit indicates the status of internal NVM bits. The CRC feature is implemented by storing a 16-bit CRC (CRC-16-CCITT) along with the NVM data each time NVM program operation (write or reload) is performed and during the device start up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM-CRC-FAIL-USER and NVM-CRC-FAIL-INT in the GENERAL-STATUS register) report any errors after the data are read from the device NVM. The alarm bits are set only at boot up.

##### 6.4.7.4.1 NVM-CRC-FAIL-USER Bit

A logic 1 on NVM-CRC-FAIL-USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see also [Section 6.4.7.2](#)) command, or cycle power to the DAC. A software reset or power-cycle also reloads the user-programmable NVM bits. In case the failure persists, reprogram the NVM.

##### 6.4.7.4.2 NVM-CRC-FAIL-INT Bit

A logic 1 on NVM-CRC-FAIL-INT bit indicates that the internal NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset (see also [Section 6.4.7.2](#)) command or cycle power to the DAC. A permanent failure in the NVM makes the device unusable.

#### 6.4.8 General-Purpose Input/Output (GPIO) Modes

Together with I<sup>2</sup>C and SPI, the AFEx32A3W also support a GPIO that can be configured in the NVM for multiple functions. This pin allows for updating the DAC output channels and reading status bits without using the programming interface, thus enabling *processor-less* operation. In the GPIO-CONFIG register, write 1 to the GPI-EN bit to set the GPIO/SDO pin as an input, or write 1 to the GPO-EN bit to set the pin as output. There are global and channel-specific functions mapped to the GPIO/SDO pin. For channel-specific functions, select the channels using the GPI-CH-SEL field in the GPIO-CONFIG register. [Table 6-9](#) lists the functional options available for the GPIO as input and [Table 6-10](#) lists the options for the GPIO as output. Some of the GP input operations are edge-triggered after the device boots up. After the power supply ramps up, the device registers the GPI level and executes the associated command. This feature allows the user to configure the initial output state at power-on. By default, the GPIO/SDO pin is not mapped to any operation. When the GPIO/SDO pin is mapped to a specific input function, the corresponding software bit functionality is disabled to avoid a race condition. When used as a  $\overline{\text{RESET}}$  input, the GPIO/SDO pin must transmit an active-low pulse for triggering a device reset. All other constraints of the functions are applied to the GPIO-based trigger.

---

#### Note

Pull the GPIO/SDO pin high or low when not used. When the GPIO/SDO pin is used as  $\overline{\text{RESET}}$ , the configuration must be programmed into the NVM. Otherwise, the setting is cleared after the device resets.

---

**Table 6-9. General-Purpose Input Function Map**

REGISTER	BIT FIELD	VALUE	CHANNELS	GPIO EDGE / LEVEL	FUNCTION
GPIO-CONFIG	GPI-CONFIG	0010	All	Falling edge	Trigger FAULT-DUMP
				Rising edge	No effect
		0100	As per GPI-CH-SEL	Falling edge	Channel power-down. Pulldown resistor as per the DAC-PDN-x setting
				Rising edge	Channel power-up
		0101	All	Falling edge	Trigger $\overline{\text{PROTECT}}$ function
				Rising edge	No effect
		0111	All	Falling edge	Trigger $\overline{\text{CLR}}$ function
				Rising edge	No effect
		1000	As per GPI-CH-SEL, both the SYNC-CONFIG-x and the GPI-CH-SEL must be configured for every channel.	Falling edge	Trigger $\overline{\text{LDAC}}$ function
				Rising edge	No effect
		1001	As per GPI-CH-SEL	Falling edge	Stop function generation
				Rising edge	Start function generation
		1010	As per GPI-CH-SEL	Falling edge	Trigger margin-low
				Rising edge	Trigger margin-high
		1011	All	Low pulse	Trigger device RESET. The RESET configuration must be programmed into the NVM.
				Rising edge	No effect
		1100	All	Falling edge	Allows NVM programming
				Rising edge	Blocks NVM programming
		1101	All	Falling edge	Allows register map update
				Rising edge	Blocks register map write except a write to the DEV-UNLOCK field through I <sup>2</sup> C or SPI and the RESET fields through I <sup>2</sup> C
Others	N/A	N/A	Not applicable		

**Table 6-10. General-Purpose Output (STATUS) Function Map**

REGISTER	BIT FIELD	VALUE	FUNCTION
GPIO-CONFIG	GPO-CONFIG	0000	ADC-DRDY
		0001	NVM-BUSY
		0100	DAC-2-BUSY
		0110	DAC-0-BUSY
		0111	DAC-1-BUSY
		1011	WIN-CMP-1
		Others	Not applicable

## 6.5 Programming

The AFE<sub>x</sub>32A3W are programmed through either a 3-wire SPI or 2-wire I<sup>2</sup>C interface. A 4-wire SPI mode is enabled by mapping the GPIO/SDO pin as SDO. The SPI readback operates at a lower SCLK than the standard SPI write operation. The type of interface is determined based on the first protocol to communicate after device power up. After the interface type is determined, the device ignores any change in the type while the device is on. The interface type can be changed after a power cycle.

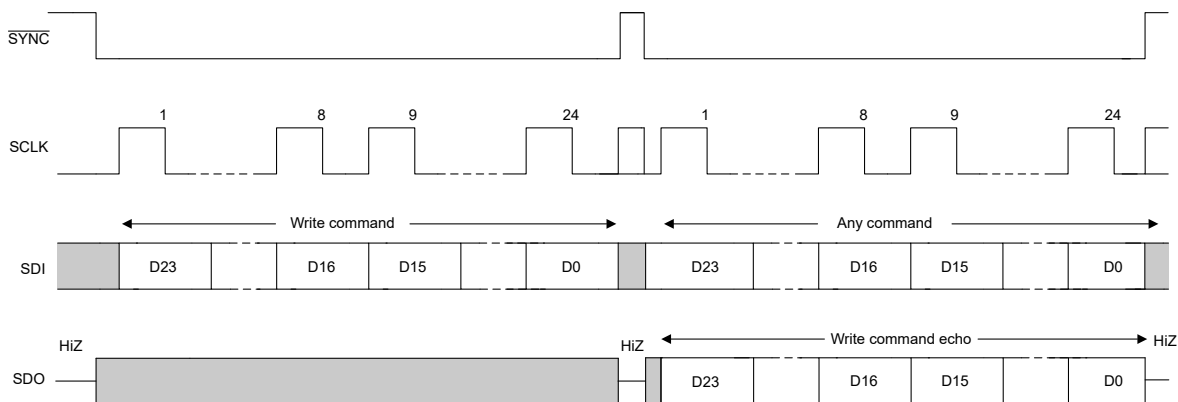
### 6.5.1 SPI Programming Mode

To initiate an SPI access cycle for the AFE<sub>x</sub>32A3W, assert the  $\overline{\text{SYNC}}$  pin low. The serial clock, SCLK, is a continuous or gated clock. SDI data are clocked on SCLK falling edges. The SPI frame for AFE<sub>x</sub>32A3W is 24 bits long. Therefore, ensure that the  $\overline{\text{SYNC}}$  pin stays low for at least 24 SCLK falling edges. The access cycle ends when the  $\overline{\text{SYNC}}$  pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. By default, the SDO function is not enabled (three-wire SPI). In the three-wire SPI mode, if the access cycle contains more than the minimum clock edges, only the first 24 bits are used by the device. When  $\overline{\text{SYNC}}$  is high, the SCLK and SDI signals are blocked, and SDO becomes Hi-Z to allow data readback from other devices connected on the bus.

Table 6-11 and Figure 6-15 describe the format for the 24-bit SPI access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 7-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

**Table 6-11. SPI Read/Write Access Cycle**

BIT	FIELD	DESCRIPTION
23	R/W	Identifies the communication as a read or write command to the address register: R/W = 0 sets a write operation. R/W = 1 sets a read operation
22-16	A[6:0]	Register address: specifies the register to be accessed during the read or write operation
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are <i>don't care</i> values.



**Figure 6-15. SPI Write Cycle**

Read operations require that the SDO function is first enabled by setting the SDO-EN bit in the INTERFACE-CONFIG register. This configuration is called four-wire SPI. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. Table 6-12 and Figure 6-16 show the output data format. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit (see also Figure 5-3).

**Table 6-12. SDO Output Access Cycle**

BIT	FIELD	DESCRIPTION
23	R/W	Echo R/W from previous access cycle
22-16	A[6:0]	Echo register address from previous access cycle
15-0	DI[15:0]	Readback data requested on previous access cycle



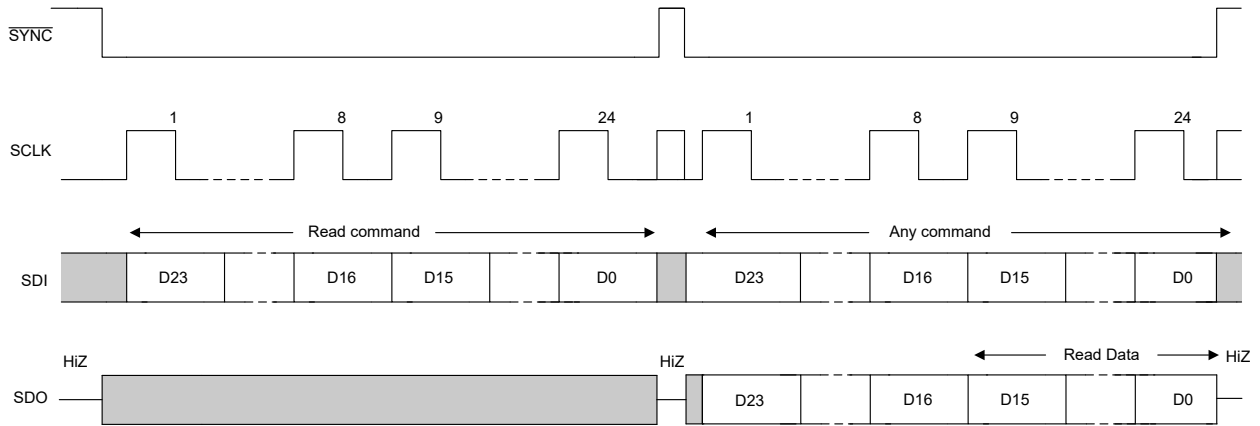


Figure 6-16. SPI Read Cycle

The daisy-chain operation is also enabled with the SDO pin. Figure 6-17 shows that in daisy-chain mode, multiple devices are connected in a *chain* with the SDO pin of one device is connected to SDI pin of the following device. The SPI host drives the SDI pin of the first device in the chain. The SDO pin of the last device in the chain is connected to the POCI pin of the SPI host. In four-wire SPI mode, if the access cycle contains multiples of 24 clock edges, only the last 24 bits are used by the device first device in the chain. If the access cycle contains clock edges that are not in multiples of 24, the SPI packet is ignored by the device. Figure 6-18 describes the packet format for the daisy-chain write cycle.

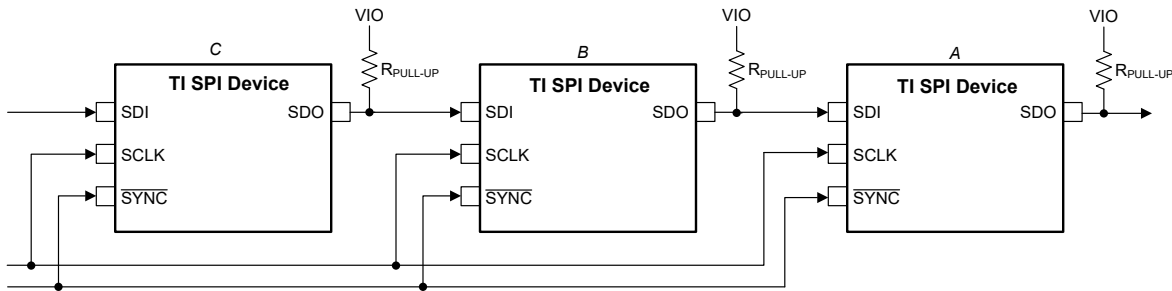


Figure 6-17. SPI Daisy-Chain Connection

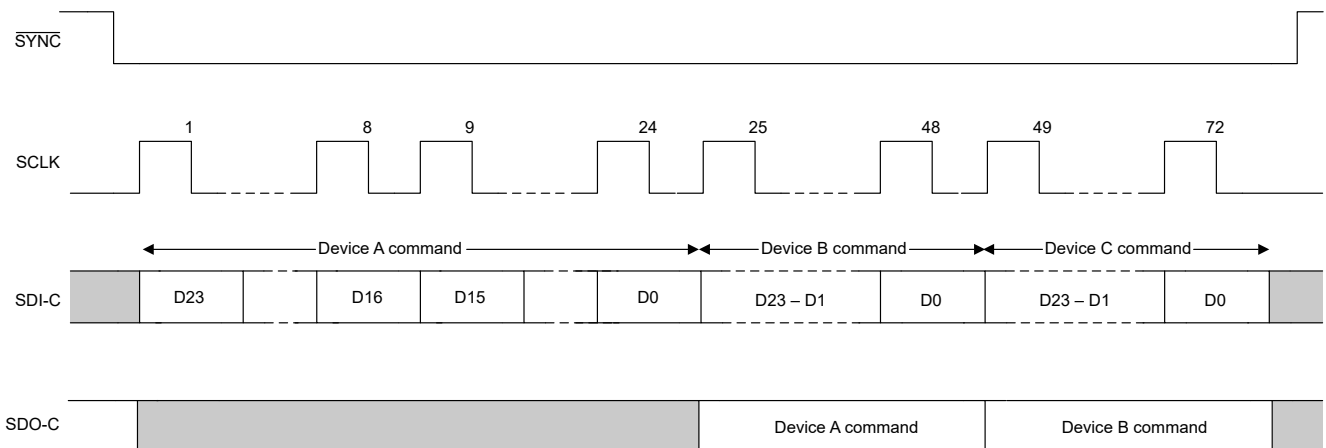


Figure 6-18. SPI Daisy-Chain Write Cycle

### 6.5.2 I<sup>2</sup>C Programming Mode

The AFEx32A3W devices have a 2-wire serial interface (SCL and SDA), and one address pin (A0); see also the pin diagram in the *Pin Configuration and Functions* section. The I<sup>2</sup>C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I<sup>2</sup>C-compatible devices connect to the I<sup>2</sup>C bus through the open drain I/O pins, SDA and SCL.

The I<sup>2</sup>C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller generates the SCL signal. The controller also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller on an I<sup>2</sup>C bus is typically a microcontroller or digital signal processor (DSP). The AFEx32A3W family operates as a target on the I<sup>2</sup>C bus. A target acknowledges controller commands, and upon controller control, receives or transmits data.

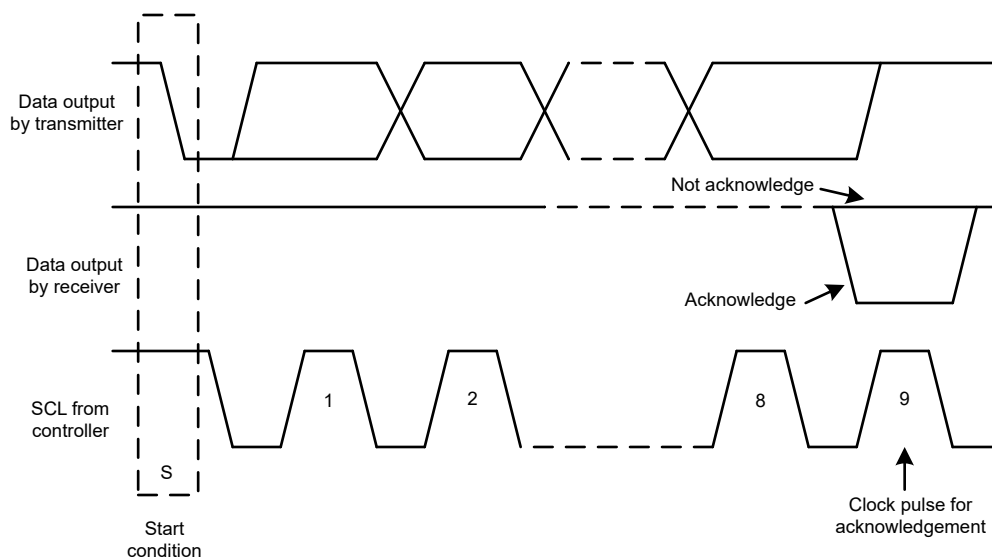
Typically, the AFEx32A3W family operates as a target receiver. A controller writes to the AFEx32A3W, a target receiver. However, if a controller requires the AFEx32A3W internal register data, the AFEx32A3W operate as a target transmitter. In this case, the controller reads from the AFEx32A3W. According to I<sup>2</sup>C terminology, read and write refer to the controller.

The AFEx32A3W family supports the following data transfer modes:

- Standard mode (100Kbps)
- Fast mode (400Kbps)
- Fast mode plus (1.0Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current is 3 mA; similar to the case of standard and fast modes. The AFEx32A3W family supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I<sup>2</sup>C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. [Figure 6-19](#) depicts a not-acknowledge, when the SDA line is left high during the high period of the ninth clock cycle.

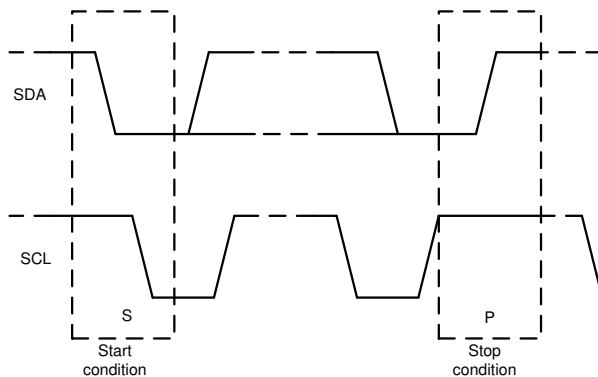


**Figure 6-19. Acknowledge and Not Acknowledge on the I<sup>2</sup>C Bus**

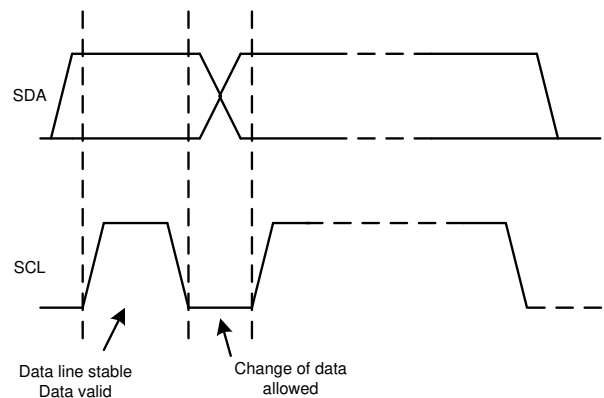
### 6.5.2.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The controller initiates data transfer by generating a start condition. [Figure 6-20](#) shows that the start condition is when a high-to-low transition occurs on the SDA line while SCL is high. All I<sup>2</sup>C-compatible devices recognize a start condition.
2. The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/W) on the SDA line. During all transmissions, the controller makes sure that data are valid. [Figure 6-21](#) shows that a valid data condition requires the SDA line to be stable during the entire high period of the clock pulse. All devices recognize the address sent by the controller and compare the address to the respective internal fixed address. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle (see also [Figure 6-19](#)). When the controller detects this acknowledge, the communication link with a target has been established.
3. The controller generates further SCL cycles to transmit (R/W bit 0) or receive (R/W bit 1) data to the target. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the controller or by the target, depending on which is the receiver. The 9-bit valid data sequences consists of eight data bits and one acknowledge-bit, and can continue as long as necessary.
4. [Figure 6-20](#) shows that to signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high. This action releases the bus and stops the communication link with the addressed target. All I<sup>2</sup>C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all target devices then wait for a start condition followed by a matching address.



**Figure 6-20. Start and Stop Conditions**



**Figure 6-21. Bit Transfer on the I<sup>2</sup>C Bus**

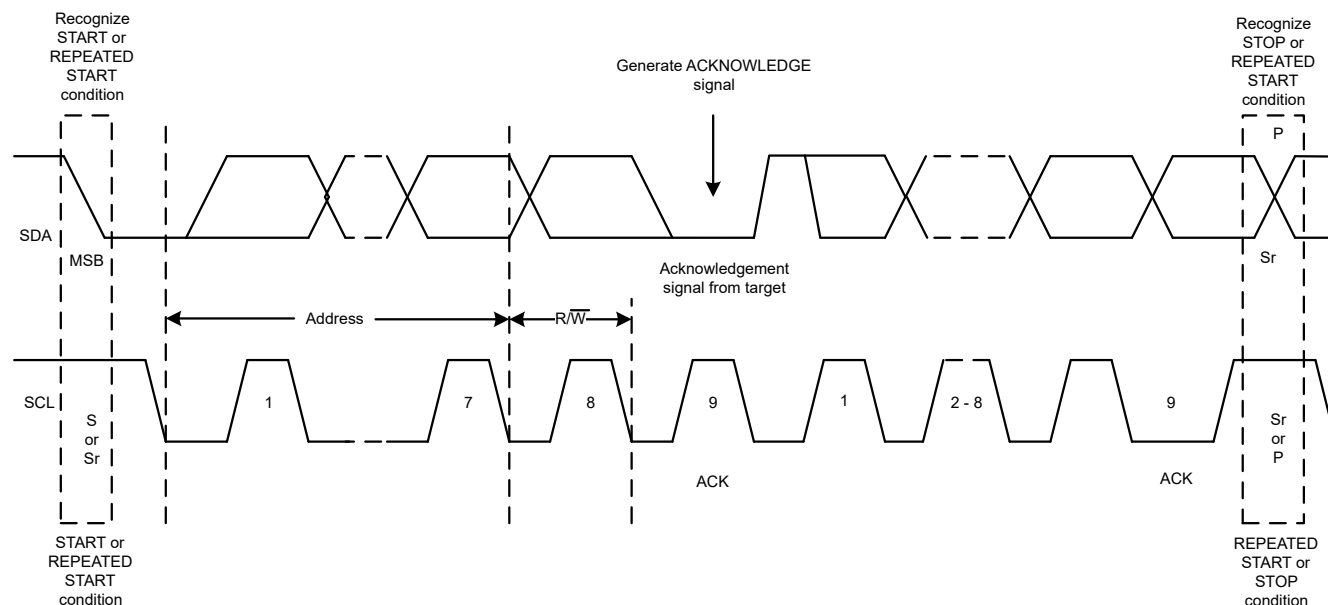
### 6.5.2.2 I<sup>2</sup>C Update Sequence

Table 6-13 shows that for a single update, the AFEx32A3W require a start condition, a valid I<sup>2</sup>C address byte, a command byte, and two data bytes.

**Table 6-13. Update Sequence**

MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte <a href="#">Section 6.5.2.2.1</a>				Command byte <a href="#">Section 6.5.2.2.2</a>				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

Figure 6-22 shows that after each byte is received, the AFEx32A3W family acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I<sup>2</sup>C address byte selects the AFEx32A3W.



**Figure 6-22. I<sup>2</sup>C Bus Protocol**

The command byte sets the operating mode of the selected AFEx32A3W device. For a data update to occur when the operating mode is selected by this byte, the AFEx32A3W device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The AFEx32A3W device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 10kSPS. Using fast mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 25kSPS. When a stop condition is received, the AFEx32A3W device releases the I<sup>2</sup>C bus and awaits a new start condition.

### 6.5.2.2.1 Address Byte

Table 6-14 depicts the address byte, the first byte received from the controller device following the start condition. The first four bits (MSBs) of the address are factory preset to 1001b. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to Table 6-15.

**Table 6-14. Address Byte**

COMMENT	MSB							LSB
	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
General address	1	0	0	1	See Table 6-15 (target address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

**Table 6-15. Address Format**

TARGET ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

The AFE432A3W supports broadcast addressing, which is used for synchronously updating or powering down multiple AFE432A3W devices. When the broadcast address is used, the AFE432A3W responds regardless of the address pin state. Broadcast is supported only in write mode.

### 6.5.2.2.2 Command Byte

The *Register Names* table in the *Register Map* section lists the command byte in the ADDRESS column.

### 6.5.2.3 I<sup>2</sup>C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a target address and the  $R/\overline{W}$  bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the target address and the  $R/\overline{W}$  bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The controller must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

The broadcast address cannot be used for reading.

**Table 6-16. Read Sequence**

S	MSB	...	R/W (0)	ACK	MSB	...	LSB	ACK	Sr	MSB	...	R/W (1)	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
	Address byte Section 6.5.2.2.1				Command byte Section 6.5.2.2.2				Sr	Address byte Section 6.5.2.2.1				MSDB				LSDB			
	From controller			Target	From controller			Target		From controller			Target	From target			Controller	From target			Controller

## 7 Register Map

**Table 7-1. Register Map: Channel-Specific Registers**

REGISTER <sup>(1)</sup> (2)	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)								
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	
NOP	NOP																
DAC-0-MARGIN-HIGH	DAC-0-MARGIN-HIGH								X								
DAC-1-MARGIN-HIGH	DAC-1-MARGIN-HIGH								X								
DAC-2-MARGIN-HIGH	DAC-2-MARGIN-HIGH								X								
DAC-0-MARGIN-LOW	DAC-0-MARGIN-LOW								X								
DAC-1-MARGIN-LOW	DAC-1-MARGIN-LOW								X								
DAC-2-MARGIN-LOW	DAC-2-MARGIN-LOW								X								
DAC-0-GAIN-CONFIG	X		REF-GAIN				X										
DAC-1-GAIN-CMP-CONFIG	X		REF-GAIN				X				CMP-1-OD-EN	CMP-1-OUT-EN	CMP-1-HIZ-IN-DIS	CMP-1-INV-EN	CMP-1-EN		
DAC-2-GAIN-CONFIG	X		IOUT-GAIN				X										
DAC-1-CMP-MODE-CONFIG	X				CMP-1-MODE				X								
DAC-0-FUNC-CONFIG	CLR-SEL-0	SYNC-CONFIG-0	BRD-CONFIG-0	FUNC-GEN-CONFIG-BLOCK-0													
DAC-1-FUNC-CONFIG	CLR-SEL-1	SYNC-CONFIG-1	BRD-CONFIG-1	FUNC-GEN-CONFIG-BLOCK-1													
DAC-2-FUNC-CONFIG	CLR-SEL-2	SYNC-CONFIG-2	BRD-CONFIG-2	FUNC-GEN-CONFIG-BLOCK-1													
DAC-0-DATA	DAC-0-DATA								X								
DAC-1-DATA	DAC-1-DATA								X								
DAC-2-DATA	DAC-2-DATA								X								
ADC-CONFIG-TRIG	RESERVED		ADC-EN	ADC-AVG				RESERVED								TRIG-ADC	
ADC-DATA	ADC-DATA								X								ADC-DRDY

**Table 7-2. Register Map: Common Registers**

REGISTER <sup>(1)</sup> (2)	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
COMMON-CONFIG	WIN-LATCH-EN	DEV-LOCK	EE-READ-ADDR	EN-INT-REF	DAC-PDN-1		RESERVED	DAC-PDN-0		RESERVED				DAC-PDN-2		RESERVED
COMMON-TRIGGER	DEV-UNLOCK			RESET				LDAC	CLR	X	FAULT-DUMP	PROTECT	READ-ONE-TRIG	NVM-PROG	NVM-RELOAD	
COMMON-DAC-TRIG	X	TRIG-MAR-LO-2	TRIG-MAR-HI-2	START-FUNC-2	X				TRIG-MAR-LO-0	TRIG-MAR-HI-0	START-FUNC-0	RESET-CMP-FLAG-1	TRIG-MAR-LO-1	TRIG-MAR-HI-1	START-FUNC-1	
GENERAL-STATUS	NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	ADC-DRDY	DAC-BUSY-1	DAC-BUSY-0	X	DAC-BUSY-2	NVM-BUSY	DEVICE-ID				VERSION-ID			
CMP-STATUS	X						PROTECT-FLAG	WIN-CMP-1	X			CMP-FLAG-1	X			
GPIO-CONFIG	GF-EN	X	GPO-EN	GPO-CONFIG				GPI-CH-SEL			GPI-CONFIG			GPI-EN		
DEVICE-MODE-CONFIG	RESERVED						PROTECT-CONFIG		RESERVED			X				
INTERFACE-CONFIG	X			TIMEOUT-EN	X			RESERVED	X				FSDO-EN	X	SDO-EN	
SRAM-CONFIG	X							SRAM-ADDR								
SRAM-DATA	SRAM-DATA															
BRDCAST-DATA	BRDCAST-DATA											X				

- (1) The highlighted gray cells indicate the register bits or fields that are stored in the NVM.  
(2) X = Don't care.

**Table 7-3. Register Names**

I <sup>2</sup> C/SPI ADDRESS	REGISTER NAME	SECTION
00h	NOP	<a href="#">Section 7.1</a>
01h	DAC-2-MARGIN-HIGH	<a href="#">Section 7.4</a>
02h	DAC-2-MARGIN-LOW	<a href="#">Section 7.7</a>
03h	DAC-2-GAIN-CONFIG	<a href="#">Section 7.10</a>
06h	DAC-2-FUNC-CONFIG	<a href="#">Section 7.14</a>
0Dh	DAC-0-MARGIN-HIGH	<a href="#">Section 7.2</a>
0Eh	DAC-0-MARGIN-LOW	<a href="#">Section 7.6</a>
0Fh	DAC-0-GAIN-CONFIG	<a href="#">Section 7.8</a>
12h	DAC-0-FUNC-CONFIG	<a href="#">Section 7.12</a>
13h	DAC-1-MARGIN-HIGH	<a href="#">Section 7.3</a>
14h	DAC-1-MARGIN-LOW	<a href="#">Section 7.6</a>
15h	DAC-1-GAIN-CMP-CONFIG	<a href="#">Section 7.9</a>
17h	DAC-1-CMP-MODE-CONFIG	<a href="#">Section 7.11</a>
18h	DAC-1-FUNC-CONFIG	<a href="#">Section 7.13</a>
19h	DAC-2-DATA	<a href="#">Section 7.17</a>
1Bh	DAC-0-DATA	<a href="#">Section 7.15</a>
1Ch	DAC-1-DATA	<a href="#">Section 7.16</a>
1Dh	ADC-CONFIG-TRIG	<a href="#">Section 7.18</a>
1Eh	ADC-DATA	<a href="#">Section 7.19</a>
1Fh	COMMON-CONFIG	<a href="#">Section 7.20</a>
20h	COMMON-TRIGGER	<a href="#">Section 7.21</a>
21h	COMMON-DAC-TRIG	<a href="#">Section 7.22</a>
22h	GENERAL-STATUS	<a href="#">Section 7.23</a>
23h	CMP-STATUS	<a href="#">Section 7.24</a>
24h	GPIO-CONFIG	<a href="#">Section 7.25</a>
25h	DEVICE-MODE-CONFIG	<a href="#">Section 7.26</a>
26h	INTERFACE-CONFIG	<a href="#">Section 7.27</a>
2Bh	SRAM-CONFIG	<a href="#">Section 7.28</a>
2Ch	SRAM-DATA	<a href="#">Section 7.29</a>
50h	BRDCAST-DATA	<a href="#">Section 7.30</a>



**Table 7-4. Access Type Codes**

Access Type	Code	Description
X	X	Don't care
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

## 7.1 NOP Register (address = 00h) [reset = 0000h]

Figure 7-1. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R-0h															

Table 7-5. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	R	0000h	No operation

## 7.2 DAC-0-MARGIN-HIGH Register (address = 0Dh) [reset = 0000h]

Figure 7-2. DAC-0-MARGIN-HIGH Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-0-MARGIN-HIGH[9:0] DAC-0-MARGIN-HIGH[7:0]												X			
R/W-000h												X-0h			

Table 7-6. DAC-0-MARGIN-HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-0-MARGIN-HIGH[9:0] DAC-0-MARGIN-HIGH[7:0]	R/W	000h	Margin-high code for DAC channel 0 output. Data are in straight-binary format. MSB left aligned. Use the following bit alignment: AFE532A3W: {DAC-0-MARGIN-HIGH[9:0], X, X} AFE432A3W: {DAC-0-MARGIN-HIGH[7:0], X, X, X, X} X = Don't care bits.
3-0	X	X	0h	Don't care

## 7.3 DAC-1-MARGIN-HIGH Register (address = 13h) [reset = 0000h]

Figure 7-3. DAC-1-MARGIN-HIGH Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-1-MARGIN-HIGH[9:0] DAC-1-MARGIN-HIGH[7:0]												X			
R/W-000h												X-0h			

Table 7-7. DAC-1-MARGIN-HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-1-MARGIN-HIGH[9:0] DAC-1-MARGIN-HIGH[7:0]	R/W	000h	Margin-high code for DAC channel 1 output. Data are in straight-binary format. MSB left aligned. Use the following bit alignment: AFE532A3W: {DAC-1-MARGIN-HIGH[9:0], X, X} AFE432A3W: {DAC-1-MARGIN-HIGH[7:0], X, X, X, X} X = Don't care bits.
3-0	X	X	0h	Don't care

## 7.4 DAC-2-MARGIN-HIGH Register (address = 01h) [reset = 0000h]

**Figure 7-4. DAC-2-MARGIN-HIGH Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-2-MARGIN-HIGH[9:0] DAC-2-MARGIN-HIGH[7:0]												X			
R/W-000h												X-0h			

**Table 7-8. DAC-2-MARGIN-HIGH Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	DAC-2-MARGIN-HIGH[9:0] DAC-2-MARGIN-HIGH[7:0]	R/W	000h	Margin-high code for DAC channel 2 output. Data are in straight-binary format. MSB left aligned. Use the following bit alignment: AFE532A3W: {DAC-2-MARGIN-HIGH[9:0], X, X} AFE432A3W: {DAC-2-MARGIN-HIGH[7:0], X, X, X, X} X = Don't care bits.
3-0	X	X	0h	Don't care

## 7.5 DAC-0-MARGIN-LOW Register (address = 0Eh) [reset = 0000h]

**Figure 7-5. DAC-0-MARGIN-LOW Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-0-MARGIN-LOW[9:0] DAC-0-MARGIN-LOW[7:0]												X			
R/W-000h												X-0h			

**Table 7-9. DAC-0-MARGIN-LOW Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	DAC-0-MARGIN-LOW[9:0] DAC-0-MARGIN-LOW[7:0]	R/W	000h	Margin-low code for DAC channel output. Data are in straight-binary format. MSB left aligned. Use the following bit alignment: {DAC-0-MARGIN-LOW[9:0], X, X} {DAC-0-MARGIN-LOW[7:0], X, X, X, X} X = Don't care bits.
3-0	X	X	0	Don't care

## 7.6 DAC-1-MARGIN-LOW Register (address = 14h) [reset = 0000h]

**Figure 7-6. DAC-1-MARGIN-LOW Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-1-MARGIN-LOW[9:0] DAC-1-MARGIN-LOW[7:0]												X			
R/W-000h												X-0h			

**Table 7-10. DAC-1-MARGIN-LOW Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	DAC-0-MARGIN-LOW[9:0] DAC-0-MARGIN-LOW[7:0]	R/W	000h	Margin-low code for DAC channel 1 output. Data are in straight-binary format. MSB left aligned. Use the following bit alignment: {DAC-1-MARGIN-LOW[9:0], X, X} {DAC-1-MARGIN-LOW[7:0], X, X, X, X} X = Don't care bits.
3-0	X	X	0	Don't care

## 7.7 DAC-2-MARGIN-LOW Register (address = 02h) [reset = 0000h]

Figure 7-7. DAC-2-MARGIN-LOW Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-2-MARGIN-LOW[9:0] DAC-2-MARGIN-LOW[7:0]												X			
R/W-000h												X-0h			

Table 7-11. DAC-2-MARGIN-LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-2-MARGIN-LOW[9:0] DAC-2-MARGIN-LOW[7:0]	R/W	000h	Margin-low code for DAC channel 2 output. Data are in straight-binary format. MSB left aligned. Use the following bit alignment: {DAC-2-MARGIN-LOW[9:0], X, X} {DAC-2-MARGIN-LOW[7:0], X, X, X, X} X = Don't care bits.
3-0	X	X	0	Don't care

## 7.8 DAC-0-GAIN-CONFIG Register (address = 0Fh) [reset = 0000h]

Figure 7-8. DAC-0-GAIN-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X		REF-GAIN-0				X									
X-0h		R/W-0h				X-000h									

Table 7-12. DAC-0-GAIN-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12-10	REF-GAIN-0	R/W	0h	001: Gain = 1 ×, VDD as reference. 010: Gain = 1.5 ×, internal reference. 011: Gain = 2 ×, internal reference. 100: Gain = 3 ×, internal reference. 101: Gain = 4 ×, internal reference. Others: Invalid.
9-0	X	X	000h	Don't care

## 7.9 DAC-1-GAIN-CMP-CONFIG Register (address = 15h) [reset = 0000h]

**Figure 7-9. DAC-1-GAIN-CMP-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X		REF-GAIN-1					X			CMP-1-OD-EN	CMP-1-OUT-EN	CMP-1-HIZ-IN-DIS	CMP-1-INV-EN	CMP-1-EN	
X-0h		R/W-0h					X-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

**Table 7-13. DAC-1-GAIN-CMP-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12-10	REF-GAIN-1	R/W	0h	001: Gain = 1 ×, VDD as reference. 010: Gain = 1.5 ×, internal reference. 011: Gain = 2 ×, internal reference. 100: Gain = 3 ×, internal reference. 101: Gain = 4 ×, internal reference. Others: Invalid.
9-5	X	X	0h	Don't care
4	CMP-1-OD-EN	R/W	0h	0: Set VOUT1/AIN1 pin as push-pull. 1: Set VOUT1/AIN1 pin as open-drain in comparator mode. (CMP-1-EN = 1 and CMP-1-OUT-EN = 1).
3	CMP-1-OUT-EN	R/W	0h	0: Generate comparator output but consume internally. 1: Bring comparator output to the respective VOUT1/AIN1 pin.
2	CMP-1-HIZ-IN-DIS	R/W	0h	0: FB1 input has high-impedance. 1: FB1 input has finite impedance as per the <i>Electrical Characteristics: Voltage Output</i> section. Set this bit to 0 in ADC mode.
1	CMP-1-INV-EN	R/W	0h	0: Don't invert the comparator output. 1: Invert the comparator output.
0	CMP-1-EN	R/W	0h	0: Disable comparator mode. 1: Enable comparator mode. DAC channel 1 must be enabled.

## 7.10 DAC-2-GAIN-CONFIG Register (address = 03h) [reset = 0000h]

**Figure 7-10. DAC-2-GAIN-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X		IOUT-GAIN					X								
X-0h		R/W-0h					X-000h								

**Table 7-14. DAC-2-GAIN-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12-10	IOUT-GAIN	R/W	0h	000: GAIN = 2/3. 001: GAIN = 1/2. Others: Invalid.
9-0	X	X	000h	Don't care

## 7.11 DAC-1-CMP-MODE-CONFIG Register (address = 17h) [reset = 0000h]

**Figure 7-11. DAC-1-CMP-MODE-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				CMP-1-MODE			X								
X-0h				R/W-0h			X-000h								

**Table 7-15. DAC-1-CMP-MODE-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	X	X	0h	Don't care
11-10	CMP-1-MODE	R/W	0h	00: No hysteresis or window function. 01: Hysteresis provided using DAC-1-MARGIN-HIGH and DAC-1-MARGIN-LOW registers. 10: Window comparator mode with DAC-1-MARGIN-HIGH and DAC-1-MARGIN-LOW registers setting window bounds. 11: Invalid.
9-0	X	X	000h	Don't care

## 7.12 DAC-0-FUNC-CONFIG Register (address = 12h) [reset = 0000h]

**Figure 7-12. DAC-0-FUNC-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR-SEL-0	SYNC-CONFIG-0	BRD-CONFIG-0	FUNC-GEN-CONFIG-BLOCK-0												
R/W-0h	R/W-0h	R/W-0h	R/W-000h												

**Table 7-16. DAC-0-FUNC-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	CLR-SEL-0	R/W	0h	0: Clear DAC channel 0 to zero scale. 1: Clear DAC channel 0 to midscale.
14	SYNC-CONFIG-0	R/W	0h	0: DAC channel 0 output updates immediately after a write command. 1: DAC channel 0 output updates with $\overline{\text{LDAC}}$ pin falling-edge or when the LDAC bit in the COMMON-TRIGGER register is set to 1.
13	BRD-CONFIG-0	R/W	0h	0: Don't update DAC channel 0 with broadcast command. 1: Update DAC channel 0 with broadcast command.

**Table 7-17. Linear-Slew Mode: FUNC-GEN-CONFIG-BLOCK-0 Field Descriptions**

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-0	R/W	0h	00: 0° 01: 120° 10: 240° 11: 90°
10-8	FUNC-CONFIG-0	R/W	0h	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-0	R/W	0h	0: Enable linear slew
6-4	CODE-STEP-0	R/W	0h	CODE-STEP for linear slew mode: 000: 1-LSB 001: 2-LSB 010: 3-LSB 011: 4-LSB 100: 6-LSB 101: 8-LSB 110: 16-LSB 111: 32-LSB
3-0	SLEW-RATE-0	R/W	0h	SLEW-RATE for linear slew mode: 0000: No slew for margin-high and margin-low. Invalid for waveform generation. 0001: 4 $\mu\text{s}/\text{step}$ 0010: 8 $\mu\text{s}/\text{step}$ 0011: 12 $\mu\text{s}/\text{step}$ 0100: 18 $\mu\text{s}/\text{step}$ 0101: 27.04 $\mu\text{s}/\text{step}$ 0110: 40.48 $\mu\text{s}/\text{step}$ 0111: 60.72 $\mu\text{s}/\text{step}$ 1000: 91.12 $\mu\text{s}/\text{step}$ 1001: 136.72 $\mu\text{s}/\text{step}$ 1010: 239.2 $\mu\text{s}/\text{step}$ 1011: 418.64 $\mu\text{s}/\text{step}$ 1100: 732.56 $\mu\text{s}/\text{step}$ 1101: 1282 $\mu\text{s}/\text{step}$ 1110: 2563.96 $\mu\text{s}/\text{step}$ 1111: 5127.92 $\mu\text{s}/\text{step}$

**Table 7-18. Logarithmic-Slew Mode: FUNC-GEN-CONFIG-BLOCK-0 Field Descriptions**

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-0	R/W	0h	00: 0° 01: 120° 10: 240° 11: 90°
10-8	FUNC-CONFIG-0	R/W	0h	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-0	R/W	0h	1: Enable logarithmic slew. In logarithmic slew mode, the DAC output moves from the DAC-0-MARGIN-LOW code to the DAC-0-MARGIN-HIGH code, or vice versa, in 3.125% steps. When slewing in the positive direction, the next step is $(1 + 0.03125)$ times the current step. When slewing in the negative direction, the next step is $(1 - 0.03125)$ times the current step. When DAC-0-MARGIN-LOW is 0, the slew starts from code 1. The time interval for each step is defined by RISE-SLEW-0 and FALL-SLEW-0.
6-4	RISE-SLEW-0	R/W	0h	SLEW-RATE for logarithmic slew mode (DAC-0-MARGIN-LOW to DAC-0-MARGIN-HIGH): 000: 4 $\mu$ s/step 001: 12 $\mu$ s/step 010: 27.04 $\mu$ s/step 011: 60.72 $\mu$ s/step 100: 136.72 $\mu$ s/step 101: 418.64 $\mu$ s/step 110: 1282 $\mu$ s/step 111: 5127.92 $\mu$ s/step
3-1	FALL-SLEW-0	R/W	0h	SLEW-RATE for logarithmic slew mode (DAC-0-MARGIN-HIGH to DAC-0-MARGIN-LOW): 000: 4 $\mu$ s/step 001: 12 $\mu$ s/step 010: 27.04 $\mu$ s/step 011: 60.72 $\mu$ s/step 100: 136.72 $\mu$ s/step 101: 418.64 $\mu$ s/step 110: 1282 $\mu$ s/step 111: 5127.92 $\mu$ s/step
0	X	X	0h	Don't care



### 7.13 DAC-1-FUNC-CONFIG Register (address = 18h) [reset = 0000h]

**Figure 7-13. DAC-1-FUNC-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR-SEL-1	SYNC-CONFIG-1	BRD-CONFIG-1	FUNC-GEN-CONFIG-BLOCK-1												
R/W-0h	R/W-0h	R/W-0h	R/W-000h												

**Table 7-19. DAC-1-FUNC-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	CLR-SEL-1	R/W	0h	0: Clear DAC channel 1 to zero scale. 1: Clear DAC channel 1 to midscale.
14	SYNC-CONFIG-1	R/W	0h	0: DAC channel 1 output updates immediately after a write command. 1: DAC channel 1 output updates with $\overline{\text{LDAC}}$ pin falling-edge or when the LDAC bit in the COMMON-TRIGGER register is set to 1.
13	BRD-CONFIG-1	R/W	0h	0: Don't update DAC channel 1 with broadcast command. 1: Update DAC channel 1 with broadcast command.

**Table 7-20. Linear-Slew Mode: FUNC-GEN-CONFIG-BLOCK-1 Field Descriptions**

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-1	R/W	0h	00: 0° 01: 120° 10: 240° 11: 90°
10-8	FUNC-CONFIG-1	R/W	0h	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-1	R/W	0h	0: Enable linear slew
6-4	CODE-STEP-1	R/W	0h	CODE-STEP for linear slew mode: 000: 1-LSB 001: 2-LSB 010: 3-LSB 011: 4-LSB 100: 6-LSB 101: 8-LSB 110: 16-LSB 111: 32-LSB
3-0	SLEW-RATE-1	R/W	0h	SLEW-RATE for linear slew mode: 0000: No slew for margin-high and margin-low. Invalid for waveform generation. 0001: 4 $\mu\text{s}/\text{step}$ 0010: 8 $\mu\text{s}/\text{step}$ 0011: 12 $\mu\text{s}/\text{step}$ 0100: 18 $\mu\text{s}/\text{step}$ 0101: 27.04 $\mu\text{s}/\text{step}$ 0110: 40.48 $\mu\text{s}/\text{step}$ 0111: 60.72 $\mu\text{s}/\text{step}$ 1000: 91.12 $\mu\text{s}/\text{step}$ 1001: 136.72 $\mu\text{s}/\text{step}$ 1010: 239.2 $\mu\text{s}/\text{step}$ 1011: 418.64 $\mu\text{s}/\text{step}$ 1100: 732.56 $\mu\text{s}/\text{step}$ 1101: 1282 $\mu\text{s}/\text{step}$ 1110: 2563.96 $\mu\text{s}/\text{step}$ 1111: 5127.92 $\mu\text{s}/\text{step}$

**Table 7-21. Logarithmic-Slew Mode: FUNC-GEN-CONFIG-BLOCK-1 Field Descriptions**

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-1	R/W	0h	00: 0° 01: 120° 10: 240° 11: 90°
10-8	FUNC-CONFIG-1	R/W	0h	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-1	R/W	0h	1: Enable logarithmic slew. In logarithmic slew mode, the DAC output moves from the DAC-1-MARGIN-LOW code to the DAC-1-MARGIN-HIGH code, or vice versa, in 3.125% steps. When slewing in the positive direction, the next step is $(1 + 0.03125)$ times the current step. When slewing in the negative direction, the next step is $(1 - 0.03125)$ times the current step. When DAC-1-MARGIN-LOW is 0, the slew starts from code 1. The time interval for each step is defined by RISE-SLEW-0 and FALL-SLEW-0.
6-4	RISE-SLEW-1	R/W	0h	SLEW-RATE for logarithmic slew mode (DAC-1-MARGIN-LOW to DAC-1-MARGIN-HIGH): 000: 4 $\mu$ s/step 001: 12 $\mu$ s/step 010: 27.04 $\mu$ s/step 011: 60.72 $\mu$ s/step 100: 136.72 $\mu$ s/step 101: 418.64 $\mu$ s/step 110: 1282 $\mu$ s/step 111: 5127.92 $\mu$ s/step
3-1	FALL-SLEW-1	R/W	0h	SLEW-RATE for logarithmic slew mode (DAC-1-MARGIN-HIGH to DAC-1-MARGIN-LOW): 000: 4 $\mu$ s/step 001: 12 $\mu$ s/step 010: 27.04 $\mu$ s/step 011: 60.72 $\mu$ s/step 100: 136.72 $\mu$ s/step 101: 418.64 $\mu$ s/step 110: 1282 $\mu$ s/step 111: 5127.92 $\mu$ s/step
0	X	X	0h	Don't care

## 7.14 DAC-2-FUNC-CONFIG Register (address = 06h) [reset = 0000h]

**Figure 7-14. DAC-2-FUNC-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR-SEL-2	SYNC-CONFIG-2	BRD-CONFIG-2	FUNC-GEN-CONFIG-BLOCK-2												
R/W-0h	R/W-0h	R/W-0h	R/W-000h												

**Table 7-22. DAC-2-FUNC-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	CLR-SEL-2	R/W	0h	0: Clear DAC channel 2 to zero scale. 1: Clear DAC channel 2 to midscale.
14	SYNC-CONFIG-2	R/W	0h	0: DAC channel 2 output updates immediately after a write command. 1: DAC channel 2 output updates with $\overline{\text{LDAC}}$ pin falling-edge or when the LDAC bit in the COMMON-TRIGGER register is set to 1.
13	BRD-CONFIG-2	R/W	0h	0: Don't update DAC channel 2 with broadcast command. 1: Update DAC channel 2 with broadcast command.

**Table 7-23. Linear-Slew Mode: FUNC-GEN-CONFIG-BLOCK-2 Field Descriptions**

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-2	R/W	0h	00: 0° 01: 120° 10: 240° 11: 90°
10-8	FUNC-CONFIG-2	R/W	0h	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-2	R/W	0h	0: Enable linear slew
6-4	CODE-STEP-2	R/W	0h	CODE-STEP for linear slew mode: 000: 1-LSB 001: 2-LSB 010: 3-LSB 011: 4-LSB 100: 6-LSB 101: 8-LSB 110: 16-LSB 111: 32-LSB
3-0	SLEW-RATE-2	R/W	0h	SLEW-RATE for linear slew mode: 0000: No slew for margin-high and margin-low. Invalid for waveform generation. 0001: 4 $\mu\text{s}/\text{step}$ 0010: 8 $\mu\text{s}/\text{step}$ 0011: 12 $\mu\text{s}/\text{step}$ 0100: 18 $\mu\text{s}/\text{step}$ 0101: 27.04 $\mu\text{s}/\text{step}$ 0110: 40.48 $\mu\text{s}/\text{step}$ 0111: 60.72 $\mu\text{s}/\text{step}$ 1000: 91.12 $\mu\text{s}/\text{step}$ 1001: 136.72 $\mu\text{s}/\text{step}$ 1010: 239.2 $\mu\text{s}/\text{step}$ 1011: 418.64 $\mu\text{s}/\text{step}$ 1100: 732.56 $\mu\text{s}/\text{step}$ 1101: 1282 $\mu\text{s}/\text{step}$ 1110: 2563.96 $\mu\text{s}/\text{step}$ 1111: 5127.92 $\mu\text{s}/\text{step}$

**Table 7-24. Logarithmic-Slew Mode: FUNC-GEN-CONFIG-BLOCK-2 Field Descriptions**

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-2	R/W	0h	00: 0° 01: 120° 10: 240° 11: 90°
10-8	FUNC-CONFIG-2	R/W	0h	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-2	R/W	0h	1: Enable logarithmic slew. In logarithmic slew mode, the DAC output moves from the DAC-2-MARGIN-LOW code to the DAC-2-MARGIN-HIGH code, or vice versa, in 3.125% steps. When slewing in the positive direction, the next step is $(1 + 0.03125)$ times the current step. When slewing in the negative direction, the next step is $(1 - 0.03125)$ times the current step. When DAC-2-MARGIN-LOW is 0, the slew starts from code 1. The time interval for each step is defined by RISE-SLEW-0 and FALL-SLEW-0.
6-4	RISE-SLEW-2	R/W	0h	SLEW-RATE for logarithmic slew mode (DAC-2-MARGIN-LOW to DAC-2-MARGIN-HIGH): 000: 4 $\mu$ s/step 001: 12 $\mu$ s/step 010: 27.04 $\mu$ s/step 011: 60.72 $\mu$ s/step 100: 136.72 $\mu$ s/step 101: 418.64 $\mu$ s/step 110: 1282 $\mu$ s/step 111: 5127.92 $\mu$ s/step
3-1	FALL-SLEW-2	R/W	0h	SLEW-RATE for logarithmic slew mode (DAC-2-MARGIN-HIGH to DAC-2-MARGIN-LOW): 000: 4 $\mu$ s/step 001: 12 $\mu$ s/step 010: 27.04 $\mu$ s/step 011: 60.72 $\mu$ s/step 100: 136.72 $\mu$ s/step 101: 418.64 $\mu$ s/step 110: 1282 $\mu$ s/step 111: 5127.92 $\mu$ s/step
0	X	X	0h	Don't care

## 7.15 DAC-0-DATA Register (address = 1Bh) [reset = 0000h]

**Figure 7-15. DAC-0-DATA Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-0-DATA[9:0] DAC-0-DATA[7:0]												X			
R/W-000h												X-0h			

**Table 7-25. DAC-0-DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	DAC-0-DATA[9:0] DAC-0-DATA[7:0]	R/W	000h	Data for DAC output. Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: AFE532A3W: {DAC-0-DATA[9:0], X, X} AFE432A3W: {DAC-0-DATA[7:0], X, X, X, X} X = Don't care bits.
3-0	X	X	0h	Don't care

## 7.16 DAC-1-DATA Register (address = 1Ch) [reset = 0000h]

**Figure 7-16. DAC-1-DATA Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-1-DATA[9:0] DAC-1-DATA[7:0]												X			
R/W-000h												X-0h			

**Table 7-26. DAC-1-DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	DAC-1-DATA[9:0] DAC-1-DATA[7:0]	R/W	000h	Data for DAC output. Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: AFE532A3W: {DAC-1-DATA[9:0], X, X} AFE432A3W: {DAC-1-DATA[7:0], X, X, X, X} X = Don't care bits.
3-0	X	X	0h	Don't care

## 7.17 DAC-2-DATA Register (address = 19h) [reset = 0000h]

**Figure 7-17. DAC-2-DATA Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-2-DATA[9:0] DAC-2-DATA[7:0]												X			
R/W-000h												X-0h			

**Table 7-27. DAC-2-DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	DAC-2-DATA[9:0] DAC-2-DATA[7:0]	R/W	000h	Data for DAC output. Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: AFE532A3W: {DAC-2-DATA[9:0], X, X} AFE432A3W: {DAC-2-DATA[7:0], X, X, X, X} X = Don't care bits.
3-0	X	X	0h	Don't care

## 7.18 ADC-CONFIG-TRIG Register (address = 1Dh) [reset = 0000h]

Figure 7-18. ADC-CONFIG-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		ADC-EN	ADC-AVG			RESERVED									TRIG-ADC
R/W-0h		R/W-0h	R/W-0h			R/W-000h									W-0h

Table 7-28. ADC-CONFIG-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Always write 0h.
13	ADC-EN	R/W	0h	0: ADC is disabled. 1: ADC is enabled on channel 1. Comparator mode must be enabled on channel 1 before setting this bit. Connect FB1 to VDD using a pullup resistor.
12-11	ADC-AVG	R/W	0h	00: 4 samples are averaged. 01: 8 samples are averaged. 10: 16 samples are averaged. 11: 32 samples are averaged.
10-1	RESERVED	R/W	000h	Always write 0b01 1110 0000 (1E0h).
0	TRIG-ADC	W	0h	Write 1 to start ADC conversion. This bit is auto-resetting. Check the ADC-DRDY bit in the GENERAL-STATUS or the ADC-DATA register for ADC data validity.

## 7.19 ADC-DATA Register (address = 1Eh) [reset = 0001h]

Figure 7-19. ADC-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC-DATA												X	ADC-DRDY		
R/W-000h												X-0h	R-1h		

Table 7-29. ADC-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	ADC-DATA[9:0]	R/W	000h	ADC data. Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment for readback: {ADC-DATA[9:0], X, X} X = Don't care bits.
3-1	X	X	0h	Don't care
0	ADC-DRDY	R	1h	0: Default state after ADC is triggered. ADC data is invalid. 1: Default state when ADC is not triggered. The value 1 indicates ADC data is valid after the ADC is triggered.

## 7.20 COMMON-CONFIG Register (address = 1Fh) [reset = 0FFFh]

**Figure 7-20. COMMON-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIN-LATCH-EN	DEV-LOCK	EE-READ-ADDR	EN-INT-REF	DAC-PDN-1	RESERVED	DAC-PDN-0	RESERVED			DAC-PDN-2	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-3h	R/W-1h	R/W-3h	R/W-Fh			R/W-3h	R/W-1h				

**Table 7-30. COMMON-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	WIN-LATCH-EN	R/W	0h	0: Non-latching window-comparator output. 1: Latching window-comparator output.
14	DEV-LOCK	R/W	0h	0: Device not locked 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	EE-READ-ADDR	R/W	0h	0: Fault-dump read enable at address 0x00. 1: Fault-dump read enable at address 0x01.
12	EN-INT-REF	R/W	0h	0: Disable internal reference. 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11-10	DAC-PDN-1	R/W	3h	00: Power-up DAC channel 1. 01: Power-down DAC channel 1 with 10 kΩ to AGND. 10: Power-down DAC channel 1 with 100 kΩ to AGND. 11: Power-down DAC channel 1 with Hi-Z to AGND.
9	RESERVED	R/W	1h	Always write 1h.
8-7	DAC-PDN-0	R/W	3h	00: Power-up DAC channel 0. 01: Power-down DAC channel 0 with 10 kΩ to AGND. 10: Power-down DAC channel 0 with 100 kΩ to AGND. 11: Power-down DAC channel 0 with Hi-Z to AGND.
6-3	RESERVED	R/W	Fh	Always write Fh.
2-1	DAC-PDN-2	R/W	3h	00: Power-up DAC channel 2. Others: Power-down DAC channel 2 with 1.2 kΩ to AGND.
0	RESERVED	R/W	1h	Always write 1h.

## 7.21 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

**Figure 7-21. COMMON-TRIGGER Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
DEV-UNLOCK				RESET				LDAC	CLR	X	FAULT-DUMP	PROTECT	READ-ONE-TRIG	NVM-PROG	NVM-RELOAD	
R/W-0h				R/W-0h				R/W-0h	R/W-0h	X-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

**Table 7-31. COMMON-TRIGGER Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	DEV-UNLOCK	R/W	0h	0101: Device unlocking password Others: Don't care
11-8	RESET	W	0h	1010: POR reset triggered. This bit self-resets. Others: Don't care
7	LDAC	R/W	0h	0: LDAC operation not triggered 1: LDAC operation triggered if the respective SYNC-CONFIG-x bit in the DAC-x-FUNC-CONFIG register is 1. This bit self-resets.
6	CLR	R/W	0h	0: DAC registers and outputs unaffected 1: DAC registers and outputs set to zero-code or mid-code based on the respective CLR-SEL-x bit in the DAC-x-FUNC-CONFIG register. This bit self-resets.
5	X	X	0h	Don't care
4	FAULT-DUMP	R/W	0h	0: Fault-dump is not triggered 1: Triggers fault-dump sequence. This bit self-resets.
3	PROTECT	R/W	0h	0: PROTECT function not triggered 1: Trigger PROTECT function. This bit self-resets.
2	READ-ONE-TRIG	R/W	0h	0: Fault-dump read not triggered 1: Read one row of NVM for fault-dump. This bit self-resets.
1	NVM-PROG	R/W	0h	0: NVM write not triggered 1: NVM write triggered. This bit self-resets.
0	NVM-RELOAD	R/W	0h	0: NVM reload not triggered 1: Reload data from NVM to register map. This bit self-resets.



## 7.22 COMMON-DAC-TRIG Register (address = 21h) [reset = 0000h]

**Figure 7-22. COMMON-DAC-TRIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	TRIG-MAR-LO-2	TRIG-MAR-HI-2	START-FUNC-2	X				TRIG-MAR-LO-0	TRIG-MAR-HI-0	START-FUNC-0	RESET-CMP-FLAG-1	TRIG-MAR-LO-1	TRIG-MAR-HI-1	START-FUNC-1	
X-0h	W-0h	W-0h	R/W-0h	X-00h				W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h	

**Table 7-32. COMMON-DAC-TRIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
14, 6, 2	TRIG-MAR-LO-x	W	0h	0: Don't care 1: Trigger margin-low command. This bit self-resets.
13, 5, 1	TRIG-MAR-HI-x	W	0h	0: Don't care 1: Trigger margin-high command. This bit self-resets.
12, 4, 0	START-FUNC-x	R/W	0h	0: Stop function generation 1: Start function generation as per FUNC-GEN-CONFIG-x in the DAC-x-FUNC-CONFIG register.
15, 11-7	X	X	00h	Don't care
3	RESET-CMP-FLAG-1	W	0h	0: Latching-comparator output unaffected 1: Reset latching-comparator and window-comparator output. This bit self-resets.

## 7.23 GENERAL-STATUS Register (address = 22h) [reset = 20h, DEVICE-ID, VERSION-ID]

**Figure 7-23. GENERAL-STATUS Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	ADC--DRDY	DAC-1-BUSY	DAC-0-BUSY	X	DAC-2-BUSY	NVM-BUSY	DEVICE-ID						VERSION-ID	
R-0h	R-0h	R-1h	R-0h	R-0h	X-0h	R-0h	R-0h	R-[DEVICE-ID]						R-0h	

**Table 7-33. GENERAL-STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0h	0: No CRC error in OTP. 1: Indicates a failure in OTP loading. A software reset or power-cycle can bring the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0h	0: No CRC error in NVM loading 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get original state. A software reset brings the device out of this temporary error condition.
13	ADC-DRDY	R	1h	0: Default state after ADC is triggered. ADC data is invalid. 1: Default state when ADC is not triggered. The value 1 indicates ADC data is valid after the ADC is triggered.
12	DAC-1-BUSY	R	0h	0: DAC channel 1 can accept commands. 1: DAC channel 1 does not accept commands.
11	DAC-0-BUSY	R	0h	0: DAC channel 0 can accept commands. 1: DAC channel 0 does not accept commands.
10	X	X	0h	Don't care
9	DAC-2-BUSY	R	0h	0: DAC channel 2 can accept commands. 1: DAC channel 2 does not accept commands.
8	NVM-BUSY	R	0h	0: NVM is available for read and write. 1: NVM is not available for read or write.
7-2	DEVICE-ID	R	AFE532A3W: 01h AFE432A3W: 02h	Device identifier.
1-0	VERSION-ID	R	00h	Version identifier.

## 7.24 CMP-STATUS Register (address = 23h) [reset = 000Ch]

**Figure 7-24. CMP-STATUS Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
X				PROTECT-FLAG				WIN-CMP-1	X				CMP-FLAG-1	X		
X-0h						R-0h		R-0h	X-0h			R-1h		X-4h		

**Table 7-34. CMP-STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-9	X	X	0h	Don't care
8	PROTECT-FLAG	R	0h	0: PROTECT operation not triggered. 1: PROTECT function is completed or in progress. This bit resets to 0 when read.
7	WIN-CMP-1	R	0h	Window comparator output from channel 1. The output is latched or unlatched based on the WINDOW-LATCH-EN setting in the COMMON-CONFIG register.
6-4	X	X	0h	Don't care
3	CMP-FLAG-1	R	1h	Synchronized comparator output from channel 1.
2-0	X	X	4h	Don't care

## 7.25 GPIO-CONFIG Register (address = 24h) [reset = 0000h]

**Figure 7-25. GPIO-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GF-EN	X	GPO-EN	GPO-CONFIG				GPI-CH-SEL				GPI-CONFIG				GPI-EN
R/W-0h	X-0h	R/W-0h	R/W-0h				R/W-0h				R/W-0h				R/W-0h

**Table 7-35. GPIO-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	GF-EN	R/W	0h	0: Glitch filter disabled for GP input. This setting provides faster response. 1: Glitch filter enabled for GPI. This setting introduces additional propagation delay but provides robustness.
14	X	X	0h	Don't care.
13	GPO-EN	R/W	0h	0: Disable output mode for GPIO/SDO pin. 1: Enable output mode for GPIO/SDO pin.
12-9	GPO-CONFIG	R/W	0h	STATUS function setting. The GPIO pin is mapped to the following register bits as output: 0000: ADC-DRDY 0001: NVM-BUSY 0100: DAC-2-BUSY 0110: DAC-0-BUSY 0111: DAC-1-BUSY 1011: WIN-CMP-1 Others: NA
8-5	GPI-CH-SEL	R/W	0h	Two bits correspond to two DAC channels. 0b is <i>disabled</i> and 1b is <i>enabled</i> . GPI-CH-SEL[0]: Channel 2 GPI-CH-SEL[1]: Don't care GPI-CH-SEL[2]: Channel 0 GPI-CH-SEL[3]: Channel 1  Example: when GPI-CH-SEL is 1001, both channel 2 and channel 1 are enabled and channel 0 is disabled.
4-1	GPI-CONFIG	R/W	0h	GPIO/SDO pin input configuration. Global settings act on the entire device. Channel-specific settings depend on the channel selection by the GPI-CH-SEL bits:  0010: $\overline{\text{FAULT-DUMP}}$ (global). GPIO falling edge triggers fault dump, GPIO = 1 has no effect.  0100: Channel power up-down (channel-specific). The output load is as per the OUT-PDN-x setting. GPIO falling edge triggers power down, GPIO rising edge triggers power up.  0101: $\overline{\text{PROTECT}}$ input (global). GPIO falling edge asserts $\overline{\text{PROTECT}}$ function, GPIO = 1 has no effect.  0111: $\overline{\text{CLR}}$ input (global). GPIO = 0 asserts $\overline{\text{CLR}}$ function, GPIO = 1 has no effect.  1000: $\overline{\text{LDAC}}$ input (channel-specific). GPIO falling edge asserts $\overline{\text{LDAC}}$ function, GPIO = 1 has no effect. Both the SYNC-CONFIG-x and the GPI-CH-SEL must be configured for every channel.  1001: Start and stop function generation (channel-specific). GPIO falling edge stops function generation. GPIO rising edge starts function generation.  1010: Trigger margin high-low (channel-specific). GPIO falling edge triggers margin low. GPIO rising edge triggers margin high.  1011: $\overline{\text{RESET}}$ input (global). The falling edge of the GPIO pin asserts the $\overline{\text{RESET}}$ function. The $\overline{\text{RESET}}$ input must be a pulse. The GPIO rising edge brings the device out of reset. The $\overline{\text{RESET}}$ configuration must be programmed into the NVM. Otherwise, the setting is cleared after the device reset.  1100: NVM write protection (global). GPIO falling edge allows NVM programming. GPIO rising edge blocks NVM programming.  1101: Register-map lock (global). GPIO falling edge allows update to the register map. GPIO rising edge blocks any register map update except a write to the DEV-UNLOCK field through I <sup>2</sup> C or SPI and to the RESET field through I <sup>2</sup> C.  Others: Invalid
0	GPI-EN	R/W	0h	0: Disable input mode for GPIO/SDO pin. 1: Enable input mode for GPIO/SDO pin.

## 7.26 DEVICE-MODE-CONFIG Register (address = 25h) [reset = 0000h]

**Figure 7-26. DEVICE-MODE-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RESERVED						PROTECT- CONFIG	RESERVED				X					
R/W-00h						R/W-0h		R/W-0h				X-00h				

**Table 7-36. DEVICE-MODE-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	00h	Always write 00h.
9-8	PROTECT-CONFIG	R/W	0h	00: Switch to Hi-Z power-down (no slew) 01: Switch to DAC code stored in NVM (no slew) and then switch to Hi-Z power-down 10: Slew to margin-low code and then switch to Hi-Z power-down 11: Slew to margin-high code and then switch to Hi-Z power-down
7-5	RESERVED	R/W	0h	Always write 0h.
4-0	X	X	00h	Don't care

## 7.27 INTERFACE-CONFIG Register (address = 26h) [reset = 0000h]

**Figure 7-27. INTERFACE-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
X		TIMEOUT- EN	X			RESERVE D	X					FSDO- EN	X	SDO- EN		
X-0h		R/W-0h		X-0h			R/W-0h		X-00h					R/W-0h	X-0h	R/W-0h

**Table 7-37. INTERFACE-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12	TIMEOUT-EN	R/W	0h	0: I <sup>2</sup> C timeout disabled 1: I <sup>2</sup> C timeout enabled
11-9	X	X	0h	Don't care
8	RESERVED	R/W	0h	Always write 0.
7-3	X	X	00h	Don't care
2	FSDO-EN	R/W	0h	0: Fast SDO disabled 1: Fast SDO enabled
1	X	X	0h	Don't care
0	SDO-EN	R/W	0h	0: SDO disabled 1: SDO enabled on GPIO/SDO pin

## 7.28 SRAM-CONFIG Register (address = 2Bh) [reset = 0000h]

Figure 7-28. SRAM-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								SRAM-ADDR							
X-00h								R/W-00h							

Table 7-38. SRAM-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X	X	00h	Don't care
7-0	SRAM-ADDR	R/W	00h	8-bit SRAM address. Writing to this register field configures the SRAM address to be accessed next. This address automatically increments after a write to the SRAM.

## 7.29 SRAM-DATA Register (address = 2Ch) [reset = 0000h]

Figure 7-29. SRAM-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM-DATA															
R/W-0000h															

Table 7-39. SRAM-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SRAM-DATA	R/W	0000h	16-bit SRAM data. This data is written to or read from the address configured in the SRAM-CONFIG register.

## 7.30 BRDCAST-DATA Register (address = 50h) [reset = 0000h]

Figure 7-30. BRDCAST-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRDCAST-DATA[9:0] BRDCAST-DATA[7:0]												X			
R/W-000h												X-0h			

Table 7-40. BRDCAST-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	BRDCAST-DATA[9:0] BRDCAST-DATA[7:0]	R/W	000h	Broadcast code for all DAC channels. Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: AFE532A3W: {BROADCAST-DATA[9:0], X, X} AFE432A3W: {BROADCAST-DATA[7:0], X, X, X, X}  X = Don't care bits. The BRD-CONFIG-X bit in the DAC-x-FUNC-CONFIG register must be enabled for the respective channels.
3-0	X	X	0h	Don't care.

## 8 Application and Implementation

### Note

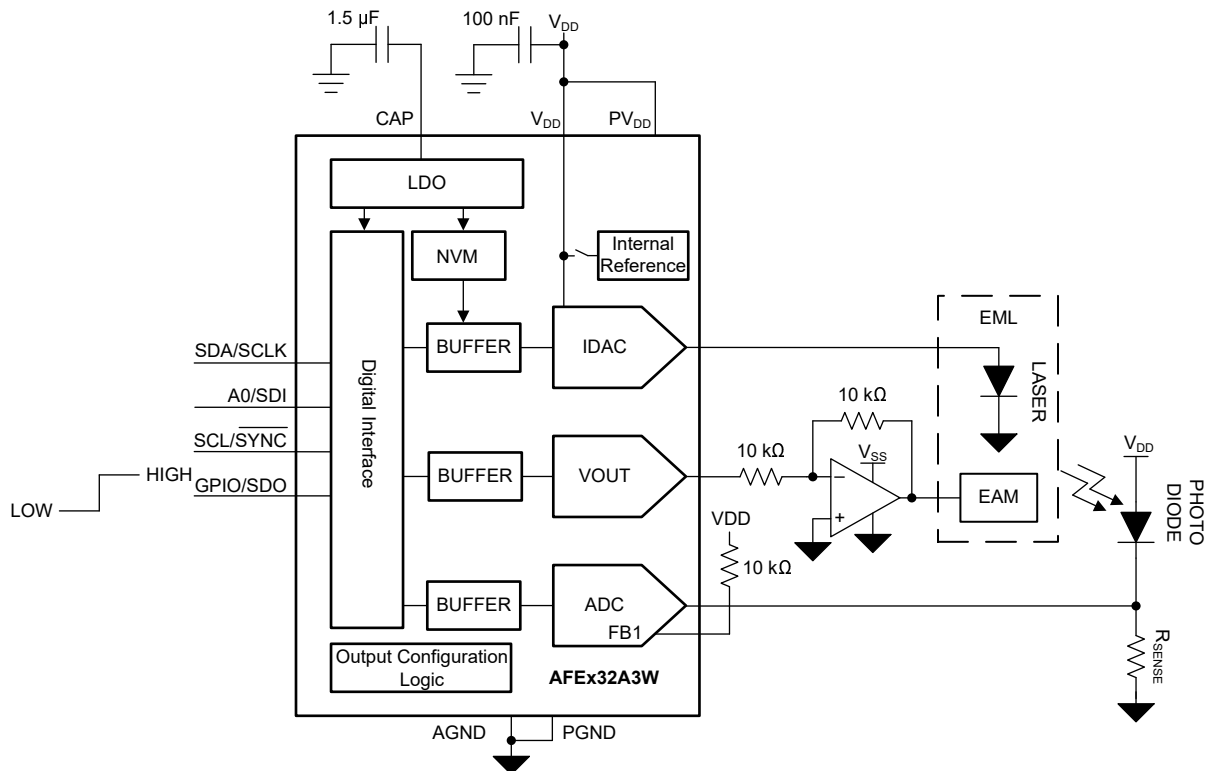
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The AFEx32A3W is a three-channel, buffered, voltage-output, current-output, and ADC input smart AFE that includes NVM and an internal reference, and is available in a 1.76-mm × 1.76-mm (nominal) package. The AFE features two dedicated DAC channels and one channel that is configurable as a DAC or an ADC. The current output DAC (IDAC) sources up to 300-mA with low headroom. The voltage-output DACs (VDACs) have configurable reference and gain options. The AFEx32A3W support Hi-Z power-down mode and Hi-Z output during power-off conditions. The multifunction GPIO, function generation, and NVM enable these smart AFEs for use without the need for run-time software.

### 8.2 Typical Application

The AFEx32A3W can be used in optical networking applications that feature electro-absorption modulated lasers (EMLs). EMLs consist of a laser and an integrated electro-absorption modulator (EAM). The AFEx32A3W IDAC output has a low headroom which is an excellent feature for applications where low-power dissipation is required. This example circuit uses the 300-mA IDAC output to bias the laser. EAMs typically require a negative voltage bias to control the intensity of the light passing through the EML. The AFEx32A3W VDAC output can be inverted with an op-amp to achieve this negative bias requirement. The integrated ADC is used to monitor the output of the EML using an external photodiode and sense resistor ( $R_{SENSE}$ ).



**Figure 8-1. Electro-Absorption Modulated Laser Biasing**

## 8.2.1 Design Requirements

**Table 8-1. Design Parameters**

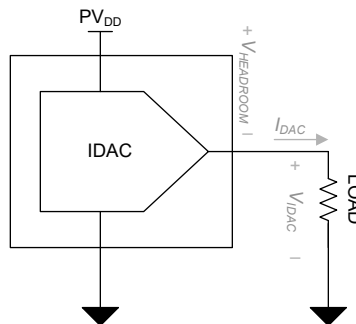
PARAMETER	VALUE
$V_{DD}$	3.3 V
$PV_{DD}$	3.3 V
IDAC nominal output	200 mA
VDAC output range	0 V to 3.3 V
ADC input range	0 V to 3.3 V
$V_{SS}$	-5 V
Negative EAM bias output range	-3.3 V to 0 V

## 8.2.2 Detailed Design Procedure

- The nominal IDAC output for this application is 200 mA. The IDAC code required to set the IDAC output to 200 mA is calculated by [Equation 9](#).

$$DAC\_2\_DATA = \frac{200 \text{ mA}}{2/3 \times 0.5241} \times 2^{10} = 586d \quad (9)$$

- The IDAC channel uses the internal reference. Enable the internal reference in the COMMON-CONFIG register before enabling the IDAC output.
- The power dissipation of the IDAC channel is a function of the  $PV_{DD}$  supply voltage, the current output, and the voltage of the IDAC pin ( $V_{IDAC}$ ). The headroom voltage ( $V_{HEADROOM}$ ) is calculated as the difference between  $PV_{DD}$  and  $V_{IDAC}$ . Minimize  $V_{HEADROOM}$  to reduce the power dissipation of the device while also meeting the minimum  $V_{HEADROOM}$  requirement. The IDAC output cannot source the full-scale current output if  $V_{HEADROOM}$  is lower than the specified voltage. [Figure 8-2](#) shows the output current directions and the key voltages that impact power dissipation. The IDAC output contributes to power dissipation proportionally to the output current multiplied by the  $V_{HEADROOM}$  voltage.



**Figure 8-2. IDAC Power Dissipation**

- The VDAC full-scale output range is set in the DAC-0-GAIN-CONFIG register. This application example uses the 3.3-V VDD as the reference with a 1 × gain. [Equation 10](#) calculates the DAC code for a 2-V output.

$$DAC\_0\_DATA = \frac{2 \text{ V}}{3.3 \text{ V}} \times 2^{10} = 621d \quad (10)$$

- The inverting op-amp circuit in this application has a gain of  $-1 \text{ V/V}$ . If the negative output range of the circuit needs to be greater than the AFE432A3W  $V_{DD}$  supply voltage, the gain of the inverting op-amp circuit can be increased. The negative op-amp supply ( $V_{SS}$ ) must be large enough to support the headroom requirement of the selected op-amp for the full-scale output of the AFE432A3W with the selected gain applied. Select an op-amp that supports the output voltage range and output current drive required by the EAM.



- When using the ADC inputs to monitor a photodiode, the value of  $R_{\text{SENSE}}$  depends on the expected current of the photodiode ( $I_{\text{PD}}$ ). Choose  $R_{\text{SENSE}}$  so that the maximum  $I_{\text{PD}}$  induces a voltage equal to the full-scale ADC input voltage. Equation 11 shows how to calculate  $R_{\text{SENSE}}$  from the maximum ADC input voltage and the maximum  $I_{\text{PD}}$ .

$$R_{\text{SENSE}} = \frac{ADC_{\text{max}}}{I_{\text{PDmax}}} \quad (11)$$

- The ADC full-scale input range is set in the DAC-1-GAIN-CMP-CONFIG register. This application example uses the 3.3-V  $V_{\text{DD}}$  as the reference with a  $1 \times$  gain. If the expected maximum  $I_{\text{PD}}$  is 10 mA,  $R_{\text{SENSE}}$  is calculated to be 330  $\Omega$  by Equation 12.

$$R_{\text{SENSE}} = \frac{3.3 \text{ V}}{10 \text{ mA}} = 330 \Omega \quad (12)$$

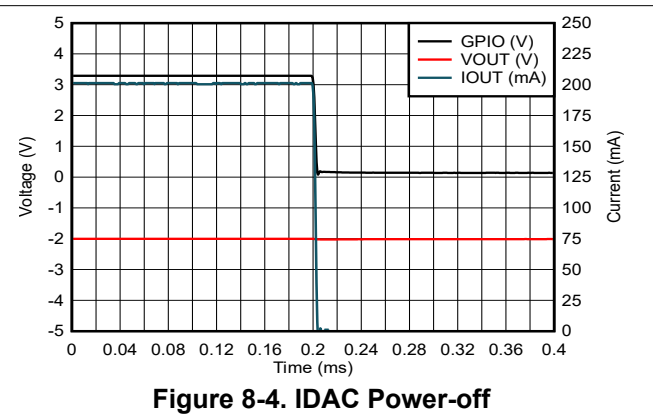
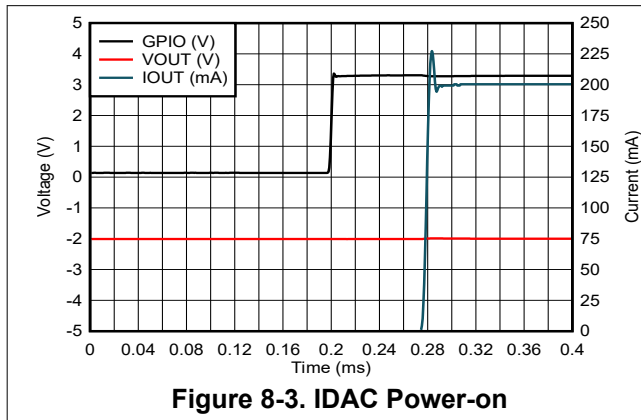
- This application uses the GPIO/SDO pin to power the IDAC output on and off. Configure the function of the GPIO/SDO pin in the GPIO-CONFIG register. The GPI-EN bit enables the GPIO/SDO pin as an input. The GPI-CH-SEL field selects which channels are controlled by the GPI. The GPI-CONFIG field selects the GPI function. Table 6-9 defines the functions for the GPI-CONFIG field.

The pseudocode for an EML bias application is as follows:

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Write DAC code for nominal IDAC output
//Set IOUT gain setting to 2/3
WRITE DAC-2-GAIN-CONFIG(0x03), 0x00, 0x00
//The 10-bit hex code for 200 mA is 0x24A. with 16-bit left alignment, this becomes 0x9280
WRITE DAC-2-DATA(0x19), 0x92, 0x80
//Set VOUT0 gain setting to 1x VDD (3.3 v)
WRITE DAC-0-GAIN-CONFIG(0x0F), 0x04, 0x00
//For a 3.3-v output range, the 10-bit hex code for 2 v is 0x26D. with 16-bit left alignment, this
becomes 0x9B40
WRITE DAC-0-DATA(0x1B), 0x9B, 0x40
//Set ADC gain setting to 1x VDD (3.3 v), enable comparator mode for ADC
WRITE DAC-1-GAIN-CMP-CONFIG(0x15), 0x04, 0x01
//Power-up output on VDAC and ADC channels, enables internal reference
WRITE COMMON-CONFIG(0x1F), 0x12, 0x5F
//Configure GPI for Power-Up, Down trigger for IDAC channel
WRITE GPIO-CONFIG(0x24), 0x00, 0x29
//Enable the ADC and configure the averaging setting and channel select
WRITE ADC-CONFIG-TRIG(0x1D), 0x23, 0xC0
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02

//Use GPIO pin to power on/off IDAC
//ADC trigger
WRITE ADC-CONFIG-TRIG(0x1D), 0x23, 0xC1
//ADC readback
READ ADC-DATA(0x1E)
```

### 8.2.3 Application Curves



### 8.3 Power Supply Recommendations

The AFE<sub>x</sub>32A3W do not require specific power-supply sequencing. These devices require a single power supply,  $V_{DD}$  and  $PV_{DD}$ . Short  $V_{DD}$  and  $PV_{DD}$  with a low-impedance PCB trace. To minimize noise from the power supply, connect a 1- $\mu$ F to 10- $\mu$ F capacitor and 100-nF bypass capacitor. Use a bypass capacitor with a value approximately 1.5  $\mu$ F for the CAP pin.

#### Note

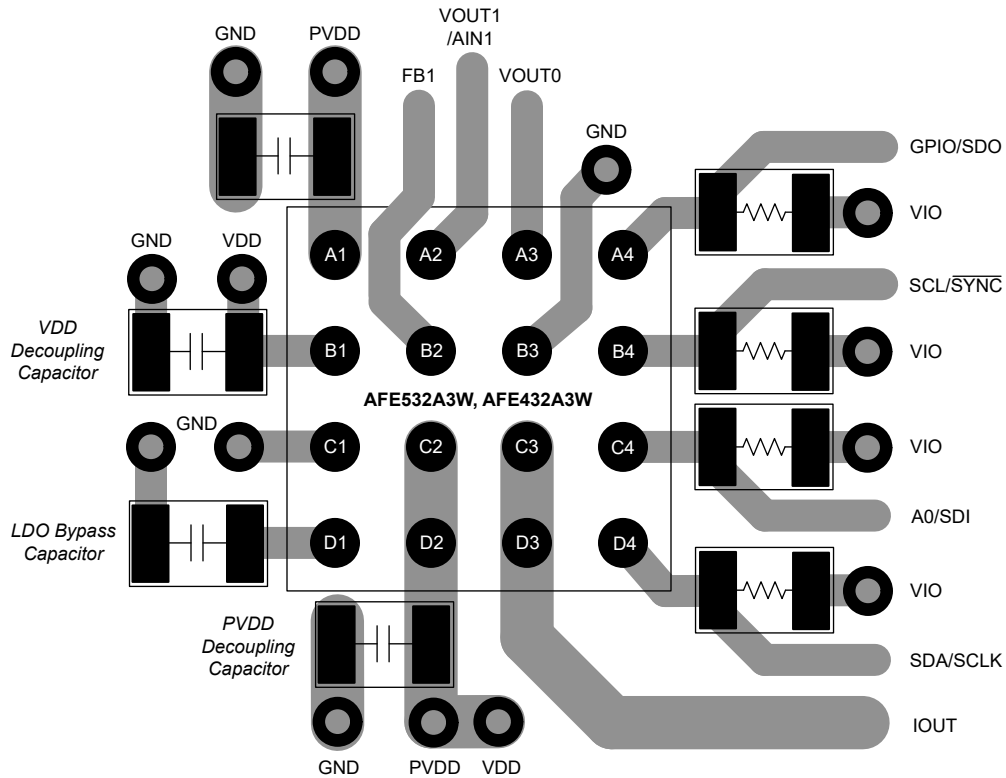
The AFE<sub>x</sub>32A3W do not provide automatic thermal shutdown. Therefore, the external circuit design must maintain the junction temperature within the specified limits.

## 8.4 Layout

### 8.4.1 Layout Guidelines

The AFE<sub>x</sub>32A3W pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

### 8.4.2 Layout Example



**Figure 8-5. Layout Example**

Note: The ground and power planes have been omitted for clarity.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

The following EVM user's guide is available: [AFE532A3W Evaluation Module](#) user's guide

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

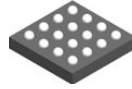
## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2023) to Revision A (July 2025)	Page
• Updated <i>Device Information</i> table.....	<a href="#">1</a>
• Changed package dimensions from 1.72-mm × 1.72-mm to 1.76-mm × 1.76-mm in <i>Application Information</i>	<a href="#">79</a>
• Updated YBH package outline with corrected dimensions.....	<a href="#">84</a>

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

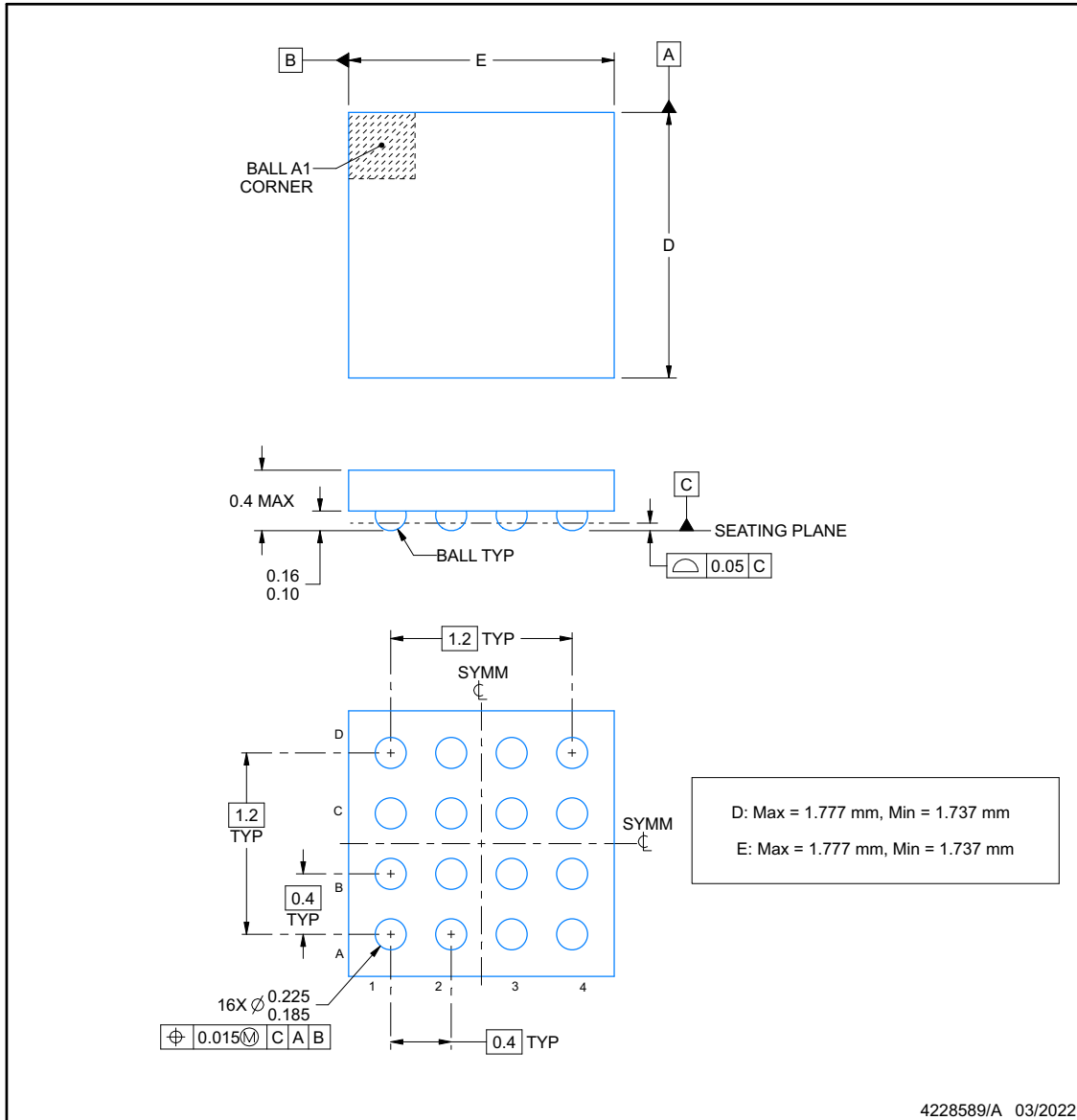


**PACKAGE OUTLINE**

**YBH0016-C03**

**DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



**NOTES:**

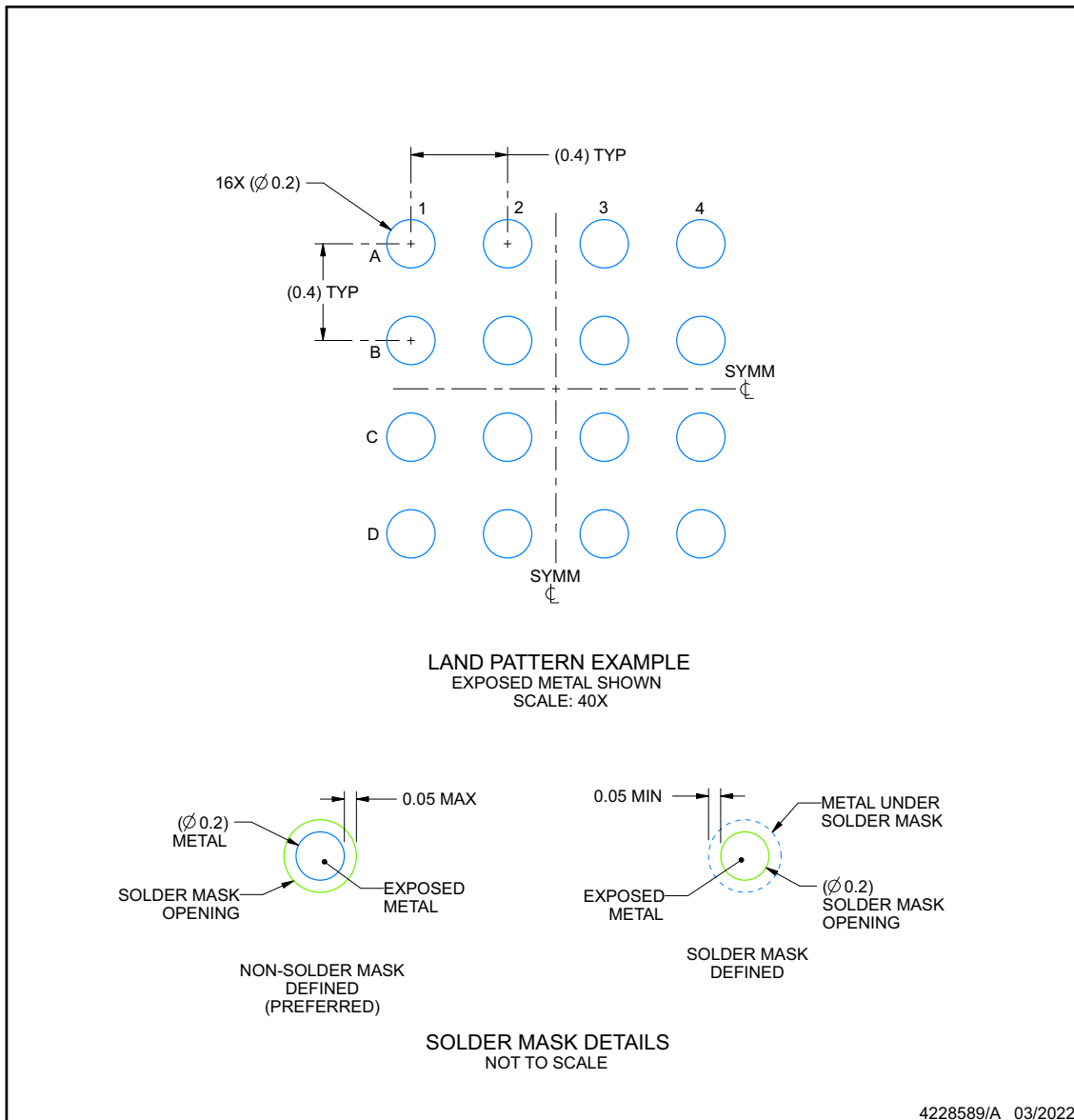
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

**YBH0016-C03**

**DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

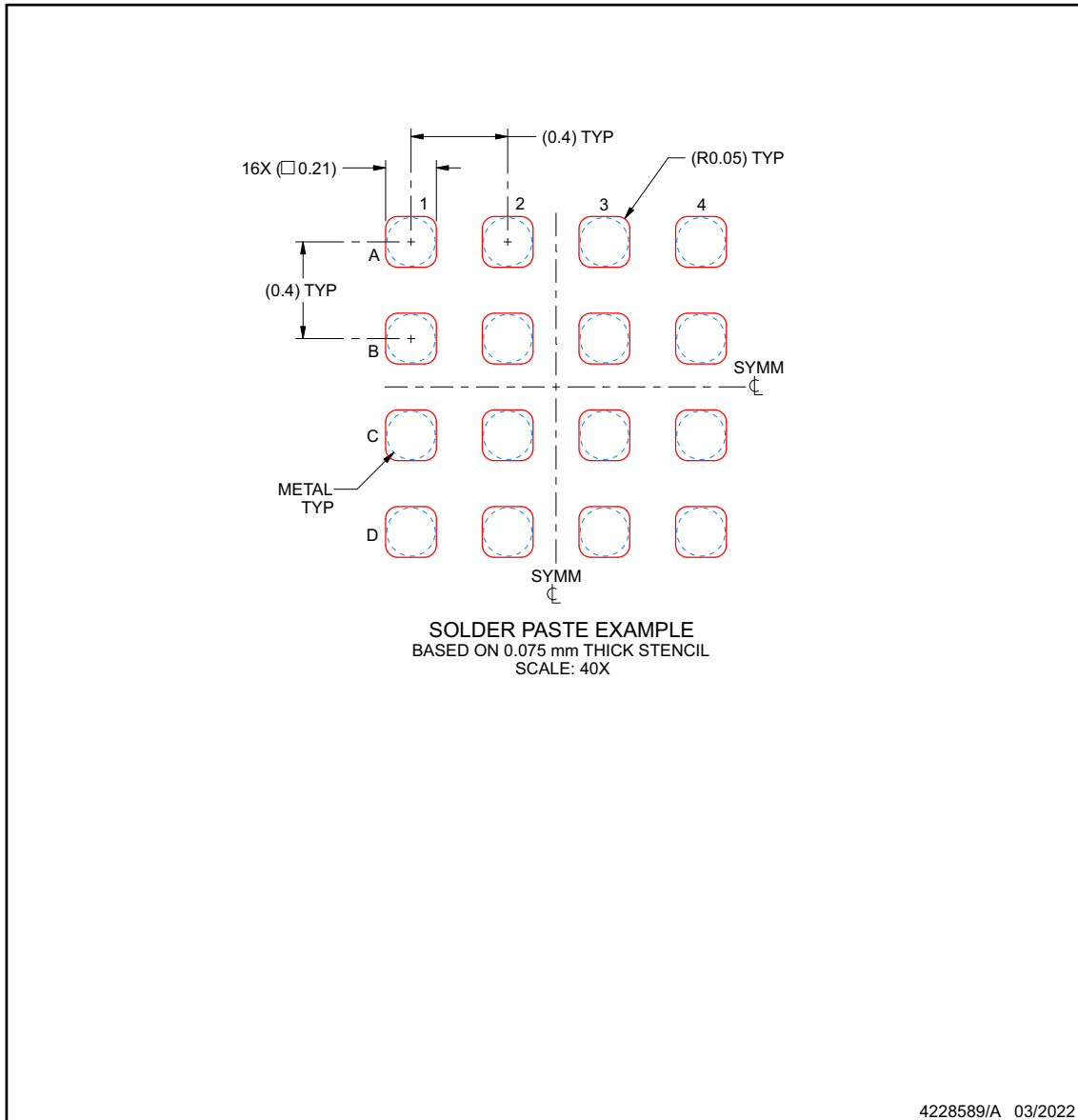
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

## EXAMPLE STENCIL DESIGN

**YBH0016-C03**

**DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">AFE432A3YBHR</a>	Active	Production	DSBGA (YBH)   16	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AFE 432A3
AFE432A3YBHR.A	Active	Production	DSBGA (YBH)   16	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AFE 432A3
<a href="#">AFE532A3YBHR</a>	Active	Production	DSBGA (YBH)   16	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AFE 532A3
AFE532A3YBHR.A	Active	Production	DSBGA (YBH)   16	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AFE 532A3

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE432A3YBHR	DSBGA	YBH	16	3000	180.0	8.4	1.94	1.94	0.69	4.0	8.0	Q1
AFE532A3YBHR	DSBGA	YBH	16	3000	180.0	8.4	1.94	1.94	0.69	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE432A3YBHR	DSBGA	YBH	16	3000	182.0	182.0	20.0
AFE532A3YBHR	DSBGA	YBH	16	3000	182.0	182.0	20.0

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