AFE10004-EP 4-Channel Power-Amplifier Precision Analog Front End With Integrated EEPROM and Gate Bias Switches

1 Features

- Specified for defense and aerospace applications
- Controlled baseline
- One assembly and test site
- One fabrication site
- Product traceability
- Extended product life cycle
- Local and remote diode temperature sensor
  - ±2.5°C error, maximum
  - 0.0625°C resolution
- Internal EEPROM for autonomous operation
  - Storage for four independent transfer functions
  - Device configuration storage
  - Open space for user storage
  - Qualified for 15-year retention
- Four analog outputs
  - Four monotonic DACs: 1.22mV resolution
  - Automatically configured output ranges:
    - Positive output voltage: 5.5V, maximum
    - Negative output voltage: –10V, minimum
  - High current drive capability:
    - Source up to 100mA
    - Sink up to 20mA
  - High capacitive load tolerant: up to 15µF
- Gate bias on and off control switches
  - Two programmable off voltages
    - Two auxiliary DACs: 1.22mV resolution
  - Fast switching time: 50ns, typical
  - Low resistance: 3Ω, maximum
- Built-in sequencing control
- Internal 2.5V reference
- SPI and I^2C interfaces: 1.7V to 3.6V operation
  - SPI: 4-wire Interface
  - I^2C: Eight selectable peripheral addresses
- Specified temperature range: –55°C to +125°C

2 Applications

- Radar
- Electronic warfare
- Communications payload
- Defense radio

3 Description

The AFE10004-EP is a highly integrated, autonomous, power-amplifier (PA) precision analog front end (AFE) that includes four temperature compensation digital-to-analog converters (DACs), integrated EEPROM, and gate bias switches. The four DACs are programmed by four independent, user-defined, temperature-to-voltage transfer functions stored in the internal EEPROM. This design allows correction any temperature effects to be corrected without additional external circuitry. After start-up, the device operates without intervention from a system controller to provide a complete system for setting and compensating bias voltages in control applications.

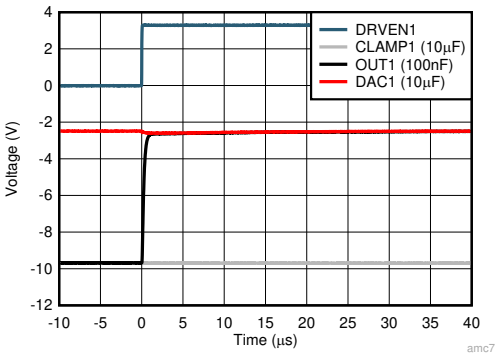
The AFE10004-EP has four gate bias outputs that are switched on and off through dedicated control pins. The gate bias switches are designed for fast response. In combination with the device PA_ON pin, this fast response enables correct power sequencing and protection of depletion-mode transistors, such as GaAs and GaN.

The function integration and wide operating temperature range make the AFE10004-EP an excellent choice as an all-in-one, autonomous bias control circuit for the power amplifiers found in RF systems. The flexible DAC output ranges and built-in sequencing features let the device be used as a biasing controller for a large variety of transistor technologies, such as LDMOS, GaAs, and GaN.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AFE10004-EP	RGE (VQFN, 24)	4mm × 4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Gate Bias Switch Response

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4 Pin Configuration and Functions

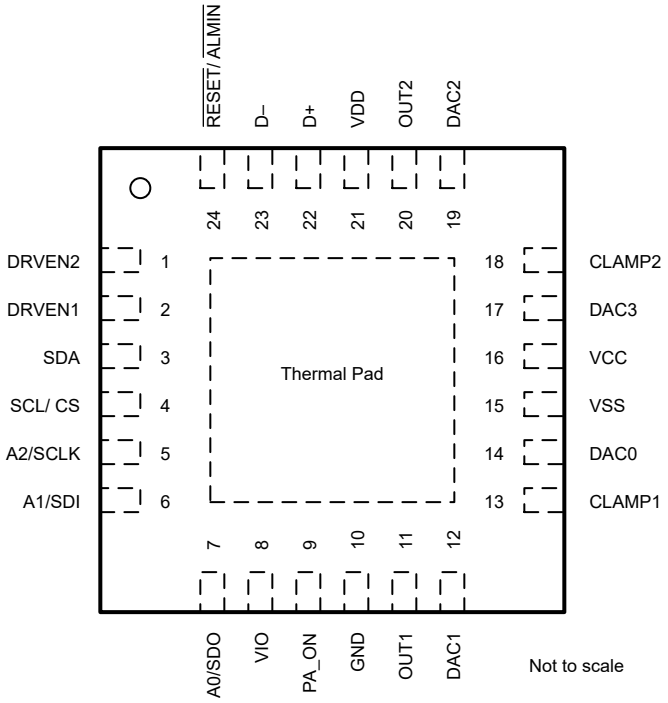

Figure 4-1. RGE Package, 24-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DRVEN2	Input	Asynchronous switch control signals.
2	DRVEN1	Input	
3	SDA	Input/Output	I^2C bidirectional data line. *This pin must be connected to GND if communicating to the device through SPI.*
4	SCL/ $\overline{CS}$	Input	I^2C: Clock input. SPI: Active-low serial data enable. This input is the frame synchronization signal for the serial data. When the signal goes low, this pin enables the serial interface input shift register.
5	A2/SCLK	Input	I^2C: Target address selector. SPI: Clock input.
6	A1/SDI	Input	I^2C: Target address selector. SPI: Data input. Data are clocked into the input shift register on each falling edge of the SCLK pin.
7	A0/SDO	Input/Output	I^2C: Target address selector. SPI: Data output. The SDO pin must be enabled before operation by setting the SDOEN bit. Data are clocked out of the input shift register on each rising edge of the SCLK pin.
8	VIO	Power	IO supply voltage (1.65V to 3.6V). This pin sets the I/O operating voltage for the device.
9	PA_ON	Output	Synchronization signal. PA_ON is a CMOS output. The PA_ON pin is set low until the device is ready for full operation or if an alarm condition is detected.
10	GND	Ground	Ground reference point for all circuitry on the device
11	OUT1	Output	DAC1 switch output
12	DAC1	Output	DAC1 buffer output
13	CLAMP1	Output	CLAMP1 buffer output
14	DAC0	Output	DAC0 buffer output
15	VSS	Power	Output buffers negative analog power supply (–11V to 0V)
16	VCC	Power	Output buffers positive analog power supply (0V to 5.5V)
17	DAC3	Output	DAC3 buffer output
18	CLAMP2	Output	CLAMP2 buffer output
19	DAC2	Output	DAC2 buffer output
20	OUT2	Output	DAC2 switch output
21	VDD	Power	Analog supply voltage (4.5V to 5.5V)
22	D+	Input	Remote temperature sensor connections. If unused, connect these pins together.
23	D–	Input	
24	$\overline{RESET}$/ $\overline{ALMIN}$	Input	Active low reset input. Logic low on this pin causes the device to initiate a reset event. Alternatively, this pin can be configured as an active-low alarm signal into the device to initiate an alarm event.
Thermal Pad	Thermal Pad	—	The thermal pad is located on the package underside. Connect the thermal pad to any internal PCB ground plane through multiple vias for good thermal performance.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Supply voltage	V_{DD} to GND	–0.3	6	V
		V_{IO} to GND	–0.3	6	V
		V_{CC} to GND	–0.3	6	V
		V_{SS} to GND	–12	0.3	V
		V_{CC} to V_{SS}	–0.3	12	V
	Pin voltage	DAC[0:3] and CLAMP[1:2] to GND	V_{SS} – 0.3	V_{CC} + 0.3	V
		OUT[1:2] to GND	V_{SS} – 0.3	V_{CC} + 0.3	V
		PA_ON and SDO to GND	–0.3	V_{IO} + 0.3	V
		Digital input pins to GND	–0.3	6	V
		Remote temperature sensor pins to GND	–0.3	V_{DD} + 0.3	V
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Analog supply voltage	4.5		5.5	V
V_{IO}	Digital IO supply voltage	1.65		3.6	V
V_{CC} (1)	Output buffer positive supply voltage	4.5		5.5	V
V_{SS} (2)	Output buffer negative supply voltage	–11		–4.5	V
$V_{CC} – V_{SS}$	Output buffer supply voltage range	4.5		11	V
	Digital pin input voltage	0		3.6	V
T_A	Operating ambient temperature	–55		125	°C
$T_{J,SPEC}$	Specified junction temperature	–55		125	°C
$T_{J,OPER}$	Operating junction temperature	–55		150	°C
$T_{J,EEPROM}$	EEPROM programming junction temperature	0		125	°C

(1) V_{CC} must be connected to GND when the device is configured for negative output voltage range operation.
(2) V_{SS} must be connected to GND when the device is configured for positive output voltage range operation.

5.4 Thermal Information

THERMAL METRIC[1]		AFE10004-EP RGE (VQFN) 24 PINS	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance	33.5	°C/W
$\Theta_{JC(top)}$	Junction-to-case (top) thermal resistance	30.2	°C/W
Θ_{JB}	Junction-to-board thermal resistance	13.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.5	°C/W
$\Theta_{JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

all minimum and maximum specifications at T_J = –55°C to +125°C and all typical specifications at T_J = 25°C, V_{DD} = 4.5V to 5.5V, V_{IO} = 1.65V to 3.6V, positive output range: V_{CC} = 4.5V to 5.5V, V_{SS} = GND, negative output range: V_{SS} = –11V to –4.5V, V_{CC} = GND, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC CHARACTERISTICS[1]						
	Resolution		13			Bits
	Full-scale output voltage	Set at start-up through auto-range detection	–10		0	V
		Set at start-up through auto-range detection	0		10	
DNL	Differential nonlinearity	Specified 13-bit monotonic	–1		1	LSB
INL	Integral nonlinearity		–4		4	LSB
TUE	Total unadjusted error		–0.4	±0.1	0.4	%FSR
	Total adjusted error	After one point calibration at 25°C, DAC output at 1/4 of full-scale range	–0.06	±0.01	0.06	%FSR
	Offset error	Positive output range	–24	±5	24	mV
		Negative output range	–24	±5	24	
	Offset error temperature drift			±2		ppm/°C
	Gain error		–0.3	±0.01	0.3	%FSR
	Gain error temperature drift			±5		ppm/°C
	Zero-scale error	Positive output range: all zeros code	0	5	24	mV
		Negative output range: all ones code	–24	–5	0	
	Zero-scale error temperature drift			±2		ppm/°C
	Full-scale error	Positive output range: all ones code	–0.25	±0.03	0.25	%FSR
		Negative output range: all zeros code	–0.4	±0.05	0.4	
	Full-scale error temperature drift			±5		ppm/°C
	Load current[2]	Source with 1V headroom from V_{CC}, high-current mode, number of active channels ≤ 2	100			mA
		Sink with 1V headroom from V_{SS}, high- and normal-current modes	20			
	Short circuit current, source[2]	Start-up current mode		12		mA
		Normal-current mode		70		
		High-current mode		120		

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5.5 Electrical Characteristics (continued)

all minimum and maximum specifications at T_J = –55°C to +125°C and all typical specifications at T_J = 25°C, V_{DD} = 4.5V to 5.5V, V_{IO} = 1.65V to 3.6V, positive output range: V_{CC} = 4.5V to 5.5V, V_{SS} = GND, negative output range: V_{SS} = –11V to –4.5V, V_{CC} = GND, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Short circuit current, sink(2)	Start-up current mode		12		mA
		Normal-current mode		40		
		High-current mode		40		
	Capacitive load stability		0		15	µF
	DC output impedance	DAC[0,3], midscale code		10		Ω
		DAC[1,2], CLAMP[1,2], midscale code		3		
	Output voltage settling time	C_L = 15 µF, 2.5V step to within 2.5mV		400		µs
	Output noise	0.1Hz to 10Hz, midscale code		70		$µV_{PP}$
	Output noise density	1kHz, midscale code		700		nV/√Hz
	AC PSRR	Midscale code, frequency = 60Hz, amplitude = 200mV_{PP} superimposed on V_{CC} or V_{SS}		75		dB
		Midscale code, frequency = 60Hz, amplitude = 200mV_{PP} superimposed on V_{DD}		60		
	DC PSRR	Midscale code, V_{DD} = 5V ± 10%, V_{CC} = 5V ± 10%, V_{SS} = –10V ± 10%		0.15		mV/V
	Channel-to-channel DC crosstalk	Measured DAC output at midscale, all other DAC outputs at full-scale, CLAMP outputs at zero-scale		150		µV
AUTO-RANGE THRESHOLD DETECTOR						
V_{SSTH}	Auto-supply monitor threshold	Narrow V_{SS} supply failure detect (default)	–3.8		–2.8	V
V_{SSWTH}	Auto-supply monitor threshold	Wide V_{SS} supply failure detect, set by register write or loaded from EEPROM	–6.8		–5.8	V
V_{CCTH}	Auto-supply monitor threshold	V_{CC} supply failure detect	2.3		3.3	V
OUTPUT SWITCH DC CHARACTERISTICS						
$R_{1,2}$	On resistance between DAC[1,2] and OUT[1,2] or CLAMP[1,2] and OUT[1,2]	Negative output range, 1.5V headroom from V_{SS}		2	3	Ω
		Positive output range, 1.5V headroom from V_{DD}		2	3	
$R_{0,3}$	On resistance between DAC buffers and DAC[0,3] or between DAC[0,3] and CLAMP[1,2]	Negative output range, 1.5V headroom from V_{SS}		9	14	Ω
		Positive output range, 1.5V headroom from V_{CC}		10	16	
C_{OUT}	OUT[1,2] output impedance			100		pF

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5.5 Electrical Characteristics (continued)

all minimum and maximum specifications at T_J = –55°C to +125°C and all typical specifications at T_J = 25°C, V_{DD} = 4.5V to 5.5V, V_{IO} = 1.65V to 3.6V, positive output range: V_{CC} = 4.5V to 5.5V, V_{SS} = GND, negative output range: V_{SS} = –11V to –4.5V, V_{CC} = GND, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOCAL TEMPERATURE SENSOR CHARACTERISTICS						
	Operating junction temperature		–55		150	°C
	Accuracy	T_J = –55°C to +125°C		1.25	2.5	°C
	Resolution	LSB size		0.0625		°C
	Update time	32 conversions per second		31.25		ms
REMOTE TEMPERATURE SENSOR CHARACTERISTICS (Using 2N3906 Transistor)						
	Operating junction temperature		–55		150	°C
	Accuracy	T_{DIODE} = –55°C to +150°C		1.25	2.5	°C
	Resolution	LSB size		0.0625		°C
	Update time	32 conversions per second		31.25		ms
DIGITAL INPUTS						
V_{IH}	High-level input voltage		1.3			V
V_{IL}	Low-level input voltage				0.45	V
	Hysteresis voltage			90		mV
	Input current			1		µA
	Input pin capacitance			5		pF
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage	Load current = 1mA	V_{IO} – 0.2			V
V_{OL}	Low-level output voltage	Load current= –1mA			0.4	V
	Output pin capacitance			5		pF
POWER REQUIREMENTS						
I_{VDD}	V_{DD} supply current	Positive output range			5	mA
		Negative output range			5	
I_{VCC}	V_{CC} supply current	Positive output range, midscale output			3	mA
I_{VSS}	V_{SS} supply current	Negative output range, 1/4 of full-scale output			3	mA
I_{VIO}	V_{IO} supply current				10	µA

(1) End point fit between codes 64 to 8128 for negative output range and 64 to 4032 for positive output range.
(2) Overload condition protection. Junction temperature potentially exceeds during current limit. Operation greater than the specified maximum junction temperature potentially impairs device reliability.

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5.6 Timing Requirements

all minimum and maximum specifications at T_J = –55°C to +125°C and all typical specifications at T_J = 25°C, V_{DD} = 4.5V to 5.5V, V_{IO} = 1.65V to 3.6V, positive output range: V_{CC} = 4.5V to 5.5V, V_{SS} = GND, negative output range: V_{SS} = –11V to –4.5V, V_{CC} = GND, and DAC outputs unloaded (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I²C TIMING REQUIREMENTS					
$f_{(SCL)}$	I²C clock frequency	10		400	kHz
$t_{(LOW)}$	SCL clock low period	1.3			µs
$t_{(HIGH)}$	SCL clock high period	0.6			µs
$t_{(HDSTA)}$	Hold time after repeated start condition. After this period, the first clock is generated	0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time	0.6			µs
$t_{(SUSTO)}$	Stop condition setup time	0.6			µs
$t_{(BUF)}$	Bus free time between stop and start condition	1.3			µs
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(HDDAT)}$	Data hold time	0		900	ns
$t_{F,SDA}$	Data fall time	20		300	ns
$t_{F,SCL}$	Clock fall time			300	ns
$t_{R,SCL}$	Clock rise time			300	ns
$t_{R,SCL100}$	Rise time for SCL ≤ 100kHz			1000	ns
	SCL and SDA timeout	20		30	ms
SPI TIMING REQUIREMENTS, V_{IO} = 2.7V to 3.6V					
$f_{(SCLK)}$	SPI clock frequency			20	MHz
$t_{(SCLKLOW)}$	Clock high time	20			ns
$t_{(SCLKHIGH)}$	Clock low time	20			ns
$t_{(SDISU)}$	Data setup time	10			ns
$t_{(SDIHD)}$	Data hold time	10			ns
$t_{(SDODLY)}$	SDO delay	0		20	ns
$t_{(SDODIS)}$	SDO disable	0		20	ns
$t_{(CSSU)}$	$\overline{CS}$ setup	10			ns
$t_{(CSHD)}$	$\overline{CS}$ hold	20			ns
$t_{(CSHIGH)}$	$\overline{CS}$ pulse-width	25			ns
SPI TIMING REQUIREMENTS, V_{IO} = 1.65V to 2.7V					
$f_{(SCLK)}$	SPI clock frequency			10	MHz
$t_{(SCLKLOW)}$	Clock high time	40			ns
$t_{(SCLKHIGH)}$	Clock low time	40			ns
$t_{(SDISU)}$	Data setup time	10			ns
$t_{(SDIHD)}$	Data hold time	10			ns
$t_{(SDODLY)}$	SDO delay	0		30	ns
$t_{(SDODIS)}$	SDO disable	0		30	ns
$t_{(CSSU)}$	$\overline{CS}$ setup	10			ns
$t_{(CSHD)}$	$\overline{CS}$ hold	20			ns
$t_{(CSHIGH)}$	$\overline{CS}$ pulse-width	25			ns

5.7 Switching Characteristics

all minimum and maximum specifications at T_J = –55°C to +125°C and all typical specifications at T_J = 25°C, V_{DD} = 4.5V to 5.5V, V_{IO} = 1.65V to 3.6V, positive output range: V_{CC} = 4.5V to 5.5V, V_{SS} = GND, negative output range: V_{SS} = –11V to –4.5V, V_{CC} = GND, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT SWITCH AC CHARACTERISTICS						
t_{ON}	On time	Midscale code, R_L = 100kΩ		40		ns
t_{OFF}	Off time	Midscale code, R_L = 100kΩ		50		ns
PA_ON CHARACTERISTICS						
t_{PA_ON}	PA_ON turn-on time	Measured from reset event, unloaded, default register configuration			120	ms
t_{PA_OFF}	PA_ON turn-off time	Measured from an $\overline{\text{ALMIN}}$ alarm event, unloaded			50	ns
OUTPUT CHARACTERISTICS						
t_{OUT_CLM}	OUT[1:2] clamp time	Time for output to go to CLAMP DAC voltage, measured from reset event, C_L = 15µF			100	ms
t_{OUT_LUT}	OUT[1:2] ready time	Time for LUT-based output to be ready, measured from reset event, C_L = 15µF			120	ms

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5.8 Timing Diagrams

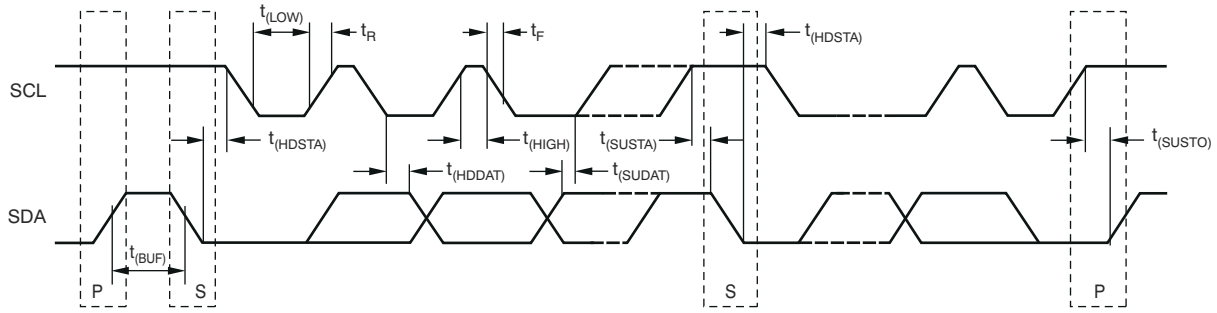

Figure 5-1. I²C Timing Diagram

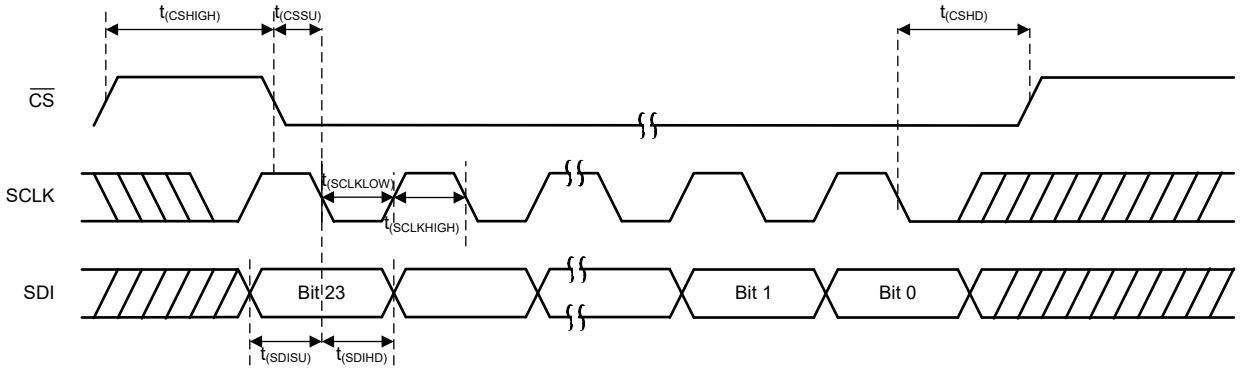

Figure 5-2. SPI Write Timing Diagram

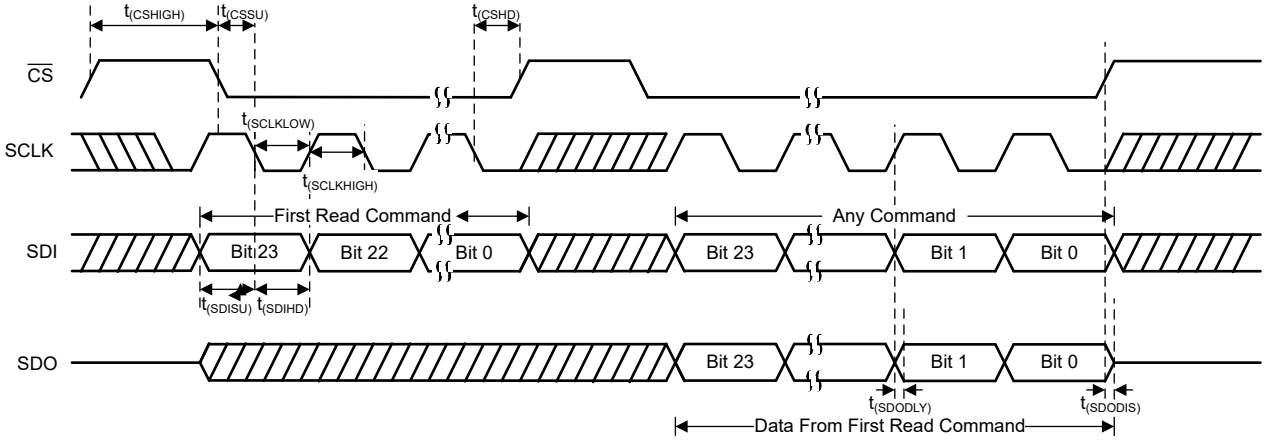

Figure 5-3. SPI Read Timing Diagram

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5.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)

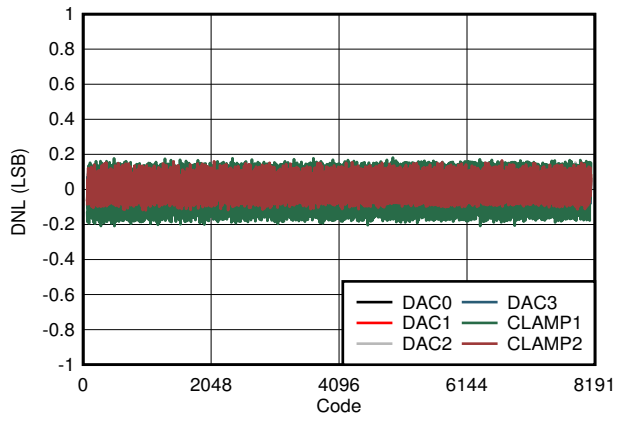


Figure 5-4. DAC DNL vs Digital Input Code

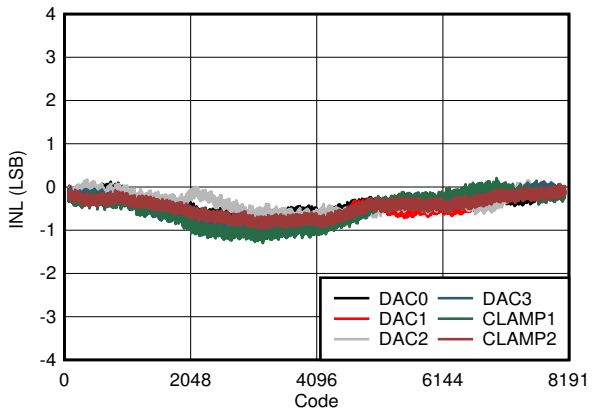


Figure 5-5. DAC INL vs Digital Input Code

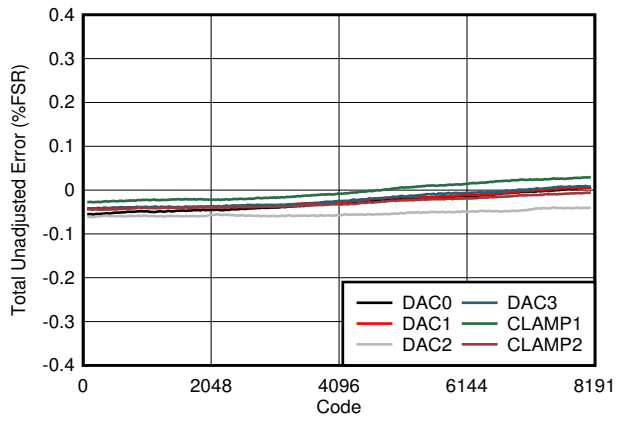


Figure 5-6. DAC TUE vs Digital Input Code

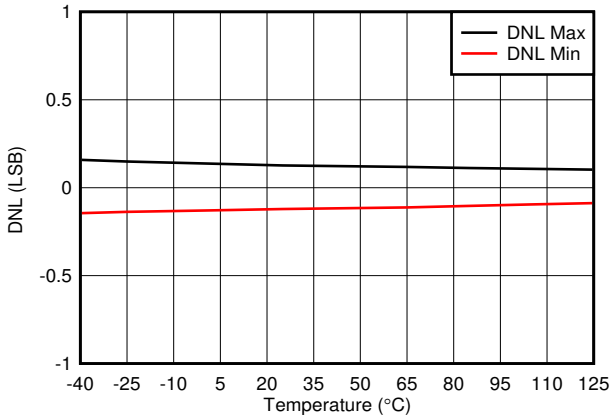


Figure 5-7. DAC DNL vs Temperature

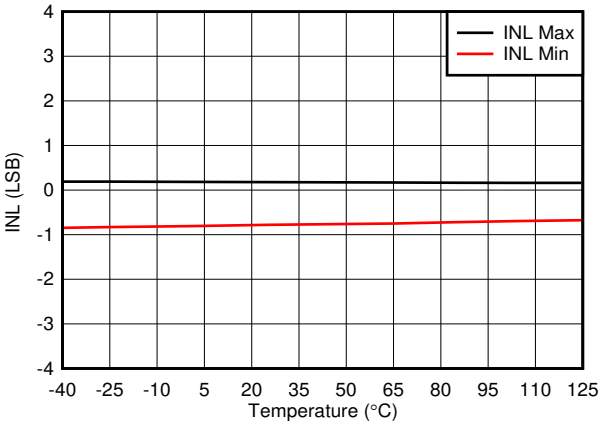
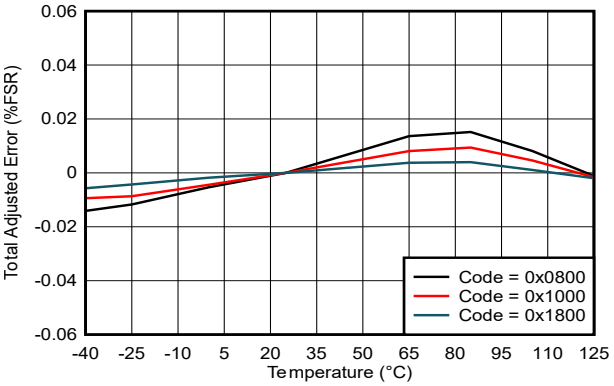


Figure 5-8. DAC INL vs Temperature



Error after one point calibration at 25°C

Figure 5-9. DAC Total Adjusted Error vs Temperature

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5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)

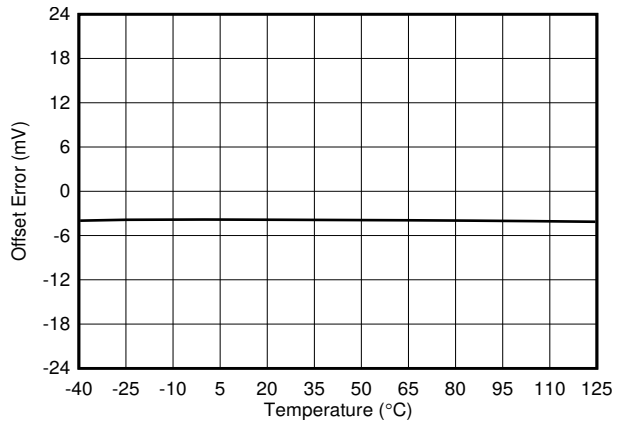


Figure 5-10. DAC Offset Error vs Temperature

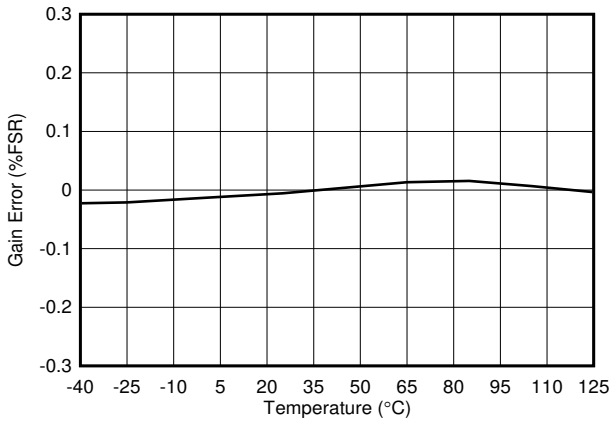
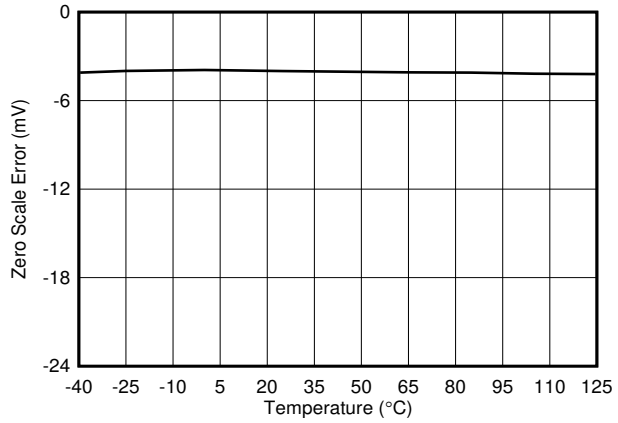
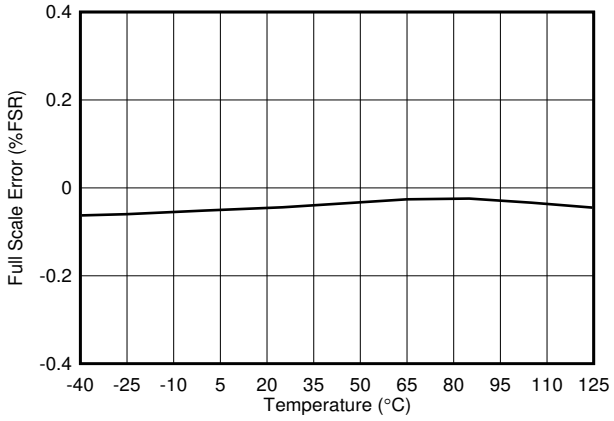


Figure 5-11. DAC Gain Error vs Temperature



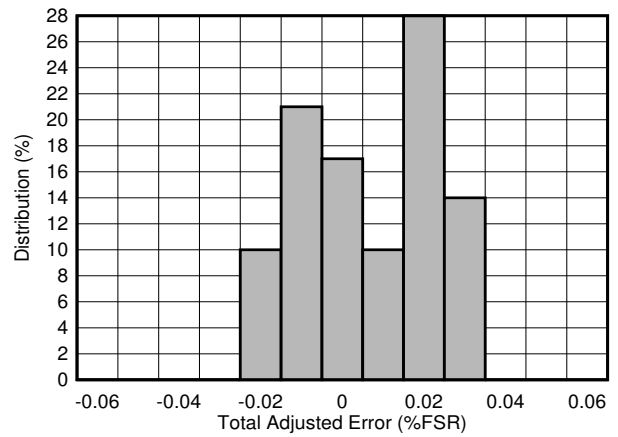
DAC code = 0x1FFF

Figure 5-12. DAC Zero-Scale Error vs Temperature



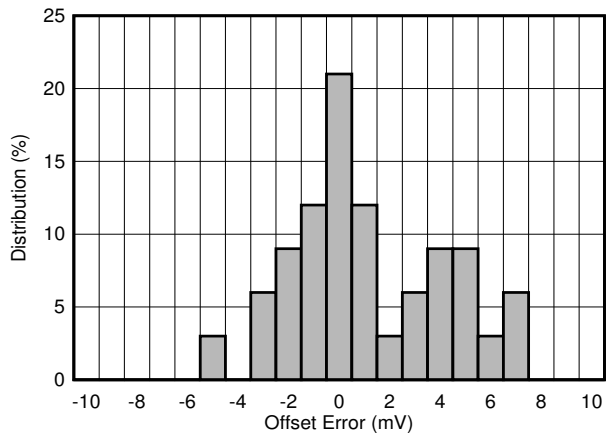
DAC code = 0x0000

Figure 5-13. DAC Full-Scale Error vs Temperature



DAC code = 0x1800
T_A = –40°C to +125°C

Figure 5-14. DAC Total Adjusted Error

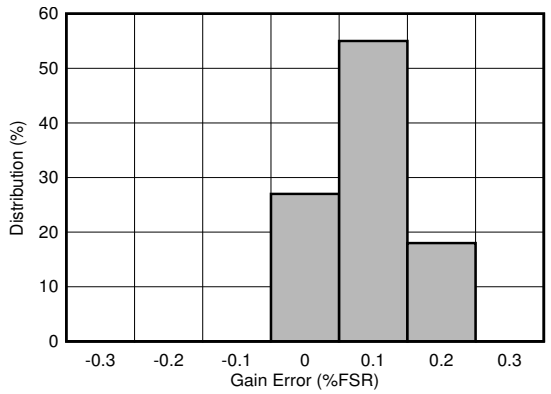


T_A = –40°C to +125°C

Figure 5-15. DAC Offset Error

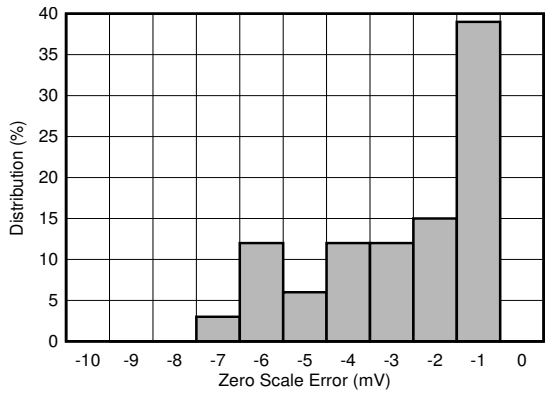
5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)



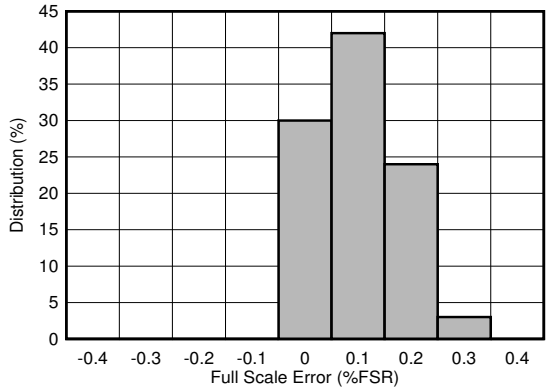
T_A = –40°C to +125°C

Figure 5-16. DAC Gain Error



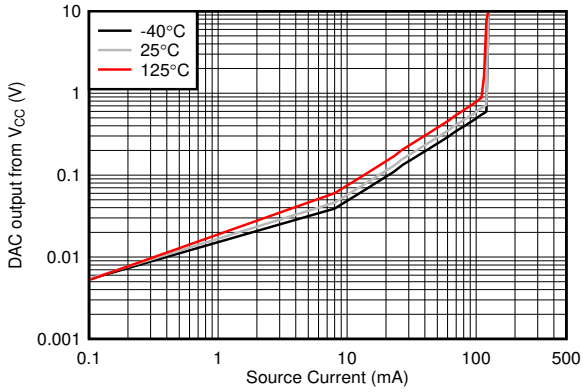
DAC code = 0x1FFF
T_A = –40°C to +125°C

Figure 5-17. DAC Zero-Scale Error



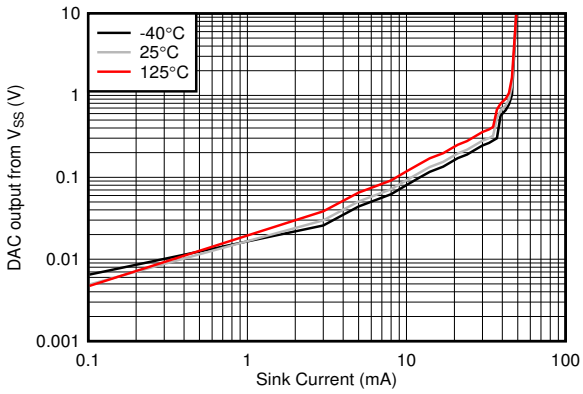
DAC code = 0x0000
T_A = –40°C to +125°C

Figure 5-18. DAC Full-Scale Error



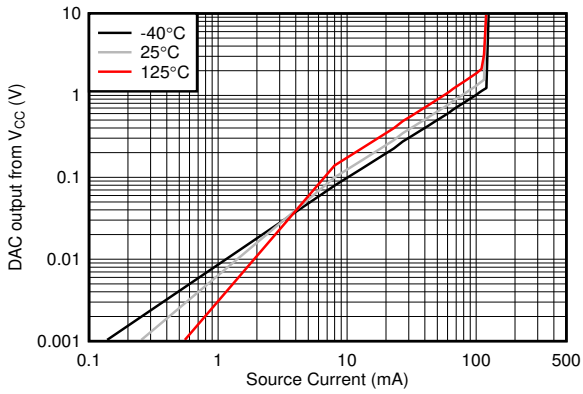
DAC code = 0x1FFF

Figure 5-19. DAC[1:2], CLAMP[1:2] Headroom vs High-Mode Sourcing Current



DAC code = 0x0000

Figure 5-20. DAC[1:2], CLAMP[1:2] Headroom vs High-Mode Sinking Current



DAC code = 0x1FFF

Figure 5-21. DAC[0:3] Headroom vs High-Mode Sourcing Current

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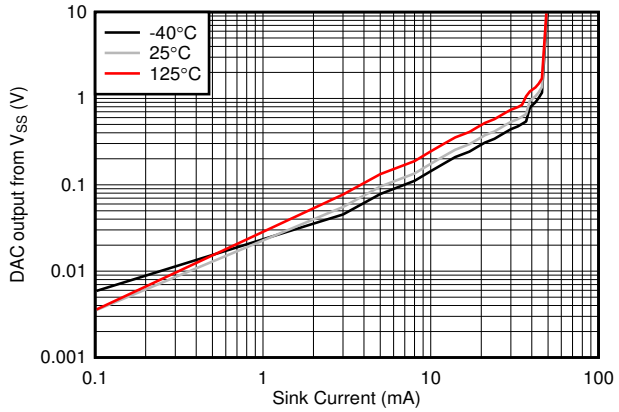
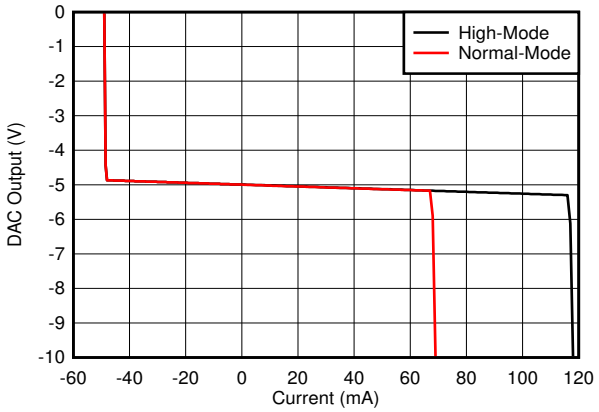
5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)



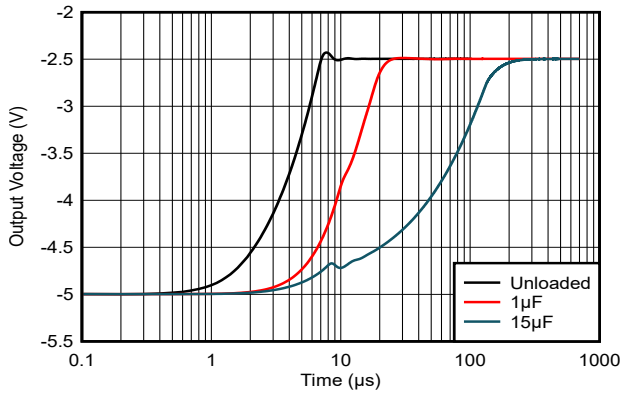
DAC code = 0x0000

Figure 5-22. DAC[0:3] Headroom vs High-Mode Sinking Current



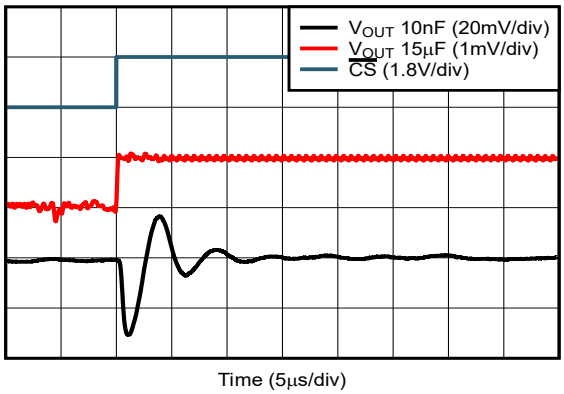
DAC code = 0x1000

Figure 5-23. Source and Sink Current Capability



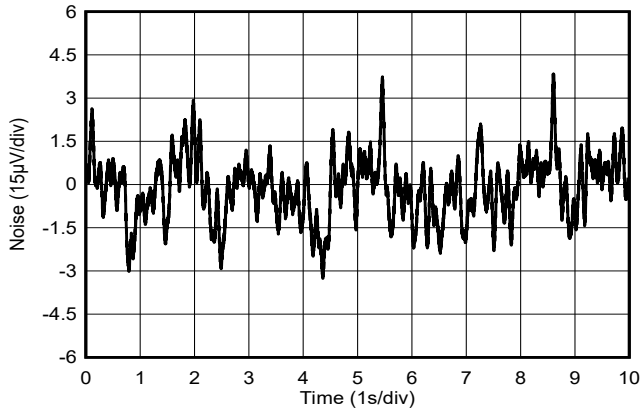
DAC step size: –5V to –2.5V

Figure 5-24. DAC Settling Time vs Capacitive Load



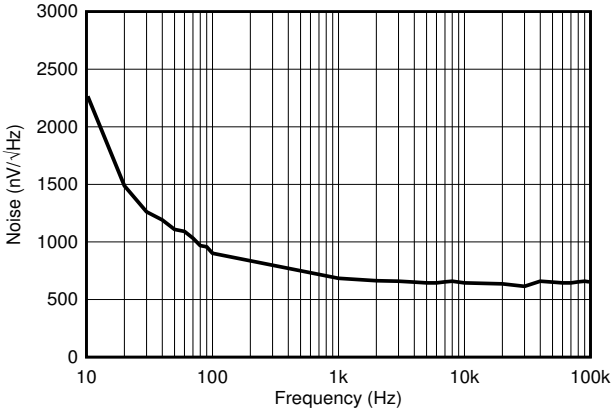
DAC code: 0x0FFF to 0x1000

Figure 5-25. DAC Glitch Impulse



DAC code = 0x1000

Figure 5-26. DAC Output Noise, 0.1Hz to 10Hz



DAC code = 0x1000

Figure 5-27. DAC Output Noise Density vs Frequency

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)

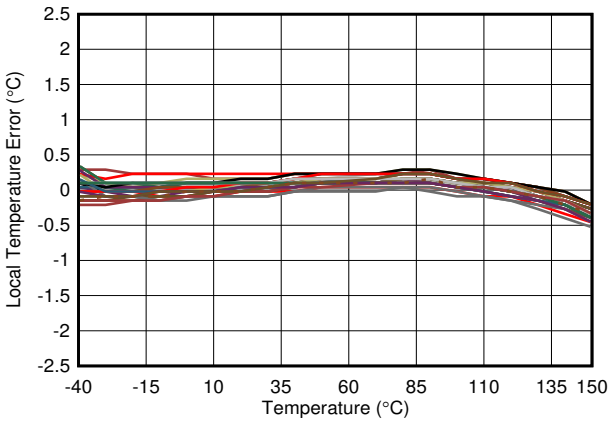


Figure 5-28. Local Temperature Sensor Error vs Temperature

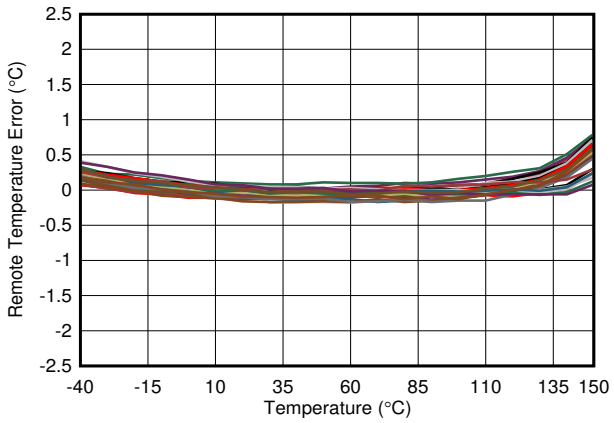


Figure 5-29. Remote Temperature Sensor Error vs Temperature

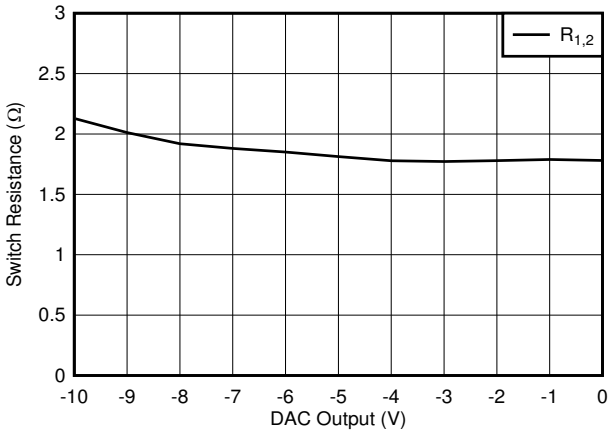


Figure 5-30. $R_{1,2}$ Switch Resistance vs DAC Output

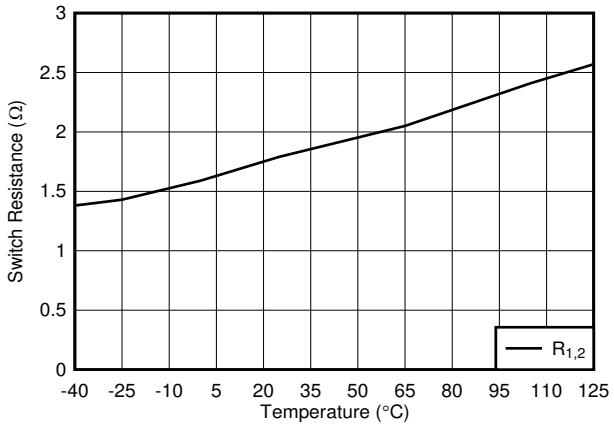


Figure 5-31. $R_{1,2}$ Switch Resistance vs Temperature

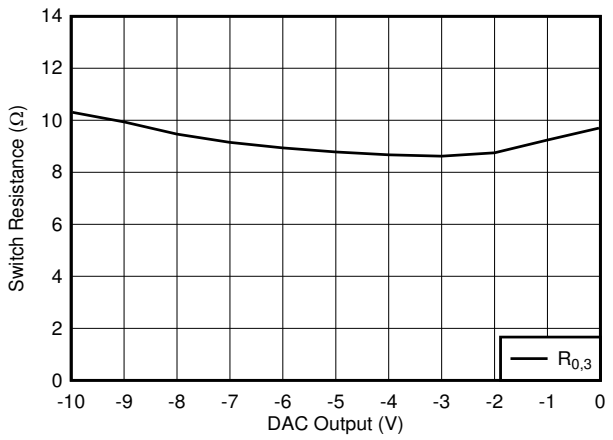


Figure 5-32. $R_{0,3}$ Switch Resistance vs DAC Output

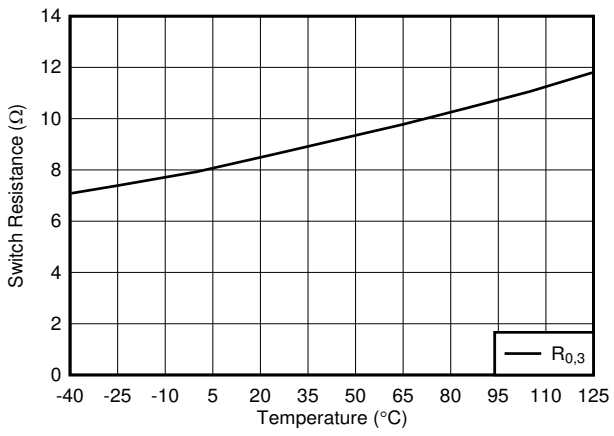


Figure 5-33. $R_{0,3}$ Switch Resistance vs Temperature

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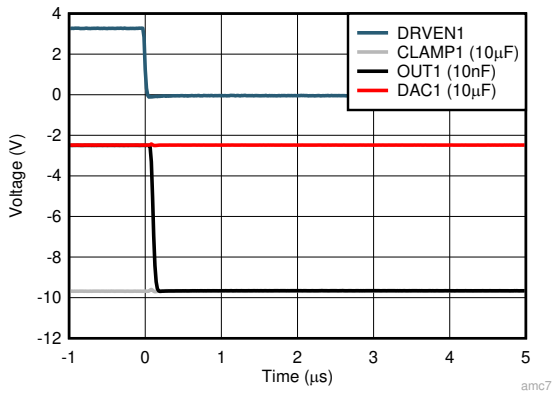
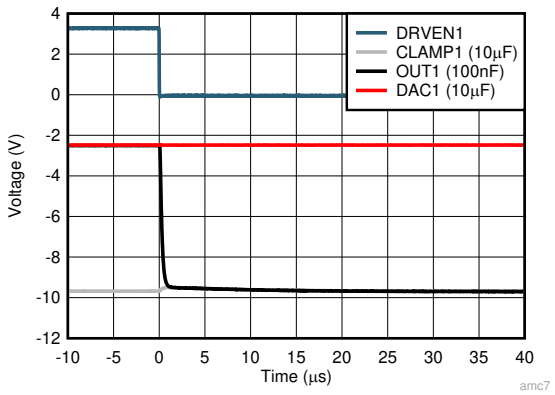
5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)



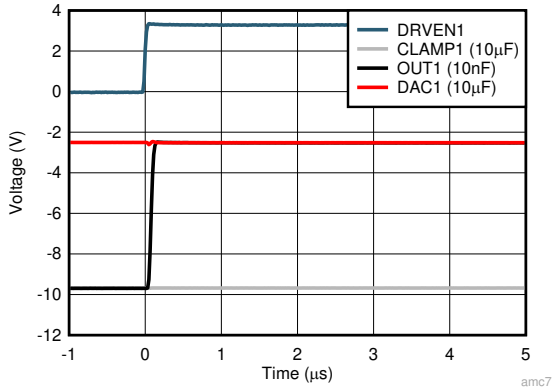
DAC output: –2.5V C_L = 10nF
CLAMP output: –9.6875V

Figure 5-34. OUT Pin: DAC to CLAMP Switch Response



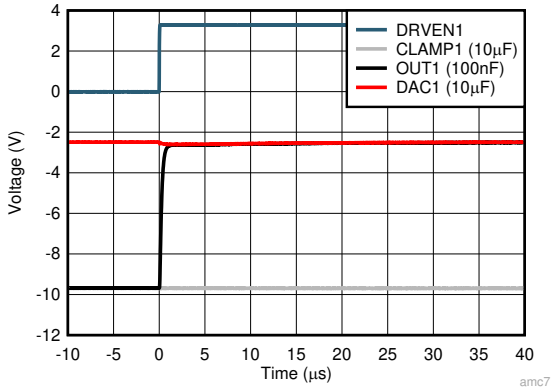
DAC output: –2.5V C_L = 100nF
CLAMP output: –9.6875V

Figure 5-35. OUT Pin: DAC to CLAMP Switch Response



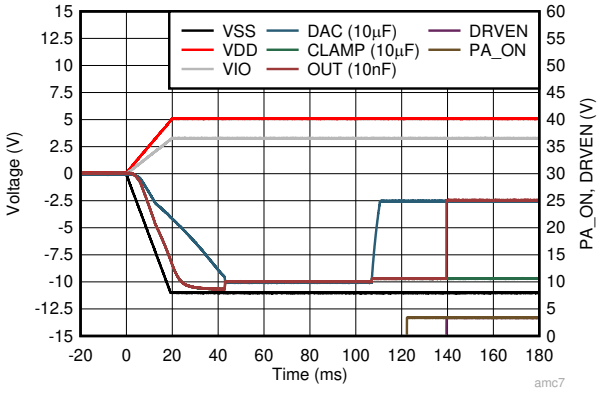
DAC output: –2.5V C_L = 10nF
CLAMP output: –9.6875V

Figure 5-36. OUT Pin: CLAMP to DAC Switch Response



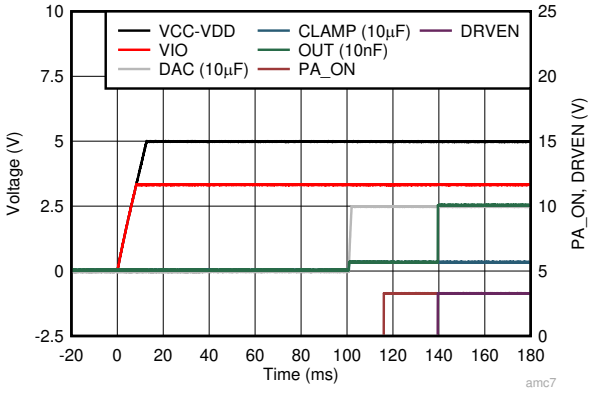
DAC output: –2.5V C_L = 100nF
CLAMP output: –9.6875V

Figure 5-37. OUT Pin: CLAMP to DAC Switch Response



DAC output: –2.5V
CLAMP output: –9.6875V

Figure 5-38. Negative Output Range Start-Up Sequence

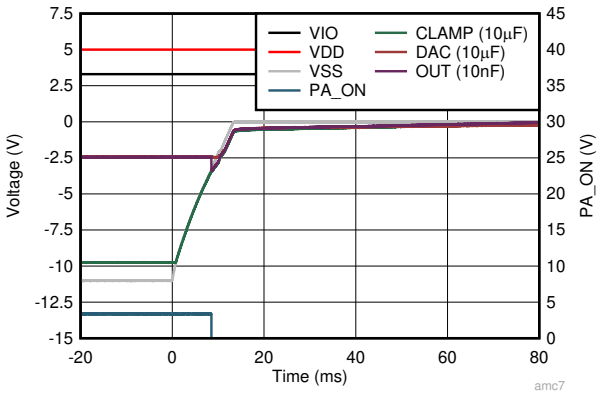


DAC output: 2.5V V_{CC} = V_{DD} = 5V
CLAMP output: 0.3125V

Figure 5-39. Positive Output Range Start-Up Sequence

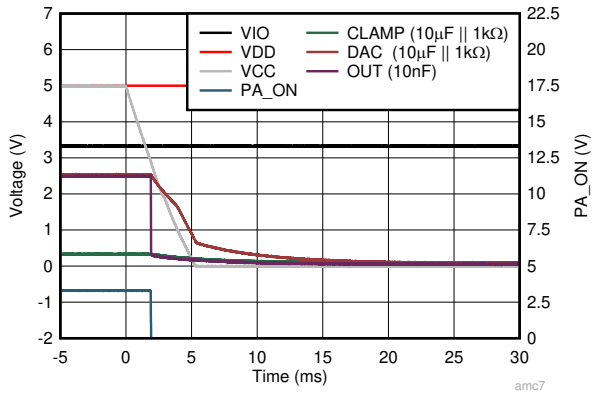
5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)



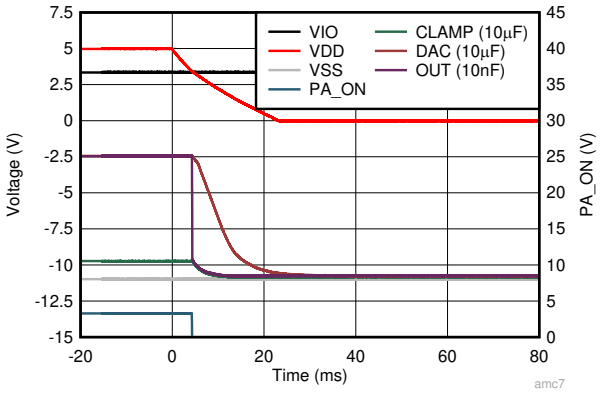
DAC output: –2.5V
CLAMP output: –9.6875V

Figure 5-40. V_{SS} Supply Collapse Response



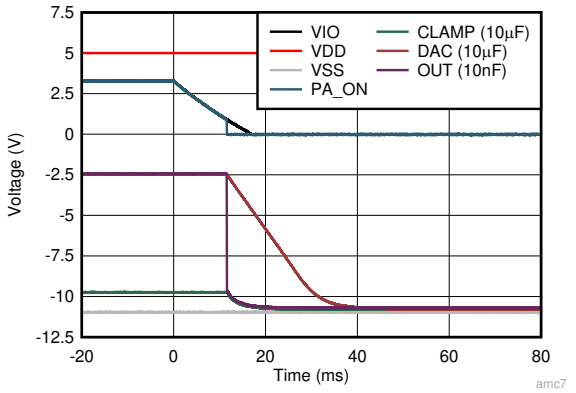
DAC output: 2.5V V_{CC} = V_{DD} = 5V
CLAMP output: 0.3125V

Figure 5-41. V_{CC} Supply Collapse Response



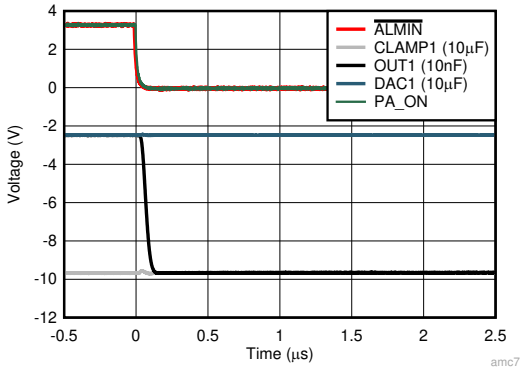
DAC output: –2.5V
CLAMP output: –9.6875V

Figure 5-42. V_{DD} Supply Collapse Response



DAC output: –2.5V
CLAMP output: –9.6875V

Figure 5-43. V_{IO} Supply Collapse Response



DAC output: –2.5V
CLAMP output: –9.6875V

Figure 5-44. $\overline{\text{ALMIN}}$ Alarm Event Response

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6 Detailed Description

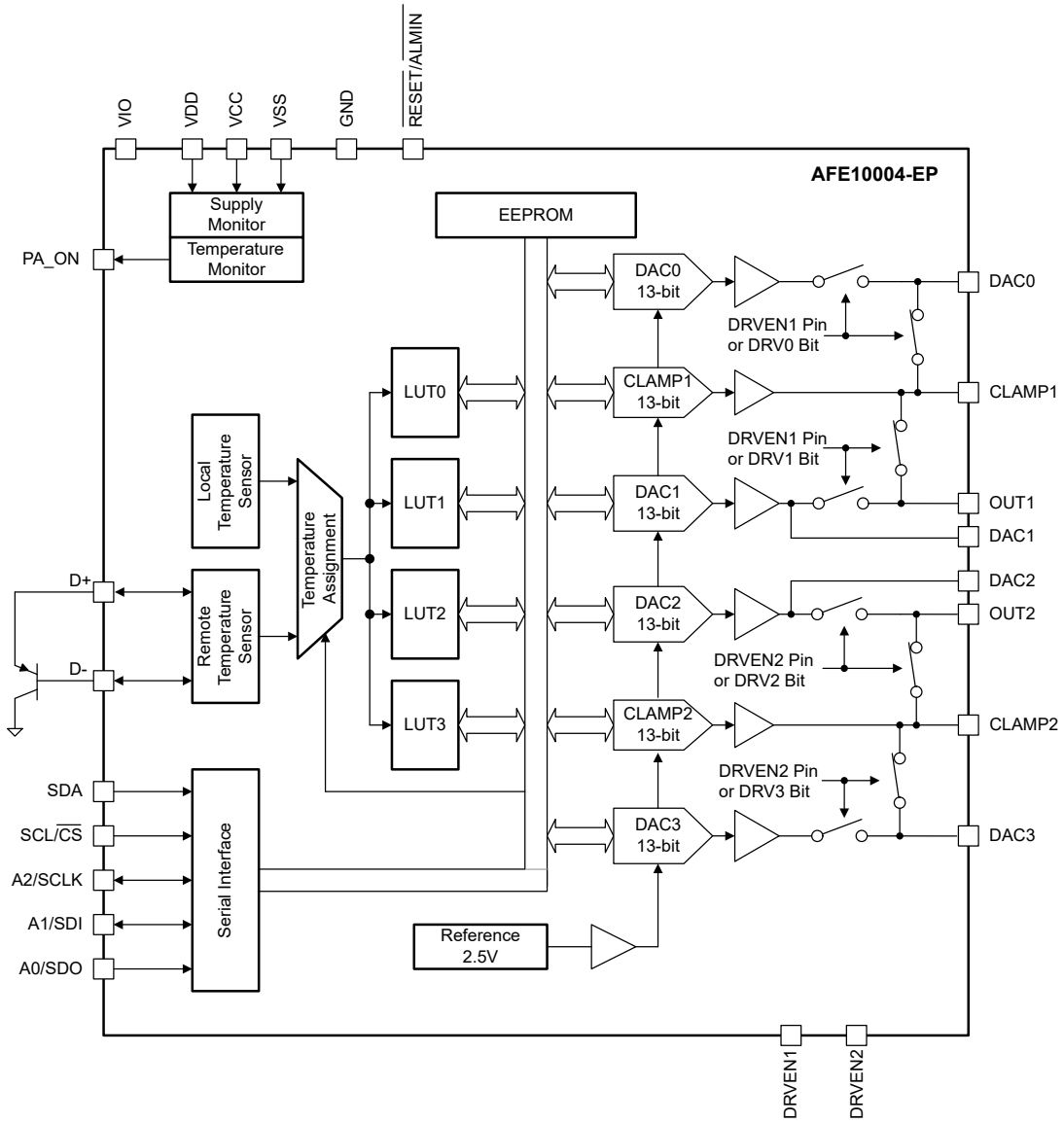
6.1 Overview

The AFE10004-EP is a four-channel power amplifier (PA) precision analog front end (AFE) with dedicated gate bias switch control and built-in sequencing features. The temperature-to-voltage transfer functions are user defined and stored in the internal EEPROM. The device contains both local and remote temperature sensor monitors that address four independently programmed look-up-tables (LUTs). The outputs of the LUTs are sent to the respective DACs to produce four independent output voltages. The device operates in either a positive or negative output voltage range.

The four gate bias outputs are switched on and off through digital control pins or software. The device enables programmable off voltages through two dedicated DACs. The gate bias switching is designed for fast response, and in combination with the device PA_ON pin enables a robust PA control system.

The device registers are configured through an SPI- and I^2C-compatible interface. The serial interface is also used to commit the device configuration and LUTs to the nonvolatile EEPROM. With the EEPROM properly configured, the device is able to operate autonomously.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Digital-to-Analog Converter (DAC) Overview

The device features four analog control channels. Each control channel is centered on a DAC that operates from the device internal reference. Two additional dedicated DACs are used for setting the internal switches off voltages. The six DACs in the device consist of a 13-bit string DAC and an output voltage buffer. Figure 6-1 shows a block diagram of the DAC architecture.

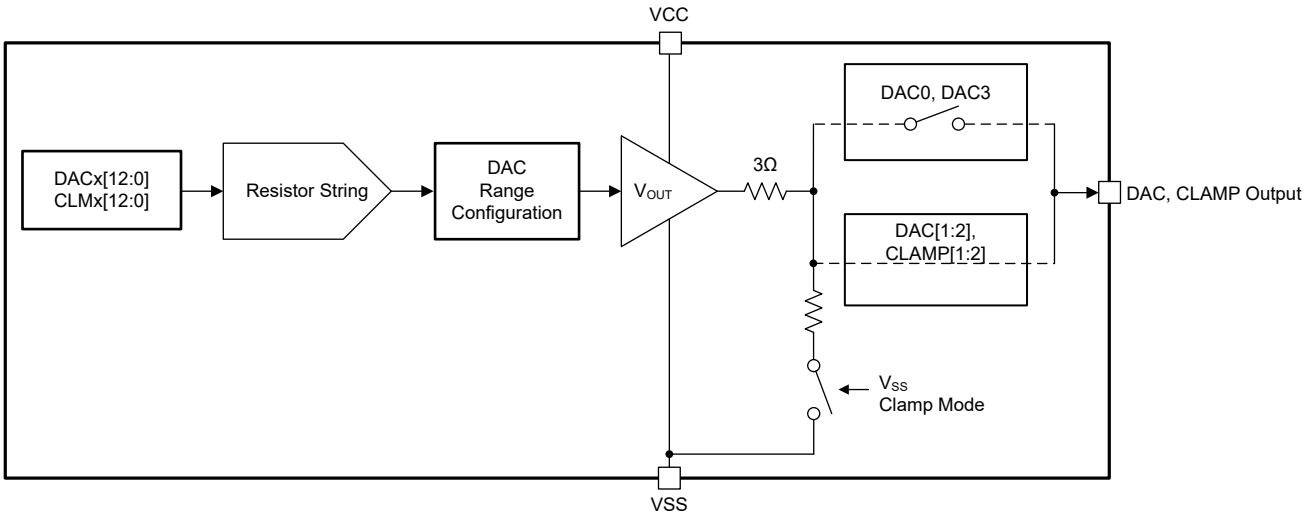


Figure 6-1. DAC Block Diagram

The DACs can be configured for positive- or negative-output-range operation with identical voltage resolution. All of the DACs in the device share the same output range. In positive-output-range operation, the full-scale range is 0V to 10V; however, the output voltage is limited by V_{CC} to a value no greater than 5.5V. In negative-output-range operation, the full-scale range is –10V to 0V. Data are written to the DAC data registers directly through the serial interface or automatically set by the look-up table (LUT) and arithmetic logic unit (ALU).

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6.3.1.1 DAC Resistor String

The resistor string structure consists of a series of resistors, each of value R, as shown in Figure 6-2. The code loaded to the DAC determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. This resistor string architecture has inherent monotonicity, voltage output, and low glitch.

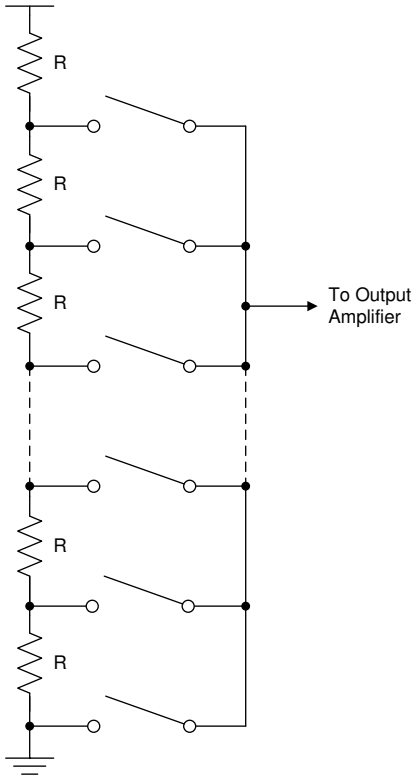

Figure 6-2. DAC Resistor String

6.3.1.2 DAC Register Structure

The DAC produces unipolar output voltages proportional to a 13-bit input data code. Input data are written to the DAC data register in straight binary format for both output ranges. The input data are either generated by the LUT and ALU or input directly through the serial interface.

Equation 1 gives the DAC transfer function.

$$V_{DAC} = \left(DACIN \; / \; 2^{13} \times 10V\right) + V_{MIN} \quad (1)$$

where:

- DACIN = the decimal equivalent of the binary code that is loaded to the DAC. DACIN range = 0 to $2^{13} – 1$.
- V_{MIN} = the lowest voltage for the selected DAC output range. Either 0V for a positive range or –10V for a negative range.

Section 6.3.4.3 describes the maximum output code span of the LUT for the given base value. The maximum slope of the transfer function stored in the LUT and the full temperature range define the maximum V_{DAC} output voltage excursion over temperature. When the DAC data are generated by the LUT and ALU, Equation 2 gives the maximum V_{DAC} output excursion over temperature.

$$dV_{DAC} = SLOPE_{MAX} \times T_{RANGE} \times V_{LSB} = 3.75LSB/℃ \times 200℃ \times \frac{10V}{2^{13}} = 916mV \quad (2)$$

However, this limitation is lifted when data are input directly to the DAC through the serial interface. In this case, the DAC input range is the full 8192 codes, and the DAC output spans the voltage ranges. Table 6-1 shows the DAC data format.

Table 6-1. DAC Data Format

DAC DATA REGISTER (1.22mV RESOLUTION)		NEGATIVE DAC OUTPUT VOLTAGE (V) V_{SS} = –11V, V_{CC} = GROUND	POSITIVE DAC OUTPUT VOLTAGE (V) V_{CC} = 5.5V, V_{SS} = GROUND
BINARY	HEX		
0 0000 0000 0000	0000	–10	0
0 0000 0000 0001	0001	–9.99878	0.00122
1 0000 0000 0000	1000	–5	5
1 0001 1001 1001	1199	–4.50073	5.49927
1 0001 1001 1010	119A	–4.49951	5.5
1 0001 1001 1011	119B	–4.49829	5.5
1 1111 1111 1110	1FFE	–0.00244	5.5
1 1111 1111 1111	1FFF	–0.00122	5.5

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6.3.1.3 DAC Buffer Amplifier

The DAC output buffer amplifiers are capable of rail-to-rail operation. The amplifier outputs are available at the DAC[0:3] and CLAMP[1:2] output pins. The buffer amplifiers are biased from the dedicated supply rails: V_{CC} and V_{SS}. The maximum DAC output voltage range is limited by these supplies.

The output amplifier is designed to drive capacitive loads as high as 15µF without oscillation. The output buffers are able to source 100mA and sink 20mA. The device implements short-circuit protection for momentary output shorts to ground and either supply. The sink short-circuit current is 40mA. The source short-circuit current is configurable to either 120mA (high-current mode) or 70mA (normal-current mode).

The high output current of the device gives good slewing characteristics even with large capacitive loads. To estimate the positive and negative slew rates for large capacitive loads, divide the source and sink short-circuit current values by the capacitor.

After start-up, the DAC output range is set automatically by the voltage present in the VSS and VCC pins. The DAC buffer amplifiers are automatically configured for positive voltage operation when V_{SS} = 0V and 4.5V ≤ V_{CC} ≤ 5.5V. Alternatively, the amplifiers are configured for negative voltage operation when V_{CC} = 0V and 4.5V ≤ V_{SS} ≤ 11V.

The device continuously monitors the buffer amplifier supplies to provide proper operation. In negative voltage operation, the valid V_{SS} supply range is optimized through the VSSRANGE bit to distinguish between the wide V_{SS} configuration (–11V ≤ V_{SS} < –7V) and the narrow V_{SS} configuration (–7V ≤ V_{SS} ≤ –4.5V). The V_{SS} range selection allows the device to detect supply failure conditions faster. The valid supply range for the device is determined at start-up. Table 6-2 shows the valid supply matrix.

Table 6-2. Valid Supply Matrix

SUPPLY CONFIGURATION	SUPPLY	
	VCC	VSS
Invalid configuration	0V ≤ V_{CC} < 4.5V	–4.5V < V_{SS} ≤ 0V
V_{CC} configuration	4.5V ≤ V_{CC} ≤ 5.5V	V_{SS} = 0V
Invalid configuration	4.5V ≤ V_{CC} ≤ 5.5V	V_{SS} < 0V
Narrow V_{SS} configuration	V_{CC} = 0V	–7V ≤ V_{SS} ≤ –4.5V
Invalid configuration	V_{CC} > 0V	–7V ≤ V_{SS} ≤ –4.5V
Wide V_{SS} configuration	V_{CC} = 0V	–11V ≤ V_{SS} < –7V
Invalid configuration	V_{CC} > 0V	–11V ≤ V_{SS} < –7V

During operation, if V_{CC} or V_{SS} fall to less than the specified threshold value associated to the supply configuration, or V_{DD} drops to less than 4.5V, a reset event is generated and the DAC outputs enter the special V_{SS} clamp mode. In V_{SS} clamp mode, the DAC output pins are internally connected to the VSS pin.

The six DAC buffer amplifiers share the V_{CC} and V_{SS} supplies; therefore, all DACs are configured to the same output range.

6.3.2 Output Switch Overview

The device facilitates rapid turn on and turn off of the voltage at the device OUT[1:2] outputs. The OUT[1:2] outputs can be switched on or off by the DRVEN[1:2] inputs or alternatively through software. The *on* voltages are set by the DAC[1:2] outputs while the *off* voltages are set by the CLAMP[1:2] outputs. The OUT[1:2] pins are driven by DAC[1:2] when the corresponding switch control pin or bit is asserted high. Otherwise, the OUT[1:2] pins are driven by the dedicated CLAMP[1:2] DAC outputs.

Additionally, the DAC0 and DAC3 outputs include a simplified switch network that facilitates fast turnoff. Switch the DAC0 and DAC3 pins on or off through one of the DRVEN[1:2] pins or through software. The DAC0 and DAC3 output pins are driven by the DAC0 and DAC3 buffers when on, and by the CLAMP[1:2] outputs when off. While fast turnoff is possible as a result of the CLAMP[1:2] output pins, turn-on time is limited by the DAC0 and DAC3 buffer bandwidth. Figure 6-3 shows a typical switch application.

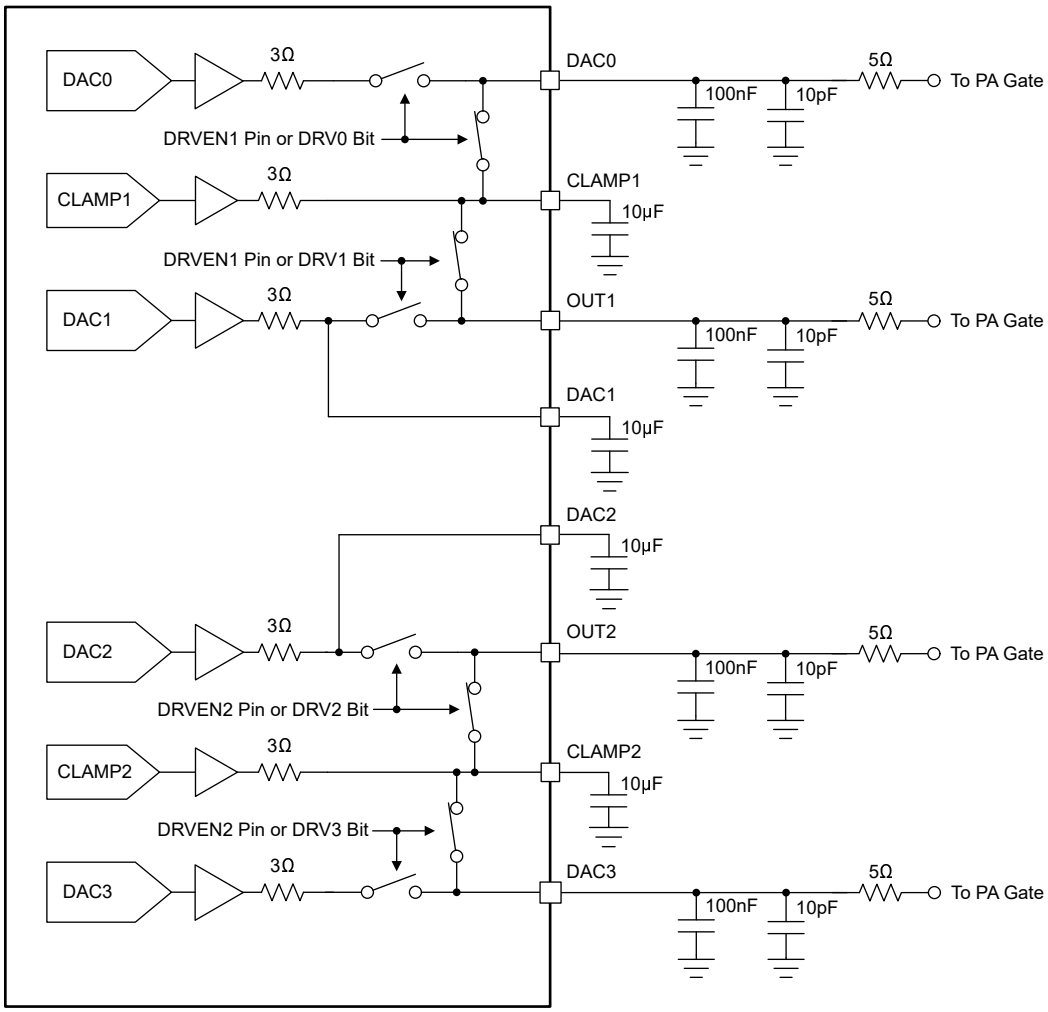

Figure 6-3. Typical Switch Application

The control and switch design is optimized for minimum delay between the DRVEN[1:2] input and the output pins voltage switching. The switches default to the off state at start-up or after an alarm event.

ADVANCE INFORMATION

6.3.3 Temperature Sensors

The device includes a remote temperature sensor monitor and a local temperature sensor. The device is configurable to continuously monitor both temperature inputs and use the conversion results as inputs to the four LUTs.

Remote temperature sensors are typically low-cost discrete NPN or PNP transistors, substrate thermal transistors, or diodes.

6.3.3.1 Temperature Data Format

The local and remote temperature sensors have a resolution of 12 bits (0.0625°C). Temperature data that result from conversions within the default measurement range are represented in binary form. Table 6-3 shows the temperature data format. Any temperatures greater than 127°C result in a value that rails to 127.9375 (7FFh). To set the device to measure over an extended temperature range, set the TMPRANGE bit. The change in measurement range and data format from standard binary to extended binary occurs at the next temperature conversion. For data captured in the extended temperature range configuration, an offset of 64 (40h) is added to the standard binary value; see the *Extended Binary* column of the table. This configuration allows measurement of temperatures as low as –64°C and as high as 191.9375°C, whereas most other remote temperature sensors operate within the range of only –55°C to +150°C. Additionally, although the local temperature sensor operates at junction temperatures ranging from –55°C to +150°C, the accuracy is specified only from –55°C to +125°C. Observe the parameter values listed in the *Absolute Maximum Ratings*.

Table 6-3. Temperature Data Format (High Byte)

TEMPERATURE (°C)	TEMPERATURE REGISTER HIGH BYTE VALUE (1°C RESOLUTION)			
	STANDARD BINARY(1)		EXTENDED BINARY(2)	
	BINARY	HEX	BINARY	HEX
–64	1100 0000	C0	0000 0000	00
–50	1100 1110	CE	0000 1110	0E
–25	1110 0111	E7	0010 0111	27
–1	1111 1111	FF	0011 1111	3F
0	0000 0000	00	0100 0000	40
1	0000 0001	01	0100 0001	41
10	0000 1010	0A	0100 1010	4A
25	0001 1001	19	0101 1001	59
50	0011 0010	32	0111 0010	72
75	0100 1011	4B	1000 1011	8B
100	0110 0100	64	1010 0100	A4
125	0111 1101	7D	1011 1101	BD
127	0111 1111	7F	1011 1111	BF
150	0111 1111	7F	1101 0110	D6
175	0111 1111	7F	1110 1111	EF
191	0111 1111	7F	1111 1111	FF

(1) Resolution is 1°C/count. Negative values are represented in 2's complement format.
(2) Resolution is 1°C/count. All values are unsigned with a –64°C offset.

Both local and remote temperature data use two bytes for data storage. The high byte stores the temperature with 1°C resolution. The second, or low, byte stores the decimal fraction value of the temperature and allows a higher measurement resolution. Table 6-4 shows the decimal fraction temperature data format. The measurement resolution for both the local and remote temperature sensors is 0.0625°C.

Table 6-4. Decimal Fraction Temperature Data Format (Low Byte)

TEMPERATURE (°C)	TEMPERATURE REGISTER LOW BYTE VALUE (0.0625°C RESOLUTION)(1)	
	STANDARD AND EXTENDED BINARY	HEX
0	0000 0000	00
0.0625	0001 0000	10
0.1250	0010 0000	20
0.1875	0011 0000	30
0.2500	0100 0000	40
0.3125	0101 0000	50
0.3750	0110 0000	60
0.4375	0111 0000	70
0.5000	1000 0000	80
0.5625	1001 0000	90
0.6250	1010 0000	A0
0.6875	1011 0000	B0
0.7500	1100 0000	C0
0.8125	1101 0000	D0
0.8750	1110 0000	E0
0.9375	1111 0000	F0

(1) Resolution is 0.0625°C/count. All possible values are shown.

6.3.3.1.1 Standard Binary-to-Decimal Temperature Data Calculation Example

High-byte conversion (for example, 0111 0011):

- Convert the right-justified binary high byte to hexadecimal.
- From hexadecimal, multiply the first number by $16^0 = 1$ and the second number by $16^1 = 16$.
- The sum equals the decimal equivalent: 0111 0011b → 73h → $(3 \times 16^0) + (7 \times 16^1) = 115$

Low-byte conversion (for example, 0111 0000):

- To convert the left-justified binary low-byte to decimal, use bits 7 through 4 and ignore bits 3 through 0 because these bits do not affect the value of the number.
- 0111b → $(0 \times 1/2)^1 + (1 \times 1/2)^2 + (1 \times 1/2)^3 + (1 \times 1/2)^4 = 0.4375$

6.3.3.1.2 Standard Decimal-to-Binary Temperature Data Calculation Example

For positive temperatures (for example, 20°C):

- (20°C) / (1°C/count) = 20 → 14h → 0001 0100
- Convert the number to binary code with 8-bit, right-justified format, and MSB = 0 to denote a positive sign.
- 20°C is stored as 0001 0100 → 14h.

For negative temperatures (for example, –20°C):

- (|–20|) / (1°C/count) = 20 → 14h → 0001 0100
- Generate the 2's complement of a negative number by complementing the absolute value binary number and adding 1.
- –20°C is stored as 1110 1100 → ECh.

ADVANCE INFORMATION

6.3.3.2 Temperature Sensor Conversion Rate

The temperature sensor conversion rate setting controls the rate at which temperature conversions are performed. The conversion rate adjusts the idle time between conversions but does not adjust the conversion time. Table 6-5 lists the conversion rate options and corresponding time between conversions. The default value of the register is 08h, which gives a default rate of 16 conversions per second.

Table 6-5. Temperature Sensor Conversion Rate

VALUE	CONVERSIONS PER SECOND	TIME (SECONDS)
00h	0.0625	16
01h	0.125	8
02h	0.25	4
03h	0.5	2
04h	1	1
05h	2	0.5
06h	4	0.25
07h	8	0.125
08h	16 (default)	0.0625 (default)
09h	32	0.03125

6.3.3.3 Remote Temperature Sensor

The device includes a remote temperature-measurement channel. Remote temperature sensors are typically low-cost discrete NPN or PNP transistors, substrate thermal transistors, or diodes. Use either NPN or PNP transistors, as long as the base-emitter junction is used as the remote temperature sense. Use diode-connected NPN transistors. Use either transistor- or diode-connected PNP transistors. Figure 6-4 shows the remote temperature sensor connection. Advanced features, such as series resistance cancellation, programmable nonideality factor (η-factor), and a programmable offset, are combined to provide a robust thermal monitoring device with improved accuracy and noise immunity.

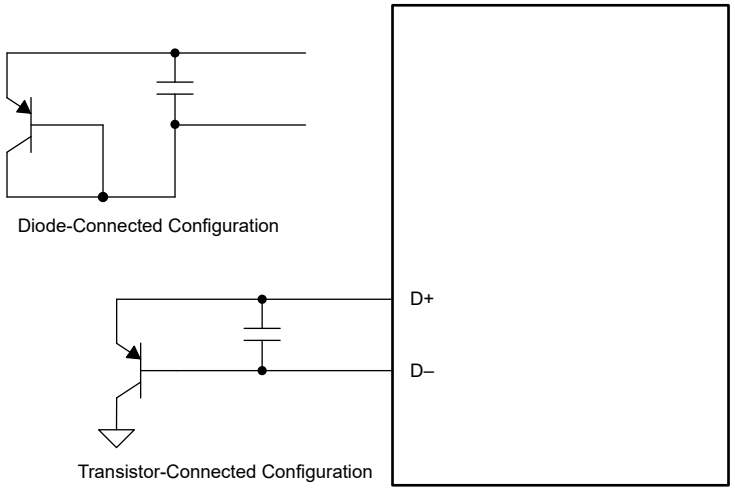

Figure 6-4. Remote Temperature Sensor Connection

6.3.3.3.1 Series Resistance Cancellation

Series resistance cancellation automatically eliminates the temperature error caused by the resistance of the routing to the remote transistor, or by the resistors of the optional external low-pass filter. The device is able to cancel a total of up to 1kΩ of series resistance, thus eliminating the need for additional characterization and temperature offset correction.

6.3.3.3.2 Differential Input Capacitance

The device tolerates differential input capacitance of up to 1000pF with minimal change in temperature error.

6.3.3.3.3 Filtering

Remote junction temperature sensors are typically implemented in a noisy environment. Noise is most often created by fast digital signals that can corrupt measurements. The device has a built-in, 65kHz filter on the D+ and D– inputs to minimize the effects of noise. However, to make the application more robust against unwanted coupled signals, place a bypass capacitor differentially across the inputs of the remote temperature sensor. For this capacitor, select a value between 100pF differential and 1nF. Some applications attain better overall accuracy with additional series resistance; however, this increased accuracy is application specific. When series resistance is added, do not let the total value exceed 1kΩ. If filtering is required, suggested component values are 100pF differential and 50Ω on each input; exact values are application specific.

Additionally, a digital filter is available for the remote temperature measurements to further reduce the effect of noise. This filter is programmable and has two levels when enabled. Level 1 performs a moving average of four consecutive samples. Level 2 performs a moving average of eight consecutive samples. The value stored in the remote temperature result register is the output of the digital filter, and is the value being monitored for alarm conditions. The digital filter provides additional immunity to noise and spikes on the thermal alarm outputs. To enable or disable the filter, program the desired levels in the digital filter register. Figure 6-5 and Figure 6-6 show the filter response to impulse and step inputs. The digital filter is disabled by default.

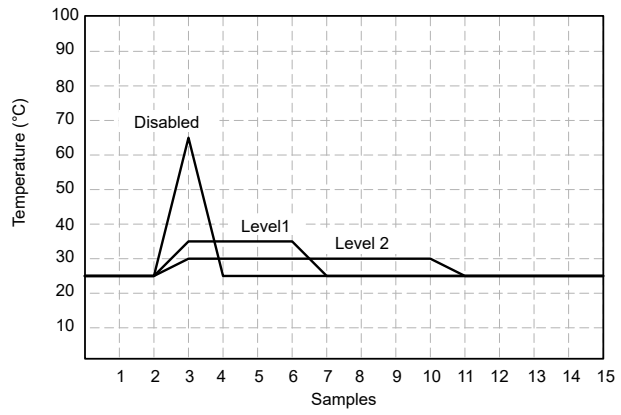

Figure 6-5. Filter Response to Impulse Inputs

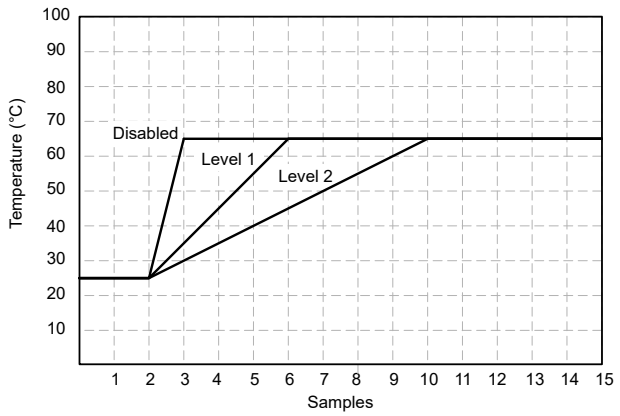

Figure 6-6. Filter Response to Step Inputs

6.3.3.3.4 Sensor Fault

The device senses a fault at the D+ input resulting from an incorrect diode connection. The device also senses an open circuit. Short-circuit conditions return a value of –64°C. The detection circuitry consists of a voltage comparator that trips when the voltage at D+ exceeds V_{DD} – 0.3V (typical). The comparator output is continuously checked during a conversion. If a fault is detected, the OPEN bit in the status register is set and the device issues an alarm event.

When not using the remote sensor in the device, the D+ and D– inputs must be connected together to prevent meaningless fault warnings.

ADVANCE INFORMATION

6.3.3.3.5 η-Factor Correction

The device allows for a different η-factor value to be used for converting remote channel measurements to temperature. The remote channel uses sequential current excitation to extract a differential V_{BE} voltage measurement to determine the temperature of the remote transistor. Equation 3 shows this voltage and temperature.

$$V_{BE2} - V_{BE1} = \frac{\eta k T}{q} \ln\left(\frac{I_2}{I_1}\right) \quad (3)$$

The value η in Equation 3 is a characteristic of the particular transistor used for the remote channel. The default value used by the device is η = 1.008. The value in the η-factor correction register can be used to adjust the effective η-factor according to Equation 4 and Equation 5.

$$\eta_{eff} = \left(\frac{1.008 \times 2088}{2088 + N_{ADJUST}}\right) \quad (4)$$

$$N_{ADJUST} = \left(\frac{1.008 \times 2088}{\eta_{eff}}\right) - 2088 \quad (5)$$

The η-factor correction value must be stored in 2's complement format, yielding an effective data range from –128 to +127. The register reset value is 00h, and has no effect unless a different value is written to the register. The resolution of the η-factor register is 0.000483. Table 6-6 shows the η-factor range.

Table 6-6. η-Factor Range

N_{ADJUST}			η
BINARY	HEX	DECIMAL	
0111 1111	7F	127	0.950205
0000 1010	0A	10	1.003195
0000 1000	08	8	1.004153
0000 0110	06	6	1.005112
0000 0100	04	4	1.006073
0000 0010	02	2	1.007035
0000 0001	01	1	1.007517
0000 0000	00	0	1.008
1111 1111	FF	–1	1.008483
1111 1110	FE	–2	1.008966
1111 1100	FC	–4	1.009935
1111 1010	FA	–6	1.010905
1111 1000	F8	–8	1.011877
1111 0110	F6	–10	1.012851
1000 0000	80	–128	1.073829

6.3.3.3.6 Remote Temperature Offset Register

The offset register allows the device to store any system offset compensation value that can result from precision calibration. The value in the register is stored in the same format as the temperature result, and is added to the remote temperature result upon every conversion. Combined with the η-factor correction, this function allows for very accurate system calibration over the entire temperature range.

6.3.3.4 Temperature Sensor Alarm Functions

The device continuously monitors the state of the temperature analog-to-digital converter (ADC), the temperature limit comparators, and the connection to the remote sensor. The results are reported through the status register. If any of these five alarm conditions trigger, the TMPSTAT bit is set, and the device generates an alarm event. Table 6-7 shows the temperature status bits.

Table 6-7. Temperature Status

BIT	DESCRIPTION
BUSY	Temperature ADC status
LHIGH	Local temperature high-limit alarm
LLOW	Local temperature low-limit alarm
RHIGH	Remote temperature high-limit alarm
RLOW	Remote temperature low-limit alarm
OPEN	Remote sensor open circuit alarm

Reading the temperature status register clears the five flags, as long as the condition that caused the setting of the flags is not present anymore (that is, the value of the corresponding result register is within the limits, or the remote sensor is connected properly and functional).

Figure 6-7 shows how the temperature sensor handles overtemperature and undertemperature alarms according to the ALERT/THERM configuration mode.

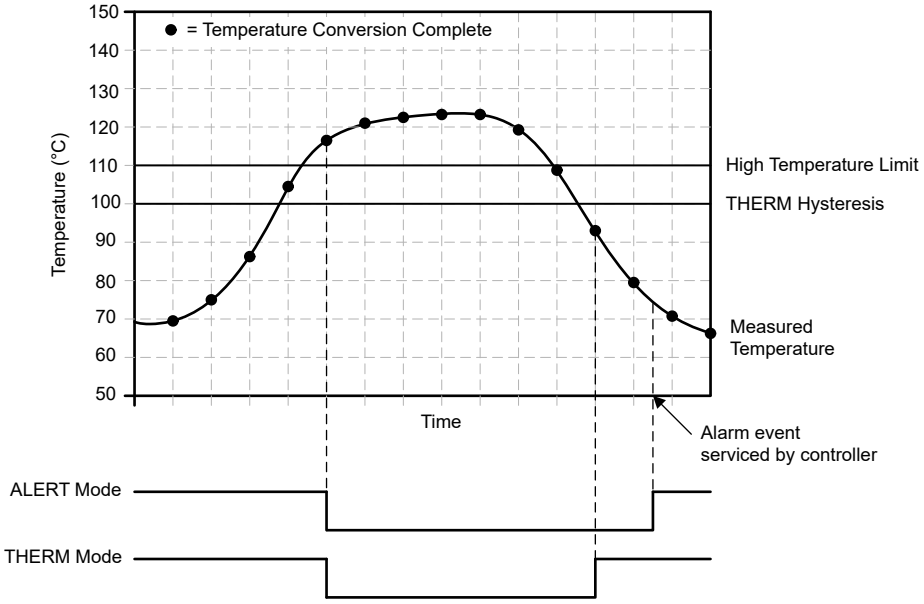

Figure 6-7. ALERT and THERM Temperature Alarm Operation

A high alarm is set when the temperature exceeds the high limit in both ALERT and THERM modes. A low alarm is set when the temperature drops to less than the low limit in ALERT mode only.

When configured in ALERT mode, the consecutive alert setting (CONAL[2:0]) determines the number of limit violations before an alarm event is generated.

When configured in THERM mode, only the high limits are monitored. The THERM hysteresis register allows hysteresis to be added so that the high flag resets when the temperature returns to or drops to less than the limit value minus the hysteresis value.

ADVANCE INFORMATION

6.3.4 Look-Up Table (LUT) and Arithmetic-Logic Unit (ALU)

Four independent LUTs are used to create arbitrary transfer functions that map temperature to the DAC[0:3] analog outputs of the device. In concept, temperature is used as a pointer to a table of discrete values that are representative of the samples of the desired temperature-dependent function.

To minimize storage requirements, the device LUTs are indexed in 4°C increments. Also, the stored values are only the increments, or first derivatives (Δ), of the modeled transfer function. The internal ALU reconstructs the original transfer function by integrating the coefficients stored in the LUTs. The errors caused by the coarseness of the temperature quantization are significantly reduced through the use of linear interpolation, which is also implemented in the ALU.

Consider the example in Figure 6-8. The top graph shows the target output versus temperature. V_{DACx} is a smooth, monotonic function with ideally infinite precision. The LUT stores only the increments, or the rise, within each 4°C interval.

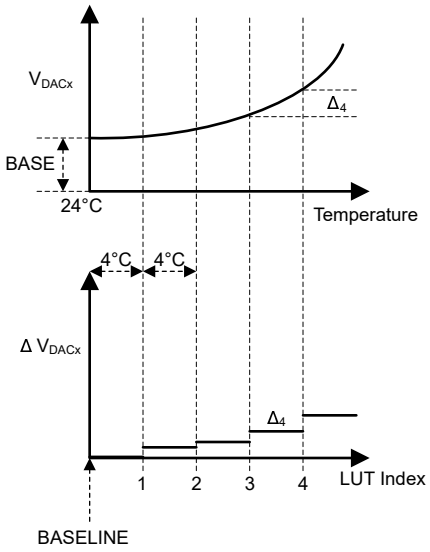

Figure 6-8. Transfer Function

To recreate the original transfer function, the series of increments must be summed together and added to the constant BASE value. BASE represents the constant offset that is lost as a result of differentiation; that is, the storage of the increments only. This process must also be referenced to the common temperature point. This reference temperature is referred to as the BASELINE, and is fixed to 24°C.

ADVANCE INFORMATION

6.3.4.1 LUT and ALU Organization

In the following figure, the TEMP column represents the temperature value to the LUT. This value is produced by either the local temperature sensor, the remote temperature sensor, or provided directly by the user.

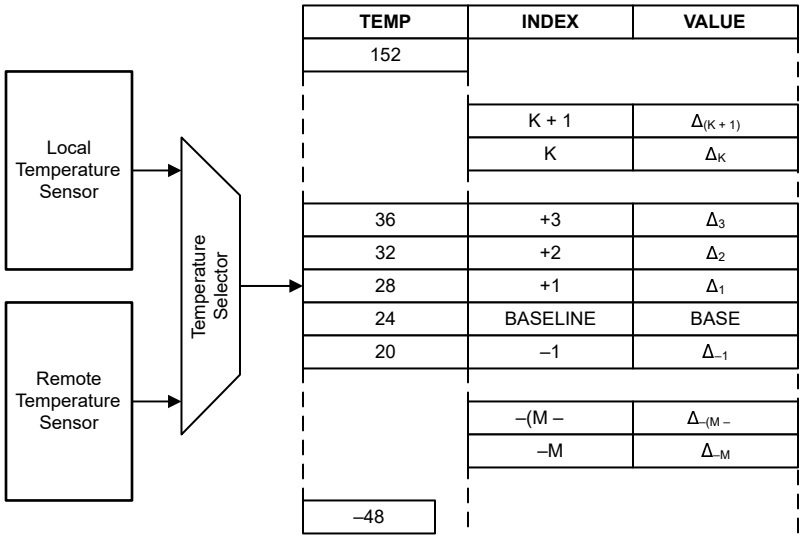

Figure 6-9. LUT Organization

TEMP is truncated to a resolution of 4°C/LSB to index the LUT. The overall transfer function is stored in the LUT as a set of unsigned 4-bit increments from the BASE value; that is, LUT location (+1) stores the value of the increment Δ_1. The baseline is set to 24°C and BASE is the numeric representation of the required output at the BASELINE temperature.

When TEMP exceeds the BASELINE temperature, the LUT is addressed greater than the BASELINE address, and all increments are added to the BASE value to produce DACIN, a numeric equivalent of the analog output. When TEMP is less than the BASELINE temperature, LUT is addressed less than the BASELINE, and all increments are subtracted from the BASE value.

The interpolation function is implemented in the ALU that follows the LUT. The truncated lower bits of the TEMP value, REM = TEMP[5:0], are used to interpolate between data points stored in the LUT. A portion of increment, $\alpha\Delta i$, is added to form the final input data to the DAC. The factor α is a fraction of 4°C temperature span, or equivalently a fraction of the 64-code temperature span, that is α = REM/64.

ADVANCE INFORMATION

Figure 6-10 depicts the process of calculating DACIN, including the interpolation. DACIN is the final 13-bit value produced by the ALU and the LUT, and forwarded to the DAC for conversion to analog domain.

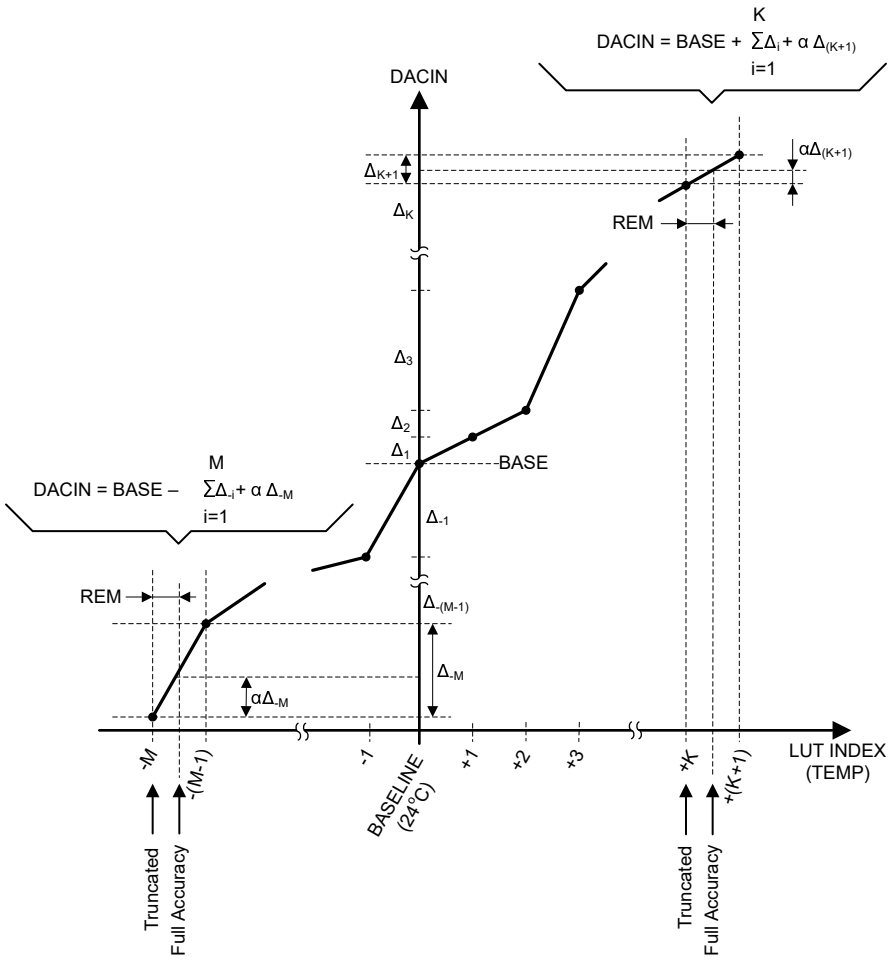

Figure 6-10. DACIN Calculation

Up to this point, the algorithm description referred only to the generation of a monotonically increasing transfer function. The device also produces a monotonically decreasing transfer function by setting the LUT polarity bit.

Figure 6-11 shows the effect of polarity reversal on the overall transfer function. The LUT content is unchanged from the original example in Figure 6-9. Notice that now, the LUT values stored at locations greater than the BASELINE address are subtracted from BASE value, and the LUT values stored at locations less than the BASELINE address are added to the BASE value.

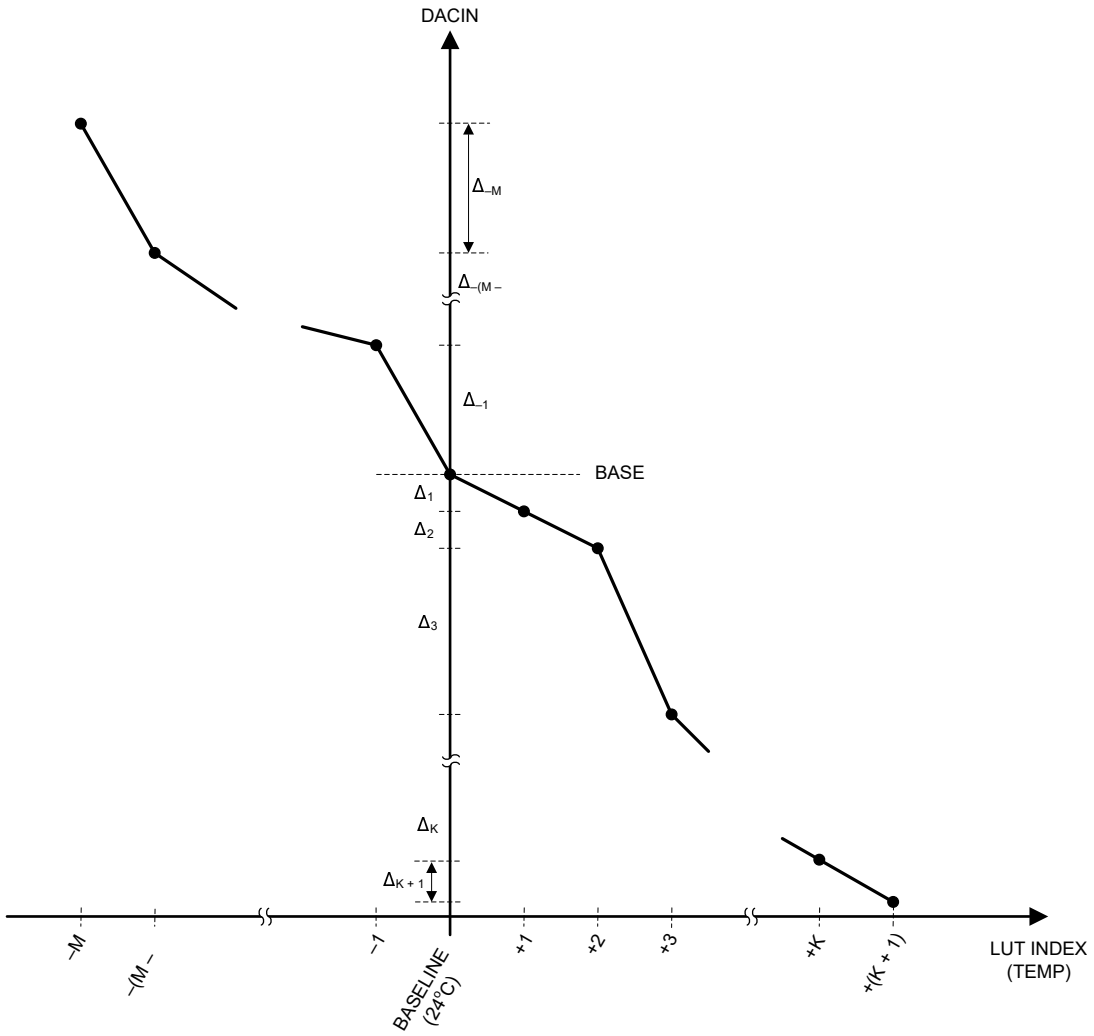

Figure 6-11. Monotonically Decreasing Transfer Function

Equation 6 and Equation 7 summarize the expressions used in the calculation of the transfer function:

LUT index > BASELINE:

$$\mathrm{DACIN} = \mathrm{BASE} + (-1)^{\mathrm{POL}}\left(\sum_{i=1}^{K} \Delta_i + \alpha\,\Delta_{(K+1)}\right) \quad (6)$$

LUT index < BASELINE:

$$\mathrm{DACIN} = \mathrm{BASE} - (-1)^{\mathrm{POL}}\left(\sum_{i=1}^{M} \Delta_{-i} - \alpha\,\Delta_{-M}\right) \quad (7)$$

ADVANCE INFORMATION

6.3.4.2 LUT Coefficient to Register Mapping

The preceding sections referred to LUT coefficients as Δ_K. These coefficients are stored in the DELTA registers. Table 6-8 shows the mapping of the Δ_K coefficients to the DELTA registers.

Table 6-8. Δ_K to DELTA Register Mapping

TEMPERATURE	FUNCTION INCREMENT	REGISTER ASSIGNMENT
–48°C	Δ_{-18}	DELTAn48
↓	↓	↓
–28°C	Δ_{-13}	DELTAn28
↓	↓	↓
20°C	Δ_{-1}	DELTAp20
28°C	Δ_{+1}	DELTAp28
↓	↓	↓
128°C	Δ_{+26}	DELTAp128
↓	↓	↓
152°C	Δ_{+32}	DELTAp152

6.3.4.3 LUT Input and Output Ranges

The LUT input range spans temperatures –48°C to +152°C. For temperatures outside this range, the LUT output is linearly extrapolated. Figure 6-12 illustrates the extrapolated LUT output to a remote temperature sensor reading of –55°C.

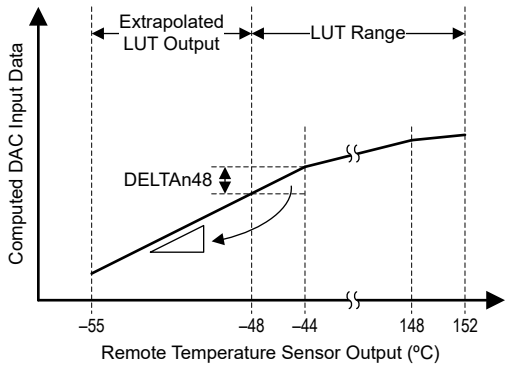

Figure 6-12. Remote Temperature Sensor Output

The increments stored in the LUT are 4-bit unsigned values. This limits the maximum slope of the transfer function stored in the LUT to:

$$\text{SLOPE}_{\text{MAX}} = \frac{15\text{LSB}}{4℃} = 3.75\text{LSB}/℃ \quad (8)$$

Given the slope limit imposed by the LUT structure, and the LUT input range of 200°C (from –48°C to +152°C), the maximum output range of the LUT corresponding to the temperature sensor input is 750LSBs for the given BASE value.

The maximum code span can reside anywhere within the code space for the 13-bit DAC inputs. The total input code to the DAC is the sum of the increments (Δs) and the 13-bit BASE value.

6.3.5 Memory

The internal memory of the device consists of two distinct areas: a user register set or operating memory and a EEPROM (nonvolatile storage) that enables autonomous device operation.

The operating memory, but not the EEPROM, is directly accessible through the serial interface. The EEPROM acquires data through transfer from the operating memory when issued a serial command.

6.3.5.1 Operating Memory Page Storage

The operating memory space provides control over the device functionality, reports internal status of the device, and stores the signal path data. A section of the operating memory, designated as the *Notepad* is available for arbitrary data storage.

Figure 6-13 shows the operating memory consists of individually accessible register pages. The default page at start-up is Page 1. Address 0x7E is used to address the different pages in the device. To read and write to one of the device registers, first select the page for that register. The page register holds the page value until a new page is programmed to the device.

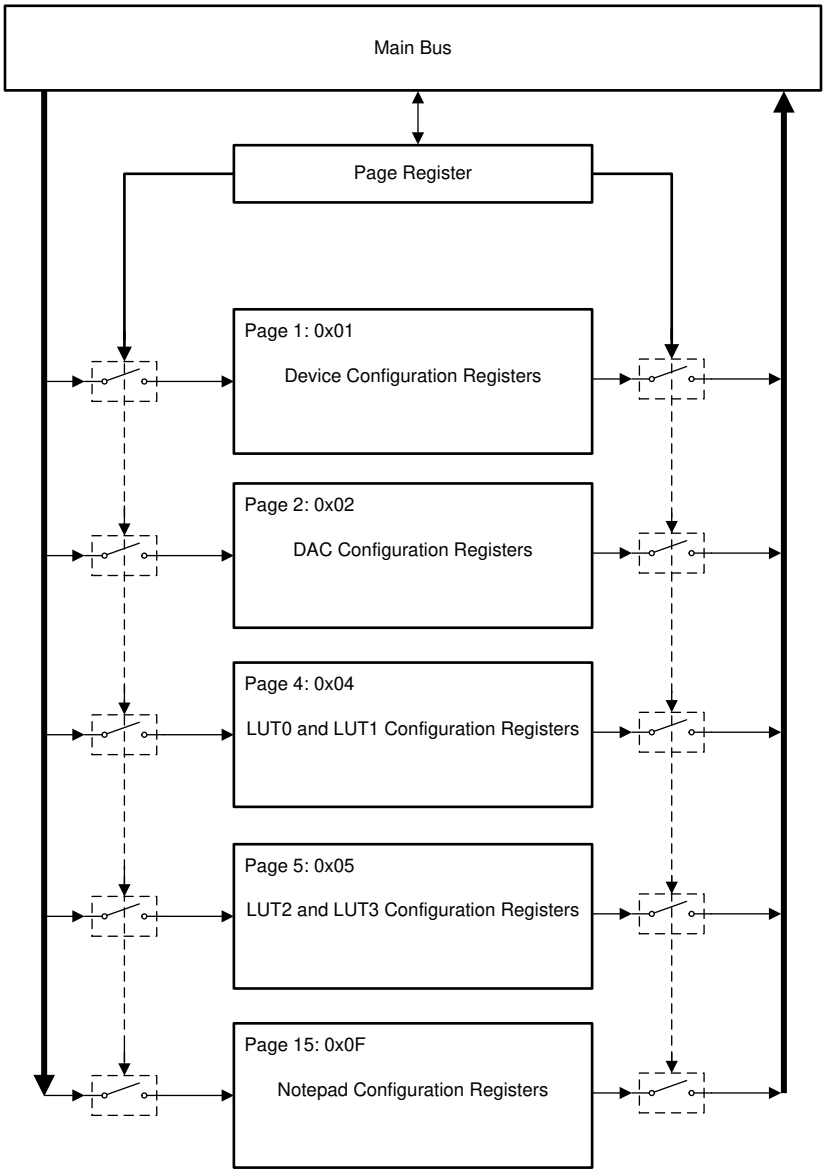

Figure 6-13. Operating Memory Page System

6.3.5.2 EEPROM Storage

The device offers the option to store the device configuration (Page 1), CLAMP overwrite values (Page 2), LUT values (Pages 4 and 5) and the Notepad (Page 15) in the EEPROM (see Figure 6-14). The move of data from the operating memory to the EEPROM (burn) is initiated by writing the program code, 0xE4, to the EEPROM burn register in Page 15.

Note

Ensure that the LUT is disabled before accessing the EEPROM.

A EEPROM burn sequence requires Pages 4, 5, and 15 to be configured before Pages 1 and 2. After the registers in all pages have been configured, initiate an EEPROM burn command by issuing the programming code. The EEPROM burn sequence takes approximately 130ms to complete. The EERDY bit provides the EEPROM burn status.

Note

Avoid reset events during the EEPROM burn sequence because of unpredictable results.

Upon start-up, the device automatically executes a EEPROM data load to the operating memory. An EEPROM load sequence takes approximately 5ms to complete.

To return all registers in the device to factory-default settings after an EEPROM load, write the register clear code (0xAD) to the software reset register. A register clear sequence takes approximately 15µs to complete. Table 6-9 summarizes both EEPROM access operations.

Table 6-9. EEPROM Access

EEPROM ACCESS	SERIAL INTERFACE OPERATION	PAGE	REGISTER	DATA	COMMENT
LOAD	N/A	N/A	N/A	N/A	Transfer of data from the EEPROM to the operating memory is done automatically after a reset event.
BURN	WRITE	15	EEPROM Burn register	0xE4	Transfer of data from the operating memory to the EEPROM.

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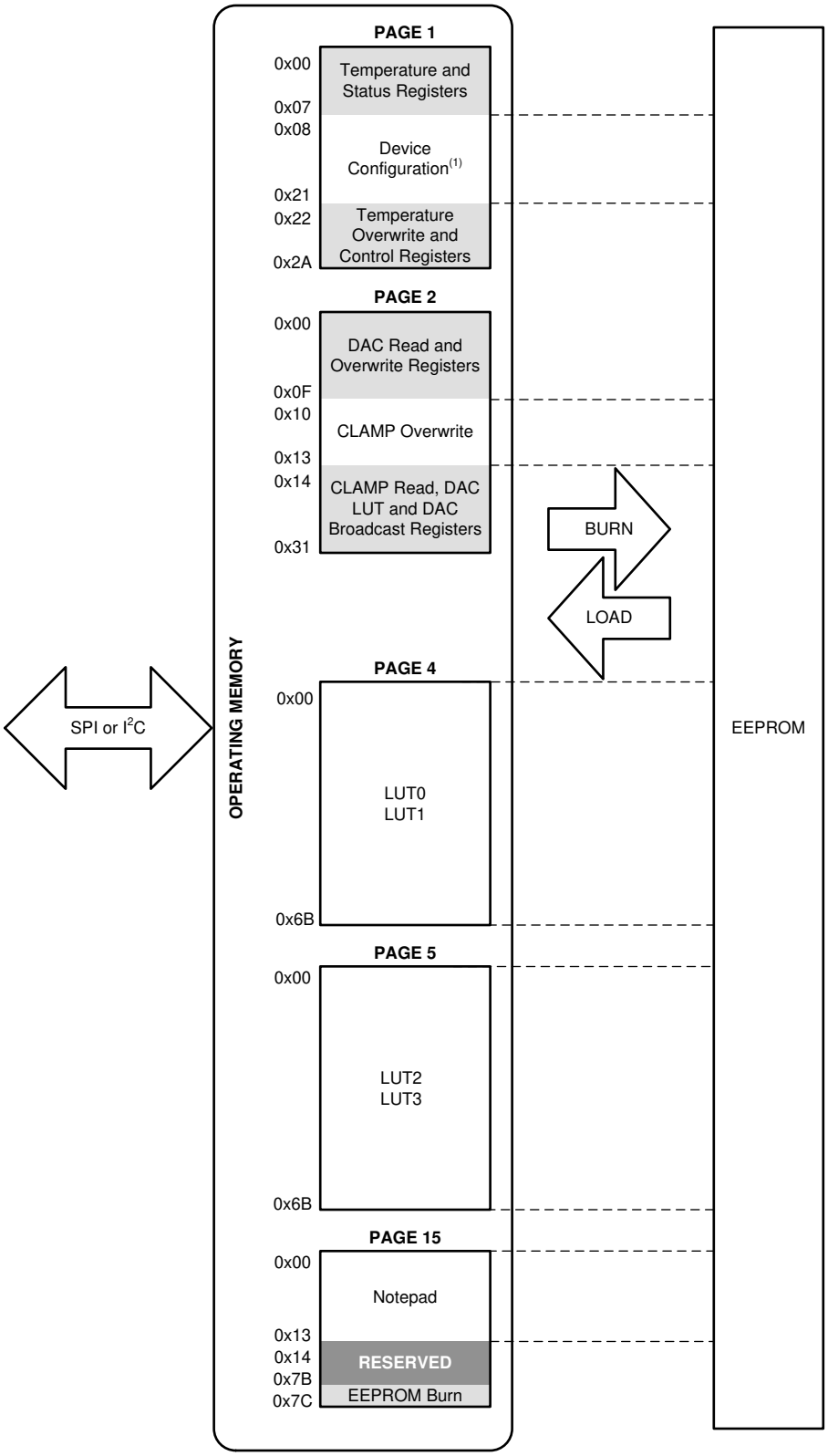


(1) Not all bits in Page 1 registers 0x08 to 0x21 are stored in the EEPROM. See *Section 7* for more information.

Figure 6-14. Memory-to-EEPROM Mapping

ADVANCE INFORMATION

6.3.5.2.1 EEPROM Integrity Check

Before completing the EEPROM load sequence, a CRC error-check is performed by the device. The CRC polynomial is $x^{12} + x^{11} + x^3 + x^2 + x + 1$. The CRC check result is reported through the EECRC bit. If a CRC error is detected, the operating memory values are compromised; reset the device or burn the EEPROM again for proper operation.

For added robustness, a single error correction and double error detection (SECDED) circuit based on the Hamming code is added to data in the LUT pages (Page 4 and Page 5). The SECDED circuit uses four Hamming code bits and a parity bit. The interleaved Hamming and LUT data are stored in EEPROM, and Table 6-10 shows these bits.

Table 6-10. Hamming Code and LUT Data Bits

DATA AND BIT POSITION	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data and Hamming code bits in operating memory	P	H3	H2	H1	H0	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0
Data and Hamming code interleaved bits	X	X	X	D7	D6	D5	D4	H3	D3	D2	D1	H2	D0	H1	H0	P

The SECDED circuit checks the data integrity on every LUT register access. The parity bit (P) and four Hamming code bits (H[3:0]) in the HAMM registers equal all zeros if no error is present in the associated LUT data register. If P = 1 then a single error has been detected and corrected. The value in the H[3:0] bits represents the position of the bit error with respect to the interleaved bits. For example, if P = 1 and H[3:0] = 0x5, an error is detected and corrected in D1.

If P = 0 and H[3:0] ≠ 0, then a double error has been detected. No correction is done in this case.

Table 6-11 summarizes the device EEPROM integrity checks.

Table 6-11. Status of EEPROM Access

STATUS BIT NAME	DESCRIPTION
EECRC	0 = No CRC error detected. 1 = A CRC error is detected during a EEPROM load. The operating memory data are compromised.
EERDY	0 = The EEPROM burn is in progress. 1 = The EEPROM burn is complete.
DED	0 = No double-bit error detected. 1 = A double-bit error is detected when accessing a LUT register in the operating memory. The error is not corrected.
SED	0 = No single-bit error detected. 1 = A single-bit error is detected when accessing a LUT register in the operating memory. The error is corrected.

6.3.6 Device Sequence Control

Depletion mode PA devices, such as those based on gallium nitride (GaN) transistors, require special gate and drain bias sequencing for proper operation and to avoid damage. The device includes an automatic sequence control circuit that, in combination with the PA_ON pin, provides proper power-up and power-down sequences for the PA transistors.

6.3.6.1 Depletion-Mode Field-Effect Transistor (FET) Bias Requirements

In depletion-mode FETs, when a negative voltage is applied between the gate and source terminals, an area of carrier depletion is formed within the channel that restricts the flow of current. In the absence of a negative gate bias voltage, the channel is fully open and maximum current can flow from drain to source, which can quickly destroy the device through electrical overstress. As the gate bias voltage becomes more negative, the device reaches the *pinch-off* state, where all the drain-to-source current flow is restricted and the FET is effectively off.

CAUTION

To prevent overcurrent damage to the transistor, bias the gate with a negative voltage less than the pinch-off voltage before applying the drain voltage. This order must be reversed when powering down the FET or when an alarm event is detected and a safe shut-down is required.

6.3.6.2 Sequence Control

The device built-in sequencer, in combination with the PA_ON pin, enables proper FET power-up and power-down sequencing. Additionally, the device includes various alarm monitoring options to execute a safety shut-down and recovery from those alarm events. Figure 6-15 shows a detailed diagram of the device sequence.

6.3.6.2.1 Start-Up Sequence

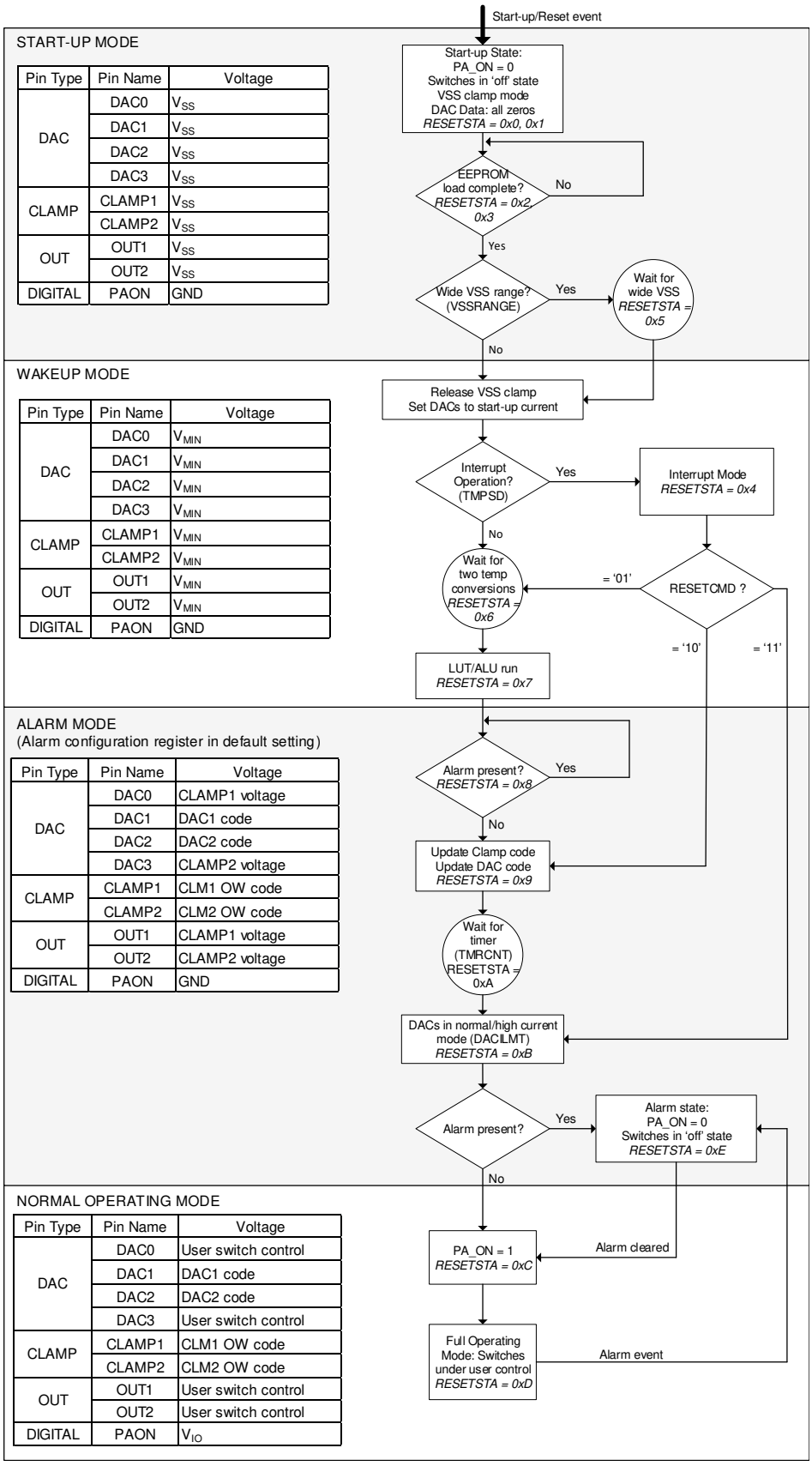
A start-up condition is generated by a reset event; either a power-on-reset, a logic low on the $\overline{\text{RESET}}$ pin, a software reset command, or an I^2C general-call reset. At start-up, all DACs are in VSS clamp mode (see *Section 6.3.1.3*), the PA_ON pin is set low, all switches are in the off state, and input data for all DACs is set to 0x0000.

After start-up, the device automatically initiates a EEPROM load sequence to configure the user memory registers, including the overwrite register value for the CLAMP DACs (CLAMP*x*OW[12:0]). Communication to the device is disabled until the EEPROM load sequence completes.

Upon completion of the EEPROM load sequence, the DACs exit VSS clamp mode. The output switches continue to be forced to the off state, thus setting the DAC0, OUT1, OUT2 and DAC3 output pins to the CLAMP voltages set by the CLAMP overwrite registers (CLAMP1: DAC0 and OUT1, CLAMP2: OUT2 and DAC3).

If the EEPROM has been configured for autonomous operation (see *Section 6.4.1*), the device confirms whether the V_{SS} supply is configured for wide-range operation (VSSRANGE bit). If so, the device waits until the V_{SS} supply has reached the valid operating range. After the valid supply ranges have been met, the device initiates two temperature sensor conversions. The second temperature measurement is input to the LUT, and the DAC[0:3] input data registers are loaded with the LUT- and ALU-generated data.

A programmable timer (TMRCNT[1:0]) is implemented to give enough time for the DAC output amplifiers to charge a capacitive load. During this time, the DAC output amplifiers are forced into start-up current mode, where source and sink capability is limited to 12mA. Start-up current mode controls the supply current being drawn by the device while charging capacitive loads. After the timer expires, the DAC output amplifiers exit start-up current mode, and assume the current-mode selected by the DACILMT bit. Then, the PA_ON pin is set high, and control of the switches is released to the user.



START-UP MODE

Pin Type	Pin Name	Voltage
DAC	DAC0	V_{SS}
	DAC1	V_{SS}
	DAC2	V_{SS}
	DAC3	V_{SS}
CLAMP	CLAMP1	V_{SS}
	CLAMP2	V_{SS}
OUT	OUT1	V_{SS}
	OUT2	V_{SS}
DIGITAL	PAON	GND

WAKEUP MODE

Pin Type	Pin Name	Voltage
DAC	DAC0	V_{MIN}
	DAC1	V_{MIN}
	DAC2	V_{MIN}
	DAC3	V_{MIN}
CLAMP	CLAMP1	V_{MIN}
	CLAMP2	V_{MIN}
OUT	OUT1	V_{MIN}
	OUT2	V_{MIN}
DIGITAL	PAON	GND

ALARM MODE
(Alarm configuration register in default setting)

Pin Type	Pin Name	Voltage
DAC	DAC0	CLAMP1 voltage
	DAC1	DAC1 code
	DAC2	DAC2 code
	DAC3	CLAMP2 voltage
CLAMP	CLAMP1	CLM1 OW code
	CLAMP2	CLM2 OW code
OUT	OUT1	CLAMP1 voltage
	OUT2	CLAMP2 voltage
DIGITAL	PAON	GND

NORMAL OPERATING MODE

Pin Type	Pin Name	Voltage
DAC	DAC0	User switch control
	DAC1	DAC1 code
	DAC2	DAC2 code
	DAC3	User switch control
CLAMP	CLAMP1	CLM1 OW code
	CLAMP2	CLM2 OW code
OUT	OUT1	User switch control
	OUT2	User switch control
DIGITAL	PAON	V_{IO}

Figure 6-15. Sequence Flow Diagram

6.3.6.2.2 Power-Down Sequence

The device continuously monitors the state of the supply voltages. If V_{DD}, V_{CC}, or V_{SS} drop to less than the respective valid thresholds, a supply-collapse reset event is generated. See also Section 6.3.1.3.

Along with a supply collapse, there are three additional reset events:

- Logic low on the $\overline{\text{RESET}}$ pin
- Software reset command
- I^2C general-call reset

All reset events generate a power-down sequence. At power down, the DAC outputs enter VSS clamp mode, the PA_ON pin is set low, and all switches are forced to the off position.

If the device supply voltages are at proper operating levels, a start-up sequence is automatically initiated after power down.

6.3.6.2.3 Alarm Event

An alarm event is generated by either a temperature sensor alarm (see *Section 6.3.3.4*), a logic low on the $\overline{\text{ALARMIN}}$ pin, or a software alarm command. The device is configured by default to set the PA_ON pin low and force all switches to the off position in response to an alarm event. After the alarm condition is released, the device returns to normal operation. The DAC input data registers are not modified during the alarm condition. To control the device response to an alarm event, program the alarm configuration register bits.

6.4 Device Functional Modes

The simplified numeric signal path for a DAC and CLAMP channels is shown in Figure 6-16. The temperature sensor serves as the input to the system. Signal processing is done by the LUT and ALU, and the output is driven to the DAC. The CLAMP input code upper eight bits (CLAMP[12:5]) are automatically controlled so that these bits never exceed the upper eight bits of the code being input to the associated DACs (CLAMP1: DAC[0:1] and CLAMP2: DAC[2:3]). The DAC and CLAMP details are omitted because the DAC and CLAMP provide a conversion from numeric domain to voltage domain only, and do not affect the signal flow.

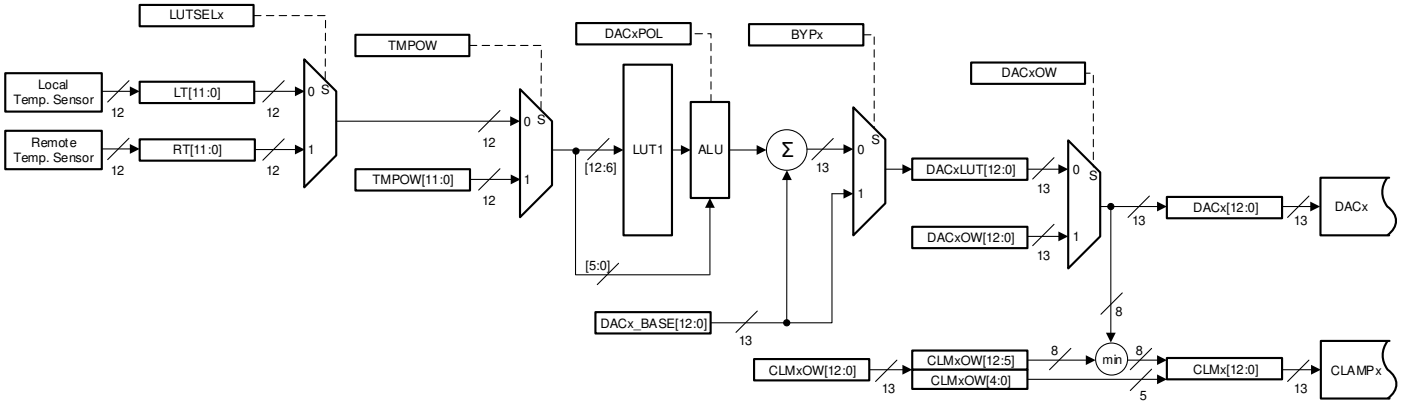


Figure 6-16. Data Path

6.4.1 Autonomous Operating Mode

Unless a different configuration has been burned in the EEPROM, autonomous operation is active upon start-up. By default, the temperature sensor is active (TMPSD = 0) and the LUT and both temperature sensors are enabled (LUTDIS = 0, REN = 1 and LEN = 1). Also by default, the temperature overwrite (TMPOW) and DAC overwrite (DAC*x*OW) bits are cleared.

In autonomous mode, the device begins temperature measurements at start-up. Each temperature sensor update triggers the ALU to recalculate the output using the user-defined coefficients, polarity, and BASE value stored in the LUT pages. The ALU output is passed on to the DAC LUT register that ultimately drives the DAC input.

The device remains in autonomous operation unless the data path is overwritten, the LUT is disabled (LUTDIS = 1), or the temperature sensor is powered down (TMPSD = 1). If the LUT is disabled or the temperature sensor is powered down, the DAC output remains at the last calculated value. The device automatically returns to autonomous operation after being reconfigured properly.

6.4.2 Manual Operating Mode

There are a number of multiplexers in the signal path that alter the data flow when the respective control bits are set. The multiplexer states that set the various modes of manual operation are described in further detail in the following subsections.

6.4.2.1 DAC Input Overwrite

The DAC inputs words can be directly written through the serial interface. In this mode, the device operates as a multichannel, 13-bit DAC. This functionality is facilitated by the multiplexers that precede the DACs, and user-writable DAC overwrite data registers (DAC*x*OW[12:0]). The multiplexer control signal is the DAC overwrite bit (DAC*x*OW). Although not required by the device, set the LUTDIS bit to optionally disable the LUT and ALU.

6.4.2.2 Temperature Sensor Overwrite

The temperature sensor output is able to be overwritten by externally supplied data. If needed, use this capability to verify the validity of the function stored in the LUT. The externally supplied data act as the temperature sweep input, and the output response caused by temperature is able to be readily observed without altering the temperature of the test setup.

This functionality is facilitated by the multiplexer that follows the temperature sensor, and user-writable temperature overwrite data register (TMPOW[11:0]). The multiplexer control signal is the TMPOW bit. To cancel the temperature sensor overwrite, clear the TMPOW bit.

6.4.2.3 ALU Bypass

The ALU bypass mode sets the output at a predetermined constant output level. To enable this mode, set the bypass bits (BYP*x*). In this mode of operation, the ALU is bypassed, and the BASE value of the LUT is presented at the input of the DAC, resulting in a constant output over the operating temperature range of the device.

6.4.3 Interrupt Mode

The interrupt mode enables device debugging. To enable interrupt mode, power down the temperature sensor (TMPSD = 1) and set the interrupt mode bit (AMCINT = 1). The interrupt mode enables individual control of the device automatic reset sequence steps. See also *Section 7.3.1.1.15*.

While the reset control module remains in interrupt mode, the device does not generate alarm events. To exit interrupt mode, clear the TMPSD and AMCINT bits. After these bits have been configured, program the RESETCMD[1:0] bits a nonzero value to restart the reset control module.

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6.5 Programming

Note

In SPI configuration, hold the SDA pin low for proper operation.

The device communicates with the system controller through a serial interface, which supports either an I²C-compatible two-wire bus, or an SPI-compatible bus. The device includes a robust mechanism that detects between an SPI-compatible or I²C-compatible controller, and automatically configures the interface accordingly. The interface detection mechanism operates at start-up, thus preventing protocol change during normal operation.

The device uses a paging system to organize registers by functionality. In both SPI and I²C configurations, address 0x7E is used to select the different pages in the device. The default page at start-up is Page 1. To read and write to one of the device registers, first select the page for that register by writing the 8-bit representation of the page number (PAGE[7:0]) to address 0x7E. Figure 6-17 shows the page access format. The page register holds the page value until a new page address is programmed to the device.

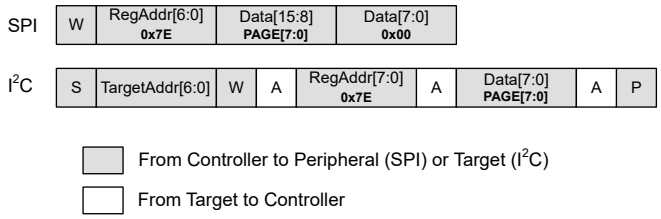

Figure 6-17. Page Access Format

6.5.1 I²C Serial Interface

In I²C mode, the device operates only as a target device on the two-wire bus. Connections to either bus are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The device supports the transmission protocol for fast (1kHz to 400kHz) mode. All data bytes are transmitted MSB first.

6.5.1.1 I²C Bus Overview

The device is I²C compatible. In I²C protocol, the device that initiates the transfer is called a *controller*, and the devices controlled by the controller are *targets*. To control the bus, use a controller device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. A START condition is indicated by pulling the data line (SDA) from a high-to-low logic level while SCL is high. All targets on the bus shift in the target address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, ensure that SDA remains stable while SCL is high because any change in SDA while SCL is high is interpreted as a control signal.

After all data have been transferred, the controller generates a STOP condition. A STOP condition is indicated by pulling SDA from low to high, while SCL is high.

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6.5.1.2 I²C Bus Definitions

The device is I²C-compatible and Table 6-12 lists the bus definitions. See Figure 6-18 and Figure 6-19 for the write and read timing diagram formats.

Table 6-12. I²C Symbol Set

CONDITION	SYMBOL	SOURCE	DESCRIPTION
START	S	Controller	Begins all bus transactions. A change in the state of the SDA line, from high to low, while the SCL line is high, defines a start condition. Each data transfer initiates with a START condition.
STOP	P	Controller	Terminates all transactions and resets bus. A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer terminates with a repeated START or STOP condition.
IDLE	I	Controller	Bus idle. Both SDA and SCL lines remain high.
ACK (Acknowledge)	A	Controller-Target	Handshaking bit (low). Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Take setup and hold times into account.
NACK (Not Acknowledge)	$\overline{A}$	Controller-Target	Handshaking bit (high). On a controller receive, data transfer termination can be signaled by the controller generating a not-acknowledge on the last byte that has been transmitted by the target.
READ	R	Controller	Active-high bit that follows immediately after the target address sequence. Indicates that the controller is initiating the target-to-controller data transfer. The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the controller device. The receiver acknowledges data transfer.
WRITE	$\overline{W}$	Controller	Active-low bit that follows immediately after the target address sequence. Indicates that the controller is initiating the controller-to-target data transfer. The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the controller device. The receiver acknowledges data transfer.
REPEATED START	Sr	Controller	Generated by the controller, same function as the START condition (highlights the fact that STOP condition is not strictly necessary.)
BLOCK ACCESS	B	Controller	Active-high bit that replaces bit 7 of the register address. This bit indicates the controller is initiating a block access data transfer.

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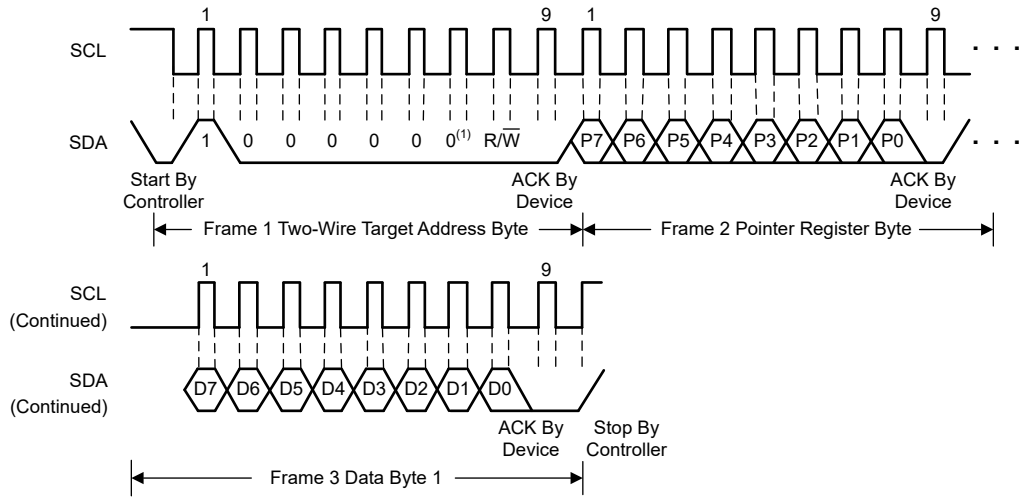
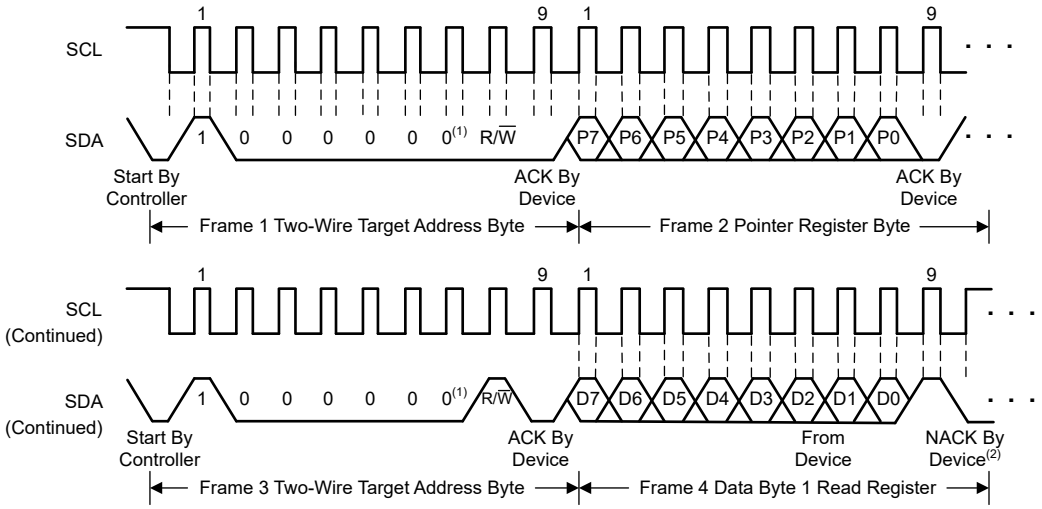


(1) Target address 1000000 shown.

Figure 6-18. I²C Timing Diagram for Write Word Format



(1) Target address 1000000 shown.

(2) Ensure that the controller sets SDA high to terminate a single-byte read operation.

Figure 6-19. I²C Timing Diagram for Single-Byte Read Format

6.5.1.3 I²C Target Address Selection

The I²C bus target address is selected by installing shunts from the A0, A1, and A2 pins to the V_{IO} or GND rails. The state of the A0, A1, and A2 pins is tested after every occurrence of START condition on the I²C bus. The device discerns between two possible options for each pin: shunt to V_{IO} (logic 1) and shunt to GND (logic 0) for a total of eight possible target addresses. Table 6-13 shows the I²C target address space.

Table 6-13. I²C Target Address Space

DEVICE PINS			I²C TARGET ADDRESS
A2	A1	A0	[A6:A0]
0	0	0	100 0000
0	0	1	100 0001
0	1	0	100 0010
0	1	1	100 0011
1	0	0	100 0100
1	0	1	100 0101
1	1	0	100 0110
1	1	1	100 0111

Figure 6-20 shows the target address alignment within the first byte following the START condition.

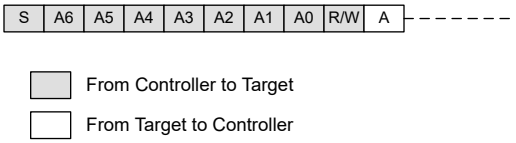


Figure 6-20. Target Address Alignment

6.5.1.4 I²C Read and Write Operations

When writing to the device, the value for the address register is the first byte transferred after the target address byte with the R/$\overline{W}$ bit low. Figure 6-21 shows that every write operation to the device requires a value for the address register.

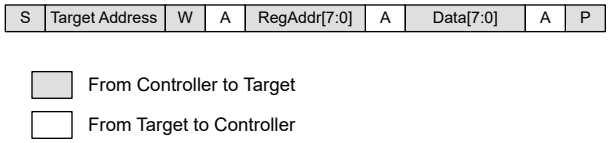


Figure 6-21. I²C Single-Byte Write Access Protocol

When reading from the device the last value stored in the address register by a write operation is used to determine which register is read by a read operation. To change which register is read for a read operation, a new value must be written to the address register. This transaction is accomplished by issuing a target address byte with the R/$\overline{W}$ bit low, followed by the address register byte; no additional data are required. The controller can then generate a START condition and send the target address byte with the R/$\overline{W}$ bit high to initiate the read command.

If repeated reads from the same register are desired, there is no need to continually send the address register bytes because the device retains the address register value until the value is changed by the next write operation. The register bytes are sent MSB first, followed by the LSB.

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Terminate read operations by issuing a *not-acknowledge* condition at the end of the last byte to be read. Figure 6-22 shows that for single-byte operation, the controller must leave the SDA line high during the acknowledge time of the first byte that is read from the target.

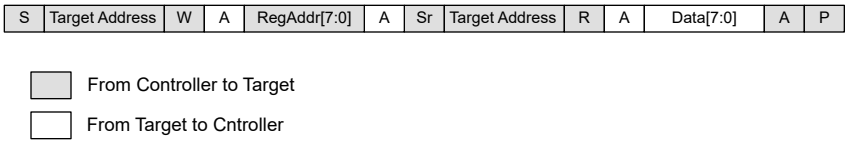

Figure 6-22. I²C Single-Byte Read Access Protocol

Block access functionality is provided to minimize the transfer overhead of large data sets. Block access enables multibyte transfers and is configured by setting bit 7 of the register address high. Figure 6-23 and Figure 6-24 show that until the transaction is terminated by the STOP condition, the device reads and writes the subsequent memory locations. If the controller reaches address 0x7E in a page, the device continues reading and writing from this address until the transaction is terminated.

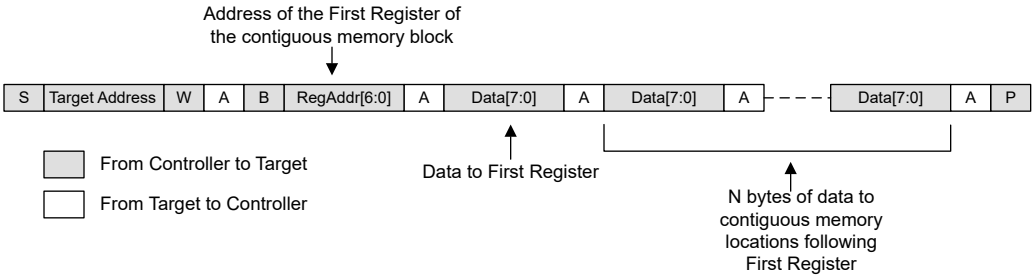

Figure 6-23. I²C Block Write Access

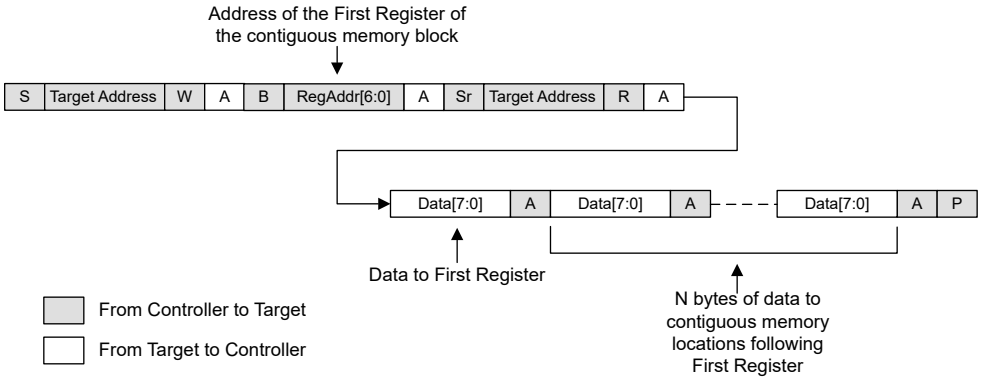

Figure 6-24. I²C Block Read Access

6.5.1.5 I²C Timeout Function

The device resets the serial interface if either SCL or SDA are held low for 25ms (typical) between a START and STOP condition. If the device is holding the bus low, the device releases the bus and waits for a START condition. To avoid activating the timeout function, maintain a communication speed of at least 1kHz for the SCL operating frequency.

6.5.1.6 I²C General-Call Reset

The device supports reset using the two-wire general call address 00h (0000 0000b). The device acknowledges the general-call address, and responds to the second byte. If the second byte is 06h (0000 0110b), the device executes a software reset. This software reset initiates a reset event. The device takes no action in response to other values in the second byte.

6.5.2 Serial Peripheral Interface (SPI)

In SPI mode, the device is controlled through a flexible four-wire serial interface that is compatible with SPI-type interfaces used on many microcontrollers and DSP controllers. The interface provides access to the device registers, and incorporates an optional error checking mode to validate SPI data communication integrity in noisy environments.

6.5.2.1 SPI Bus Overview

A serial interface access cycle is initiated by asserting the $\overline{CS}$ pin low. The serial clock SCLK is able to be a continuous or gated clock. SDI data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long with error checking disabled, and 32 bits long with error checking enabled. Thus, ensure that the $\overline{CS}$ pin stays low for at least 24 or 32 SCLK falling edges. The access cycle ends when the $\overline{CS}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the last 24 or 32 bits are used by the device. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked and the SDO pin is in a Hi-Z state.

In an error checking disabled access cycle (24-bits long), the first byte input to SDI is the instruction cycle that identifies the request as a read or write command, and the 7-bit address to be accessed. The following bits in the cycle form the data cycle. Table 6-14 shows the SPI access cycle.

Table 6-14. SPI Access Cycle

BIT	FIELD	DESCRIPTION
23	R/W	Identifies the communication as a read or write command to the addressed register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
22:16	A[6:0]	Register address. Specifies the register to be accessed during the read or write operation.
15:0	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values written to the register with address A[6:0]. If a read command, the data cycle bits are don't care values.

Read operations require that the SDO pin is first enabled by setting the SDOEN bit. A read operation is initiated by issuing a read command access cycle. After the read command, issue a second access cycle to get the requested data; see also Table 6-15. The lower eight bits of the status register (STATUS[7:0]) and data are clocked out on the SDO pin on SCLK rising edges.

Table 6-15. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23:16	STATUS[7:0]	Lower eight bits of the status register.
15:0	DO[15:0]	Readback data requested on previous access cycle.

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6.5.2.2 SPI Frame Error Check

If the device is used in a noisy environment, error checking is used to check the integrity of SPI data communication between the device and the host processor. This feature is enabled by setting the CRCEN bit.

The error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, 100000111). When error checking is enabled, the serial interface access cycle width is 32 bits. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before sending the data to the device. Table 6-16 shows the SPI error checking serial interface access cycle. In all serial interface readback operations the CRC polynomial is output on the SDO pin as part of the 32-bit cycle.

Table 6-16. SPI Error Checking Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
31	R/W	Identifies the communication as a read or write command to the addressed register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
30:24	A[6:0]	Register address. Specifies the register to be accessed during the read or write operation.
23:8	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are don't care values.
7:0	CRC	8-bit CRC polynomial.

The device decodes the 32-bit access cycle to compute the CRC remainder on $\overline{CS}$ rising edges. If no error exists, the CRC remainder is zero and data are accepted by the device. A write operation failing the CRC check causes the data to be ignored by the device.

After the write command, issue a second access cycle to determine the device status, including the CRC error check result (SPICRC bit), on the SDO pin. Table 6-17 shows the SPI write operation error checking cycle. After being set, write a 1 to the SPICRC bit in the Status register to clear the bit.

Table 6-17. SPI Write Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31:24	STATUS[7:0]	Lower eight bits of the status register.
23:8	DO[15:0]	Echo data from previous access cycle.
7:0	CRC	Calculated CRC value of bits 31:8.

To get the requested data on the SDO pin, follow a read operation with a second access cycle. As in the case of a write operation, the device status is output on the SDO pin; see also Table 6-18.

Table 6-18. SPI Read Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31:24	STATUS[7:0]	Lower eight bits of the Status register.
23:8	DO[15:0]	Readback data requested on previous access cycle.
7:0	CRC	Calculated CRC value of bits 31:8.

7 Register Maps

7.1 I²C Register Maps

Table 7-1. I²C Page 1: Device Configuration Register Map

ADDR (HEX)	TYPE	FACTORY (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*								REGISTER DESCRIPTION
			7	6	5	4	3	2	1	0	
00	R	N/A	LT[11:4]								Local temperature (high byte)
01	R	N/A	LT[3:0]				0	0	0	0	Local temperature (low byte)
02	R	N/A	RT[11:4]								Remote temperature (high byte)
03	R	N/A	RT[3:0]				0	0	0	0	Remote temperature (low byte)
04	R	N/A	BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	X	X	Temperature status
05	R	N/A	TMPSTAT	PAON	EECRC	X	EERDY	DED	SEC	GAN	AMC status
07	W	00	SOFTRST[7:0]								Software reset
08	R/W	01	X	TMPSD	ALERT/THERM	VSSRANGE	DACILMT	TMPRANGE	TMRCNT[1:0]		Configuration 1
09	R/W	08	X	X	HAMMOFF	X	CR[3:0]				Configuration 2
0A	R/W	03	X	X	LUTSTAT	LUTDIS	LUTSEL2	LUTSEL1	REN	LEN	LUT Configuration
0B	R/W	00	BYP3	BYP2	BYP1	BYP0	DAC3OW	DAC2OW	DAC1OW	DAC0OW	DAC overwrite enable
0C	R/W	00	X	X	DRVEN3	DRVEN2	X	X	DRVEN1	DRVEN0	Drive enable
0D	R/W	00	X	X	DRVSEL3	DRVSEL2	X	X	DRVSEL1	DRVSEL0	Drive enable select
0E	R/W	4F	ALMINEN	PAONDIS	X	X	DAC3OFF	OUT2OFF	OUT1OFF	DAC0OFF	Alarm configuration
0F	R/W	00	RESETCMD[1:0]		X	AMCINT	DRVENRLS	PAONRLS	DACHCRLS	DACRLS	Interrupt mode
10	R/W	7F	LTHL[11:4]								Local temperature high limit (high byte)
11	R/W	80	LTLL[11:4]								Local temperature low limit (high byte)
12	R/W	7F	RTHL[11:4]								Remote temperature high limit (high byte)
13	R/W	F0	RTHL[3:0]				X	X	X	X	Remote temperature high limit (low byte)
14	R/W	80	RTLL[11:4]								Remote temperature low limit (high byte)
15	R/W	00	RTLL[3:0]				X	X	X	X	Remote temperature low limit (low byte)
16	R/W	00	RTOS[11:4]								Remote temperature offset (high byte)
17	R/W	00	RTOS[3:0]				X	X	X	X	Remote temperature offset (low byte)
1A	R/W	0A	HYS[11:4]								THERM hysteresis
1B	R/W	01	X	X	X	X	CONAL[2:0]			1	Consecutive ALERT
1C	R/W	00	NC[7:0]								η-factor correction
1D	R/W	00	X	X	X	X	X	X	DF[1:0]		Digital filter control
1E	R	00	VERSION[7:0]								Version ID
1F	R	A3	ID[7:0]								Device ID
22	R/W	00	TMPOW[11:4]								Temperature overwrite (high byte)
23	R/W	00	TMPOW[3:0]				X	X	X	TMPOW	Temperature overwrite (low byte)
24	R	N/A	X	X	X	X	RESETSTA[3:0]				Reset status
28	W	00	TMPONE[7:0]								One-shot temperature
2A	R/W	00	0	0	0	0	0	0	0	SWALM	Software alarm

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Table 7-2. I²C Page 2: DAC Configuration Register Map

ADDR (HEX)	TYPE	FACTORY (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*								REGISTER DESCRIPTION
			7	6	5	4	3	2	1	0	
00	R	00	0	0	0	DAC0[12:8]					DAC0 (high byte)
01	R	00	DAC0[7:0]								DAC0 (low byte)
02	R	00	0	0	0	DAC1[12:8]					DAC1 (high byte)
03	R	00	DAC1[7:0]								DAC1 (low byte)
04	R	00	0	0	0	DAC2[12:8]					DAC2 (high byte)
05	R	00	DAC2[7:0]								DAC2 (low byte)
06	R	00	0	0	0	DAC3[12:8]					DAC3 (high byte)
07	R	00	DAC3[7:0]								DAC3 (low byte)
08	R/W	00	X	X	X	DAC0OW[12:8]					DAC0 overwrite (high byte)
09	R/W	00	DAC0OW[7:0]								DAC0 overwrite (low byte)
0A	R/W	00	X	X	X	DAC1OW[12:8]					DAC1 overwrite (high byte)
0B	R/W	00	DAC1OW[7:0]								DAC1 overwrite (low byte)
0C	R/W	00	X	X	X	DAC2OW[12:8]					DAC2 overwrite (high byte)
0D	R/W	00	DAC2OW[7:0]								DAC2 overwrite (low byte)
0E	R/W	00	X	X	X	DAC3OW[12:8]					DAC3 overwrite (high byte)
0F	R/W	00	DAC3OW[7:0]								DAC3 overwrite (low byte)
10	R/W	00	X	X	X	CLM1OW[12:8]					CLAMP1 overwrite (high byte)
11	R/W	00	CLM1OW[7:0]								CLAMP1 overwrite (low byte)
12	R/W	00	X	X	X	CLM2OW[12:8]					CLAMP2 overwrite (high byte)
13	R/W	00	CLM2OW[7:0]								CLAMP2 overwrite (low byte)
18	R	00	0	0	0	CLM1[12:8]					CLAMP1 (high byte)
19	R	00	CLM1[7:0]								CLAMP1 (low byte)
1A	R	00	0	0	0	CLM2[12:8]					CLAMP2 (high byte)
1B	R	00	CLM2[7:0]								CLAMP2 (low byte)
20	R	00	0	0	0	DAC0LUT[12:8]					DAC0 LUT (high byte)
21	R	00	DAC0LUT[7:0]								DAC0 LUT (low byte)
22	R	00	0	0	0	DAC1LUT[12:8]					DAC1 LUT (high byte)
23	R	00	DAC1LUT[7:0]								DAC1 LUT (low byte)
24	R	00	0	0	0	DAC2LUT[12:8]					DAC2 LUT (high byte)
25	R	00	DAC2LUT[7:0]								DAC2 LUT (low byte)
26	R	00	0	0	0	DAC3LUT[12:8]					DAC3 LUT (high byte)
27	R	00	DAC3LUT[7:0]								DAC3 LUT (low byte)
30	R/W	00	X	X	X	BRDCST[12:8]					Broadcast (high byte)
31	R/W	00	BRDCST[7:0]								Broadcast (low byte)

Table 7-3. I²C Page 4: LUT0 and LUT1 Configuration Register Map

ADDR (HEX)	TYPE	FACTORY (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*								REGISTER DESCRIPTION
			7	6	5	4	3	2	1	0	
00	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn48: –48°C
01	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn48: –48°C
02	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn44: –44°C
03	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn44: –44°C
04	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn40: –40°C
05	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn40: –40°C
06	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn36: –36°C
07	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn36: –36°C
08	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn32: –32°C
09	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn32: –32°C
0A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn28: –28°C
0B	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn28: –28°C
0C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn24: –24°C
0D	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn24: –24°C
0E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn20: –20°C
0F	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn20: –20°C
10	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn16: –16°C
11	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn16: –16°C
12	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn12: –12°C
13	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn12: –12°C
14	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn8: –8°C
15	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn8: –8°C
16	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn4: –4°C
17	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAn4: –4°C
18	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp0: 0°C
19	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp0: 0°C
1A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp4: 4°C
1B	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp4: 4°C
1C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp8: 8°C
1D	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp8: 8°C
1E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp12: 12°C
1F	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp12: 12°C
20	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp16: 16°C
21	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp16: 16°C
22	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp20: 20°C
23	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp20: 20°C
24	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp28: 28°C
25	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp28: 28°C

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Table 7-3. I²C Page 4: LUT0 and LUT1 Configuration Register Map (continued)

ADDR (HEX)	TYPE	FACTORY (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*								REGISTER DESCRIPTION
			7	6	5	4	3	2	1	0	
26	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp32: 32°C
27	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp32: 32°C
28	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp36: 36°C
29	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp36: 36°C
2A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp40: 40°C
2B	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp40: 40°C
2C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp44: 44°C
2D	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp44: 44°C
2E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp48: 48°C
2F	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp48: 48°C
30	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp52: 52°C
31	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp52: 52°C
32	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp56: 56°C
33	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp56: 56°C
34	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp60: 60°C
35	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp60: 60°C
36	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp64: 64°C
37	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp64: 64°C
38	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp68: 68°C
39	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp68: 68°C
3A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp72: 72°C
3B	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp72: 72°C
3C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp76: 76°C
3D	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp76: 76°C
3E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp80: 80°C
3F	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp80: 80°C
40	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp84: 84°C
41	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp84: 84°C
42	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp88: 88°C
43	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp88: 88°C
44	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp92: 92°C
45	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp92: 92°C
46	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp96: 96°C
47	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp96: 96°C
48	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp100: 100°C
49	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp100: 100°C
4A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp104: 104°C
4B	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp104: 104°C

Table 7-3. I²C Page 4: LUT0 and LUT1 Configuration Register Map (continued)

ADDR (HEX)	TYPE	FACTORY (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*								REGISTER DESCRIPTION
			7	6	5	4	3	2	1	0	
4C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp108: 108°C
4D	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp108: 108°C
4E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp112: 112°C
4F	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp112: 112°C
50	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp116: 116°C
51	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp116: 116°C
52	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp120: 120°C
53	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp120: 120°C
54	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp124: 124°C
55	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp124: 124°C
56	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp128: 128°C
57	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp128: 128°C
58	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp132: 132°C
59	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp132: 132°C
5A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp136: 136°C
5B	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp136: 136°C
5C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp140: 140°C
5D	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp140: 140°C
5E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp144: 144°C
5F	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp144: 144°C
60	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp148: 148°C
61	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp148: 148°C
62	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp152: 152°C
63	R/W	FF	DAC1[3:0]					DAC0[3:0]			DELTAp152: 152°C
64	R/W	00	P	HAMM[3:0]				X	X	X	HAMM BASE0 High
65	R/W	00	X	X	DAC0POL	DAC0BASE[12:8]					DAC0 BASE (high byte)
66	R/W	00	P	HAMM[3:0]				X	X	X	HAMM BASE0 Low
67	R/W	00	DAC0BASE[7:0]								DAC0 BASE (low byte)
68	R/W	00	P	HAMM[3:0]				X	X	X	HAMM BASE1 High
69	R/W	00	X	X	DAC1POL	DAC1BASE[12:8]					DAC1 BASE (high byte)
6A	R/W	00	P	HAMM[3:0]				X	X	X	HAMM BASE1 Low
6B	R/W	00	DAC1BASE[7:0]								DAC1 BASE (low byte)

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Table 7-4. I²C Page 5: LUT2 and LUT3 Configuration Register Map

ADDR (HEX)	TYPE	FACTORY (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*								REGISTER DESCRIPTION
			7	6	5	4	3	2	1	0	
00	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn48: –48°C
01	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn48: –48°C
02	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn44: –44°C
03	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn44: –44°C
04	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn40: –40°C
05	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn40: –40°C
06	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn36: –36°C
07	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn36: –36°C
08	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn32: –32°C
09	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn32: –32°C
0A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn28: –28°C
0B	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn28: –28°C
0C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn24: –24°C
0D	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn24: –24°C
0E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn20: –20°C
0F	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn20: –20°C
10	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn16: –16°C
11	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn16: –16°C
12	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn12: –12°C
13	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn12: –12°C
14	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn8: –8°C
15	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn8: –8°C
16	R/W	00	P	HAMM[3:0]				X	X	X	HAMMn4: –4°C
17	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAn4: –4°C
18	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp0: 0°C
19	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp0: 0°C
1A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp4: 4°C
1B	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp4: 4°C
1C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp8: 8°C
1D	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp8: 8°C
1E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp12: 12°C
1F	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp12: 12°C
20	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp16: 16°C
21	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp16: 16°C
22	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp20: 20°C
23	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp20: 20°C
24	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp28: 28°C
25	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp28: 28°C

Table 7-4. I²C Page 5: LUT2 and LUT3 Configuration Register Map (continued)

ADDR (HEX)	TYPE	FACTORY (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*								REGISTER DESCRIPTION
			7	6	5	4	3	2	1	0	
26	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp32: 32°C
27	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp32: 32°C
28	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp36: 36°C
29	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp36: 36°C
2A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp40: 40°C
2B	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp40: 40°C
2C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp44: 44°C
2D	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp44: 44°C
2E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp48: 48°C
2F	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp48: 48°C
30	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp52: 52°C
31	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp52: 52°C
32	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp56: 56°C
33	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp56: 56°C
34	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp60: 60°C
35	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp60: 60°C
36	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp64: 64°C
37	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp64: 64°C
38	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp68: 68°C
39	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp68: 68°C
3A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp72: 72°C
3B	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp72: 72°C
3C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp76: 76°C
3D	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp76: 76°C
3E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp80: 80°C
3F	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp80: 80°C
40	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp84: 84°C
41	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp84: 84°C
42	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp88: 88°C
43	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp88: 88°C
44	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp92: 92°C
45	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp92: 92°C
46	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp96: 96°C
47	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp96: 96°C
48	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp100: 100°C
49	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp100: 100°C
4A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp104: 104°C
4B	R/W	FF	DAC3[3:0]					DAC2[3:0]			DELTAp104: 104°C

ADVANCE INFORMATION

Table 7-4. I²C Page 5: LUT2 and LUT3 Configuration Register Map (continued)

ADDR (HEX)	TYPE	FACTORY (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*								REGISTER DESCRIPTION
			7	6	5	4	3	2	1	0	
4C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp108: 108°C
4D	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp108: 108°C
4E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp112: 112°C
4F	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp112: 112°C
50	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp116: 116°C
51	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp116: 116°C
52	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp120: 120°C
53	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp120: 120°C
54	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp124: 124°C
55	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp124: 124°C
56	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp128: 128°C
57	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp128: 128°C
58	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp132: 132°C
59	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp132: 132°C
5A	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp136: 136°C
5B	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp136: 136°C
5C	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp140: 140°C
5D	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp140: 140°C
5E	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp144: 144°C
5F	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp144: 144°C
60	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp148: 148°C
61	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp148: 148°C
62	R/W	00	P	HAMM[3:0]				X	X	X	HAMMp152: 152°C
63	R/W	FF	DAC3[3:0]				DAC2[3:0]				DELTAp152: 152°C
64	R/W	00	P	HAMM[3:0]				X	X	X	HAMM BASE2 High
65	R/W	00	X	X	DAC2POL	DAC2BASE[12:8]					DAC2 BASE (high byte)
66	R/W	00	P	HAMM[3:0]				X	X	X	HAMM BASE2 Low
67	R/W	00	DAC2BASE[7:0]								DAC2 BASE (low byte)
68	R/W	00	P	HAMM[3:0]				X	X	X	HAMM BASE3 High
69	R/W	00	X	X	DAC3POL	DAC3BASE[12:8]					DAC3 BASE (high byte)
6A	R/W	00	P	HAMM[3:0]				X	X	X	HAMM BASE3 Low
6B	R/W	00	DAC3BASE[7:0]								DAC3 BASE (low byte)

Table 7-5. I²C Page 15: Notepad Register Map

ADDR (HEX)	TYPE	FACTORY (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*								REGISTER DESCRIPTION
			7	6	5	4	3	2	1	0	
00	R/W	00	PAD0[7:0]								Notepad 0
01	R/W	00	PAD1[7:0]								Notepad 1
02	R/W	00	PAD2[7:0]								Notepad 2
03	R/W	00	PAD3[7:0]								Notepad 3
04	R/W	00	PAD4[7:0]								Notepad 4
05	R/W	00	PAD5[7:0]								Notepad 5
06	R/W	00	PAD6[7:0]								Notepad 6
07	R/W	00	PAD7[7:0]								Notepad 7
08	R/W	00	PAD8[7:0]								Notepad 8
09	R/W	00	PAD9[7:0]								Notepad 9
0A	R/W	00	PAD10[7:0]								Notepad 10
0B	R/W	00	PAD11[7:0]								Notepad 11
0C	R/W	00	PAD12[7:0]								Notepad 12
0D	R/W	00	PAD13[7:0]								Notepad 13
0E	R/W	00	PAD14[7:0]								Notepad 14
0F	R/W	00	PAD15[7:0]								Notepad 15
10	R/W	00	PAD16[7:0]								Notepad 16
11	R/W	00	PAD17[7:0]								Notepad 17
12	R/W	00	PAD18[7:0]								Notepad 18
13	R/W	00	PAD19[7:0]								Notepad 19
7C	W	00	EEBURN[7:0]								EEPROM burn

ADVANCE INFORMATION

7.2 SPI Register Maps

Table 7-6. SPI Page 1: Device Configuration Register Map

ADDR (HEX)	TYPE	FACT (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*																REGISTER DESCRIPTION
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	R	N/A	LT[11:0]												0	0	0	0	Local temperature
02	R	N/A	RT[11:0]												0	0	0	0	Remote temperature
04	R	N/A	BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	X	X	TMP STAT	PAON	EECRC	SPICRC	EERDY	DED	SEC	GAN	Status
06	W	0000	X	X	X	X	X	X	X	X	SOFTRST[7:0]								Software reset
08	R/W	0108	X	TMPSD	ALERT/ THERM	VSS RANGE	DAC ILMT	TMP RANGE	TMRCNT[1:0]		CRCEN	SDOEN	HAMM OFF	X	CR[3:0]				Configuration
0A	R/W	0300	X	X	LUT STAT	LUT DIS	LUT SEL2	LUT SEL1	REN	LEN	BYP3	BYP2	BYP1	BYP0	DAC3OW	DAC2OW	DAC1OW	DAC0OW	LUT/DAC configuration
0C	R/W	0000	X	X	DRV EN3	DRV EN2	X	X	DRV EN1	DRV EN0	X	X	DRV SEL3	DRV SEL2	X	X	DRV SEL1	DRV SEL0	Drive enable configuration
0E	R/W	4F00	ALMIN EN	PAON DIS	X	X	DAC3 OFF	OUT2 OFF	OUT1 OFF	DAC0 OFF	RESETCMD[1:0]		X	AMC INT	DRVEN RLS	PAON RLS	DACHC RLS	DAC RLS	Alarm configuration
10	R/W	7F80	LTHL[11:4]								LTLL[11:4]								Local temperature limit
12	R/W	7FF0	RTHL[11:4]								RTHL[3:0]				X	X	X	X	Remote temperature high limit
14	R/W	8000	RTLL[11:4]								RTLL[3:0]				X	X	X	X	Remote temperature low limit
16	R/W	0000	RTOS[11:0]												X	X	X	X	Remote temperature offset
1A	R/W	0A01	HYS[11:4]								X	X	X	X	CONAL[2:0]			1	Temperature configuration 1
1C	R/W	0000	NC[7:0]								X	X	X	X	X	X	DF[1:0]		Temperature configuration 2
1E	R	00A3	VERSION[7:0]								ID[7:0]								Device ID
22	R/W	0000	TMPOW[11:0]												0	0	0	TMPOW	Temperature overwrite
24	R	N/A	X	X	X	X	RESETSTA[3:0]				0	0	0	0	0	0	0	0	Reset status
28	W	0000	TMPONE[15:0]																One-shot temperature
2A	R/W	0000	X	X	X	X	X	X	X	SW ALM	X	X	X	X	X	X	X	X	Software alarm

ADVANCE INFORMATION

Table 7-7. SPI Page 2: DAC Configuration Register Map

ADDR (HEX)	TYPE	FACT (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*																REGISTER DESCRIPTION
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	R	0000	0	0	0	DAC0[12:0]													DAC0
02	R	0000	0	0	0	DAC1[12:0]													DAC1
04	R	0000	0	0	0	DAC2[12:0]													DAC2
06	R	0000	0	0	0	DAC3[12:0]													DAC3
08	R/W	0000	X	X	X	DAC0OW[12:0]													DAC0 overwrite
0A	R/W	0000	X	X	X	DAC1OW[12:0]													DAC1 overwrite
0C	R/W	0000	X	X	X	DAC2OW[12:0]													DAC2 overwrite
0E	R/W	0000	X	X	X	DAC3OW[12:0]													DAC3 overwrite
10	R/W	0000	X	X	X	CLM1OW[12:0]													CLAMP1 overwrite
12	R/W	0000	X	X	X	CLM2OW[12:0]													CLAMP2 overwrite
18	R	0000	0	0	0	CLM1[12:0]													CLAMP1
1A	R	0000	0	0	0	CLM2[12:0]													CLAMP2
20	R	0000	0	0	0	DAC0LUT[12:0]													DAC0 LUT
22	R	0000	0	0	0	DAC1LUT[12:0]													DAC1 LUT
24	R	0000	0	0	0	DAC2LUT[12:0]													DAC2 LUT
26	R	0000	0	0	0	DAC3LUT[12:0]													DAC3 LUT
30	R/W	0000	X	X	X	BRDCST[12:0]													Broadcast

ADVANCE INFORMATION

Table 7-8. SPI Page 4: LUT0 and LUT1 Configuration Register Map

ADDR (HEX)	TYPE	FACT (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*																REGISTER DESCRIPTION
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn48: –48°C
02	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn44: –44°C
04	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn40: –40°C
06	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn36: –36°C
08	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn32: –32°C
0A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn28: –28°C
0C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn24: –24°C
0E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn20: –20°C
10	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn16: –16°C
12	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn12: –12°C
14	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn8: –8°C
16	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAn4: –4°C
18	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp0: 0°C
1A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp4: 4°C
1C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp8: 8°C
1E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp12: 12°C
20	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp16: 16°C
22	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp20: 20°C
24	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp28: 28°C
26	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp32: 32°C
28	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp36: 36°C
2A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp40: 40°C
2C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp44: 44°C
2E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp48: 48°C
30	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp52: 52°C
32	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp56: 56°C
34	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp60: 60°C
36	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp64: 64°C
38	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp68: 68°C
3A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp72: 72°C
3C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp76: 76°C
3E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp80: 80°C
40	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp84: 84°C
42	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp88: 88°C
44	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp92: 92°C
46	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp96: 96°C
48	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp100: 100°C
4A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp104: 104°C

Table 7-8. SPI Page 4: LUT0 and LUT1 Configuration Register Map (continued)

ADDR (HEX)	TYPE	FACT (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*																REGISTER DESCRIPTION
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
4C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp108: 108°C
4E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp112: 112°C
50	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp116: 116°C
52	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp120: 120°C
54	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp124: 124°C
56	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp128: 128°C
58	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp132: 132°C
5A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp136: 136°C
5C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp140: 140°C
5E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp144: 144°C
60	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp148: 148°C
62	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC1[3:0]				DAC0[3:0]				DELTAp152: 152°C
64	R/W	0000	P	HAMM[3:0]				X	X	X	X	X	DAC0 POL	DAC0BASE[12:8]					DAC0 BASE (high)
66	R/W	0000	P	HAMM[3:0]				X	X	X	DAC0BASE[7:0]								DAC0 BASE (low)
68	R/W	0000	P	HAMM[3:0]				X	X	X	X	X	DAC1 POL	DAC1BASE[12:8]					DAC1 BASE (high)
6A	R/W	0000	P	HAMM[3:0]				X	X	X	DAC1BASE[7:0]								DAC1 BASE (low)

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Table 7-9. SPI Page 5: LUT2 and LUT3 Configuration Register Map

ADDR (HEX)	TYPE	FACT (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*																REGISTER DESCRIPTION
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn48: –48°C
02	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn44: –44°C
04	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn40: –40°C
06	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn36: –36°C
08	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn32: –32°C
0A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn28: –28°C
0C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn24: –24°C
0E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn20: –20°C
10	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn16: –16°C
12	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn12: –12°C
14	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn8: –8°C
16	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAn4: –4°C
18	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp0: 0°C
1A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp4: 4°C
1C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp8: 8°C
1E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp12: 12°C
20	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp16: 16°C
22	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp20: 20°C
24	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp28: 28°C
26	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp32: 32°C
28	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp36: 36°C
2A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp40: 40°C
2C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp44: 44°C
2E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp48: 48°C
30	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp52: 52°C
32	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp56: 56°C
34	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp60: 60°C
36	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp64: 64°C
38	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp68: 68°C
3A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp72: 72°C
3C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp76: 76°C
3E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp80: 80°C
40	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp84: 84°C
42	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp88: 88°C
44	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp92: 92°C
46	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp96: 96°C
48	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp100: 100°C
4A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp104: 104°C

Table 7-9. SPI Page 5: LUT2 and LUT3 Configuration Register Map (continued)

ADDR (HEX)	TYPE	FACT (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*																REGISTER DESCRIPTION
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
4C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp108: 108°C
4E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp112: 112°C
50	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp116: 116°C
52	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp120: 120°C
54	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp124: 124°C
56	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp128: 128°C
58	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp132: 132°C
5A	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp136: 136°C
5C	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp140: 140°C
5E	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp144: 144°C
60	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp148: 148°C
62	R/W	00FF	P	HAMM[3:0]				X	X	X	DAC3[3:0]				DAC2[3:0]				DELTAp152: 152°C
64	R/W	0000	P	HAMM[3:0]				X	X	X	X	X	DAC2 POL	DAC2BASE[12:8]					DAC2 BASE (high)
66	R/W	0000	P	HAMM[3:0]				X	X	X	DAC2BASE[7:0]								DAC2 BASE (low)
68	R/W	0000	P	HAMM[3:0]				X	X	X	X	X	DAC3 POL	DAC3BASE[12:8]					DAC3 BASE (high)
6A	R/W	0000	P	HAMM[3:0]				X	X	X	DAC3BASE[7:0]								DAC3 BASE (low)

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Table 7-10. SPI Page 15: Notepad Register Map

ADDR (HEX)	TYPE	FACT (HEX)	BIT DESCRIPTION *(Shaded Bits are not Stored in EEPROM)*																REGISTER DESCRIPTION
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	R/W	0000	PAD0[7:0]								PAD1[7:0]								Notepad 0-1
02	R/W	0000	PAD2[7:0]								PAD3[7:0]								Notepad 2-3
04	R/W	0000	PAD4[7:0]								PAD5[7:0]								Notepad 4-5
06	R/W	0000	PAD6[7:0]								PAD7[7:0]								Notepad 6-7
08	R/W	0000	PAD8[7:0]								PAD9[7:0]								Notepad 8-9
0A	R/W	0000	PAD10[7:0]								PAD11[7:0]								Notepad 10-11
0C	R/W	0000	PAD12[7:0]								PAD13[7:0]								Notepad 12-13
0E	R/W	0000	PAD14[7:0]								PAD15[7:0]								Notepad 14-15
10	R/W	0000	PAD16[7:0]								PAD17[7:0]								Notepad 16-17
12	R/W	0000	PAD18[7:0]								PAD19[7:0]								Notepad 18-19
7C	W	0000	EEBURN[7:0]								X	X	X	X	X	X	X	X	EEPROM burn

ADVANCE INFORMATION

7.3 Registers

7.3.1 I²C Registers

7.3.1.1 I²C Page 1: Device Configuration Register Information

7.3.1.1.1 Local Temperature High Byte Register (offset = 00h) [reset = N/A]

Figure 7-1. Local Temperature High Byte Register

7	6	5	4	3	2	1	0
LT[11:4]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-11. Local Temperature High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LT[11:4]	R	0h	Local temperature high byte. The resolution of the LSB in this register is 1°C. This register is read-only and is updated each time a temperature measurement is completed. When the full temperature value is needed, reading the high byte register first causes the low byte register value to be locked until the register is read. If the low byte is read first, then the high byte register value is locked until the register is read. With this mechanism, both bytes of the read operation come from the same temperature conversion, and remain valid only until another register is read. For proper operation, read the high byte of the temperature result first. Read the low byte register in the next read command; if the low byte is not needed, leave the register unread.

7.3.1.1.2 Local Temperature Low Byte Register (offset = 01h) [reset = N/A]

Figure 7-2. Local Temperature Low Byte Register

7	6	5	4	3	2	1	0
LT[3:0]				RESERVED			
R-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-12. Local Temperature Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	LT[3:0]	R	0h	Local temperature low byte. The resolution of the four bits in this register is 0.0625C. This register is read-only and is updated each time a temperature measurement is completed. When the full temperature value is needed, reading the high byte register first causes the low byte register value to be locked until the register is read. If the low byte is read first, then the high byte register value is locked until the register is read. With this mechanism, both bytes of the read operation come from the same temperature conversion, and remain valid only until another register is read. For proper operation, read the high byte of the temperature result first. Read the low byte register in the next read command; if the low byte is not needed, leave the register unread.

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7.3.1.1.3 Remote Temperature High Byte Register (offset = 02h) [reset = N/A]

Figure 7-3. Remote Temperature High Byte Register

7	6	5	4	3	2	1	0
RT[11:4]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-13. Remote Temperature High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RT[11:4]	R	0h	Remote temperature high byte. The resolution of the LSB in this register is 1°C. This register is read-only and is updated each time a temperature measurement is completed. When the full temperature value is needed, reading the high byte register first causes the low byte register value to be locked until the register is read. If the low byte is read first, then the high byte register value is locked until the register is read. With this mechanism, both bytes of the read operation come from the same temperature conversion, and remain valid only until another register is read. For proper operation, read the high byte of the temperature result first. Read the low byte register in the next read command; if the low byte is not needed, do not read the register.

7.3.1.1.4 Remote Temperature Low Byte Register (offset = 03h) [reset = N/A]

Figure 7-4. Remote Temperature Low Byte Register

7	6	5	4	3	2	1	0
RT[3:0]				RESERVED			
R-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-14. Remote Temperature Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RT[3:0]	R	0h	Remote temperature low byte. The resolution of the LSB in this register is 0.0625°C. This register is read-only and is updated each time a temperature measurement is completed. When the full temperature value is needed, reading the high byte register first causes the low byte register value to be locked until the register is read. If the low byte is read first, then the high byte register value is locked until the register is read. With this mechanism, both bytes of the read operation come from the same temperature conversion, and remain valid only until another register is read. For proper operation, read the high byte of the temperature result first. Read the low byte register in the next read command; if the low byte is not needed, leave the register unread. The resolution of these four bits is 0.0625°C.

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7.3.1.1.5 Temperature Status Register (offset = 04h) [reset = N/A]

Figure 7-5. Temperature Status Register

7	6	5	4	3	2	1	0
BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-15. Temperature Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSY	R	0h	Temperature ADC status indicator 1 = ADC is converting. 0 = ADC is not converting.
6	LHIGH	R	0h	Local temperature high limit status indicator 1 = Local temperature value exceeds the Local Temperature High Limit Register value. This bit is cleared upon reading the Temperature Status Register providing that the condition causing the over temperature result is no longer present. 0 = Local temperature value does not exceed the Local Temperature High Limit Register value.
5	LLOW	R	0h	Local temperature low limit status indicator 1 = Local temperature value is below the Local Temperature Low Limit Register value. This bit is cleared upon reading the Temperature Status Register providing that the condition causing the under temperature result is no longer present. 0 = Local temperature value is not below the Local Temperature Low Limit Register value.
4	RHIGH	R	0h	Remote temperature high limit status indicator 1 = Remote temperature value exceeds the Remote Temperature High Limit Register value. This bit is cleared upon reading the Temperature Status Register providing that the condition causing the over temperature result is no longer present. 0 = Remote temperature value does not exceed the Remote Temperature High Limit Register value.
3	RLOW	R	0h	Remote temperature low limit status indicator 1 = Remote temperature value is below the Remote Temperature Low Limit Register value. This bit is cleared upon reading the Temperature Status Register providing that the condition causing the under temperature result is no longer present. 0 = Remote temperature value is not below the Remote Temperature Low Limit Register value.
2	OPEN	R	0h	Remote junction open circuit detection 1 = The remote junction is an open circuit. This bit is cleared upon reading the Temperature Status Register providing that the condition causing the open circuit is no longer present. 0 = The remote junction is not an open circuit.

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7.3.1.1.6 AMC Status Register (offset = 05h) [reset = N/A]

Figure 7-6. AMC Status Register

7	6	5	4	3	2	1	0
TMPSTAT	PAON	EECRC	RESERVED	EERDY	DED	SEC	GAN
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-16. AMC Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TMPSTAT	R	0h	Temperature alarm status indicator 1 = Temperature alarm event issued. This bit clears automatically after the temperature alarm bits are cleared.
6	PAON	R	0h	PA_ON status indicator 1 = PA_ON pin is high. 0 = PA_ON pin is low.
5	EECRC	R	0h	EEPROM load CRC error indicator 1 = Indicates a CRC error during EEPROM load to the user register space. To clear this bit, write a 1.
3	EERDY	R	0h	EEPROM ready indicator 0 = The EEPROM BURN is in progress. 1 = The EEPROM BURN is complete.
2	DED	R	0h	Double error detection status indicator 1 = Double bit error detected when accessing a LUT register in the operating memory. Error not corrected. To clear this bit, write a 1.
1	SEC	R	0h	Single error correction status indicator 1 = Single bit error detected when accessing a LUT register in the operating memory. Error is corrected. To clear this bit, write a 1.
0	GAN	R	0h	GAN ready indicator 1 = The device is in negative output range operation. 0 = The device is in positive output range operation.

7.3.1.1.7 Software Reset Register (offset = 07h) [reset = 00h]

Figure 7-7. Software Reset Register

7	6	5	4	3	2	1	0
SOFTRST[7:0]							
W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-17. Software Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SOFTRST[7:0]	W	0h	Software reset command 0x05 = Writing 0x05 to this register initiates a reset event. 0xAD = Writing 0xAD to this register initiates a register clear event that returns all operating memory registers to factory-default values. Wait 15µs before the next serial interface command.

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7.3.1.1.8 Configuration 1 Register (offset = 08h) [reset = 01h]

Figure 7-8. Configuration 1 Register

7	6	5	4	3	2	1	0
RESERVED	TMPSD	ALERT/THERM	VSSRANGE	DACILMT	TMPRANGE	TMRCNT[1:0]	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-18. Configuration 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
6	TMPSD	R/W	0h	Temperature sensor shutdown control 1 = Places the temperature sensors in shutdown mode 0 = Places the temperature sensors in continuous conversion mode
5	ALERT/THERM	R/W	0h	ALERT or THERM temperature alarm mode select 1 = THERM mode 0 = ALERT mode
4	VSSRANGE	R/W	0h	V_{SS} auto-threshold detector control. Sets the valid V_{SS} supply range. Set to 0 if operating in positive output range. 1 = Wide V_{SS} Configuration: $-11V \le V_{SS} < -7V$ 0 = Narrow V_{SS} Configuration: $-7V \le V_{SS} \le -4.5V$
3	DACILMT	R/W	0h	DAC output current mode select 1 = High-current mode 0 = Normal-current mode
2	TMPRANGE	R/W	0h	This bit configures the range of the temperature measurement. *Use the selected range format for all temperature data registers (high and low limits, offset and overwrite).* 1 = –64°C to +191°C 0 = –40°C to +127°C
1:0	TMRCNT[1:0]	R/W	1h	Start-up timer select. Sets the wait time between the DAC outputs being set at start-up and the PA_ON release 00 = 1ms 01 = 15ms 10 = 30ms 11 = 60ms

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7.3.1.1.9 Configuration 2 Register (offset = 09h) [reset = 08h]

Figure 7-9. Configuration 2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	HAMMOFF	RESERVED	CR[3:0]			
R-0h	R-0h	R/W-0h	R-0h	R/W-8h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-19. Configuration 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	HAMMOFF	R/W	0h	Hamming-based SECDED module for LUT data access 0 = Enables the SECDED module 1 = Disables the SECDED module
3:0	CR[3:0]	R/W	8h	Conversion rate selection (see Table 7-20).

Table 7-20. Conversion Rate

VALUE	CONVERSIONS PER SECOND	TIME (SECONDS)
00h	0.0625	16
01h	0.125	8
02h	0.25	4
03h	0.5	2
04h	1	1
05h	2	0.5
06h	4	0.25
07h	8	0.125
08h	16 (default)	0.0625 (default)
09h	32	0.03125

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7.3.1.1.10 LUT Configuration Register (offset = 0Ah) [reset = 03h]

Figure 7-10. LUT Configuration Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LUTSTAT	LUTDIS	LUTSEL2	LUTSEL1	REN	LEN
R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-21. LUT Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
5	LUTSTAT	R	0h	LUT status indicator 0 = The LUT/ALU engine is disabled. 1 = The LUT/ALU engine is enabled.
4	LUTDIS	R/W	0h	LUT/ALU control 0 = Enables the LUT/ALU engine. 1 = Disables the LUT/ALU engine. The temperature sensor remains active. Disable the LUT/ALU engine during EEPROM access or register access to pages 4, 5 and 15.
3	LUTSEL2	R/W	0h	LUT2 and LUT3 temperature input 0 = Local temperature sensor. 1 = Remote temperature sensor.
2	LUTSEL1	R/W	0h	LUT0 and LUT1 temperature input 0 = Local temperature sensor. 1 = Remote temperature sensor.
1	REN	R/W	1h	Remote temperature sensor control 0 = Disables remote temperature sensor conversions. 1 = Enables remote temperature sensor conversions.
0	LEN	R/W	1h	Local temperature sensor control 0 = Disables local temperature sensor conversions. 1 = Enables local temperature sensor conversions.

7.3.1.1.11 DAC Overwrite Enable Register (offset = 0Bh) [reset = 00h]

Figure 7-11. DAC Overwrite Enable Register

7	6	5	4	3	2	1	0
BYP3	BYP2	BYP1	BYP0	DAC3OW	DAC2OW	DAC1OW	DAC0OW
R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-22. DAC Overwrite Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BYP3	R/W	0h	DACx ALU bypass control 0 = ALU output sent to DACx. 1 = Bypass the ALU output. Send BASEx value to DACx.
6	BYP2	R/W	0h	
5	BYP1	R/W	0h	
4	BYP0	R/W	0h	
3	DAC3OW	R/W	0h	DACx overwrite control 0 = DACx input is generated by LUT. 1 = DACx input is supplied by the serial interface accessible DACxOW[12:0] data register.
2	DAC2OW	R/W	0h	
1	DAC1OW	R/W	0h	
0	DAC0OW	R/W	0h	

ADVANCE INFORMATION

7.3.1.1.12 Drive Enable Register (offset: 0Ch) [reset = 00h]

Figure 7-12. Drive Enable Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	DRV3	DRV2	RESERVED	RESERVED	DRV1	DRV0
R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-23. Drive Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
5	DRV3	R/W	0h	DAC3 switch control if configured for software operation 0 = OFF voltage. 1 = ON voltage.
4	DRV2	R/W	0h	OUT2 switch control if configured for software operation 0 = OFF voltage. 1 = ON voltage.
1	DRV1	R/W	0h	OUT1 switch control if configured for software operation 0 = OFF voltage. 1 = ON voltage.
0	DRV0	R/W	0h	DAC0 switch control if configured for software operation 0 = OFF voltage. 1 = ON voltage.

7.3.1.1.13 Drive Enable Select Register (offset: 0Dh) [reset = 00h]

Figure 7-13. Drive Enable Select Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	DRVSEL3	DRVSEL2	RESERVED	RESERVED	DRVSEL1	DRVSEL0
R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-24. Drive Enable Select Register Field Descriptions

Bit	Field	Type	Reset	Description
5	DRVSEL3	R/W	0h	DAC3 switch control select 0 = DRVEN2 pin. 1 = DRV3 bit.
4	DRVSEL2	R/W	0h	OUT2 switch control select 0 = DRVEN2 pin. 1 = DRV2 bit.
1	DRVSEL1	R/W	0h	OUT1 software switch control 0 = DRVEN1 pin. 1 = DRV1 bit.
0	DRVSEL0	R/W	0h	DAC0 software switch control 0 = DRVEN1 pin. 1 = DRV0 bit.

ADVANCE INFORMATION

7.3.1.1.14 Alarm Configuration Register (offset: 0Eh) [reset = 4Fh]

Figure 7-14. Alarm Configuration Register

7	6	5	4	3	2	1	0
ALMINEN	PAONDIS	RESERVED	RESERVED	DAC3OFF	OUT2OFF	OUT1OFF	DAC0OFF
R/W-0h	R/W-1h	R-0h	R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-25. Alarm Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALMINEN	R/W	0h	$\overline{\text{ALARMIN}}$ functionality for $\overline{\text{RESET}}$ pin 1 = $\overline{\text{ALARMIN}}$. 0 = $\overline{\text{RESET}}$.
6	PAONDIS	R/W	1h	PA_ON alarm control 0 = PA_ON is unaffected by an alarm event. 1 = PA_ON is set low during an alarm event.
3	DAC3OFF	R/W	1h	DAC3 alarm control 0 = DAC3 is unaffected by an alarm event. 1 = DAC3 is switched OFF during an alarm event.
2	OUT2OFF	R/W	1h	OUT2 alarm control 0 = OUT2 is unaffected by an alarm event. 1 = OUT2 is switched OFF during an alarm event.
1	OUT1OFF	R/W	1h	OUT1 alarm control 0 = OUT1 is unaffected by an alarm event. 1 = DAC3 is switched OFF during an alarm event.
0	DAC2OFF	R/W	1h	DAC0 alarm control 0 = DAC0 is unaffected by an alarm event. 1 = DAC0 is switched OFF during an alarm event.

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7.3.1.1.15 Interrupt Mode Register (offset = 0Fh) [reset = 00h]

Figure 7-15. Interrupt Mode Register

7	6	5	4	3	2	1	0
RESETCMD[1:0]		RESERVED	AMCINT	DRVENRLS	PAONRLS	DACHCRLS	DACRLS
R/W-0h		R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-26. Interrupt Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESETCMD[1:0]	R/W	0h	Reset command 00 = No operation. 01 = Wait for end of temperature conversion. 10 = Release DACs. 11 = Release DACs from start-up current mode.
4	AMCINT	R/W	0h	AMC interrupt mode 0 = Normal operation. 1 = Sets device in interrupt mode where the automatic reset control signals are ignored.
3	DRVENRLS	R/W	0h	DRVEN control when device is set in interrupt mode 0 = Forces all internal DRVEN switch control signals to zero. 1 = Enables control of the DRVEN signals.
2	PAONRLS	R/W	1h	PA_ON control when device is set in interrupt mode 0 = PA_ON pin is forced low. 1 = PA_ON pin is forced high.
1	DACHCRLS	R/W	1h	DAC output current control when device is set in interrupt mode 0 = DACs are forced into start-up current mode. 1 = DACs are released from start-up current mode.
0	DACRLS	R/W	1h	DAC output control when device is set in interrupt mode 0 = DACs input code is forced to all zeros. 1 = DACs input code can be accessed.

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7.3.1.1.16 Local Temperature High Limit Register (offset = 10h) [reset = 7Fh]

Figure 7-16. Local Temperature High Limit Register

7	6	5	4	3	2	1	0
LTHL[11:4]							
R/W-7Fh							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-27. Local Temperature High Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LTHL[11:4]	R/W	7Fh	These bits determine the value of the high temperature limit to which the local temperature measurement is compared. The resolution of the LSB in this register is 1°C. Format denoted by the TMPRANGE bit.

7.3.1.1.17 Local Temperature Low Limit Register (offset = 11h) [reset = 80h]

Figure 7-17. Local Temperature Low Limit Register

7	6	5	4	3	2	1	0
LTLL[11:4]							
R/W-80h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-28. Local Temperature Low Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LTLL[11:4]	R/W	80h	These bits determine the value of the low temperature limit to which the local temperature measurement is compared. The resolution of the LSB in this register is 1°C. Format denoted by the TMPRANGE bit.

7.3.1.1.18 Remote Temperature High Limit High Byte Register (offset = 12h) [reset = 7Fh]

Figure 7-18. Remote Temperature High Limit High Byte Register

7	6	5	4	3	2	1	0
RTHL[11:4]							
R/W-7Fh							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-29. Remote Temperature High Limit High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RTHL[11:4]	R/W	7Fh	These bits determine the value of the high byte of the high temperature limit to which the remote temperature measurement is compared. The resolution of the LSB in this register is 1°C. Format denoted by the TMPRANGE bit.

7.3.1.1.19 Remote Temperature High Limit Low Byte Register (offset = 13h) [reset = F0h]

Figure 7-19. Remote Temperature High Limit Low Byte Register

7	6	5	4	3	2	1	0
RTHL[3:0]				RESERVED			
R/W-Fh				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-30. Remote Temperature High Limit Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RTHL[3:0]	R/W	Fh	These bits determine the value of the low byte of the high temperature limit to which the remote temperature measurement is compared. The resolution of the four bits in this register is 0.0625°C. Format denoted by the TMPRANGE bit.

7.3.1.1.20 Remote Temperature Low Limit High Byte Register (offset = 14h) [reset = 80h]

Figure 7-20. Remote Temperature Low Limit High Byte Register

7	6	5	4	3	2	1	0
RTLL[11:4]							
R/W-80h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-31. Remote Temperature Low Limit High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RTLL[11:4]	R/W	80h	These bits determine the value of high byte of the low temperature limit to which the remote temperature measurement is compared. The resolution of the LSB in this register is 1°C. Format denoted by the TMPRANGE bit.

7.3.1.1.21 Remote Temperature Low Limit Low Byte Register (offset = 15h) [reset = 00h]

Figure 7-21. Remote Temperature Low Limit Low Byte Register

7	6	5	4	3	2	1	0
RTLL[3:0]				RESERVED			
R/W-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-32. Remote Temperature Low Limit Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RTLL[3:0]	R/W	0h	These bits determine the value of the low byte of the low temperature limit to which the remote temperature measurement is compared. The resolution of the four bits in this register is 0.0625°C. Format denoted by the TMPRANGE bit.

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7.3.1.1.22 Remote Temperature Offset High Byte Register (offset = 16h) [reset = 00h]

Figure 7-22. Remote Temperature Offset High Byte Register

7	6	5	4	3	2	1	0
RTOS[11:4]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-33. Remote Temperature Offset High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RTOS[11:4]	R/W	0h	Remote temperature offset high byte. The value of this register is added to the value the ADC conversion with the result stored in the remote temperature register. This register is used to add or subtract a temperature offset value to the ADC conversion result in applications requiring calibration. The resolution of the LSB in this register is 1°C. Format denoted by the TMPRANGE bit.

7.3.1.1.23 Remote Temperature Offset Low Byte Register (offset = 17h) [reset = 00h]

Figure 7-23. Remote Temperature Offset Low Byte Register

7	6	5	4	3	2	1	0
RTOS[3:0]				RESERVED			
R/W-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-34. Remote Temperature Offset Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RTOS[3:0]	R/W	0h	Remote temperature offset low byte. The value of this register is added to the value the ADC conversion with the result stored in the remote temperature register. This register is used to add or subtract a temperature offset value to the ADC conversion result in applications requiring calibration. The resolution of these four bits is 0.0625°C. Format denoted by the TMPRANGE bit.

7.3.1.1.24 THERM Hysteresis Register (offset = 1Ah) [reset = 0Ah]

Figure 7-24. THERM Hysteresis Register

7	6	5	4	3	2	1	0
HYS[11:4]							
R/W-Ah							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-35. THERM Hysteresis Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	HYS[11:4]	R/W	Ah	THERM hysteresis value. These bits determine the amount of hysteresis applied to the THERM function. The resolution of the LSB in this register is 1°C.

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7.3.1.1.25 Consecutive ALERT Register (offset = 1Bh) [reset = 01h]

Figure 7-25. Consecutive ALERT Register

7	6	5	4	3	2	1	0
RESERVED				CONAL[2:0]			RESERVED
R-0h				R/W-0h			R-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-36. Consecutive ALERT Register Field Descriptions

Bit	Field	Type	Reset	Description
3:1	CONAL[2:0]	R/W	0h	Number of consecutive out-of-limit measurements required to activate an ALERT temperature alarm.

Table 7-37. Consecutive Alert Configuration

VALUE	NUMBER OF CONSECUTIVE OUT-OF-LIMIT MEASUREMENTS REQUIRED
0h	1
1h	2
3h	3
7h	4

7.3.1.1.26 η-Factor Correction Register (offset = 1Ch) [reset = 00h]

Figure 7-26. η-Factor Correction Register

7	6	5	4	3	2	1	0
NC[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-38. η-Factor Correction Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NC[7:0]	R/W	0h	η-factor value.

Table 7-39. η-Factor Range

N_{ADJUST}			η
BINARY	HEX	DECIMAL	
0111 1111	7F	127	0.950205
0000 1010	0A	10	1.003195
0000 1000	08	8	1.004153
0000 0110	06	6	1.005112
0000 0100	04	4	1.006073
0000 0010	02	2	1.007035
0000 0001	01	1	1.007517
0000 0000	00	0	1.008
1111 1111	FF	–1	1.008483
1111 1110	FE	–2	1.008966
1111 1100	FC	–4	1.009935
1111 1010	FA	–6	1.010905
1111 1000	F8	–8	1.011877
1111 0110	F6	–10	1.012851
1000 0000	80	–128	1.073829

ADVANCE INFORMATION

7.3.1.1.27 Digital Filter Control Register (offset = 1Dh) [reset = 00h]

Figure 7-27. Digital Filter Control Register

7	6	5	4	3	2	1	0
RESERVED						DF[1:0]	
R-0h						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-40. Digital Filter Control Register Field Descriptions

Bit	Field	Type	Reset	Description
1:0	DF[1:0]	R/W	0h	Configures the amount of filtering for the remote temperature results.

Table 7-41. Digital Filter Configuration

VALUE	NUMBER OF REMOTE TEMPERATURE MEASUREMENTS AVERAGED
0h	Averaging off
1h	4
2h	8
4h	not used

7.3.1.1.28 Version ID Register (offset = 1Eh) [reset = 00h]

Figure 7-28. Version ID Register

7	6	5	4	3	2	1	0
VERSION[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-42. Version ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VERSION[7:0]	R	0h	Device version ID. **Subject to change.**

7.3.1.1.29 Device ID Register (offset = 1Fh) [reset = A3h]

Figure 7-29. Device ID Register

7	6	5	4	3	2	1	0
ID[7:0]							
R-A3h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-43. Device ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ID[7:0]	R	A3h	Device identification information.

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7.3.1.1.30 Temperature Overwrite High Byte Register (offset = 22h) [reset = 00h]

Figure 7-30. Temperature Overwrite High Byte Register

7	6	5	4	3	2	1	0
TEMPOW[11:4]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-44. Temperature Overwrite High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMPOW[11:4]	R/W	0h	Temperature sensor overwrite value high byte. Format denoted by the TMPRANGE bit.

7.3.1.1.31 Temperature Overwrite Low Byte Register (offset = 23h) [reset = 00h]

Figure 7-31. Temperature Overwrite Low Byte Register

7	6	5	4	3	2	1	0
TEMPOW[3:0]				RESERVED			TEMPOW
R/W-0h				R-0h			R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-45. Temperature Overwrite Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TEMPOW[3:0]	R/W	0h	Temperature sensor overwrite value low byte. Format denoted by the TMPRANGE bit.
0	TEMPOW	R/W	0h	Temperature sensor overwrite control 0 = The temperature sensor outputs are used to index the LUT. 1 = The serial interface accessible TEMPOW[11:0] data register is used to index the LUT.

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7.3.1.1.32 Reset Status Register (offset = 24h) [reset = N/A]

Figure 7-32. Reset Status Register

7	6	5	4	3	2	1	0
RESERVED				RESETSTA[3:0]			
R-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-46. Reset Status Register Field Descriptions

Bit	Field	Type	Reset	Description
3:0	RESETSTA[3:0]	R	0h	Reset control status. Read the register twice for data validation. If two consecutive readings do not match, issue additional read commands until the data are equivalent.

Table 7-47. Reset Control Status

VALUE	STATE
0h	Idle
1h	Wait for device start
2h	EEPROM load start
3h	EEPROM load in progress
4h	Interrupt mode
5h	Check for valid output buffer supply ranges
6h	Temperature conversion in progress
7h	Wait for LUT/ALU
8h	Wait for alarm event
9h	Release DACs from all zero-code
Ah	Wait for timer between DACs and PA_ON assert
Bh	Release DACs from start-up current mode
Ch	Set PA_ON
Dh	Release DRVEN switch controls
Eh	Alarm event
Fh	Reserved

7.3.1.1.33 One-Shot Temperature Register (offset = 28h) [reset = 00h]

Figure 7-33. One-Shot Temperature Register

7	6	5	4	3	2	1	0
TEMPONE[7:0]							
W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-48. One-Shot Temperature Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMPONE[7:0]	W	0h	When the temperature sensor is in shutdown mode, write any value to this register to trigger a one-shot temperature conversion.

7.3.1.1.34 Software Alarm Register (offset = 2Ah) [reset = 00h]

Figure 7-34. Software Alarm Register

7	6	5	4	3	2	1	0
RESERVED							SWALM
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-49. Software Alarm Register Field Descriptions

Bit	Field	Type	Reset	Description
0	SWALM	R/W	0h	Software Alarm 1 = Setting the SWALM bit initiates an alarm event. The alarm condition persists until the bit is cleared to 0.

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7.3.1.2 I²C Page 2: DAC Configuration Register Information

7.3.1.2.1 DAC0 Input Data Register (offset = 00h - 01h) [reset = 00h]

ADDRESS	NAME
0x00	DAC0 (high byte)
0x01	DAC0 (low byte)

Figure 7-35. DAC0 Input Data High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC0[12:8]				
R-0	R-0	R-0	R-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-50. DAC0 Input Data High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC0[12:8]	R	0h	DAC0[12:8] input data.

Figure 7-36. DAC0 Input Data Low Byte Register

7	6	5	4	3	2	1	0
DAC0[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-51. DAC0 Input Data Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC0[7:0]	R	0h	DAC0[7:0] input data.

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7.3.1.2.2 DAC1 Input Data Register (offset = 02h - 03h) [reset = 00h]

ADDRESS	NAME
0x02	DAC1 (high byte)
0x03	DAC1 (low byte)

Figure 7-37. DAC1 Input Data High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC1[12:8]				
R-0	R-0	R-0	R-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-52. DAC1 Input Data High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC1[12:8]	R	0h	DAC1[12:8] input data.

Figure 7-38. DAC1 Input Data Low Byte Register

7	6	5	4	3	2	1	0
DAC1[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-53. DAC1 Input Data Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC1[7:0]	R	0h	DAC1[7:0] input data.

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7.3.1.2.3 DAC2 Input Data Register (offset = 04h - 05h) [reset = 00h]

ADDRESS	NAME
0x04	DAC2 (high byte)
0x05	DAC2 (low byte)

Figure 7-39. DAC2 Input Data High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC2[12:8]				
R-0	R-0	R-0	R-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-54. DAC2 Input Data High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC2[12:8]	R	0h	DAC2[12:8] input data.

Figure 7-40. DAC2 Input Data Low Byte Register

7	6	5	4	3	2	1	0
DAC2[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-55. DAC2 Input Data Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC2[7:0]	R	0h	DAC2[7:0] input data.

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7.3.1.2.4 DAC3 Input Data Register (offset = 06h - 07h) [reset = 00h]

ADDRESS	NAME
0x06	DAC3 (high byte)
0x07	DAC3 (low byte)

Figure 7-41. DAC3 Input Data High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC3[12:8]				
R-0	R-0	R-0	R-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-56. DAC3 Input Data High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC3[12:8]	R	0h	DAC3[12:8] input data.

Figure 7-42. DAC3 Input Data Low Byte Register

7	6	5	4	3	2	1	0
DAC3[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-57. DAC3 Input Data Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC3[7:0]	R	0h	DAC3[7:0] input data.

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7.3.1.2.5 DAC0 Overwrite Register (offset = 08h - 09h) [reset = 00h]

ADDRESS	NAME
0x08	DAC0 Overwrite (high byte)
0x09	DAC0 Overwrite (low byte)

Figure 7-43. DAC0 Overwrite High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC0OW[12:8]				
R-0	R-0	R-0	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-58. DAC0 Overwrite High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC0OW[12:8]	R/W	0h	DAC0[12:8] overwrite data. Data are updated after the low byte is written. Write high byte data first.

Figure 7-44. DAC0 Overwrite Low Byte Register

7	6	5	4	3	2	1	0
DAC0OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-59. DAC0 Overwrite Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC0OW[7:0]	R/W	0h	DAC0[7:0] overwrite data. Data are updated after the low byte is written. Write high byte data first.

ADVANCE INFORMATION

7.3.1.2.6 DAC1 Overwrite Register (offset = 0Ah - 0Bh) [reset = 00h]

ADDRESS	NAME
0x0A	DAC1 Overwrite (high byte)
0x0B	DAC1 Overwrite (low byte)

Figure 7-45. DAC1 Overwrite High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC1OW[12:8]				
R-0	R-0	R-0	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-60. DAC1 Overwrite High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC1OW[12:8]	R/W	0h	DAC1[12:8] overwrite data. Data are updated after the low byte is written. Write high byte data first.

Figure 7-46. DAC1 Overwrite Low Byte Register

7	6	5	4	3	2	1	0
DAC1OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-61. DAC1 Overwrite Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC1OW[7:0]	R/W	0h	DAC1[7:0] overwrite data. Data are updated after the low byte is written. Write high byte data first.

ADVANCE INFORMATION

7.3.1.2.7 DAC2 Overwrite Register (offset = 0Ch - 0Dh) [reset = 00h]

ADDRESS	NAME
0x0C	DAC2 Overwrite (high byte)
0x0C	DAC2 Overwrite (low byte)

Figure 7-47. DAC2 Overwrite High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC2OW[12:8]				
R-0	R-0	R-0	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-62. DAC2 Overwrite High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC2OW[12:8]	R/W	0h	DAC2[12:8] overwrite data. Data are updated after the low byte is written. Write high byte data first.

Figure 7-48. DAC2 Overwrite Low Byte Register

7	6	5	4	3	2	1	0
DAC2OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-63. DAC2 Overwrite Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC2OW[7:0]	R/W	0h	DAC2[7:0] overwrite data. Data are updated after the low byte is written. Write high byte data first.

ADVANCE INFORMATION

7.3.1.2.8 DAC3 Overwrite Register (offset = 0Eh - 0Fh) [reset = 00h]

ADDRESS	NAME
0x0E	DAC3 Overwrite (high byte)
0x0F	DAC3 Overwrite (low byte)

Figure 7-49. DAC3 Overwrite High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC3OW[12:8]				
R-0	R-0	R-0	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-64. DAC3 Overwrite High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC3OW[12:8]	R/W	0h	DAC3[12:8] overwrite data. Data are updated after the low byte is written. Write high byte data first.

Figure 7-50. DAC3 Overwrite Low Byte Register

7	6	5	4	3	2	1	0
DAC3OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-65. DAC3 Overwrite Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC3OW[7:0]	R/W	0h	DAC3[7:0] overwrite data. Data are updated after the low byte has been written. Write high byte data first.

ADVANCE INFORMATION

7.3.1.2.9 CLAMP1 Overwrite Register (offset: 10h - 11h) [reset = 00h]

ADDRESS	NAME
0x10	CLAMP1 Overwrite (high byte)
0x11	CLAMP1 Overwrite (low byte)

Figure 7-51. CLAMP1 Overwrite High Byte Register

7	6	5	4	3	2	1	0
0	0	0	CLM1OW[12:8]				
R-0	R-0	R-0	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-66. CLAMP1 Overwrite High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	CLM1OW[12:8]	R/W	0h	CLAMP1[12:8] overwrite data. Data are updated after the low byte is written. Write high byte data first.

Figure 7-52. CLAMP1 Overwrite Low Byte Register

7	6	5	4	3	2	1	0
CLM1OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-67. CLAMP1 Overwrite Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CLM1OW[7:0]	R/W	0h	CLAMP1[7:0] overwrite data. Data are updated after the low byte is written. Write high byte data first.

ADVANCE INFORMATION

7.3.1.2.10 CLAMP2 Overwrite Register (offset: 12h - 13h) [reset = 00h]

ADDRESS	NAME
0x12	CLAMP2 Overwrite (high byte)
0x13	CLAMP2 Overwrite (low byte)

Figure 7-53. CLAMP2 Overwrite High Byte Register

7	6	5	4	3	2	1	0
0	0	0	CLM2OW[12:8]				
R-0	R-0	R-0	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-68. CLAMP2 Overwrite High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	CLM2OW[12:8]	R/W	0h	CLAMP2[12:8] overwrite data. Data are updated after the low byte is written. Write high byte data first.

Figure 7-54. CLAMP2 Overwrite Low Byte Register

7	6	5	4	3	2	1	0
CLM2OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-69. CLAMP2 Overwrite Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CLM2OW[7:0]	R/W	0h	CLAMP2[7:0] overwrite data. Data are updated after the low byte is written. Write high byte data first.

ADVANCE INFORMATION

7.3.1.2.11 CLAMP1 Input Data Register (offset: 18h - 19h) [reset = 00h]

ADDRESS	NAME
0x18	CLAMP1 (high byte)
0x19	CLAMP1 (low byte)

Figure 7-55. CLAMP1 Input Data High Byte Register

7	6	5	4	3	2	1	0
0	0	0	CLM1[12:8]				
R-0	R-0	R-0	R-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-70. CLAMP1 Input Data High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	CLM1[12:8]	R	0h	CLAMP1[12:8] input data.

Figure 7-56. CLAMP1 Input Data Low Byte Register

7	6	5	4	3	2	1	0
CLM1[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-71. CLAMP1 Input Data Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CLM1[7:0]	R	0h	CLAMP1[7:0] input data.

7.3.1.2.12 CLAMP2 Input Data Register (offset: 1Ah - 1Bh) [reset = 00h]

ADDRESS	NAME
0x1A	CLAMP2 (high byte)
0x1B	CLAMP2 (low byte)

Figure 7-57. CLAMP2 Input Data High Byte Register

7	6	5	4	3	2	1	0
0	0	0	CLM2[12:8]				
R-0	R-0	R-0	R-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-72. CLAMP2 Input Data High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	CLM2[12:8]	R	0h	CLAMP2[12:8] input data.

Figure 7-58. CLAMP2 Input Data Low Byte Register

7	6	5	4	3	2	1	0
CLM2[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-73. CLAMP2 Input Data Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CLM2[7:0]	R	0h	CLAMP2[7:0] input data.

ADVANCE INFORMATION

7.3.1.2.13 DAC0 LUT Data Register (offset = 20h - 21h) [reset = 00h]

ADDRESS	NAME
0x20	DAC0 LUT (high byte)
0x21	DAC0 LUT (low byte)

Figure 7-59. DAC0 LUT Data High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC0LUT[12:8]				
R-0	R-0	R-0	R-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-74. DAC0 LUT Data High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC0LUT[12:8]	R	0h	DAC0[12:8] LUT data.

Figure 7-60. DAC0 LUT Data Low Byte Register

7	6	5	4	3	2	1	0
DAC0LUT[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-75. DAC0 LUT Data Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC0LUT[7:0]	R	0h	DAC0[7:0] LUT data.

ADVANCE INFORMATION

7.3.1.2.14 DAC1 LUT Data Register (offset = 22h - 23h) [reset = 00h]

ADDRESS	NAME
0x22	DAC1 LUT (high byte)
0x23	DAC1 LUT (low byte)

Figure 7-61. DAC1 LUT Data High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC1LUT[12:8]				
R-0	R-0	R-0	R-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-76. DAC1 LUT Data High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC1LUT[12:8]	R	0h	DAC1[12:8] LUT data.

Figure 7-62. DAC1 LUT Data Low Byte Register

7	6	5	4	3	2	1	0
DAC1LUT[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-77. DAC1 LUT Data Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC1LUT[7:0]	R	0h	DAC1[7:0] LUT data.

ADVANCE INFORMATION

7.3.1.2.15 DAC2 LUT Data Register (offset = 24h - 25h) [reset = 00h]

ADDRESS	NAME
0x24	DAC2 LUT (high byte)
0x25	DAC2 LUT (low byte)

Figure 7-63. DAC2 LUT Data High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC2LUT[12:8]				
R-0	R-0	R-0	R-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-78. DAC2 LUT Data High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC2LUT[12:8]	R	0h	DAC2[12:8] LUT data.

Figure 7-64. DAC2 LUT Data Low Byte Register

7	6	5	4	3	2	1	0
DAC2LUT[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-79. DAC2 LUT Data Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC2LUT[7:0]	R	0h	DAC2[7:0] LUT data.

ADVANCE INFORMATION

7.3.1.2.16 DAC3 LUT Data Register (offset = 26h - 27h) [reset = 00h]

ADDRESS	NAME
0x26	DAC3 LUT (high byte)
0x27	DAC3 LUT (low byte)

Figure 7-65. DAC3 LUT Data High Byte Register

7	6	5	4	3	2	1	0
0	0	0	DAC3LUT[12:8]				
R-0	R-0	R-0	R-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-80. DAC3 LUT Data High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	DAC3LUT[12:8]	R	0h	DAC3[12:8] LUT data.

Figure 7-66. DAC3 LUT Data Low Byte Register

7	6	5	4	3	2	1	0
DAC3LUT[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-81. DAC3 LUT Data Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC3LUT[7:0]	R	0h	DAC3[7:0] LUT data.

ADVANCE INFORMATION

7.3.1.2.17 Broadcast Register (offset = 30h - 31h) [reset = 00h]

ADDRESS	NAME
0x30	Broadcast (high byte)
0x31	Broadcast (low byte)

Figure 7-67. Broadcast High Byte Register

7	6	5	4	3	2	1	0
0	0	0	BRDCST[12:8]				
R-0	R-0	R-0	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-82. Broadcast High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
4:0	BRDCST[12:8]	R/W	0h	BRDCST[12:8] data sent to all DAC channels (DAC[0:3] and CLAMP[1:2]) simultaneously.

Figure 7-68. Broadcast Low Byte Register

7	6	5	4	3	2	1	0
BRDCST[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-83. Broadcast Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BRDCST[7:0]	R/W	0h	BRDCST[7:0] data sent to all DAC channels (DAC[0:3] and CLAMP[1:2]) simultaneously.

ADVANCE INFORMATION

7.3.1.3 I²C Page 4: LUT0 and LUT1 Configuration Register Information

Page 4 stores the LUT0 and LUT1 values at locations corresponding to 4°C increments from –48°C to +152°C. There is no increment corresponding to 24°C because this temperature is a BASELINE, and the corresponding LUT value is the 13-bit BASE.

Each odd address row stores a pair of DELTA registers. The LUT requires the DELTA values to represent a monotonic function. The function is either increasing or decreasing, and is determined by the POL bit in each DAC BASE register. DELTA values are unsigned. Each even address contains the SECDED parity and Hamming bits for the corresponding odd address.

The BASE values for DAC0 and DAC1, along with the corresponding SECDED codes are stored in addresses 0x64 to 0x6B.

The required method for updating the LUT entries is to disable the LUT, update the entries, and then enable the LUT.

7.3.1.3.1 DELTA HAMM Registers (offset = 00h - 63h) [reset = 00h (even addresses), FFh (odd addresses)]

ADDRESS	NAME
0x00	HAMMn48 (–48°C)
0x01	DELTAn48 (–48°C)
0x02	HAMMn44 (–44°C)
0x03 ↓ 0x22	DELTAn44 (–44°C) ↓ HAMMp20 (20°C)
0x23	DELTAp20 (20°C)
0x24	HAMMp28 (28°C)
0x25 ↓ 0x60	DELTAp28 (28°C) ↓ HAMMp148 (148°C)
0x61	DELTAp148 (148°C)
0x62	HAMMp152 (152°C)
0x63	DELTAp152 (152°C)

Figure 7-69. HAMM Register

7	6	5	4	3	2	1	0
P	HAMM[3:0]				X	X	X
R/W-0h	R/W-0h				R-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-84. HAMM Register Field Descriptions

Bit	Field	Type	Reset	Description
7	P	R/W	0h	Parity bit
6:3	HAMM[3:0]	R/W	0h	Hamming bits

Figure 7-70. DELTA Register

7	6	5	4	3	2	1	0
DAC1[3:0]				DAC0[3:0]			
R/W-Fh				R/W-Fh			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-85. DELTA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DAC1[3:0]	R/W	Fh	4-bit LUT1 entry
3:0	DAC0[3:0]	R/W	Fh	4-bit LUT0 entry

ADVANCE INFORMATION

7.3.1.3.2 DAC0 BASE HAMM Registers (offset = 64h - 67h) [reset = 00h]

ADDRESS	NAME
0x64	HAMM BASE0 High
0x65	DAC0 BASE (high byte)
0x66	HAMM BASE0 Low
0x67	DAC0 BASE (low byte)

Figure 7-71. HAMM BASE0 (High/Low) Register

7	6	5	4	3	2	1	0
P	HAMM[3:0]				X	X	X
R/W-0h	R/W-0h				R-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-86. HAMM BASE0 (High/Low) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	P	R/W	0h	Parity bit
6:3	HAMM[3:0]	R/W	0h	Hamming bits

Figure 7-72. DAC0 BASE Register (high byte)

7	6	5	4	3	2	1	0
X	X	DAC0POL	DAC0BASE[12:8]				
R-0h	R-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-87. DAC0 BASE Register (High Byte) Field Descriptions

Bit	Field	Type	Reset	Description
5	DAC0POL	R/W	0h	LUT increment polarity control: 1: This setting realizes a monotonically decreasing LUT transfer function. 0: This setting realizes a monotonically increasing LUT transfer function.
4:0	DAC0BASE[12:8]	R/W	0h	LUT BASE value bits [12:8] (LUT output at +24°C).

Figure 7-73. DAC0 BASE Register (Low Byte)

7	6	5	4	3	2	1	0
DAC0BASE[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-88. DAC0 BASE Register (Low Byte) Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC0BASE[7:0]	R/W	0h	LUT BASE value bits [7:0] (LUT output at +24°C).

7.3.1.3.3 DAC1 BASE HAMM Registers (offset = 68h - 6Bh) [reset = 00h]

ADDRESS	NAME
0x68	HAMM BASE1 High
0x69	DAC1 BASE (high byte)
0x6A	HAMM BASE1 Low
0x6B	DAC1 BASE (low byte)

Figure 7-74. HAMM BASE1 (High/Low) Register

7	6	5	4	3	2	1	0
P	HAMM[3:0]				X	X	X
R/W-0h	R/W-0h				R-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-89. HAMM BASE1 (High/Low) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	P	R/W	0h	Parity bit
6:3	HAMM[3:0]	R/W	0h	Hamming bits

Figure 7-75. DAC1 BASE Register (high byte)

7	6	5	4	3	2	1	0
X	X	DAC1POL	DAC1BASE[12:8]				
R-0h	R-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-90. DAC1 BASE Register (High Byte) Field Descriptions

Bit	Field	Type	Reset	Description
5	DAC1POL	R/W	0h	LUT increment polarity control: 1: This setting realizes a monotonically decreasing LUT transfer function. 0: This setting realizes a monotonically increasing LUT transfer function.
4:0	DAC1BASE[12:8]	R/W	0h	LUT BASE value bits [12:8] (LUT output at +24°C).

Figure 7-76. DAC1 BASE Register (Low Byte)

7	6	5	4	3	2	1	0
DAC1BASE[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-91. DAC1 BASE Register (Low Byte) Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC1BASE[7:0]	R/W	0h	LUT BASE value bits [7:0] (LUT output at +24°C).

ADVANCE INFORMATION

7.3.1.4 I²C Page 5: LUT2 and LUT3 Configuration Register Information

Page 5 stores the LUT2 and LUT3 values at locations corresponding to 4°C increments from –48°C to +152°C. There is no increment corresponding to 24°C because this temperature is a BASELINE, and the corresponding LUT value is the 13-bit BASE.

Each odd address row stores a pair of DELTA registers. The LUT requires the DELTA values to represent a monotonic function. The function is either increasing or decreasing, and is determined by the POL bit in each DAC BASE register. DELTA values are unsigned. Each even address contains the SECDED parity and Hamming bits for the corresponding odd address.

The BASE values for DAC2 and DAC3, along with the corresponding SECDED codes are stored in addresses 0x64 to 0x6B.

The required method for updating the LUT entries is to disable the LUT, update the entries, and then enable the LUT.

7.3.1.4.1 DELTA HAMM Registers (offset = 00h - 63h) [reset = 00h (even addresses, FFh (odd addresses)]

ADDRESS	NAME
0x00	HAMMn48 (–48°C)
0x01	DELTAn48 (–48°C)
0x02	HAMMn44 (–44°C)
0x03 ↓ 0x22	DELTAn44 (–44°C) ↓ HAMMp20 (20°C)
0x23	DELTAp20 (20°C)
0x24	HAMMp28 (28°C)
0x25 ↓ 0x60	DELTAp28 (28°C) ↓ HAMMp148 (148°C)
0x61	DELTAp148 (148°C)
0x62	HAMMp152 (152°C)
0x63	DELTAp152 (152°C)

Figure 7-77. HAMM Register

7	6	5	4	3	2	1	0
P	HAMM[3:0]				X	X	X
R/W-0h	R/W-0h				R-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-92. HAMM Register Field Descriptions

Bit	Field	Type	Reset	Description
7	P	R/W	0h	Parity bit
6:3	HAMM[3:0]	R/W	0h	Hamming bits

Figure 7-78. DELTA Register

7	6	5	4	3	2	1	0
DAC3[3:0]				DAC2[3:0]			
R/W-Fh				R/W-Fh			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-93. DELTA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DAC3[3:0]	R/W	Fh	4-bit LUT3 entry
3:0	DAC2[3:0]	R/W	Fh	4-bit LUT2 entry

ADVANCE INFORMATION

7.3.1.4.2 DAC2 BASE HAMM Registers (offset = 64h - 67h) [reset = 00h]

ADDRESS	NAME
0x64	HAMM BASE2 High
0x65	DAC2 BASE (high byte)
0x66	HAMM BASE2 Low
0x67	DAC2 BASE (low byte)

Figure 7-79. HAMM BASE2 (High/Low) Register

7	6	5	4	3	2	1	0
P	HAMM[3:0]				X	X	X
R/W-0h	R/W-0h				R-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-94. HAMM BASE2 (High/Low) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	P	R/W	0h	Parity bit
6:3	HAMM[3:0]	R/W	0h	Hamming bits

Figure 7-80. DAC2 BASE Register (high byte)

7	6	5	4	3	2	1	0
X	X	DAC2POL	DAC2BASE[12:8]				
R-0h	R-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-95. DAC2 BASE Register (High Byte) Field Descriptions

Bit	Field	Type	Reset	Description
5	DAC2POL	R/W	0h	LUT increment polarity control: 1: This setting realizes a monotonically decreasing LUT transfer function. 0: This setting realizes a monotonically increasing LUT transfer function.
4:0	DAC2BASE[12:8]	R/W	0h	LUT BASE value bits [12:8] (LUT output at +24°C).

Figure 7-81. DAC2 BASE Register (Low Byte)

7	6	5	4	3	2	1	0
DAC2BASE[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-96. DAC2 BASE Register (Low Byte) Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC2BASE[7:0]	R/W	0h	LUT BASE value bits [7:0] (LUT output at +24°C).

7.3.1.4.3 DAC3 BASE HAMM Registers (offset = 68h - 6Bh) [reset = 00h]

ADDRESS	NAME
0x68	HAMM BASE3 High
0x69	DAC3 BASE (high byte)
0x6A	HAMM BASE3 Low
0x6B	DAC3 BASE (low byte)

Figure 7-82. HAMM BASE3 (High/Low) Register

7	6	5	4	3	2	1	0
P	HAMM[3:0]				X	X	X
R/W-0h	R/W-0h				R-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-97. HAMM BASE3 (High/Low) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	P	R/W	0h	Parity bit
6:3	HAMM[3:0]	R/W	0h	Hamming bits

Figure 7-83. DAC3 BASE Register (high byte)

7	6	5	4	3	2	1	0
X	X	DAC3POL	DAC3BASE[12:8]				
R-0h	R-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-98. DAC3 BASE Register (High Byte) Field Descriptions

Bit	Field	Type	Reset	Description
5	DAC3POL	R/W	0h	LUT increment polarity control: 1: This setting realizes a monotonically decreasing LUT transfer function. 0: This setting realizes a monotonically increasing LUT transfer function.
4:0	DAC3BASE[12:8]	R/W	0h	LUT BASE value bits [12:8] (LUT output at +24°C).

Figure 7-84. DAC3 BASE Register (Low Byte)

7	6	5	4	3	2	1	0
DAC3BASE[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-99. DAC3 BASE Register (Low Byte) Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DAC3BASE[7:0]	R/W	0h	LUT BASE value bits [7:0] (LUT output at +24°C).

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7.3.1.5 I²C Page 15: Notepad Register Information

Page 15 includes 20 bytes of memory for arbitrary data storage. These data do not affect the operation of the device. Disable the LUT and ALU functionality to access the data on these registers. If the LUT or ALU is enabled, writing commands to the Notepad registers is blocked and read data are invalid. The SECDED engine is not applied to this section of the memory.

7.3.1.5.1 Notepad Registers (offset = 00h to 13h) [reset = 00h]

ADDRESS	NAME
0x00 ↓ 0x13	Notepad 0 ↓ Notepad 19

Figure 7-85. Notepad Register

7	6	5	4	3	2	1	0
PADx[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-100. Notepad Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PADx[7:0]	R/W	0h	20 bytes of memory for arbitrary data storage. This data does not affect the operation of the device.

7.3.1.5.2 EEPROM Burn Register (offset = 7Ch) [reset = 00h]

Figure 7-86. EEPROM Burn Register

7	6	5	4	3	2	1	0
EEBURN[7:0]							
W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-101. EEPROM Burn Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	EEBURN[7:0]	W	0h	EEPROM burn command register Writing 0xE4 to this register initiates a EEPROM burn sequence.

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7.3.2 SPI Registers

7.3.2.1 SPI Page 1: Device Configuration Register Information

7.3.2.1.1 Local Temperature Register (offset = 00h) [reset = N/A]

Figure 7-87. Local Temperature Register

15	14	13	12	11	10	9	8
LT[11:4]							
R-0h							
7	6	5	4	3	2	1	0
LT[3:0]				RESERVED			
R-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-102. Local Temperature Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	LT[11:4]	R	0h	Local temperature high byte. The resolution of the LSB in this register is 1°C. This register is read-only and is updated each time a temperature measurement is completed.
7:4	LT[3:0]	R	0h	Local temperature low byte. The resolution of the four bits in this register is 0.0625C. This register is read-only and is updated each time a temperature measurement is completed.

7.3.2.1.2 Remote Temperature Register (offset = 02h) [reset = N/A]

Figure 7-88. Remote Temperature Register

15	14	13	12	11	10	9	8
RT[11:4]							
R-0h							
7	6	5	4	3	2	1	0
RT[3:0]				RESERVED			
R-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-103. Remote Temperature Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RT[11:4]	R	0h	Remote temperature high byte. The resolution of the LSB in this register is 1°C. This register is read-only and is updated each time a temperature measurement is completed.
7:4	RT[3:0]	R	0h	Remote temperature low byte. The resolution of the four bits in this register is 0.0625C. This register is read-only and is updated each time a temperature measurement is completed.

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7.3.2.1.3 Status Register (offset = 04h) [reset = N/A]

Figure 7-89. Status Register

15	14	13	12	11	10	9	8
BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
TMPSTAT	PAON	EECRC	SPICRC	EERDY	DED	SEC	GAN
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-104. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BUSY	R	0h	Temperature ADC status indicator 1 = ADC is converting 0 = ADC is not converting
14	LHIGH	R	0h	Local temperature high limit status indicator 1 = Local temperature value exceeds the Local Temperature High Limit register value. This bit clears upon reading the Status register providing that the condition causing the over temperature result is no longer present. 0 = Local temperature value does not exceed the Local Temperature High Limit register value.
13	LLOW	R	0h	Local temperature low limit status indicator 1 = Local temperature value is below the Local Temperature Low Limit register value. This bit clears upon reading the Status register providing that the condition causing the under temperature result is no longer present. 0 = Local temperature value is not below the Local Temperature Low Limit register value.
12	RHIGH	R	0h	Remote temperature high limit status indicator 1 = Remote temperature value exceeds the Remote Temperature High Limit register value. This bit clears upon reading the Status register providing that the condition causing the overtemperature result is no longer present. 0 = Remote temperature value does not exceed the Remote Temperature High Limit register value.
11	RLOW	R	0h	Remote temperature low limit status indicator 1 = Remote temperature value is below the Remote Temperature Low Limit register value. This bit clears upon reading the Status register providing that the condition causing the undertemperature result is no longer present. 0 = Remote temperature value is not below the Remote Temperature Low Limit register value.
10	OPEN	R	0h	Remote junction open circuit detection 1 = The remote junction is an open circuit. This bit clears upon reading the Status register providing that the condition causing the open circuit is no longer present. 0 = The remote junction is not an open circuit.
7	TMPSTAT	R	0h	Temperature alarm status indicator 1 = A temperature alarm event was issued. This bit clears automatically after the temperature alarm bits clear.
6	PAON	R	0h	PA_ON status indicator 1 = PA_ON pin is high. 0 = PA_ON pin is low.
5	EECRC	R	0h	EEPROM load CRC error indicator 1 = Indicates a CRC error during EEPROM load to the user register space. To clear this bit, write a 1.

Table 7-104. Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SPICRC	R	0h	SPI command CRC error indicator 1 = Indicates a CRC error during an SPI command. To clear this bit, write a 1.
3	EERDY	R	0h	EEPROM ready indicator 0 = The EEPROM BURN is in progress. 1 = The EEPROM BURN is complete
2	DED	R	0h	Double error detection status indicator 1 = A double bit error is detected when accessing a LUT register in the operating memory. The error is not corrected. To clear this bit, write a 1.
1	SEC	R	0h	Single error correction status indicator 1 = A single bit error is detected when accessing a LUT register in the operating memory. The error is corrected. To clear this bit, write a 1.
0	GAN	R	0h	GAN ready indicator 1 = The device is in negative output range operation. 0 = The device is in positive output range operation.

7.3.2.1.4 Software Reset Register (offset = 06h) [reset = 0000h]

Figure 7-90. Software Reset Register

15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
SOFTRST[7:0]							
W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-105. Software Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SOFTRST[7:0]	W	0h	Software reset command 0x05 = Writing 0x05 to SOFTRST[7:0] initiates a reset event. 0xAD = Writing 0xAD to SOFTRST[7:0] initiates a register clear event that returns all operating memory registers to factory-default values. Wait 15µs before the next serial interface command.

7.3.2.1.5 Configuration Register (offset = 08h) [reset = 0108h]

Figure 7-91. Configuration 1 Register

15	14	13	12	11	10	9	8
RESERVED	TMPSD	ALERT/THERM	VSSRANGE	DACILMT	TMPRANGE	TMRCNT[1:0]	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
CRCEN	SDOEN	HAMMOFF	RESERVED	CR[3:0]			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-8h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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Table 7-106. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
14	TMPSD	R/W	0h	Temperature sensor shutdown control 1 = Places the temperature sensors in shutdown mode. 0 = Places the temperature sensors in continuous conversion mode.
13	ALERT/THERM	R/W	0h	ALERT or THERM temperature alarm mode select 1 = THERM mode. 0 = ALERT mode.
12	VSSRANGE	R/W	0h	V_{SS} auto-threshold detector control. Sets the valid V_{SS} supply range. Must be set to 0 if operating in positive output range 1 = Wide V_{SS} Configuration: –11V ≤ V_{SS} < –7V. 0 = Narrow V_{SS} Configuration: –7V ≤ V_{SS} ≤ –4.5V.
11	DACILMT	R/W	0h	DAC output current mode select 1 = High-current mode. 0 = Normal-current mode.
10	TMPRANGE	R/W	0h	This bit configures the range of the temperature measurement. *The selected range format must be used for all temperature data registers (high and low limits, offset and overwrite).* 1 = –64°C to +191°C. 0 = –40°C to +127°C.
9:8	TMRCNT[1:0]	R/W	1h	Start-up timer select. Sets the wait time between the DAC outputs being set at start-up and the PA_ON release 00 = 1ms. 01 = 15ms. 10 = 30ms. 11 = 60ms.
7	CRCEN	R/W	0h	SPI CRC error-check 1 = Enables the CRC SPI frame error check 0 = Disables the CRC SPI frame error check
6	SDOEN	R/W	0h	SDO pin enable 1 = The SDO pin is operational 0 = The SDO pin is in high-impedance mode
5	HAMMOFF	R/W	0h	Hamming-based SECDED module for LUT data access 0 = Enables the SECDED module. 1 = Disables the SECDED module.
3:0	CR[3:0]	R/W	8h	Conversion rate selection.

Table 7-107. Conversion Rate

VALUE	CONVERSIONS PER SECOND	TIME (SECONDS)
00h	0.0625	16
01h	0.125	8
02h	0.25	4
03h	0.5	2
04h	1	1
05h	2	0.5
06h	4	0.25
07h	8	0.125
08h	16 (default)	0.0625 (default)
09h	32	0.03125

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7.3.2.1.6 LUT/DAC Configuration Register (offset = 0Ah) [reset = 0300h]

Figure 7-92. LUT/DAC Configuration Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	LUTSTAT	LUTDIS	LUTSEL2	LUTSEL1	REN	LEN
R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
BYP3	BYP2	BYP1	BYP0	DAC3OW	DAC2OW	DAC1OW	DAC0OW
R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-108. LUT/DAC Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
13	LUTSTAT	R	0h	LUT status indicator 0 = The LUT/ALU engine is disabled. 1 = The LUT/ALU engine is enabled.
12	LUTDIS	R/W	0h	LUT/ALU control 0 = Enables the LUT/ALU engine. 1 = Disables the LUT/ALU engine. The temperature sensor remains active. The LUT/ALU engine must be disabled during EEPROM access or register access to pages 4, 5 and 15.
11	LUTSEL2	R/W	0h	LUT2 and LUT3 temperature input 0 = Local temperature sensor. 1 = Remote temperature sensor.
10	LUTSEL1	R/W	0h	LUT0 and LUT1 temperature input 0 = Local temperature sensor. 1 = Remote temperature sensor.
9	REN	R/W	1h	Remote temperature sensor control 0 = Disables remote temperature sensor conversions. 1 = Enables remote temperature sensor conversions.
8	LEN	R/W	1h	Local temperature sensor control 0 = Disables local temperature sensor conversions. 1 = Enables local temperature sensor conversions.
7	BYP3	R/W	0h	DACx ALU bypass control 0 = ALU output sent to DACx. 1 = Bypass the ALU output. Send BASEx value to DACx.
6	BYP2	R/W	0h	
5	BYP1	R/W	0h	
4	BYP0	R/W	0h	
3	DAC3OW	R/W	0h	DACx overwrite control 0 = DACx input is generated by LUT. 1 = DACx input is supplied by the serial interface accessible DACxOW[12:0] data register.
2	DAC2OW	R/W	0h	
1	DAC1OW	R/W	0h	
0	DAC0OW	R/W	0h	

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7.3.2.1.7 Drive Enable Configuration Register (offset: 0Ch) [reset = 0000h]

Figure 7-93. Drive Enable Configuration Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	DRV3	DRV2	RESERVED	RESERVED	DRV1	DRV0
R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	DRVSEL3	DRVSEL2	RESERVED	RESERVED	DRVSEL1	DRVSEL0
R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-109. Drive Enable Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
13	DRV3	R/W	0h	DAC3 switch control if configured for software operation 0 = OFF voltage. 1 = ON voltage.
12	DRV2	R/W	0h	OUT2 switch control if configured for software operation 0 = OFF voltage. 1 = ON voltage.
9	DRV1	R/W	0h	OUT1 switch control if configured for software operation 0 = OFF voltage. 1 = ON voltage.
8	DRV0	R/W	0h	DAC0 switch control if configured for software operation 0 = OFF voltage. 1 = ON voltage.
5	DRVSEL3	R/W	0h	DAC3 switch control select 0 = DRVEN2 pin. 1 = DRV3 bit.
4	DRVSEL2	R/W	0h	OUT2 switch control select 0 = DRVEN2 pin. 1 = DRV2 bit.
1	DRVSEL1	R/W	0h	OUT1 software switch control 0 = DRVEN1 pin. 1 = DRV1 bit.
0	DRVSEL0	R/W	0h	DAC0 software switch control 0 = DRVEN1 pin. 1 = DRV0 bit.

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7.3.2.1.8 Alarm Configuration Register (offset: 0Eh) [reset = 4F00h]

Figure 7-94. Alarm Configuration Register

15	14	13	12	11	10	9	8
ALMINEN	PAONDIS	RESERVED	RESERVED	DAC3OFF	OUT2OFF	OUT1OFF	DAC0OFF
R/W-0h	R/W-1h	R-0h	R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
RESETCMD[1:0]		RESERVED	AMCINT	DRVENRLS	PAONRLS	DACHCRLS	DACRLS
R/W-0h		R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-110. Alarm Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ALMINEN	R/W	0h	$\overline{\text{ALARMIN}}$ functionality for $\overline{\text{RESET}}$ pin 1 = $\overline{\text{ALARMIN}}$. 0 = $\overline{\text{RESET}}$.
15	PAONDIS	R/W	1h	PA_ON alarm control 0 = PA_ON is unaffected by an alarm event. 1 = PA_ON is set low during an alarm event.
11	DAC3OFF	R/W	1h	DAC3 alarm control 0 = DAC3 is unaffected by an alarm event. 1 = DAC3 is switched OFF during an alarm event.
10	OUT2OFF	R/W	1h	OUT2 alarm control 0 = OUT2 is unaffected by an alarm event. 1 = OUT2 is switched OFF during an alarm event.
9	OUT1OFF	R/W	1h	OUT1 alarm control 0 = OUT1 is unaffected by an alarm event. 1 = DAC3 is switched OFF during an alarm event.
8	DAC2OFF	R/W	1h	DAC0 alarm control 0 = DAC0 is unaffected by an alarm event. 1 = DAC0 is switched OFF during an alarm event.
7:6	RESETCMD[1:0]	R/W	0h	Reset command 00 = No operation. 01 = Wait for end of temperature conversion. 10 = Release DACs. 11 = Release DACs from start-up current mode.
4	AMCINT	R/W	0h	AMC interrupt mode 0 = Normal operation. 1 = Sets device in interrupt mode where the automatic reset control signals are ignored.
3	DRVENRLS	R/W	0h	DRVEN control when device is set in interrupt mode 0 = Forces all internal DRVEN switch control signals to zero. 1 = Enables control of the DRVEN signals.
2	PAONRLS	R/W	1h	PA_ON control when device is set in interrupt mode 0 = PA_ON pin is forced low. 1 = PA_ON pin is forced high.
1	DACHCRLS	R/W	1h	DAC output current control when device is set in interrupt mode 0 = DACs are forced into start-up current mode. 1 = DACs are released from start-up current mode.
0	DACRLS	R/W	1h	DAC output control when device is set in interrupt mode 0 = DACs input code is forced to all zeros. 1 = DACs input code can be accessed.

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7.3.2.1.9 Local Temperature Limit Register (offset = 10h) [reset = 7F80h]

Figure 7-95. Local Temperature Limit Register

15	14	13	12	11	10	9	8
LTHL[11:4]							
R/W-7Fh							
7	6	5	4	3	2	1	0
LTLL[11:4]							
R/W-80h							

7	6	5	4	3	2	1	0
LTHL[11:4]							
R/W-7Fh							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-111. Local Temperature Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	LTHL[11:4]	R/W	7Fh	These bits determine the value of the high temperature limit to which the local temperature measurement is compared. The resolution of the LSB in this register is 1°C. Format denoted by the TMPRANGE bit.
7:0	LTLL[11:4]	R/W	80h	These bits determine the value of the low temperature limit to which the local temperature measurement is compared. The resolution of the LSB in this register is 1°C. Format denoted by the TMPRANGE bit.

7.3.2.1.10 Remote Temperature High Limit Register (offset = 12h) [reset = 7FF0h]

Figure 7-96. Remote Temperature High Limit Register

15	14	13	12	11	10	9	8
RTHL[11:4]							
R/W-7Fh							
7	6	5	4	3	2	1	0
RTHL[3:0]				RESERVED			
R/W-Fh				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-112. Remote Temperature High Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RTHL[11:4]	R/W	7Fh	These bits determine the value of the high byte of the high temperature limit to which the remote temperature measurement is compared. The resolution of the LSB in this register is 1°C. Format denoted by the TMPRANGE bit.
7:4	RTHL[3:0]	R/W	Fh	These bits determine the value of the low byte of the high temperature limit to which the remote temperature measurement is compared. The resolution of the four bits in this register is 0.0625°C. Format denoted by the TMPRANGE bit.

7.3.2.1.11 Remote Temperature Low Limit Register (offset = 14h) [reset = 8000h]

Figure 7-97. Remote Temperature Low Limit Register

15	14	13	12	11	10	9	8
RTLL[11:4]							
R/W-80h							
7	6	5	4	3	2	1	0
RTLL[3:0]				RESERVED			
R/W-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-113. Remote Temperature Low Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RTLL[11:4]	R/W	80h	These bits determine the value of high byte of the low temperature limit to which the remote temperature measurement is compared. The resolution of the LSB in this register is 1°C. Format denoted by the TMPRANGE bit.
7:4	RTLL[3:0]	R/W	0h	These bits determine the value of the low byte of the low temperature limit to which the remote temperature measurement is compared. The resolution of the four bits in this register is 0.0625°C. Format denoted by the TMPRANGE bit.

7.3.2.1.12 Remote Temperature Offset Register (offset = 16h) [reset = 0000h]

Figure 7-98. Remote Temperature Offset Register

15	14	13	12	11	10	9	8
RTOS[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
RTOS[3:0]				RESERVED			
R/W-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-114. Remote Temperature Offset Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RTOS[11:4]	R/W	0h	Remote temperature offset high byte. The value of this register is added to the value the ADC conversion with the result stored in the remote temperature register. This register is used to add or subtract a temperature offset value to the ADC conversion result in applications requiring calibration. The resolution of the LSB in this register is 1°C. Format denoted by the TMPRANGE bit.
7:4	RTOS[3:0]	R/W	0h	Remote temperature offset low byte. The value of this register is added to the value the ADC conversion with the result stored in the remote temperature register. This register is used to add or subtract a temperature offset value to the ADC conversion result in applications requiring calibration. The resolution of these four bits is 0.0625°C. Format denoted by the TMPRANGE bit.

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7.3.2.1.13 Temperature Configuration 1 Register (offset = 1Ah) [reset = 0A01h]

Figure 7-99. Temperature Configuration 1 Register

15	14	13	12	11	10	9	8
HYS[11:4]							
R/W-0Ah							
7	6	5	4	3	2	1	0
RESERVED				CONAL[2:0]			RESERVED
R-0h				R/W-0h			R-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-115. Temperature Configuration 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS[11:4]	R/W	0Ah	THERM hysteresis value. These bits determine the amount of hysteresis applied to the THERM function. The resolution of the LSB in this register is 1°C.
3:1	CONAL[2:0]	R/W	0h	Number of consecutive out-of-limit measurements required to activate an ALERT temperature alarm.

Table 7-116. Consecutive Alert Configuration

VALUE	NUMBER OF CONSECUTIVE OUT-OF-LIMIT MEASUREMENTS REQUIRED
0h	1
1h	2
3h	3
7h	4

7.3.2.1.14 Temperature Configuration 2 Register (offset = 1Ch) [reset = 0000h]

Figure 7-100. Temperature Configuration 2 Register

15	14	13	12	11	10	9	8
NC[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						DF[1:0]	
R-0h						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-117. Temperature Configuration 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	NC[7:0]	R/W	0h	η-factor value.
1:0	DF[1:0]	R/W	0h	Configures the amount of filtering for the remote temperature results.

Table 7-118. η-Factor Range

N_{ADJUST}			η
BINARY	HEX	DECIMAL	
0111 1111	7F	127	0.950205
0000 1010	0A	10	1.003195
0000 1000	08	8	1.004153
0000 0110	06	6	1.005112
0000 0100	04	4	1.006073
0000 0010	02	2	1.007035
0000 0001	01	1	1.007517
0000 0000	00	0	1.008
1111 1111	FF	–1	1.008483
1111 1110	FE	–2	1.008966
1111 1100	FC	–4	1.009935
1111 1010	FA	–6	1.010905
1111 1000	F8	–8	1.011877
1111 0110	F6	–10	1.012851
1000 0000	80	–128	1.073829

Table 7-119. Digital Filter Configuration

VALUE	NUMBER OF REMOTE TEMPERATURE MEASUREMENTS AVERAGED
0h	Averaging off
1h	4
2h	8
4h	not used

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7.3.2.1.15 Device ID Register (offset = 1Eh) [reset = 00A3h]

Figure 7-101. Device ID Register

15	14	13	12	11	10	9	8
VERSION[7:0]							
R-0h							
7	6	5	4	3	2	1	0
ID[7:0]							
R-A3h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-120. Device ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	VERSION[7:0]	R	0h	Device version ID. **Subject to change.**
7:0	ID[7:0]	R	A3h	Device identification information.

7.3.2.1.16 Temperature Overwrite Register (offset = 22h) [reset = 0000h]

Figure 7-102. Temperature Overwrite Register

15	14	13	12	11	10	9	8
TEMPOW[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
TEMPOW[3:0]				RESERVED			TEMPOW
R/W-0h				R-0h			R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-121. Temperature Overwrite Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	TEMPOW[11:4]	R/W	0h	Temperature sensor overwrite value high byte. Format denoted by the TMPRANGE bit.
7:4	TEMPOW[3:0]	R/W	0h	Temperature sensor overwrite value low byte. Format denoted by the TMPRANGE bit.
0	TEMPOW	R/W	0h	Temperature sensor overwrite control 0 = The temperature sensor outputs are used to index the LUT. 1 = The serial interface accessible TEMPOW[11:0] data register is used to index the LUT.

7.3.2.1.17 Reset Status Register (offset = 24h) [reset = N/A]

Figure 7-103. Reset Status Register

15	14	13	12	11	10	9	8
RESERVED				RESETSTA[3:0]			
R-0h				R-0h			
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-122. Reset Status Register Field Descriptions

Bit	Field	Type	Reset	Description
11:8	RESETSTA[3:0]	R	0h	Reset control status. Read the register twice for data validation. If two consecutive readings do not match, issue additional read commands until the data are equivalent.

Table 7-123. Reset Control Status

VALUE	STATE
0h	Idle
1h	Wait for device start
2h	EEPROM load start
3h	EEPROM load in progress
4h	Interrupt mode
5h	Check for valid output buffer supply ranges
6h	Temperature conversion in progress
7h	Wait for LUT/ALU
8h	Wait for alarm event
9h	Release DACs from all zero-code
Ah	Wait for timer between DACs and PA_ON assert
Bh	Release DACs from start-up current mode
Ch	Set PA_ON
Dh	Release DRVEN switch controls
Eh	Alarm event
Fh	Reserved

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7.3.2.1.18 One-Shot Temperature Register (offset = 28h) [reset = 0000h]

Figure 7-104. One-Shot Temperature Register

15	14	13	12	11	10	9	8
TEMPONE[15:8]							
W-0h							
7	6	5	4	3	2	1	0
TEMPONE[7:0]							
W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-124. One-Shot Temperature Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TEMPONE[15:0]	W	0h	When the temperature sensor is in shutdown mode, write any value to this register to trigger a one-shot temperature conversion.

7.3.2.1.19 Software Alarm Register (offset = 2Ah) [reset = 0000h]

Figure 7-105. Software Alarm Register

15	14	13	12	11	10	9	8
RESERVED							SWALM
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-125. Software Alarm Register Field Descriptions

Bit	Field	Type	Reset	Description
8	SWALM	R/W	0h	Software Alarm 1 = Setting the SWALM bit initiates an alarm event. The alarm condition persists until the bit is cleared to 0.

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7.3.2.2 SPI Page 2: DAC Configuration Register Information

7.3.2.2.1 DAC0 Input Data Register (offset = 00h) [reset = 0000h]

Figure 7-106. DAC0 Input Data Register

15	14	13	12	11	10	9	8
0	0	0	DAC0[12:8]				
R-0	R-0	R-0	R-0h				
7	6	5	4	3	2	1	0
DAC0[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-126. DAC0 Input Data Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC0[12:0]	R	0h	DAC0[12:0] input data.

7.3.2.2.2 DAC1 Input Data Register (offset = 02h) [reset = 0000h]

Figure 7-107. DAC1 Input Data Register

15	14	13	12	11	10	9	8
0	0	0	DAC1[12:8]				
R-0	R-0	R-0	R-0h				
7	6	5	4	3	2	1	0
DAC1[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-127. DAC1 Input Data Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC1[12:0]	R	0h	DAC1[12:0] input data.

7.3.2.2.3 DAC2 Input Data Register (offset = 04h) [reset = 0000h]

Figure 7-108. DAC2 Input Data Register

15	14	13	12	11	10	9	8
0	0	0	DAC2[12:8]				
R-0	R-0	R-0	R-0h				
7	6	5	4	3	2	1	0
DAC2[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-128. DAC2 Input Data Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC2[12:0]	R	0h	DAC2[12:0] input data.

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7.3.2.2.4 DAC3 Input Data Register (offset = 06h) [reset = 0000h]

Figure 7-109. DAC3 Input Data Register

15	14	13	12	11	10	9	8
0	0	0	DAC3[12:8]				
R-0	R-0	R-0	R-0h				
7	6	5	4	3	2	1	0
DAC3[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-129. DAC3 Input Data Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC3[12:0]	R	0h	DAC3[12:0] input data.

7.3.2.2.5 DAC0 Overwrite Register (offset = 08h) [reset = 0000h]

Figure 7-110. DAC0 Overwrite Register

15	14	13	12	11	10	9	8
0	0	0	DAC0OW[12:8]				
R-0	R-0	R-0	R/W-0h				
7	6	5	4	3	2	1	0
DAC0OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-130. DAC0 Overwrite Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC0OW[12:0]	R/W	0h	DAC0[12:0] overwrite data.

7.3.2.2.6 DAC1 Overwrite Register (offset = 0Ah) [reset = 0000h]

Figure 7-111. DAC1 Overwrite Register

15	14	13	12	11	10	9	8
0	0	0	DAC1OW[12:8]				
R-0	R-0	R-0	R/W-0h				
7	6	5	4	3	2	1	0
DAC1OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-131. DAC1 Overwrite Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC1OW[12:0]	R/W	0h	DAC1[12:0] overwrite data.

7.3.2.2.7 DAC2 Overwrite Register (offset = 0Ch) [reset = 0000h]

Figure 7-112. DAC2 Overwrite Register

15	14	13	12	11	10	9	8
0	0	0	DAC2OW[12:8]				
R-0	R-0	R-0	R/W-0h				
7	6	5	4	3	2	1	0
DAC2OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-132. DAC2 Overwrite Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC2OW[12:0]	R/W	0h	DAC2[12:0] overwrite data.

7.3.2.2.8 DAC3 Overwrite Register (offset = 0Eh) [reset = 0000h]

Figure 7-113. DAC3 Overwrite Register

15	14	13	12	11	10	9	8
0	0	0	DAC3OW[12:8]				
R-0	R-0	R-0	R/W-0h				
7	6	5	4	3	2	1	0
DAC3OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-133. DAC3 Overwrite Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC3OW[12:0]	R/W	0h	DAC3[12:0] overwrite data.

7.3.2.2.9 CLAMP1 Overwrite Register (offset: 10h) [reset = 0000h]

Figure 7-114. CLAMP1 Overwrite Register

15	14	13	12	11	10	9	8
0	0	0	CLM1OW[12:8]				
R-0	R-0	R-0	R/W-0h				
7	6	5	4	3	2	1	0
CLM1OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-134. CLAMP1 Overwrite Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	CLM1OW[12:0]	R/W	0h	CLAMP1[12:0] overwrite data.

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7.3.2.2.10 CLAMP2 Overwrite Register (offset: 12h) [reset = 0000h]

Figure 7-115. CLAMP2 Overwrite Register

15	14	13	12	11	10	9	8
0	0	0	CLM2OW[12:8]				
R-0	R-0	R-0	R/W-0h				
7	6	5	4	3	2	1	0
CLM2OW[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-135. CLAMP2 Overwrite Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	CLM2OW[12:0]	R/W	0h	CLAMP2[12:0] overwrite data.

7.3.2.2.11 CLAMP1 Input Data Register (offset: 18h) [reset = 0000h]

Figure 7-116. CLAMP1 Input Data Register

15	14	13	12	11	10	9	8
0	0	0	CLM1[12:8]				
R-0	R-0	R-0	R-0h				
7	6	5	4	3	2	1	0
CLM1[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-136. CLAMP1 Input Data Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	CLM1[12:0]	R	0h	CLAMP1[12:0] input data.

7.3.2.2.12 CLAMP2 Input Data Register (offset: 1Ah) [reset = 0000h]

Figure 7-117. CLAMP2 Input Data Register

15	14	13	12	11	10	9	8
0	0	0	CLM2[12:8]				
R-0	R-0	R-0	R-0h				
7	6	5	4	3	2	1	0
CLM2[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-137. CLAMP2 Input Data Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	CLM2[12:0]	R	0h	CLAMP2[12:0] input data.

7.3.2.2.13 DAC0 LUT Data Register (offset = 20h) [reset = 0000h]

Figure 7-118. DAC0 LUT Data Register

15	14	13	12	11	10	9	8
0	0	0	DAC0LUT[12:8]				
R-0	R-0	R-0	R-0h				
7	6	5	4	3	2	1	0
DAC0LUT[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-138. DAC0 LUT Data Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC0LUT[12:0]	R	0h	DAC0[12:0] LUT data.

7.3.2.2.14 DAC1 LUT Data Register (offset = 22h) [reset = 0000h]

Figure 7-119. DAC1 LUT Data Register

15	14	13	12	11	10	9	8
0	0	0	DAC1LUT[12:8]				
R-0	R-0	R-0	R-0h				
7	6	5	4	3	2	1	0
DAC1LUT[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-139. DAC1 LUT Data Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC1LUT[12:0]	R	0h	DAC1[12:0] LUT data.

7.3.2.2.15 DAC2 LUT Data Register (offset = 24h) [reset = 0000h]

Figure 7-120. DAC2 LUT Data Register

15	14	13	12	11	10	9	8
0	0	0	DAC2LUT[12:8]				
R-0	R-0	R-0	R-0h				
7	6	5	4	3	2	1	0
DAC2LUT[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-140. DAC2 LUT Data Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC2LUT[12:0]	R	0h	DAC2[12:0] LUT data.

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7.3.2.2.16 DAC3 LUT Data Register (offset = 26h) [reset = 0000h]

Figure 7-121. DAC3 LUT Data Register

15	14	13	12	11	10	9	8
0	0	0	DAC3LUT[12:8]				
R-0	R-0	R-0	R-0h				
7	6	5	4	3	2	1	0
DAC3LUT[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-141. DAC3 LUT Data Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	DAC3LUT[12:0]	R	0h	DAC3[12:0] LUT data.

7.3.2.2.17 Broadcast Register (offset = 30h) [reset = 0000h]

Figure 7-122. Broadcast Register

15	14	13	12	11	10	9	8
0	0	0	BRDCST[12:8]				
R-0	R-0	R-0	R/W-0h				
7	6	5	4	3	2	1	0
BRDCST[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-142. Broadcast Register Field Descriptions

Bit	Field	Type	Reset	Description
12:0	BRDCST[12:0]	R/W	0h	BRDCST[12:0] data sent to all DAC channels (DAC[0:3] and CLAMP[1:2]) simultaneously.

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7.3.2.3 SPI Page 4: LUT0 and LUT1 Configuration Register Information

Page 4 stores the LUT0 and LUT1 values at locations corresponding to 4°C increments from –48°C to 152°C. There is no increment corresponding to 24°C because this temperature is a BASELINE, and the corresponding LUT value is the 13-bit BASE.

Each address row stores a pair of DELTA registers and the corresponding SECDED parity and Hamming bits. The LUT requires the DELTA values to represent a monotonic function. The function is either increasing or decreasing, and is determined by the POL bit in each DAC BASE register. DELTA values are unsigned.

The BASE values for DAC0 and DAC1, along with the corresponding SECDED codes are stored in addresses 0x64 to 0x6A.

The required method for updating the LUT entries is to disable the LUT, update the entries, and then enable the LUT.

7.3.2.3.1 DELTA Registers (offset = 00h - 62h) [reset = 00FFh]

ADDRESS	NAME
0x00	DELTAn48 (–48°C)
0x02 ↓ 0x22	DELTAn44 (–44°C) ↓ DELTAp20 (20°C)
0x24 ↓ 0x60	DELTAp28 (28°C) ↓ DELTAp148 (148°C)
0x62	DELTAp152 (152°C)

Figure 7-123. DELTA Register

15	14	13	12	11	10	9	8
P	HAMM[3:0]				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DAC1[3:0]				DAC0[3:0]			
R/W-Fh				R/W-Fh			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-143. DELTA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	P	R/W	0h	Parity bit
14:11	HAMM[3:0]	R/W	0h	Hamming bits
7:4	DAC1[3:0]	R/W	Fh	4-bit LUT1 entry
3:0	DAC0[3:0]	R/W	Fh	4-bit LUT0 entry

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7.3.2.3.2 DAC0 BASE Registers (offset = 64h - 66h) [reset = 0000h]

ADDRESS	NAME
0x64	DAC0 BASE (high)
0x66	DAC0 BASE (low)

Figure 7-124. DAC0 BASE (High) Register

15	14	13	12	11	10	9	8
P	HAMM[3:0]				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	DAC0POL	DAC0[12:8]				
R-0h	R-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-144. DAC0 BASE (High) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	P	R/W	0h	Parity bit
14:11	HAMM[3:0]	R/W	0h	Hamming bits
5	DAC0POL	R/W	0h	LUT increment polarity control: 1: This setting realizes a monotonically decreasing LUT transfer function. 0: This setting realizes a monotonically increasing LUT transfer function.
4:0	DAC0BASE[12:8]	R/W	0h	LUT BASE value bits [12:8] (LUT output at +24°C).

Figure 7-125. DAC0 BASE (Low) Register

15	14	13	12	11	10	9	8
P	HAMM[3:0]				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DAC0BASE[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-145. DAC2 BASE (Low) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	P	R/W	0h	Parity bit
14:11	HAMM[3:0]	R/W	0h	Hamming bits
7:0	DAC0BASE[7:0]	R/W	0h	LUT BASE value bits [7:0] (LUT output at +24°C).

7.3.2.3.3 DAC1 BASE Registers (offset = 68h - 6Ah) [reset = 0000h]

ADDRESS	NAME
0x68	DAC1 BASE (high)
0x6A	DAC1 BASE (low)

Figure 7-126. DAC1 BASE (High) Register

15	14	13	12	11	10	9	8
P	HAMM[3:0]				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	DAC1POL	DAC1[12:8]				
R-0h	R-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-146. DAC1 BASE (High) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	P	R/W	0h	Parity bit
14:11	HAMM[3:0]	R/W	0h	Hamming bits
5	DAC1POL	R/W	0h	LUT increment polarity control: 1: This setting realizes a monotonically decreasing LUT transfer function. 0: This setting realizes a monotonically increasing LUT transfer function.
4:0	DAC1BASE[12:8]	R/W	0h	LUT BASE value bits [12:8] (LUT output at 24°C).

Figure 7-127. DAC1 BASE (Low) Register

15	14	13	12	11	10	9	8
P	HAMM[3:0]				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DAC1BASE[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-147. DAC1 BASE (Low) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	P	R/W	0h	Parity bit
14:11	HAMM[3:0]	R/W	0h	Hamming bits
7:0	DAC1BASE[7:0]	R/W	0h	LUT BASE value bits [7:0] (LUT output at 24°C).

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7.3.2.4 SPI Page 5: LUT2 and LUT3 Configuration Register Information

Page 5 stores the LUT2 and LUT3 values at locations corresponding to 4°C increments from –48°C to 152°C. There is no increment corresponding to 24°C because this temperature is a BASELINE, and the corresponding LUT value is the 13-bit BASE.

Each address row stores a pair of DELTA registers and the corresponding SECDED parity and Hamming bits. The LUT requires the DELTA values to represent a monotonic function. The function is either increasing or decreasing, and is determined by the POL bit in each DAC BASE register. DELTA values are unsigned.

The BASE values for DAC2 and DAC3, along with the corresponding SECDED codes are stored in addresses 0x64 to 0x6A.

The required method for updating the LUT entries is to disable the LUT, update the entries, and then enable the LUT.

7.3.2.4.1 DELTA Registers (offset = 00h - 62h) [reset = 00FFh]

ADDRESS	NAME
0x00	DELTAn48 (–48°C)
0x02 ↓ 0x22	DELTAn44 (–44°C) ↓ DELTAp20 (20°C)
0x24 ↓ 0x60	DELTAp28 (28°C) ↓ DELTAp148 (148°C)
0x62	DELTAp152 (152°C)

Figure 7-128. DELTA Register

15	14	13	12	11	10	9	8
P	HAMM[3:0]				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DAC3[3:0]				DAC2[3:0]			
R/W-Fh				R/W-Fh			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-148. DELTA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	P	R/W	0h	Parity bit
14:11	HAMM[3:0]	R/W	0h	Hamming bits
7:4	DAC3[3:0]	R/W	Fh	4-bit LUT3 entry
3:0	DAC2[3:0]	R/W	Fh	4-bit LUT2 entry

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7.3.2.4.2 DAC2 BASE Registers (offset = 64h - 66h) [reset = 0000h]

ADDRESS	NAME
0x64	DAC2 BASE (high)
0x66	DAC2 BASE (low)

Figure 7-129. DAC2 BASE (High) Register

15	14	13	12	11	10	9	8
P	HAMM[3:0]				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	DAC2POL	DAC2[12:8]				
R-0h	R-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-149. DAC2 BASE (High) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	P	R/W	0h	Parity bit
14:11	HAMM[3:0]	R/W	0h	Hamming bits
5	DAC2POL	R/W	0h	LUT increment polarity control: 1: This setting realizes a monotonically decreasing LUT transfer function. 0: This setting realizes a monotonically increasing LUT transfer function.
4:0	DAC2BASE[12:8]	R/W	0h	LUT BASE value bits [12:8] (LUT output at +24°C).

Figure 7-130. DAC2 BASE (Low) Register

15	14	13	12	11	10	9	8
P	HAMM[3:0]				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DAC2BASE[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-150. DAC2 BASE (Low) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	P	R/W	0h	Parity bit
14:11	HAMM[3:0]	R/W	0h	Hamming bits
7:0	DAC2BASE[7:0]	R/W	0h	LUT BASE value bits [7:0] (LUT output at +24°C).

ADVANCE INFORMATION

7.3.2.4.3 DAC3 BASE Registers (offset = 68h - 6Ah) [reset = 0000h]

ADDRESS	NAME
0x68	DAC3 BASE (high)
0x6A	DAC3 BASE (low)

Figure 7-131. DAC3 BASE (High) Register

15	14	13	12	11	10	9	8
P	HAMM[3:0]				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	DAC3POL	DAC3[12:8]				
R-0h	R-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-151. DAC3 BASE (High) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	P	R/W	0h	Parity bit
14:11	HAMM[3:0]	R/W	0h	Hamming bits
5	DAC3POL	R/W	0h	LUT increment polarity control: 1: This setting realizes a monotonically decreasing LUT transfer function. 0: This setting realizes a monotonically increasing LUT transfer function.
4:0	DAC3BASE[12:8]	R/W	0h	LUT BASE value bits [12:8] (LUT output at +24°C).

Figure 7-132. DAC3 BASE (Low) Register

15	14	13	12	11	10	9	8
P	HAMM[3:0]				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DAC3BASE[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-152. DAC3 BASE (Low) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	P	R/W	0h	Parity bit
14:11	HAMM[3:0]	R/W	0h	Hamming bits
7:0	DAC3BASE[7:0]	R/W	0h	LUT BASE value bits [7:0] (LUT output at +24°C).

7.3.2.5 SPI Page 15: Notepad Register Information

Page 15 includes 20 bytes of memory for arbitrary data storage. These data do not affect the operation of the device. The LUT and ALU functionality must be disabled to access the data on these registers. If the LUT or ALU is enabled, writing commands to the Notepad registers is blocked and read data are invalid. The SECDED engine is not applied to this section of the memory.

7.3.2.5.1 Notepad Registers (offset = 00h to 12h) [reset = 0000h]

ADDRESS	NAME
0x00 ↓ 0x12	Notepad 0-1 ↓ Notepad 18-19

Figure 7-133. Notepad *x-y* Register

15	14	13	12	11	10	9	8
PAD*x*[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
PAD*y*[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-153. Notepad Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PAD*x*[7:0]	R/W	0h	20 bytes of memory for arbitrary data storage. This data does not affect the operation of the device.
7:0	PAD*y*[7:0]	R/W	0h	20 bytes of memory for arbitrary data storage. This data does not affect the operation of the device.

7.3.2.5.2 EEPROM Burn Register (offset = 7Ch) [reset = 0000h]

Figure 7-134. EEPROM Burn Register

15	14	13	12	11	10	9	8
EEBURN[7:0]							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							
W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-154. EEPROM Burn Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	EEBURN[7:0]	W	0h	EEPROM burn command register Writing 0xE4 to EEBURN[7:0] initiates a EEPROM burn sequence.

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The primary application of the AFE10004-EP device is to provide power amplifier (PA) gate-bias control. The integrated switches allow the gate bias to be switched between a temperature-adjusted *on voltage* and a static, lower-potential *off voltage*. The application is made more efficient by the temperature look-up table, which adjusts the DAC output based on user-defined transfer function coefficients. These coefficients allow the bias voltage to be optimized for the temperature performance of a specific PA.

In addition, the AFE10004-EP has features to track alarm conditions, and in response, turn-off the gate voltages and send an interrupt to protect the PA during these events.

8.1.1 Output Switching Timing

The externally applied output capacitors allow for noise filtering, and enable fast switching on the output channels of the device. Large capacitors can be connected to the output of the static channels: DAC1, DAC2, CLAMP1, and CLAMP2. Capacitors of lower values can be connected to the dynamic channels, DAC0, DAC3, OUT1, and OUT2. This capacitor arrangement means that the larger capacitors can quickly charge the smaller capacitors instead of relying on the DAC output buffers.

Figure 8-1 shows a simplified model of switch arrangement for the OUT1 channel. The on-resistance of the switches are represented by R_{SW1} and R_{SW2}.The on-resistance is specified for the channels in the *Electrical Characteristics*. The resistance primarily limits the settling time of V_{OUT1} after a switching event, as the settling time is essentially an RC function.

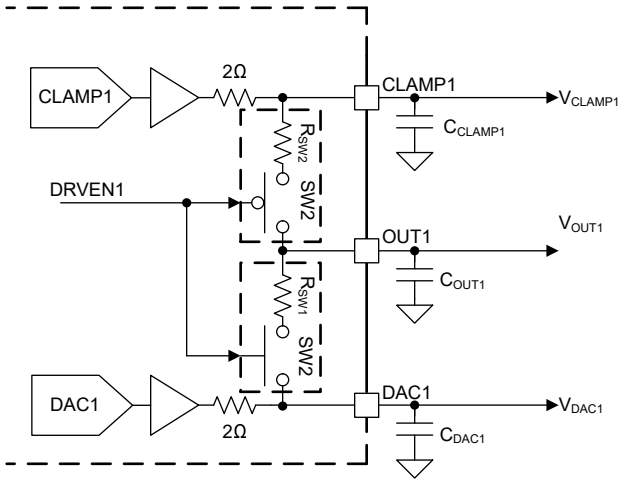


Figure 8-1. Switching Transients

For example, consider the case where DRVEN1 changes from a low-state to a high-state. The steady-state of VOUT1 is equal to V_{CLAMP} before the switch event. After the DRVEN1 goes high, SW2 closes, connecting C_{OUT1} and C_{DAC1} to each other. As these capacitors are now in parallel, the voltages across each equalize to a new voltage. This voltage, described as $V_{CDAC||COUT}$ in the following equation, can be calculated by finding the charge stored in each capacitor. The total charge on the two capacitors in parallel is equal to the sum of the charge of each capacitor.

$$Q_{CDAC||COUT} = Q_{CDAC} + Q_{COUT} \tag{9}$$

$$V_{CDAC||COUT}\left(C_{DAC1} + C_{OUT1}\right) = V_{DAC1} \times C_{DAC1} + V_{OUT1} \times C_{OUT1} \tag{10}$$

$$V_{CDAC||COUT} = \frac{V_{DAC1} \times C_{DAC1} + V_{OUT1} \times C_{OUT1}}{C_{DAC1} + C_{OUT1}} \tag{11}$$

The time required for the two output to equalize, described as the *Capacitive Settling Period* in Figure 8-2, is calculated using the equation below. As CLAMP1 is lower potential than DAC1, V_{OUT1} can be expressed as a charging function.

$$V_{OUT1}(t) = \left(V_{CDAC||COUT} - V_{OUT1}(t_0)\right)\left(1 - e^{\frac{-t}{R_{SW1} \times C_{OUT1}}}\right) + V_{OUT1}(t_0) \tag{12}$$

During the capacitive settling period, V_{DAC1} is expressed as a discharging RC function.

$$V_{DAC1}(t) = V_{DAC1}(t_0) - \left(V_{DAC1}(t_0) - V_{CDAC||COUT}\right)\left(1 - e^{\frac{-t}{R_{SW1} \times C_{OUT1}}}\right) \tag{13}$$

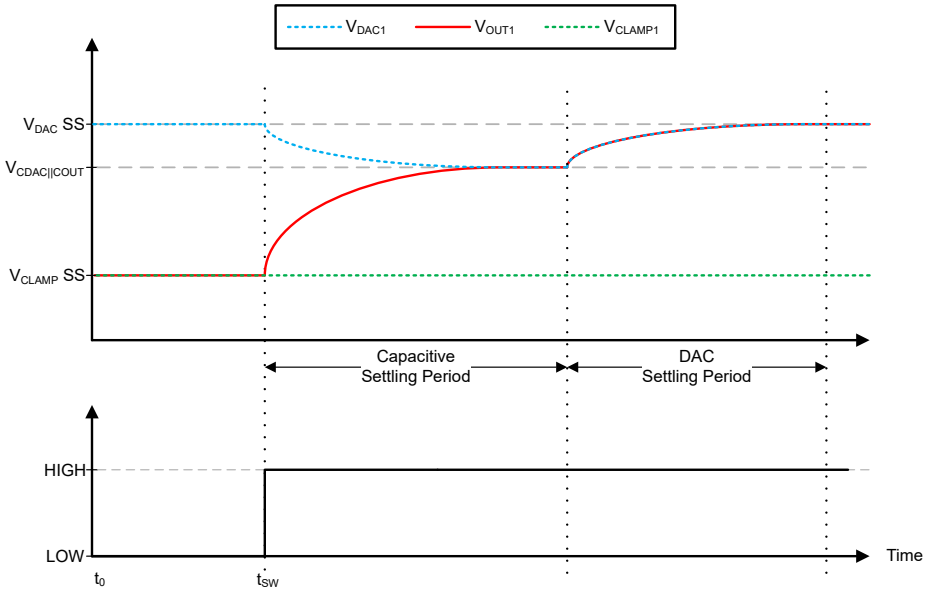


Figure 8-2. Switching Timing

Connecting the capacitors together allows the output to change to $V_{CDAC||COUT}$ quickly, but after that period, the DAC output buffer continues to charge C_{OUT1} to the V_{DAC1} value. The settling time for that final transition depends on the RC function formed by the series resistance on the DAC output, the switch resistance, and the capacitive load on the DAC. In addition, the output current of the DAC is limited.

Figure 8-3 and Figure 8-4 show the switching transients in the application with 10µF capacitors on the static channels and 100nF capacitors on the dynamic channels. Figure 8-5 shows the small-signal settling time of the OUT signal switching to the DAC output.

ADVANCE INFORMATION

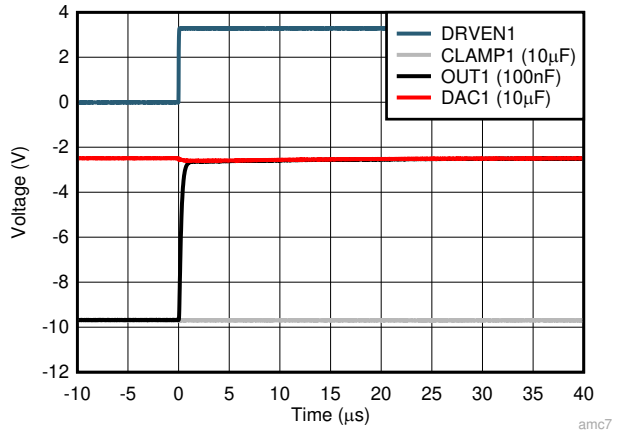


Figure 8-3. CLAMP-to-DAC Switch Response

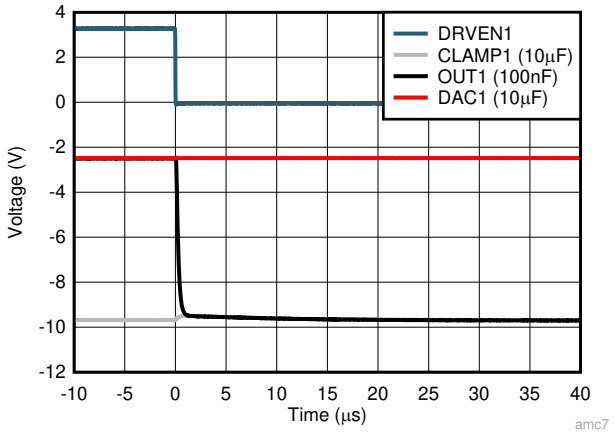


Figure 8-4. DAC-to-CLAMP Switch Response

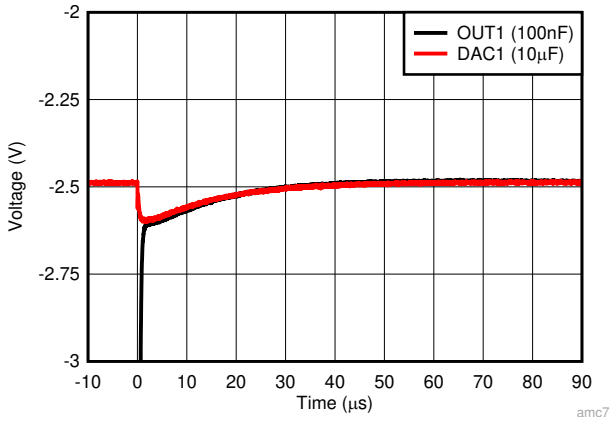


Figure 8-5. CLAMP-to-DAC Small Transient Switch Response

Large capacitor values are potentially prohibitive in applications where small component size is required. This requirement results in capacitor selection where the capacitors on static channels are not orders-of-magnitude larger than the dynamic channels. For example, with 10nF and 1nF for the static and dynamic channels, respectively, the DAC settling capability dominates the charging time. Figure 8-6 shows the switch response for this case.

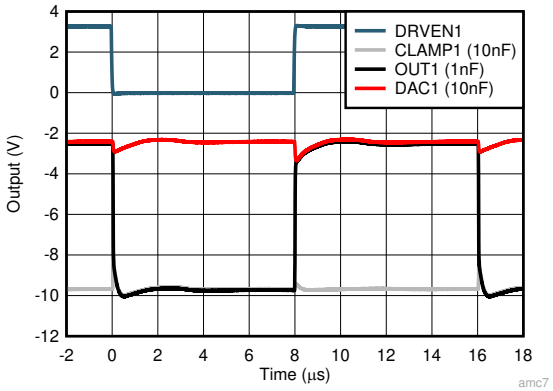


Figure 8-6. Low-Capacitance Switch Response

8.2 Typical Applications

8.2.1 Temperature-Compensated Bias Generator for an LDMOS Power Amplifier (PA)

A typical application for the AFE10004-EP is to bias the gate voltage of an LDMOS PA so that the drain current is constant. A positive bias is required to enable the power amplifier, and the drain current must be constant over a wide temperature. The remote or local temperature sensors of the AFE10004-EP allow the PA temperature to be measured and the bias voltage adjusted accordingly. The D+ and D– pins of the AFE10004-EP are connected to a remote diode, which is located close to the power amplifiers.

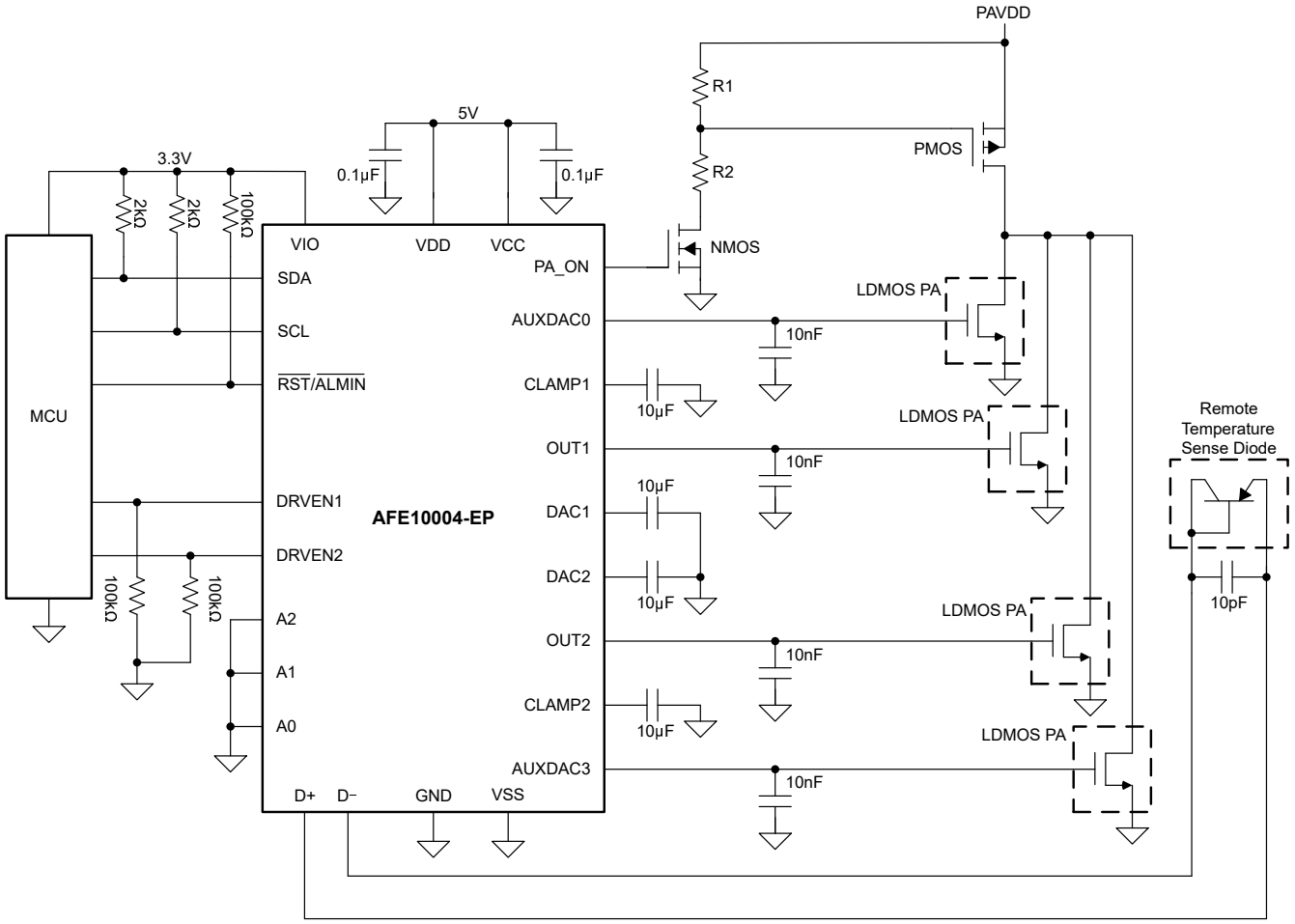


Figure 8-7. Typical LDMOS Application

ADVANCE INFORMATION

8.2.1.1 Design Requirements

Table 8-1 shows the design requirements for the circuit shown in Figure 8-7

Table 8-1. Design Requirements

PARAMETER	VALUE
V_{IO}	3.3V
V_{DD}	5V
V_{CC}	4.5V to 5.5V
V_{SS}	0V
DAC output range	0V to V_{CC}
Remote temperature sensing	One remote temperature diode driver
PAVDD isolation from power amplifier	External PMOS
PA bias voltage during power on	0V

8.2.1.2 Detailed Design Procedure

Use the following parameters to facilitate the design process.

- VCC and VSS voltage values
- DAC output voltage range
- Remote temperature sensing
- PAVDD isolation from the power amplifiers using PA_ON

8.2.1.2.1 Supply Voltage Selection

In LDMOS applications, ensure that the DAC range is positive. For the AFE10004-EP to operate in the positive range, connect the VSS supply pin to ground, and bias the VCC supply pin between 4.5V to 5.5V. The maximum output of the DAC is limited to be less than the VCC pin voltage. The output requires headroom from the V_{CC} supply, with additional voltage required when the DAC is sourcing current.

8.2.1.2.2 DAC Output Voltage Range

Express the DAC voltage output with the following equation, though the output maximum is limited by the V_{CC} supply.

$$V_{OUT}(DACIN) = -10V \times \left(1 - \frac{DACIN}{8192}\right) \quad (14)$$

8.2.1.2.3 Temperature-Sensing Applications

The AFE10004-EP has a local temperature and a temperature diode driver. Figure 8-8 shows a typical setup for the temperature diode-driver inputs. To achieve additional noise filtering, place a bypass capacitor across the inputs of the remote temperature sensors. Use a high-quality ceramic capacitor, type NP0 or X7R, because of the optimized performance of the capacitor across temperature. See also Section 6.3.3.3.

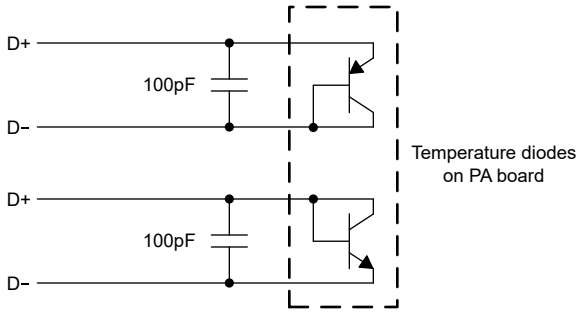


Figure 8-8. Remote Temperature Sensor

8.2.1.2.4 PAVDD Isolation From the Power Amplifier

The PAVDD voltage is separated from the drain voltage of the power amplifier with a series PMOS transistor. The activation of the PMOS transistor connects the PAVDD voltage supply to the drain pin of the power amplifier. The PMOS transistor is driven with a voltage divider that swings from PAVDD to PAVDD(R2 / (R1 + R2)). The NMOS transistor shown in Figure 8-7 is connected to the PA_ON output of the AFE10004-EP.

8.2.1.3 Application Curves

Figure 8-9 shows the OUT1, CLAMP1, and PA_ON outputs during start up with the AFE10004-EP configured in the positive range.

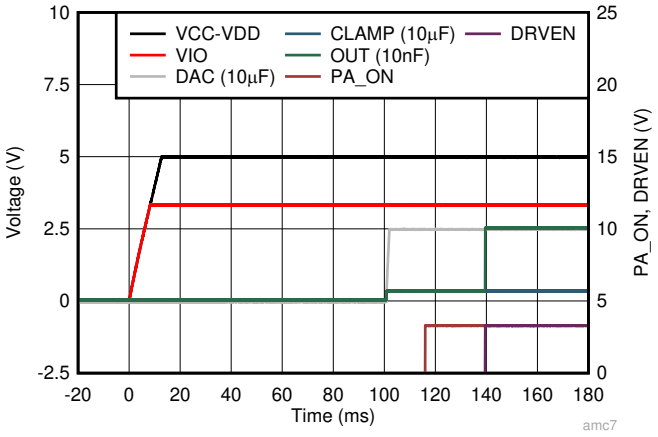


Figure 8-9. Positive Range Power-On Response

ADVANCE INFORMATION

8.2.2 Temperature-Compensated Bias Generator for a Gallium Nitride (GaN) Power Amplifier (PA)

A typical application for the AFE10004-EP is the biasing of GaN power amplifiers in RF systems. These applications require the bias voltage to be negative and to be adjusted over a wide operating temperature range to maintain a constant drain current through the PA. The remote or local temperature sensors of the AFE10004-EP allow the PA temperature to be measured and the bias voltage adjusted accordingly. The D+ and D– pins of the AFE10004-EP are connected to a remote diode, which is located close to the power amplifiers.

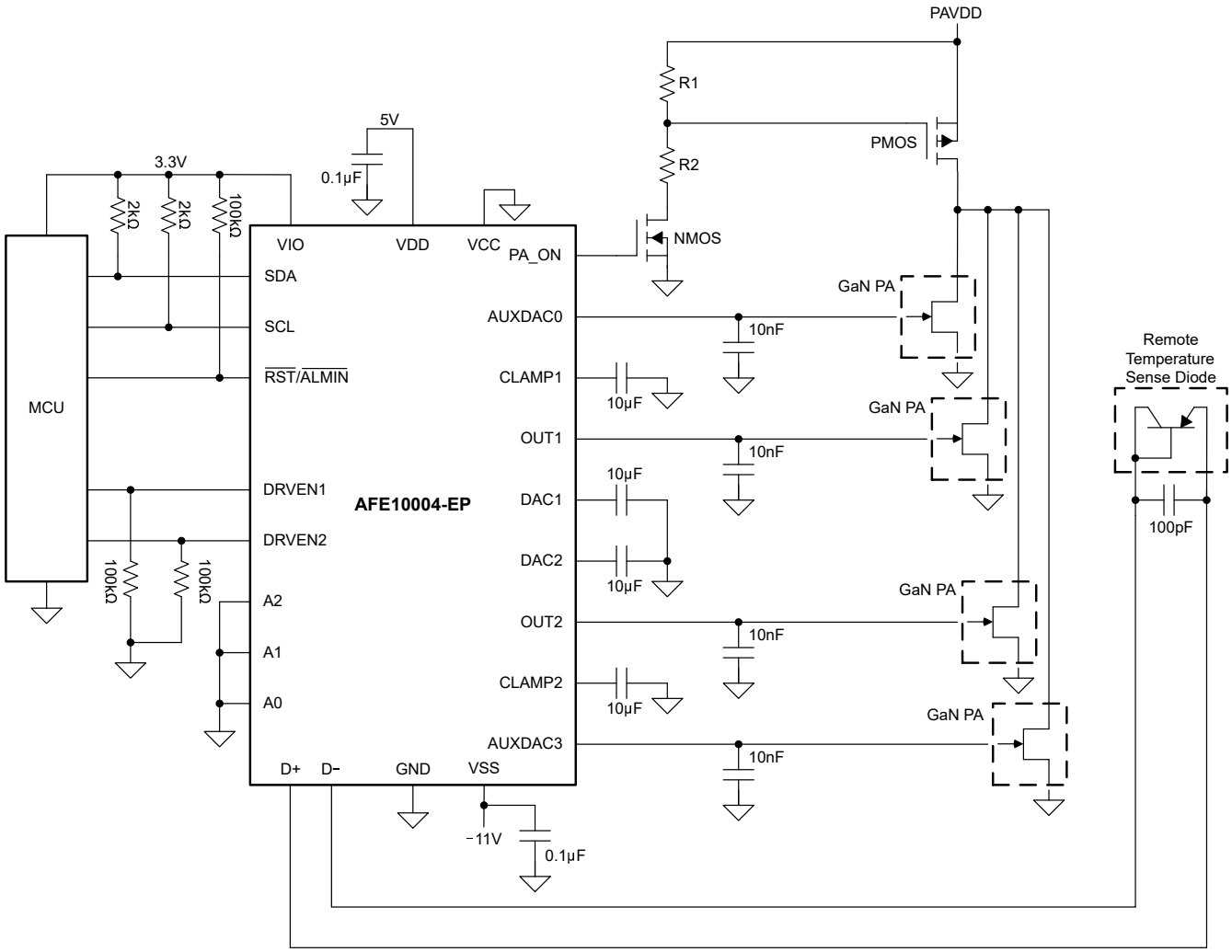


Figure 8-10. Typical GaN Application

8.2.2.1 Design Requirements

Table 8-2 shows the design requirements for the circuit shown in Figure 8-10.

Table 8-2. Design Requirements

PARAMETER	Value
V_{IO}	3.3V
V_{DD}	5V
V_{CC}	0V
V_{SS}	–4.5V to –11V
DAC output range	–10V or V_{SS} (whichever is greater) to 0V
Remote temperature sensing	One remote temperature diode driver
PAVDD isolation from power amplifier	External PMOS
PA bias voltage during power on	V_{SS}

8.2.2.2 Detailed Design Procedure

Use the following parameters to facilitate the design process:

- VCC and VSS voltage values
- DAC output voltage range
- Remote temperature sensing
- PAVDD isolation from power amplifier using PA_ON

8.2.2.2.1 Supply Voltage Selection

In GaN applications, the DAC range is negative. For the AFE10004-EP to operate in the negative range, ground the VCC pin while the VSS pin is between –4.5V and –11V. The DAC range is from –10V to 0V, with one caveat: ensure that the output of the DAC is only as low as the VSS pin voltage, with the addition of supply headroom. If the DAC is sinking current, the headroom is greater.

8.2.2.2.2 DAC Output Voltage Range

The DAC voltage output is expressed with the following equation, though the output minimum is limited by the V_{SS} supply.

$$V_{OUT}(DACIN) = -10V \times \left(1 - \frac{DACIN}{8192}\right) \quad (15)$$

8.2.2.3 Application Curves

Figure 8-11 shows the OUT1, CLAMP1, and PA_ON outputs during start up with the AFE10004-EP configured in the negative range.

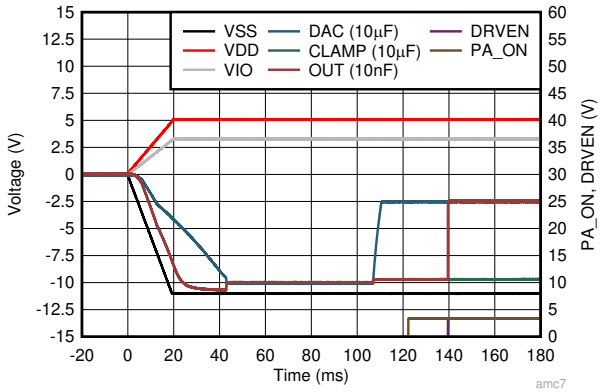


Figure 8-11. Negative Range Power-On Response

ADVANCE INFORMATION

8.3 Initialization Setup

To do the initial programming of the device EEPROM, follow these steps:

1. Write 1 to the LUTDIS field in the LUT Configuration register (page 1, address 0x0A).
2. Write the desired DAC code to the CLAMP1 overwrite and CLAMP2 overwrite (page 2, addresses 0x10 to 0x13).
3. Write the desired DAC BASE, polarity, and transfer coefficients to Pages 4 and 5.
4. Configure the other EEPROM registers located in page 1 accordingly.
5. When the register values have been configured, the values are mirrored into the nonvolatile EEPROM memory by writing the program code, 0xE4, to the EEPROM Burn register (page 15, address 0x7C). The EERDY field in the AMC Status register (page 1, address 0x05) indicate when the EEPROM programming is completed.
6. Power cycle the device, issue a software reset, or write 0 to the LUTDIS field for the device to enter the LUT mode.

8.4 Power Supply Recommendations

There is no required supply sequence, but be aware that the device stays in the reset state until all supplies reach the power-good threshold.

In applications where a negative voltage is applied to VSS first, some small negative voltages is potentially present at other supply pins, such as the VIO and VDD. The negative voltages at the supply pins potentially exceed the values listed in the *Absolute Maximum Ratings*, but because these voltages are created from intrinsic circuitry, the voltage levels are safe for operation.

8.5 Layout

8.5.1 Layout Guidelines

- Bypass all power supply pins to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitor has a value of 1µF and is ceramic with X7R or NP0 dielectric.
- Place capacitors on the DAC[0:3], CLAMP[1:2] and OUT[1:2] pins as close to the device as possible. This placement reduces the impact of parasitic inductance and resistance from the switching path. Parasitic inductance and resistance delays the output settling time.
- Connect the thermal pad on the device to a large copper area, preferably a ground plane.
- When using the local temperature sensor for the output bias voltage temperature compensations, place the device geographically close to the PA, preferably sharing a solid ground plane for thermal conduction.

ADVANCE INFORMATION

8.5.2 Layout Example

8.5.2.1 Positive Output Range Layout Example

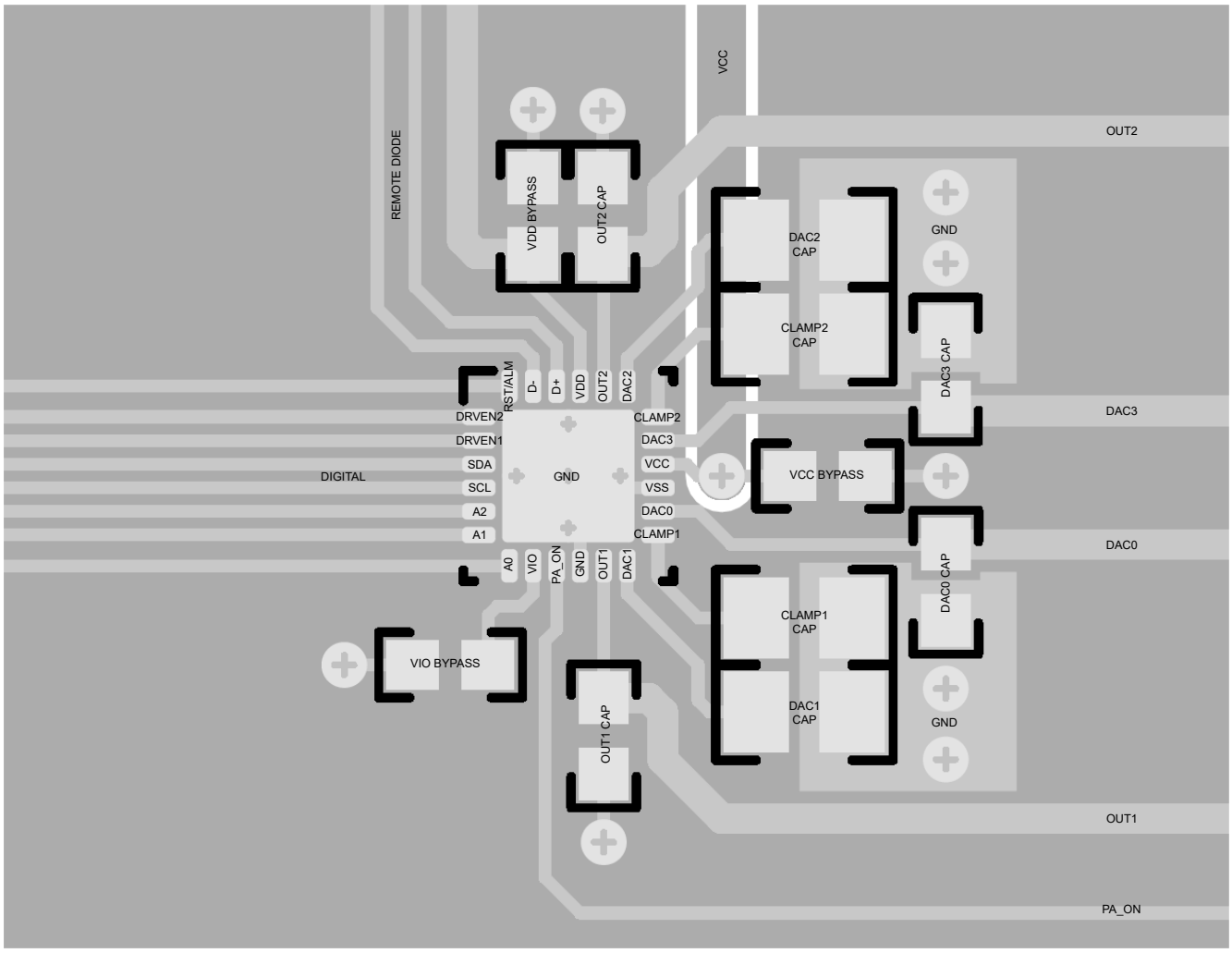


Figure 8-12. Positive Output Layout Example

ADVANCE INFORMATION

8.5.2.2 Negative Output Range Layout Example

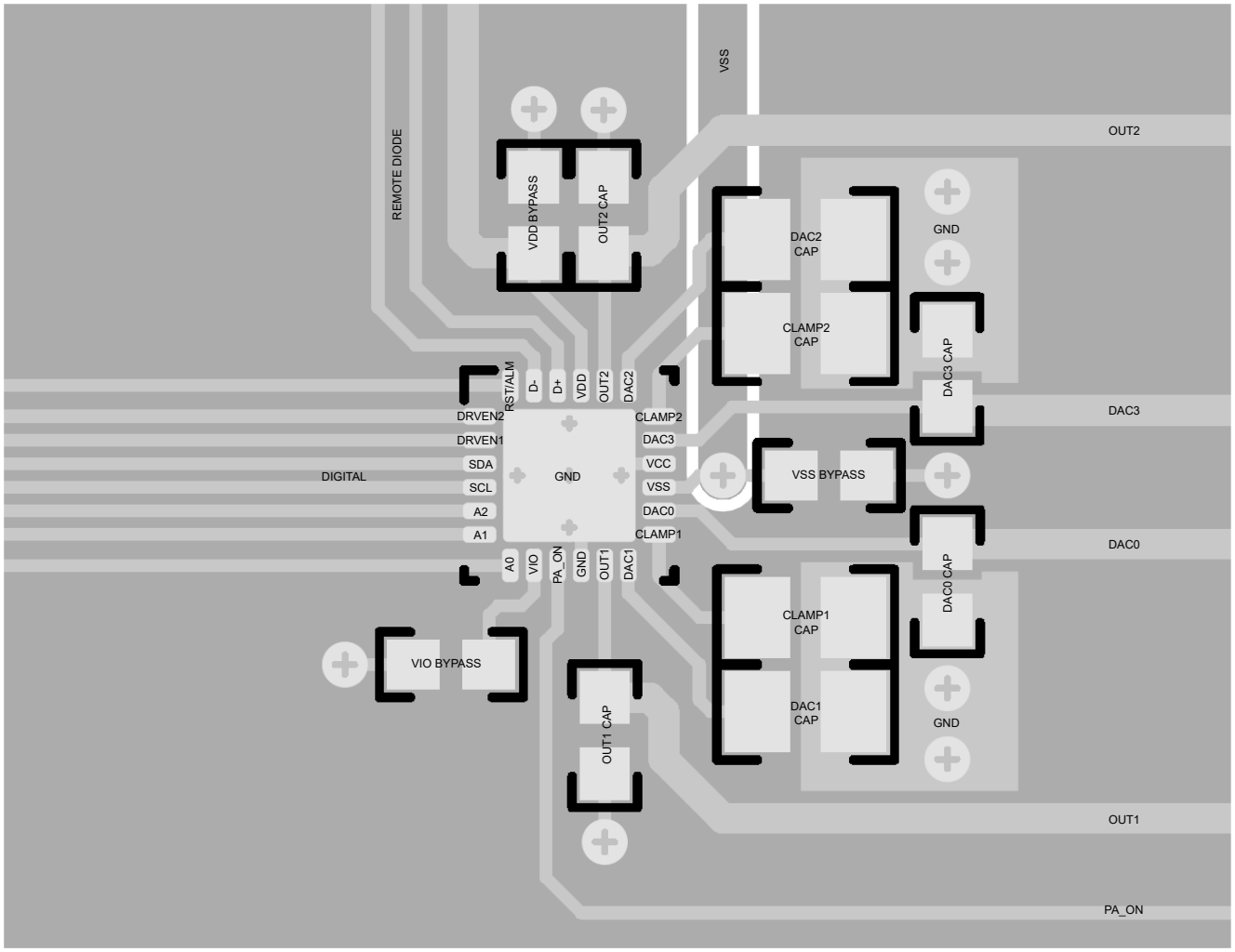


Figure 8-13. Negative Output Layout Example

9 Device and Documentation Support

9.1 Documentation Support

Note

TI is transitioning to use more inclusive terminology. Some language can be different than what is expected for certain technology areas.

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, AFE10004EVM user's guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
June 2025	*	Initial release.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

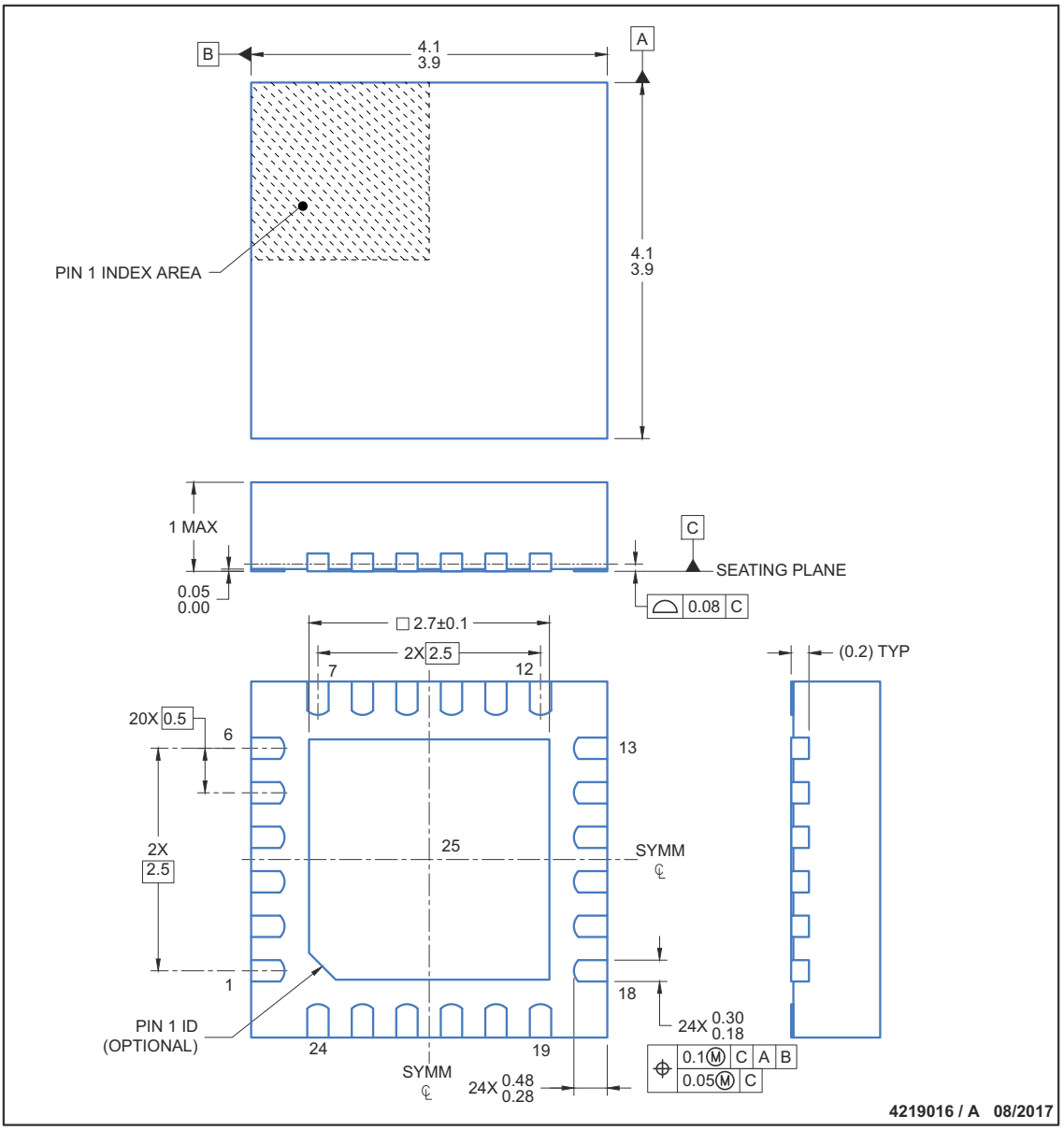
ADVANCE INFORMATION

PACKAGE OUTLINE

RGE0024H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

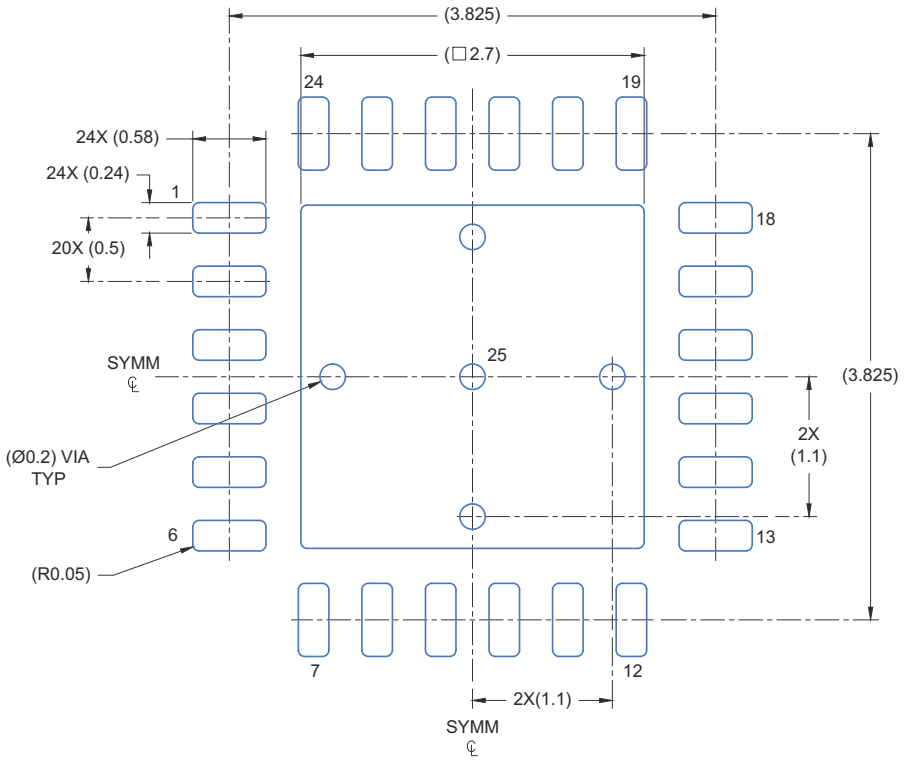
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

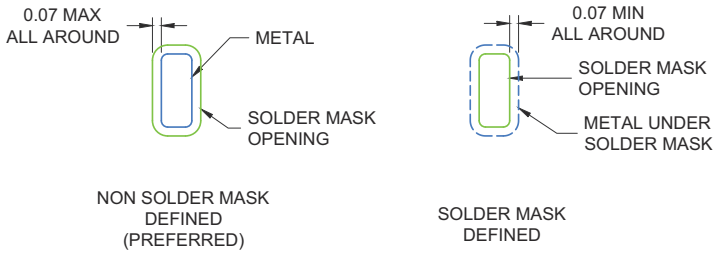
RGE0024H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

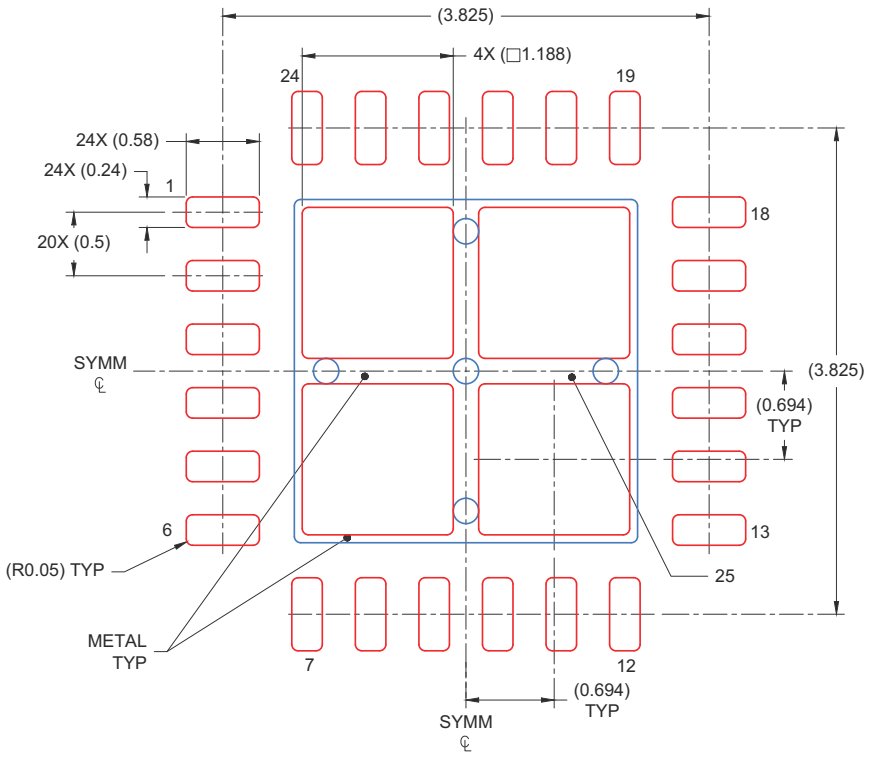
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGE0024H — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PAFE10004RGETEP	Active	Preproduction	VQFN (RGE) | 24	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF AFE10004-EP :

- Catalog : AFE10004

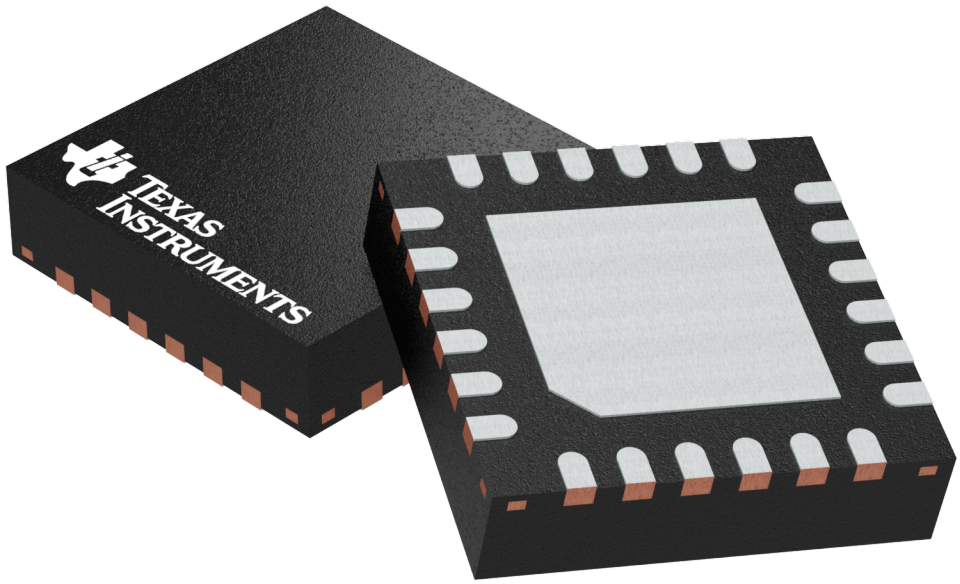
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

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