64 Channel Analog Front End for Digital X-Ray Detector

Check for Samples :AFE0064

FEATURES

- **64 Channels**
- **28.32 µSec Min Scan Time (including integration and data transfer for all 64 channels)**
- **7.5 MHz Max Data Transfer Rate**
- **Noise 824 e-RMS with 30 pF Sensor Capacitor in 1.2 pC Range**
- **Integral Nonlinearity: ±0.006% of FSR**
- **Eight Adjustable Full Scale Ranges (0.13 pC min to 9.5 pC max)**
- **Built in CDS (signal sample – offset sample)**
- **Selectable Integration Up/Down Mode**
- **Low Power: 175 mW**
- **NAP Mode: 49.5 mW**
- **14 mm × 14 mm 128 Pin TQFP Package**

APPLICATIONS

- **Digital Radiography**
- **CT Scanners**
- **Baggage Scanners**
- **Infrared Spectroscopy**

DESCRIPTION

The AFE0064 is a 64 channel analog front end designed to suit the requirements of flat panel detector based digital X-ray systems.

The device includes 64 integrators, a PGA for full scale charge level selection, correlated double sampler, 64 as to 2 multiplexer, and two differential output drivers.

Hardware selectable Integration polarity allows integration of a positive or negative charge and provides more flexibility in system design. In addition, the device features TFT (Thin Film Transistor from Flat Panel Detector) charge injection compensation. This feature helps maximize the usable signal charge range of the device.

The nap feature enables substantial power saving. This is especially useful for power saving during long X-ray exposure periods.

The AFE0064 is available in a 128 pin TQFP package.

ORDERING INFORMATION(1)

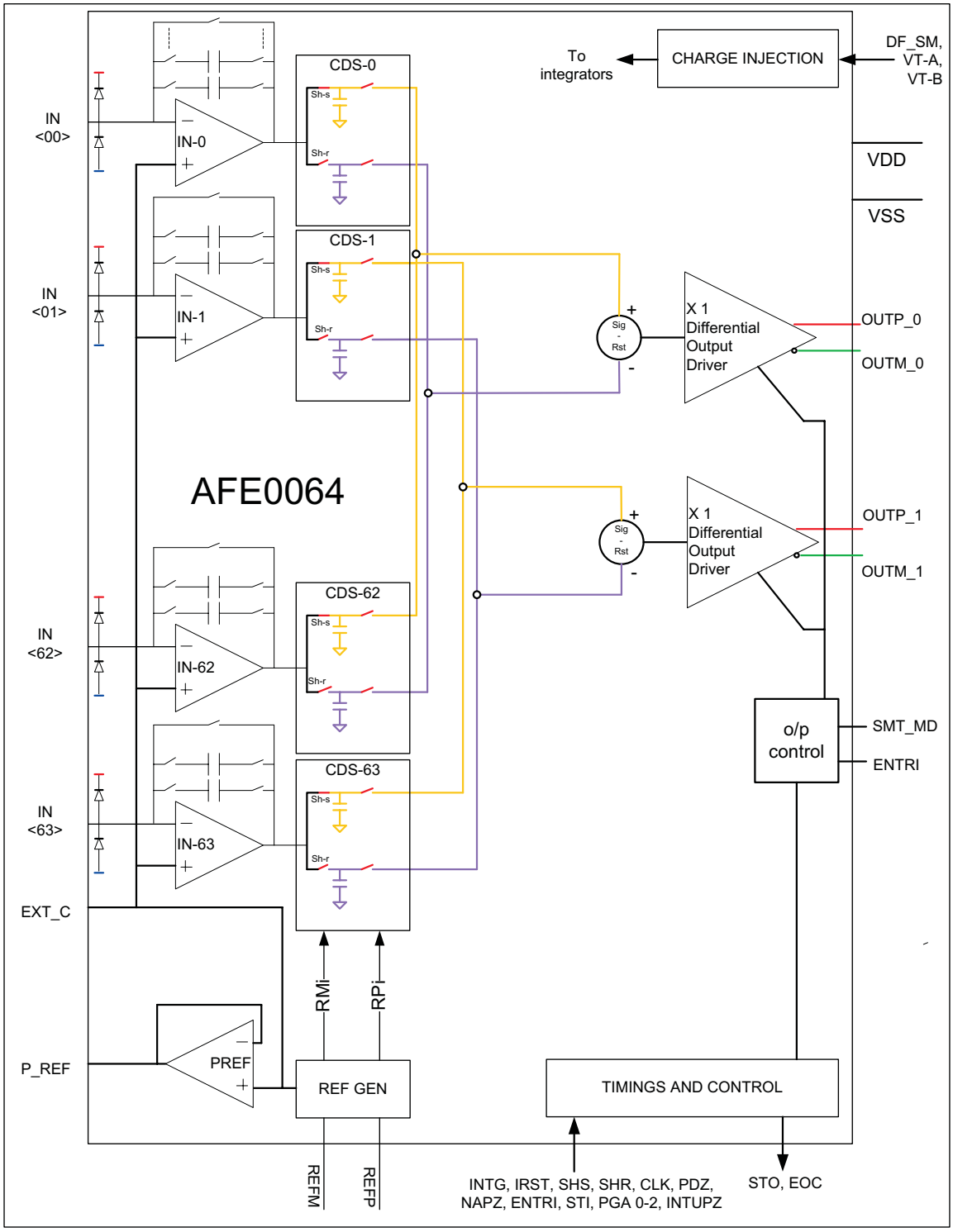
MODEL	INTEGRAL LINEARITY % of FS	POWER DISSIPATION	MIN SCAN TIME (µSec)	NUMBER OF CHANNELS	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
AFE0064	0.006	175 mW	28.32	64	TQFP	PBK	–40 to 85°C	AFE0064IPBK	90(5+1)
								AFE0064IPBKR	1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE / UNIT
IN <n> to VSS		–0.3 V to +VDD + 0.3 V
VDD to AGND		–0.3 V to 5 V
Digital input voltage to GND		–0.3 V to (+VDD + 0.3 V)
Digital output to GND		–0.3 V to (+VDD + 0.3 V)
Operating temperature range		–40°C to 85°C
Storage temperature range		–65°C to 150°C
Junction temperature ($T_J$max)		150°C
TQFP package(2)	Power dissipation	(T_J max – T_A)/ θJA
	θJA Thermal impedance	45°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device confirms to MSL level 3 at 260°C as per JEDEC -033.

SPECIFICATIONS

T_A = 25 to 85°C, +VDD = 3.3 V, f_{CLK} = 15 MHz for sequential mode and 3.75 MHz for simultaneous mode, scan time = 28.32 µs (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT RANGE					
Range 0			0.13		pC
Range 1			0.25		pC
Range 2			0.5		pC
Range 3			1.2		pC
Range 4			2.4		pC
Range 5			4.8		pC
Range 6			7.2		pC
Range 7			9.6		pC
Input current			30		µA
Integrator positive input voltage		1.66	1.68	1.70	V
ANALOG OUTPUT					
Differential full scale analog output	For all ranges	–(REFP-REFM)	±1.4	(REFP-REFM)	V
Output common-mode voltage (REFP+REFM)/2			1.55		

SPECIFICATIONS (continued)

T_A = 25 to 85°C, +VDD = 3.3 V, f_{CLK} = 15 MHz for sequential mode and 3.75 MHz for simultaneous mode, scan time = 28.32 µs (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACCURACY					
Noise in electrons referred to input of integrator	C-sensor(1)1= 30 pF, Range 3, 14 µSec integration time		824		e-
	C-sensor(1) = 20 pF, Range 3 14 µSec integration time		600		
	C-sensor(1)= 30 pF, Range 3, 270 µSec integration time		1400		
Integral nonlinearity			±0.006		% of FSR(2)
Analog input channel leakage current	This current is integrated and reflects as a part of offset error.		2		pA
Channel to channel full-scale error matching	For ranges 3 to 7		±0.7		% of FSR(2)
Offset error	Device output offset, resulting from integration of input leakage current		±0.07		% of FSR(2)
Channel to channel offset error matching			±0.07		% of FSR(2)
Integrator input offset:(difference between integrator positive and negative terminal)	Integrator input offset mean across channels		±0.002		mV
Integrator input offset matching across channels	±3 sigma limit of integrator input offset across channels		±1.5		mV
Channel to channel crosstalk	Aggressor channel with full scale charge to next adjacent channel		0.08		% of FSR(2)
EXTERNAL REFERENCE INPUT					
REFP		2.24	2.25	+VDD - 0.85	V
REFM		0.84	0.85	0.86	V
Input current			50		nA
P_REF output			1.68		V
P_REF current source capacity			±1		mA
POWER SUPPLY REQUIREMENTS					
Power supply voltage, +VDD		3.2	3.3	3.6	
Power supply current	During operation		53	58	mA
	During NAP		15		mA
Power up time from NAP			10		µSec
DIGITAL INPUT OUTPUT					
Logic levels					
V_{IH}		0.8×VDD		VDD+0.1	
V_{IL}		–0.1		0.2×VDD	
V_{OH}	I_{OH} = -500 µA	VDD–0.4			
V_{OL}	I_{OL} = 500 µA			0.4	
TEMPERATURE RANGE					
Operating free air		0		85	°C

(1) C-Sensor is total external capacitance seen at IN(x) pin. This includes capacitance of all the TFT switches connected to that node and the routing capacitance.
(2) FSR is full-scale range. There are eight ranges from 0.13 pC to 9.6 pC.

TIMING REQUIREMENTS

T_A = 0 to 85°C, +VDD = 3.3 V

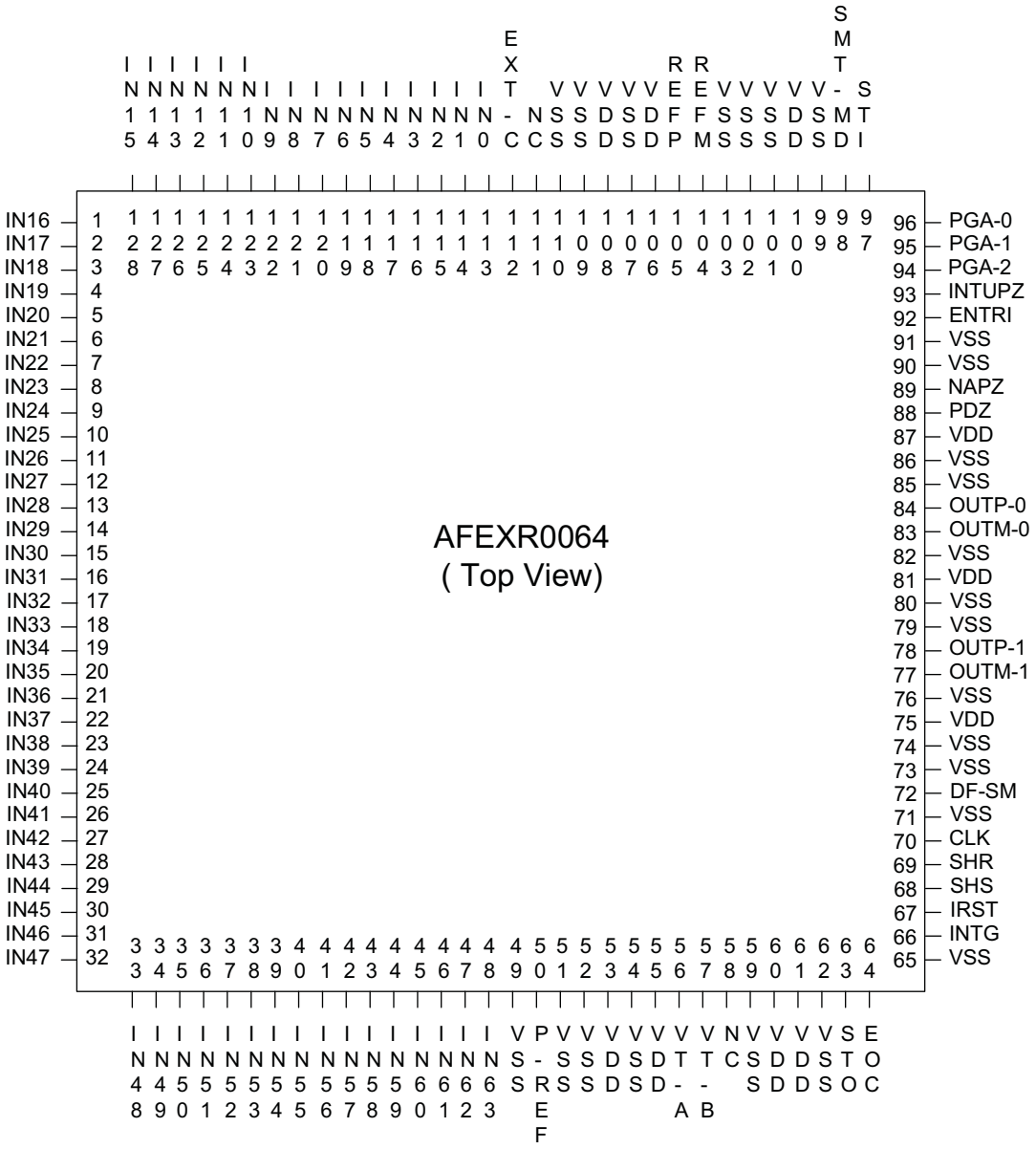
PARAMETER		MIN	TYP	MAX	UNIT
SAMPLING AND CONVERSION RELATED					
t-scan	Scan time, See Figure 1, Figure 7	28.32		See (1)	µSec
t1	IRST, SHR, SHS, STI high duration, See Figure 1, Figure 7	30			nSec
t2	Setup time, STI falling edge to first clock rising edge, See Figure 1, Figure 7	30			nSec
t2	Setup time, IRST falling edge to first clock rising edge, See Figure 1, Figure 7	30			nSec
t3	Delay time, 133rd clock rising edge to SHR rising edge, See Figure 1, Figure 7	400			nSec
t4	Delay time, SHR rising edge to INTG rising edge, See Figure 1, Figure 7	30			nSec
t5	INTG high duration (TFT on time), See Figure 1, Figure 7	14		See (2)	µSec
t6	Delay time, INTG falling edge to SHS rising edge, See Figure 1, Figure 7	4.5			µSec
t7	Delay time, SHS rising edge to IRST rising edge, See Figure 1	30			nSec
t8	Delay time, SHS rising edge to STI rising edge, See Figure 1, Figure 7	30			nSec
t9	Hold time, STI falling edge to IRST falling edge, See Figure 1, Figure 7	10			nSec
In sequential mode	Clock (CLK) frequency	1		15	MHz
In simult mode		0.25		3.75	
	OUTP or OUTM settling time to 16 bit accuracy with 30 pF load and full scale step			375	nSec
	OUTP or OUTM settling time to 16 bit accuracy with 15 pF load and full scale step			250	nSec

(1) See max specification for t5 and minimum specification for CLK frequency. Also see the section Running the Device at Higher Scan Time.

(2) There is no real limit on maximum integration time, however as integration time increases the offset value changes due to integration of leakage current (2 pA typical) also the 1/f noise contribution to output increases, refer to the typical noise numbers at 14 and 270 µSec integration time in the Specifications table and also see Figure 28 .

DEVICE INFORMATION

PIN ASSIGNMENTS



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NUMBER	NAME		
ANALOG INPUT PINS			
113..128	IN<0>… IN<15>	I	Analog input channels from 0 to 63
1.. 48	IN<16>… IN<63>	I	
DIFFERENTIAL ANALOG OUTPUT PINS			
84	OUTP-0	O	Driver 0-analog output positive terminal
83	OUTM-0	O	Driver 0-analog output negative terminal
Driver 0 outputs analog data for channels 31 to 0			

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NUMBER	NAME		
78	OUTP-1	O	Driver 1-analog output positive terminal
77	OUTM-1	O	Driver 1-analog output negative terminal
Driver 1 outputs analog data for channels 63 to 32			
Note that the device output is differential (OUTP-OUTM) with common mode of (OUTP+OUTM)/2			
REFERENCE			
105	REFP	I	Positive reference input
104	REFM	I	Negative reference input
Decouple REFP and REFM terminals to VSS with suitable capacitor and use low noise reference, noise on these terminals will add to noise at output terminals.			
112	EXT_C	O	Terminal available for decoupling internally generated integrator common-mode voltage (1.68 V). Decouple this pin to VSS with 1 µF ceramic capacitor. Internally connected to +ve terminals of all 64 integrators.
50	P_REF	O	Internally generated 1.68 V reference output available for referencing photodiode cathodes.
CONTROL PINS			
63	STO	O	Delayed ST for cascading next ASIC
64	EOC	O	End of data shifting, EOC is low during data read.
66	INTG	I	Filter bandwidth control for Signal sample (SHS). Filter BW is high when this signal is high and filter BW is low when this signal is low. Typically this signal should go high with TFT switch turn on and should go low ~0.5 µSec after TFT switch off.
67	IRST	I	Resets the integrator capacitors on rising edge of this input.
68	SHS	I	Device samples 'signal' level of integrator output(0 to 63) onto the respective CDS on rising edge of this input.
69	SHR	I	Device samples 'reset' level of integrator output (0 to 63) onto the respective CDS on rising edge of this input.
70	CLK	I	For simultaneous mode: Device serially outputs the analog voltage from each integrator channel on each rising edge of CLK.
			For sequential mode: Device serially outputs the analog voltage from each integrator channel on every fourth rising edge of CLK.
88	PDz	I	Low level puts device in powerdown mode.
89	NAPz	I	Low level puts device in NAP mode, this is useful for power saving during X-ray exposure period.
92	ENTRI	I	High on this pin enables 3-state of analog output drivers after shift out of data for all 64 channels.
97	STI	I	Rising edge resets the channel counter. Falling edge enables data transfer on OUTP and OUTM terminals.
PGA-I/P RANGE SELECTION			
94	PGA-2	I	Selects eight different analog input ranges. Three bit word with these three bits represents binary number corresponding to Analog Input Range. PGA-2 is MSB and PGA-0 is LSB. Example 000 is range 0 and 100 is range 4.
95	PGA-1	I	
96	PGA-0	I	
MODE SELECTION			
93	INTUPz	I	High level selects 'integration-down' mode. In this mode device integrates positive pixel current into each channels, starting from reset level (REFP) down to REFM low level selects 'integration-up' mode. In this mode the device integrates negative pixel current into each channel, starting from reset level (REFM) up to REFP.
98	SMT-MD	I	High level selects simultaneous mode. Device outputs data simultaneously on both differential output drivers OUTP-OUTM<0> and OUTP-OUTM<1> in this mode. Low level on this input selects sequential mode. In this mode device output data for driver 0 is skewed by two clocks from driver 1. This is useful when a two channel multiplexed ADC is used after AFE.
POWER SUPPLY			
53, 55, 60, 61, 75, 81, 87, 100, 106, 108	VDD	I	Device power supply

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NUMBER	NAME		
49, 51, 52, 54, 59, 62, 65, 71, 73, 74, 76, 79, 80, 82, 85, 86, 90, 91, 99, 101, 102, 103, 107, 109, 110	VSS	I	Ground for device power supply
TFT CHARGE INJECTION COMPENSATION			
72	DF-SM	I	Digital control to dump compensation charge on integrator capacitor; this is useful to nullify the effect of pixel TFT charge injection.
56	VT-A	I	External voltage to control the amount of charge dump for TFT charge injection compensation. Charge dump = (V-voltage at 'EXT_C')*0.857 pC where V is external voltage at pins 56, 57. Short pins 56 and 57 externally and apply external voltage for charge injection compensation.
57	VT-B	I	
NC PINS			
58, 111			These pins should be connected to VSS.

DESCRIPTIONS AND TIMING DIAGRAMS

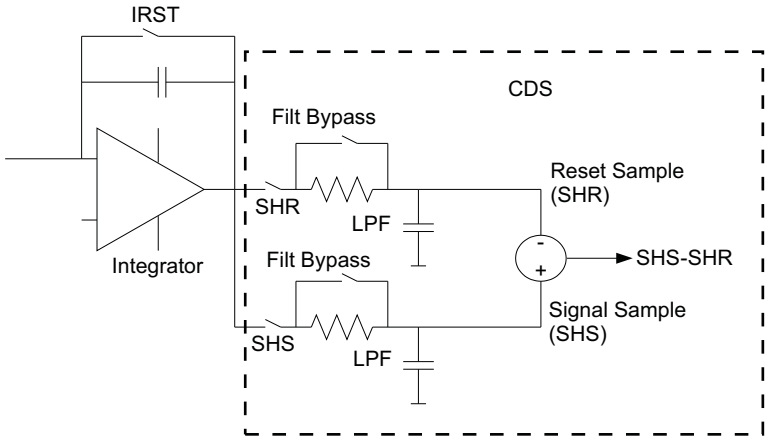


Figure 1. Integrator Channel Schematic

Figure 1 shows the typical schematic of an integrator channel. As shown, each integrator has a reset (IRST) switch which resets the integrator output to the 'reset-level'. The device integrates input current while this switch is open. There are two sample and hold circuits connected to each integrator output. SHR samples integrator reset level output and SHS samples integrator output post integration of signal charge. The device subtracts the SHR sample from the SHS sample. The difference is then available at device output in a differential format. This action is called 'Correlated Double Sampling' (CDS). CDS removes integrator offset and low frequency noise from device output.

Each sample and hold has a built-in low pass filter. This filter limits sampling bandwidth so as to limit sampled noise to an acceptable level. Detailed functioning of individual blocks is described further with timing diagrams.

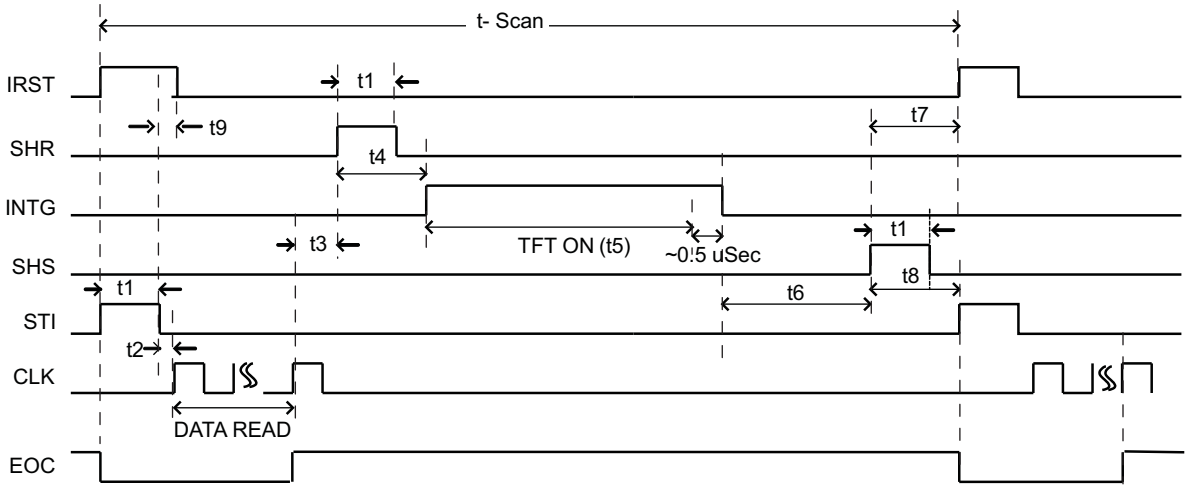


Figure 2. Integration and Data Read

As shown in Figure 2, the device performs two functions, 'Integration' and 'Data Read' during each scan (indicated by 't-Scan'). Signals IRST, SHR, SHS, INTG, CLK control 'Integration Function' and STI, CLK control 'Data Read Function'. EOC is a device output and a low level on the EOC pin indicates a data read is in progress.

Charge Integration

Integration function consists of two phases namely 'Reset' and 'Integration'.

IRST rising edge starts the 'Reset' phase which ends with SHR rising edge. Figure 3 shows the detailed timing waveform for the reset phase.

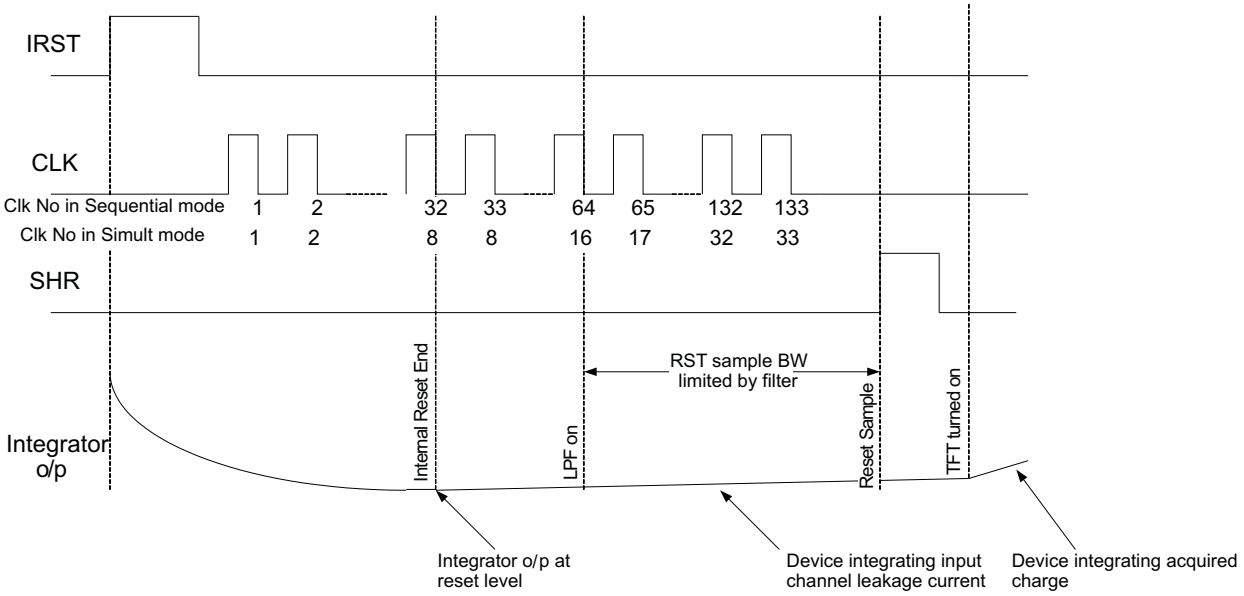


Figure 3. Timing Diagram Showing Details of Reset Phase

In this phase the device resets all 64 integration capacitors. This reset-level voltage depends on the integration mode (selected by the INTUPz pin). Integrator output is reset to REFM for 'integration-up' mode and is reset to REFP in 'integration-down' mode. Note that the integrator reset switch is on from IRST rising edge to the end of the 32nd clock for sequential mode and up to the 8th clock for simultaneous mode. SHR and filter bypass switches (see Figure 1) are on right from IRST rising edge to the 64th clock falling edge.

In this period, the reset sample capacitor is tracking the integrator output voltage. On the 64th CLK falling edge, the filter bypass switch is opened. This kicks in the low pass filter. The filter has a fixed time constant of 1 µSec (160 kHz BW). The device samples and holds (SHR switch opens) the integrator reset output at rising edge of SHR. The low pass filter cuts off high frequency noise during sampling.

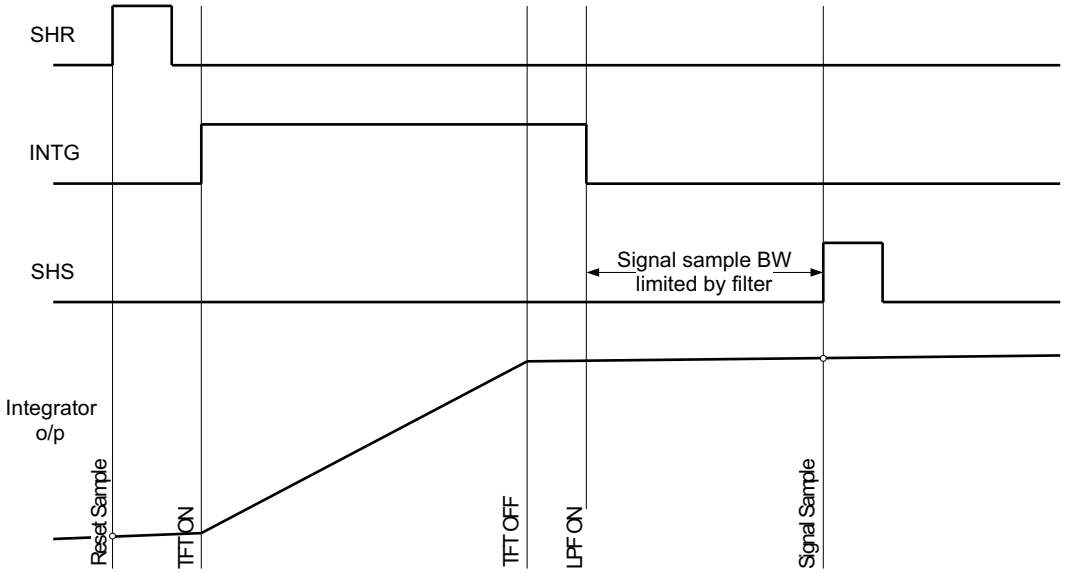


Figure 4. Timing Diagram Showing Details of Integration Phase

Here after the integration phase starts. The device integrates pixel charge during on time of the external TFT switch. The device integrates pixel charge starting from the reset level (as described previously).

In integration up mode, the integrator output moves up from REFM (reset level). As shown in the Specifications table there are 8 different ranges for the integrator. For any range, the device can linearly integrate input charge until the integrator output reaches REFP.

In integration down mode, the integrator output moves down from REFP (reset level). For any analog input range , the device can linearly integrate input charge until the integrator output reaches REFM.

It is clear that the linear output range for the integrator is 'REFP-REFM' volts. One can calculate the integrator feedback capacitor with formula; Q = CV. Here Q is the specified charge for range '0 to 7' and V is the linear output range of the integrator (REFP-REFM). Refer to Table 1 for more details.

It is recommended to assert (pull high) the INTG signal along with TFT switch turn on. Note that the TFT switch is external to the device, and the device still integrates without the INTG signal. INTG can be held high for 0.5 µSec after TFT switch turn off. This makes sure the SHS low pass filter is bypassed all through integration and for 0.5 µSec after integration. This extra 0.5 µSec ensures charge injection during TFT switch turn off is settled and the SHS sampling capacitor is tracking the integrator output. As shown in Figure 4, the device turns on the LPF on the falling edge of INTG. Like SHR sampling, this filter has a 1 µSec time constant (160kHz BW), and it cuts off high frequency noise during sampling. Timing 't6' in the Timing Requirements table specifies that the settling of voltage on the SHS capacitor is close to the 16 bit level while filter BW is low.

On the rising edge of SHS, the device samples and holds integrator output voltage on the correlated double sampler (CDS). The CDS output voltage is proportional to the difference of the 'SHS' and 'SHR' samples. This scheme removes offset and noise coming from integrator reset. The integration phase ends with the SHS falling edge and data corresponding to all 64 channels is ready to read during the next 'scan'.

Data Read:

Device output is differential even though the integrator output (internal to device) is single ended. Here is the relation between integrator output and AFE0064 output (OUTP and OUTM):

Case 1: (Integrator up mode, INTUPz = 0)

As explained before the device samples the integrator output twice, Reset sample (SHR) and Signal sample (SHS).

$V_{OUTM} = REFM + (V_{SHS} – V_{SHR})$
$V_{OUTP} = REFP – (V_{SHS} – V_{SHR})$

Case 2: (Integrator down mode, INTUPz = 1)

As explained before the device samples the integrator output twice, Reset sample (SHR) and Signal sample (SHS).

$V_{OUTM} = REFP + (V_{SHS} – V_{SHR})$
$V_{OUTP} = REFM – (V_{SHS} – V_{SHR})$

The differential output from the AFE0064 rejects common-mode noise from the board helping to maximize noise performance of the system. The following table provides details of integrator feedback ranges, feedback capacitor, and corresponding AFE0064 output at zero and full scale input charge.

Table 1. AFE0064 Range Selection to Device Analog Output Mapping

REFP	2.25	REFP-REFM	1.4							
REFM	0.85									
			INTEGRATE UP MODE (INTUPz=0), e– counting				INTEGRATE DOWN MODE (INTUPz=1), hole+ counting			
			At 0 charge I/p		At FS charge I/p		At 0 charge I/p		At FS charge I/p	
Range	Typical FS Charge Range (Qr) pC	Int FB Cap= (Qr)/ (REFP-REFM) … pF	OUTP	OUTM	OUTP	OUTM	OUTP	OUTM	OUTP	OUTM
0	0.13	0.0929	2.25	0.85	0.85	2.25	0.85	2.25	2.25	0.85
1	0.25	0.1786								
2	0.5	0.3571								
3	1.2	0.8571								
4	2.4	1.7143								
5	4.8	3.4286								
6	7.2	5.1429								
7	9.6	6.8571								

The following section provides detailed timing of data read. There are two output drivers. Data for channel number 63 to 32 is available on output driver 1 and data for channel number 31 to 0 is available on output driver 0. Data from two drivers can be available simultaneously or sequentially depending on the status of pin SMT_MD.

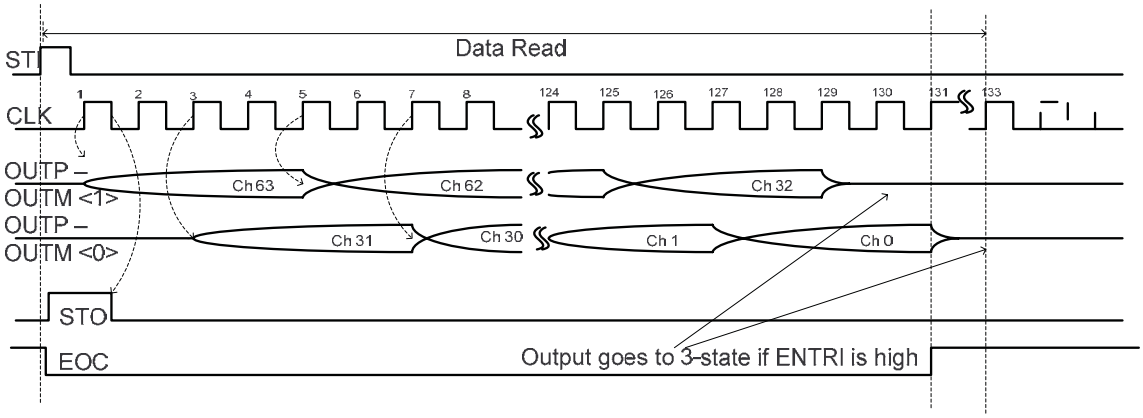


Figure 5. Device Data Read in Sequential Mode (SMT_MD = 0)

A high pulse on STI activates the data read function and resets the channel counter to zero. As shown in Figure 5, the device outputs the analog voltage from channel 63 on the first rising edge of CLK after STI falling edge. Channel 63 to 32 data is available on the OUTP<1> and OUTM<1> terminals. Next the lower output channel is connected to the output after four clocks.

Data on the OUTP<0> and OUTM<0> terminals is skewed by two clocks with respect to OUTP<1> and OUTM<1>. Channel 31 to 0 data is available on the OUTP<0> and OUTM<0> terminals.

The skew between the two output drivers allows the user to connect a two channel multiplexed input ADC to the AFE output.

The device output goes to 3-state after all of the data on the particular differential output driver (0 or 1) is transferred, if ENTRI is tied to high level. Otherwise, both differential output drivers stay at output common-mode voltage after data transfer.

Maximum Data Transfer Rate: As shown in Figure 5, the device outputs new channel data on every alternate rising edge of the clock. Effectively the data transfer rate is one-half of the clock speed. The maximum data transfer rate is 7.5 MHz as the device supports a maximum 15 MHz clock frequency.

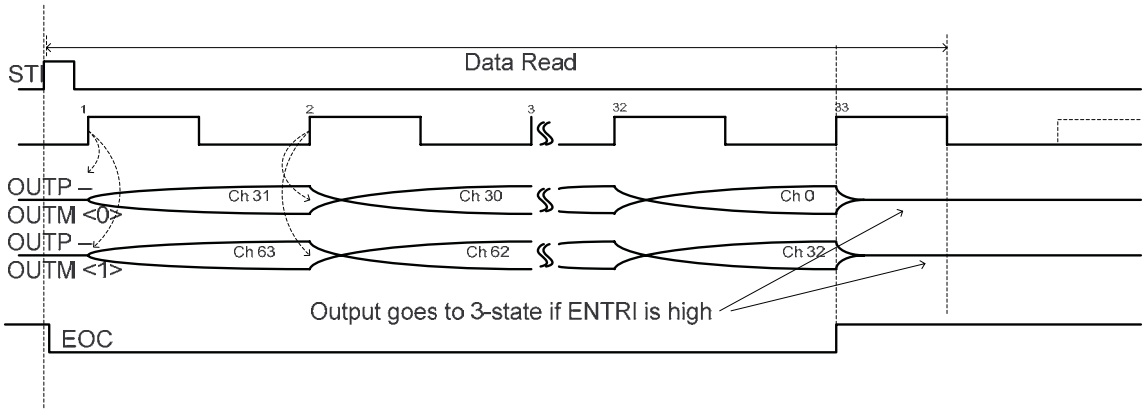


Figure 6. Device Data Read in Simultaneous Mode (SMT_MD=1)

A high level on the 'SIMULT_MODE' pin selects simultaneous mode. the device outputs data simultaneously on both differential output drivers OUTP-OUTM<0> and OUTP-OUTM<1> in this mode. This means the device outputs both Ch31 and Ch63 outputs on the first rising edge of the clock, Ch30 and Ch62 on the 2nd rising edge and so on. This mode is useful when two separate single channel ADCs or one simultaneous sampling ADC is used to digitize OUTP-OUTM<0> and OUTP-OUTM<1>. Unlike sequential mode, simultaneous mode needs only 33 clocks to read all 64 channels of data. In this case the output data transfer rate per output driver is the same as the clock frequency. The device can work at a maximum clock frequency of 3.75 MHz.

Running the Device at Minimum Scan Time:

Minimum scan time is achieved if a data read overlaps the reset phase (as shown in Figure 1). This can be done if an IRST rising edge and STI rising edge occur simultaneously. It is recommended to stop the clock after the device receives 133 clocks after STI falling edge, if sequential mode selected (or 33 clocks if simultaneous mode is selected). It is possible to keep the clock free running throughout the scan, but it can potentially deteriorate noise performance. With t-scan (min) = t1+t2+132 (t-clk)+t3+t4+t5+0.5µSec+t6+t7 and all timing values used are the minimum specified values, then t-scan (min) = 28.32 µSec.

Running the Device at Higher Scan Time (for lesser frame rate):

It is possible to run the device at a higher scan time to achieve a lesser frame rate without affecting performance. (Note that violating the maximum limits on the specified timings and also the minimum specification on the clock frequency results in charge leakage on the integration or CDS capacitors. This causes additional offset and gain errors.)

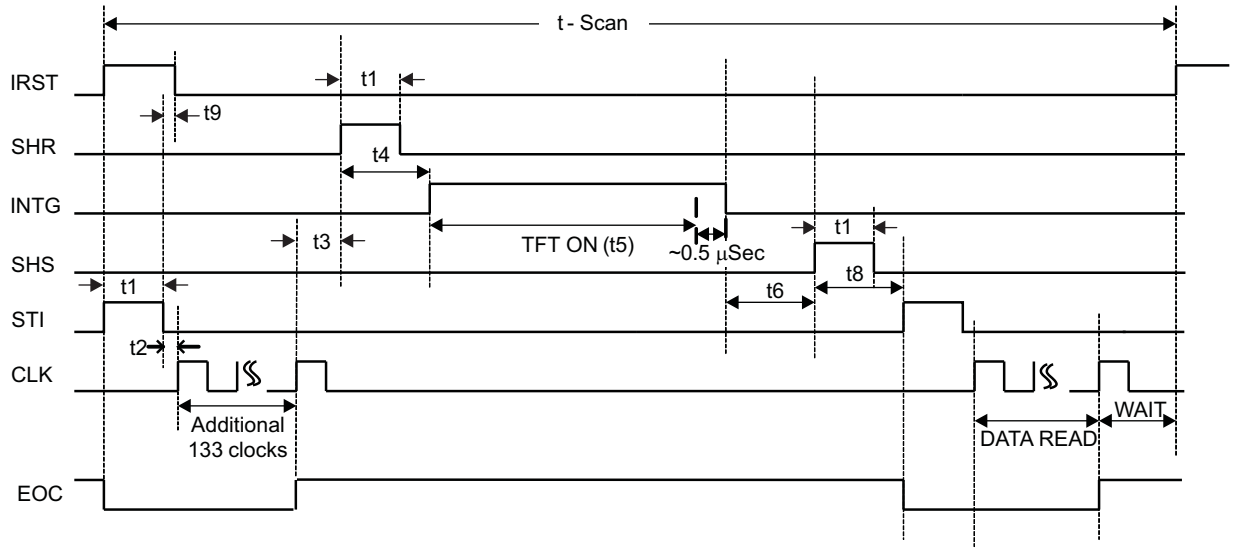


Figure 7. Device Operation at Higher Scan Times (sequential mode shown, however the same is possible for simultaneous mode)

As shown in Figure 7, a data read can be started by issuing a STI pulse after SHS and well before IRST. In this case the device goes into a 'wait' state after the data read is complete. The device remains in this wait state until it receives IRST and STI rising edges. Note that the clock can be stopped (or kept running) in the wait state however it is necessary to provide an additional 133 or 33 clocks after IRST falling edge depending on sequential or simultaneous mode selection respectively. It is recommended to stop the clock after the device receives 133 or 33 clocks depending on mode selection until the next STI pulse. This helps to get maximum SNR from the device. However it is allowed to use a free running clock.

Cascading Two AFE0064 Devices to Scan 128 Channels:

It is possible to cascade two AFE0064 devices to scan 128 channels. This feature is useful for sequential mode and allows the use of a 4 channel, multiplexed input ADC for two AFEs.

In that case, STO of device 1 is connected to STI of device 2. Other control pins (INTG, IRTS, SHR, SHS, CLK) of both devices are connected to each other.

As shown in figure 8, STO falling edge is delayed by one clock from STI falling edge. (STO falling edge aligns with first clock falling edge.) Device 2 data out starts with the second clock rising edge (the first CLK rising edge after STI falling edge for device 2). Effectively, data from the four output drivers of the two devices is presented on every rising edge in the following sequence:

Clock 1,5,9...: OUT-1 of Device 1
Clock 2,6,10...: OUT-1 of Device 2
Clock 3,7,11...: OUT-0 of Device 1
Clock 4,8,12...: OUT-0 of Device 2

Note this output sequence when connecting a multiplexed input ADC at a device output.

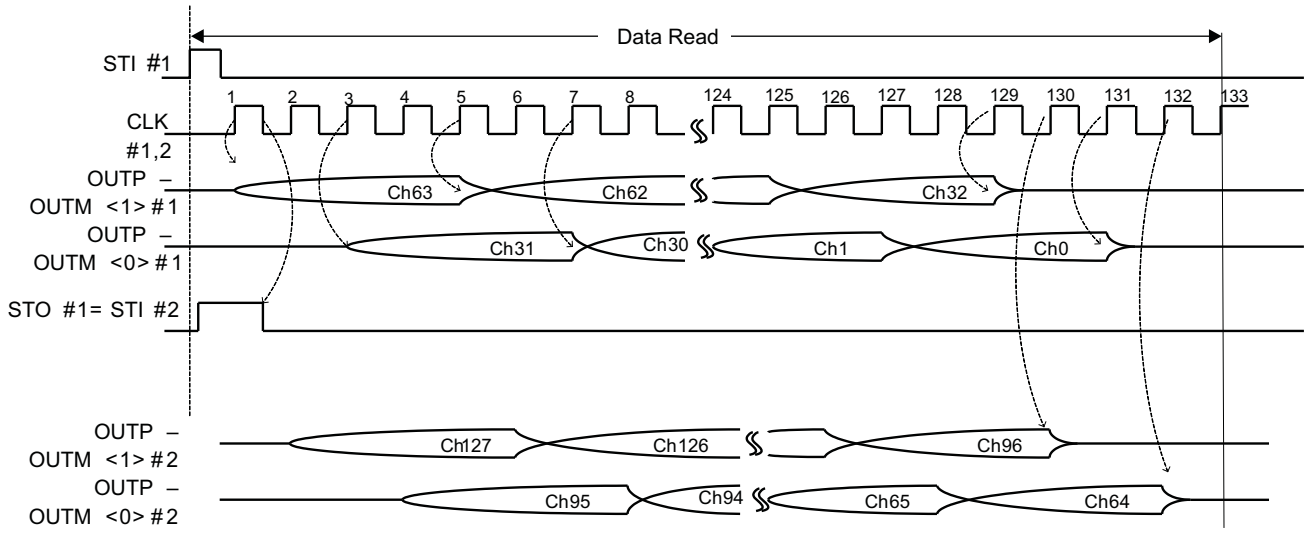


Figure 8. Data Read with Two Devices in Cascade

This mode allows the use of a single, four channel, 15 MHz (or more) ADC for digitizing the data from 128 channels in single scan. In this mode the effective maximum data transfer rate is 15 MHz.

TFT Charge Injection Compensation: The AFE0064 allows compensation for the charge injected by the TFT during turn on and turn off. During turn on, typically a TFT injects a positive charge forcing the integrator output below zero. One way to handle this is to allow negative swing on the integrator. In that case the pixel charge is integrated from the –ve value resulting from TFT charge injection. For this scheme the device output dynamic range covers all voltage levels starting from fixed –ve voltage arising from maximum anticipated charge injection to maximum positive voltage from the integrator. This can result in loss of dynamic range in the case where TFT charge injection is less than the maximum anticipated charge injection.

To overcome this problem, the AFE0064 provides a special feature to compensate for positive or negative charge during TFT turn on and opposite polarity charge during TFT turn off. The user can adjust the compensation charge with the help of external voltage on the VTEST-A and VTEST-B pins.

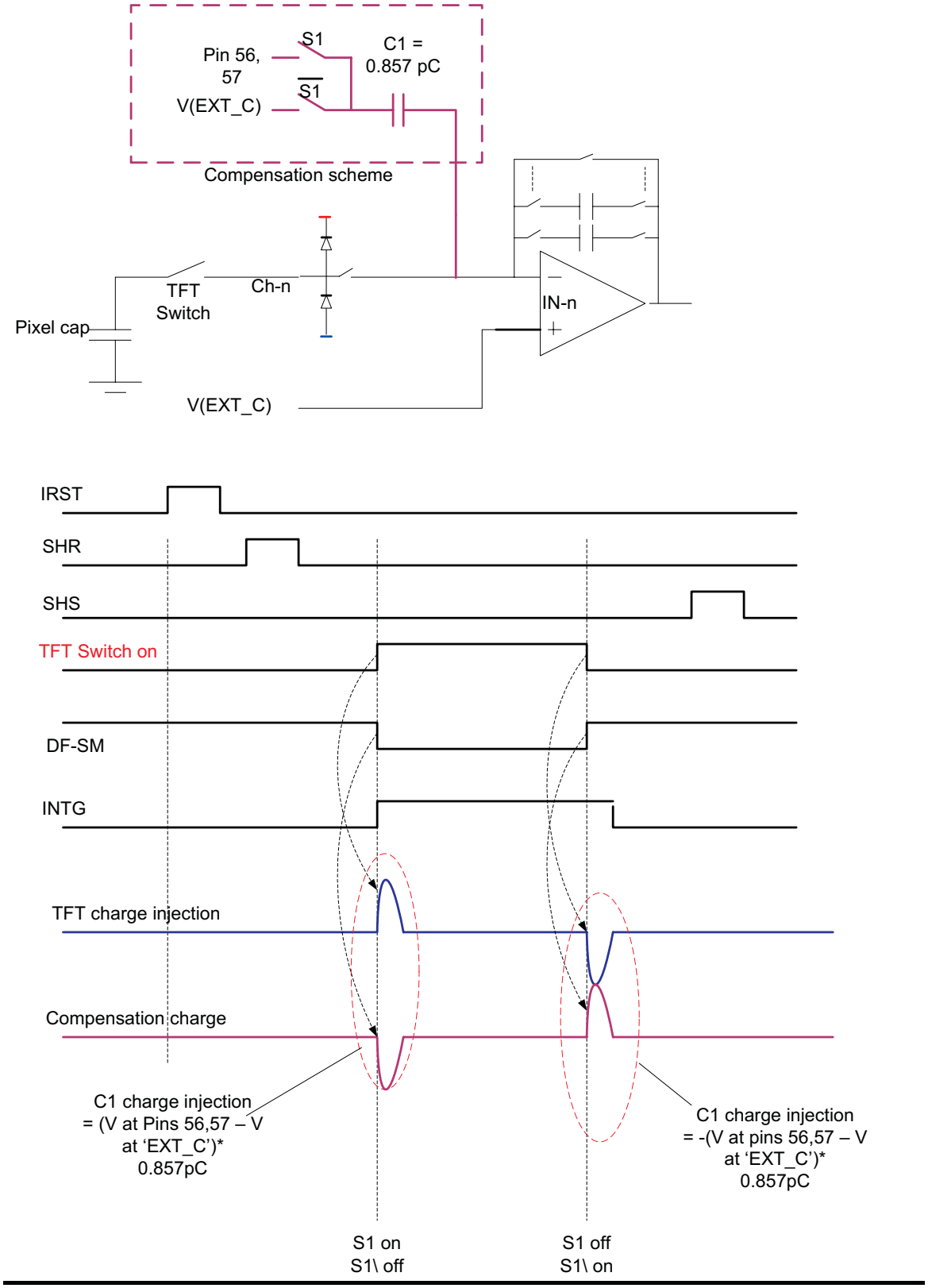


Figure 9. TFT Charge Injection Compensation Scheme

As shown in Figure 9, the TFT injects a charge during turn on and an opposite polarity charge during turn off. (For this example the injected charge during TFT turn on is positive.) This drives the integrator output –ve. Depending on the magnitude of the injected charge, the integrator may saturate or may be within linear range. The device starts integration from this –ve output voltage. At the end of integration the device sees an opposite polarity charge injection roughly of the same magnitude. This opposite polarity charge may or may not nullify the initial injected charge depending on whether the integrator was still within linear range or there was charge leakage due to integrator output saturation. The voltage at pins 56, 57 can be adjusted so that the compensation charge equals the TFT injected charge with opposite polarity. This nullifies the TFT injected charge both during turn on and turn off, to always keep the integrator in the linear region. So for the positive charge injection during TFT turn on, inject a –ve compensation charge. For this, the voltage at pins 56,57 needs to be set below the voltage at 'EXT_C'. The device injects the charge on the falling edge of the DF_SM signal. The compensation charge formulas are:

Compensation charge for TFT turn on = (V at pins 56,57 – V_'EXT_C') × 0.857 pC

Compensation charge for TFT turn off = –(V at pins 56,57 – V_'EXT_C') × 0.857 pC

Select voltage at pins 56,57 higher than the voltage at 'EXT_C' for compensating –ve charge during TFT turn on.

The device always injects an equal and opposite compensation charge at the rising edge of the DF_SM signal.

Allowing Limited Hole Counting (+ve charge) for Applications with Electron Counting (–ve charge) and Vice a Versa:

The charge compensation scheme can be used to offset the integrator output at the start of integration so as to allow a linear charge range in both directions. As discussed previously (refer to Figure 9), it is possible to inject a fixed +ve or –ve charge at the start of integration. The device can integrate up or down starting from this offset level. Note the integrator output is linear within the bounds of REFM and REFP. One can calculate the offset charge at integration start as Qcomp = (V at pins 56,57 – V_'EXT_C') × 0.857 pC.

The resulting integrator o/p offset voltage in the case of integration up or down is given by the following formula:

In the case of integration up:

Vint_off = REFM – (Qcomp × Int FB cap) — Refer to Table 1 for the Int FB cap for the selected range. Qcomp is negative for integration up, so that the integration output has a positive offset allowing headroom for hole counting.

In the case of integration down:

Vint_off = REFP – (Qcomp × Int FB cap) — Refer to Table 1 for the Int FB cap for the selected range. Qcomp is positive for integration up, so that the integration output has a negative offset allowing headroom for electron counting.

As shown in Figure 10, DF_SM rising edge is pushed after SHS rising edge. This avoids opposite charge injection which can corrupt integrator output.

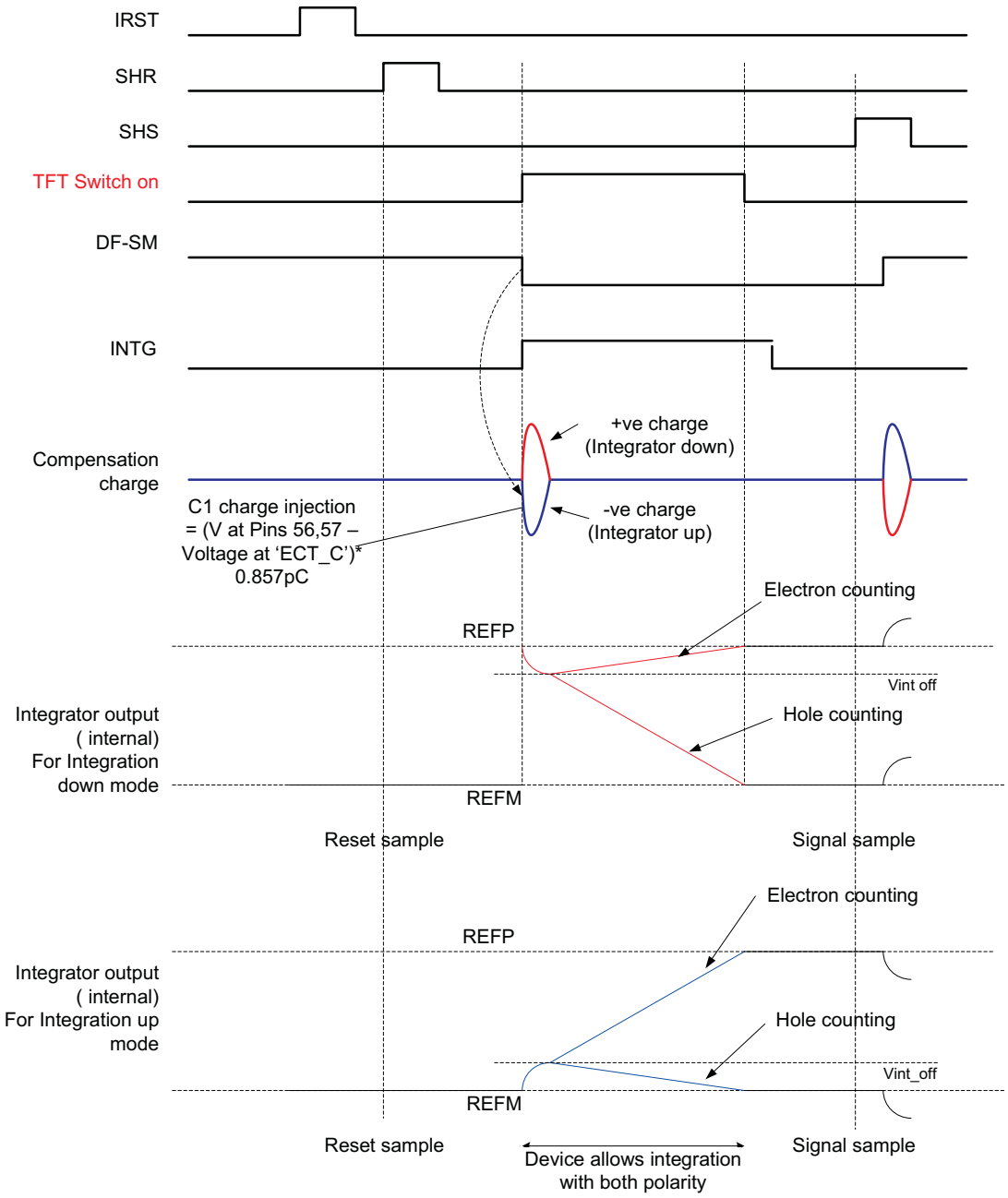


Figure 10. Handling Bipolar Charge Range Using Charge Injection Scheme

Note the relation between the integrator output and AFE0064 output (OUTP and OUTM) described in the Data Read section.

TYPICAL CHARACTERISTICS

HISTOGRAM OF OUTPUT OFFSET DRIFT WITH +VDD SUPPLY VARIATION

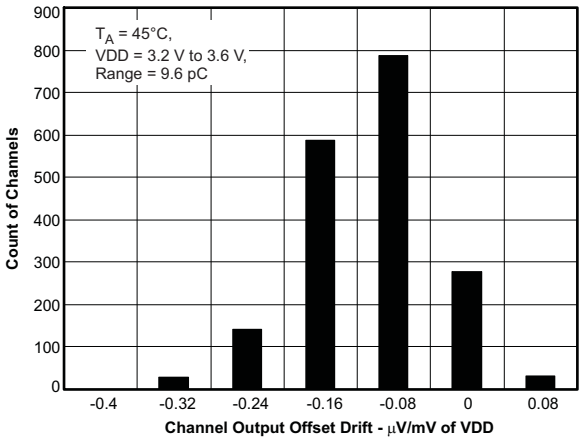


Figure 11.

HISTOGRAM OF OUTPUT OFFSET DRIFT WITH FREE-AIR TEMPERATURE

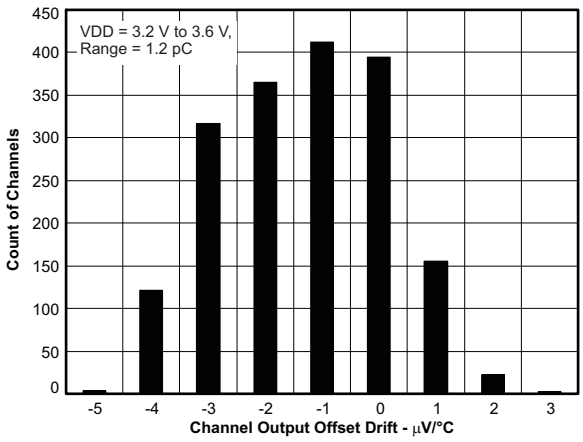


Figure 12.

HISTOGRAM OF GAIN ERROR VARIATION WITH +VDD

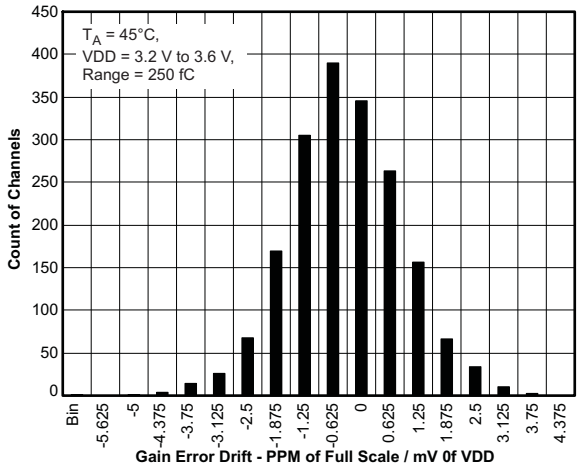


Figure 13.

HISTOGRAM OF GAIN ERROR DRIFT WITH FREE-AIR TEMPERATURE

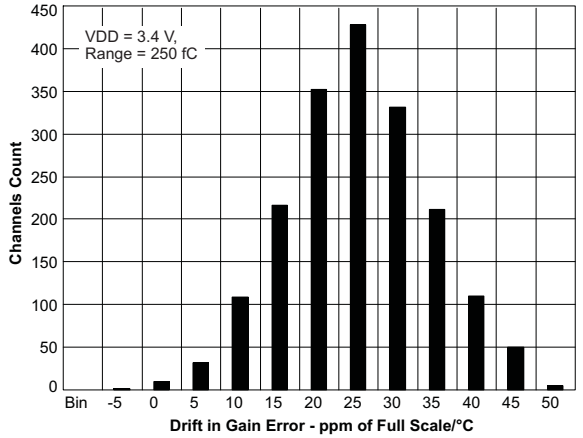


Figure 14.

TYPICAL CHARACTERISTICS (continued)

GAIN ERROR vs RANGE

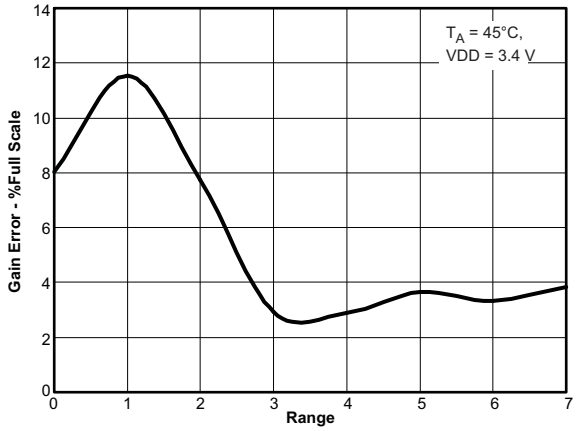


Figure 15.

CHANNEL TO CHANNEL CROSSTALK vs CHANNEL NUMBER

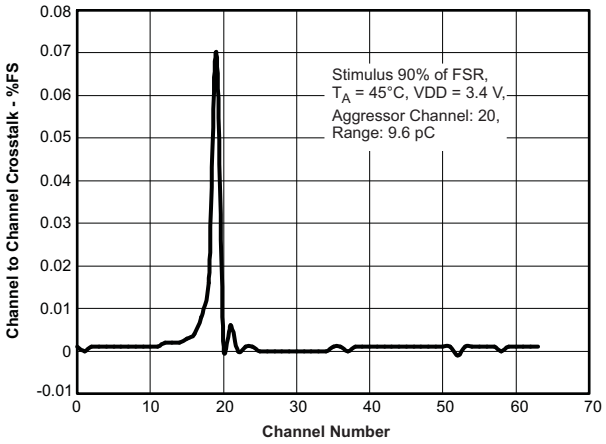


Figure 16.

SCAN TO SCAN CROSSTALK vs CHANNEL NUMBER

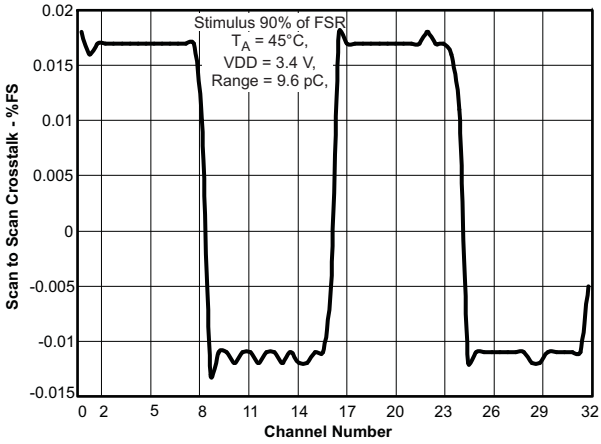


Figure 17.

COUNT OF CHANNELS vs LEAKAGE CURRENT DRIFT WITH +VDD

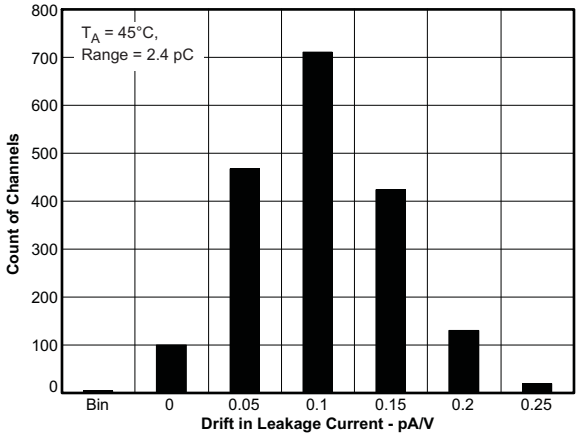


Figure 18.

TYPICAL CHARACTERISTICS (continued)

COUNT OF CHANNELS vs LEAKAGE CURRENT DRIFT WITH FREE-AIR TEMPERATURE

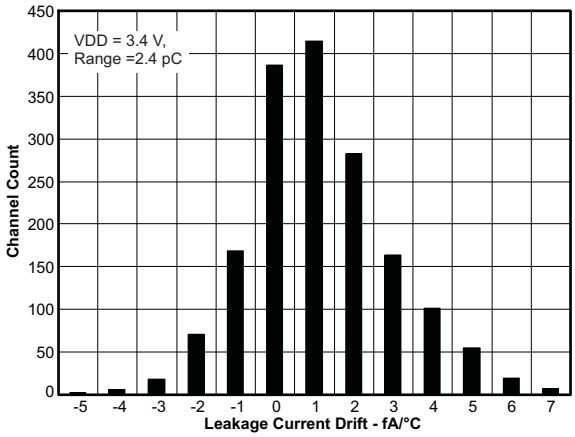


Figure 19.

NOISE vs CHANNEL NUMBER IN RANGE 0

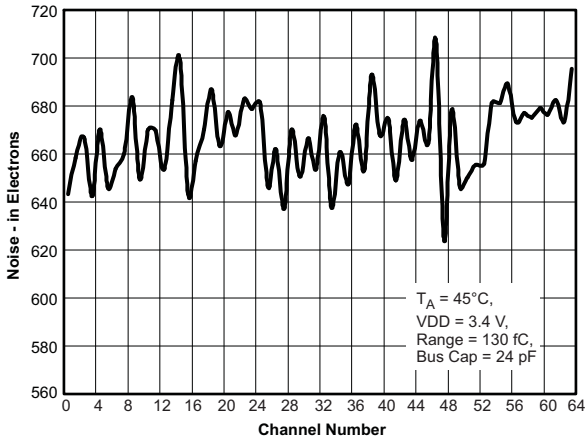


Figure 20.

NOISE vs CHANNEL NUMBER IN RANGE 1

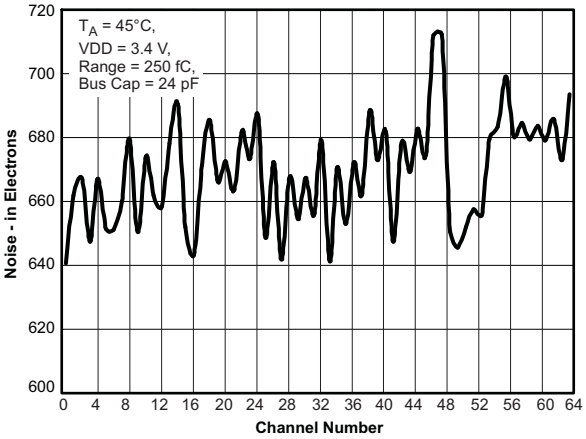


Figure 21.

NOISE vs CHANNEL NUMBER IN RANGE 2

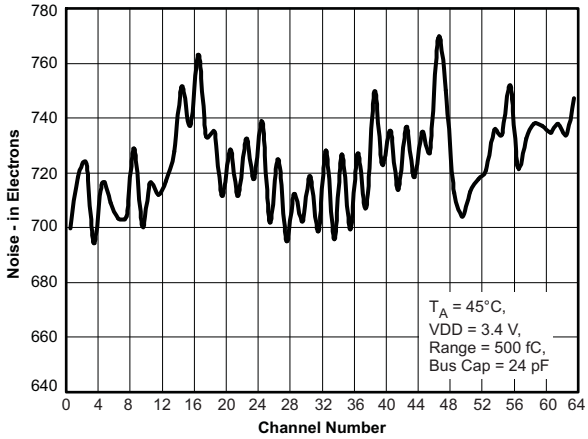


Figure 22.

TYPICAL CHARACTERISTICS (continued)

NOISE vs CHANNEL NUMBER IN RANGE 3

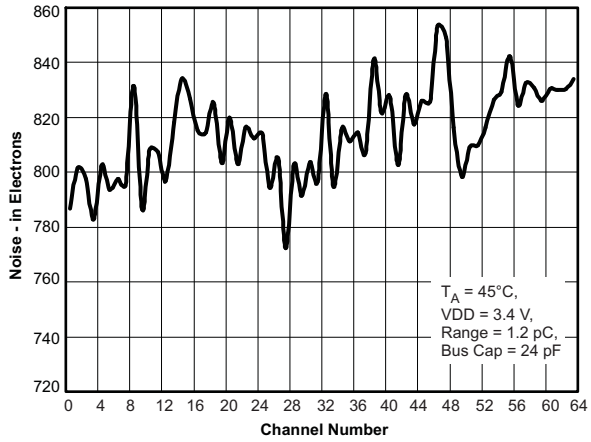


Figure 23.

NOISE vs CHANNEL NUMBER IN RANGE 4

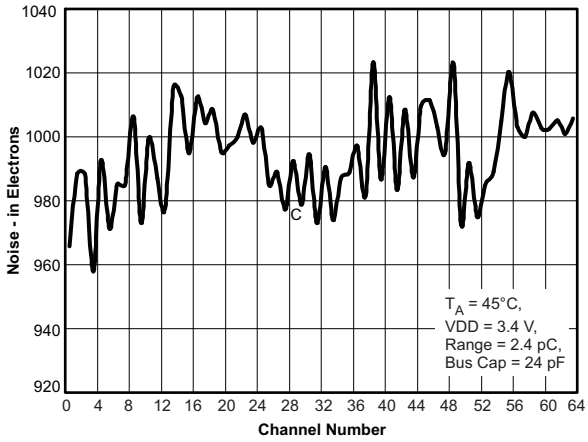


Figure 24.

NOISE vs CHANNEL NUMBER IN RANGE 5

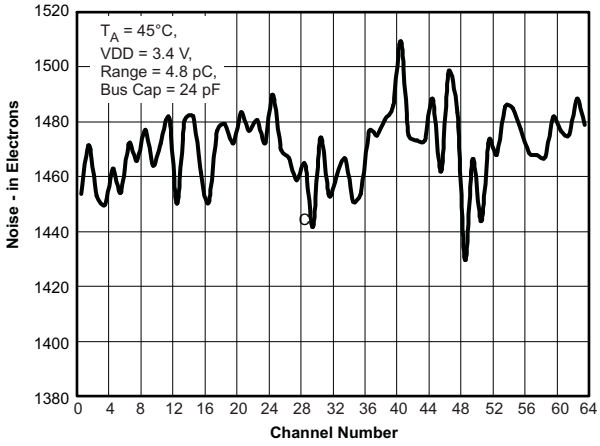


Figure 25.

NOISE vs CHANNEL NUMBER IN RANGE 6

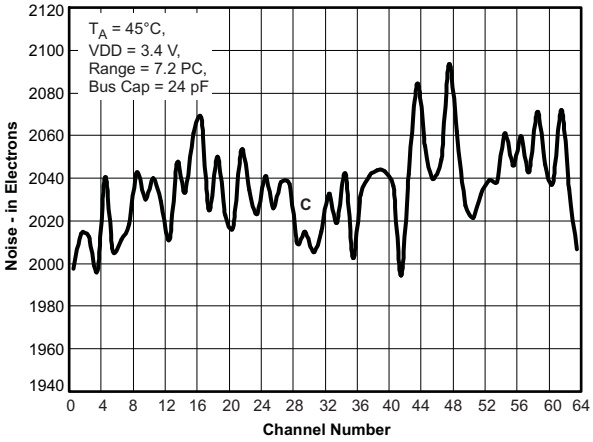


Figure 26.

TYPICAL CHARACTERISTICS (continued)

NOISE vs CHANNEL NUMBER IN RANGE 7

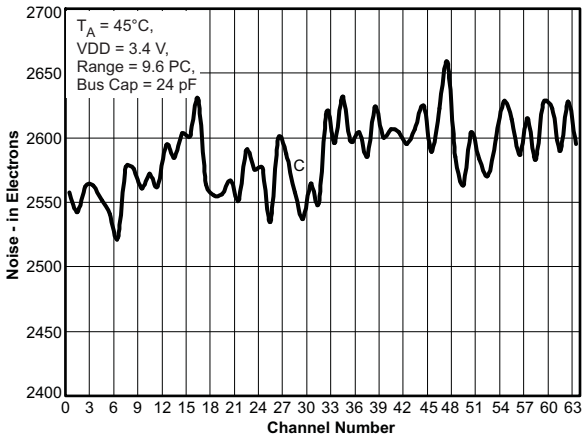


Figure 27.

NOISE vs INTEGRATION TIME

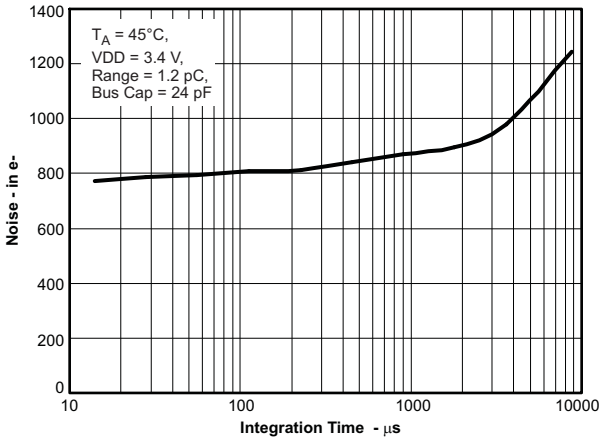


Figure 28.

NONLINEARITY ACROSS 30 DEVICES/64 CHANNELS

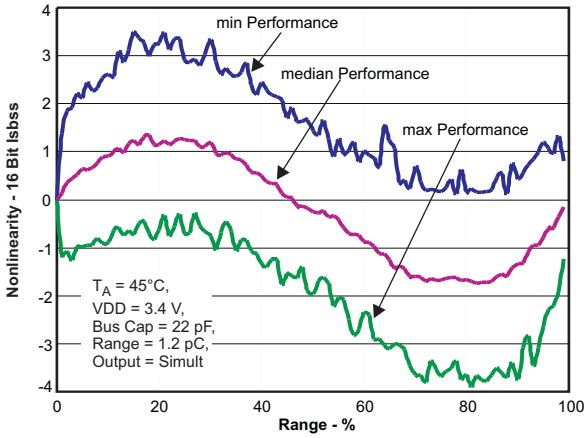


Figure 29.

NONLINEARITY ACROSS 30 DEVICES/64 CHANNELS

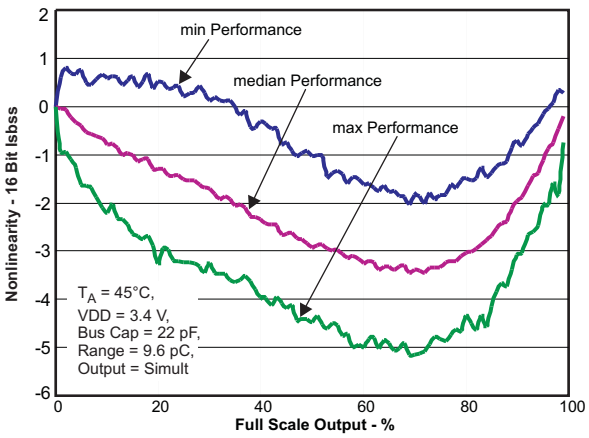


Figure 30.

+VDD CURRENT vs FREE-AIR TEMPERATURE

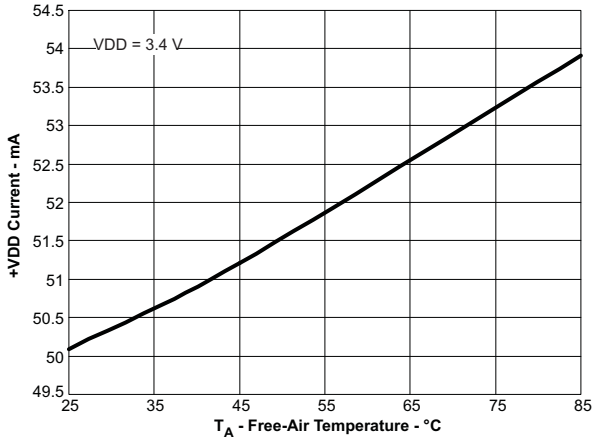


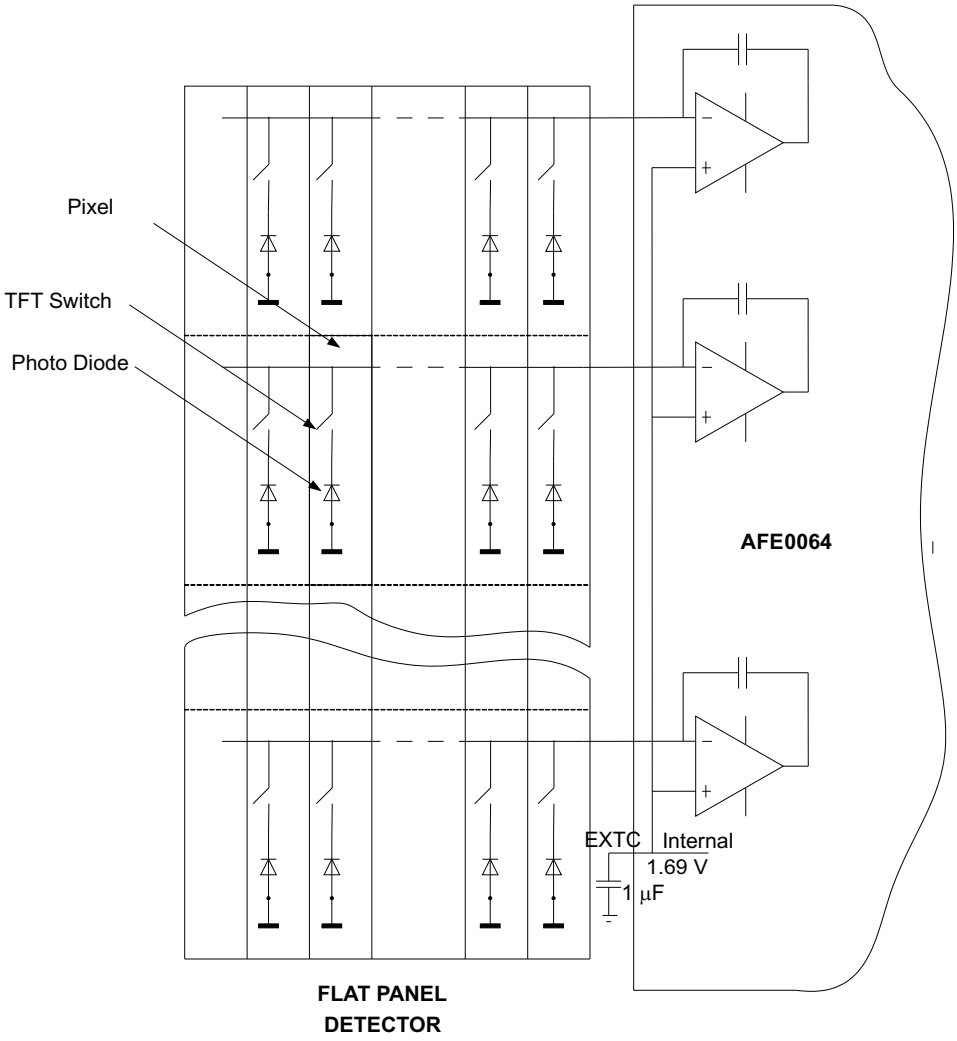
Figure 31.

APPLICATION INFORMATION

INTERFACING FLAT PANEL DETECTOR (FPD)

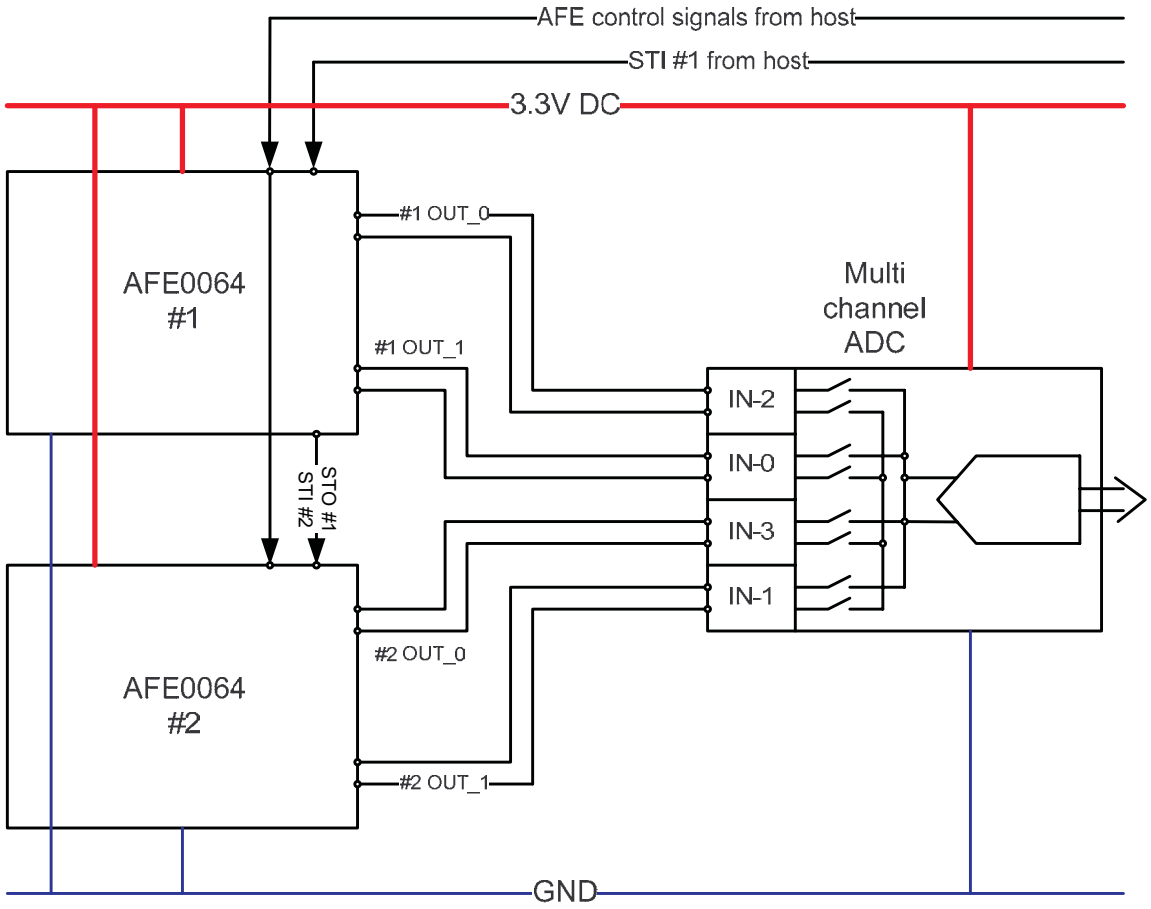
The following figure shows interfacing a flat panel detector to an AFE0064. The flat panel detector is a matrix of pixels. Each pixel consists of a photo diode and Thin Film Transistor switch. All of the pixels in a single row (or column depending on the convention used) are connected to a single bus. This bus interfaces with a single integrator. There is a separate integrator channel per row.

On X-Ray exposure (converted to light with scintillator) individual photo diodes acquire a charge proportional to incident light intensity. This charge is sampled in self capacitance of the photo diode. The columns are scanned one by one and the AFE0064 converts an individual photo diode charge into a proportional voltage.



ADC INTERFACE WITH AFE OUTPUT

Each AFE0064 has two differential output drivers as mentioned previously. AFE allows cascading of two devices which can work together like a single 128 channel device. Refer to Figure 8 for the timing diagram.



Contact TI sales for suitable ADC.

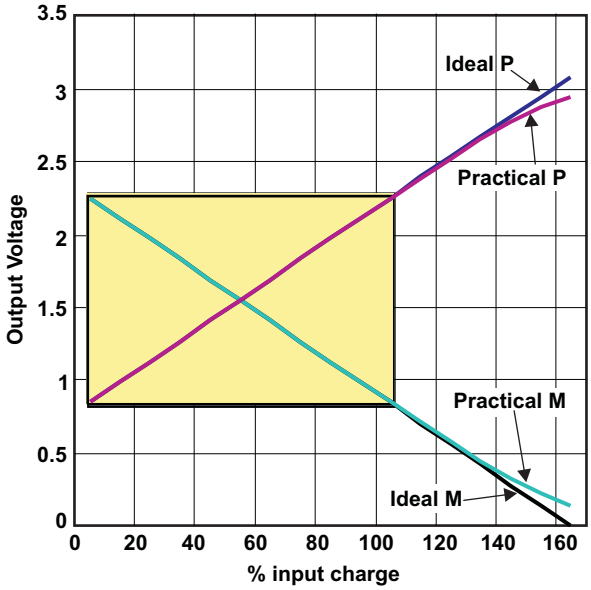
Figure 32. Typical Schematic Showing Four Channel ADC Interface with Two AFEs

RESETTING THE FPD PANEL

It is possible to reset the photo diodes using IRST. The integrator acts like a unity gain buffer during reset and the device can source or sink 50 µA through each of the 64 input pins while in the reset phase. For example, to reset a 10 pC charge it requires 10pC/50µA = 1/5 µSec.

Refer to Figure 3 for the reset timing details. The device is in the reset phase for 32/8 clocks after IRST rising edge in sequential/simultaneous mode respectively. The reset duration is controlled by selecting a clock speed or holding one of the 32/8 clocks for the required time in sequential/simultaneous mode respectively.

AFE TRANSFER CHARACTERISTICS



The plot above shows AFE transfer characteristics in integrator down mode. (For integrator up mode the P and M plots are interchanged.) AFE output is linear in the charge range bound by the rectangle shown.

The four corners of the rectangle in clockwise direction, starting with bottom left corner are as follows:
(0%, 0.85 V), (0%, 2.25 V), (100%, 2.25 V), (100%, 0.85 V) where REFP = 2.25 V and REFM = 0.85 V.

Beyond this range, the AFE output still responds to input charge however linearity is not specified. Linearity deteriorates as the output reaches close to the rails.

One can detect overrange once the output is beyond the linear rectangle and select a higher AFE range. It is also recommended to clamp the ADC input once it crosses 100% FS.

AFE REFERENCE DRIVING

Figure 33 shows generation of the 0.85 V and 2.25 V references for an AFE. Note that the device uses internal buffers on the reference inputs. As a result, it is possible to share a reference to multiple AFEs in a system. However, it is recommended to use a separate 100-Ω, 1-µF LPF for each individual AFE. Use 1% tolerance resistors for dividing 2.5 V to 2.25 V and 0.85 V.

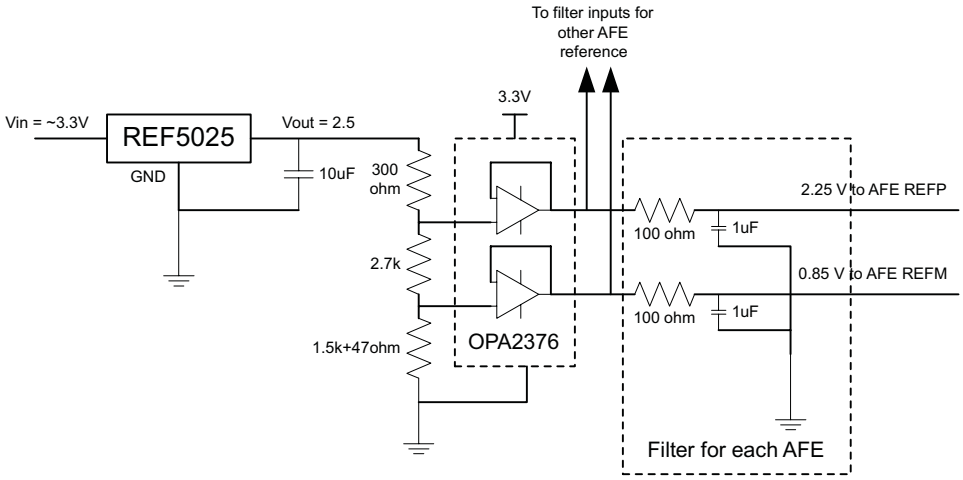


Figure 33. Typical Reference Generation and Driving Circuit for the AFE0064

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE0064IPBK	Active	Production	LQFP (PBK) | 128	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AFE0064
AFE0064IPBK.A	Active	Production	LQFP (PBK) | 128	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AFE0064
AFE0064IPBK.B	Active	Production	LQFP (PBK) | 128	90 | JEDEC TRAY (5+1)	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AFE0064
AFE0064IPBKR	Active	Production	LQFP (PBK) | 128	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AFE0064
AFE0064IPBKR.A	Active	Production	LQFP (PBK) | 128	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AFE0064

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

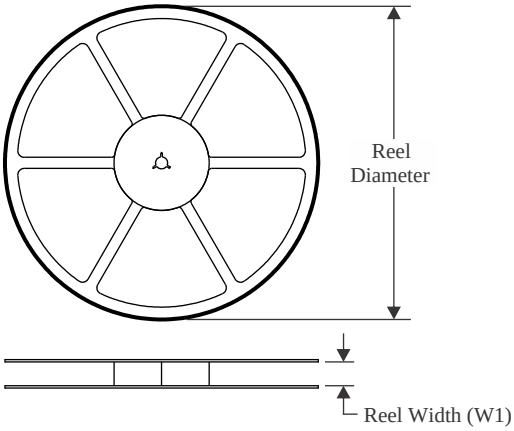
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

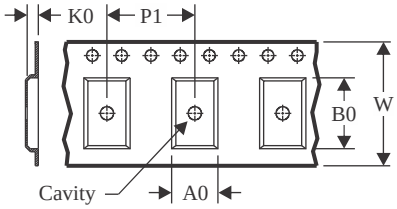
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

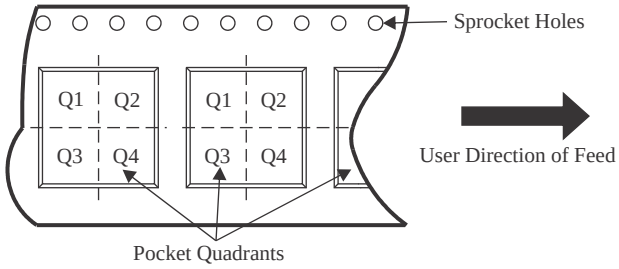


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

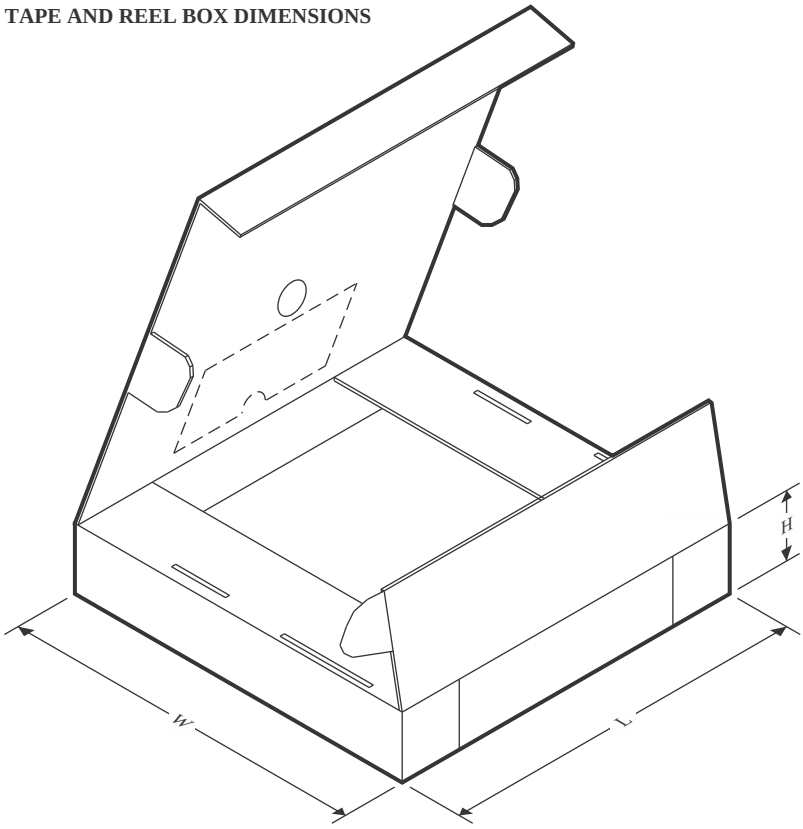
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE0064IPBKR	LQFP	PBK	128	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q1

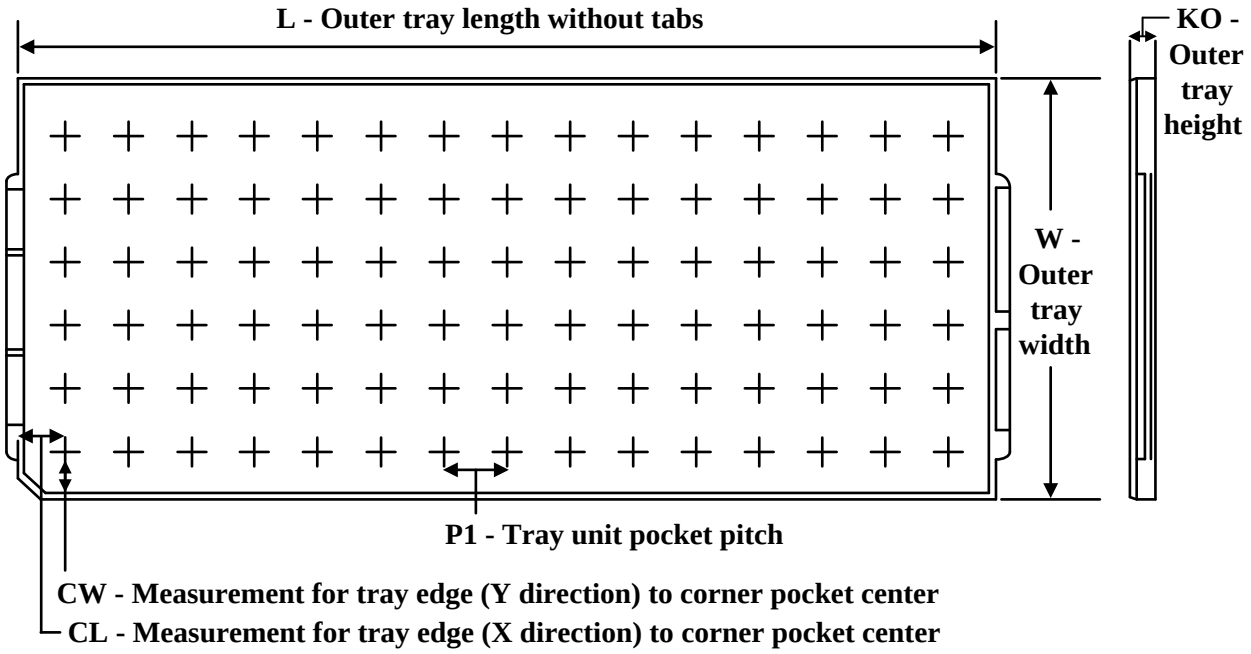
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE0064IPBKR	LQFP	PBK	128	1000	350.0	350.0	43.0

TRAY

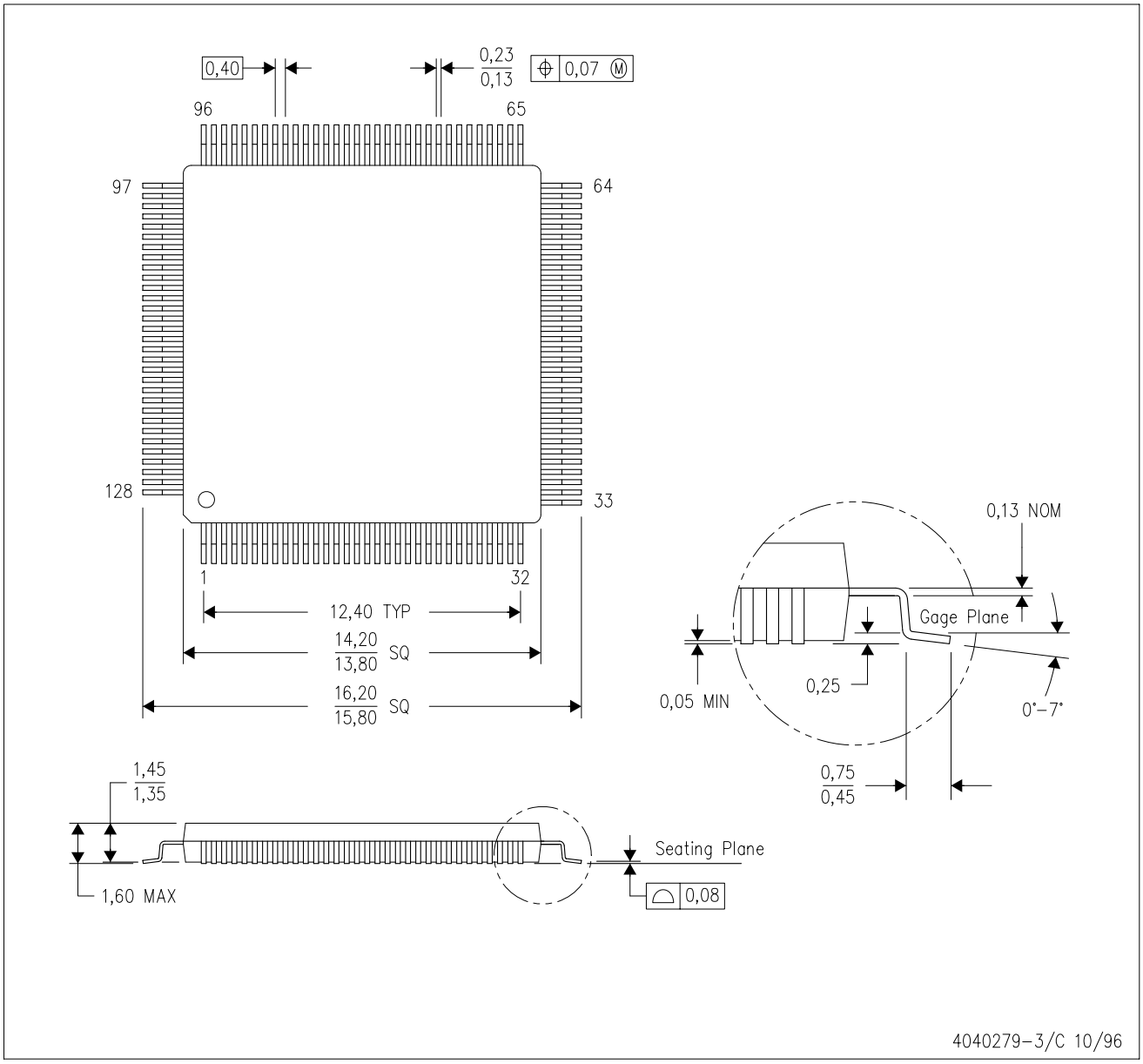


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

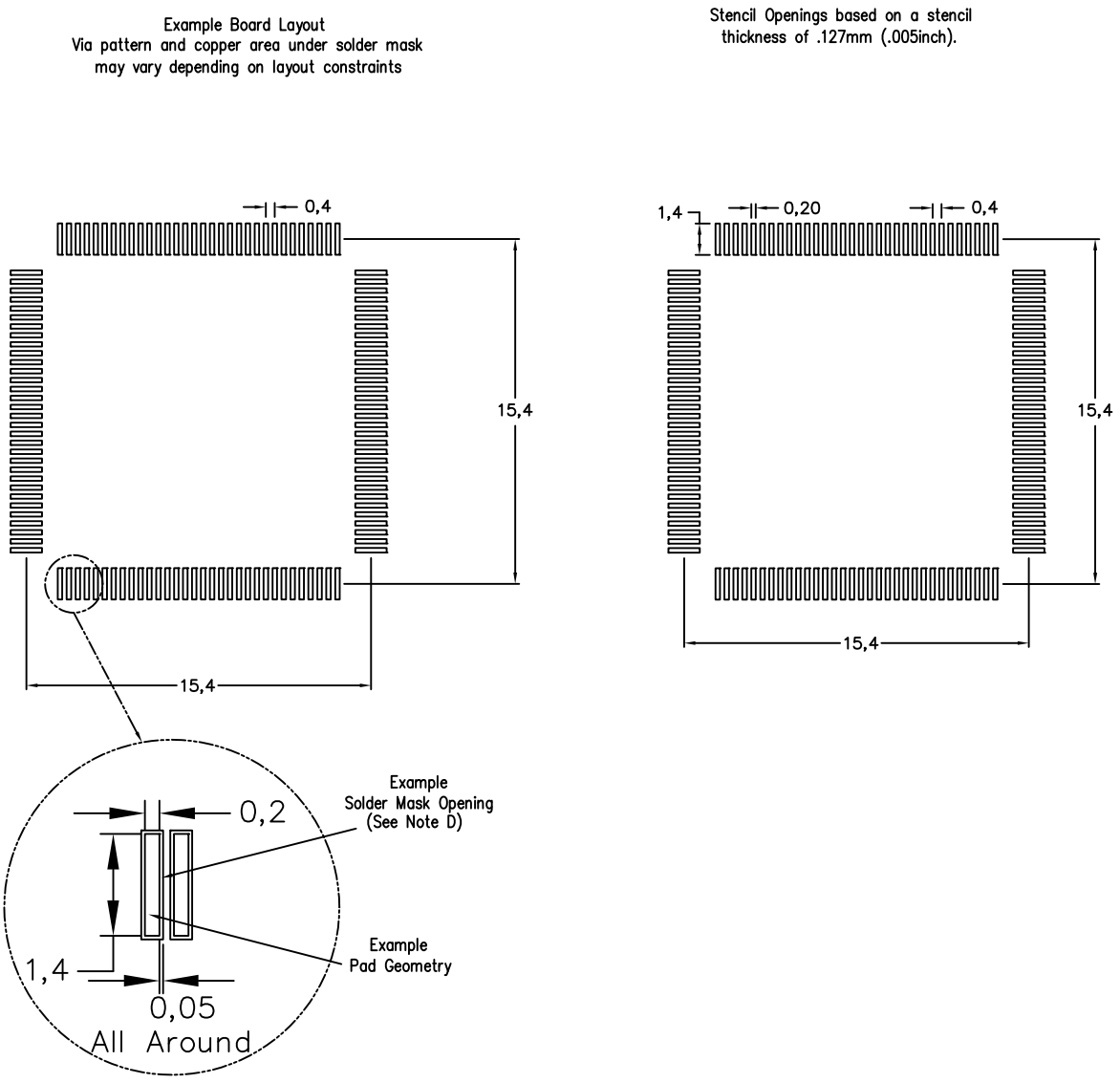
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE0064IPBK	PBK	LQFP	128	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
AFE0064IPBK.A	PBK	LQFP	128	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
AFE0064IPBK.B	PBK	LQFP	128	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45

PBK (S–PQFP–G128) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–026

PBK (S–PQFP–G128) PLASTIC QUAD FLAT PACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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