ADS9813 18-Bit, 2MSPS, 8-Channel, Simultaneous-Sampling ADC With Integrated Analog Front-End

1 Features

- 8-channel, 18-bit ADC with analog front-end:
  - Simultaneous sampling
  - Constant 1MΩ input impedance front-end
- Programmable analog input ranges:
  - ±12V, ±10V, ±7V, ±5V, ±3.5V, and ±2.5V
  - Single-ended and differential inputs
  - Common-mode voltage range: ±12V
  - Input overvoltage protection: Up to ±18V
- User-selectable analog input bandwidth:
  - 22.7kHz and 700kHz
- Integrated low-drift precision references:
  - ADC reference: 4.096V
  - 2.5V reference output for external circuits
- Excellent AC and DC performance at full-throughput:
  - DNL: ±0.35LSB, INL: ±0.8LSB
  - SNR: 90.3dBFS, THD: –113dB
- Power supply:
  - Analog and digital: 5V and 1.8V
  - Digital interface: 1.2V to 1.8V
- Temperature range: –40°C to +125°C

2 Applications

- Semiconductor test
- Programmable DC power supplies
- Parametric measurement units (PMU)

3 Description

The ADS9813 is an eight-channel data acquisition (DAQ) system based on a simultaneous sampling, 18-bit successive approximation register (SAR) analog-to-digital converter (ADC). The ADS9813 features a complete analog front-end (AFE) for each channel with an input clamp. The device also features a 1MΩ input impedance and a programmable gain amplifier (PGA) with user-selectable bandwidth options. The high input impedance allows direct connection with sensors and transformers, thus eliminating the need for external driver circuits. Configure the ADS9813 to accept ±12V, ±10V, ±7V, ±5V, ±3.5V, and ±2.5V bipolar inputs with up to ±12V input common-mode voltage.

A digital interface supporting 1.2V to 1.8V operation enables the ADS9813 to be used without external voltage level translators.

Package Information

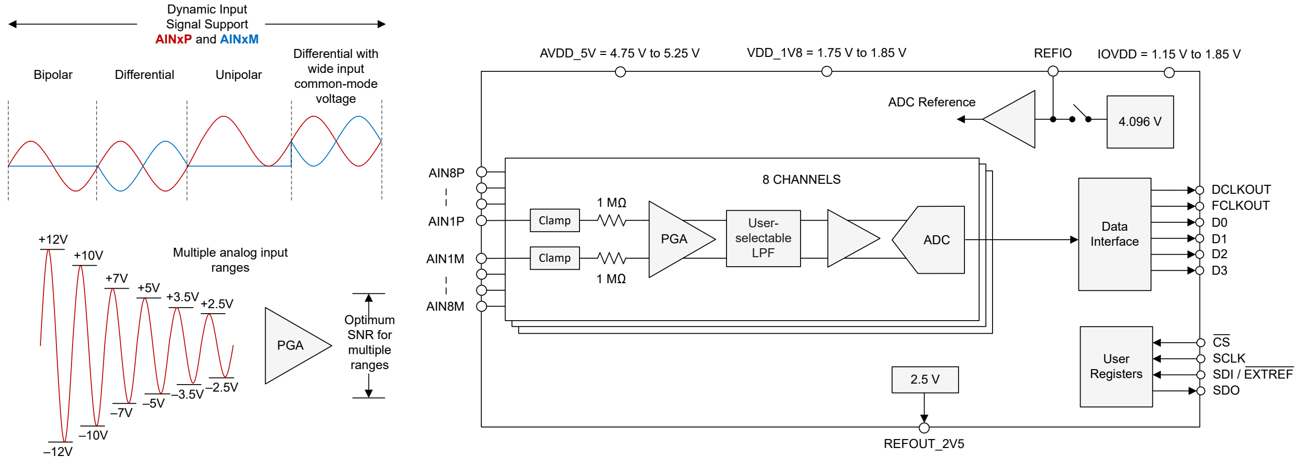
PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
ADS9813, ADS9811, ADS9810	RSH (VQFN, 56)	7mm × 7mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	SPEED	TOTAL POWER
ADS9813	2MSPS/channel	244mW
ADS9811, ADS9810	1MSPS/channel	177mW



Device Block Diagram

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4 Pin Configuration and Functions

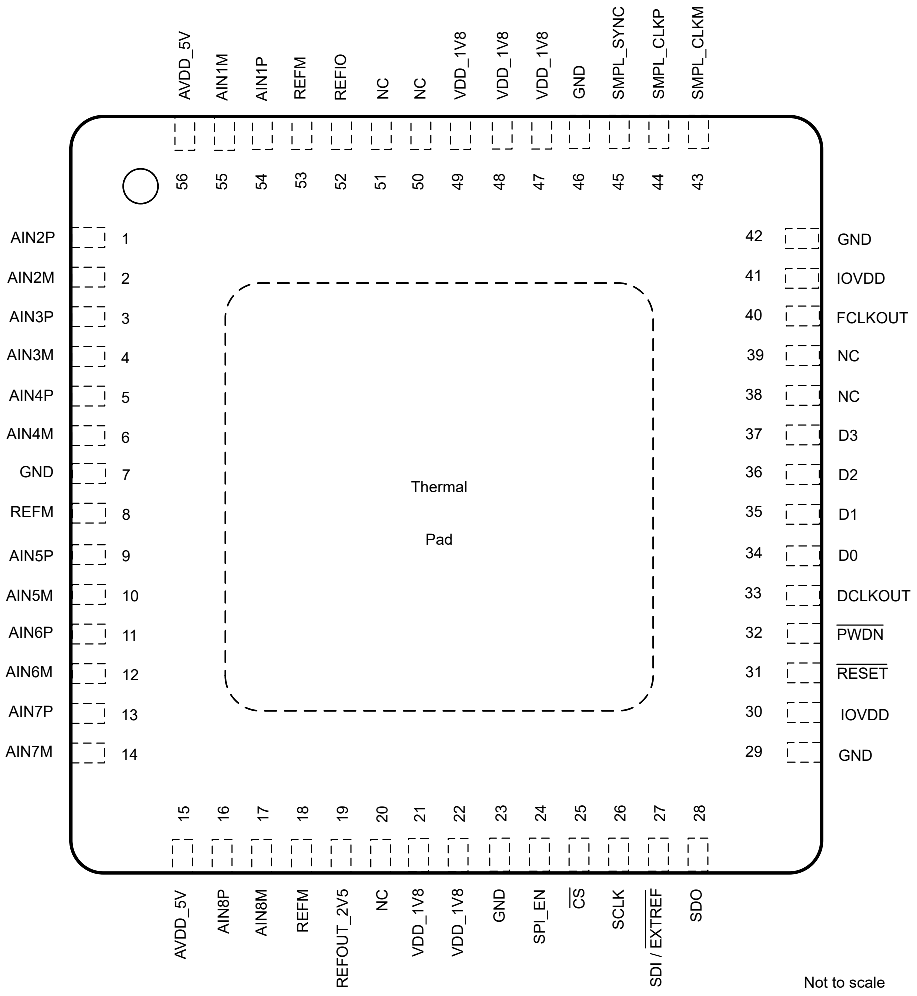


Figure 4-1. RSH Package, 56-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AIN1M	55	AI	Analog input channel 1, negative input.
AIN1P	54	AI	Analog input channel 1, positive input.
AIN2M	2	AI	Analog input channel 2, negative input.
AIN2P	1	AI	Analog input channel 2, positive input.
AIN3M	4	AI	Analog input channel 3, negative input.
AIN3P	3	AI	Analog input channel 3, positive input.
AIN4M	6	AI	Analog input channel 4, negative input.
AIN4P	5	AI	Analog input channel 4, positive input.
AIN5M	10	AI	Analog input channel 5, negative input.
AIN5P	9	AI	Analog input channel 5, positive input.
AIN6M	12	AI	Analog input channel 6, negative input.
AIN6P	11	AI	Analog input channel 6, positive input.
AIN7M	14	AI	Analog input channel 7, negative input.
AIN7P	13	AI	Analog input channel 7, positive input.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AIN8M	17	AI	Analog input channel 8, negative input.
AIN8P	16	AI	Analog input channel 8, positive input.
AVDD_5V	15, 56	P	5V analog supply. Connect 1µF and 0.1µF decoupling capacitors to GND.
$\overline{\text{CS}}$	25	DI	Chip-select input for the SPI interface configuration; active low. This pin has an internal 100kΩ pullup resistor to IOVDD.
D0	34	DO	Serial output data lane 0.
D1	35	DO	Serial data output lane 1.
D2	36	DO	Serial data output lane 2.
D3	37	DO	Serial data output lane 3.
DCLKOUT	33	DO	Clock output for the data interface.
FCLKOUT	40	DO	Frame synchronization output for the data interface.
GND	7, 23, 29, 42, 46	P	Ground.
IOVDD	30, 41	P	Digital I/O supply for the data interface. Connect 1µF and 0.1µF decoupling capacitors to GND.
NC	20, 38, 39, 50, 51	—	Not connected. No external connection.
$\overline{\text{PWDN}}$	32	DI	Power-down control; active low. $\overline{\text{PWDN}}$ has an internal 100kΩ pullup resistor to the digital interface supply.
REFIO	52	AI/AO	REFIO acts as an internal reference output when the internal reference is enabled. REFIO functions as an input pin for the external reference when the internal reference is disabled. Connect a 10µF decoupling capacitor to the REFM pins.
REFM	8, 18, 53	AI	Reference ground potential. Connect to GND.
REFOUT_2V5	19	AO	2.5V reference output. Connect a decoupling 10µF capacitor to the REFM pins.
$\overline{\text{RESET}}$	31	DI	Reset input for the device; active low. $\overline{\text{RESET}}$ has an internal 100kΩ pullup resistor to the digital interface supply.
SCLK	26	DI	Serial clock input for the configuration interface. $\overline{\text{SCLK}}$ has an internal 100kΩ pulldown resistor to the digital interface ground.
SDI/$\overline{\text{EXTREF}}$	27	DI	SDI is a multifunction logic input. Pin function is determined by the SPI_EN pin. SDI has an internal 100kΩ pulldown resistor to GND. SPI_EN = 0b: SDI is the logic input to select between the internal or external reference. Connect SDI to GND for the external reference. Connect SDI to IOVDD for the internal reference. SPI_EN = 1b: Serial data input for the configuration interface.
SDO	28	DO	Serial data output for the configuration interface.
SMPL_CLKM	43	DI	Connect SMPL_CLKM to GND for a single-ended ADC sampling clock input. SMPL_CLKM is the negative input for the differential sampling clock input to the ADC.
SMPL_CLKP	44	DI	Single-ended ADC sampling clock input. SMPL_CLKP is the positive input for the differential sampling clock input to the ADC.
SMPL_SYNC	45	DI	Synchronization input. See the *Synchronizing Multiple ADCs* section on how to use the SMPL_SYNC pin.
SPI_EN	24	DI	Logic input to enable the SPI interface configuration ($\overline{\text{CS}}$, SCLK, SDI, and SDO). SPI_EN has an internal 100kΩ pullup resistor to the digital interface supply.
VDD_1V8	21, 22, 47, 48, 49	P	1.8V power-supply. Connect 1µF and 0.1µF decoupling capacitors to GND.
Thermal pad	—	P	Exposed thermal pad; connect to GND.

(1) I = input, O = output, I/O = input or output, G = ground, and P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
AVDD_5V to GND	–0.3	6	V
VDD_1V8 to GND	–0.3	2.1	V
IOVDD to GND	–0.3	2.1	V
AINxP and AINxM to GND	–18	18	V
REFIO to REFM	REFM – 0.3	AVDD_5V + 0.3	V
REFM to GND	GND – 0.3	GND + 0.3	V
Digital inputs to GND	GND – 0.3	2.1	V
Input current to any pin except supply pins[2]	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Limit pin current to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification ANSI/ESDA/JEDEC JS-002, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD_5V	Analog power supply	AVDD_5V to GND	4.75	5	5.25	V
VDD_1V8	Power supply	VDD_1V8 to GND	1.75	1.8	1.85	V
IOVDD	Digital interface power supply	IOVDD to GND	1.15	1.8	1.85	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage to the ADC	External reference	4.088	4.096	4.104	V
ANALOG INPUTS						
V_{FSR}	Full-scale input range	RANGE_CHx = 2	–2.5		2.5	V
		RANGE_CHx = 1	–3.5		3.5	
		RANGE_CHx = 0	–5		5	
		RANGE_CHx = 3	–7		7	
		RANGE_CHx = 4	–10		10	
		RANGE_CHx = 5	–12		12	
AINxP	Operating input voltage, positive input	AINxP to GND	–17		17	V
AINxM	Operating input voltage, negative input	AINxM to GND	–17		17	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		ADS981x	UNIT
		RSH (VQFN)	
		56 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at AVDD_5V = 4.75V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.15V to 1.85V, V_{REF} = 4.096V (external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
R_{IN}	Input impedance	All input ranges	0.8	1	1.2	MΩ
	Input impedance thermal drift	All input ranges		10	30	ppm/°C
	Input capacitance			10		pF
ANALOG INPUT FILTER						
$BW_{(-3\ dB)}$	Analog input LPF bandwidth –3 dB	Low-bandwidth filter, all input ranges		22.7		kHz
		Wide-bandwidth filter, input range = ±2.5V		221		
		Wide-bandwidth filter, input range = ±3.5V		325		
		Wide-bandwidth filter, input range = ±5V		500		
		Wide-bandwidth filter, input range = ±7V		700		
		Wide-bandwidth filter, input range = ±10V		691		
		Wide-bandwidth filter, input range = ±12V		664		
DC PERFORMANCE(3) (4)						
	Resolution	No missing codes	18			Bits
DNL	Differential nonlinearity	Wide CM enabled and disabled, all ranges	–0.99	±0.35	0.99	LSB
INL	Integral nonlinearity	RANGE = ±5V and ±10V, T_A = 20°C to 60°C, AVDD_5V = 4.9V to 5.1V ADS9813 and ADS9811	–2	±0.8	2	LSB
		All ranges	–4	±0.8	4	
	Offset error	RANGE = ±5V, ±10V, and ±12V	–75	±15	75	LSB
		RANGE = ±3.5V and ±7V	–100	±25	100	
		RANGE = ±2.5V	–175	±25	175	
		All other conditions		±50		
	Offset error thermal drift	All ranges, T_A = 0°C to 70°C		0.6	2	ppm/°C
		All ranges		0.6		
	Gain error	All ranges	–0.038	±0.008	0.038	%FSR
	Gain error thermal drift	All ranges, T_A = 0°C to 70°C		0.6	3	ppm/°C
		All ranges		0.6		

5.5 Electrical Characteristics (continued)

at AVDD_5V = 4.75V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.15V to 1.85V, V_{REF} = 4.096V (external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE(3) (4)						
SNR	Signal-to-noise ratio	Low-noise filter, f_{IN} = 2kHz, range = ±2.5V	85.3	87.4		dBFS
		Low-noise filter, f_{IN} = 2kHz, range = ±3.5V	86.3	88.4		
		Low-noise filter, f_{IN} = 2kHz, range = ±5V	87	89.1		
		Low-noise filter, f_{IN} = 2kHz, range = ±7V	87.5	89.8		
		Low-noise filter, f_{IN} = 2kHz, range = ±10V	88	90.2		
		Low-noise filter, f_{IN} = 2kHz, range = ±12V	88.1	90.3		
		Wide-bandwidth filter, f_{IN} = 2kHz, range = ±2.5V	77.1	79.1		
		Wide-bandwidth filter, f_{IN} = 2kHz, range = ±3.5V	77.4	79.4		
		Wide-bandwidth filter, f_{IN} = 2kHz, range = ±5V	77.5	79.7		
		Wide-bandwidth filter, f_{IN} = 2kHz, range = ±7V	77.7	79.9		
		Wide-bandwidth filter, f_{IN} = 2kHz, range = ±10V	79.5	81.6		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±12V	80.2	82.4		
SINAD	Signal-to-noise + distortion ratio	Low-noise filter, f_{IN} = 2kHz, range = ±2.5V	85.2	87.3		dB
		Low-noise filter, f_{IN} = 2kHz, range = ±3.5V	86.2	88.3		
		Low-noise filter, f_{IN} = 2kHz, range = ±5V	86.9	89		
		Low-noise filter, f_{IN} = 2kHz, range = ±7V	87.4	89.7		
		Low-noise filter, f_{IN} = 2kHz, range = ±10V	87.9	90.1		
		Low-noise filter, f_{IN} = 2kHz, range = ±12V	88	90.2		
		Wide-bandwidth filter, f_{IN} = 2kHz, range = ±2.5V	77	79		
		Wide-bandwidth filter, f_{IN} = 2kHz, range = ±3.5V	77.3	79.3		
		Wide-bandwidth filter, f_{IN} = 2kHz, range = ±5V	77.4	79.6		
		Wide-bandwidth filter, f_{IN} = 2kHz, range = ±7V	77.6	79.8		
		Wide-bandwidth filter, f_{IN} = 2kHz, range = ±10V	79.4	81.5		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±12V	80.1	82.3		
THD	Total harmonic distortion	Low-noise filter, f_{IN} = 2kHz, all ranges		–113		dB
		Wide-bandwidth filter, f_{IN} = 2kHz, all ranges		–113		
SFDR	Spurious-free dynamic range	f_{IN} = 2kHz		102		dB
		f_{IN} = 2kHz, *data averaging* enabled		113		
	CMRR	At dc		–70		dB
	Isolation crosstalk	At dc		–100		dB
INTERNAL REFERENCE						
V_{REF} (1)	Voltage on REFIO pin (configured as output)	1µF capacitor on REFIO pin, T_A = 25°C	4.092	4.096	4.1	V
	Reference temperature drift			7	20	ppm/°C

5.5 Electrical Characteristics (continued)

at AVDD_5V = 4.75V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.15V to 1.85V, V_{REF} = 4.096V (external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS						
V_{IL}	Input low logic level		–0.3		0.3 IOVDD	V
V_{IH}	Input high logic level		0.7 IOVDD		IOVDD	V
	Input capacitance			6		pF
LVDS SAMPLING CLOCK INPUT						
V_{TH}	High-level input voltage (P – M)	AC coupled	100			mV
		DC coupled	300			
V_{TL}	Low-level input voltage (P – M)	AC coupled			–100	mV
		DC coupled			–300	
V_{ICM}	Input common-mode voltage		0.5	1.2	1.4	V
DIGITAL OUTPUTS						
V_{OL}	Output low logic level	I_{OL} = 200µA sink	0		0.2 IOVDD	V
V_{OH}	Output high logic level	I_{OH} = 200µA source	0.8 IOVDD		IOVDD	V
POWER SUPPLY - ADS9813						
	Total power dissipation	Maximum throughput		244	304	mW
I_{AVDD_5V}	Supply current from AVDD_5V	Maximum throughput, internal reference		28.3	32	mA
		Power-down		0.2	2	
I_{VDD_1V8}	Supply current from VDD_1V8	Maximum throughput, internal reference		52	70	mA
		Power-down		0.2	8	
I_{IOVDD}	Supply current from IOVDD	Maximum throughput, C_L = 10pF		5	10	mA
		Power-down		0.1	2	
POWER SUPPLY - ADS9811 and ADS9810						
	Total power dissipation	Maximum throughput		177	215	mW
I_{AVDD_5V}	Supply current from AVDD_5V	Maximum throughput, internal reference		21.3	25	mA
	Supply current from AVDD_5V	Power-down		0.2	2	
I_{VDD_1V8}	Supply current from VDD_1V8	Maximum throughput, internal reference		35	43	mA
	Supply current from VDD_1V8	Power-down		0.2	8	
I_{IOVDD}	Supply current from IOVDD	Maximum throughput, C_L = 10pF		4	7	mA
	Supply current from IOVDD	Power-down		0.1	2	

(1) Does not include the variation in voltage resulting from solder shift effects.
(2) Measured with analog input common-mode voltage range ≤ ±RANGE/2 as described in *Wide Common-Mode Configuration for Differential Inputs*
(3) Minimum and maximum specifications are applicable for low-bandwidth filter setting.

5.6 Timing Requirements

at AVDD_5V = 4.75V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.15V to 1.85V, V_{REF} = 4.096V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

			MIN	MAX	UNIT
CONVERSION CYCLE					
f_{SMPL_CLK}	Sampling frequency	ADS9813	3.9	8.1	MHz
f_{SMPL_CLK}	Sampling frequency	ADS9811 and ADS9810	3.9	4.1	MHz
t_{SMPL_CLK}	Sampling time interval		1 / f_{SMPL_CLK}		ns
$t_{PL\_SMPL\_CLK}$	SMPL_CLK low time		0.45 t_{SMPL_CLK}	0.55 t_{SMPL_CLK}	ns
$t_{PH\_SMPL\_CLK}$	SMPL_CLK high time		0.45 t_{SMPL_CLK}	0.55 t_{SMPL_CLK}	ns
SPI INTERFACE TIMINGS (CONFIGURATION INTERFACE)					
f_{SCLK}	Maximum SCLK frequency			20	MHz
t_{PH_CK}	SCLK high time		0.48	0.52	t_{CLK}
t_{PL_CK}	SCLK low time		0.48	0.52	t_{CLK}
t_{hi_CS}	Pulse duration: $\overline{CS}$ high		220		ns
t_{d_CSCK}	Delay time: $\overline{CS}$ falling to the first SCLK capture edge		20		ns
t_{su_CKDI}	Setup time: SDI data valid to the SCLK rising edge		10		ns
t_{ht_CKDI}	Hold time: SCLK rising edge to data valid on SDI		5		ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising		5		ns
CMOS DATA INTERFACE					
t_{su_SS}	Setup time: SMPL_SYNC rising edge to SMPL_CLK falling edge		10		ns
t_{ht_SS}	Hold time: SMPL_CLK falling edge to SMPL_SYNC high		10		ns

5.7 Switching Characteristics

at AVDD_5V = 4.75V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.15V to 1.85V, V_{REF} = 4.096V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
RESET					
t_{PU}	Power-up time for device			30	ms
SPI INTERFACE TIMINGS (Configuration Interface)					
t_{den_CKDO}	Delay time: 8th SCLK rising edge to data enable			22	ns
t_{dz_CKDO}	Delay time: 24th SCLK rising edge to SDO going Hi-Z			50	ns
t_{d_CKDO}	Delay time: SCLK falling edge to corresponding data valid on SDO			16	ns
t_{ht_CKDO}	Delay time: SCLK falling edge to previous data valid on SDO		2		ns
CMOS DATA INTERFACE					
t_{DCLK}	Data clock output	DDR mode	10		ns
		SDR mode	20		
	Clock duty cycle		45	55	%
$t_{off\_DCLKDO\_r}$	Time offset: DCLK rising to corresponding data valid	DDR mode	t_{DCLK} / 4 – 1.5	t_{DCLK} / 4 + 1.5	ns
$t_{off\_DCLKDO\_f}$	Time offset: DCLK falling to corresponding data valid	DDR mode	t_{DCLK} / 4 – 1.5	t_{DCLK} / 4 + 1.5	ns
t_{d_DCLKDO}	Time delay: DCLK rising to corresponding data valid	SDR mode	–1	1	ns
$t_{d\_SYNC\_FCLK}$	Time delay: SMPL_CLK falling edge with SYNC signal to corresponding FCLKOUT rising edge		3	4	t_{SMPL_CLK}

5.8 Timing Diagrams

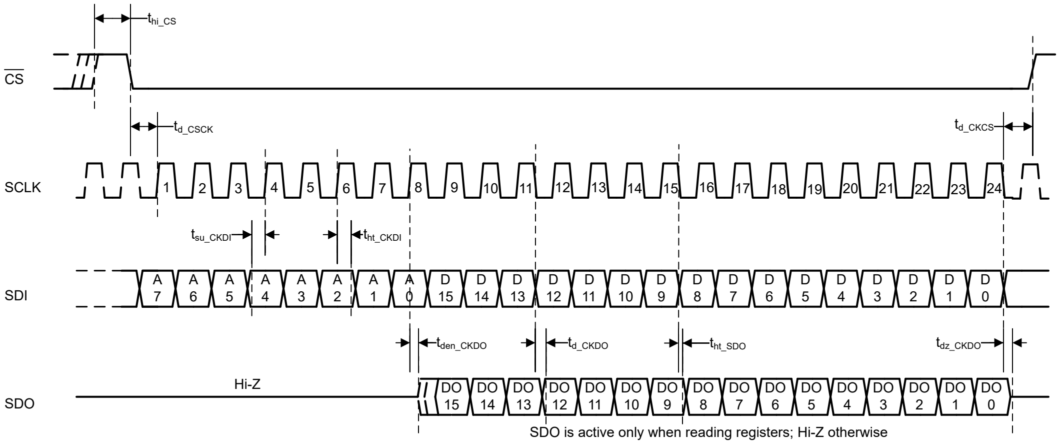


Figure 5-1. SPI Configuration Interface

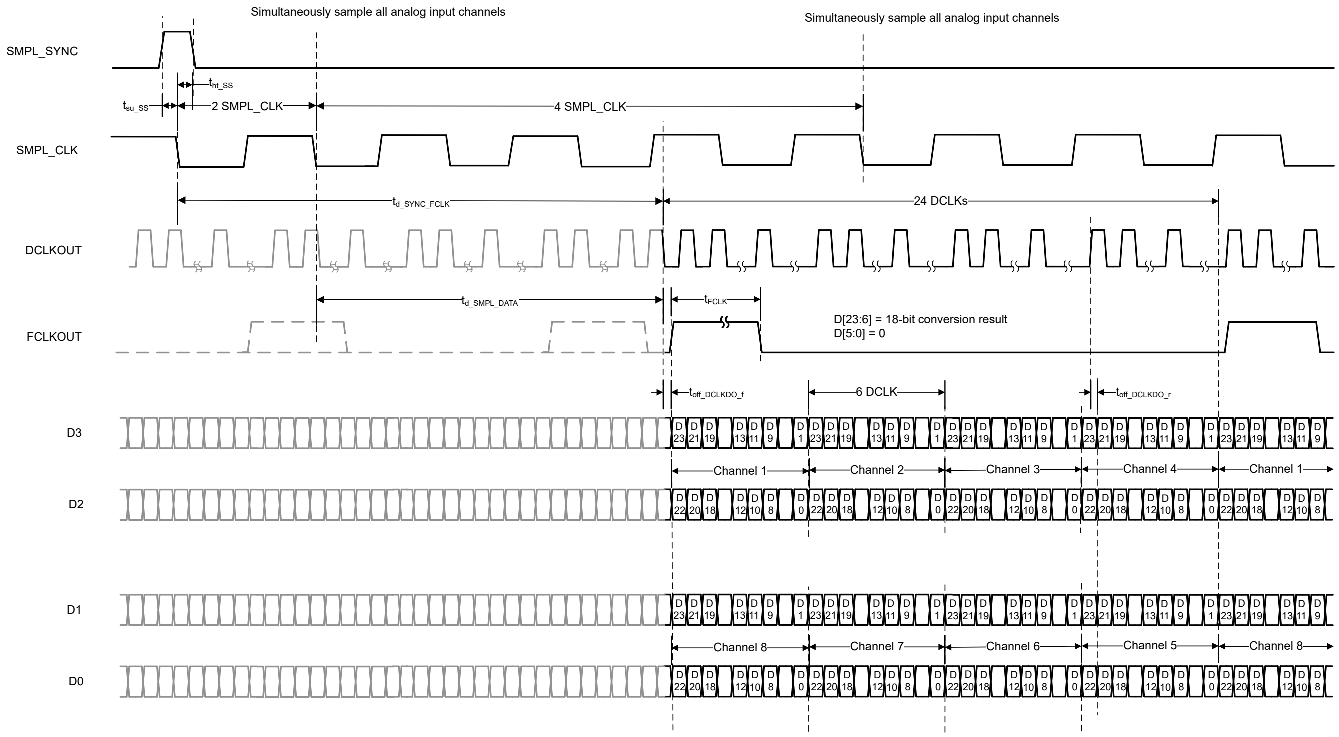


Figure 5-2. 4-SDO DDR CMOS Data Interface

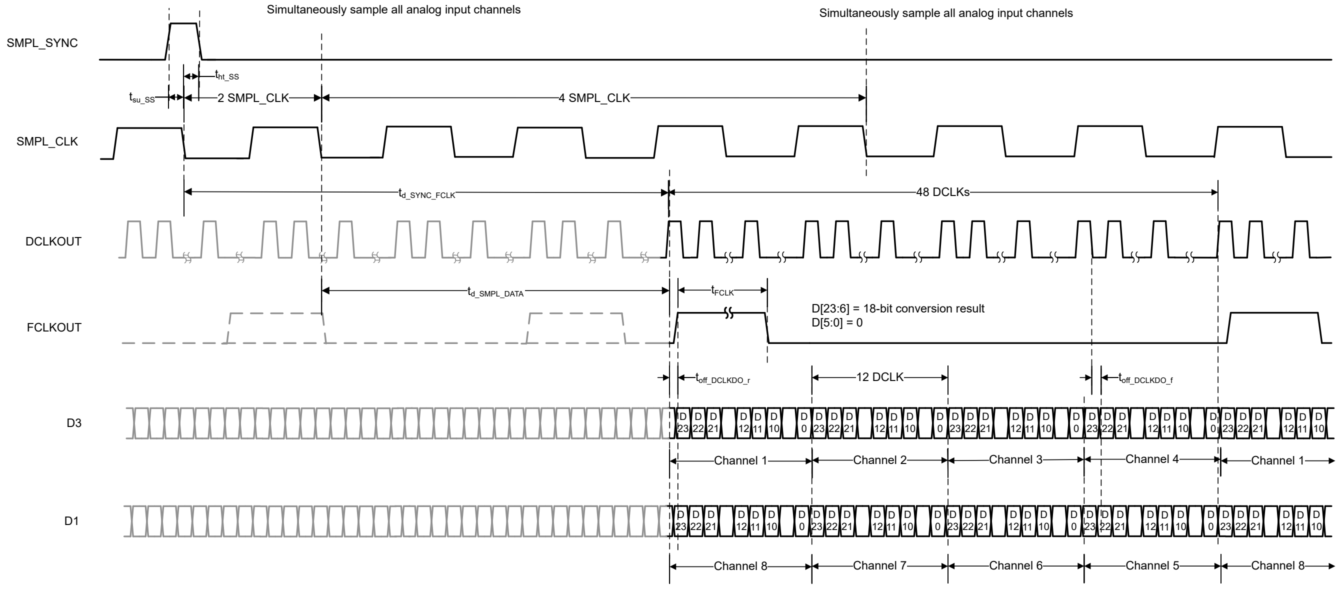


Figure 5-3. 2-SDO DDR CMOS Data Interface

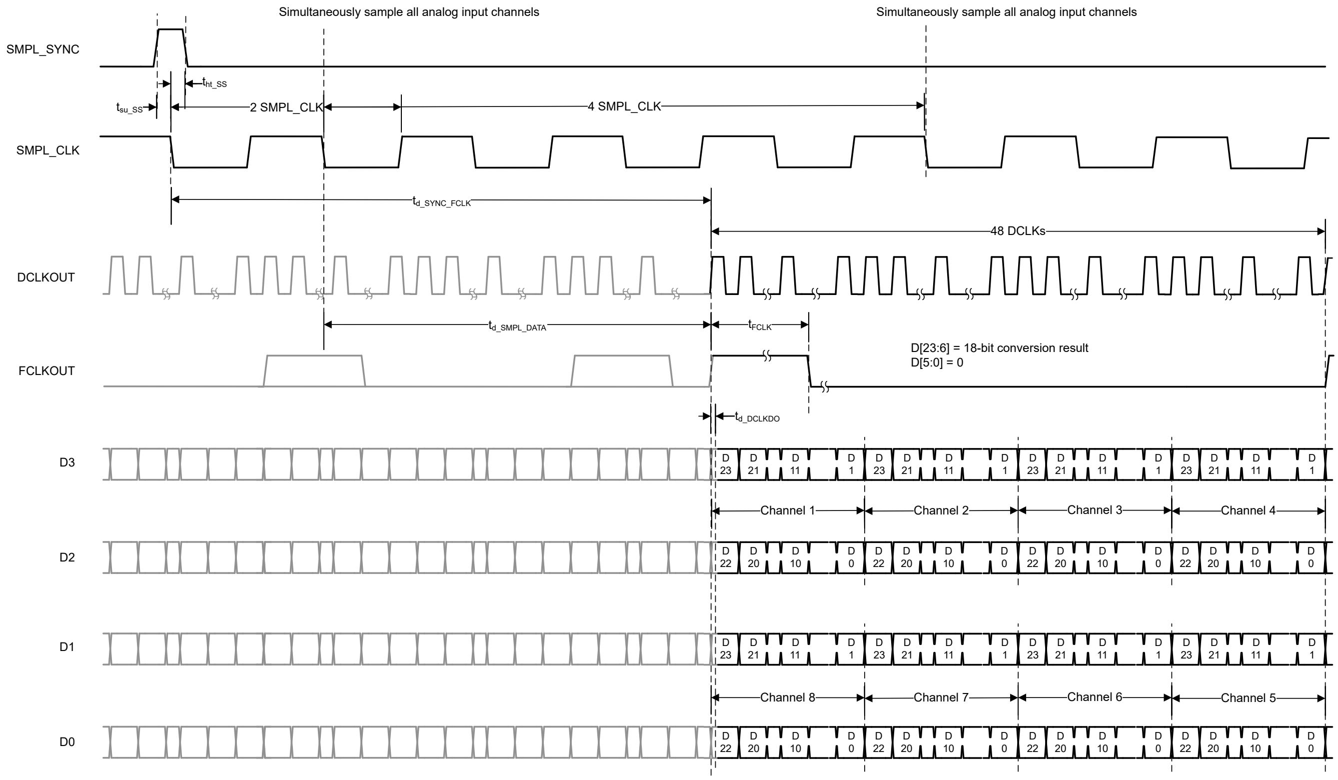


Figure 5-4. 4-SDO SDR CMOS Data Interface

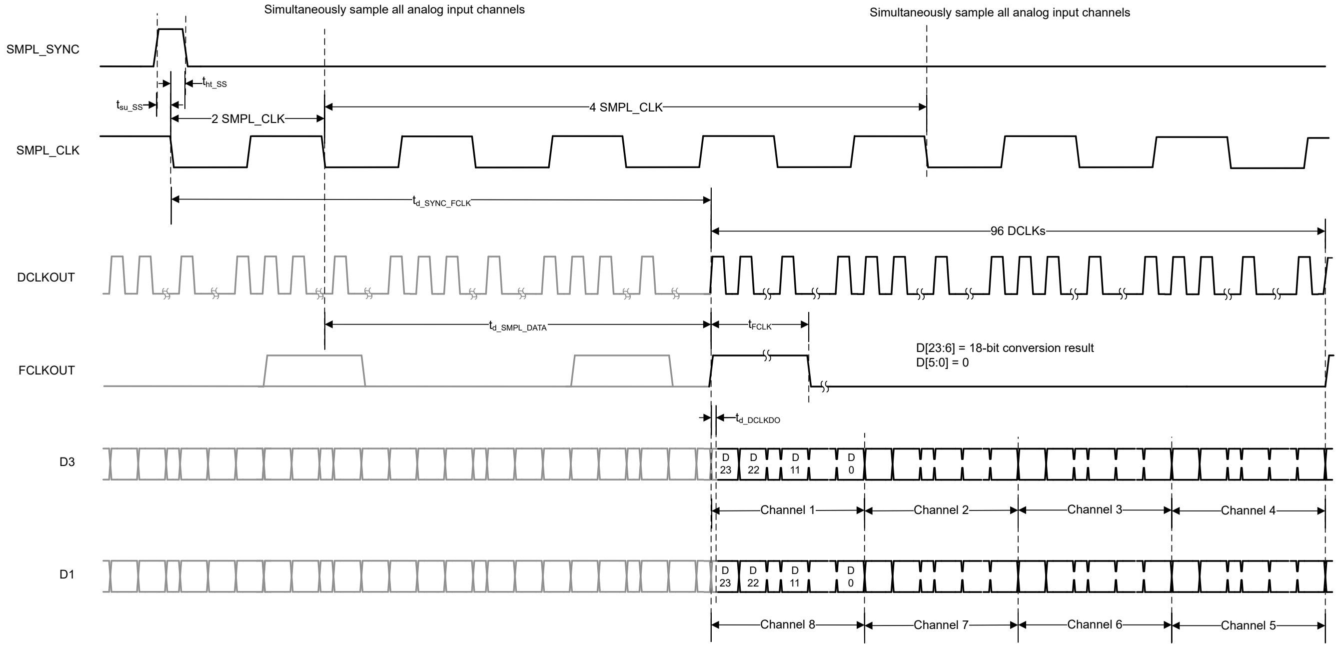


Figure 5-5. 2-SDO SDR CMOS Data Interface

5.9 Typical Characteristics

at T_A = 25°C, AVDD_5V = 5V, AVDD_1V8 = 1.8V, DVDD_1V8 = 1.8V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

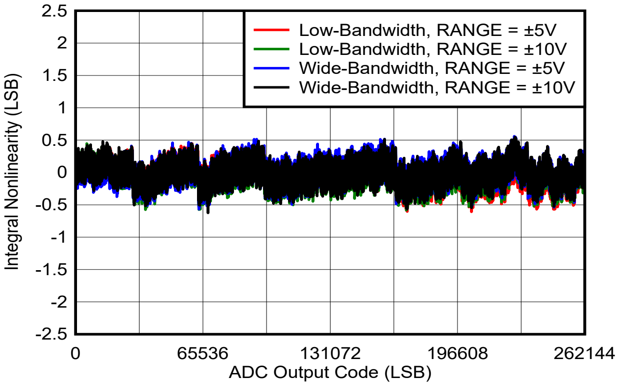


Figure 5-6. Typical INL

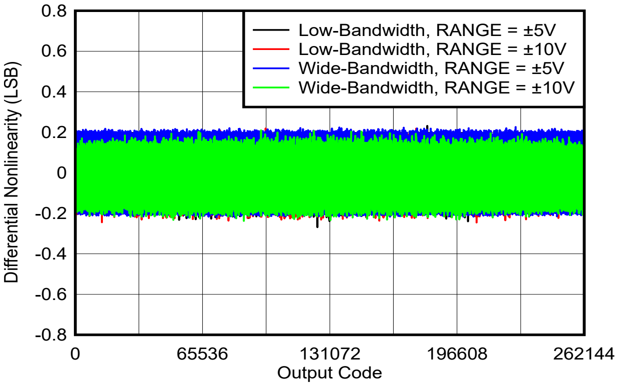
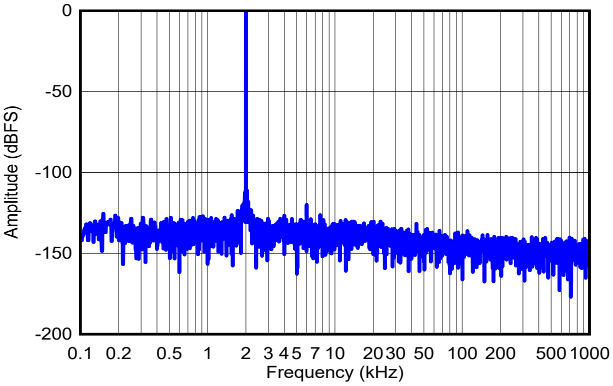
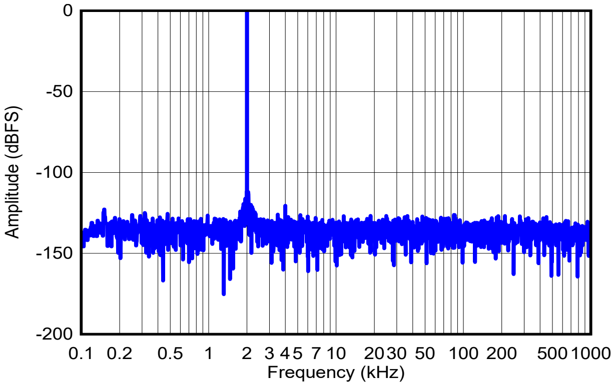


Figure 5-7. Typical DNL With Low-Noise LPF



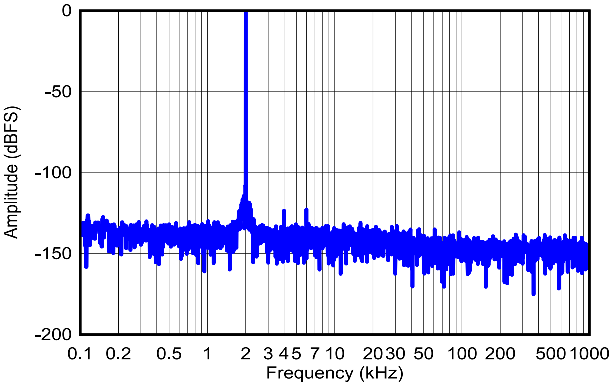
SNR = 89.1dBFS, THD = –116dB at f_{IN} = 2kHz

Figure 5-8. Typical FFT With Low-Bandwidth LPF, RANGE = ±5V



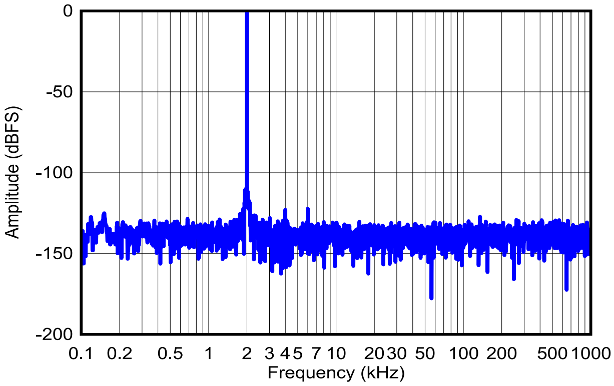
SNR = 79.7dBFS, THD = –117.3dB at f_{IN} = 2kHz

Figure 5-9. Typical FFT With Wide-Bandwidth LPF, RANGE = ±5V



SNR = 90.2dBFS, THD = –114dB at f_{IN} = 2kHz

Figure 5-10. Typical FFT With Low-Bandwidth LPF, RANGE = ±10V

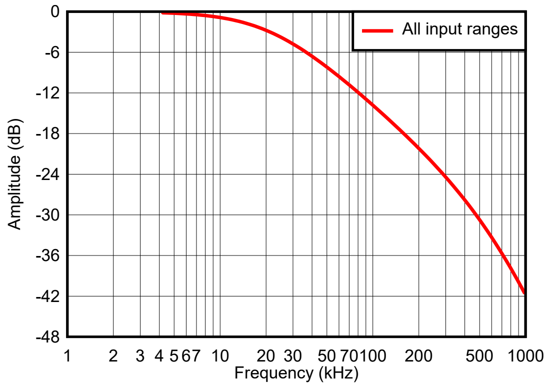


SNR = 81.6dBFS, THD = –116dB at f_{IN} = 2kHz

Figure 5-11. Typical FFT With Wide-Bandwidth LPF, RANGE = ±10V

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5V, AVDD_1V8 = 1.8V, DVDD_1V8 = 1.8V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



Typical bandwidth (–3dB) = 22.7kHz

Figure 5-12. Low-Noise LPF Frequency Response Across Input Ranges

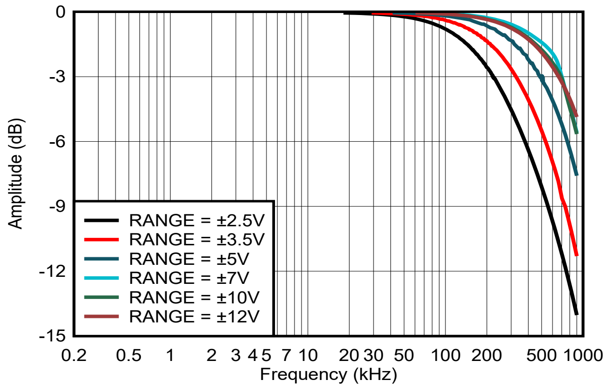
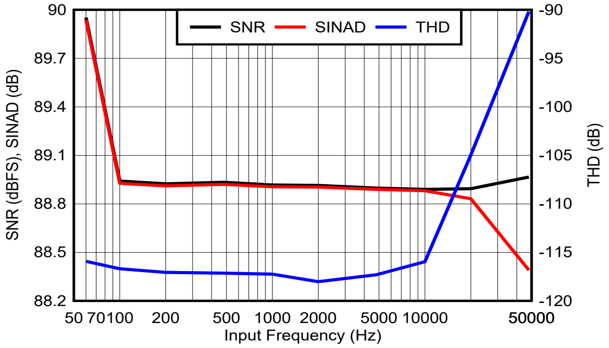
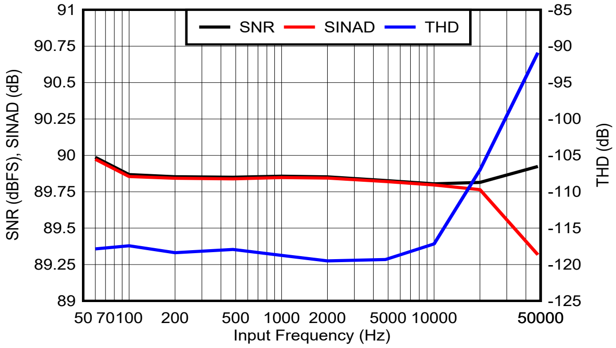


Figure 5-13. Wide-Bandwidth LPF Frequency Response Across Input Ranges



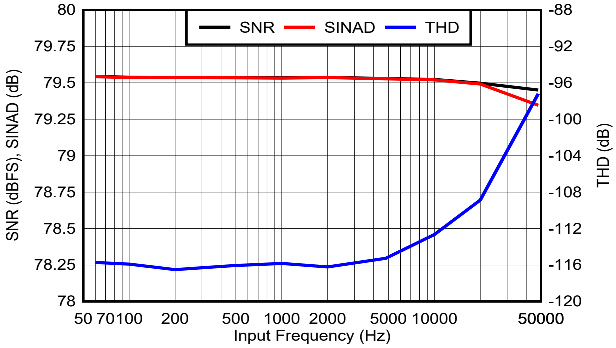
Low-Bandwidth LPF and RANGE = ±5V

Figure 5-14. SNR, SINAD, and THD vs Input Signal Frequency



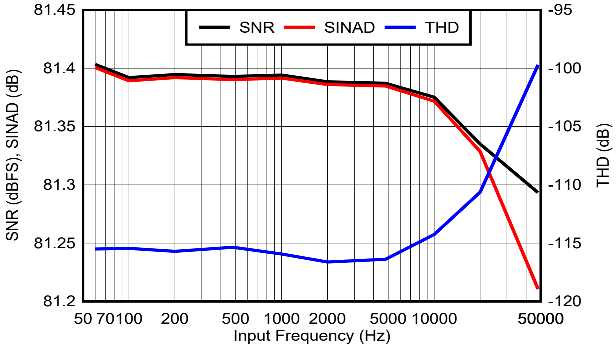
Low-Bandwidth LPF and RANGE = ±10V

Figure 5-15. SNR, SINAD, and THD vs Input Signal Frequency



Wide-Bandwidth LPF and RANGE = ±5V

Figure 5-16. SNR, SINAD, and THD vs Input Signal Frequency



Wide-Bandwidth LPF and RANGE = ±10V

Figure 5-17. SNR, SINAD, and THD vs Input Signal Frequency

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5V, AVDD_1V8 = 1.8V, DVDD_1V8 = 1.8V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

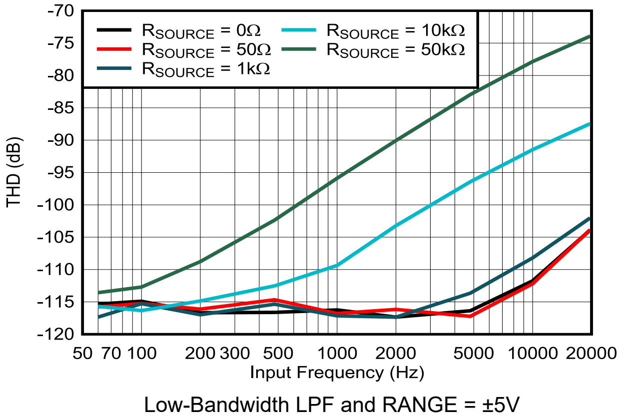


Figure 5-18. THD vs Input Signal Frequency Across External Source Impedance

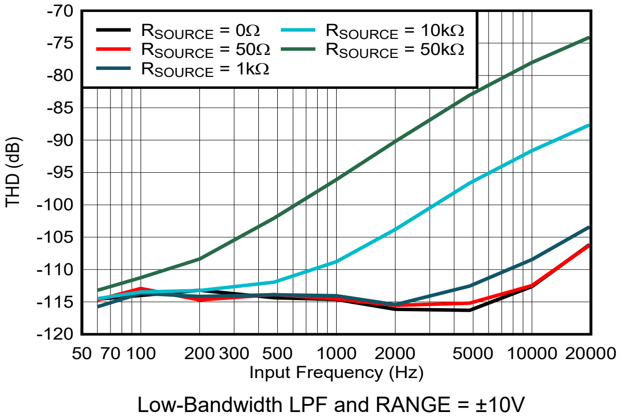


Figure 5-19. THD vs Input Signal Frequency Across External Source Impedance

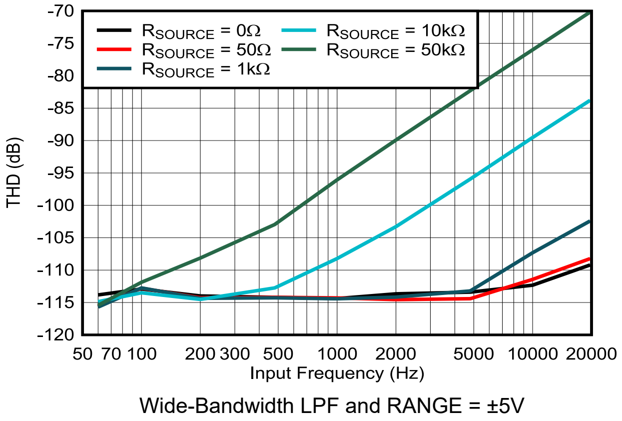


Figure 5-20. THD vs Input Signal Frequency Across External Source Impedance

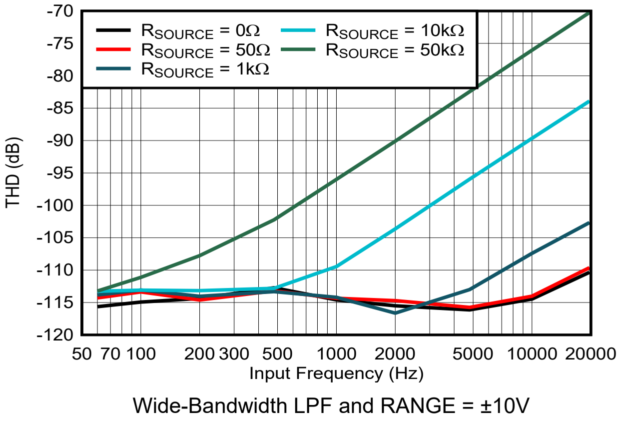


Figure 5-21. THD vs Input Signal Frequency Across External Source Impedance

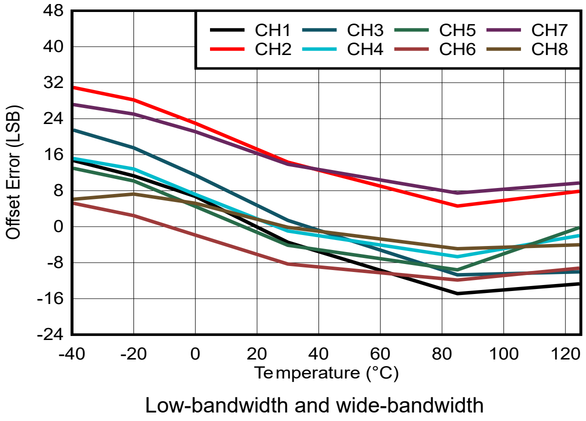


Figure 5-22. Offset Error vs Temperature, RANGE = ±5V

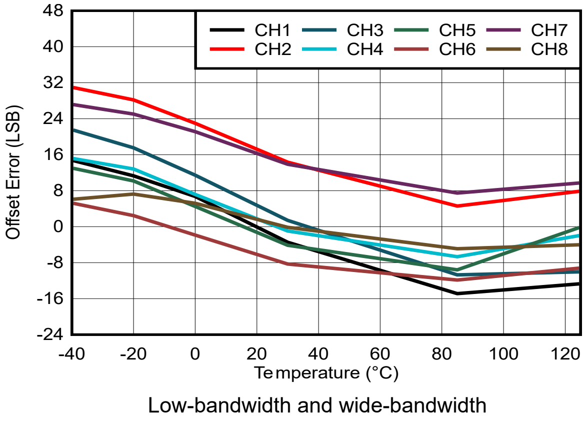
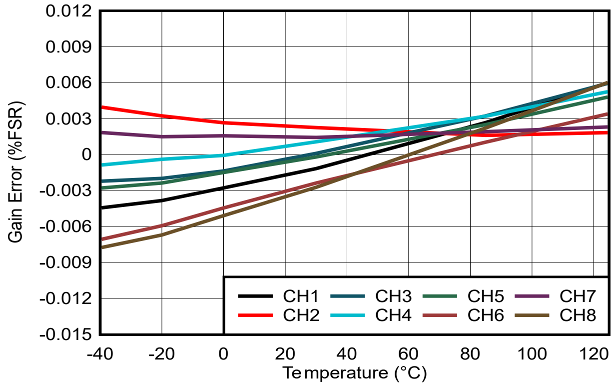


Figure 5-23. Offset Error vs Temperature, RANGE = ±10V

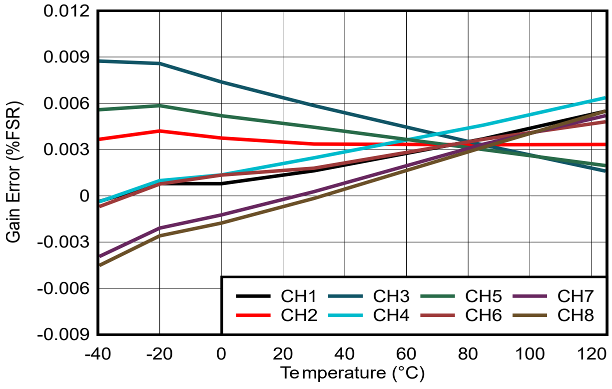
5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5V, AVDD_1V8 = 1.8V, DVDD_1V8 = 1.8V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



Low-bandwidth and wide-bandwidth

Figure 5-24. Gain Error vs Temperature, RANGE = ±5V



Low-bandwidth and wide-bandwidth

Figure 5-25. Gain Error vs Temperature, RANGE = ±10V

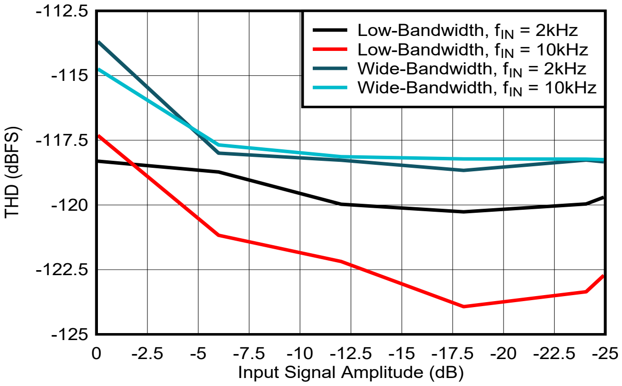


Figure 5-26. THD vs Input Signal Amplitude Across Input Signal Frequency, RANGE = ±5V

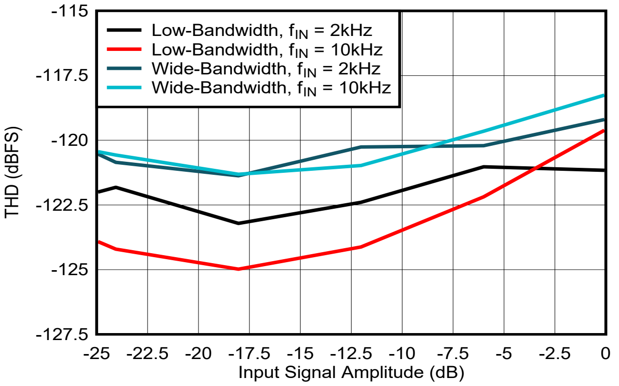


Figure 5-27. THD vs Input Signal Amplitude Across Input Signal Frequency, RANGE = ±10V

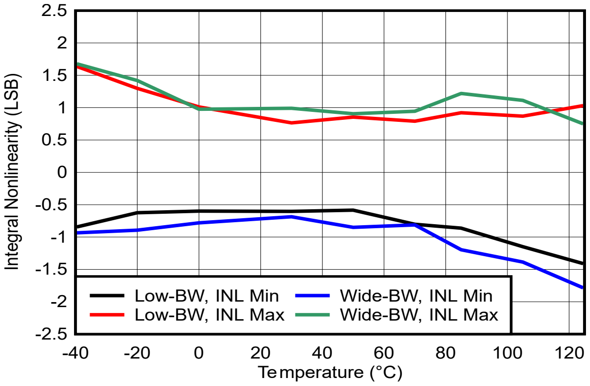


Figure 5-28. INL vs Temperature

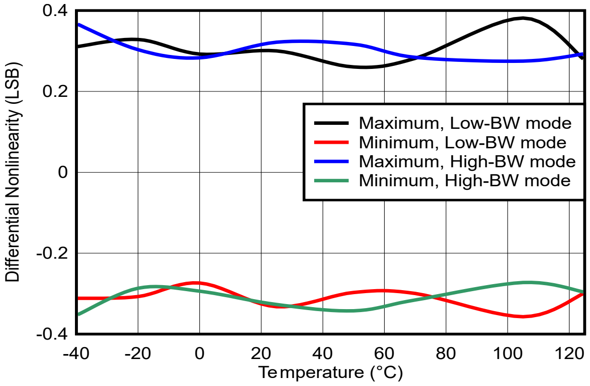


Figure 5-29. DNL vs Temperature

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5V, AVDD_1V8 = 1.8V, DVDD_1V8 = 1.8V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

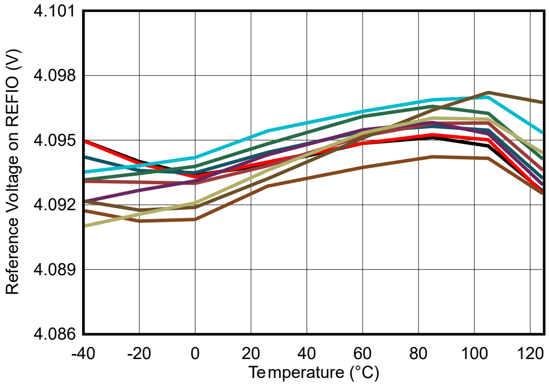


Figure 5-30. REFIO vs Temperature

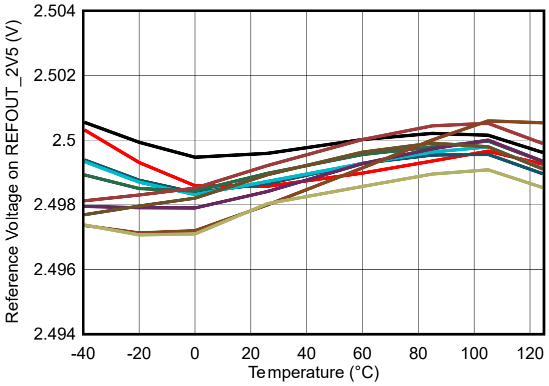
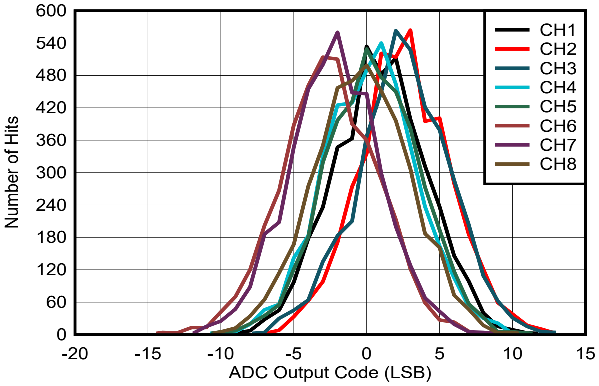
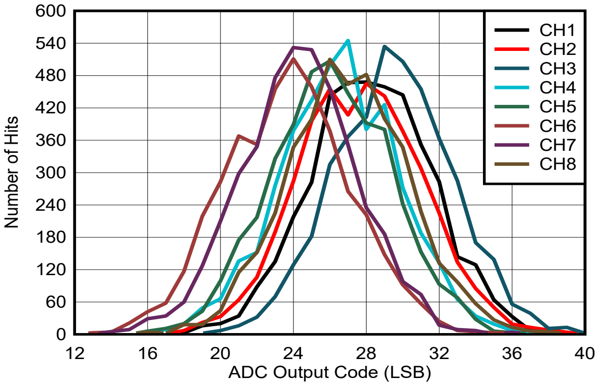


Figure 5-31. REFOUT_2V5 vs Temperature



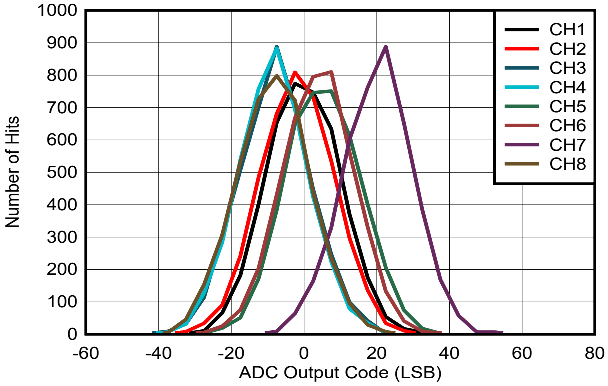
Standard deviation = 3.25LSB, number of hits = 4096

Figure 5-32. DC Histogram of Codes for AINxP = AINxM = GND, Low-Bandwidth, RANGE = ±5V



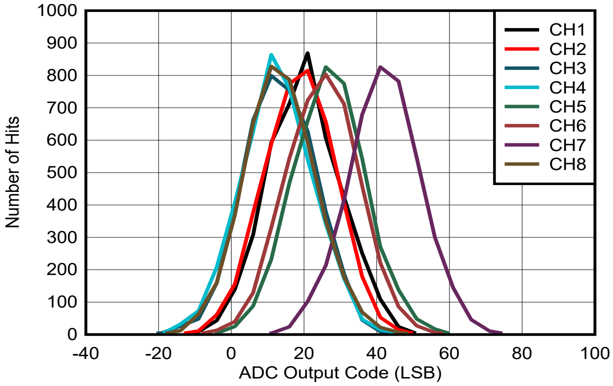
Standard deviation = 3.25LSB, number of hits = 4096

Figure 5-33. DC Histogram of Codes for V_{IN} = 1mV, Low-Bandwidth, RANGE = ±5V



Standard deviation = 9.76LSB, number of hits = 4096

Figure 5-34. DC Histogram of Codes for AINxP = AINxM = GND, Wide-Bandwidth, RANGE = ±5V



Standard deviation = 9.76LSB, number of hits = 4096

Figure 5-35. DC Histogram of Codes for V_{IN} = 1mV, Wide-Bandwidth, RANGE = ±5V

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5V, AVDD_1V8 = 1.8V, DVDD_1V8 = 1.8V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

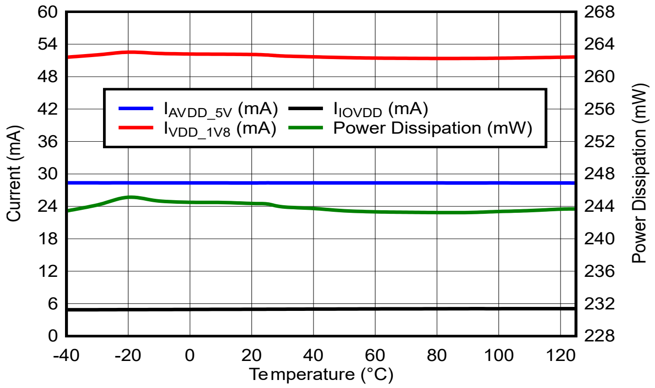


Figure 5-36. Supply Currents and Total Power Dissipation vs Temperature

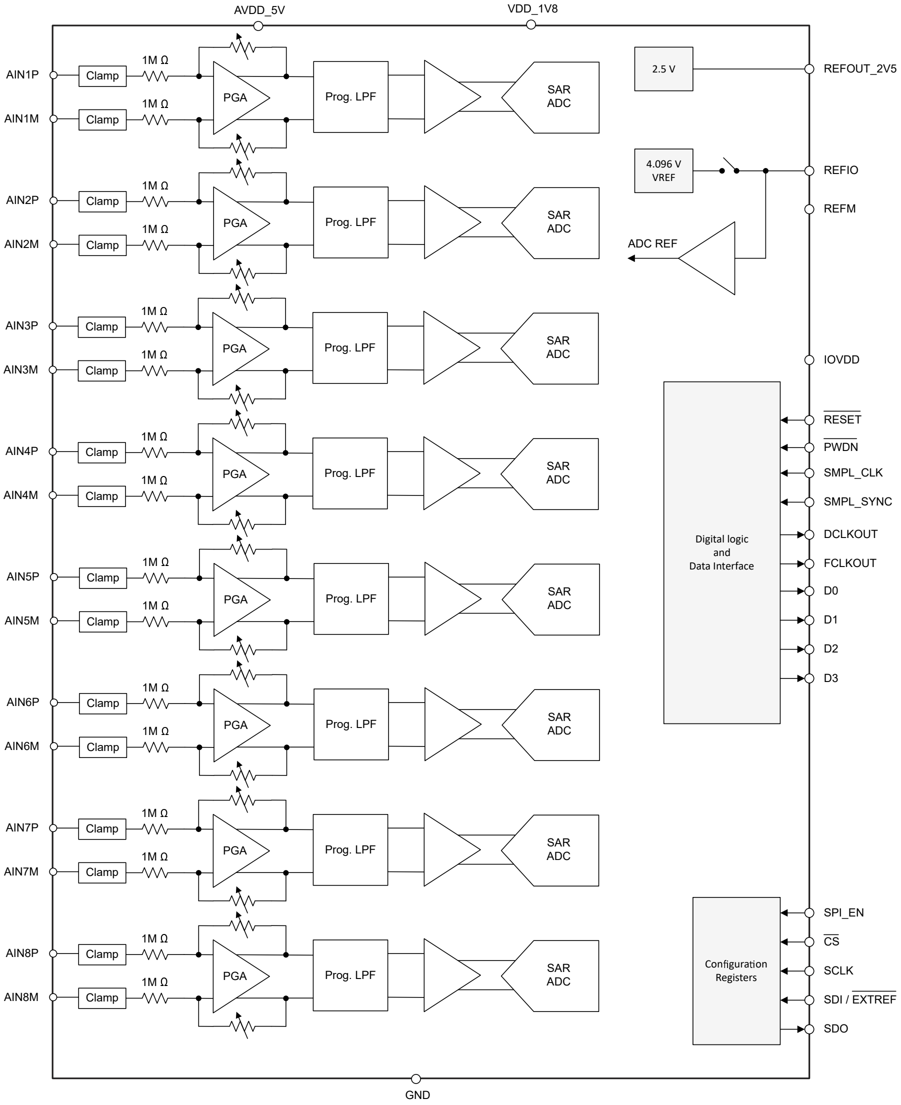
6 Detailed Description

6.1 Overview

The ADS9813 is an 18-bit data acquisition (DAQ) system with eight analog input channels configurable as either single-ended or differential. Each analog input channel consists of an input clamp protection circuit and a programmable gain amplifier (PGA) with user-selectable bandwidth options. The input signals are digitized with an 18-bit analog-to-digital converter (ADC), based on the successive approximation register (SAR) architecture. This overall system achieves a maximum throughput of 2MSPS per channel for all channels. The device has a 4.096V internal reference with several features that provide communication with a wide variety of digital hosts. These features include a fast-settling buffer, a programmable digital averaging filter to improve noise performance, and a high-speed data interface.

The device operates from 5V and 1.8V analog supplies and accommodates true bipolar input signals. The input clamp protection circuitry tolerates voltages up to ±18V. The device offers a constant 1MΩ resistive input impedance irrespective of the sampling frequency or the selected input range. The ADS9813 offers a simplified end solution without requiring external high-voltage bipolar supplies and complicated driver circuits.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Inputs

The ADS9813 incorporates eight, simultaneous sampling, 18-bit successive approximation register (SAR) analog-to-digital converters (ADCs). The device has a total of eight analog input pairs. The ADC digitizes the voltage difference between the analog input pairs AINxP – AINxM. Figure 6-1 shows the simplified circuit schematic for each analog input channel. This figure also shows the input clamp protection circuit, programmable gain amplifier (PGA), low-pass filter, high-speed ADC driver, and a precision 18-bit SAR ADC. Typical SNR for analog input ranges vs input common-mode ranges are shown in Table 6-5 for low-bandwidth mode and Table 6-6 for wide-bandwidth mode.

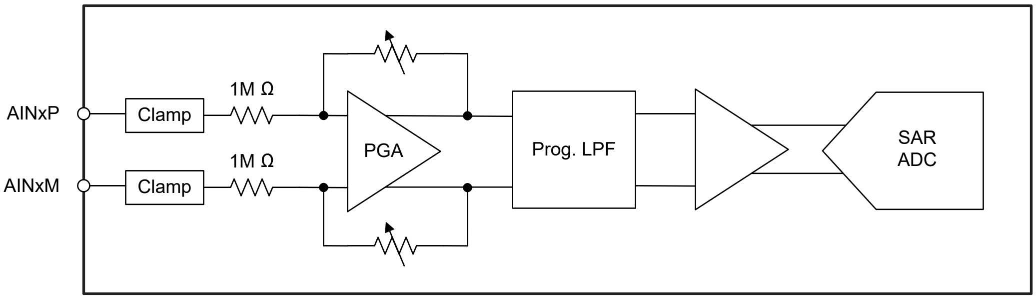


Figure 6-1. Front-End Circuit Schematic for the Selected Analog Input Channel

6.3.1.1 Input Clamp Protection Circuit

The ADS9813 features an internal clamp protection circuit (Figure 6-1) on each of the eight analog input channels. The input clamp protection circuit allows each analog input to swing up to a maximum voltage of ±18V. Beyond an input voltage of ±18V, the input clamp circuit turns on and still operates from the single 5V supply. Figure 6-2 shows a typical current versus voltage characteristic curve for the input clamp.

For input voltages above the clamp threshold, make sure that the input current never exceeds ±10mA. A resistor placed in series with the analog inputs is an effective way to limit the input current. In addition to limiting the input current, the series resistor also provides an antialiasing, low-pass filter (LPF) when coupled with a capacitor. Matching the external source impedance on the AINxP and AINxM pins cancels any additional offset error.

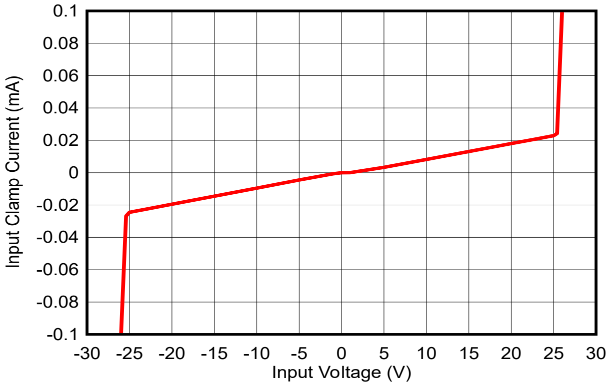


Figure 6-2. Input Protection Clamp Profile, Input Clamp Current vs Source Voltage

6.3.1.2 Programmable Gain Amplifier (PGA)

The ADS9813 features a PGA at every analog input channel. The PGA supports single-ended and differential inputs with a bipolar signal swing. Table 6-1 lists the supported analog input ranges. Configure the analog input range independently for each channel with the RANGE_CHx register fields in address 0xC2 and address 0xC3.

Table 6-1. Analog Input Ranges

DIFFERENTIAL INPUTS	SINGLE-ENDED INPUTS	RANGE_CHx CONFIGURATION
±12V	±12V	5
±10V	±10V	4
±7V	±7V	3
±5V	±5V	0
±3.5V	±3.5V	1
±2.5V	±2.5V	2

Each analog input channel features an antialiasing, low-pass filter (LPF) at the output of the PGA. Table 6-2 lists the various programmable LPF options available in the ADS9813 corresponding to the analog input range. Figure 5-12 and Figure 5-13 illustrate the frequency responses for low-bandwidth and wide-bandwidth LPF configurations. Select the analog input bandwidth for the eight analog input channels with the ANA_BW[7:0] bits in address 0xC0 of register bank 1.

Table 6-2. Low-Pass Filter Corner Frequency

LPF	ANALOG INPUT RANGE	CORNER FREQUENCY (–3dB)
Low-bandwidth	All input ranges	22.7kHz
Wide-bandwidth	±12V	664kHz
	±10V	691kHz
	±7V	700kHz
	±5V	500kHz
	±3.5V	325kHz
	±2.5V	221kHz

6.3.1.3 Wide-Common-Mode Voltage Rejection Circuit

The ADS9813 features a common-mode (CM) rejection circuit at the analog inputs that supports CM voltages up to ±12V. The CM voltage for differential inputs is given by Equation 1. On power-up or after reset, the common-mode voltage range for the analog input channels is ±12V (CM_CTRL_EN = 0b). In all cases, make sure the voltage at the analog inputs is within the *Absolute Maximum Ratings*.

$$\text{Common mode voltage} = \frac{(\text{Voltage on AINP}) + (\text{Voltage on AINM})}{2} \tag{1}$$

As described in Table 6-3, optimize the CM voltage rejection circuit for various CM voltages for differential inputs.

Table 6-3. Wide Common-Mode Configuration for Differential Inputs

COMMON-MODE (CM) RANGE	CM_CTRL_EN	ANALOG INPUT CHANNELS 1–4		ANALOG INPUT CHANNELS 5–8	
		CM_EN_CH[4:1]	CM_RNG_CH[4:1]	CM_EN_CH[8:5]	CM_RNG_CH[8:5]
CM ≤ ±1V	1	0	Don't care	0	Don't care
CM ≤ ±RANGE / 2		1	0	1	0
CM ≤ ±6V			1		1
CM ≤ ±12V			2		2

The CM voltage rejection circuit is configured depending on the analog input range of the PGA when using single-ended inputs. Table 6-4 lists the recommended configuration for single-ended inputs for various analog input voltage ranges.

Table 6-4. Wide Common-Mode Configuration for Single-Ended Inputs

PGA ANALOG INPUT RANGE	CM_CTRL_EN	ANALOG INPUT CHANNELS 1–4		ANALOG INPUT CHANNELS 5–8	
		CM_EN_CH[4:1]	CM_RNG_CH[4:1]	CM_EN_CH[8:5]	CM_RNG_CH[8:5]
±2.5V, ±3.5V, and ±5V	1	0	Don't care	0	Don't care
±7V, ±10V, and ±12V		1	0	1	0

Typical SNR for analog input ranges vs input common-mode ranges are shown in Table 6-5 for low-bandwidth mode and Table 6-6 for wide-bandwidth mode.

Table 6-5. Typical SNR (dBFS) for Analog Input Range vs Common-Mode Range in Low-Bandwidth Mode

RANGE	CM ≤ ±1V	CM ≤ ±RANGE / 2	CM ≤ ±6V	CM ≤ ±12V
±2.5V	88.3	87.4	85.2	83.4
±3.5V	88.3	88.4	87.0	85.4
±5V	90.1	89.1	88.4	87.2
±7V	–	89.8	89.4	88.5
±10V	–	90.2	90.2	89.5
±12V	–	90.3	90.3	89.9

Table 6-6. Typical SNR (dBFS) for Analog Input Range vs Common-Mode Range in Wide-Bandwidth Mode

RANGE	CM ≤ ±1V	CM ≤ ±RANGE / 2	CM ≤ ±6V	CM ≤ ±12V
±2.5V	80.5	79.1	76.7	74.7
±3.5V	81.1	79.4	77.6	75.8
±5V	81.6	79.7	78.4	76.7
±7V	–	80.0	79.2	77.5
±10V	–	81.6	81.2	79.7
±12V	–	82.4	82.4	80.9

6.3.2 ADC Transfer Function

The ADS9813 outputs 18 bits of conversion data in either straight-binary or binary two's-complement formats. The format for the output codes is the same across all analog channels. Select the format for the output codes with the DATA_FORMAT register bits. Figure 6-3 and Table 6-7 show the transfer characteristics for the ADS9813. The LSB size depends on the analog input range selected.

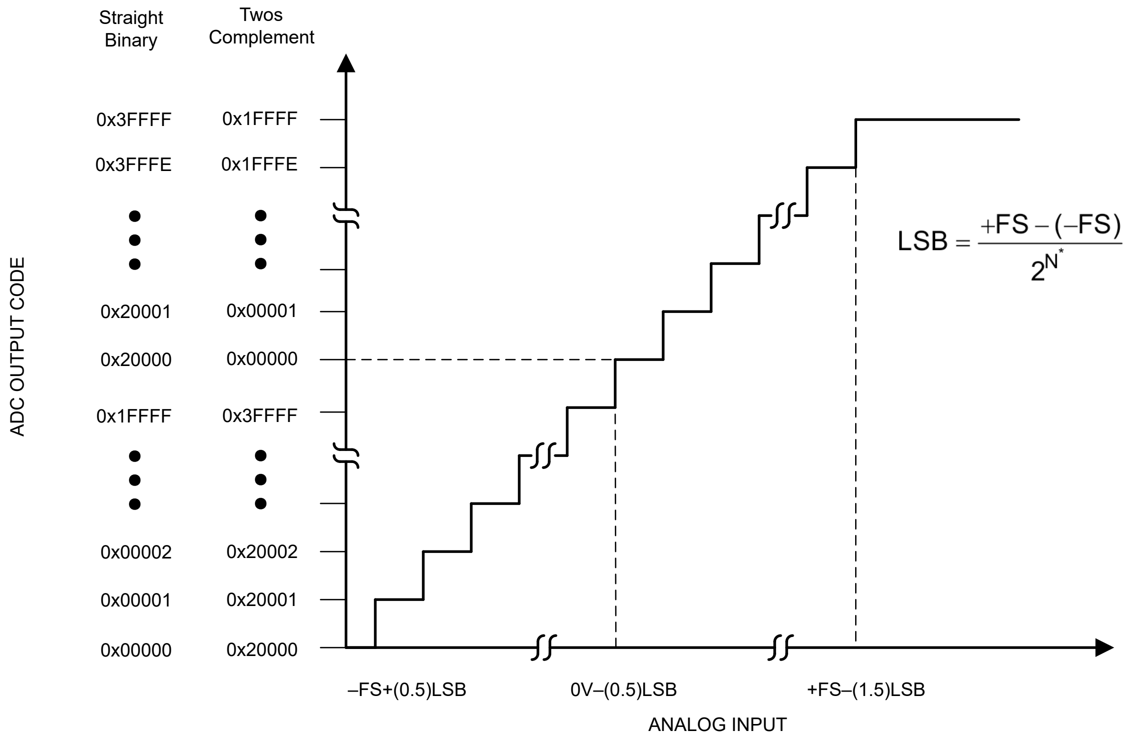


Figure 6-3. Transfer Characteristics

Table 6-7. ADC Full-Scale Range and LSB Size

RANGE	+FS	MIDSCALE	–FS	LSB
±2.5V	2.5V	0V	–2.5V	19.07µV
±3.5V	3.5V	0V	–3.5V	26.70µV
±5V	5V	0V	–5V	38.15µV
±7V	7V	0V	–7V	53.41µV
±10V	10V	0V	–10V	76.29µV
±12V	12V	0V	–12V	91.55µV

6.3.3 ADC Sampling Clock Input

Operate the ADS9813 with a differential or a single-ended clock input where the single-ended clock consumes less power consumption. Make sure the sampling clock is a free-running continuous clock. After a free-running sampling clock is applied, the ADC generates valid output data, the data clock, and the frame clock $t_{PU\_SMPL\_CLK}$. These parameters are specified in the *Switching Characteristics* section. The ADC output data, data clock, and frame clock are invalid when the sampling clock is stopped.

Figure 6-4 and Figure 6-5 show that the sampling clock is either differential or single-ended, respectively.

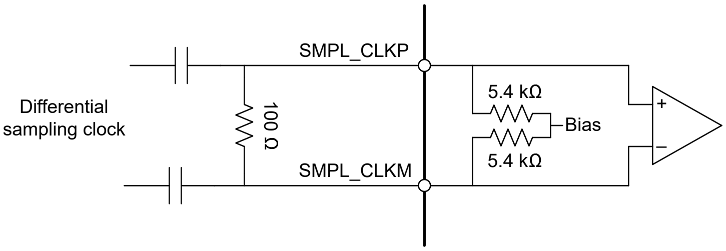


Figure 6-4. AC-Coupled Differential Sampling Clock

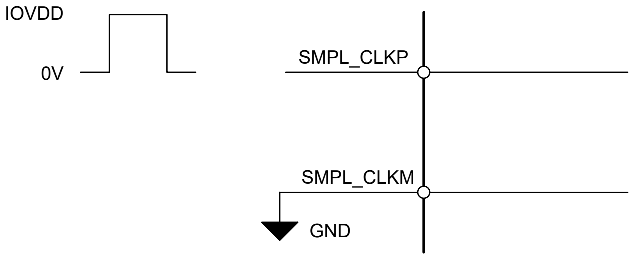


Figure 6-5. Single-Ended Sampling Clock

6.3.4 Synchronizing Multiple ADCs

Use the SMPL_SYNC signal to simultaneously sample all analog input channels of multiple ADS9813 devices. All ADS9813 devices share the same SMPL_CLK and SMPL_SYNC signals with identical delays external to the ADC. A positive pulse on the SMPL_SYNC pin centered around the falling edge of the SMPL_CLK signal synchronizes all ADCs; see Figure 5-2. The synchronization signal is only required one time after power-up with the sampling clock free-running, or after restarting sampling clock, or after a device reset. As illustrated in Figure 5-2, Figure 5-3, Figure 5-4, and Figure 5-5, the SYNC signal resets the internal analog channel selection logic and aligns the FCLKOUT signal to the data frame. If no SYNC signal is given, the internal analog channel selection logic and FCLKOUT are not synchronized, which can lead to a different alignment between the sequence of channel output data and FCLKOUT. When using multiple ADCs with the same sampling clock, the SYNC signal makes sure all ADCs sample the same respective analog input channel at the same time.

6.3.5 Reference Voltage

The ADS9813 has a precision, low-drift voltage reference internal to the device. For best performance, the internal reference noise is filtered (as shown in Figure 6-6) by connecting a 10µF ceramic bypass capacitor to the REFIO pin. As shown in Figure 6-7, an external reference is also connected at the REFIO pin. When using an external reference, disable the internal reference voltage by either of the following two options:

- Configure the SPI (SPI_EN pin = logic 1). Write PD_REF = 1b in address 0xC1 of register bank 1.
- Use the SDI/$\overline{\text{EXTREF}}$ pin (SPI_EN pin = logic 0). Set the SDI/EXTREF pin to logic 0 using a pulldown resistor.

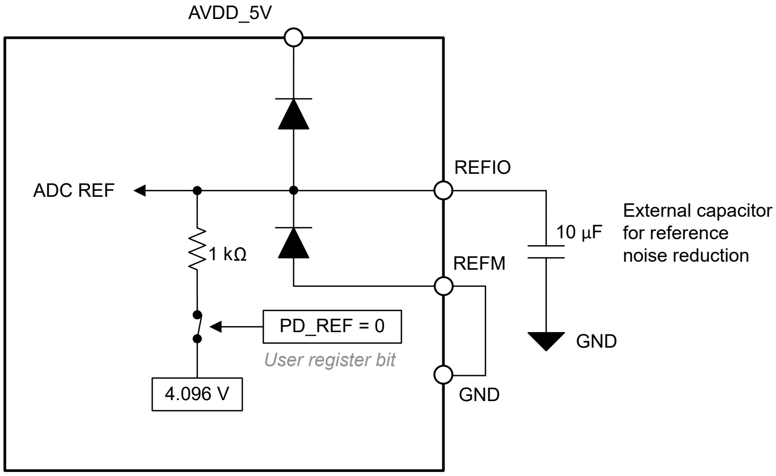


Figure 6-6. Internal Reference Voltage

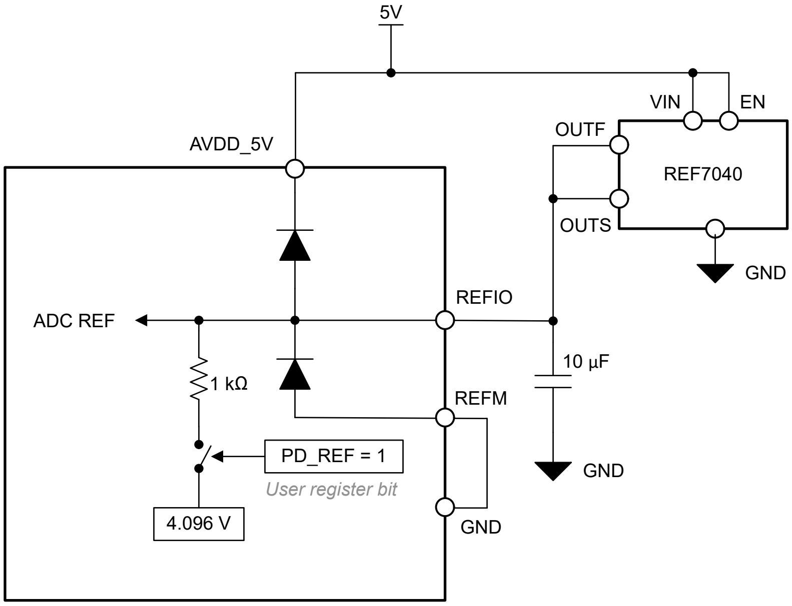


Figure 6-7. External Reference Voltage

6.3.6 Data Interface

The ADS9813 supports 2-lane and 4-lane mode with single-data-rate (SDR) and double-data-rate (DDR) interface modes. The data interface can be selected using the configuration SPI as described in Table 6-8. The ADC generates the data (D[3:0]), data clock (DCLKOUT), and frame clock (FCLKOUT) in response to the sampling clock signal on the SMPL_CLK input pin. The 18-bit ADC conversion result is output MSB first in a 24-bit data packet and the last six bits are zeroes.

The data interface signals can be described as:

- D[3:0]: Data output from the ADC. In 4-lane mode all four lanes are used, whereas in 2-lane mode D3 and D1 are used to output ADC data.
- DCLKOUT: Data clock output from the ADC.
- FCLKOUT: Frame clock output from the ADC delimiting each set of 8-channel data. A SYNC pulse is required on power-up or after device reset to align the rising edge of FCLKOUT with channel 1 data output, as described in the *Synchronizing Multiple ADCs* section.

Use the registers in Table 6-8 to configure the data interface.

Table 6-8. Register Configurations For Interface Modes

INTERFACE MODE	FIGURE	DATA_RATE (Address = 0xC1)	DATA_LANES (Address = 0xC1)
4-lane, DDR	Figure 5-2	0	0
2-lane, DDR	Figure 5-3	0	1
4-lane, SDR	Figure 5-4	1	0
2-lane, SDR	Figure 5-5	1	1

6.3.6.1 Data Clock Output

The ADS9813 features a source-synchronous data interface where the ADC provides the output data and the clock to capture the data. The clock to capture the data is output on the DCLKOUT pin. The clock frequency depends on the sampling clock speed, data rate (SDR or DDR), and number of output lanes (four lanes or two lanes) and is given by Equation 2. The frame clock frequency is given by Equation 3.

$$\text{Data clock frequency} = \frac{24\ \text{bits/channel} \times 8\ \text{channels}}{\text{Number of data lanes} \times \text{Data rate (SDR} = 1,\ \text{DDR} = 2)} \times \text{Frame clock frequency} \tag{2}$$

$$\text{Frame clock frequency} = \frac{\text{Sampling clock frequency}}{4} \tag{3}$$

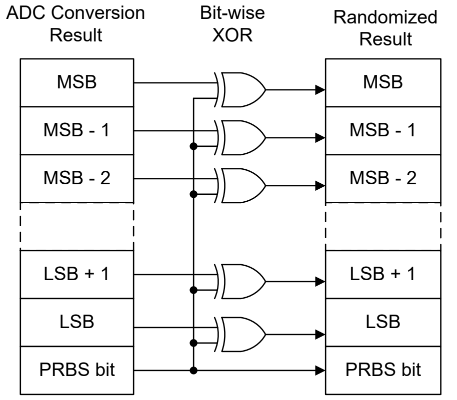
Table 6-9 shows the data clock frequency for the maximum sampling rates for the ADS9817 and ADS9815 for various interface modes.

Table 6-9. Data Clock Frequency for Interface Modes

INTERFACE MODE	ADS9815 (f_{SMPL_CLK} = 4MHz)	ADS9817 (f_{SMPL_CLK} = 8MHz)
4-lane, DDR	24MHz	48MHz
2-lane, DDR	48MHz	96MHz
4-lane, SDR	48MHz	96MHz
2-lane, SDR	96MHz	Not supported

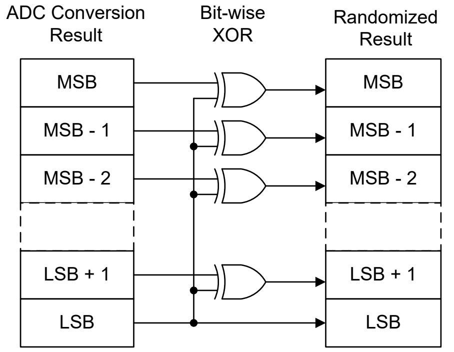
6.3.6.2 ADC Output Data Randomizer

The ADS9813 features a data output randomizer. When enabled, the ADC conversion result is bit-wise exclusive-ORed (XOR) with either the LSB of the conversion result (Figure 6-9) or XOR_PRBS bit that can be appended to the ADC data output (Figure 6-8). The LSB of the ADC conversion result and XOR_PRBS have equal probability of being either 1 or 0. As a result of the XOR operation, the data output from the ADS9813 is randomized. The ground bounce created by the transmission of this randomized result over the data interface is uncorrelated with the analog input voltage. This uncorrelated transmission helps minimize interference between data transmission and analog performance of the ADC when the PCB layout does not minimize ground bounce.



PRBS bit is appended after LSB of conversion result
Register XOR_PRBS = 0b

Figure 6-8. Bit-Wise XOR Operation with PRBS Bit



LSB of conversion result is used for XOR operation
Register XOR_PRBS = 1b

Figure 6-9. Bit-Wise XOR Operation with ADC LSB

6.3.6.3 Data Averaging

The ADS9813 features two modes of data averaging to improve SNR - simple average and moving average. Simple averaging reduces the output data rate by a factor of 2 whereas moving average does not affect the output data rate. Table 6-10 and Table 6-11 show the register operations to enable and disable the simple average and moving average respectively.

Table 6-10. Register Operations for Simple Average

STEP #	REGISTER FIELD	ENABLE SIMPLE AVERAGE	DISABLE SIMPLE AVERAGE
1	REG_BANK_SEL	2	2
2	EN_AVG	1	0
3	AVG_CFG3	1	0
4	AVG_CFG2	3	0
5	AVG_CFG1	1	0
6	AVG_CFG4	3	0

Table 6-11. Register Operations for Moving Average

STEP #	REGISTER FIELD	ENABLE SIMPLE AVERAGE	DISABLE SIMPLE AVERAGE
1	REG_BANK_SEL	2	2
2	EN_AVG	1	0
3	EN_MVG_AVG	1	0

6.3.6.4 Test Patterns for Data Interface

The ADS9813 features test patterns used by the host for debugging and verifying the data interface. The test patterns replace the ADC output data with predefined digital data. Enable the test patterns by configuring the corresponding register addresses 0x13 through 0x1B in bank 1.

Table 6-12 lists the test patterns supported by the ADS9813.

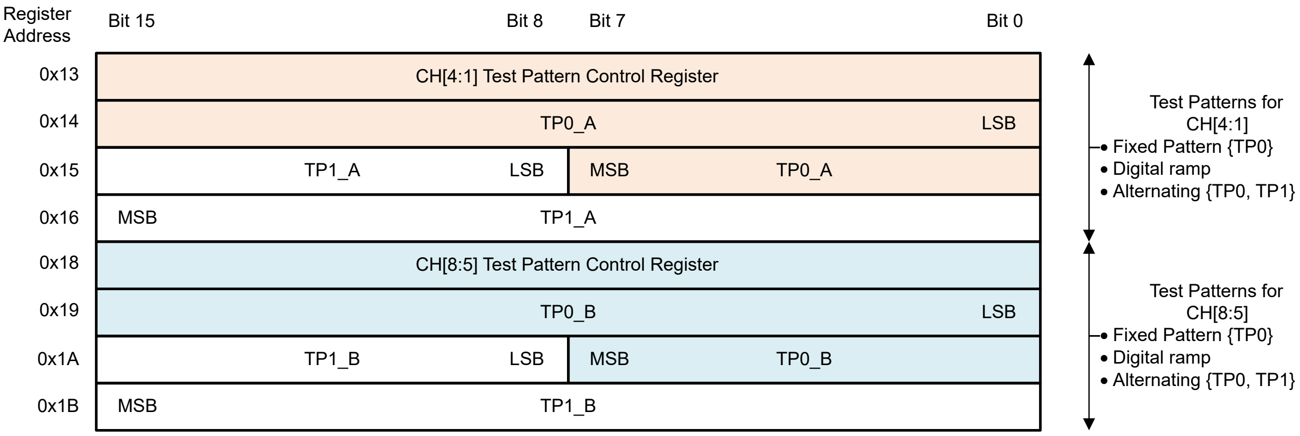


Figure 6-10. Register Bank for Test Patterns

Table 6-12. Test Pattern Configurations

ADC OUTPUT	TP_EN_CH[4:1] TP_EN_CH[8:5]	TP_MODE_CH[4:1] TP_MODE_CH[8:5]	SECTION	RESULT[1]
ADC conversion result	0			
Fixed pattern	1	0 or 1	*Fixed Pattern*	CH[4:1] = TP0_A CH[8:5] = TP0_B
Digital ramp	1	2	*Digital Ramp*	CH[4:1] = Digital ramp CH[8:5] = Digital ramp
Alternating test patterns	1	3	*Alternating Test Pattern*	CH[4:1] = TP0_A, TP1_A CH[8:5] = TP0_B, TP1_B

Note

1. Configure the test patterns for two separate channel groups CH[4:1] and CH[8:5].

6.3.6.4.1 Fixed Pattern

The ADC outputs fixed patterns defined in the TP0_A and TP0_B registers in place of the CH[4:1] and CH[8:5] data, respectively.

- Configure the test patterns in TP0_A and TP0_B
- Set TP_EN_CH[4:1] = 1, TP_MODE_CH[4:1] = 0 (address = 0x13), TP_EN_CH[8:5] = 1, and TP_MODE_CH[8:5] = 0 (address = 0x18)

6.3.6.4.2 Digital Ramp

The ADC outputs digital ramp values with increments specified in the RAMP_INC_A and RAMP_INC_B registers in place of the CH[4:1] and CH[8:5] data, respectively.

- Configure the increment value between two successive steps of the digital ramp in the RAMP_INC_A (address = 0x13) and RAMP_INC_B (address = 0x18) registers, respectively. The digital ramp increments by N + 1, where N is the value configured in these registers.
- Set TP_EN_CH[4:1] = 1, TP_MODE_CH[4:1] = 2 (address = 0x13), TP_EN_CH[8:5] = 1, and TP_MODE_CH[8:5] = 2 (address = 0x18)

6.3.6.4.3 Alternating Test Pattern

The ADC outputs alternating test patterns defined in the TP0_A, TP1_A and TP0_B, TP1_B registers in place of the CH[4:1] and CH[8:5] data, respectively.

- Configure the test patterns in TP0_A, TP1_A, TP0_B, and TP1_B
- Set TP_EN_CH[4:1] = 1, TP_MODE_CH[4:1] = 3 (address = 0x13), TP_EN_CH[8:5] = 1, and TP_MODE_CH[8:5] = 3 (address = 0x18)

6.4 Device Functional Modes

6.4.1 Reset

Power down the ADS9813 with a logic 0 on the $\overline{\text{RESET}}$ pin or write 1b to the RESET field of address 0x00 in register bank 0. The device registers are initialized to the default values after reset and the device is initialized with a sequence of register write operations. See the *Initialization Sequence* section for further information.

6.4.2 Power-Down

Power down the ADS9813 with a logic 0 on the $\overline{\text{PWDN}}$ pin or write 11b to the PD_CH field in address 0xC0 in register bank 1. The device registers are initialized to the default values after power-up and the device is initialized with a sequence of register write operations. See the *Initialization Sequence* section for further information.

6.4.3 Initialization Sequence

As shown in Table 6-13, initialize the ADS9813 with a sequence of register writes after device power-up or reset. Connect a free-running sampling clock to the ADC before executing the initialization sequence. The ADS9813 registers are initialized with the default value after the initialization sequence is complete.

Table 6-13. ADS9813 Initialization Sequence

STEP	REGISTER			COMMENT
	BANK	ADDRESS	VALUE[15:0]	
1	0	0x04	0x000B	INIT_1 configured
2	0	0x03	0x0010	Select register bank 2
3	2	0x92	0x0002	INIT_2 configured
3	2	0xC5	0x0604	Initialize PGA and conifgure INIT_3

As shown in Table 6-14, change the default settings of the ADS9813 for the user-defined configuration. Changes to the analog inputs changes the analog input range, bandwidth, and common-mode voltage range. Changes to the data interface change the number of output lanes (either single or double data rate).

Table 6-14. ADS9813 User-Configuration

STEP	REGISTER			COMMENT
	BANK	ADDRESS	VALUE[15:0]	
1	1	0xC1	User defined	Configure data interface and select internal or external reference
2	1	0xC2 and 0xC3	User defined	Select analog input ranges, see Table 6-1
3	1	0xC0	User defined	Select analog input bandwidth, see Table 6-2
4	1	0xC4 and 0xC5	User defined	Select common-mode range for analog inputs, see Table 6-3 and Table 6-4

6.4.4 Normal Operation

After the ADS9813 is initialized (see the *Initialization Sequence* section), the ADS9813 converts analog input voltages to digital output voltages. A free-running sampling clock is required for normal device operation; see the *ADC Sampling Clock Input* section.

6.4.5 Speed-Boost Mode

ADS9813 supports a speed-boost mode that allows up to 8MSPS sampling rate for a user-selected analog input channel pair. In the speed-boost mode, only the user-selected channel pair is converted while the remaining 6 analog input channels are idle. The sampling rate is equal to the sampling clock frequency. The user can select any pair combination of analog inputs from the list below:

- CH1 and CH8
- CH2 and CH7
- CH3 and CH6
- CH4 and CH5

The data output interface specifications remain the same as normal mode of operation. CH[4:1] and CH[8:5] output data is replaced, respectively, by data corresponding to the channel pair selected.

Table 6-15 shows the register operations to enable or disable the speed-boost mode.

Table 6-15. Register operations for Speed-Boost Mode

STEP #	REGISTER FIELD	ENABLE SPEED-BOOST	DISABLE SPEED-BOOST
1	REG_BANK_SEL	2	2
2	BOOST_CFG1	3	0
3	BOOST_CFG2	1	0
4	EN_BOOST	1	0
5	SEL_CH_BOOST	• 0 for CH1 and CH8 • 1 for CH2 and CH7 • 2 for CH3 and CH6 • 3 for CH4 and CH5	0
6	REG_BANK_SEL	16	16
7	BOOST_CFG3	1	0
8	BOOST_CFG4	1	0

6.5 Programming

6.5.1 Register Write

Register write access is enabled by setting SPI_RD_EN = 0b. The 16-bit configuration registers are grouped in three register banks and are addressable with an 8-bit register address. Select register bank 1 and register bank 2 for read or write operation by configuring the REG_BANK_SEL bits. Registers in bank 0 are always accessible, irrespective of the REG_BANK_SEL bits. These register addresses are unique and are therefore not used in register banks 1 and 2.

As shown in Figure 6-11, steps to write to a register are:

1. Frame 1: Write to register address 0x03 in register bank 0 to select either register bank 1 or bank 2 for a subsequent register write. This frame has no effect when writing to registers in bank 0.
2. Frame 2: Write to the register in the bank selected in frame 1. Repeat this step for writing to multiple registers in the same register bank.

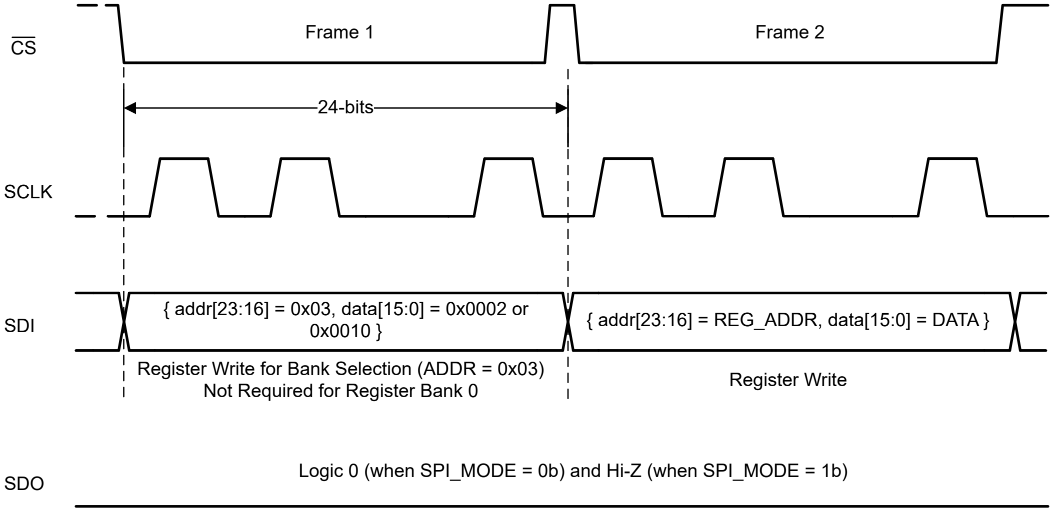


Figure 6-11. Register Write

6.5.2 Register Read

Select the desired register bank by writing to register address 0x03 in register bank 0. Register read access is enabled by setting SPI_RD_EN = 1b and SPI_MODE = 1b in register bank 0. As illustrated in Figure 6-12, read registers by using two 24-bit SPI frames after the SPI_RD_EN and SPI_MODE bits are set. The first SPI frame selects the register bank. The ADC returns the 16-bit register value in the second SPI frame corresponding to the 8-bit register address.

As illustrated in Figure 6-12, the steps to read a register are:

1. Frame 1: With SPI_RD_EN = 0b, write to register address 0x03 in register bank 0 to select the desired register bank 0 for reading.
2. Frame 2: Set SPI_RD_EN = 1b and SPI_MODE = 1b in register address 0x00 in register bank 0.
3. Frame 3: Read any register in the selected bank using a 24-bit SPI frame containing the desired register address. Repeat this step with the address of any register in the selected bank to read the corresponding register.
4. Frame 4: Set SPI_RD_EN = 0 to disable register read and re-enable register writes.
5. Repeat steps 1 through 4 to read registers in a different bank.

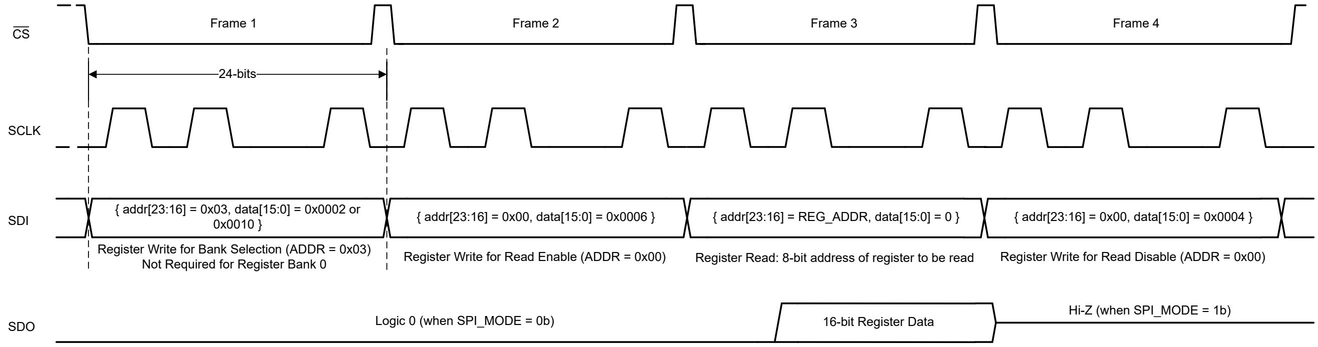


Figure 6-12. Register Read

6.5.3 Multiple Devices in a Daisy-Chain Topology for SPI Configuration

Figure 6-13 shows a typical connection diagram with multiple devices in a daisy-chain topology.

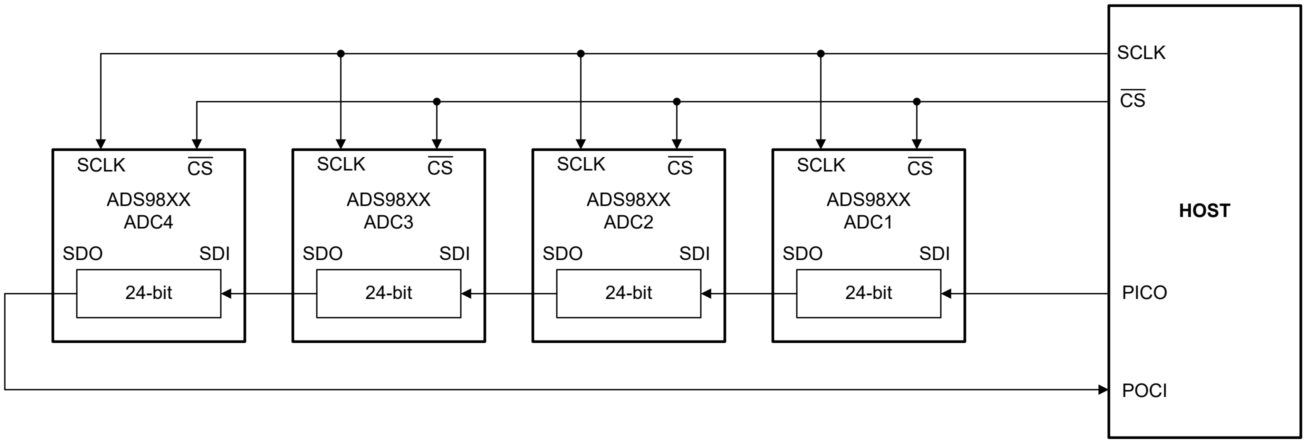


Figure 6-13. Daisy-Chain Connections for Configuration SPI

The $\overline{\text{CS}}$ and SCLK inputs of all ADCs are connected together and controlled by a single $\overline{\text{CS}}$ and SCLK pin of the controller, respectively. The SDI input pin of the first ADC in the chain (ADC1) is connected to the peripheral IN controller OUT (PICO) pin of the controller. Then, the SDO output pin of ADC1 is connected to the SDI input pin of ADC2, and so on. The SDO output pin of the last ADC in the chain (ADC4) is connected to the peripheral OUT controller IN (POCI) pin of the controller. The data on the PICO pin passes through ADC1 with a 24-SCLK delay, as long as $\overline{\text{CS}}$ is active.

Enable daisy-chain after power-up or after the device is reset. Set the daisy-chain length in the DAISY_CHAIN_LEN register to enable daisy-chain mode. The daisy-chain length is the number of ADCs in the chain excluding ADC1. In Figure 6-13, the DAISY_CHAIN_LEN is 3.

6.5.3.1 Register Write With Daisy-Chain

Writing to registers in daisy-chain requires N × 24 SCLKs in one SPI frame. As depicted in Figure 6-13, a register write operation in a daisy-chain containing four ADCs requires 96 SCLKs.

Daisy-chain mode is enabled on power-up or after device reset. Configure the DAISY_CHAIN_LEN field to enable daisy-chain mode. Repeat the waveform shown in Figure 6-14 N times, where N is the number of ADCs in daisy-chain. Figure 6-15 provides the SPI waveform, containing N SPI frames, for enabling daisy-chain mode for N ADCs.

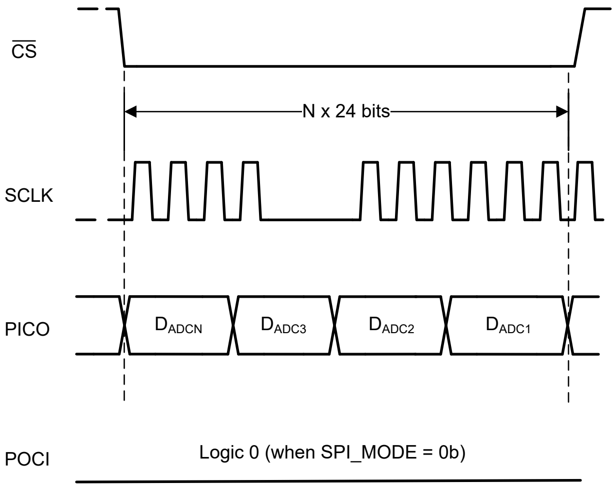


Figure 6-14. Register Write With Daisy-Chain

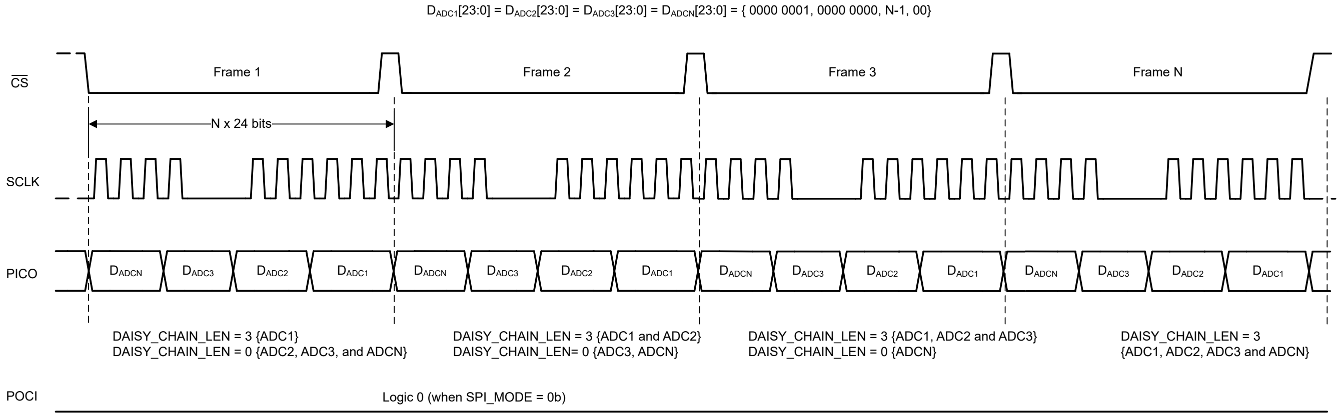


Figure 6-15. Register Write to Configure the Daisy-Chain Length

6.5.3.2 Register Read With Daisy-Chain

Figure 6-16 depicts an SPI waveform for reading registers in daisy-chain. Steps for reading registers from N ADCs connected in daisy-chain are:

1. A register read is enabled by writing to the following registers using the *register write with daisy-chain operation*:
   a. Write to REG_BANK_SEL to select the desired register bank
   b. Enable register reads by writing SPI_RD_EN = 0b (default on power-up)
2. With the register bank selected and SPI_RD_EN = 0b, the controller reads register data in the following two steps:
   a. The N × 24-bit SPI frame containing the 8-bit register address is read: N-times {0xFE, 0x00, 8-bit register address}
   b. The N × 24-bit SPI frame to read out register data is read: N-times {0xFF, 0xFF, 0xFF}

The 0xFE in step 2a configures the ADC for register reads from the specified 8-bit address. At the end of step 2a, the output shift register in the ADC is loaded with register data. The ADC returns the 8-bit register address and corresponding 16-bit register data in step 2b.

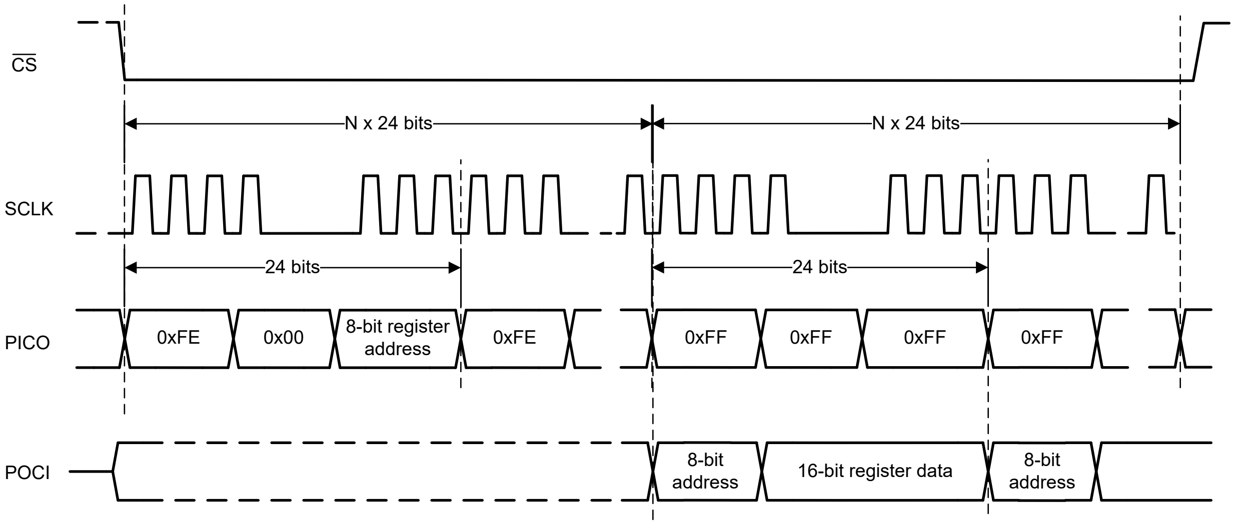


Figure 6-16. Register Read With Daisy-Chain

7 Register Map

7.1 Register Bank 0

Figure 7-1. Register Bank 0 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	RESERVED													SPI_MODE	SPI_RD_EN	RESET
01h	RESERVED									DAISY_CHAIN_LEN					RESERVED	
03h	RESERVED								REG_BANK_SEL							
04h	RESERVED												INIT_1			
06h	REG_00H_READBACK															

Table 7-1. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 Register 00h (offset = 0h) [reset = 0h]

Figure 7-2. Register 00h

15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					SPI_MODE	SPI_RD_EN	RESET
W-0h					W-0h	W-0h	W-0h

Figure 7-3. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	W	0h	Reserved. Do not change from the default reset value.
2	SPI_MODE	W	0h	Select between legacy SPI mode and daisy-chain SPI mode for the configuration interface for register access. 0 : Daisy-chain SPI mode 1 : Legacy SPI mode
1	SPI_RD_EN	W	0h	Enable register read access in legacy SPI mode. This bit has no effect in daisy-chain SPI mode. 0 : Register read disabled 1 : Register read enabled
0	RESET	W	0h	ADC reset control. 0 : Normal device operation 1 : Reset ADC and all registers

7.1.2 Register 01h (offset = 1h) [reset = 0h]

Figure 7-4. Register 01h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DAISY_CHAIN_LEN					RESERVED	
R/W-0h	R/W-0h					R/W-0h	

Figure 7-5. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6-2	DAISY_CHAIN_LEN	R/W	0h	Number of ADCs connected in SPI daisy-chain 0 : 1 ADC 1 : 2 ADCs 31 : 32 ADCs
1-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.1.3 Register 03h (offset = 3h) [reset = 2h]

Figure 7-6. Register 03h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REG_BANK_SEL							
R/W-2h							

Figure 7-7. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-0	REG_BANK_SEL	R/W	2h	Register bank selection for read and write operations. 0 : Select register bank 0 2 : Select register bank 1 16 : Select register bank 2

7.1.4 Register 04h (offset = 4h) [reset = 0h]

Figure 7-8. Register 04h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				INIT_1			
R/W-0h				R/W-0h			

Figure 7-9. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
3-0	INIT_1	R/W	0h	Set to 0011b for normal operation. Refer to section on *Initialization Sequence* for more details.

7.1.5 Register 06h (offset = 6h) [reset = 2h]

Figure 7-10. Register 06h

15	14	13	12	11	10	9	8
REG_00H_READBACK							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REG_00H_READBACK							
R-5h							

Figure 7-11. Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	REG_00H_READBACK	R	2h	This register is a copy of the register address 0x00 for readback.

7.2 Register Bank 1

Figure 7-12. Register Bank 1 Map

<table>
<tr><th>ADD</th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Dh</td><td colspan="2">RESERVED</td><td>DATA_FORMAT</td><td colspan="6">RESERVED</td><td>EN_AVG</td><td colspan="5">RESERVED</td><td>EN_MVG_AVG</td></tr>
<tr><td>12h</td><td colspan="11">RESERVED</td><td>XOR_PRBS</td><td>XOR_EN</td><td colspan="3">RESERVED</td></tr>
<tr><td>13h</td><td colspan="8">RESERVED</td><td colspan="4">RAMP_INC_A</td><td colspan="2">TP_MODE_A</td><td>TP_EN_A</td><td>RESERVED</td></tr>
<tr><td>14h</td><td colspan="16">TP0_A</td></tr>
<tr><td>15h</td><td colspan="8">TP1_A</td><td colspan="8">TP0_A</td></tr>
<tr><td>16h</td><td colspan="16">TP1_A</td></tr>
<tr><td>18h</td><td colspan="8">RESERVED</td><td colspan="4">RAMP_INC_B</td><td colspan="2">TP_MODE_B</td><td>TP_EN_B</td><td>RESERVED</td></tr>
<tr><td>19h</td><td colspan="16">TP0_B</td></tr>
<tr><td>1Ah</td><td colspan="8">TP1_B</td><td colspan="8">TP0_B</td></tr>
<tr><td>1Bh</td><td colspan="16">TP1_B</td></tr>
<tr><td>1Ch</td><td colspan="2">RESERVED</td><td colspan="6">USER_BITS_CH[8:5]</td><td colspan="2">RESERVED</td><td colspan="6">USER_BITS_CH[4:1]</td></tr>
<tr><td>37h</td><td colspan="13">RESERVED</td><td colspan="2">BOOST_CH_SEL</td><td>EN_BOOST</td></tr>
<tr><td>3Ch</td><td colspan="8">RESERVED</td><td>AVG_CFG3</td><td colspan="7">RESERVED</td></tr>
<tr><td>92h</td><td colspan="14">RESERVED</td><td>INIT_2</td><td>RESERVED</td></tr>
<tr><td>C0h</td><td colspan="6">RESERVED</td><td colspan="8">ANA_BW</td><td colspan="2">PD_CH</td></tr>
<tr><td>C1h</td><td colspan="4">RESERVED</td><td>PD_REF</td><td>RESERVED</td><td>DATA_LANES</td><td>DATA_RATE</td><td colspan="8">RESERVED</td></tr>
<tr><td>C2h</td><td colspan="4">RANGE_CH4</td><td colspan="4">RANGE_CH3</td><td colspan="4">RANGE_CH2</td><td colspan="4">RANGE_CH1</td></tr>
<tr><td>C3h</td><td colspan="4">RANGE_CH8</td><td colspan="4">RANGE_CH7</td><td colspan="4">RANGE_CH6</td><td colspan="4">RANGE_CH5</td></tr>
<tr><td>C4h</td><td colspan="6">RESERVED</td><td colspan="2">CM_RNG_CH[8:5]</td><td colspan="2">CM_RNG_CH[4:1]</td><td colspan="2">AVG_CFG2</td><td>CM_EN_CH[8:5]</td><td>CM_EN_CH[4:1]</td><td>AVG_CFG1</td><td>PD_CHIP</td></tr>
<tr><td>C5h</td><td colspan="2">BOOST_CFG1</td><td colspan="3">RESERVED</td><td>INIT_3</td><td>PGA_IN1T2</td><td colspan="2">RESERVED</td><td colspan="2">AVG_CFG4</td><td>CM_CTRL_EN</td><td>BOOST_CFG2</td><td>PGA_IN1T1</td><td colspan="2">RESERVED</td></tr>
</table>

Table 7-2. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-*n*		Value after reset or the default value

7.2.1 Register 0Dh (offset = Dh) [reset = 2002h]

Figure 7-13. Register 0Dh

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td>DATA_FORMAT</td><td colspan="5">RESERVED</td></tr>
<tr><td colspan="2">R/W-0h</td><td>R/W-1h</td><td colspan="5">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>EN_AVG</td><td colspan="5">RESERVED</td><td>EN_MVG_AVG</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td colspan="5">R/W-1h</td><td>R/W-0h</td></tr>
</table>

Figure 7-14. Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13	DATA_FORMAT	R/W	1h	Select data format for the ADC conversion result. 0 : Straight binary format 1 : Two's-complement format
12-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6	EN_AVG	R/W	0h	Set 1b to enable data averaging. See Table 6-10 and Table 6-11 for more details.
5-1	RESERVED	R/W	1h	Reserved. Do not change from the default reset value.
0	EN_MVG_AVG	R/W	0h	Set 1b to enable moving data average. See Table 6-11 for more details.

Register 12h (offset = 12h) [reset = 2h]

Figure 7-15. Register 12h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>XOR_PRBS</td><td>XOR_EN</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="3">R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td colspan="3">R/W-2h</td></tr>
</table>

Figure 7-16. Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
4	XOR_PRBS	R/W	0h	Select bit for XOR operation when XOR_EN = 1b. 0 : PRBS is appended after the LSB of the ADC conversion result. The ADC conversion result is bit-wise XOR with the PRBS bit. 1 : The ADC conversion result is bit-wise XOR with the LSB of the ADC conversion result.
3	XOR_EN	R/W	0h	Enables XOR operation on the ADC conversion result. 0 : XOR operation is disabled 1 : Bit-wise XOR operation on ADC conversion result is enabled
2-0	RESERVED	R/W	2h	Reserved. Do not change from the default reset value.

7.2.2 Register 13h (offset = 13h) [reset = 0h]

Figure 7-17. Register 13h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RAMP_INC_A</td><td colspan="2">TP_MODE_A</td><td>TP_EN_A</td><td>RESERVED</td></tr>
<tr><td colspan="4">R/W-0h</td><td colspan="2">R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

Figure 7-18. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-4	RAMP_INC_A	R/W	0h	Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register.
3-2	TP_MODE_A	R/W	0h	Select digital test pattern for analog input channels 1, 2, 3, and 4. 0 : Fixed pattern from the TP0_A register 1 : Fixed pattern from the TP0_A register 2 : Digital ramp output 3 : Alternate fixed pattern output from the TP0_A and TP1_A registers
1	TP_EN_A	R/W	0h	Enable digital test pattern for data corresponding to channels 1, 2, 3, and 4. 0 : Data output is the ADC conversion result 1 : Data output is the digital test pattern for channels 1, 2, 3, and 4
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.3 Register 14h (offset = 14h) [reset = 0h]

Figure 7-19. Register 14h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TP0_A[15:0]</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TP0_A[15:0]</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

Figure 7-20. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TP0_A[15:0]	R/W	0h	Lower 16 bits of test pattern 0

7.2.4 Register 15h (offset = 15h) [reset = 0h]

Figure 7-21. Register 15h

15	14	13	12	11	10	9	8
TP1_A[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TP0_A[23:16]							
R/W-0h							

Figure 7-22. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TP1_A[7:0]	R/W	0h	Lower eight bits of test pattern 1
7-0	TP0_A[23:16]	R/W	0h	Upper eight bits of test pattern 0

7.2.5 Register 16h (offset = 16h) [reset = 0h]

Figure 7-23. Register 16h

15	14	13	12	11	10	9	8
TP1_A[23:8]							
R/W-0h							
7	6	5	4	3	2	1	0
TP1_A[23:8]							
R/W-0h							

Figure 7-24. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TP1_A[23:8]	R/W	0h	Upper 16 bits of test pattern 1

7.2.6 Register 18h (offset = 18h) [reset = 0h]

Figure 7-25. Register 18h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMP_INC_B				TP_MODE_B		TP_EN_B	RESERVED
R/W-0h				R/W-0h		R/W-0h	R/W-0h

Figure 7-26. Register 18h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-4	RAMP_INC_B	R/W	0h	Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register.
3-2	TP_MODE_B	R/W	0h	Select digital test pattern for analog input channels 5, 6, 7, and 8. 0 : Fixed pattern from the TP0_B register 1 : Fixed pattern from the TP0_B register 2 : Digital ramp output 3 : Alternate fixed pattern output from the TP0_B and TP1_B registers
1	TP_EN_B	R/W	0h	Enable digital test pattern for data corresponding to channels 5, 6, 7, and 8. 0 : Data output is the ADC conversion result 1 : Data output is the digital test pattern
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.7 Register 19h (offset = 19h) [reset = 0h]

Figure 7-27. Register 19h

15	14	13	12	11	10	9	8
TP0_B[15:0]							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TP0_B[15:0]							
R/W-0h							

Figure 7-28. Register 19h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TP0_B[15:0]	R/W	0h	Lower 16 bits of test pattern 0

7.2.8 Register 1Ah (offset = 1Ah) [reset = 0h]

Figure 7-29. Register 1Ah

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TP1_B[7:0]</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TP0_B[23:16]</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

Figure 7-30. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TP1_B[7:0]	R/W	0h	Lower eight bits of test pattern 1
7-0	TP0_B[23:16]	R/W	0h	Upper eight bits of test pattern 0

7.2.9 Register 1Bh (offset = 1Bh) [reset = 0h]

Figure 7-31. Register 1Bh

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TP1_B[23:8]</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TP1_B[23:8]</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

Figure 7-32. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TP1_B[23:8]	R/W	0h	Upper 16 bits of test pattern 1

Register 1Ch (offset = 1Ch) [reset = 0h]

Figure 7-33. Register 1Ch

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">USER_BITS_CH[8:5]</td></tr>
<tr><td colspan="2">R/W-0h</td><td colspan="6">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">USER_BITS_CH[4:1]</td></tr>
<tr><td colspan="2">R/W-0h</td><td colspan="6">R/W-0h</td></tr>
</table>

Figure 7-34. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13-8	USER_BITS_CH[8:5]	R/W	0h	User-defined bits appended to the ADC conversion result from channels 5, 6, 7, and 8.
7-6	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
5-0	USER_BITS_CH[4:1]	R/W	0h	User-defined bits appended to the ADC conversion result from channels 1, 2, 3, and 4.

7.2.10 Register 37h (offset = 37h) [reset = 0h]

Figure 7-35. Register 37h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					BOOST_CH_SEL		EN_BOOST
R/W-0h					R/W-0h		R/W-0h

Figure 7-36. Register 37h Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
2-1	BOOST_CH_SEL	R/W	0h	Select analog input channel pair for speed-boost mode. 0: CH1 and CH8 1: CH2 and CH7 2: CH3 and CH6 3: CH4 and CH5
0	EN_BOOST	R/W	0h	Enable speed-boost mode. See section on *Speed-Boost Mode* for more details.

7.2.11 Register 3Ch (offset = 3Ch) [reset = 0h]

Figure 7-37. Register 3Ch

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AVG_CFG3	RESERVED						
R/W-0h	R/W-0h						

Figure 7-38. Register 3Ch Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7	AVG_CFG3	R/W	0h	Configuration for simple averaging. See Table 6-10 for more details.
6-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.12 Register 92h (offset = 92h) [reset = 0h]

Figure 7-39. Register 92h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						INIT_2	RESERVED
R/W-0h						R/W-0h	R/W-0h

Figure 7-40. Register 92h Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1	INIT_2	R/W	0h	Set to 1b for normal operation. Refer to section on *Initialization Sequence* for more details.
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.13 Register C0h (offset = C0h) [reset = 0h]

Figure 7-41. Register C0h

15	14	13	12	11	10	9	8
RESERVED						ANA_BW	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
ANA_BW						PD_CH	
R/W-0h						R/W-0h	

Figure 7-42. Register C0h Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9-2	ANA_BW	R/W	0h	Select analog input bandwidth for the respective analog input channels. MSB = BW control for channel 8 LSB = BW control for channel 1 0 : Low-noise mode 1 : Wide-bandwidth mode
1-0	PD_CH	R/W	0h	Power-down control for the analog input channels. 0 : Normal operation 1 : Channels 5, 6, 7, and 8 powered down 2 : Channels 1, 2, 3, and 4 powered down 3 : All channels powered down

7.2.14 Register C1h (offset = C1h) [reset = 0h]

Figure 7-43. Register C1h

15	14	13	12	11	10	9	8
RESERVED				PD_REF	RESERVED	DATA_LANES	DATA_RATE
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

Figure 7-44. Register C1h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
11	PD_REF	R/W	0h	ADC reference voltage source selection. 0 : Internal reference enabled. 1 : Internal reference disabled. Connect the external reference voltage to the REFIO pin.
10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9	DATA_LANES	R/W	0h	Select number of output data lanes per ADC channel. 0 : 4-lane mode. CH[4:1] data are output on pins D3 and D2. CH[8:5] data are output on pins D1 and D0. 1 : 2-lane mode. CH[4:1] data are output on pin D3. CH[8:5] data are output on pin D1.
8	DATA_RATE	R/W	0h	Select data rate for the data interface. 0 : Double data rate (DDR) 1 : Single data rate (SDR)
7-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.15 Register C2h (offset = C2h) [reset = 0h]

Figure 7-45. Register C2h

15	14	13	12	11	10	9	8
RANGE_CH4				RANGE_CH3			
R/W-0h				R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RANGE_CH2				RANGE_CH1			
R/W-0h				R/W-0h			

Figure 7-46. Register C2h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RANGE_CH4	R/W	0h	Select the analog input voltage range. 0 : ±5V 1 : ±3.5V 2 : ±2.5V 3 : ±7V 4 : ±10V 5 : ±12V
11-8	RANGE_CH3	R/W	0h	
7-4	RANGE_CH2	R/W	0h	
3-0	RANGE_CH1	R/W	0h	

7.2.16 Register C3h (offset = C3h) [reset = 0h]

Figure 7-47. Register C3h

15	14	13	12	11	10	9	8
RANGE_CH8				RANGE_CH7			
R/W-0h				R/W-0h			

7	6	5	4	3	2	1	0
RANGE_CH6				RANGE_CH5			
R/W-0h				R/W-0h			

Figure 7-48. Register C3h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RANGE_CH8	R/W	0h	Select the analog input voltage range. 0 : ±5V 1 : ±3.5V 2 : ±2.5V 3 : ±7V 4 : ±10V 5 : ±12V
11-8	RANGE_CH7	R/W	0h	
7-4	RANGE_CH6	R/W	0h	
3-0	RANGE_CH5	R/W	0h	

Register C4h (offset = C4h) [reset = 0h]

Figure 7-49. Register C4h

15	14	13	12	11	10	9	8
RESERVED						CM_RNG_CH[8:5]	
R/W-0h						R/W-0h	

7	6	5	4	3	2	1	0
CM_RNG_CH[4:1]		AVG_CFG2		CM_EN_ CH[8:5]	CM_EN_ CH[4:1]	AVG_CFG1	PD_CHIP
R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

Figure 7-50. Register C4h Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9-8	CM_RNG_CH[8:5]	R/W	0h	CM_RNG_CH[4:1] sets the common-mode range for channels 1, 2, 3, and 4. CM_RNG_CH[8:5] sets the common-mode range for channels 5, 6, 7, and 8. 0 : CM range is equal to ±RANGE / 2 1 : CM range is equal to ±6V 2 : CM range is equal to ±12V
7-6	CM_RNG_CH[4:1]	R/W	0h	
5-4	AVG_CFG2	R/W	0h	Configuration for simple averaging. See Table 6-10 for more details.
3	CM_EN_CH[8:5]	R/W	0h	CM_EN_CH[4:1] enables wide common-mode range control for channels 1 to 4. CM_EN_CH[8:5] enables the wide common-mode range control for channels 5 to 8. 0 : Wide common-mode range control disabled 1 : Wide common-mode range control enabled
2	CM_EN_CH[4:1]	R/W	0h	
1	AVG_CFG1	R/W	0h	Configuration for simple averaging. See Table 6-10 for more details.
0	PD_CHIP	R/W	0h	Full chip power-down control. 0 : Normal device operation 1 : Full device powered-down

7.2.17 Register C5h (offset = C5h) [reset = 0h]

Figure 7-51. Register C5h

15	14	13	12	11	10	9	8
BOOST_CFG1		RESERVED			INIT_3	PGA_INIT2	RESERVED
R/W-0h		R/W-0h			R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
RESERVED	AVG_CFG4		CM_CTRL_EN	BOOST_CFG2	PGA_INIT2	RESERVED	
R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Figure 7-52. Register C5h Field Descriptions

Bit	Field	Type	Reset	Description
15-14	BOOST_CFG1	R/W	0h	Configuration for speed-boost mode. See Table 6-15 for more details.
13-11	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
10	INIT_3	R/W	0h	Set to 1 for normal operation. Refer to *Initialization Sequence* for more details.
9	PGA_INIT2	R/W	0h	Conifguration for PGA initialization. Set to 1 for normal operation. Refer to *Initialization Sequence* for more details.
8-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6-5	AVG_CFG4	R/W	0h	Configuration for simple averaging. See Table 6-10 for more details.
4	CM_CTRL_EN	R/W	0h	Enable the wide common-mode range control for all analog input channels. 0 : CM range for all analog input channels is ±12V 1 : CM range is user-defined in the CM_EN_CH[4:1], CM_EN_CH[8:5], CM_RNG_CH[4:1], and CM_RNG_CH[8:5] registers
3	BOOST_CFG2	R/W	0h	Configuration for speed-boost mode. See Table 6-15 for more details.
2	PGA_INIT1	R/W	0h	Conifguration for PGA initialization. Set to 1 for normal operation. Refer to *Initialization Sequence* for more details.
1-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.3 Register Bank 2

Figure 7-53. Register Bank 2 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
25h	RESERVED				BOOST_CFG4	RESERVED	BOOST_CFG3	RESERVED								

Table 7-3. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

7.3.1 Register 25h (offset = 25h) [reset = 0h]

Figure 7-54. Register 25h

15	14	13	12	11	10	9	8
RESERVED				BOOST_CFG4	RESERVED	BOOST_CFG3	RESERVED
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Figure 7-55. Register 25h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
11	BOOST_CFG4	R/W	0h	Configuration for speed-boost mode. See Table 6-15 for more details.
10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9	BOOST_CFG3	R/W	0h	Configuration for speed-boost mode. See Table 6-15 for more details.
8-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ADS9813 enables high-precision measurement of up to eight analog signals. The following section gives an example application circuit and recommendations for using the ADS9813 in automated test equipment (ATE) systems.

8.2 Typical Application

8.2.1 Parametric Measurement Unit (PMU)

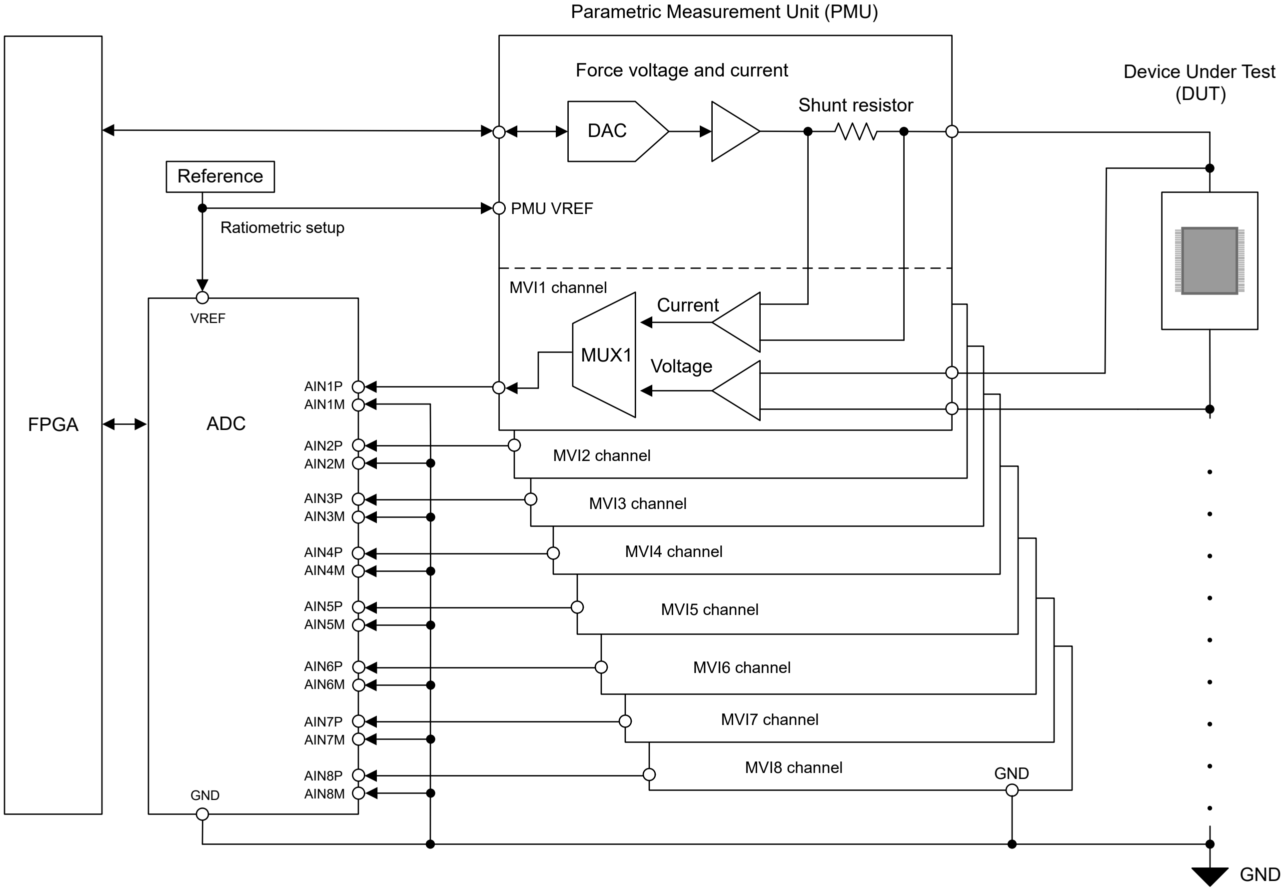


Figure 8-1. Typical PMU

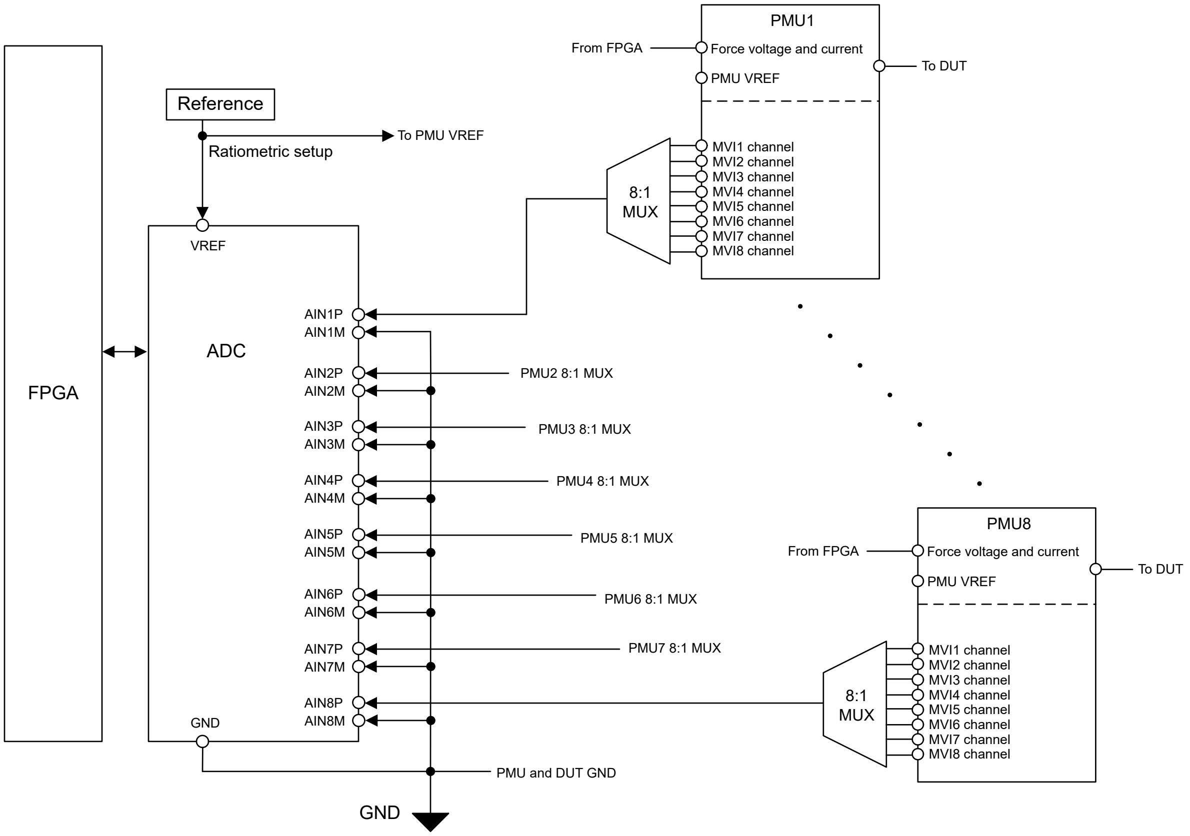


Figure 8-2. PMU With a Multiplexer

8.2.2 Design Requirements

The goal of this application is to select an ADC for ATE applications. Table 8-1 shows the parameters for this design example.

Table 8-1. Design Parameters

PARAMETER	VALUE
Sampling rate	Up to 2MSPS/channel
Total unadjusted error (TUE) over 25°C ±5°C	<0.01% with calibration
Supports external switches or multiplexer	Full-scale step settling to 99.95% of full-scale in <10μs

8.2.3 Detailed Design Procedure

The ADS9813 is an eight-channel, 18-bit, 2MSPS data acquisition (DAQ) system. The device has a built-in analog front-end that makes the ATE signal chain easier to design and more accurate.

The ADC accuracy is based on the total-unadjusted-error (TUE), which combines INL, offset, and gain errors. Calibrate the external system for offset and gain errors at a specified temperature and supply voltage. When calibrated (as described in Table 8-2), only the INL, thermal offset drifts, and gain contribute to TUE. The ADS9813 has a TUE of 0.0015% at 25°C ±5°C post-calibration, meeting the design error requirement.

Table 8-2. TUE at T_A = 25°C Calculation for RANGE = ±5V

CALIBRATION	INL (ppm)	OFFSET ERROR (ppm)	GAIN ERROR (ppm)	TUE (ppm)	ERROR (%)
No calibration	±3.2	±60	±80	±100.05	±0.0100
Post-calibration	±3.2	0	0	±3.2	±0.0003
Post-calibration ±5°C	±3.2	±7.5	±12.5	±14.92	±0.0015

The pin-electronics subsystem manages the PMU outputs. The subsystem connects each PMU output to separate ADC channels (Figure 8-1) or uses a multiplexer to link multiple PMU outputs to one ADC channel (Figure 8-2). This subsystem allows more pin-electronics channels on the card. The ADC requires more bandwidth with multiplexers (Table 8-3) for fast settling when switching PMU channels. The ADS9813 has two bandwidth modes: Low-noise (up to 22.7kHz) and wide-bandwidth (up to 700kHz). As described in Figure 8-3 the wide-bandwidth mode samples multiplexed PMU signals and settles to 99.95% FS in 7.5µs.

Table 8-3. Step-Settling Performance for RANGE = ±5V

ANALOG INPUT BANDWIDTH	SETTLING TIME (99.95% of FS)	SNR (Typical)
Low BW (22.7kHz)	55µs	89.1dB
Wide BW (500kHz)	7.5µs	79.7dB

8.2.4 Application Curve

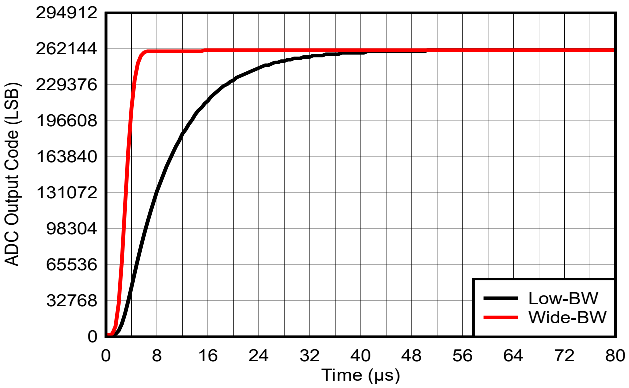


Figure 8-3. Step-Settling Performance

8.3 Power Supply Recommendations

The ADS9813 has three separate power supplies: AVDD_5V, VDD_1V8, and IOVDD. There is no requirement for a specific power-up sequence. The data and configuration digital interfaces are powered by IOVDD. A common 1.8V supply powers the VDD_1V8 and IOVDD pins. Figure 8-4 illustrates the decoupling capacitor connections for the respective power supplies. Make sure each power-supply pin has separate decoupling capacitors.

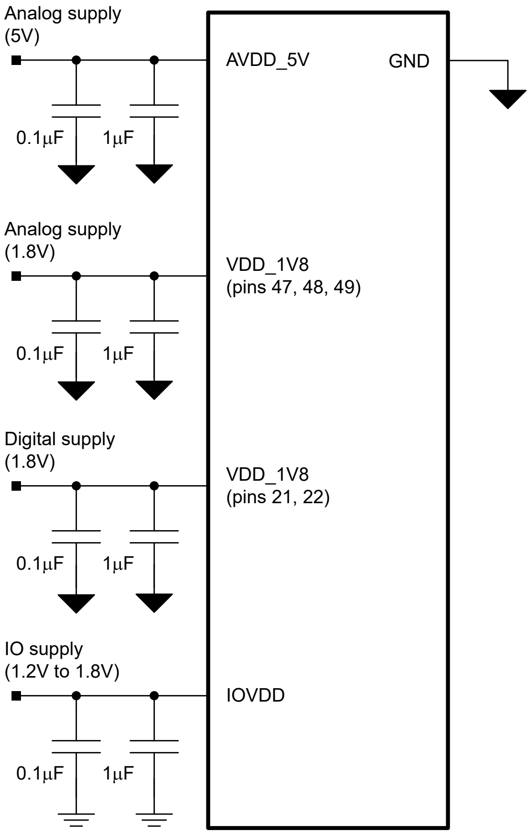


Figure 8-4. Power-Supply Decoupling

8.4 Layout

8.4.1 Layout Guidelines

Figure 8-5 illustrates a board layout example for the ADS9813. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources.

Use 0.1µF ceramic bypass capacitors in close proximity to the AVDD_5V, VDD_1V8, and IOVDD power-supply pins. Avoid placing vias between the power-supply pins and the bypass capacitors.

Place the reference decoupling capacitor close to the device REFIO and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND and REFM pins to a ground plane using short, low-impedance paths.

8.4.2 Layout Example

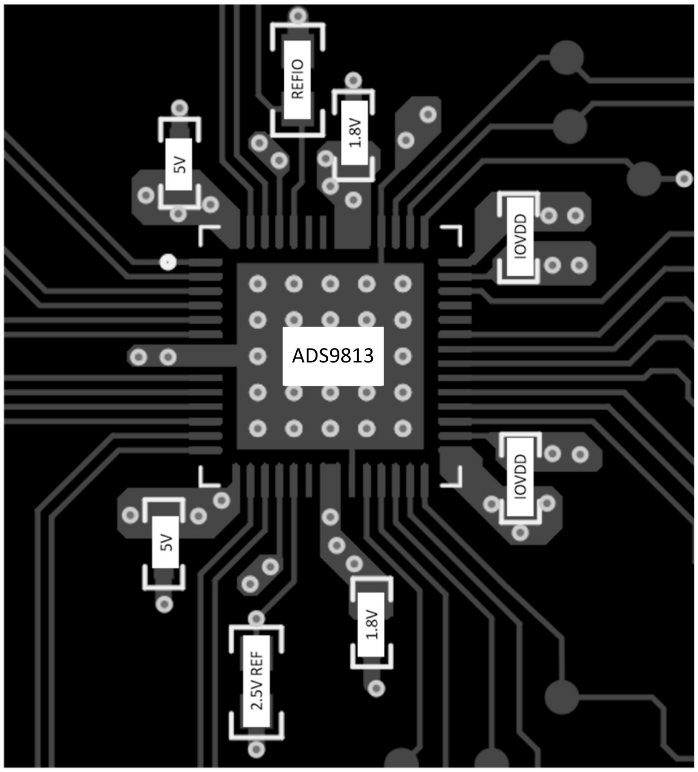


Figure 8-5. Example Layout

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2024) to Revision A (November 2024)	Page
• Changed the document from Advanced information to *Production* data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS9810RSHR	Active	Production	VQFN (RSH) | 56	4000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9810
ADS9810RSHR.A	Active	Production	VQFN (RSH) | 56	4000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9810
ADS9811RSHR	Active	Production	VQFN (RSH) | 56	4000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9811
ADS9811RSHR.A	Active	Production	VQFN (RSH) | 56	4000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9811
ADS9813RSHR	Active	Production	VQFN (RSH) | 56	4000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9813
ADS9813RSHR.A	Active	Production	VQFN (RSH) | 56	4000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9813

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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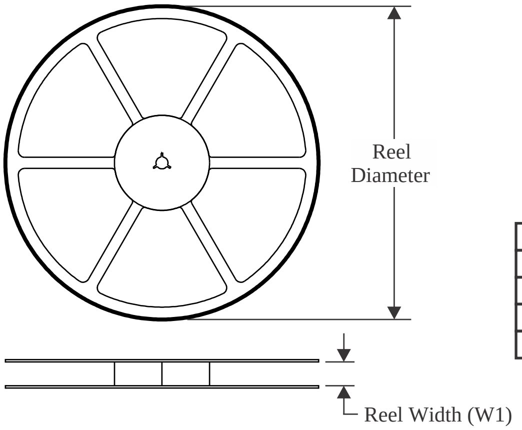
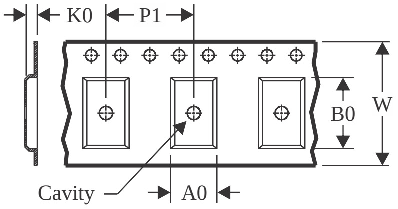
TAPE AND REEL INFORMATION

REEL DIMENSIONS

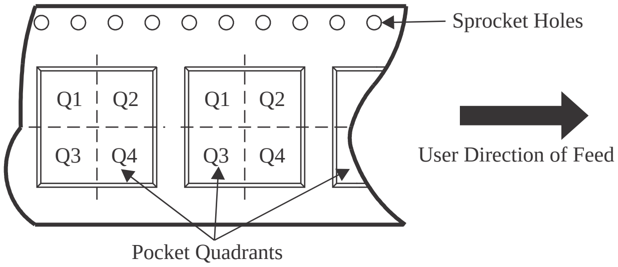


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

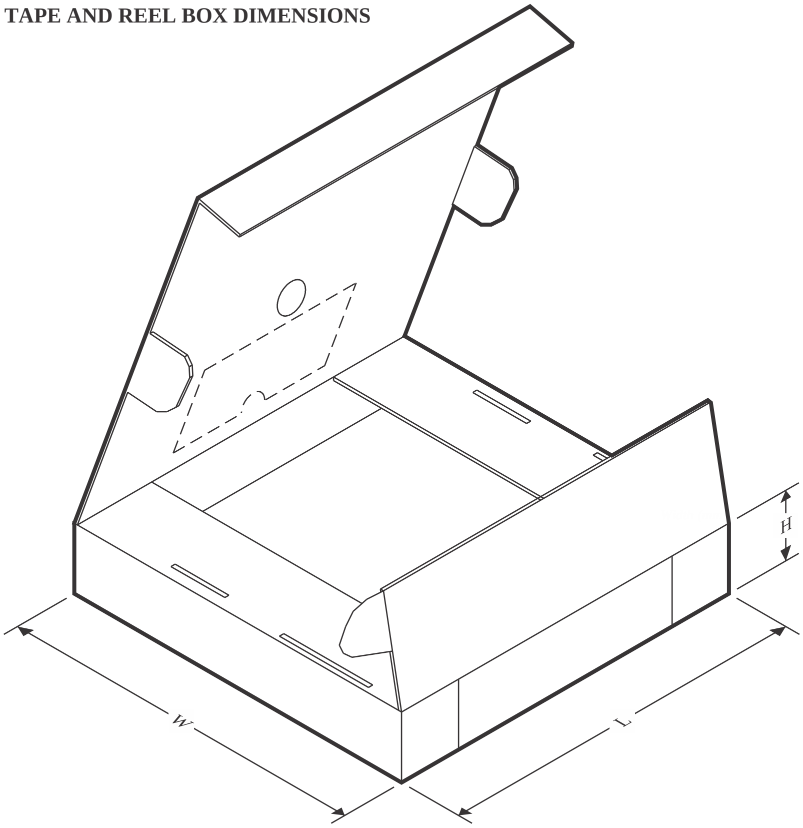
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS9810RSHR	VQFN	RSH	56	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
ADS9811RSHR	VQFN	RSH	56	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
ADS9813RSHR	VQFN	RSH	56	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

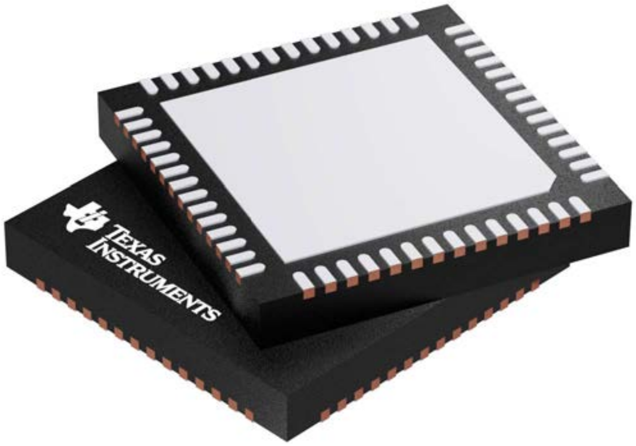
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS9810RSHR	VQFN	RSH	56	4000	367.0	367.0	35.0
ADS9811RSHR	VQFN	RSH	56	4000	367.0	367.0	35.0
ADS9813RSHR	VQFN	RSH	56	4000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RSH 56

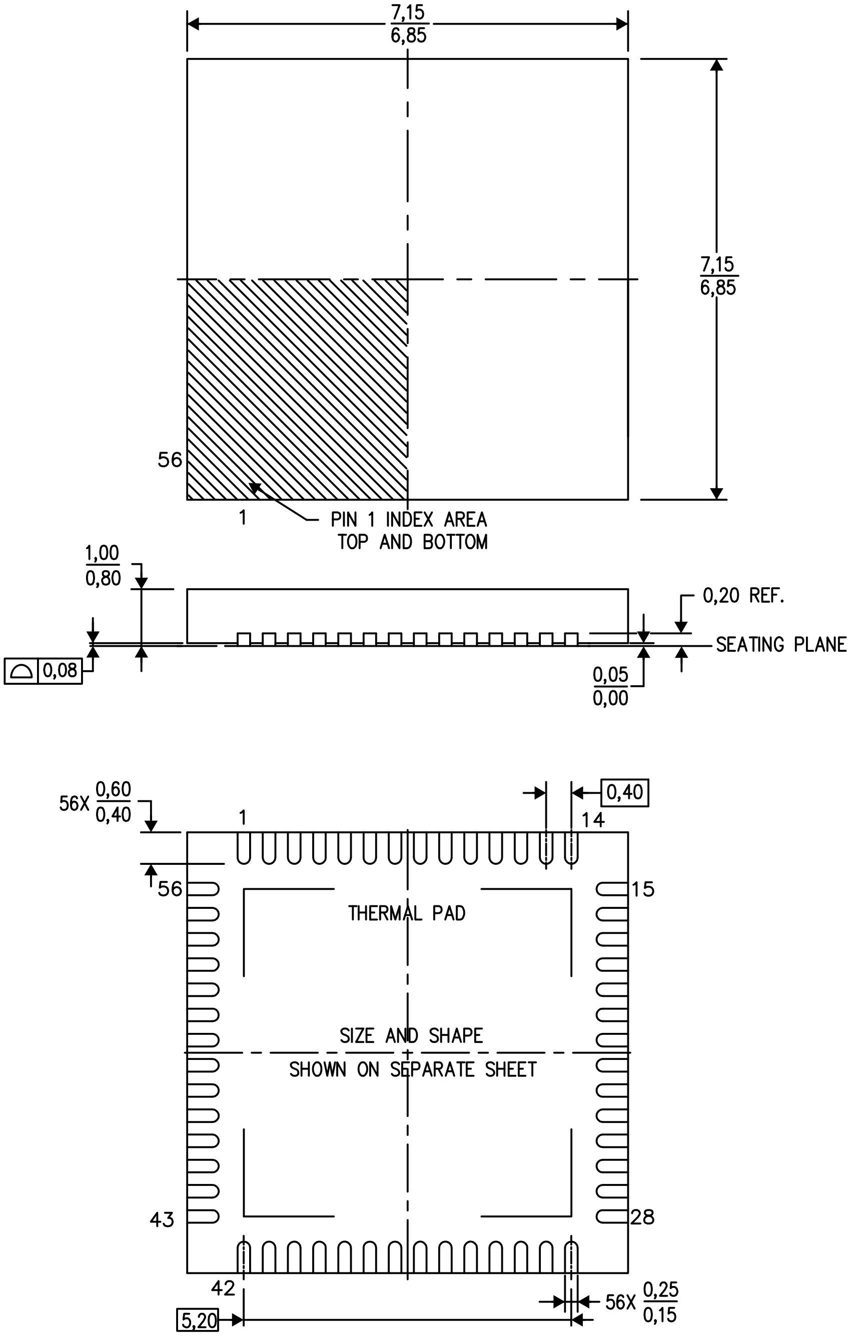
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



4207513/C 03/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

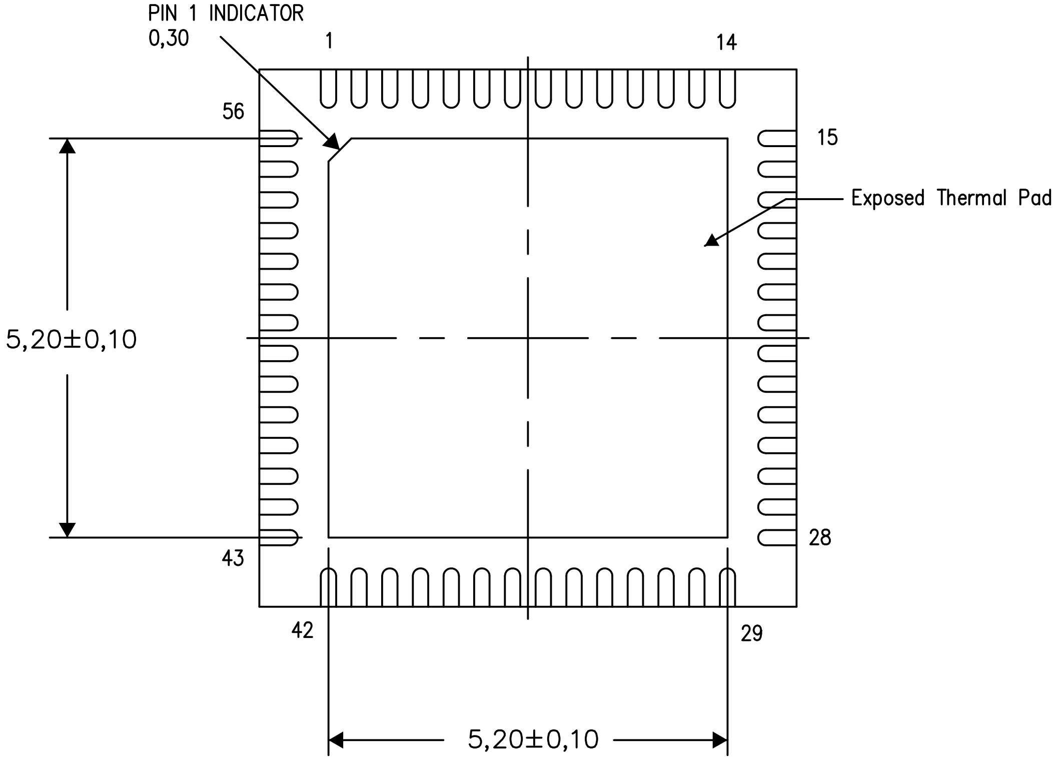
RSH (S-PVQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



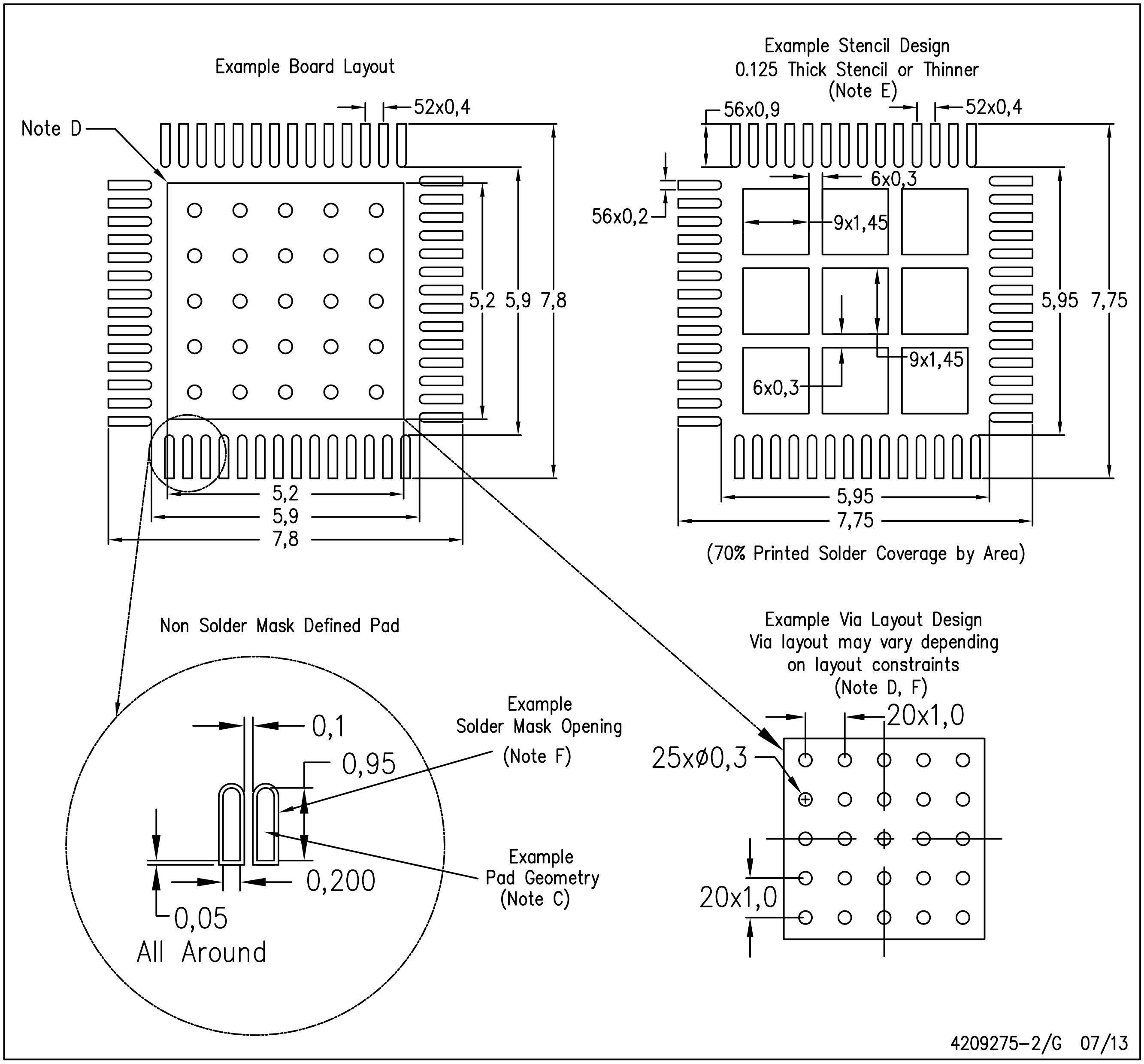
Bottom View

Exposed Thermal Pad Dimensions

4207553-2/I 07/13

NOTE: All linear dimensions are in millimeters

RSH (S-PVQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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