

ADS932x Dual, Simultaneous-Sampling, Small-Size, 16-Bit, 5MSPS SAR ADC

1 Features

- 16-bit SAR ADC family
 - ADS9327: 5MSPS/ch
 - ADS9326: 3MSPS/ch
- Two fully differential, simultaneously sampled channels
- Supports 5V and 3.3V analog supply operation
- Excellent DC and AC performance:
 - SNR: 93dB at 5MSPS
 - INL: $\pm 1\text{LSB}$, DNL: $\pm 0.75\text{LSB}$
- Feature integration:
 - Internal reference
 - Integrated buffer for external reference input
 - Simple data average up to 128 samples
- Configurable serial interface:
 - 2 serial outputs for each ADC channel
 - 1 serial output for each ADC channel
 - 1 serial output for both ADC channels
 - Supports daisy-chain functionality
- 8-bit CRC on serial interface
- Extended temperature range: -40°C to $+125^{\circ}\text{C}$

2 Applications

- [Absolute optical encoders](#)
- [Absolute magnetic encoders](#)
- [Servo drive position feedback](#)
- [Ultrasound scanners](#)
- [Programmable DC power supplies, electronic loads](#)
- [SONAR](#)

3 Description

The ADS932x is a high-speed, dual, simultaneous-sampling, analog-to-digital converter (ADC) with an integrated reference and reference buffer. The ADS932x has excellent AC performance, which makes the device optimum for wide-bandwidth data acquisition (DAQ) systems.

The device supports an SPI-compatible serial interface. This interface makes the ADS932x easy to pair with a diversity of microcontrollers, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs). This device also supports a data averaging feature that provides an AC performance boost in noisy environments.

Package Information

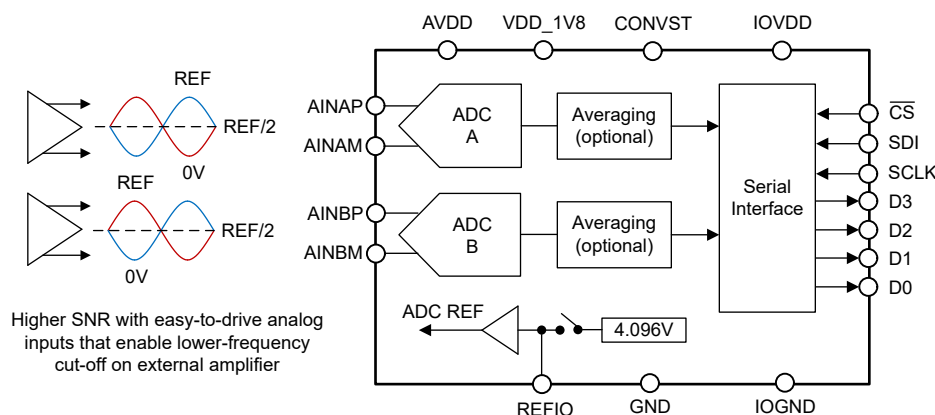
PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
ADS932x	VAE (VQFN, 22)	3.5mm × 3.5mm

(1) For more information, see the [Mechanical, Packaging, and Orderable Information](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

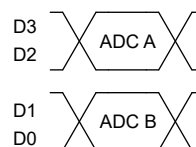
Device Information

PART NUMBER	RESOLUTION	SNR	INL
ADS932x	16 bits	93dB	$\pm 1\text{LSB}$

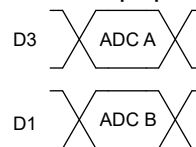


Device Block Diagram

2 serial outputs per ADC



1 serial output per ADC



1 serial output for both ADCs

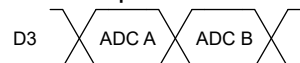


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4 Device Comparison

RESOLUTION (Bits)	5MSPS	3MSPS
18	ADS9317	ADS9316
16	ADS9327	ADS9326
14	ADS9337	ADS9336
12	ADS9347	ADS9346

5 Pin Configuration and Functions

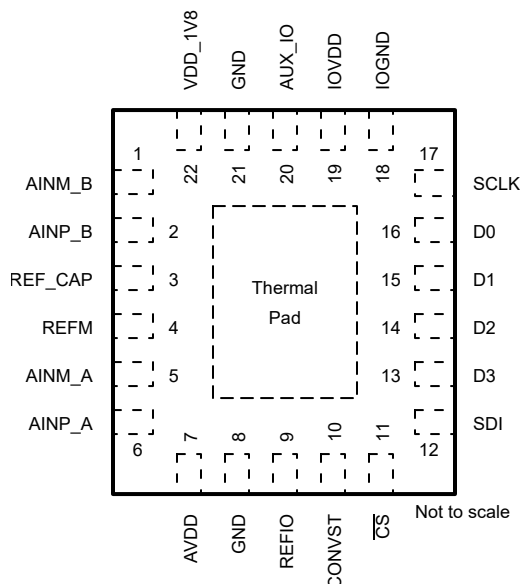


Figure 5-1. VAE Package, 22-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
AINM_A	5	I	Negative analog input for ADC A.
AINM_B	1	I	Negative analog input for ADC B.
AINP_A	6	I	Positive analog input for ADC A.
AINP_B	2	I	Positive analog input for ADC B.
AUX_IO	20	I/O	Auxiliary IO pin. Connect a 100nF capacitor to GND. Future function: REF_SEL/VCMOULT. REF_SEL selects the internal or external reference on power-up. Connect a 0Ω resistor to GND or IOVDD. VCMOULT sets the common-mode voltage output at the ADC inputs.
AVDD	7	P	5V or 3.3V analog power-supply pin. Connect a 1μF decoupling capacitor between pins 7 and 8.
CONVST	10	I	Conversion start input pin. A CONVST falling edge starts the conversion for ADC A and ADC B.
CS	11	I	Chip-select input pin; active low. The host and device communicate when CS is low. The data output pins go to Hi-Z when CS is high.
D0	16	O	Serial communication pin: data output 0.
D1	15	O	Serial communication pin: data output 1.
D2	14	O	Serial communication pin: data output 2.
D3	13	O	Serial communication pin: data output 3.
GND	8, 21	G	Ground.
IOGND	18	G	Ground for IOVDD supply. Connect to GND externally.
IOVDD	19	P	Interface power-supply pin. Connect a 0.1μF decoupling capacitor between pins 18 and 19.
REFIO	9	I/O	Internal reference output. External reference input. Connect a 1μF decoupling capacitor to GND.

Table 5-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
REF_CAP	3	O	Internal reference voltage output. Connect a 1µF decoupling capacitor between pins 3 and 4.
REFM	4	G	Negative reference input for the ADCs. Externally connect to the device GND.
SCLK	17	I	Clock input pin for the serial interface.
SDI	12	I	Serial data input pin. This pin programs the device registers.
VDD_1V8	22	P	1.8V analog power-supply pin. Connect a 1µF decoupling capacitor between pins 21 and 22.
Thermal Pad	Pad	P	Exposed thermal pad. Connect to GND.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
AVDD to GND	–0.3	5.5	V
VDD_1V8 to GND	–0.3	2.1	V
IOVDD to IOGND	–0.3	3.7	V
AINAP, AINAM, AINBP, and AINBM to GND	–0.3	AVDD + 0.3	V
REFIO to REFM	–0.3	AVDD + 0.3	V
Digital inputs to IOGND	–0.3	IOVDD + 0.3	V
REFM to GND	–0.3	0.3	V
IOGND to GND	–0.3	0.3	V
Input current to any pin except supply pins ⁽²⁾	–10	10	mA
Junction temperature, T _J	–40	150	°C
Storage temperature, T _{stg}	–60	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Limit pin current to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC ⁽¹⁾		ADS93x7	UNIT
		VAE (VQFN)	
		22 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	36.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	26.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	7.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	7.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	11.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog power supply	AVDD to GND, AVDD = 5V	4.75	5	5.25	V
		AVDD to GND, AVDD = 3.3V	3.1	3.3	3.5	
VDD_1V8	Power supply	VDD_1V8 to GND	1.75	1.8	1.85	V
IOVDD	Interface supply	IOVDD to IOGND	1.75		3.5	V
REFERENCE VOLTAGE						
V _{REF}	Reference voltage to the ADC	External reference, AVDD = 5V	4.076	4.096	4.116	V
		External reference, AVDD = 3.3V	2.48	2.5	2.52	
ANALOG INPUTS						
V _{IN}	Absolute input voltage	AINx ⁽¹⁾ to GND	0		AVDD	V
FSR	Full-scale input range	(A _{INP} _x – A _{INM} _x)	–V _{REF}		V _{REF}	V
V _{CM}	Common-mode input range	(A _{INP} _x + A _{INM} _x) / 2	0.46 x V _{REF}	0.5 x V _{REF}	0.63 x V _{REF}	V
TEMPERATURE RANGE						
T _A	Ambient temperature		–40	25	125	°C

(1) AINx refers to analog inputs AINAP, AINAM, AINBP, and AINBM.

6.5 Electrical Characteristics: AVDD = 5V

at AVDD = 4.75V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal $V_{REF} = 4.096V$, and maximum throughput (unless otherwise noted); minimum and maximum values at $T_A = -40^{\circ}C$ to $+125^{\circ}C$; typical values at $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
	Resolution	No missing codes		16		Bits
DNL	Differential nonlinearity		−0.75	±0.4	0.75	LSB
INL	Integral nonlinearity		−1	±0.6	1	LSB
$V_{(OS)}$	Input offset error		−1	±0.8	1	LSB
dV_{OS}/dT	Input offset error thermal drift			0.8		$\mu V/^{\circ}C$
	Offset error match	$V_{(OS)} (ADC_A - ADC_B)$		1		LSB
G_E	Gain error ⁽¹⁾		−0.005	±0.001	0.005	%FSR
dG_E/dT	Gain error thermal drift	Reference buffer on ⁽¹⁾		1		ppm/ $^{\circ}C$
		Reference buffer off ⁽²⁾		0.4		
	Gain error match	$G_E (ADC_A - ADC_B)$		±0.001		%FSR
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	$f_{IN} = 2kHz$	TBD	92.9		dB
		$f_{IN} = 1MHz$		91.5		
SNR	Signal-to-noise ratio	$f_{IN} = 2kHz$	TBD	93		dB
		$f_{IN} = 1MHz$		91.6		
THD	Total harmonic distortion	$f_{IN} = 2kHz$		−115		dB
		$f_{IN} = 1MHz$		−100		
SFDR	Spurious-free dynamic range	$f_{IN} = 2kHz$		115		dB
		$f_{IN} = 1MHz$		100		
CMRR	Common-mode rejection ratio	$f_{IN} = dc$ to 1kHz, $V_{IN} = 500mV_{PP}$		70		dB
	Channel-to-channel isolation	$f_{IN_ADCA} = 15kHz$ at 10% FSR, $f_{IN_ADCB} = 25kHz$ at 100% FSR		−110		dB
POWER SUPPLY						
I_{AVDD}	Supply current from AVDD	Full-speed (ADS9327)		3.7	4	mA
		Full-speed (ADS9326)		2.8	3.1	
		No conversion (idle) (ADS9327)		1.5	1.8	
		No conversion (idle) (ADS9326)		1.35	1.65	
		Power-down		0.6	0.9	
I_{VDD_1V8}	Supply current from VDD_1V8	Full-speed (ADS9327)		9.5	10.2	mA
		Full-speed (ADS9326)		6.9	7.4	
		No conversion (idle) (ADS9327)		6.4	7.2	
		No conversion (idle) (ADS9326)		4.9	5.5	
		Power-down		0.78	1	
I_{IOVDD}	Supply current from IOVDD	Full-speed (ADS9327)		2.6	2.9	mA
		Full-speed (ADS9326)		1.6	1.8	
		No conversion (idle)		0.25	0.35	
		Power-down		0.25	0.35	

(1) These specifications include full temperature range variation but not the error contribution from internal reference.

(2) For more details, see [External Reference with External Reference Buffer](#).

6.6 Electrical Characteristics: AVDD = 3.3V

at AVDD = 3.1V to 3.5V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal $V_{REF} = 2.5V$, and maximum throughput (unless otherwise noted); minimum and maximum values at $T_A = -40^{\circ}C$ to $+125^{\circ}C$; typical values at $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
	Resolution	No missing codes		16		Bits
DNL	Differential nonlinearity		-0.75	±0.4	0.75	LSB
INL	Integral nonlinearity		-1	±0.6	1	LSB
$V_{(OS)}$	Input offset error		-1	±0.8	1	LSB
dV_{OS}/dT	Input offset error thermal drift			0.8		$\mu V/^{\circ}C$
	Offset error match	$V_{(OS)} (ADC_A - ADC_B)$		1		LSB
G_E	Gain error ⁽¹⁾		-0.005	±0.001	0.005	%FSR
dG_E/dT	Gain error thermal drift	Reference buffer on ⁽¹⁾		1		ppm/ $^{\circ}C$
		Reference buffer off ⁽²⁾		0.4		
	Gain error match	$G_E (ADC_A - ADC_B)$		±0.001		%FSR
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	$f_{IN} = 2kHz$	TBD	89.9		dB
		$f_{IN} = 1MHz$		88.5		
SNR	Signal-to-noise ratio	$f_{IN} = 2kHz$	TBD	90		dB
		$f_{IN} = 1MHz$		88.6		
THD	Total harmonic distortion	$f_{IN} = 2kHz$		-112		dB
		$f_{IN} = 1MHz$		-100		
SFDR	Spurious-free dynamic range	$f_{IN} = 2kHz$		112		dB
		$f_{IN} = 1MHz$		100		
CMRR	Common-mode rejection ratio	$f_{IN} = dc$ to 1kHz, $V_{IN} = 500mV_{PP}$		70		dB
	Channel-to-channel isolation	$f_{IN_ADCA} = 15kHz$ at 10% FSR, $f_{IN_ADCB} = 25kHz$ at 100% FSR		-110		dB
POWER SUPPLY						
I_{AVDD}	Supply current from AVDD	Full-speed (ADS9327)		2.7	3	mA
		Full-speed (ADS9326)		2.1	2.5	
		No conversion (idle) (ADS9327)		1.2	1.5	
		No conversion (idle) (ADS9326)		1.2	1.5	
		Power-down		0.6	0.9	
I_{VDD_1V8}	Supply current from VDD_1V8	Full-speed (ADS9327)		9.5	10.2	mA
		Full-speed (ADS9326)		6.9	7.4	
		No conversion (idle) (ADS9327)		6.4	7.2	
		No conversion (idle) (ADS9326)		4.9	5.5	
		Power-down		0.78	1	
I_{IOVDD}	Supply current from IOVDD	Full-speed (ADS9327)		2.6	2.9	mA
		Full-speed (ADS9326)		1.6	1.8	
		No conversion (idle)		0.25	0.35	
		Power-down		0.25	0.35	

(1) These specifications include full temperature range variation but not the error contribution from internal reference.

(2) For more details, see [External Reference with External Reference Buffer](#).

6.7 Electrical Characteristics

at AVDD = 3V to 5.25V, VDD_1V8 = 1.75V to 1.85V, internal reference, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
CSH	Sampling capacitance			18		pF
BW	Analog input bandwidth	–3dB		45		MHz
		–0.1dB input signal		1.5		
I _B	Analog input leakage current	Idle-channel		0.5	1	μA
SAMPLING DYNAMICS						
t _A	Aperture delay			4		ns
	Aperture mismatch			100		ps
t _{JITTER}	Aperture jitter			1		ps
DIGITAL INPUTS						
V _{IL}	Input low logic level		–0.1		0.5	V
V _{IH}	Input high logic level		IOVDD – 0.5		IOVDD	V
DIGITAL OUTPUTS						
V _{OL}	Output low logic level	I _{OL} = 200μA sink	0		0.4	V
V _{OH}	Output high logic level	I _{OH} = 200μA source	IOVDD – 0.4		IOVDD	V

6.8 Timing Requirements

at AVDD = 3V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal reference, and maximum throughput (unless otherwise noted); $C_L = 10\text{pF}$; minimum and maximum values at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$; typical values at $T_A = 25^\circ\text{C}$

			MIN	MAX	UNIT
CONVERSION CYCLE					
f_{CYCLE}	Sampling frequency	ADS9327		5	MHz
		ADS9326		3	
t_{CYCLE}	ADC cycle-time period		$1/f_{\text{CYCLE}}$		s
f_{CLK}	Maximum SCLK frequency			65	MHz
t_{CLK}	Minimum SCLK time period		16.7		ns
t_{ACQ}	Acquisition time	ADS9327	70		ns
		ADS9326	133.33		
$t_{\text{PH_CV}}$	CONVST high time		10		ns
$t_{\text{PL_CV}}$	CONVST low time		10		ns
SPI INTERFACE TIMINGS					
$t_{\text{hi_CSZ}}$	Pulse duration: $\overline{\text{CS}}$ high		5		ns
$t_{\text{PH_CK}}$	SCLK high time		0.40	0.60	t_{CLK}
$t_{\text{PL_CK}}$	SCLK low time		0.40	0.60	t_{CLK}
$t_{\text{d_CSCK}}$	Setup time: $\overline{\text{CS}}$ falling to the first SCLK rising edge		12		ns
$t_{\text{su_CKDI}}$	Setup time: SDI data valid to the corresponding SCLK rising edge		3		ns
$t_{\text{ht_CKDI}}$	Hold time: SCLK rising edge to corresponding data valid on SDI		1		ns
$t_{\text{ht_CVCS}}$	Hold time: CONVST falling edge to $\overline{\text{CS}}$ falling edge		10		ns
$t_{\text{ht_CKCS}}$	Hold time: last SCLK falling edge to $\overline{\text{CS}}$ rising		10		ns

6.9 Switching Characteristics

at AVDD = 3V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal reference, and maximum throughput (unless otherwise noted); $C_L = 10\text{pF}$; minimum and maximum values at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$; typical values at $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
CONVERSION CYCLE					
t _{CONV}	ADC conversion time	ADS9327		130	ns
		ADS9326		200	
RESET					
t _{PU}	Power-up time for device			150	ms
SPI INTERFACE TIMINGS					
t _{den_CSDO}	Time delay: $\overline{\text{CS}}$ falling edge to data valid on SDO			16	ns
t _{dz_CSDO}	Time delay: $\overline{\text{CS}}$ rising edge to SDO going Hi-Z			7.5	ns
t _{ht_CKDO}	Hold time: SCLK launch edge to previous data valid on SDO		7.6		ns
t _{d_CKDO}	Time delay: SCLK launch edge to corresponding data valid on SDO			17	ns

6.10 Timing Diagrams

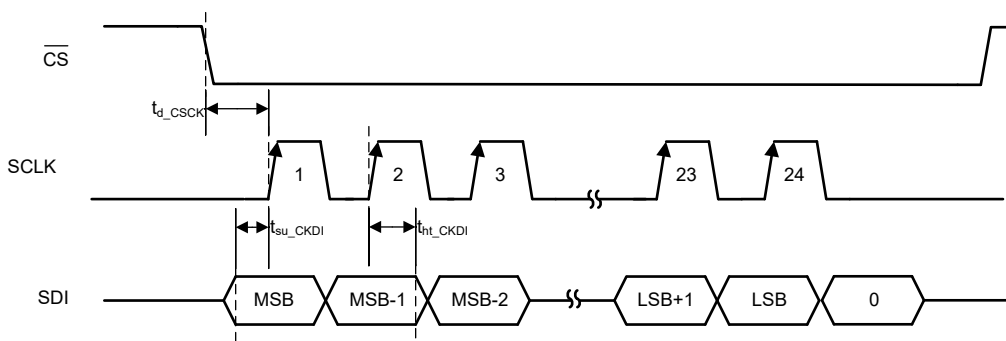


Figure 6-1. SDI Timing for Register Operations

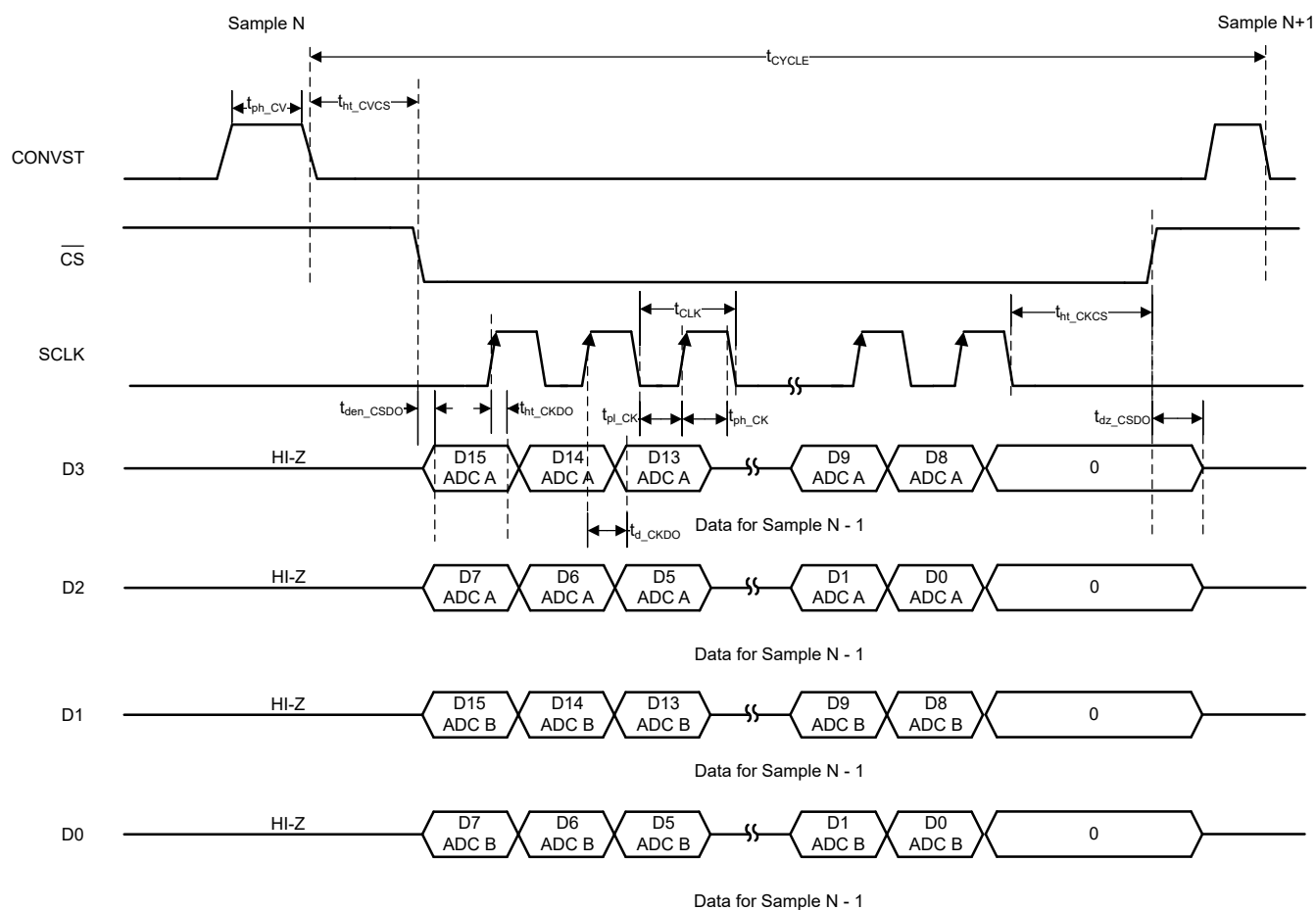


Figure 6-2. Conversion Cycle Timing: 4-Lane Default Operation

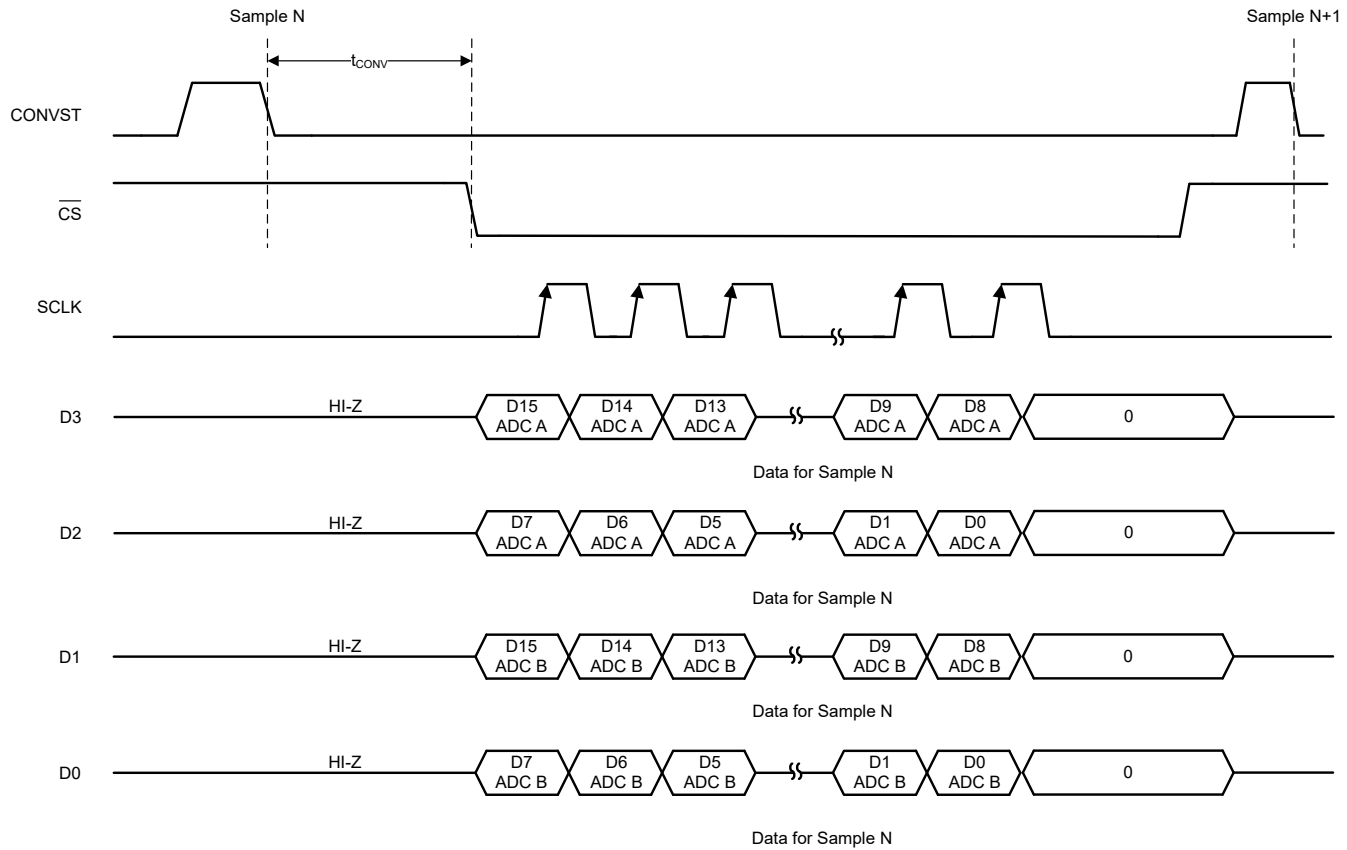


Figure 6-3. Conversion Cycle Timing: 4-Lane Low-Latency Mode

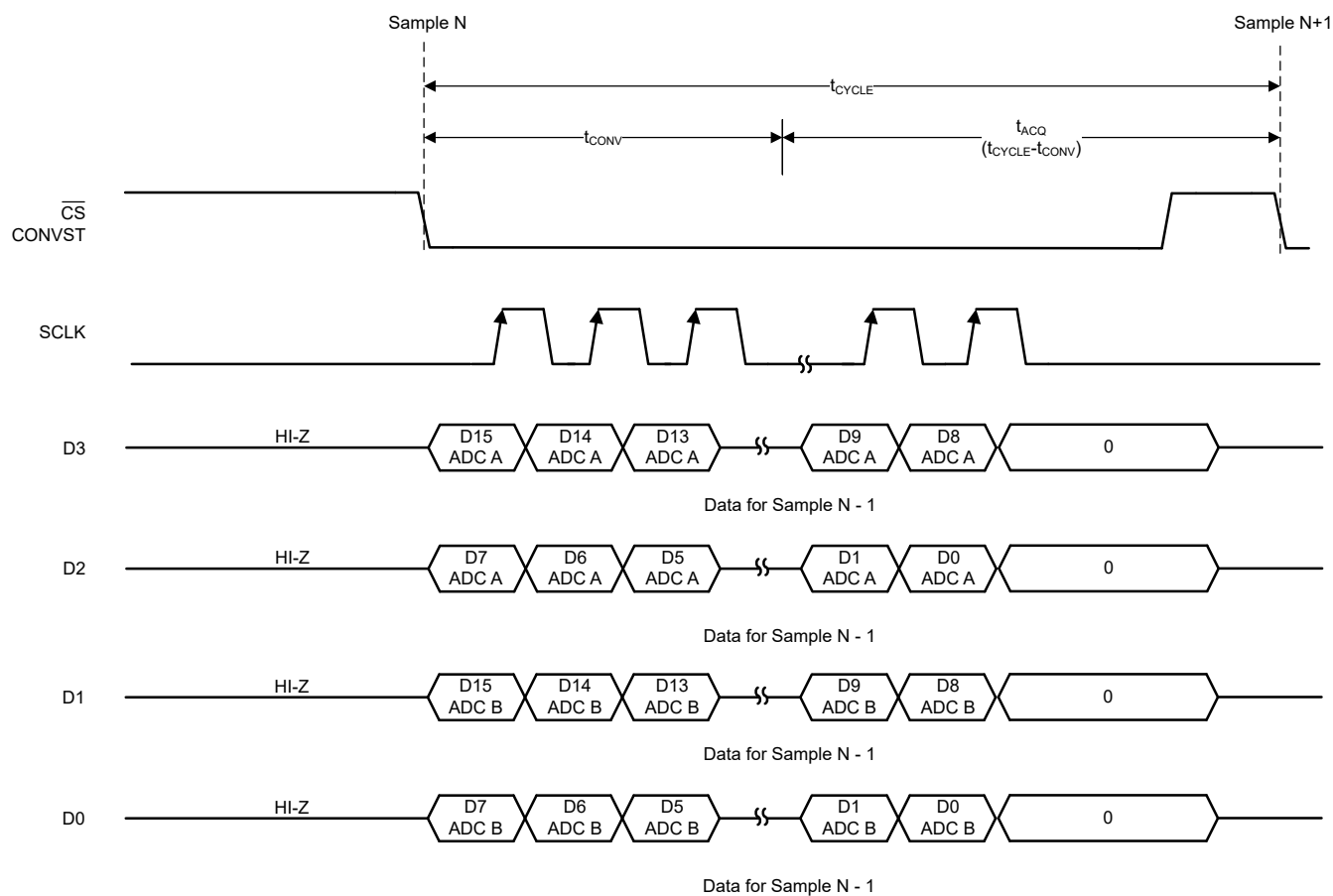
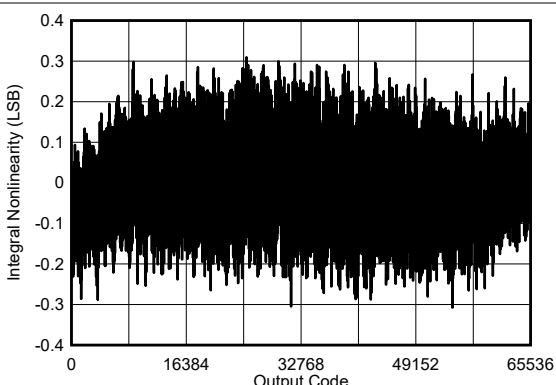


Figure 6-4. Conversion Cycle Timing: 4-Lane $\overline{\text{CS}}$ -CONVST Short Mode

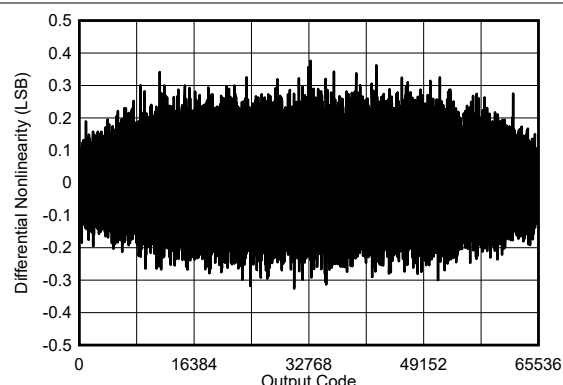
6.11 Typical Characteristics: AVDD = 5V

at $T_A = 25^\circ\text{C}$, AVDD = 5V, VDD_1V8 = 1.8V, external $V_{REF} = 4.096\text{V}$, and maximum throughput (unless otherwise noted)



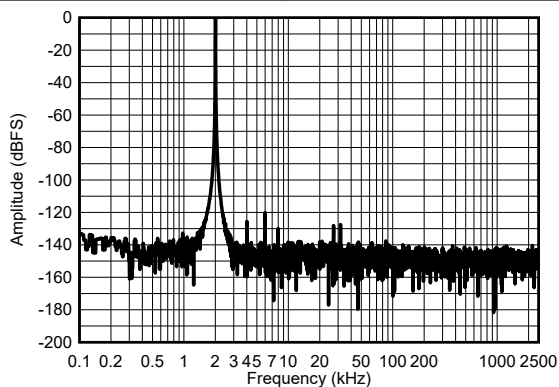
Typical INL = $\pm 0.3\text{LSB}$

Figure 6-5. Typical INL



Typical DNL = $\pm 0.35\text{LSB}$

Figure 6-6. Typical DNL



$f_{IN} = 2\text{kHz}$, SNR = 93.2dB, THD = -118dB

Figure 6-7. Typical FFT for $f_{IN} = 2\text{kHz}$

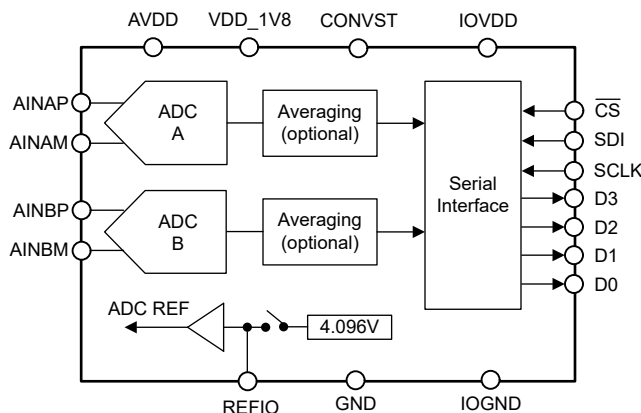
7 Detailed Description

7.1 Overview

The ADS932x (ADS9326, ADS9327) is a family of 16-bit, dual, simultaneous-sampling, analog-to-digital converters (ADCs) with an integrated reference. The ADS932x supports fully differential analog input signals and features built-in data averaging.

The ADS932x provides a simple, serial interface to the host controller and operates over a wide range of analog and digital power supplies. The serial interface is compatible with traditional SPI protocols and supports daisy-chain connection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs

This device supports unipolar, fully differential, analog input signals. Figure 7-1 shows a small-signal equivalent circuit of the sample-and-hold circuit. Each sampling switch is represented by a resistance (R_{S1} and R_{S2} , typically 200 Ω) in series with sampling switches (SW_1 and SW_2). The sampling capacitors, C_{S1} and C_{S2} , are typically 18pF.

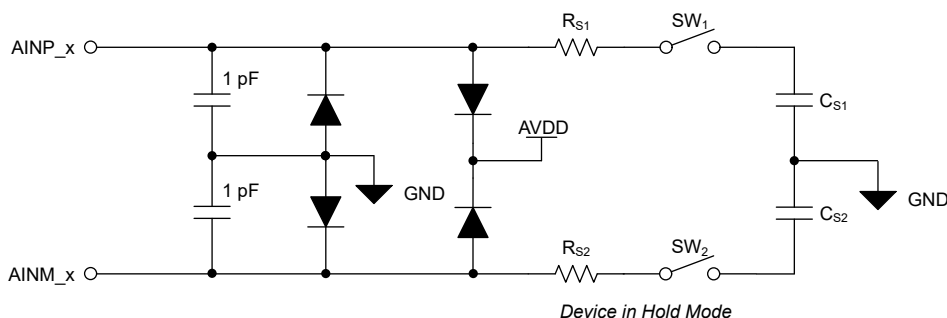


Figure 7-1. Analog Inputs

7.3.2 Reference

The ADS932x has a precision, low-drift voltage reference internal to the device. For best performance, filter the internal reference noise by connecting a 1µF ceramic bypass capacitor to the REFIO pin. On power-up, as described in [Table 7-1](#), the reference source is selected by writing to PD_REF in address 0x0C in register bank 1.

Table 7-1. Reference Source Selection

PD_REF REGISTER VALUE	ADC REFERENCE SOURCE
10b	Internal reference is active.
11b	Internal reference is inactive. Force an external reference with REFIO (pin 9).

7.3.2.1 Internal Reference

The ADS932x features an internal reference voltage with a nominal output voltage of 4.096V when AVDD = 5V and 2.5V when AVDD = 3.3V. To enable the internal reference, write 10b to PD_REF in register bank 1. As shown in [Figure 7-2](#), place a minimum 1µF decoupling capacitor between the REFIO and REF_M pins.

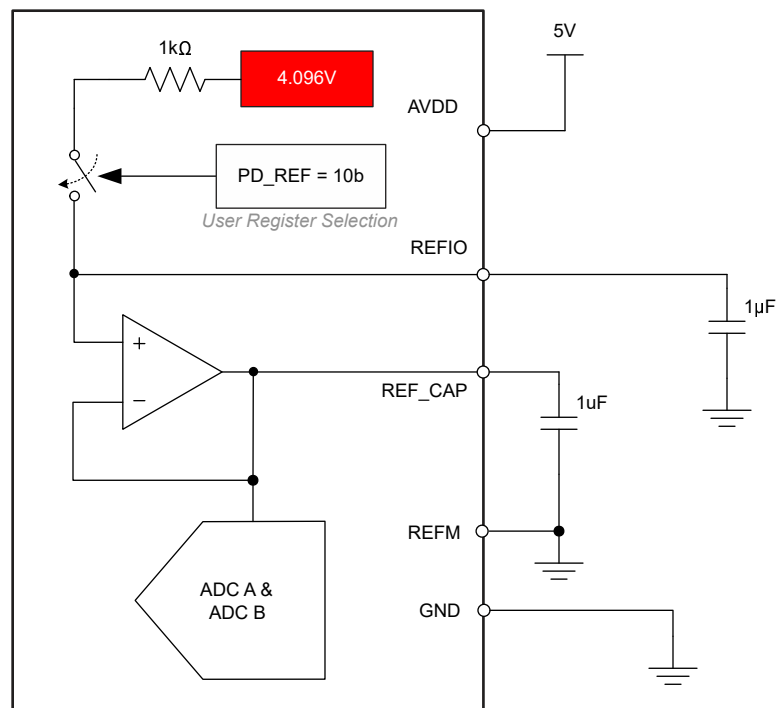


Figure 7-2. Internal Reference: AVDD = 5V

7.3.2.2 External Reference

Connect an external reference voltage, as shown in Figure 7-3, at the REFIO pin with an appropriate decoupling capacitor placed between the REFIO and REFM pins. For improved thermal drift performance, use the REF7040. To disable the internal reference, set PD_REF = 11b in address 0x0C in register bank 1 as described in the Reference section. The REFIO pin has electrostatic discharge (ESD) protection diodes connected to the AVDD and REFM pins. In default configuration, the ADS932x supports a 2.5V nominal external reference value when AVDD = 3.3V and a 4.096V value when AVDD = 5V. Configure the ADS932x to support a nominal external reference value from 3V to 4.096V by writing 0x0010 to address 0x33 in register bank 2.

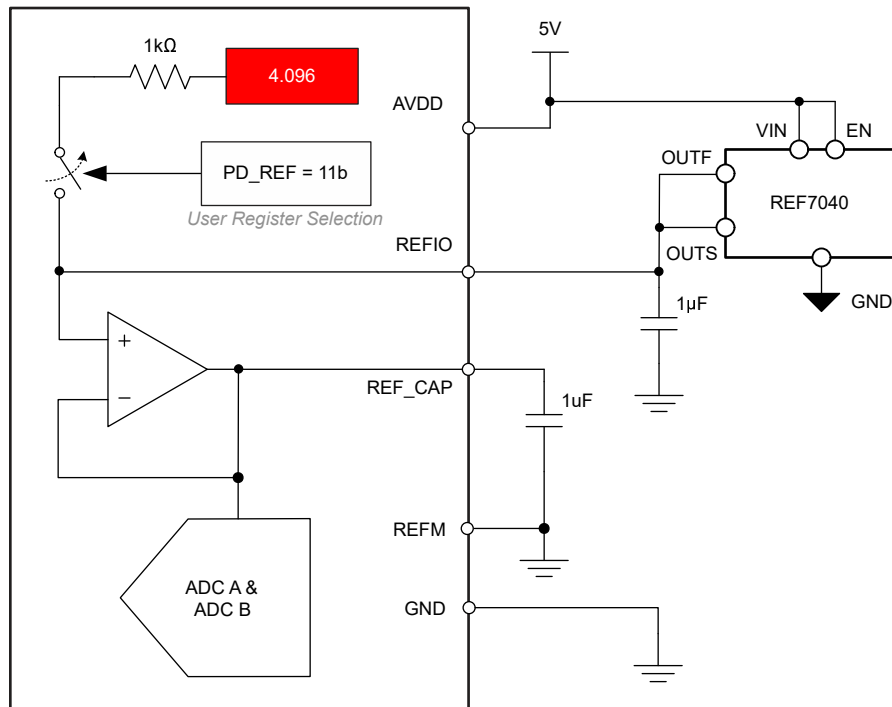


Figure 7-3. External Reference: AVDD = 5V

7.3.2.3 External Reference With External Reference Buffer

To improve system gain error thermal drift, power off the internal device reference buffer and connect an external, low-drift reference buffer to the device. As illustrated in Figure 7-4, connect the output of the external reference buffer to the REFIO and REF_CAP pins and power down the internal reference buffer. Make sure the connection to REF_CAP is less than 2Ω. Table 7-2 describes the sequence to power down the internal reference buffer.

Table 7-2. Sequence to Power Down the Internal Reference Buffer

FRAME NUMBER	REGISTER		DESCRIPTION
	ADDRESS	VALUE[15:0]	
1	0x02	0x0002	Select register bank 1
2	0x0C	0x0300	Power down the internal reference
3	0x03	0x000B	Unlock register bank 2
4	0x02	0x0008	Select register bank 2
5	0x09	0x0010	Power down the internal reference buffer
6	0x02	0x0002	Select register bank 1

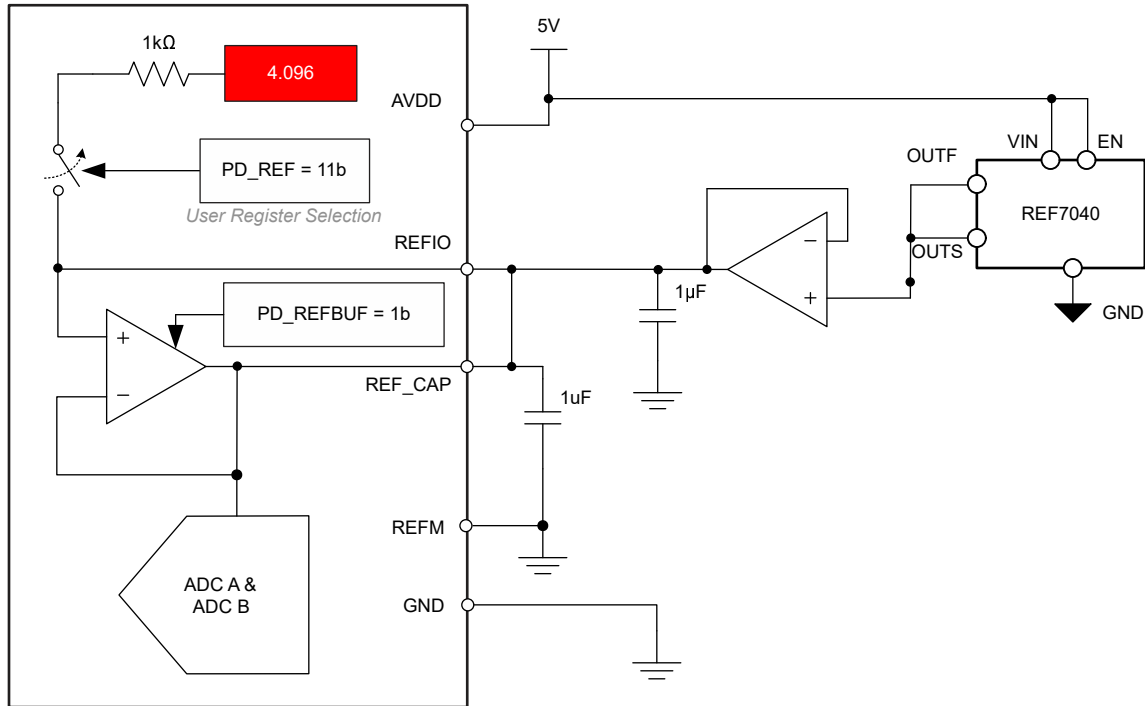


Figure 7-4. External Reference With External Reference Buffer

7.3.3 ADC Transfer Function

The ADS932x outputs 16 bits of conversion data in either two's-complement or straight-binary format. By default, conversion data is output in two's-complement format. To enable straight-binary format, write 1b to DATA_FORMAT in address 0x0D. Table 7-3 and Figure 7-5 describe the transfer characteristics for the ADS932x. Equation 1 gives the least significant bit (LSB) for the ADC.

$$1\text{LSB} = (2 \times V_{\text{REFIO}}) / 2^N \quad (1)$$

where:

- N = Device resolution

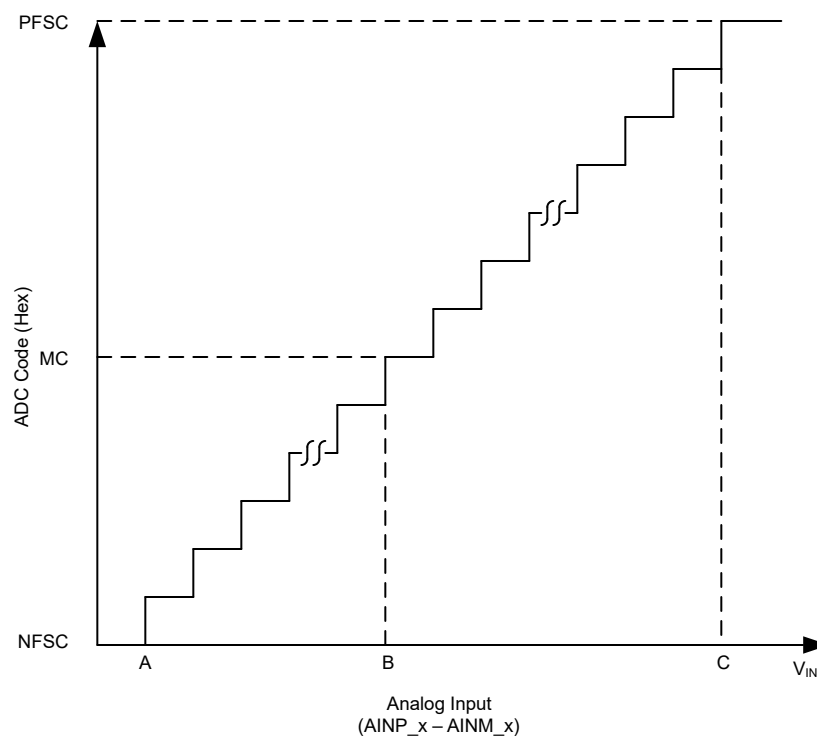


Figure 7-5. Transfer Characteristics

Table 7-3. Transfer Characteristics

STEP	INPUT VOLTAGE ($AINP_x - AINM_x$)	CODE	DESCRIPTION	16-BIT OUTPUT CODE (Two's Complement)	16-BIT OUTPUT CODE (Straight Binary)
A	$\leq -(V_{REFIO} + 1\text{LSB})$	NFSC	Negative full-scale code	0x8000	0x0000
B	$0V + 1\text{LSB}$	MC	Mid-code	0x0000	0x8000
C	$\geq (V_{REFIO} - 1\text{LSB})$	PFSC	Positive full-scale code	0x7FFF	0xFFFF

7.3.4 Data Interface

The ADS932x features an SPI-compatible serial interface with 1-lane, 2-lane, and 4-lane options for the data output. [Table 7-4](#) shows the register settings to configure the number of output data lanes and the corresponding ADC conversion data output on each serial data output pin.

Table 7-4. Output Data Interface Configuration Settings

NUMBER OF OUTPUT DATA LANES	NUM_DATA_LANES REGISTER VALUE	SERIAL DATA OUTPUT PIN	ADC CONVERSION DATA OUTPUT
4 lanes	000b	D3	ADC A[15:8]
		D2	ADC A[7:0]
		D1	ADC B[15:8]
		D0	ADC B[7:0]
2 lanes	101b	D3	ADC A[15:0]
		D2	Hi-Z
		D1	ADC B[15:0]
		D0	Hi-Z
1 lane	110b	D3	ADC A[15:0], 0x00, ADC B[15:0], 0x00
		D2	Hi-Z
		D1	Hi-Z
		D0	Hi-Z

7.3.5 Programmable Data Averaging Filter

The ADS932x features a built-in programmable data averaging filter:

- Simple data average: As shown in [Figure 7-6](#), the ADC output is the average of conversion results in a fixed-size window. This window is defined in the SAVG_MODE field in address 0x0D in register bank 1. The output data rate of the ADC reduces with an increased window size for data averaging. To enable simple data averaging, write 1b to SAVG_EN in address 0x0D and select the window size by writing to SAVG_MODE in address 0x0D.

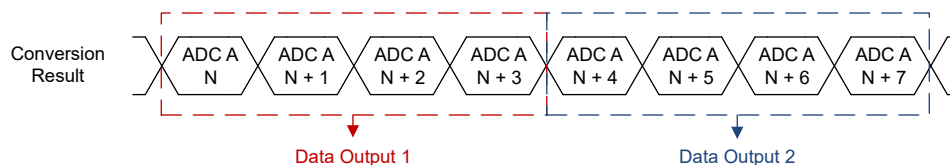


Figure 7-6. Simple Average Data Output

[Table 7-5](#) specifies the improvement in SNR with data averaging and corresponding impact on ADC output rate. [Figure 7-7](#) illustrates the ADC output for an average of four samples. When averaging is enabled, the output data frame width increases by four bits, as described in the [Data Frame Width](#) section.

Table 7-5. ADC Output Data Rate and SNR vs Data Averaging

OVERSAMPLING RATIO	SNR - ADS9327 (16-BIT)	MAXIMUM OUTPUT DATA RATE
No averaging	93dB	5MSPS
2	95.7dB	2.5MSPS
4	98.3dB	1.25MSPS
8	101dB	625kSPS
16	103.6dB	312.5kSPS
32	106.3dB	156.25kSPS
64	108.9dB	78.125kSPS
128	111.6dB	39.0625kSPS

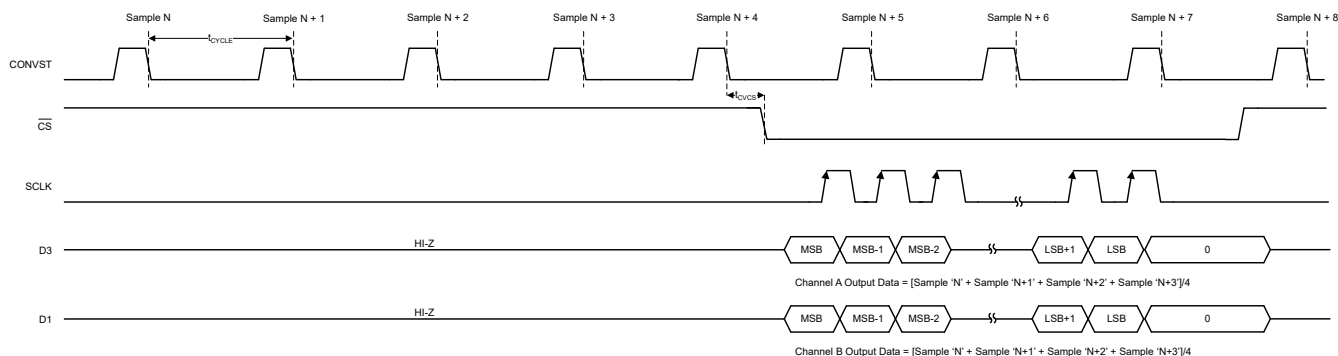


Figure 7-7. ADC Output Example for Simple Average of 4 Samples in 2-Lane Data Interface Mode

7.3.6 CRC on Output Data Interface

The cyclic redundancy check (CRC) is an error checking code that detects communication errors to the host. CRC is the division remainder of the data payload bytes by a fixed polynomial. The CRC mode is optional and is enabled by the CRC_EN bit in address 0x0D in register bank 1. The CRC in the ADS932x is only implemented on the output data interface and is not used for register read or write operations. When CRC is enabled, the CRC data byte is appended to the ADC conversion result, see the [Data Frame Width](#) section.

The CRC data byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the argument by a CRC polynomial. The CRC polynomial is based on the CRC-8-CCITT: $X^8 + X^2 + X^1 + 1$. The CRC calculation is preset with 0b11111111.

7.3.7 ADC Output Data Randomizer

The ADS932x features a data output randomizer. When enabled, the ADC conversion result is bit-wise exclusive-ORed (XOR) with the four pseudo-random binary sequence (PRBS) bits appended to the ADC data output. See the [Data Frame Width](#) section. The XOR PRBS bits have equal probability of being either 1 or 0. As a result of the XOR operation, the data from the ADS932x is randomized. The ground bounce created by the transmission of this randomized result over the data interface is uncorrelated with the analog input voltage. This uncorrelated transmission helps minimize interference between data transmission and analog performance of the ADC when the PCB layout does not minimize ground bounce. To enable the output data randomizer, write 01111b to XOR_EN in address 0x0D in register bank 1. [Figure 7-8](#) shows the data output when the data output randomizer is enabled.

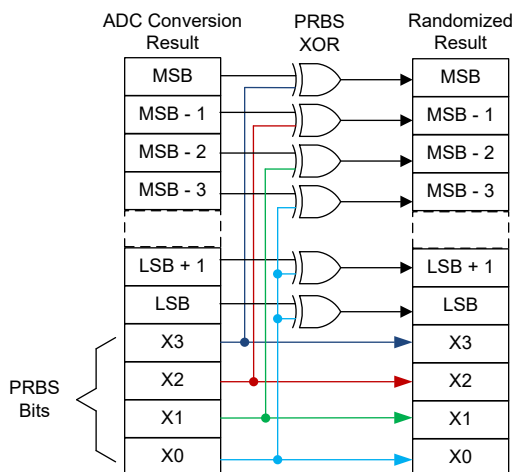


Figure 7-8. XOR Operation With 4-Bit PRBS

7.3.8 Data Frame Width

The ADS932x supports 16-bit, 20-bit, and 24-bit data frame width options. The default output data frame width is 16 bits. As shown in [Table 7-6](#), the output data frame width increases to 20 or 24 bits depending on the use of averaging, XOR, and CRC.

Table 7-6. Output Data Frames

CRC_EN	SAVG_EN	XOR_EN	OUTPUT WIDTH (Bits)	OUTPUT DATA FRAME
CRC module disabled	No averaging	XOR disabled	16	{Conversion result [15:0]}
		XOR enabled	20	{Conversion result [15:0], PRBS[3:0]}
	Averaging enabled	XOR disabled	20	{Conversion result [17:0], 0b00}
		XOR enabled	24	{Conversion result [17:0], PRBS[3:0], 0b00}
CRC module enabled	No averaging	XOR disabled	24	{Conversion result [15:0], CRC[7:0]}
		XOR enabled	N/A	Not supported
	Averaging enabled	XOR disabled	N/A	Not supported
		XOR enabled	N/A	Not supported

7.3.9 Daisy-Chain Mode

The ADS932x operates either as a single converter or in a system with multiple converters. To take advantage of the simple, high-speed, SPI serial interface, cascade converters in a daisy-chain configuration when multiple converters are used. No register configuration is required to enable daisy-chain mode. [Figure 7-9](#) shows a typical connection of three converters in daisy-chain mode.

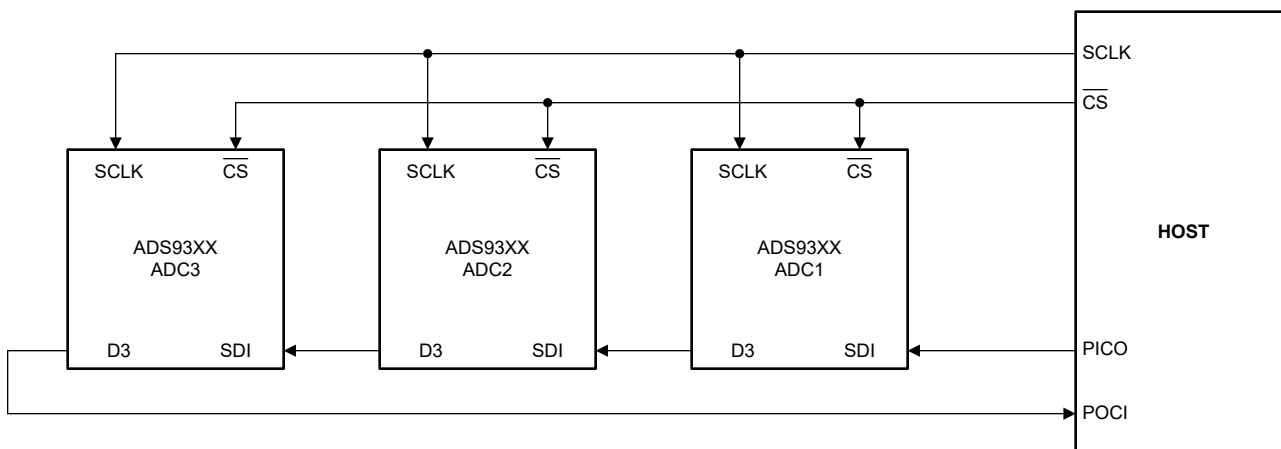


Figure 7-9. Daisy-Chain Connections

When the ADS932x is connected in daisy-chain mode, make sure the device operates in 1-lane interface mode by writing 110b to NUM_DATA_LANES. See the [Data Interface](#) section. The serial input data passes through the device with a 48 SCLK delay as long as CS is active. [Figure 7-10](#) illustrates a detailed timing diagram of this mode when the conversion in each converter is performed simultaneously.

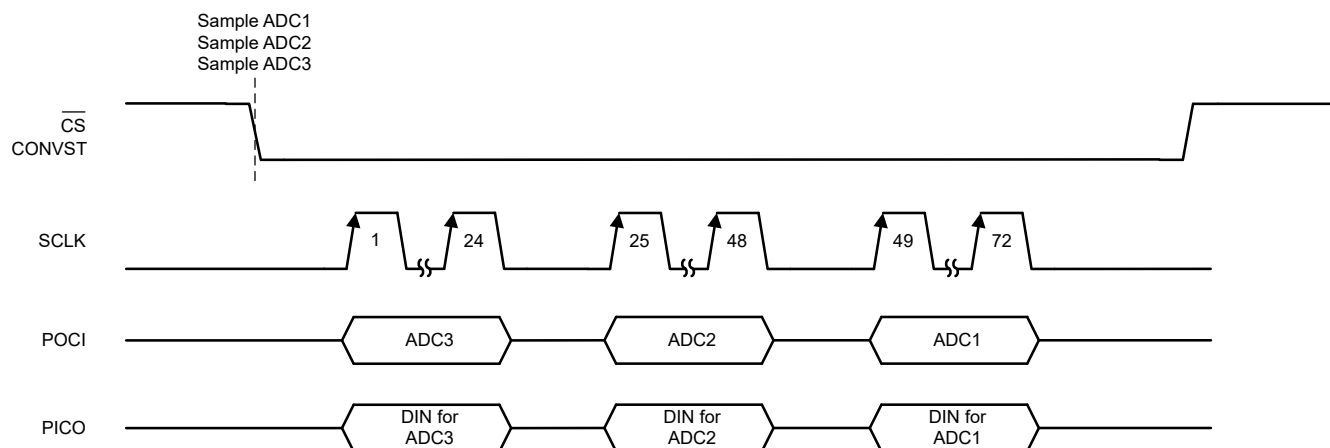


Figure 7-10. Simplified Daisy-Chain Timing

7.3.9.1 Daisy-Clock Mode

When operating in a daisy-chain configuration, as shown in [Figure 7-11](#), the ADS932x features an option to feed-through SCLK on D0. To enable daisy-clock mode, write 1b to DAISY_CLK in address 0x09.

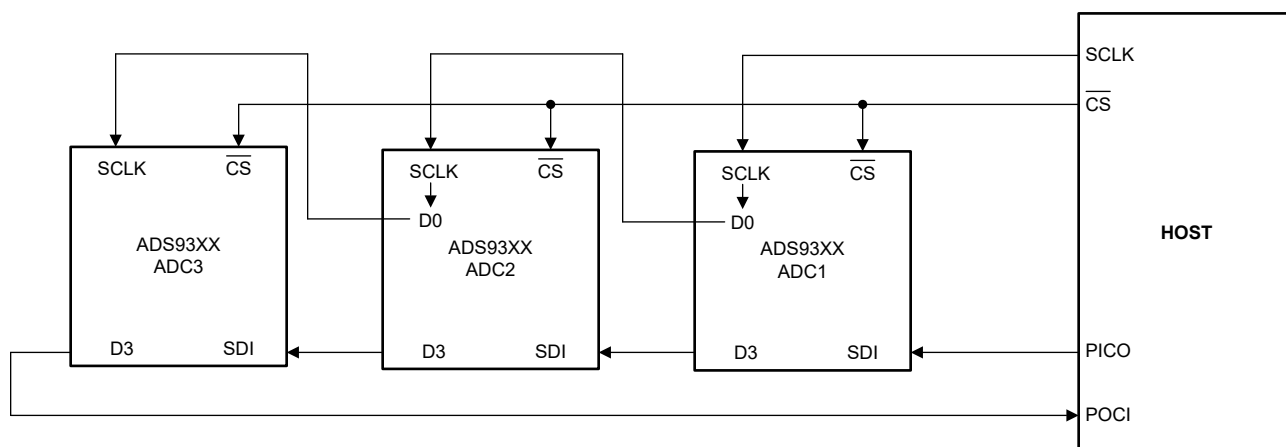


Figure 7-11. Daisy-Chain Connections With Daisy-Clock Mode Enabled

7.4 Device Functional Modes

7.4.1 Reset

Reset the ADS932x by writing 1b to the RESET field in address 0x01. The device registers are initialized to the default values after reset.

7.4.2 Normal Operation

In normal operating mode, the ADS932x is powered up and digitizes sample N on the falling edge of CONVST. Data corresponding to sample N – 1 is launched on the digital interface on the falling edge of $\overline{CS}$ as illustrated in Figure 6-2.

7.4.3 Low-Latency Mode

In low-latency mode, the conversion for sample N starts on the falling edge of CONVST. Data corresponding to sample N are launched on the digital interface on the falling edge of $\overline{CS}$. As illustrated in Figure 6-3, the host provides a minimum time of t_{CONV} between the falling edges of CONVST and $\overline{CS}$. To enter low-latency mode, write 1b to LATENCY_MODE in address 0x09.

7.4.4 $\overline{CS}$ -CONVST Short Mode

In $\overline{CS}$ -CONVST short mode, tie $\overline{CS}$ and CONVST together externally. As illustrated in Figure 6-4, the ADS932x digitizes sample N on the falling edge of CONVST. Data corresponding to sample N – 1 are launched on the digital interface on the falling edge of $\overline{CS}$. To enter $\overline{CS}$ -CONVST short mode, write 101b to CSZ_CONVST_SHORT_EN in address 0x13 in register bank 1.

7.4.5 Register Read Mode

In register read mode, the device launches the requested device register data on D3. To enter register read mode, set DATA_SEL = 1b as described in the [Register Read](#) section.

7.4.6 Initialization Sequence

As shown in Table 7-7, initialize the ADS932x with a sequence of register writes after device power-up or reset. The device registers are initialized with the default value after the initialization sequence is complete.

Table 7-7. ADS932x Initialization Sequence

STEP NUMBER	REGISTER			DESCRIPTION
	BANK	ADDRESS	VALUE[15:0]	
1	0	0x01	0x0002	Software reset
2	Wait 1ms			
3	0	0x01	0x0000	Clear software reset
4	0	0xFE	0xB38F	Register map unlock sequence frame 1
5	0	0xFE	0xABCD	Register map unlock sequence frame 2
6	0	0x02	0x0002	Select register bank 1
7	1	0x0C	0x1200	Select internal reference and INIT_0(0xC[12]) = 1
8	Wait 25ms			
9	1	0x0C	0x0200	INIT_0(0xC[12]) = 0
10	0	0x03	0x000B	Unlock register bank 2
11	0	0x02	0x0008	Select register bank 2
12	2	0x22	0x0080	INIT_2 = 1
13	0	0x02	0x0002	Select register bank 1
14	0	0xFE	0x1234	Register map lock sequence

7.5 Programming

7.5.1 SPI Frame Length for Register Operations

As described in [Table 7-8](#), use a 24-bit or 48-bit SPI for register read or write operations, depending on the number of output data lanes used. If the SPI frame length is longer or shorter than required, this disparity results in unintentional writes to the user registers.

Table 7-8. SPI Frame Length Requirements

NUMBER OF OUTPUT DATA LANES	NUMBER OF SCLKS REQUIRED
4	24
2	24
1	48

7.5.2 Register Map Lock

The ADS932x implements a register map lock feature that prevents an accidental or unintended write to the device registers. By default, the device register map is locked. Unlock the register map by following the sequence shown in [Table 7-9](#) before writing or reading a register.

Table 7-9. ADS932x Register Map Unlock Sequence

STEP NUMBER	REGISTER		
	BANK	ADDRESS	VALUE[15:0]
1	0	0xFE	0xB38F
2	0	0xFE	0xABCD

After writing or reading registers, lock the register map to prevent unintended register writes. Writing any value other than the register map unlock sequence to address 0xFE locks the register map. [Table 7-10](#) shows an example sequence to lock the device register map.

Table 7-10. ADS932x Example Register Map Lock Sequence

STEP NUMBER	REGISTER		
	BANK	ADDRESS	VALUE[15:0]
1	0	0xFE	0x1234

7.5.3 Register Write

Register write access is enabled by following the register map unlock sequence described in the [Register Map Lock](#) section. The 16-bit registers are grouped in two register banks and are addressable with an 8-bit register address. Register bank 1 is selected for read or write operation by writing 0x02 to REG_BANK_SEL in address 0x02. Registers in bank 0 are always accessible, irrespective of the REG_BANK_SEL bits. The register addresses in bank 0 are unique and are not used in register bank 1. The 24-bit data on SDI consist of an 8-bit address and 16-bit data. The data on SDI are latched on the rising edge of SCLK. The device decodes the write command on the $\overline{CS}$ rising edge and updates the specified register with 16-bit data specified in the register write operation. [Figure 7-12](#) shows a 24-bit SPI frame for a register write and [Table 7-11](#) describes the steps required to write a register.

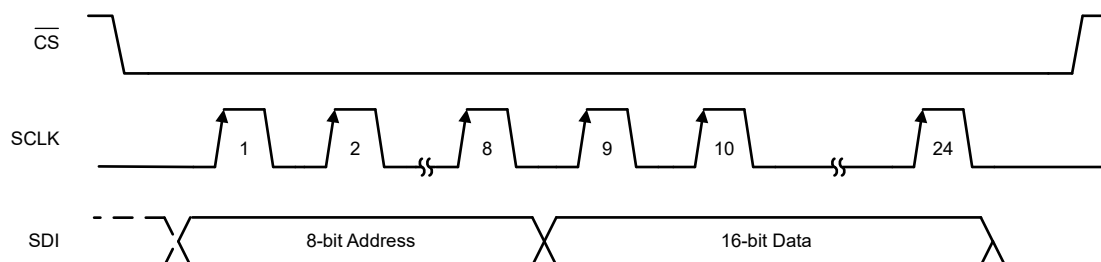


Figure 7-12. Register Write Frame

Table 7-11. Register Write Sequence

FRAME NUMBER	REGISTER		DESCRIPTION
	ADDRESS	VALUE[15:0]	
1	0xFE	0xB38F	Unlocks the register map.
2	0xFE	0xABCD	
3	0x02	0x02	Selects register bank 1. This step is only required for register bank 1.
4	REG_ADDR	DATA	Writes user data to the desired address. Repeat this step for the required number of register writes.
5	0xFE	0x1234	Locks the register map after register writes are completed.

7.5.4 Register Read

Register access is enabled by following the register map unlock sequence described in the [Register Map Lock](#) section. To read registers in bank 1, write 0x02 to register address 0x02. As shown in [Figure 7-13](#), 24-bit or 48-bit SPI frames are required to read registers. [Table 7-12](#) describes the sequence required to read a register. After the register map is unlocked and the register bank is selected, write the register address to be read to REG_READ_ADDR. Set DATA_SEL = 1 in address 0x01 to launch the register data on D3 in the next frame. On the rising edge of $\overline{CS}$, the read command is decoded and the requested register data are available for reading during the next frame. During the next frame, the first 16 bits on D3 correspond to the requested register read. Use SDI to initiate another operation or set SDI to 0. To begin launching ADC conversion results on the digital interface in the following frame, set DATA_SEL = 0b. After register operations are completed, lock the register map as described in the [Register Map Lock](#) section.

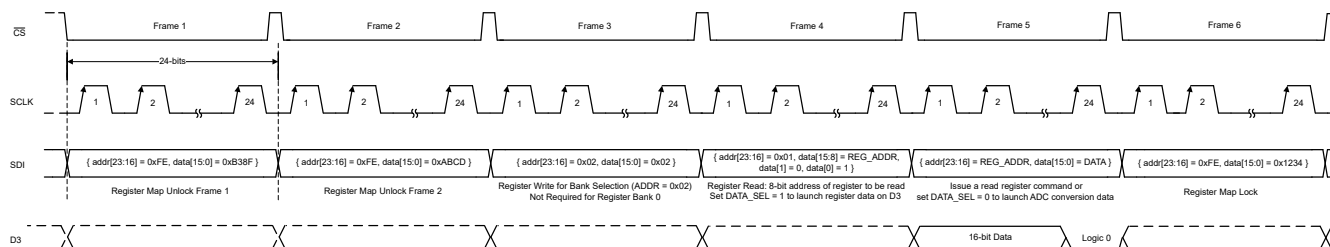
**Figure 7-13. Register Read**

Table 7-12. Register Read Sequence

FRAME NUMBER	REGISTER		DESCRIPTION
	ADDRESS	VALUE[15:0]	
1	0xFE	0xB38F	Unlocks the register map.
2	0xFE	0xABCD	
3	0x02	0x02	Selects register bank 1. This step is only required for register bank 1.
4	0x01	REG_READ_ADDR[15:8] = REG_ADDR, RESET[1] = 0, DATA_SEL[0] = 1	REG_READ_ADDR selects the address to be read and DATA_SEL launches the selected register data on D3 in the following frame.
5	REG_ADDR	DATA	The 16-bit data requested in the previous frame is available on D3. In this frame, issue another read register command or write DATA_SEL = 0 in address 0x01. This setting begins launching ADC conversion data on the data interface in the next frame. Repeat this step for the required number of register reads.
6	0xFE	0x1234	Locks the register map after register operations are completed.

8 Register Map

8.1 Register Bank 0

Table 8-1 lists the memory-mapped registers for the register bank 0 registers. Consider all register offset addresses not listed in Table 8-1 as reserved locations and do not modify the register contents.

Table 8-1. Register Map Bank 0

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	Register 01h	REG_READ_ADDR[7:0]							
		RESERVED						RESET	DATA_SEL
0x02	Register 02h	RESERVED							
		RESERVED				REG_BANK_SEL[3:0]			
0x03	Register 03h	RESERVED							
		RESERVED				BANK_2_UNLOCK[3:0]			
0xFE	Register FEh	REG_LOCK[15:0]							
		REG_LOCK[15:0]							

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. Register Bank 0 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 Register 01h (Address = 0x01) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-1. Register 01h

15	14	13	12	11	10	9	8
REG_READ_ADDR[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED						RESET	DATA_SEL
R/W-000000b						R/W-0b	R/W-0b

Table 8-3. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
15:8	REG_READ_ADDR[7:0]	R/W	00000000b	8-bit address of the register to be read.
7:2	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
1	RESET	R/W	0b	ADC reset control. 0b = Normal device operation 1b = Reset ADC and all registers
0	DATA_SEL	R/W	0b	Select data to be launched on serial interface of the ADC. 0b = ADC conversion result is output 1b = Register data is output on D3

8.1.2 Register 02h (Address = 0x02) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-2. Register 02h

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				REG_BANK_SEL[3:0]			
R/W-000000000000b				R/W-0000b			

Table 8-4. Register 02h Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3:0	REG_BANK_SEL[3:0]	R/W	0000b	Register bank selection for read and write operations. 0000b = Select register bank 0 0010b = Select register bank 1 1000b = Select register bank 2

8.1.3 Register 03h (Address = 0x03) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-3. Register 03h

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				BANK_2_UNLOCK[3:0]			
R/W-000000000000b				R/W-0000b			

Table 8-5. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3:0	BANK_2_UNLOCK[3:0]	R/W	0000b	Key to unlock register bank 2. 1011b = Unlock register bank 2

8.1.4 Register FEh (Address = 0xFE) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-4. Register FEh

15	14	13	12	11	10	9	8
REG_LOCK[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
REG_LOCK[15:0]							
R/W-0000000000000000b							

Table 8-6. Register FEh Field Descriptions

Bit	Field	Type	Reset	Description
15:0	REG_LOCK[15:0]	R/W	000000000000000b	Key to unlock and lock the register map. To unlock the register map, write 0xB38F followed by 0xABCD. To lock the register map, write 0x1234.

8.2 Register Bank 1

Table 8-7 lists the memory-mapped registers for the register bank 1 registers. Consider all register offset addresses not listed in Table 8-7 as reserved locations and do not modify the register contents.

Table 8-7. Register Map Bank 1

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	Register 08h	RESERVED							
		RESERVED				PDN_CH[1:0]		RESERVED	PDN_CTL
0x09	Register 09h	RESERVED					LATENCY_MODE	RESERVED	
		RESERVED	NUM_DATA_LANES[2:0]			RESERVED			DAISY_CLK
0x0A	Register 0Ah	RESERVED							
		RESERVED				DIG_DELAY_EN	DRIVE_STRENGTH[2:0]		
0x0B	Register 0Bh	RESERVED				DIG_DELAY_D3[2:0]			DIG_DELAY_D2[2:0]
		DIG_DELAY_D2[2:0]		DIG_DELAY_D1[2:0]			DIG_DELAY_D0[2:0]		
0x0C	Register 0Ch	RESERVED						PD_REF[1:0]	
		RESERVED	CLK_PWR[2:0]			RESERVED			
0x0D	Register 0Dh	XOR_EN[4:0]					CRC_EN	RESERVED	DATA_FORMAT
		SAVG_MODE[3:0]				RESERVED		AVG_SYNC	SAVG_EN
0x0F	Register 0Fh	RESERVED							
		RESERVED		TEST_PATT_INCR[1:0]		TEST_PATT_MODE[1:0]		RESERVED	TEST_PATT_EN
0x10	Register 10h	TEST_PATT_1[15:0]							
		TEST_PATT_1[15:0]							
0x11	Register 11h	TEST_PATT_2[15:0]							
		TEST_PATT_2[15:0]							
0x13	Register 13h	RESERVED						CSZ_CONVST_SHORT_EN[2:0]	
		CSZ_CONVST_SHORT_EN[2:0]	RESERVED						

Complex bit access types are encoded to fit into small table cells. Table 8-8 shows the codes that are used for access types in this section.

Table 8-8. Register Bank 1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 Register 08h (Address = 0x08) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-5. Register 08h

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				PDN_CH[1:0]		RESERVED	PDN_CTL
R/W-000000000000b				R/W-00b		R/W-0b	R/W-0b

Table 8-9. Register 08h Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3:2	PDN_CH[1:0]	R/W	00b	Power-down control for the analog input channels. 00b = Normal device operation 01b = Channel A powered down 10b = Channel B powered down 11b = Both channels powered down
1	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
0	PDN_CTL	R/W	0b	Full device power-down control 0b = Normal device operation 1b = Full device power-down control

8.2.2 Register 09h (Address = 0x09) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-6. Register 09h

15	14	13	12	11	10	9	8
RESERVED					LATENCY_MODE	RESERVED	
R/W-00000b					R/W-0b	R/W-000b	
7	6	5	4	3	2	1	0
RESERVED	NUM_DATA_LANES[2:0]			RESERVED			DAISY_CLK
R/W-000b	R/W-000b			R/W-000b			R/W-0b

Table 8-10. Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.
10	LATENCY_MODE	R/W	0b	Control to select latency mode. 0b = Data corresponding to sample N – 1 is launched on the $\overline{CS}$ falling edge during the sample N frame. 1b = Low-latency mode is active. Data corresponding to sample N are launched on the $\overline{CS}$ falling edge during the sample N frame. $\overline{CS}$ is high until $t_{CONV(max)}$.
9:7	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
6:4	NUM_DATA_LANES[2:0]	R/W	000b	Control to select the number of lanes used for the serial data interface. 000b = ADC A data output on D[3:2] and ADC B data output on D[1:0]. 101b = ADC A data output on D3 and ADC B data output on D1. D2 and D0 are Hi-Z. 110b = ADC A and ADC B data output on D3. D[2:0] are Hi-Z.
3:1	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
0	DAISY_CLK	R/W	0b	Control to feed through SCLK (pin 17) on D0 (pin 16) when multiple devices are daisy-chained. 0b = D0 outputs data as per the data interface configuration 1b = D0 feeds through SCLK

8.2.3 Register 0Ah (Address = 0x0A) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-7. Register 0Ah

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				DIG_DELAY_EN	DRIVE_STRENGTH[2:0]		
R/W-000000000000b				R/W-0b	R/W-000b		

Table 8-11. Register 0Ah Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3	DIG_DELAY_EN	R/W	0b	Control for digital delay on the output buffer path. 0b = Normal device operation. 1b = Digital delay on the output buffer path is enabled. The magnitude is controlled by the DIG_DELAY_Dx fields in address 0Bh.
2:0	DRIVE_STRENGTH[2:0]	R/W	000b	Control to configure the drive strength of the digital output buffer. 000b = Normal device operation 101b = 0.5x drive strength 110b = 2x drive strength 111b = 1.5x drive strength

8.2.4 Register 0Bh (Address = 0x0B) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-8. Register 0Bh

15	14	13	12	11	10	9	8
RESERVED				DIG_DELAY_D3[2:0]			DIG_DELAY_D2[2:0]
R/W-0000b				R/W-000b			R/W-000b
7	6	5	4	3	2	1	0
DIG_DELAY_D2[2:0]		DIG_DELAY_D1[2:0]			DIG_DELAY_D0[2:0]		
R/W-000b		R/W-000b			R/W-000b		

Table 8-12. Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.
11:9	DIG_DELAY_D3[2:0]	R/W	000b	Programmable digital delay on D3. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
8:6	DIG_DELAY_D2[2:0]	R/W	000b	Programmable digital delay on D2. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
5:3	DIG_DELAY_D1[2:0]	R/W	000b	Programmable digital delay on D1. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
2:0	DIG_DELAY_D0[2:0]	R/W	000b	Programmable digital delay on D0. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay

8.2.5 Register 0Ch (Address = 0x0C) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-9. Register 0Ch

15	14	13	12	11	10	9	8
RESERVED						PD_REF[1:0]	
R/W-000000b						R/W-00b	
7	6	5	4	3	2	1	0
RESERVED		CLK_PWR[2:0]			RESERVED		
R/W-0b		R/W-000b			R/W-0000b		

Table 8-13. Register 0Ch Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:8	PD_REF[1:0]	R/W	00b	ADC reference voltage source selection. 10b = Internal reference is active. 11b = Internal reference is inactive. Force an external reference with REFIO (pin 9).
7	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
6:4	CLK_PWR[2:0]	R/W	000b	Control to select the power-supply domain for the input clock. 000b = IOVDD domain 101b = VDD_1V8 domain
3:0	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.

8.2.6 Register 0Dh (Address = 0x0D) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-10. Register 0Dh

15	14	13	12	11	10	9	8
XOR_EN[4:0]					CRC_EN	RESERVED	DATA_FORMAT
R/W-00000b					R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
SAVG_MODE[3:0]				RESERVED		AVG_SYNC	SAVG_EN
R/W-0000b				R/W-00b		R/W-0b	R/W-0b

Table 8-14. Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
15:11	XOR_EN[4:0]	R/W	00000b	Control to enable XOR operation on the ADC conversion result. 00000b = XOR operation is inactive 01111b = Bit-wise XOR operation on the ADC conversion result is active
10	CRC_EN	R/W	0b	Control to enable CRC on the data interface. 0b = CRC module is inactive 1b = CRC module is active
9	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
8	DATA_FORMAT	R/W	0b	Control to select the data format for the ADC conversion result. 0b = Two's-complement format 1b = Straight-binary format
7:4	SAVG_MODE[3:0]	R/W	0000b	Control for the number of samples to be averaged in simple averaging mode. 0000b = 2 samples averaged 0001b = 4 samples averaged 0010b = 8 samples averaged 0011b = 16 samples averaged 0100b = 32 samples averaged 0101b = 64 samples averaged 0110b = 128 samples averaged
3:2	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
1	AVG_SYNC	R/W	0b	Synchronization control for the internal averaging filter. Write 1b to trigger when averaging starts from the subsequent cycle.
0	SAVG_EN	R/W	0b	Control to enable simple averaging. Select the number of samples to be averaged in SAVG_MODE. 0b = Simple averaging is inactive 1b = Simple averaging is active

8.2.7 Register 0Fh (Address = 0x0F) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-11. Register 0Fh

15	14	13	12	11	10	9	8
RESERVED							
R/W-0000000000b							
7	6	5	4	3	2	1	0
RESERVED		TEST_PATT_INCR[1:0]		TEST_PATT_MODE[1:0]		RESERVED	TEST_PATT_EN
R/W-0000000000b		R/W-00b		R/W-00b		R/W-0b	R/W-0b

Table 8-15. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R/W	0000000000b	Reserved. Do not change from the default reset value.
5:4	TEST_PATT_INCR[1:0]	R/W	00b	Increment value for the ramp pattern output. 00b = 1024 01b = 2048 10b = 3072 11b = 4096
3:2	TEST_PATT_MODE[1:0]	R/W	00b	Type of test pattern at the data interface. 00b = ADC outputs constant pattern defined in TEST_PATT_1 in address 0x10 and TEST_PATT_2 in address 0x11 for ADC A and ADC B, respectively 01b = Ramp pattern 10b = Alternate pattern between AAAA and 5555 toggled at each readout
1	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
0	TEST_PATT_EN	R/W	0b	Control to enable digital test pattern for data. 0b = ADC conversion result is launched on the data interface 1b = Digital test pattern is launched on the data interface

8.2.8 Register 10h (Address = 0x10) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-12. Register 10h

15	14	13	12	11	10	9	8
TEST_PATT_1[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TEST_PATT_1[15:0]							
R/W-0000000000000000b							

Table 8-16. Register 10h Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TEST_PATT_1[15:0]	R/W	0000000000000000 000b	16-bit test pattern corresponding to ADC A.

8.2.9 Register 11h (Address = 0x11) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-13. Register 11h

15	14	13	12	11	10	9	8
TEST_PATT_2[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TEST_PATT_2[15:0]							
R/W-0000000000000000b							

Table 8-17. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TEST_PATT_2[15:0]	R/W	000000000000000b	16-bit test pattern corresponding to ADC B.

8.2.10 Register 13h (Address = 0x13) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-14. Register 13h

15	14	13	12	11	10	9	8
RESERVED						CSZ_CONVST_SHORT_EN[2:0]	
R/W-000000b						R/W-000b	
7	6	5	4	3	2	1	0
CSZ_CONVST_SHORT_EN[2:0]	RESERVED						
R/W-000b	R/W-0000000b						

Table 8-18. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:7	CSZ_CONVST_SHORT_EN[2:0]	R/W	000b	Control to enable CS-CONVST short mode. 000b = Normal device operation 101b = CS-CONVST short mode is active
6:0	RESERVED	R/W	0000000b	Reserved. Do not change from the default reset value.

8.3 Register Bank 2

Table 8-19 lists the memory-mapped registers for the register bank 2 registers. Consider all register offset addresses not listed in Table 8-19 as reserved locations and do not modify the register contents.

Table 8-19. Register Map Bank 2

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	Register 09h	RESERVED							
		RESERVED			PD_REFBUF	RESERVED			

Complex bit access types are encoded to fit into small table cells. Table 8-20 shows the codes that are used for access types in this section.

Table 8-20. Register Bank 2 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.1 Register 09h (Address = 0x09) [Reset = 0x0000]

Return to the [Summary Table](#).

Figure 8-15. Register 09h

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED			PD_REFBUF	RESERVED			
R/W-000000000000b			R/W-0b	R/W-0000b			

Table 8-21. Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED	R/W	00000000000b	Reserved. Do not change from the default reset value.
4	PD_REFBUF	R/W	0b	Control to power down the internal reference buffer. 0b = Internal reference buffer is active. 1b = Internal reference buffer is inactive. Use an external reference buffer and connect the external reference to the REFIO and REF_CAP pins.
3:0	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The ADS932x with integrated averaging filters enables a low-latency, precision measurement of DC and AC signals. The following section gives an example circuit and recommendations for using the ADS932x to measure the analog $1V_{pp}$ output of sine-cosine encoders.

9.2 Typical Application

9.2.1 Analog $1V_{pp}$ Sine-Cosine Encoder Interface

The application circuit in [Figure 9-1](#) shows a 2-channel circuit to measure the output of an analog $1V_{pp}$ sine-cosine encoder. Use the [THS4552](#) as the fully differential amplifier that drives the ADS932x.

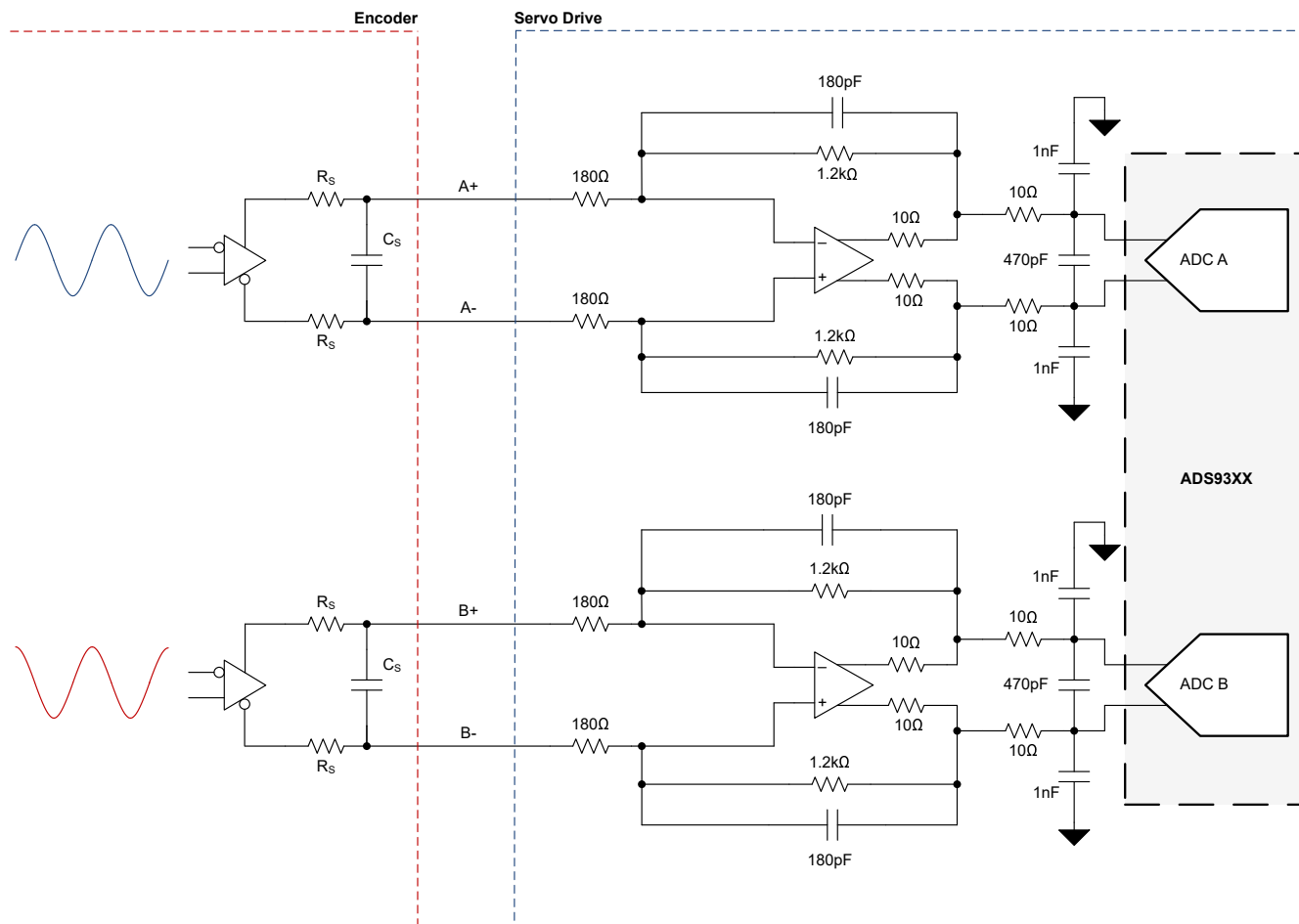


Figure 9-1. Sine-Cosine Encoder Interface Circuit With 500kHz Input Signal Bandwidth

9.2.2 Design Requirements

Table 9-1 lists the parameters for a $1V_{pp}$ sine-cosine encoder interface.

Table 9-1. Design Parameters

PARAMETER	VALUE
ADC resolution	16 bits
SNR	> 90dB
-3dB signal bandwidth	> 500kHz

9.2.3 Detailed Design Procedure

A typical encoder with an analog $1V_{pp}$ output has a maximum signal frequency of 500kHz. The -3dB cutoff frequency of the fully differential amplifier (FDA) circuit is designed for greater than 500kHz. Thus, supporting signals up to the maximum signal frequency of the encoder output. Choose the FDA such that the FDA settles the transient switching load from the sampling capacitor of the ADC within the ADC acquisition time (t_{ACQ}).

The output of a sine-cosine encoder has a typical amplitude of $1V_{pp}$ with a maximum amplitude of $1.2V_{pp}$. The full-scale range of the ADS932x is $\pm V_{REF}$, where the typical value of V_{REF} is 4.096V. To use the input range of the ADC, the gain of the FDA circuit is set to 6.8V/V.

To improve the SNR of the signal chain, the ADS932x offers integrated averaging filters as described in the [Programmable Data Averaging Filter](#) section. The results are shown in Table 9-2, which includes the typical SNR of the circuit with different averaging window sizes.

Table 9-2. THS4552 and ADS932x Data Summary

AVERAGING WINDOW SIZE (Simple Average)	OUTPUT DATA RATE (MSPS)	SNR (dB)	ENOB (Bits)
0	5	93	15.16
2	2.5	95.7	15.60
4	1.25	98.3	16.04
8	0.625	101	16.48
16	0.3125	103.6	16.92
32	0.15625	106.3	17.36
64	0.078125	108.9	17.80
128	0.0390625	111.6	18.25

9.3 Power Supply Recommendations

The ADS932x has three separate power supplies: AVDD, VDD_1V8, and IOVDD. There is no requirement for a specific power-up sequence. The data and configuration digital interfaces are powered by IOVDD. [Figure 9-2](#) shows the decoupling capacitor connections for the respective power supplies. Make sure each power-supply pin has separate decoupling capacitors.

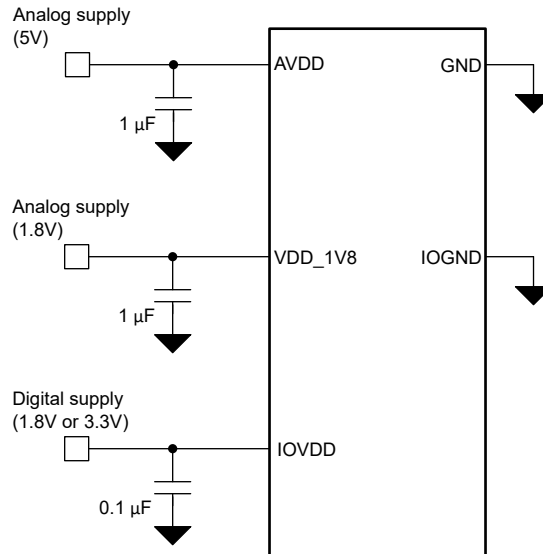


Figure 9-2. Power-Supply Decoupling

9.4 Layout

9.4.1 Layout Guidelines

[Figure 9-3](#) illustrates a board layout example for the ADS932x. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources. Use 1µF ceramic bypass capacitors in close proximity to the analog (AVDD and VDD_1V8), and digital (IOVDD) power-supply pins. Avoid placing vias between the power-supply pins and bypass capacitors. Place the reference decoupling capacitor close to the device REF_CAP and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND and REFM pins to a ground plane using short, low-impedance paths.

9.4.2 Layout Example

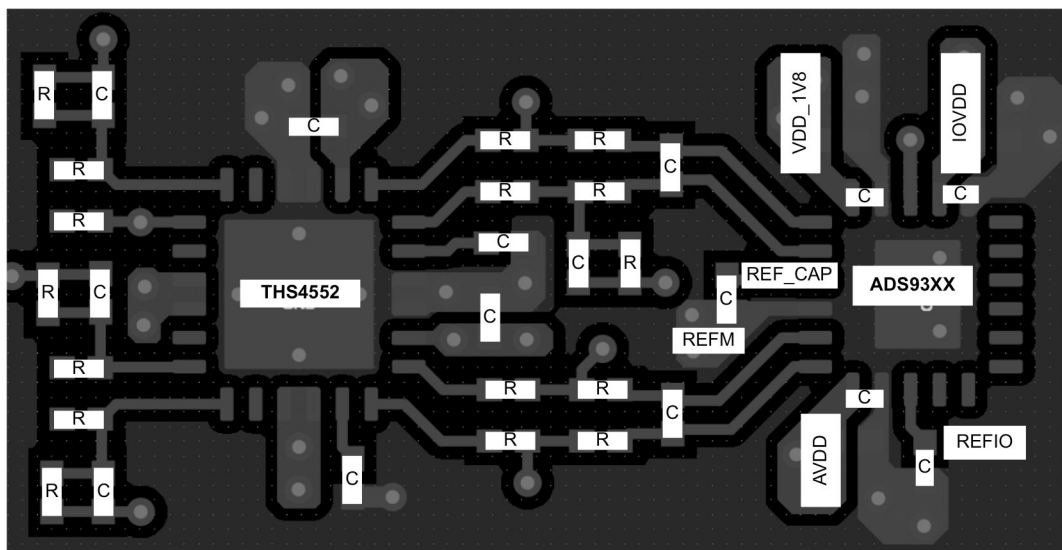


Figure 9-3. Example Layout

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [REF70 2 ppm/°C Maximum Drift, 0.23 ppmp-p 1/f Noise, Precision Voltage Reference data sheet](#)
- Texas Instruments, [THS4552 Dual-Channel, Low-Noise, Precision, 150-MHz, Fully Differential Amplifier data sheet](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

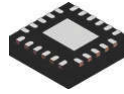
DATE	REVISION	NOTES
May 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Mechanical Data

ADVANCE INFORMATION

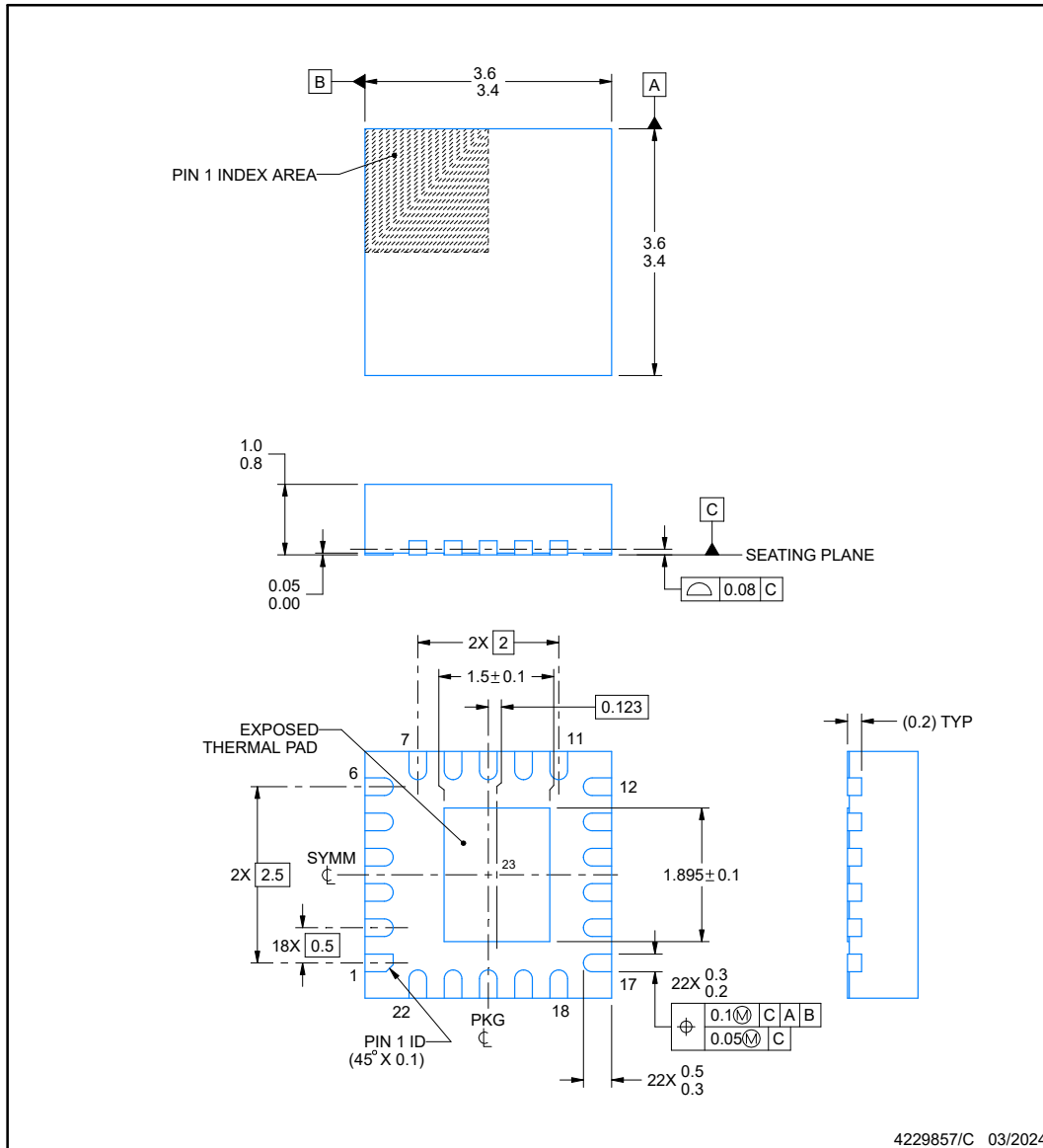


VAE0022A

PACKAGE OUTLINE

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

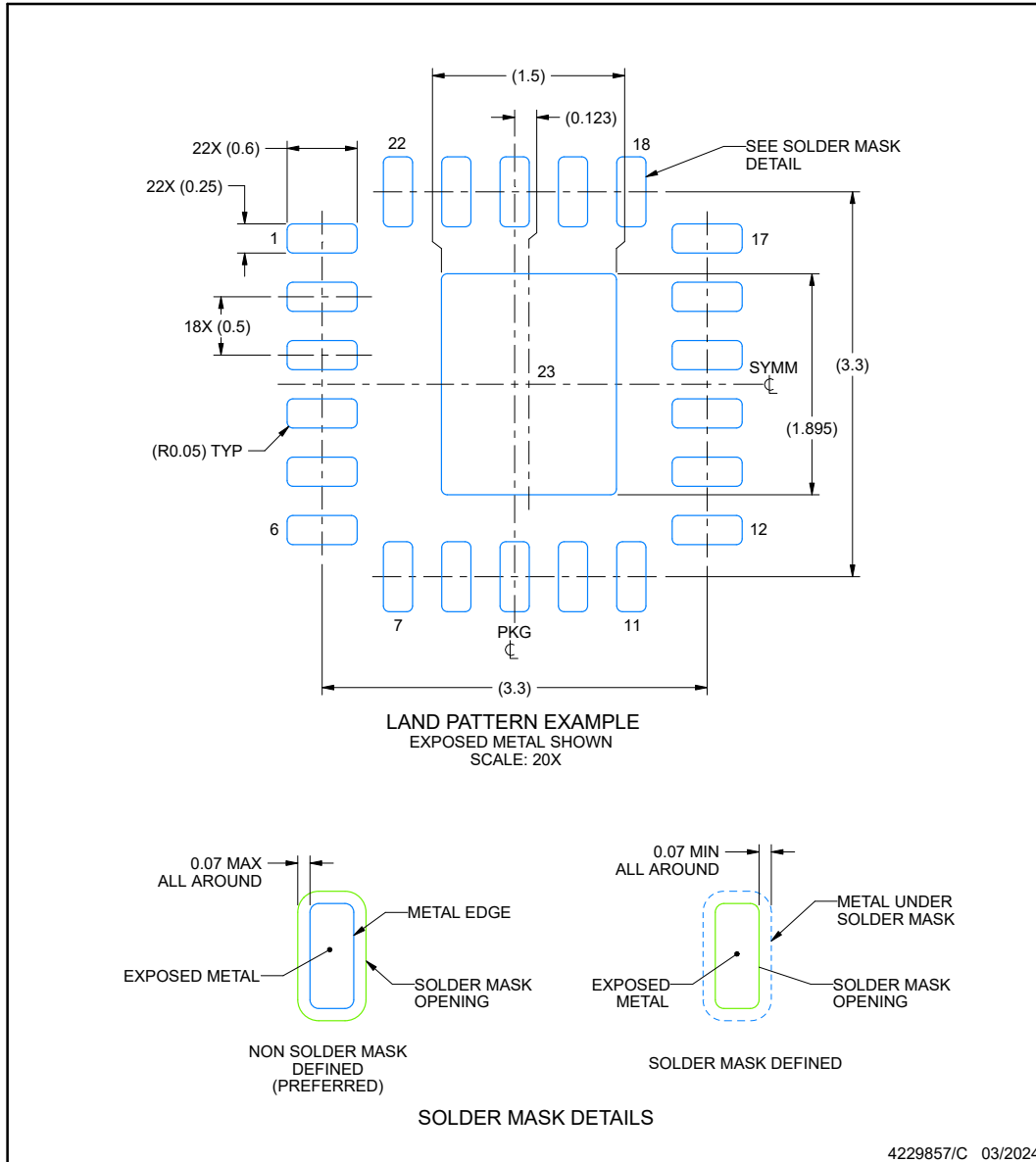
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

VAE0022A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

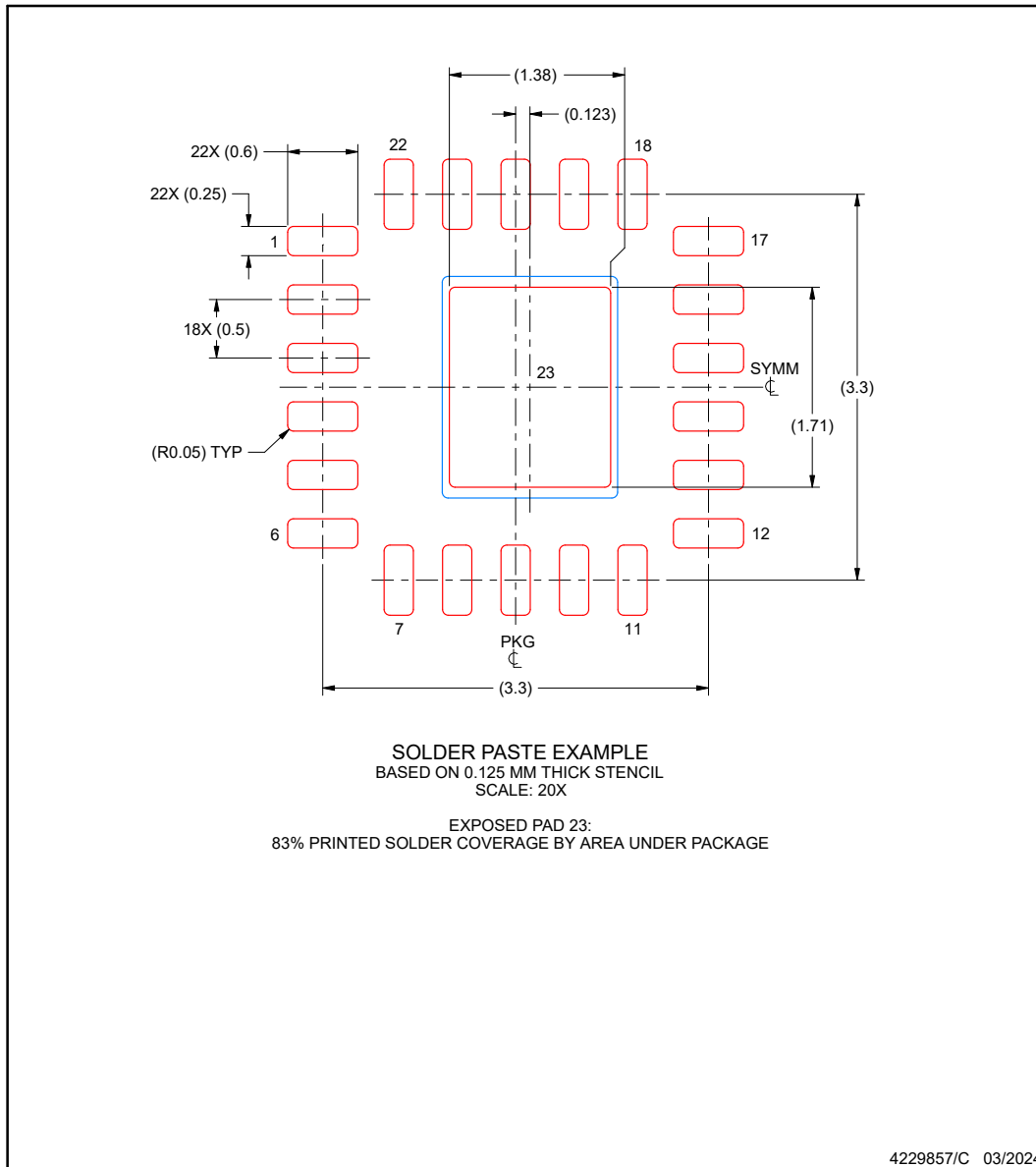
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VAE0022A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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