ADS932x Dual, Simultaneous-Sampling, Small-Size, 16-Bit, 5MSPS SAR ADC

1 Features

- 16-bit SAR ADC family
  - ADS9327: 5MSPS/ch
  - ADS9326: 3MSPS/ch
- Two differential, simultaneously sampled channels
- Supports 5V and 3.3V analog supply operation
- Excellent DC and AC performance:
  - SNR: 93dB at 5MSPS
  - INL: ±1LSB, DNL: ±0.75LSB
- Feature integration:
  - Internal reference
  - Common-mode voltage output buffer
  - Integrated buffer for external reference input
  - Simple data average up to 128 samples
  - Moving data average up to 8 samples
- Configurable serial interface:
  - 2 serial outputs for each ADC channel
  - 1 serial output for each ADC channel
  - 1 serial output for both ADC channels
  - Supports daisy-chain functionality
- 8-bit CRC on serial interface
- Extended temperature range: –40°C to +125°C

2 Applications

- Absolute optical encoders
- Absolute magnetic encoders
- Servo drive position feedback
- Ultrasound scanners
- Programmable DC power supplies, electronic loads
- SONAR

3 Description

The ADS932x is a high-speed, dual, simultaneous-sampling, analog-to-digital converter (ADC) with an integrated reference and reference buffer. The ADS932x has excellent AC performance, which makes the device optimum for wide-bandwidth data acquisition (DAQ) systems.

The device supports an SPI-compatible serial interface. This interface makes the ADS932x easy to pair with a diversity of microcontrollers, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs). This device also supports a data averaging feature that provides an AC performance boost in noisy environments.

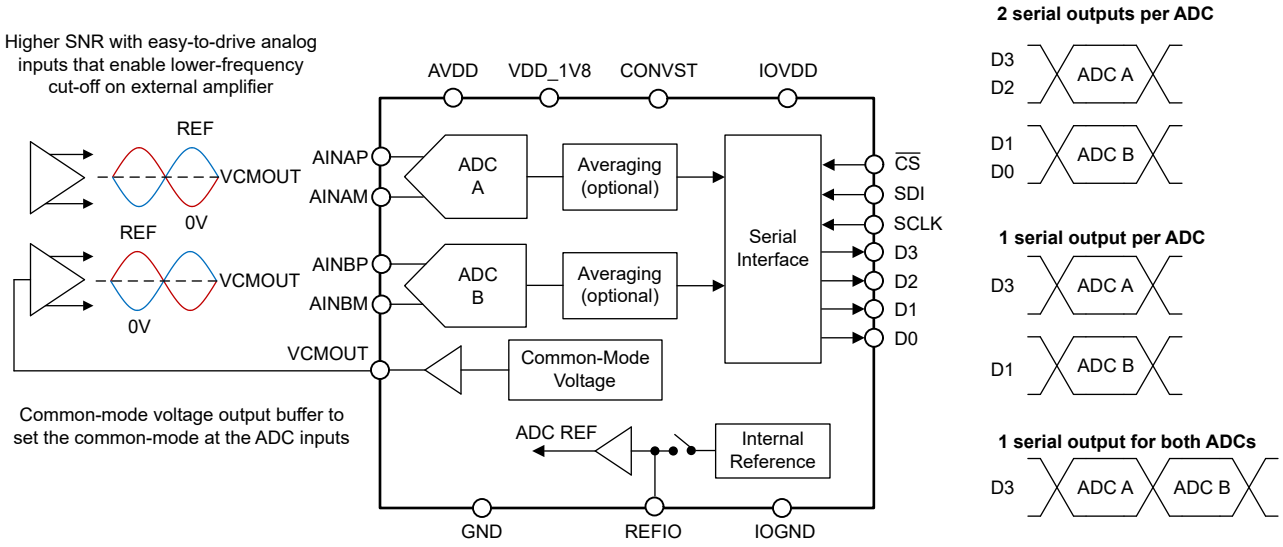
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS932x	VAE (VQFN, 22)	3.5mm × 3.5mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	RESOLUTION	SNR	INL
ADS932x	16 bits	93dB	±1LSB



Device Block Diagram

Table of Contents

4 Device Comparison

RESOLUTION (Bits)	5MSPS	3MSPS
18	ADS9317	ADS9316
16	ADS9327	ADS9326
14	ADS9337	ADS9336
12	ADS9347	ADS9346

5 Pin Configuration and Functions

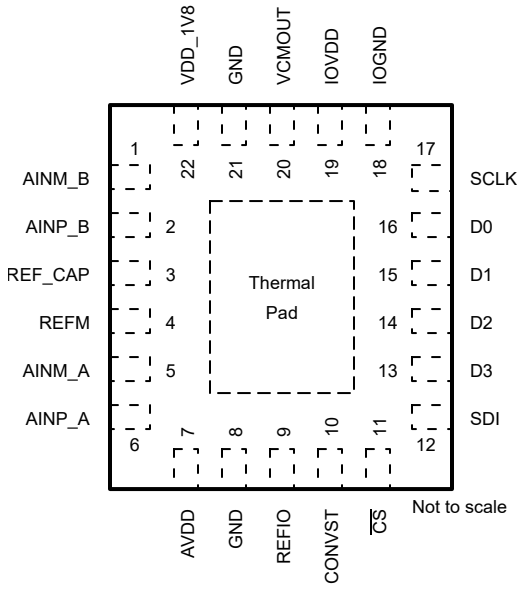


Figure 5-1. VAE Package, 22-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AINM_A	5	I	Negative analog input for ADC A.
AINM_B	1	I	Negative analog input for ADC B.
AINP_A	6	I	Positive analog input for ADC A.
AINP_B	2	I	Positive analog input for ADC B.
AVDD	7	P	5V or 3.3V analog power-supply pin. Connect a 1µF decoupling capacitor between pins 7 and 8.
CONVST	10	I	Conversion start input pin. A CONVST falling edge starts the conversion for ADC A and ADC B.
$\overline{CS}$	11	I	Chip-select input pin; active low. The host and device communicate when $\overline{CS}$ is low. The data output pins go to Hi-Z when $\overline{CS}$ is high.
D0	16	O	Serial communication pin: data output 0.
D1	15	O	Serial communication pin: data output 1.
D2	14	O	Serial communication pin: data output 2.
D3	13	O	Serial communication pin: data output 3.
GND	8, 21	G	Ground.
IOGND	18	G	Ground for IOVDD supply. Connect to GND externally.
IOVDD	19	P	Interface power-supply pin. Connect a 0.1µF decoupling capacitor between pins 18 and 19.
REFIO	9	I/O	Internal reference output. External reference input. Connect a 1µF decoupling capacitor to GND.
REF_CAP	3	O	Internal reference voltage output. Connect a 1µF decoupling capacitor between pins 3 and 4.
REFM	4	G	Negative reference input for the ADCs. Externally connect to the device GND.
SCLK	17	I	Clock input pin for the serial interface.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SDI	12	I	Serial data input pin. This pin programs the device registers.
VCMOUT[2]	20	O	Common-mode voltage output. Use VCMOUT to set the common-mode voltage at the ADC inputs. Connect a 100nF decoupling capacitor to ground.
VDD_1V8	22	P	1.8V analog power-supply pin. Connect a 1µF decoupling capacitor between pins 21 and 22.
Thermal Pad	Pad	P	Exposed thermal pad. Connect to GND.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) Not applicable for PADS9326VAER. Connect a 100nF decoupling capacitor to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD to GND	–0.3	5.5	V
VDD_1V8 to GND	–0.3	2.1	V
IOVDD to IOGND	–0.3	3.7	V
AINAP, AINAM, AINBP, and AINBM to GND	–0.3	AVDD + 0.3	V
REFIO to REFM	–0.3	AVDD + 0.3	V
Digital inputs to IOGND	–0.3	IOVDD + 0.3	V
REFM to GND	–0.3	0.3	V
IOGND to GND	–0.3	0.3	V
Input current to any pin except supply pins(2)	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Limit pin current to 10mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		ADS93x7 VAE (VQFN) 22 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog power supply	AVDD to GND, AVDD = 5V	4.5	5	5.25	V
		AVDD to GND, AVDD = 3.3V	3.1	3.3	3.5	
VDD_1V8	Power supply	VDD_1V8 to GND	1.75	1.8	1.85	V
IOVDD	Interface supply	IOVDD to IOGND	1.75		3.5	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage to the ADC	External reference, AVDD = 5V	2.48	4.096	4.116	V
		External reference, AVDD = 3.3V	2.48	2.5	2.52	
ANALOG INPUTS						
V_{IN}	Absolute input voltage	AINx(1) to GND	0		AVDD	V
FSR	Full-scale input range	(AINP_x – AINM_x)	$-V_{REF}$		V_{REF}	V
V_{CM}	Common-mode input range	(AINP_x + AINM_x) / 2	V_{CMOUT} – 0.04		V_{CMOUT} + 0.04	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

(1) AINx refers to analog inputs AINAP, AINAM, AINBP, and AINBM.

6.5 Electrical Characteristics

at AVDD = 3V to 5.25V, VDD_1V8 = 1.75V to 1.85V, internal reference, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
	Resolution	No missing codes		16		Bits
DNL	Differential nonlinearity		–0.75	±0.4	0.75	LSB
INL	Integral nonlinearity		–1	±0.25	1	LSB
$V_{(OS)}$	Input offset error		–2	±0.4	2	LSB
dV_{OS}/dT	Input offset error thermal drift			0.6	2	µV/°C
	Offset error match	$V_{(OS)}$ (ADC_A – ADC_B)		1		LSB
G_E	Gain error(1)		–0.02	±0.002	0.02	%FSR
dG_E/dT	Gain error thermal drift	Reference buffer on(1)		0.8	2.2	ppm/°C
dG_E/dT	Gain error thermal drift	Reference buffer off(2)		0.25	0.9	ppm/°C
	Gain error match	G_E (ADC_A – ADC_B)		±0.002		%FSR
POWER SUPPLY						
PSRR	Power-supply rejection ratio	100mV_{pp} ripple on AVDD of frequency < 100kHz		80		dB
ANALOG INPUTS						
CSH	Sampling capacitance			18		pF
BW	Analog input bandwidth	–0.1dB input signal		1.5		MHz
I_B	Analog input leakage current	Idle-channel		0.5	1	µA
COMMON-MODE OUTPUT BUFFER						
V_{CMOUT}	Common-mode output voltage	V_{REF} = 4.096V	2.2	2.24	2.28	V
	Output current drive		0		15	µA
INTERNAL REFERENCE						
V_{REF}	Voltage on REFIO pin (configured as output)	1µF capacitor on REFIO pin, T_A = 25°C	V_{REF} – 0.005	V_{REF}	V_{REF} + 0.005	V
	Reference temperature drift			5	15	ppm/°C
DIGITAL INPUTS						
V_{IL}	Input low logic level		–0.1		0.5	V
V_{IH}	Input high logic level		IOVDD – 0.5		IOVDD	V
DIGITAL OUTPUTS						
V_{OL}	Output low logic level	I_{OL} = 200µA sink	0		0.4	V
V_{OH}	Output high logic level	I_{OH} = 200µA source	IOVDD – 0.4		IOVDD	V
SAMPLING DYNAMICS						
t_A	Aperture delay			4		ns
	Aperture mismatch			100		ps
t_{JITTER}	Aperture jitter			1		ps

(1) These specifications include full temperature range variation but not the error contribution from internal reference.
(2) For more details, see External Reference with External Reference Buffer.

6.6 Electrical Characteristics: AVDD = 5V

at AVDD = 4.75V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	f_{IN} = 2kHz	90.5	92.9		dB
		f_{IN} = 1MHz		91.4		
SNR	Signal-to-noise ratio	f_{IN} = 2kHz	90.8	93		dB
		f_{IN} = 1MHz		91.5		
THD	Total harmonic distortion	f_{IN} = 2kHz		–115		dB
		f_{IN} = 1MHz		–100		
SFDR	Spurious-free dynamic range	f_{IN} = 2kHz		115		dB
		f_{IN} = 1MHz		100		
CMRR	Common-mode rejection ratio	f_{IN} = dc to 1kHz, V_{IN} = 50mV_{PP}		70		dB
	Channel-to-channel isolation	V_{IN_ADCA} = 0V, f_{IN_ADCB} = 10kHz at 100% FSR		–110		dB
POWER SUPPLY						
I_{AVDD}	Supply current from AVDD	Full-speed (ADS9327)		4.2	4.9	mA
		Full-speed (ADS9326)		2.8	3.1	
		No conversion (idle) (ADS9327)		1.5	1.8	
		No conversion (idle) (ADS9326)		1.35	1.65	
		Power-down		0.4	0.8	
I_{VDD_1V8}	Supply current from VDD_1V8	Full-speed (ADS9327)		9.5	10.3	mA
		Full-speed (ADS9326)		6.9	7.4	
		No conversion (idle) (ADS9327)		6.4	7.2	
		No conversion (idle) (ADS9326)		4.9	5.5	
		Power-down		0.9	1.1	
I_{IOVDD}	Supply current from IOVDD	Full-speed (ADS9327), C_{LOAD} = 10pF		2.7	3	mA
		Full-speed (ADS9326), C_{LOAD} = 10pF		1.6	1.8	
		No conversion (idle), C_{LOAD} = 10pF		0.25	0.35	
		Power-down, C_{LOAD} = 10pF		0.25	0.35	

6.7 Electrical Characteristics: AVDD = 3.3V

at AVDD = 3.1V to 3.5V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal V_{REF} = 2.5V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	f_{IN} = 2kHz	87.9	90.3		dB
		f_{IN} = 1MHz		88.4		
SNR	Signal-to-noise ratio	f_{IN} = 2kHz	88.1	90.4		dB
		f_{IN} = 1MHz		88.5		
THD	Total harmonic distortion	f_{IN} = 2kHz		–112		dB
		f_{IN} = 1MHz		–100		
SFDR	Spurious-free dynamic range	f_{IN} = 2kHz		112		dB
		f_{IN} = 1MHz		100		
CMRR	Common-mode rejection ratio	f_{IN} = dc to 1kHz, V_{IN} = 50mV_{PP}		70		dB
	Channel-to-channel isolation	V_{IN_ADCA} = 0V, f_{IN_ADCB} = 10kHz at 100% FSR		–110		dB
POWER SUPPLY						
I_{AVDD}	Supply current from AVDD	Full-speed (ADS9327)		3	3.4	mA
		Full-speed (ADS9326)		2.1	2.5	
		No conversion (idle) (ADS9327)		1.2	1.5	
		No conversion (idle) (ADS9326)		1.2	1.5	
		Power-down		0.4	0.8	
I_{VDD_1V8}	Supply current from VDD_1V8	Full-speed (ADS9327)		9.5	10.3	mA
		Full-speed (ADS9326)		6.9	7.4	
		No conversion (idle) (ADS9327)		6.4	7.2	
		No conversion (idle) (ADS9326)		4.9	5.5	
		Power-down		0.9	1.1	
I_{IOVDD}	Supply current from IOVDD	Full-speed (ADS9327), C_{LOAD} = 10pF		2.7	3	mA
		Full-speed (ADS9326), C_{LOAD} = 10pF		1.6	1.8	
		No conversion (idle), C_{LOAD} = 10pF		0.25	0.35	
		Power-down, C_{LOAD} = 10pF		0.25	0.35	

6.8 Timing Requirements

at AVDD = 3V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal reference, and maximum throughput (unless otherwise noted); C_L = 10pF; minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

			MIN	MAX	UNIT
CONVERSION CYCLE					
f_{CYCLE}	Sampling frequency	ADS9327		5	MHz
		ADS9326		3	
t_{CYCLE}	ADC cycle-time period		$1/f_{CYCLE}$		s
f_{CLK}	Maximum SCLK frequency			80	MHz
t_{CLK}	Minimum SCLK time period		12.5		ns
t_{ACQ}	Acquisition time	ADS9327	70		ns
		ADS9326	133.33		
t_{PH_CV}	CONVST high time		10		ns
t_{PL_CV}	CONVST low time		10		ns
SPI INTERFACE TIMINGS					
t_{hi_CSZ}	Pulse duration: $\overline{CS}$ high		5		ns
t_{PH_CK}	SCLK high time		0.40	0.60	t_{CLK}
t_{PL_CK}	SCLK low time		0.40	0.60	t_{CLK}
t_{d_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK rising edge		17		ns
t_{su_CKDI}	Setup time: SDI data valid to the corresponding SCLK rising edge		3		ns
t_{ht_CKDI}	Hold time: SCLK rising edge to corresponding data valid on SDI		1		ns
t_{ht_CVCS}	Hold time: CONVST falling edge to $\overline{CS}$ falling edge		5		ns
t_{ht_CKCS}	Hold time: last SCLK falling edge to $\overline{CS}$ rising		10		ns

6.9 Switching Characteristics

at AVDD = 3V to 5.25V, VDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal reference, and maximum throughput (unless otherwise noted); C_L = 10pF; minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
CONVERSION CYCLE					
t_{CONV}	ADC conversion time	ADS9327		130	ns
		ADS9326		200	
RESET					
t_{PU}	Power-up time for device			100	ms
SPI INTERFACE TIMINGS					
t_{den_CSDO}	Time delay: $\overline{CS}$ falling edge to data valid on SDO			16	ns
t_{dz_CSDO}	Time delay: $\overline{CS}$ rising edge to SDO going Hi-Z			7.5	ns
t_{ht_CKDO}	Hold time: SCLK launch edge to previous data valid on SDO		7.6		ns
t_{d_CKDO}	Time delay: SCLK launch edge to corresponding data valid on SDO			17	ns

6.10 Timing Diagrams

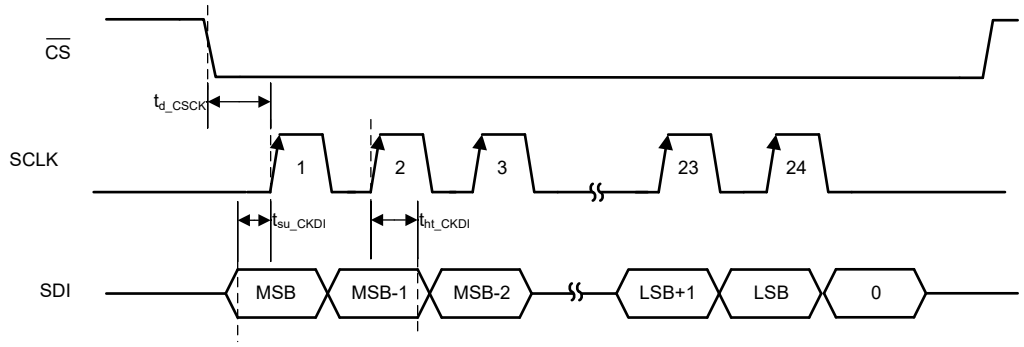


Figure 6-1. SDI Timing for Register Operations

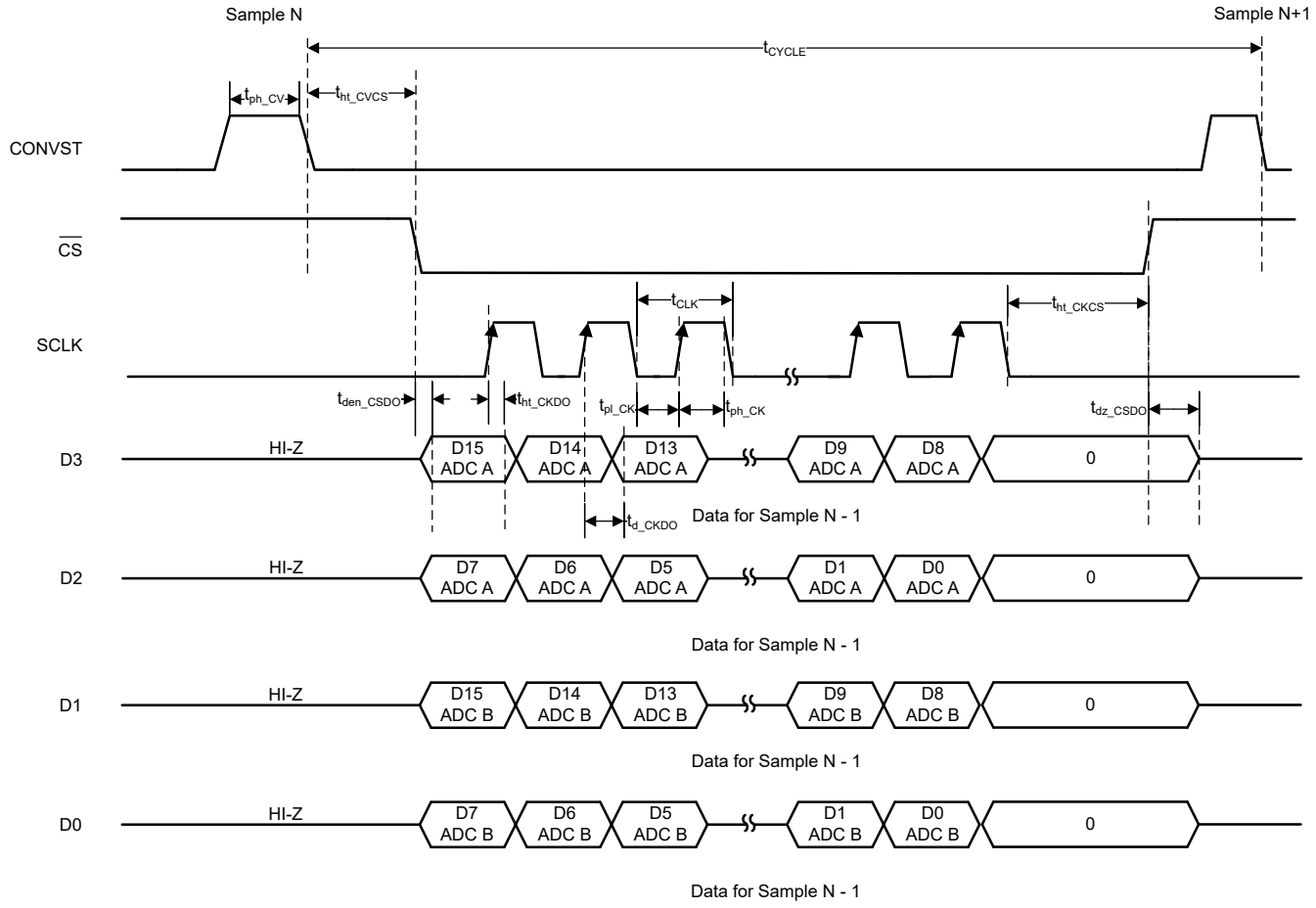


Figure 6-2. Conversion Cycle Timing: 4-Lane Default Operation

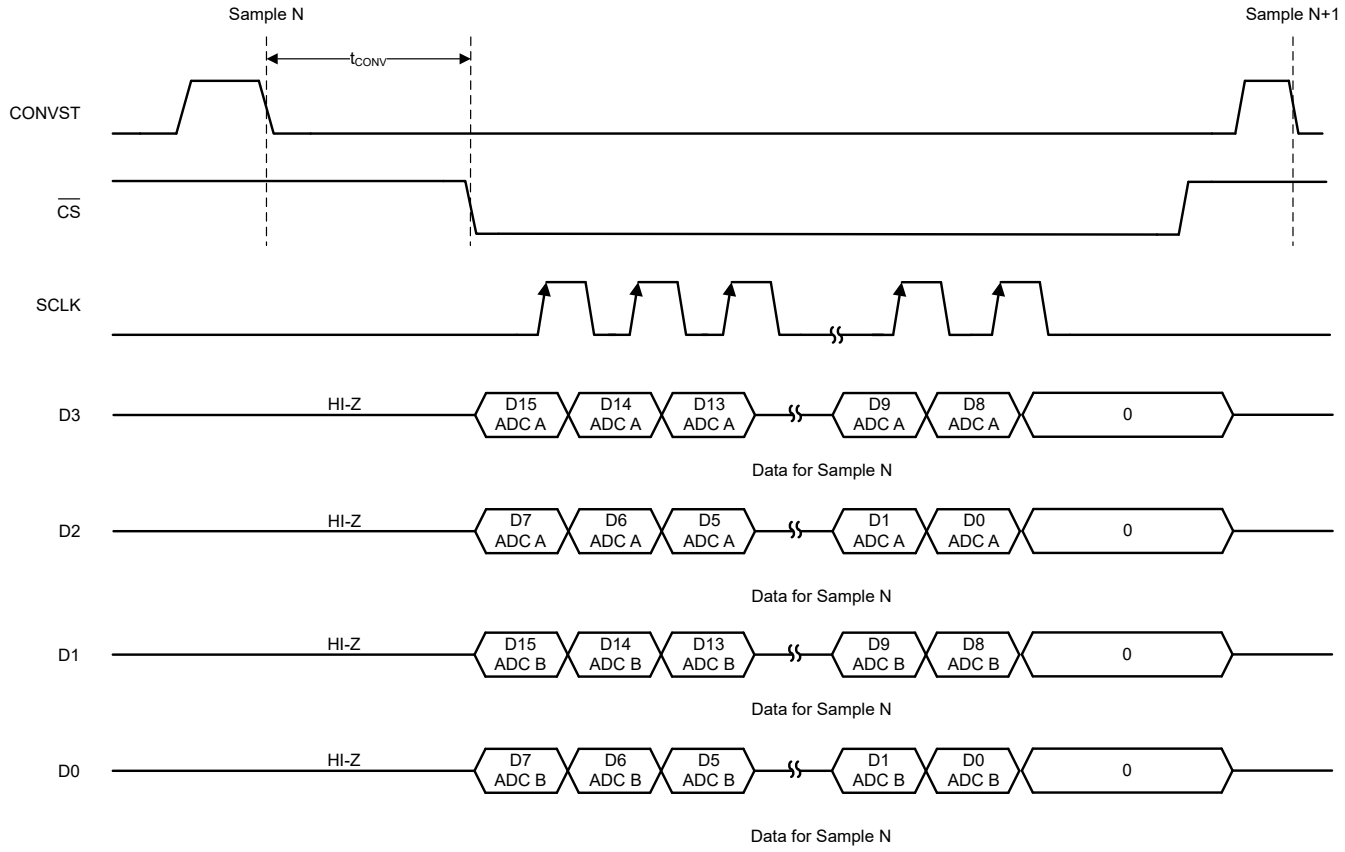


Figure 6-3. Conversion Cycle Timing: 4-Lane Low-Latency Mode

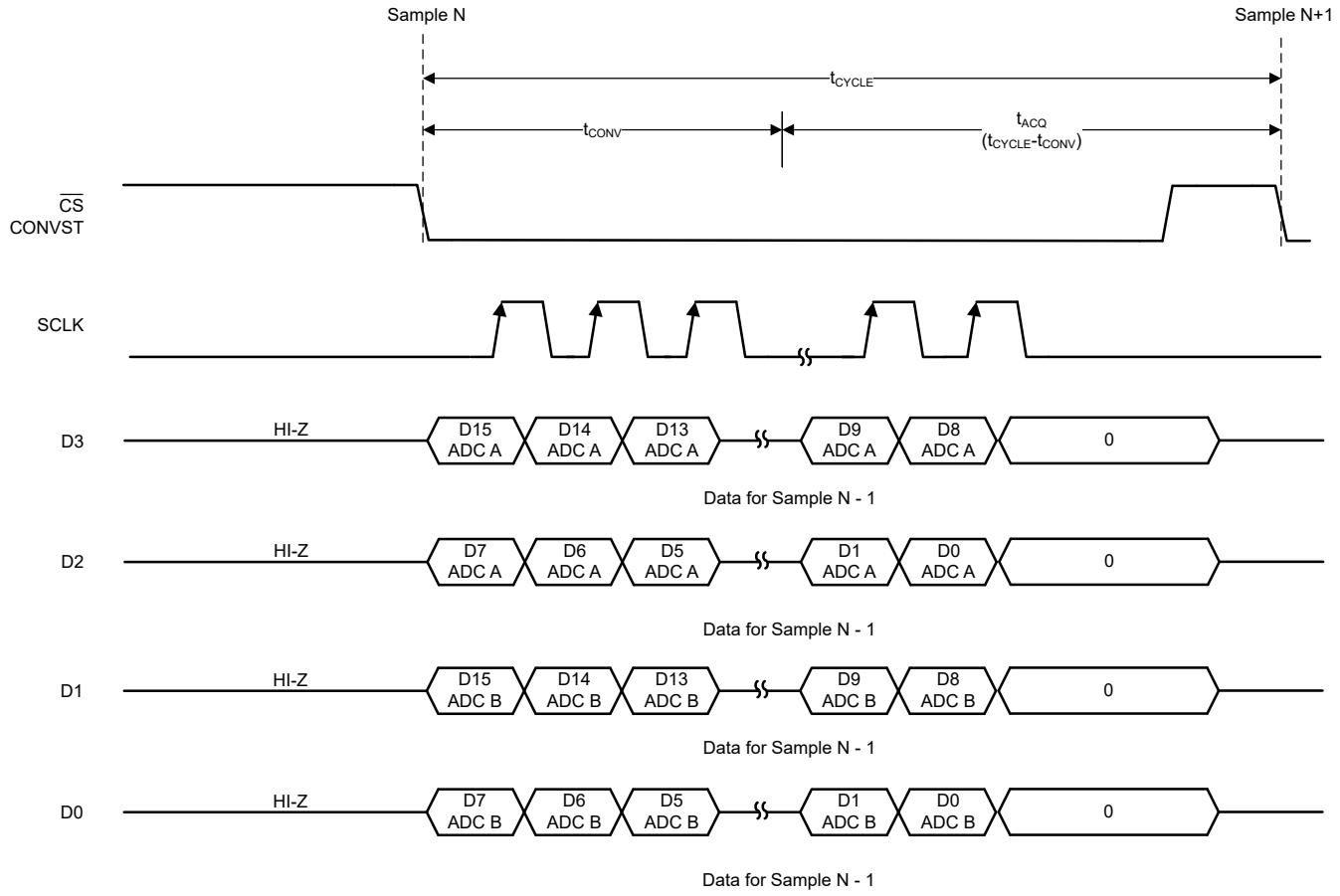
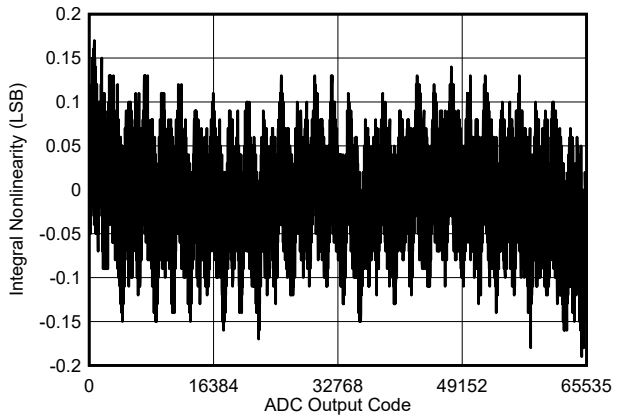


Figure 6-4. Conversion Cycle Timing: 4-Lane Mode with $\overline{CS}$ and CONVST Shorted

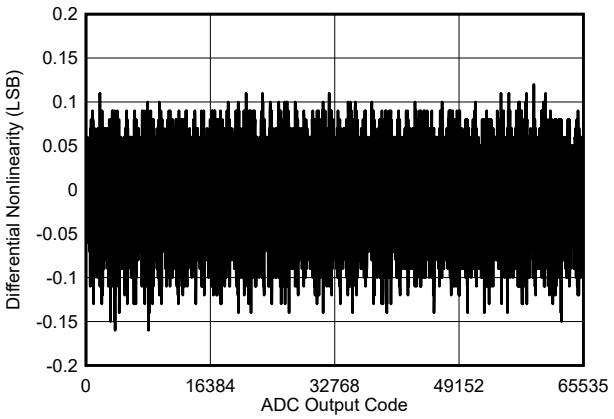
6.11 Typical Characteristics

at T_A = 25°C, AVDD = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



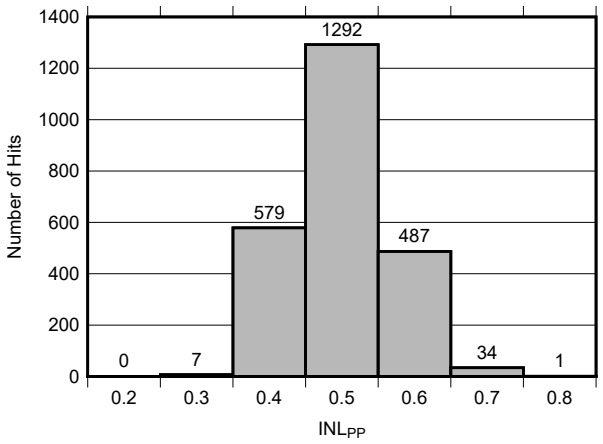
Typical INL = ±0.2LSB

Figure 6-5. Typical INL



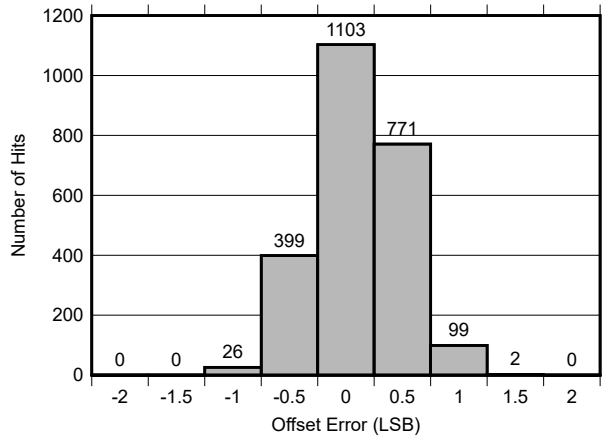
Typical DNL = ±0.15LSB

Figure 6-6. Typical DNL



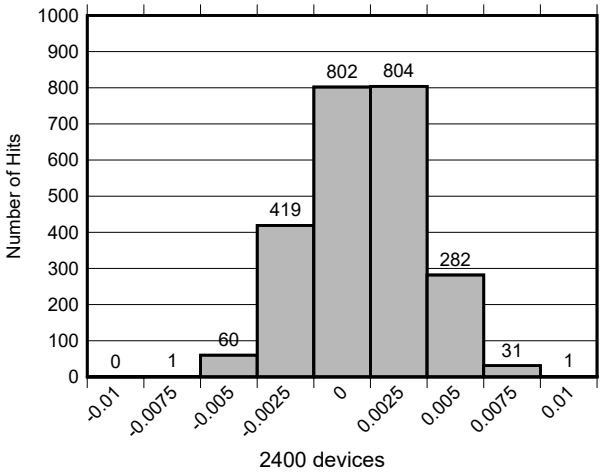
2400 devices

Figure 6-7. Typical INL Distribution (LSB)



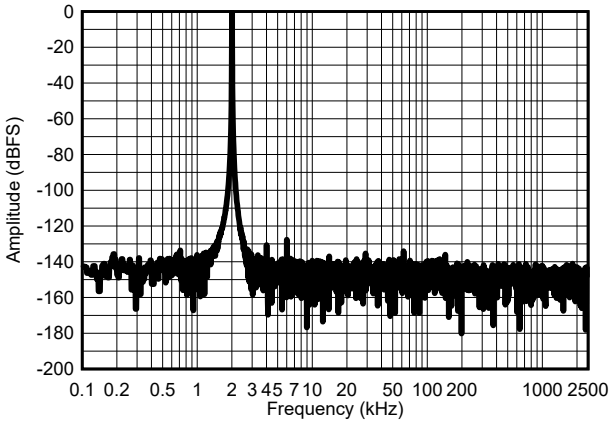
2400 devices

Figure 6-8. Typical Offset Error Distribution (LSB)



2400 devices

Figure 6-9. Typical Gain Error Distribution (% FSR)

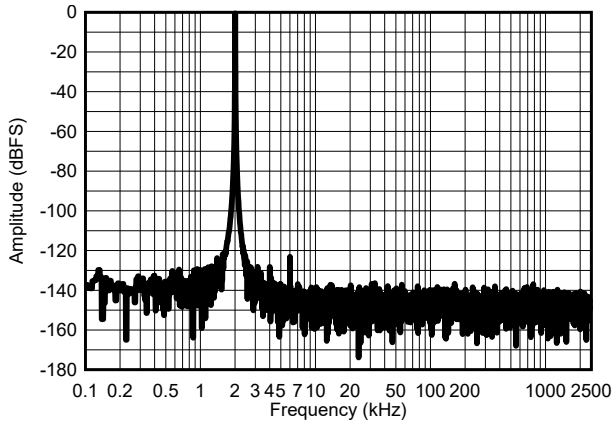


f_{IN} = 2kHz, SNR = 93dB, THD = −120dB

Figure 6-10. Typical FFT for f_{IN} = 2kHz

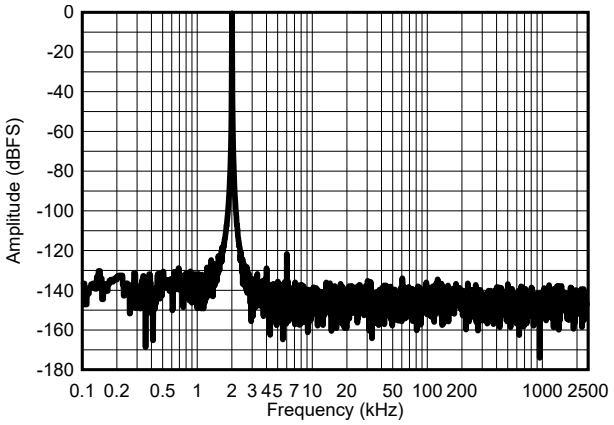
6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



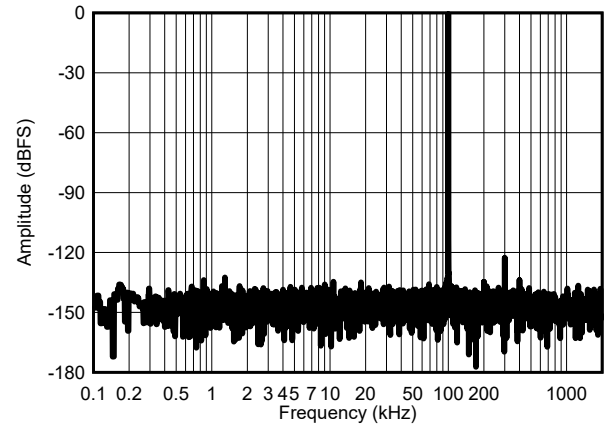
f_{IN} = 2kHz, SNR = 91.5dB, THD = −119dB

Figure 6-11. Typical FFT for f_{IN} = 2kHz, external V_{REF} = 3.3V



f_{IN} = 2kHz, SNR = 90.4dB, THD = −117dB

Figure 6-12. Typical FFT for f_{IN} = 2kHz, external V_{REF} = 2.5V



f_{IN} = 2kHz, SNR = 92.6dB, THD = −115dB

Figure 6-13. Typical FFT for f_{IN} = 100kHz

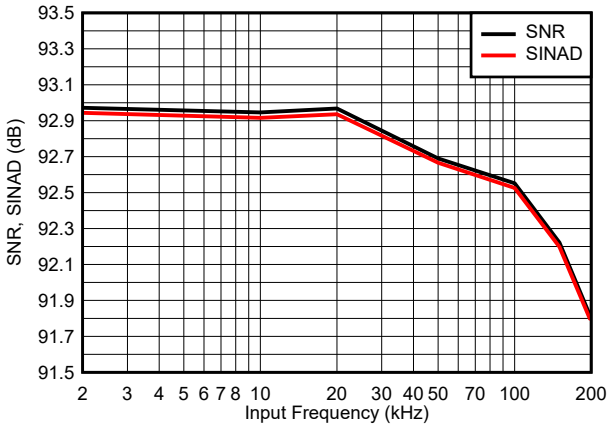


Figure 6-14. SNR and SINAD vs Input Signal Frequency

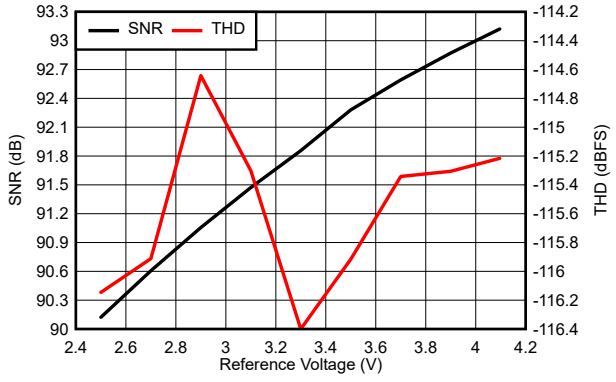


Figure 6-15. SNR and THD vs Reference Voltage

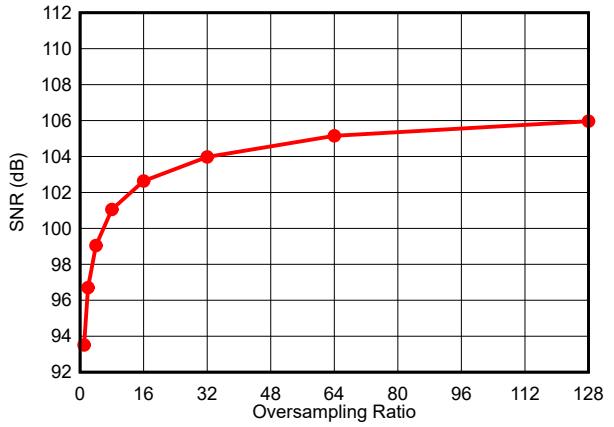


Figure 6-16. SNR vs Simple Average Oversampling Ratio

6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

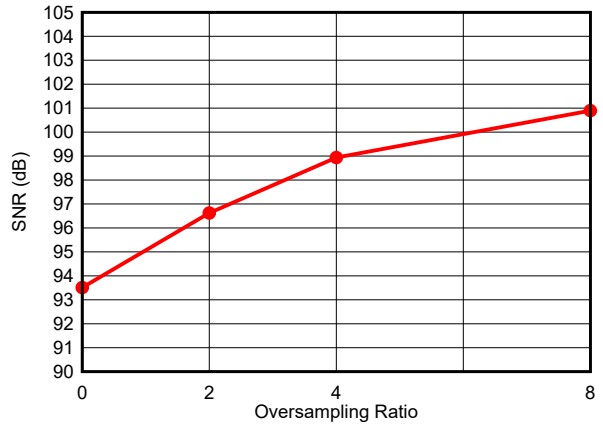


Figure 6-17. SNR vs Moving Average Oversampling Ratio

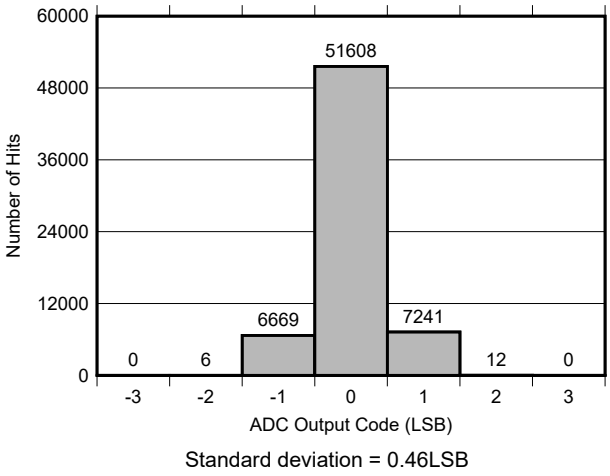


Figure 6-18. DC Input Histogram

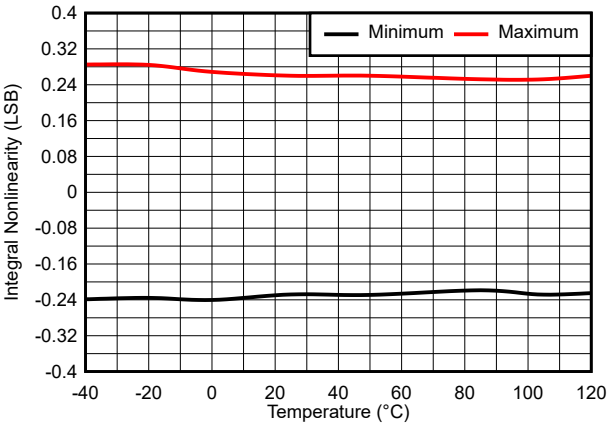


Figure 6-19. INL vs Temperature

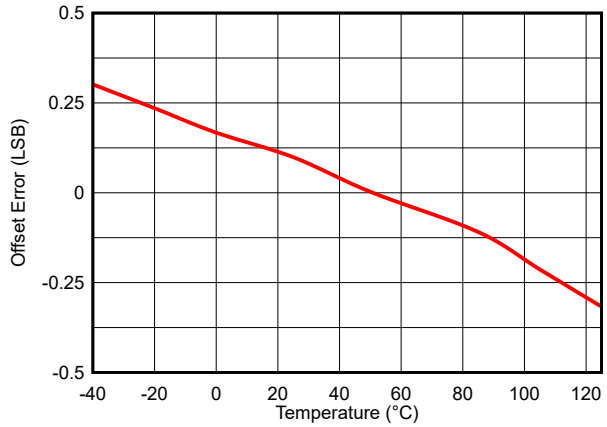


Figure 6-20. Offset Error vs Temperature

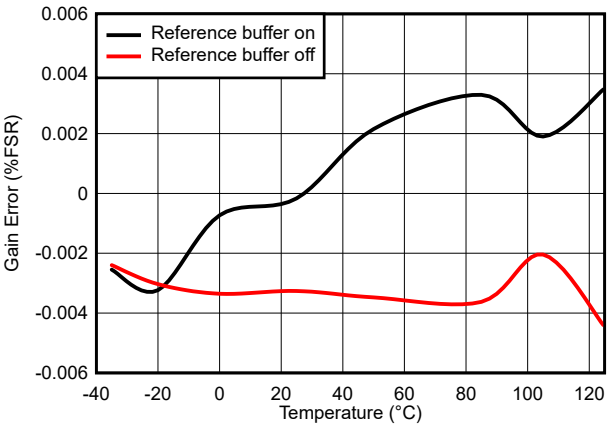


Figure 6-21. Gain Error vs Temperature

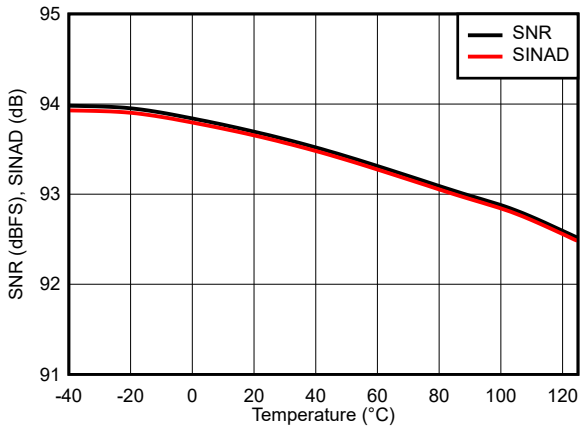


Figure 6-22. SNR and SINAD vs Temperature

6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

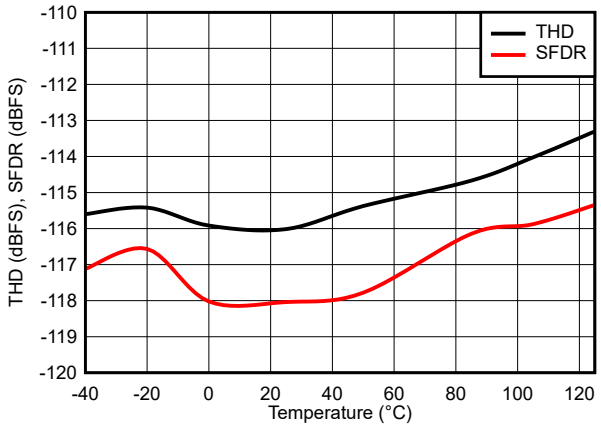


Figure 6-23. THD and SFDR vs Temperature

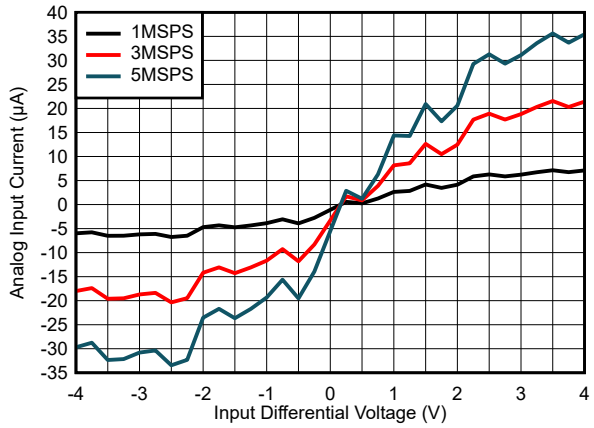


Figure 6-24. Analog Input Current vs Input Differential Voltage

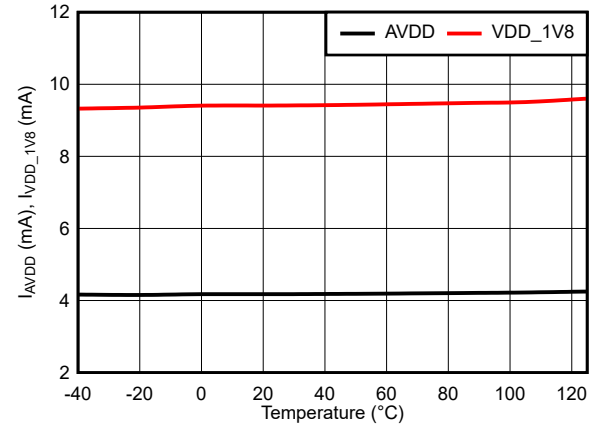


Figure 6-25. AVDD and VDD_1V8 Current vs Temperature

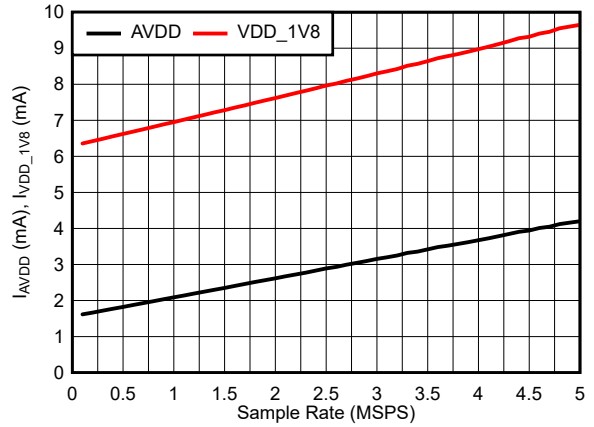


Figure 6-26. AVDD and VDD_1V8 Current vs Sample Rate

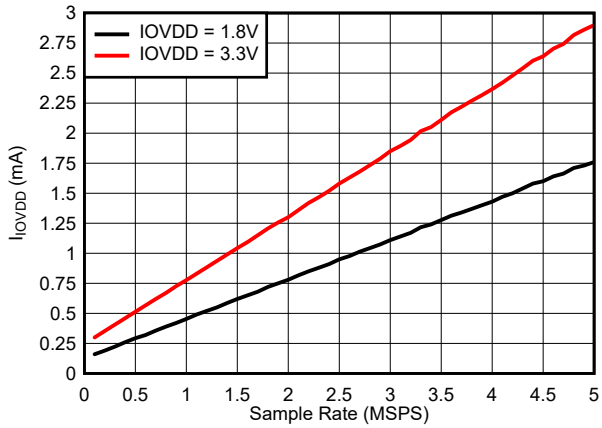


Figure 6-27. IOVDD Current vs Sample Rate

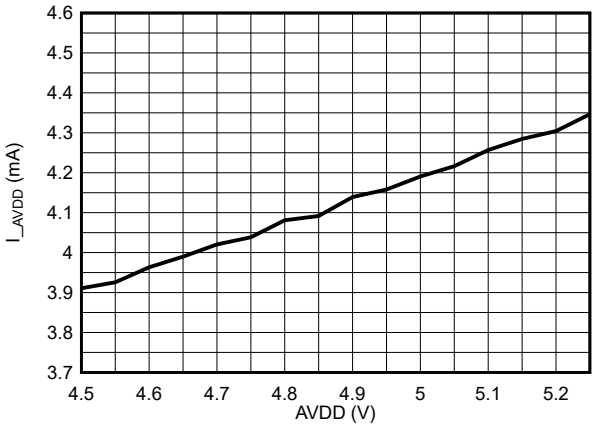


Figure 6-28. AVDD Current vs AVDD Voltage with 4.096V Reference

6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

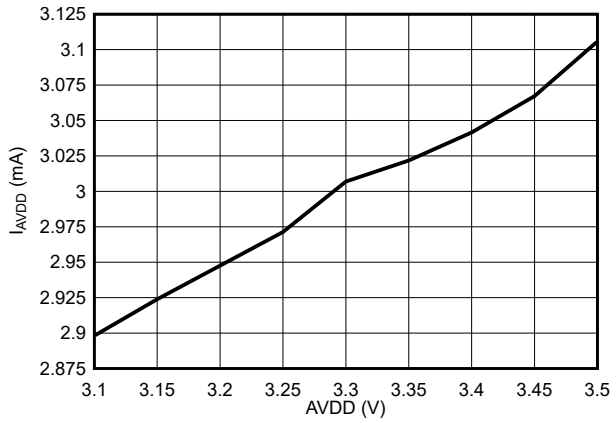


Figure 6-29. AVDD Current vs AVDD Voltage with 2.5V Reference

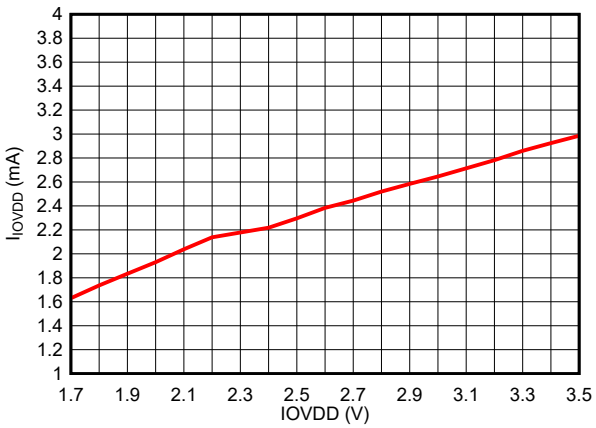


Figure 6-30. IOVDD Current vs IOVDD Voltage

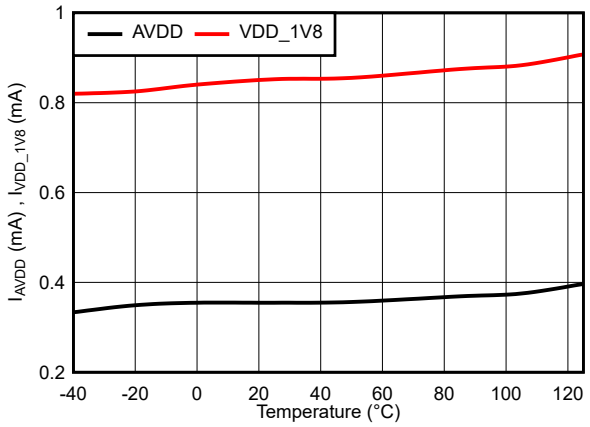


Figure 6-31. AVDD and VDD_1V8 Power-Down Current vs Temperature

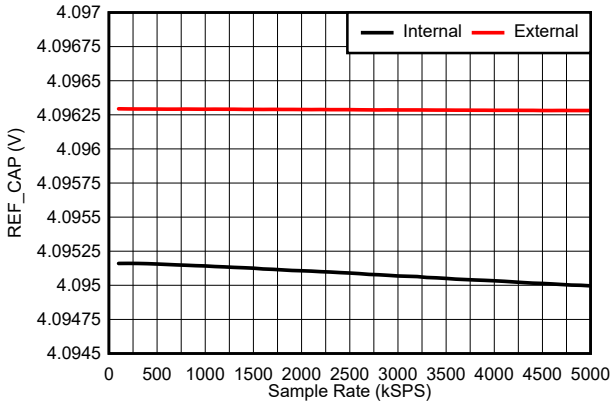


Figure 6-32. REF_CAP vs Sample Rate with 4.096V Reference

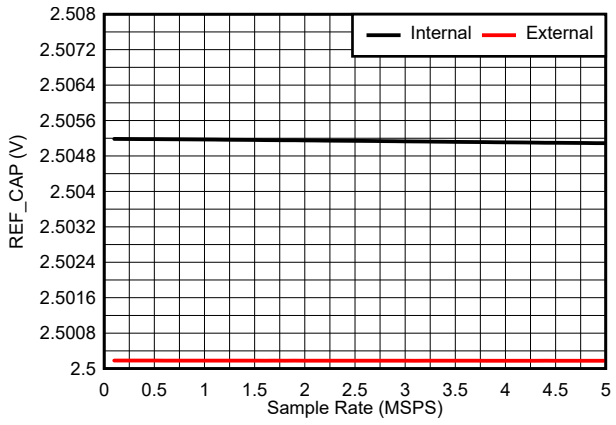


Figure 6-33. REF_CAP vs Sample Rate with 2.5V Reference

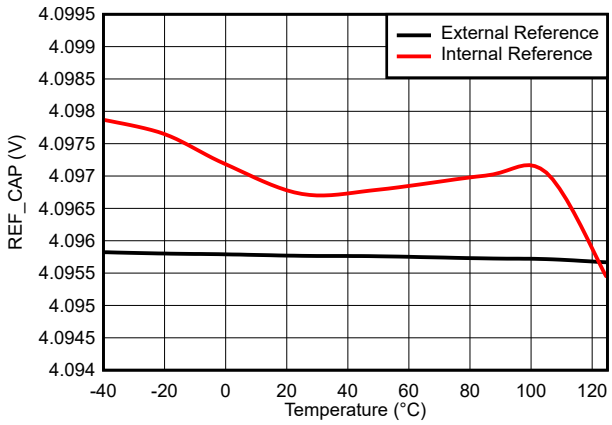


Figure 6-34. REF_CAP Voltage vs Temperature

6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

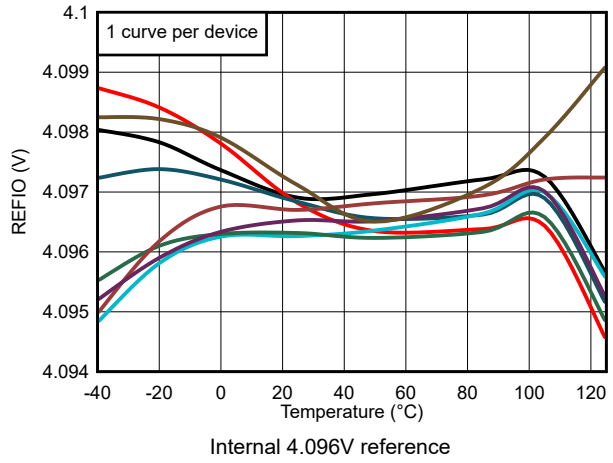


Figure 6-35. REFIO Voltage vs Temperature with 4.096V Reference

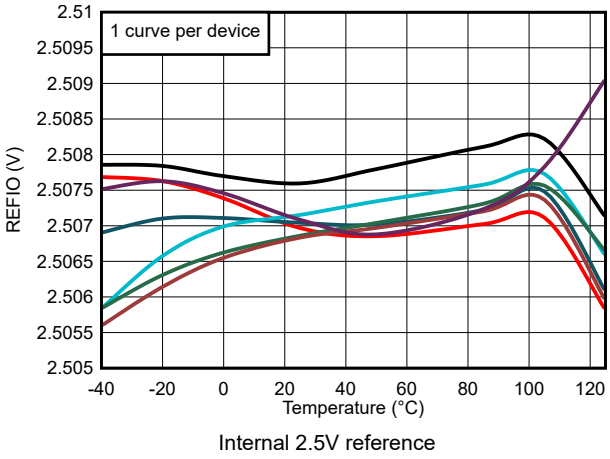


Figure 6-36. REFIO Voltage vs Temperature with 2.5V Reference

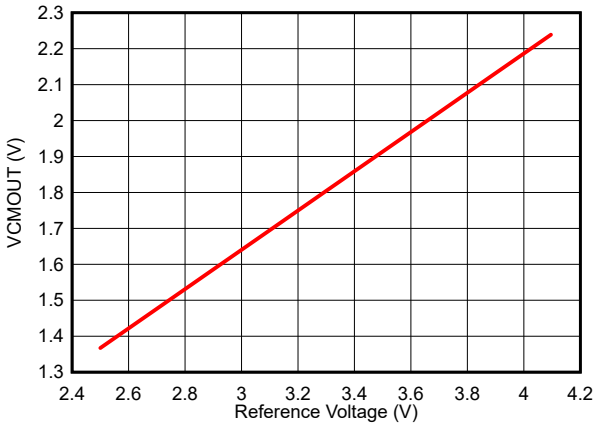


Figure 6-37. VCMOUT Voltage vs Reference Voltage

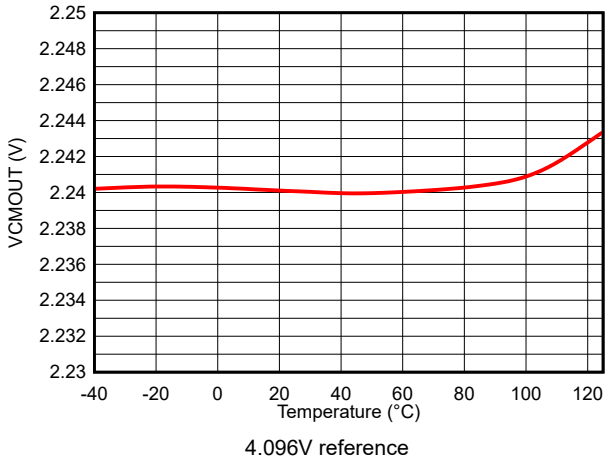


Figure 6-38. VCMOUT Voltage vs Temperature with 4.096V Reference

6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

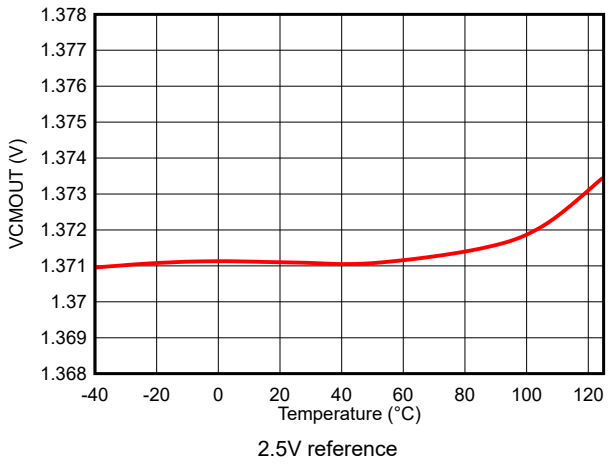


Figure 6-39. VCMOUT Voltage vs Temperature with 2.5V Reference

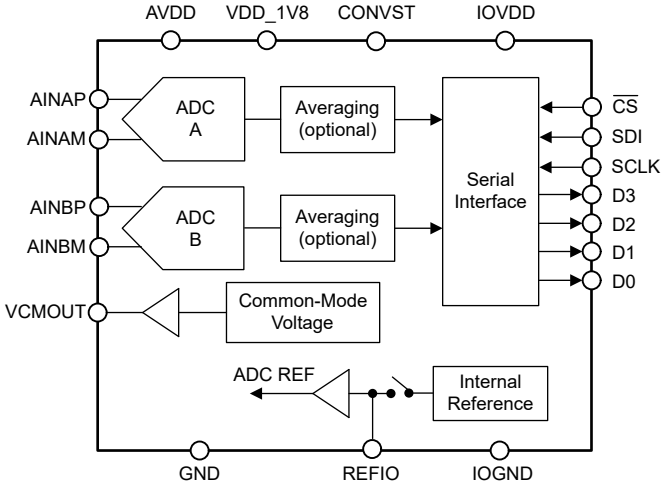
7 Detailed Description

7.1 Overview

The ADS932x (ADS9326, ADS9327) is a family of 16-bit, dual, simultaneous-sampling, analog-to-digital converters (ADCs) with an integrated reference. The ADS932x supports fully differential analog input signals and features built-in data averaging.

The ADS932x provides a simple, serial interface to the host controller and operates over a wide range of analog and digital power supplies. The serial interface is compatible with traditional SPI protocols and supports daisy-chain connection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs

This device supports unipolar, fully differential, analog input signals. Figure 7-1 shows a small-signal equivalent circuit of the sample-and-hold circuit. Each sampling switch is represented by a resistance (R_{S1} and R_{S2}, typically 25Ω) in series with sampling switches (SW_1 and SW_2). The sampling capacitors, C_{S1} and C_{S2}, are typically 18pF.

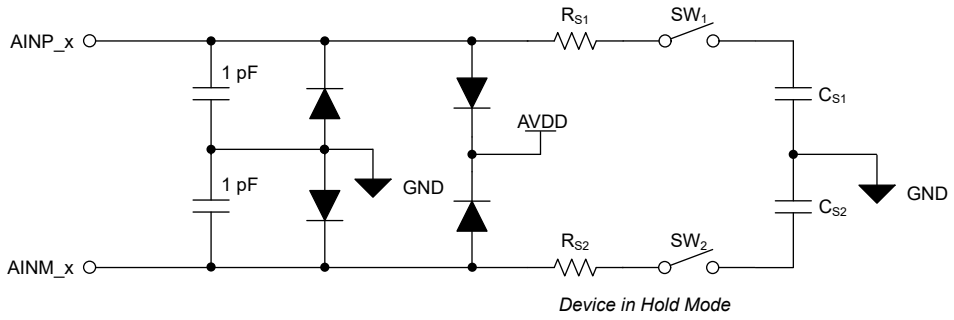


Figure 7-1. Analog Inputs

7.3.2 Reference

The ADS932x has a precision, low-drift voltage reference internal to the device. For best performance, filter the internal reference noise by connecting a 1µF ceramic bypass capacitor to the REFIO pin. On power-up, as described in Table 7-1, the reference source is selected by writing to PD_REF in address 0x0C in register bank 1.

Table 7-1. Reference Source Selection

PD_REF REGISTER VALUE	ADC REFERENCE SOURCE
10b	Internal reference is active.
11b	Internal reference is inactive. Force an external reference with REFIO (pin 9).

7.3.2.1 Internal Reference

The ADS932x features an internal reference voltage with a nominal output voltage of 4.096V when AVDD = 5V and 2.5V when AVDD = 3.3V. To enable the internal reference, write 10b to PD_REF in register bank 1. As shown in Figure 7-2 and Figure 7-3, place a minimum 1µF decoupling capacitor between the REFIO and REFM pins.

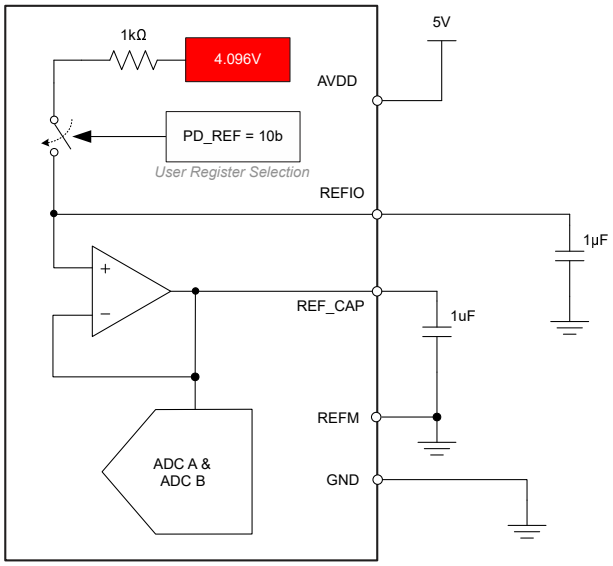


Figure 7-2. Internal Reference: AVDD = 5V

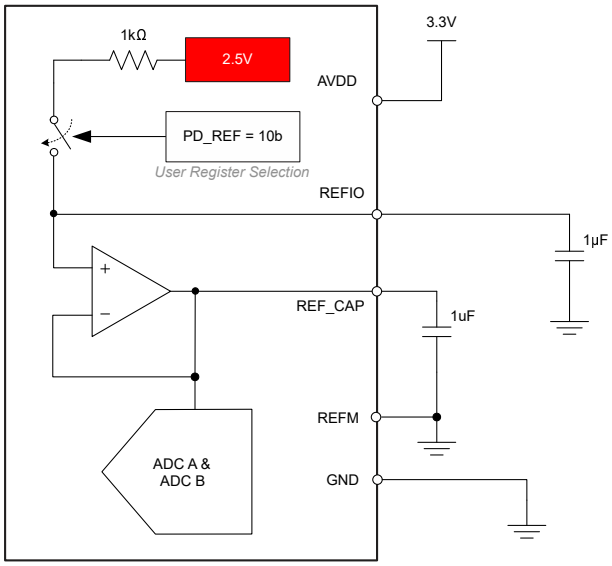


Figure 7-3. Internal Reference: AVDD = 3.3V

7.3.2.1.1 Selectable Internal Reference with 5V AVDD

When AVDD = 5V, the ADS932x offers a selectable internal reference value of 4.096V, 3.3V, or 2.5V. Select the internal reference value by writing to INT_REF_MODE in register bank 1 as shown in Table 7-2.

Table 7-2. Internal Reference Selection when AVDD = 5V

Internal Reference Value	INT_REF_MODE
4.096V	0b
3.3V	11b
2.5V	1b

1. This section is not applicable for PADS9326VAER.

7.3.2.2 External Reference

Connect an external reference voltage, as shown in Figure 7-4, at the REFIO pin with an appropriate decoupling capacitor placed between the REFIO and REFM pins. For improved thermal drift performance, use the REF7040. To disable the internal reference, set PD_REF = 11b in address 0x0C in register bank 1 as described in the *Reference* section. The REFIO pin has electrostatic discharge (ESD) protection diodes connected to the AVDD and REFM pins.

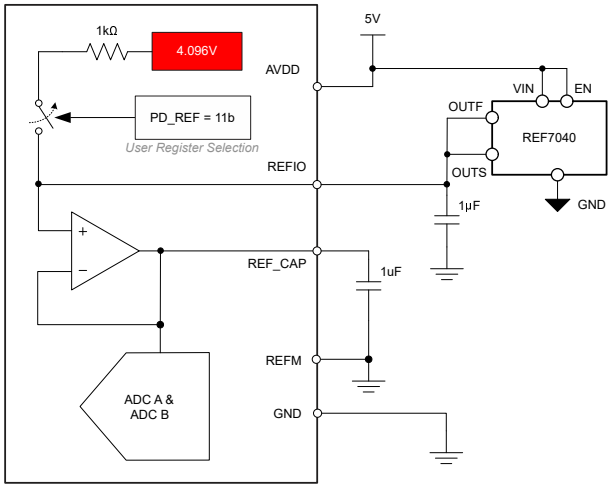


Figure 7-4. External Reference: AVDD = 5V

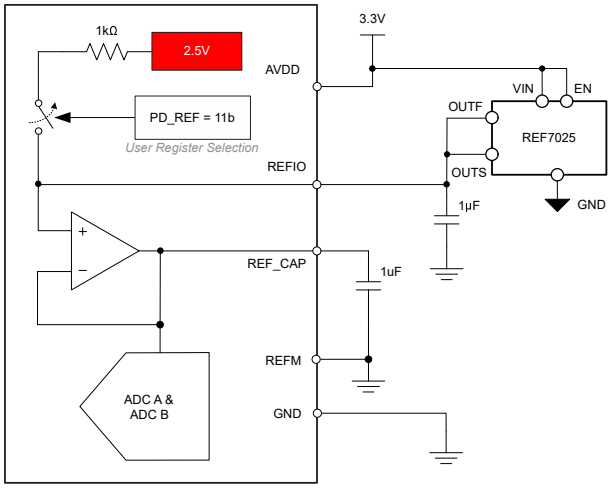


Figure 7-5. External Reference: AVDD = 3.3V

7.3.2.3 External Reference With External Reference Buffer

To improve system gain error thermal drift, power off the internal device reference buffer and connect an external, low-drift reference buffer to the device. As illustrated in Figure 7-6, connect the output of the external reference buffer to the REFIO and REF_CAP pins and power down the internal reference buffer. Make sure the connection to REF_CAP is less than 2Ω. Table 7-3 describes the sequence to power down the internal reference buffer.

Table 7-3. Sequence to Power Down the Internal Reference Buffer

FRAME NUMBER	REGISTER		DESCRIPTION
	ADDRESS	VALUE[15:0]	
1	0x02	0x0002	Select register bank 1
2	0x0C	0x0300	Power down the internal reference
3	0x03	0x000B	Unlock register bank 2
4	0x02	0x0008	Select register bank 2
5	0x09	0x0010	Power down the internal reference buffer
6	0x02	0x0002	Select register bank 1

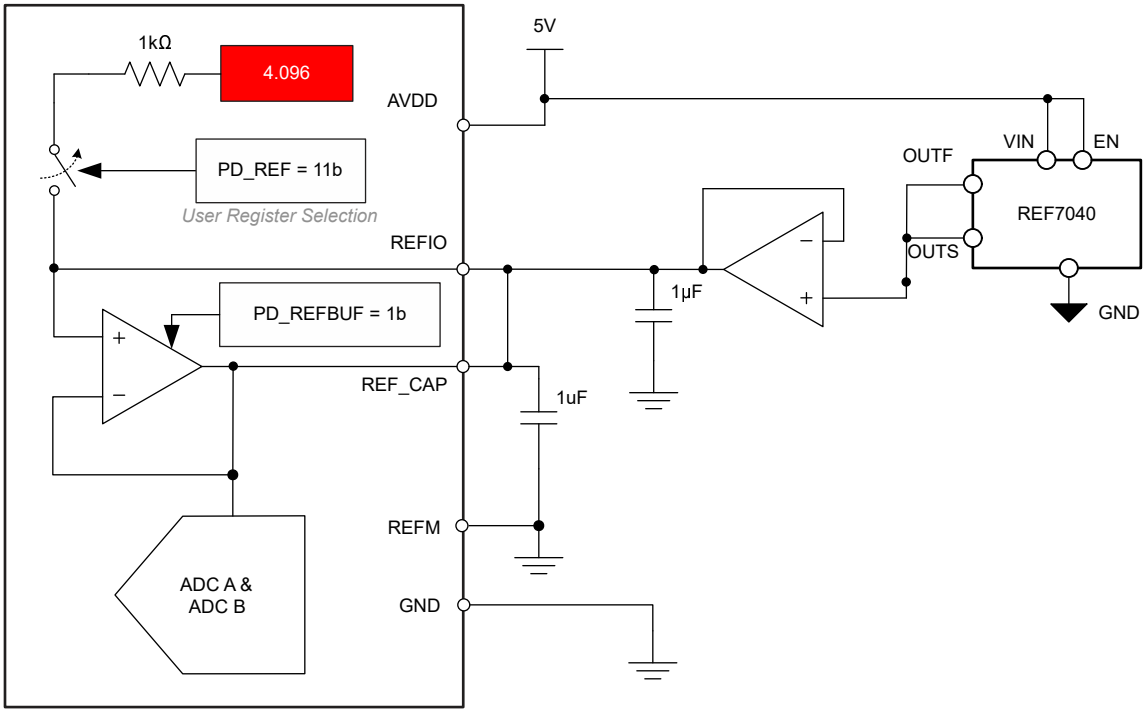


Figure 7-6. External Reference With External Reference Buffer

7.3.3 ADC Transfer Function

The ADS932x outputs 16 bits of conversion data in either two's-complement or straight-binary format. By default, conversion data is output in two's-complement format. To enable straight-binary format, write 1b to DATA_FORMAT in address 0x0D. Table 7-4 and Figure 7-7 describe the transfer characteristics for the ADS932x. Equation 1 gives the least significant bit (LSB) for the ADC.

$$1LSB = (2 \times V_{REFIO}) / 2^{N} \quad (1)$$

where:

- N = Device resolution

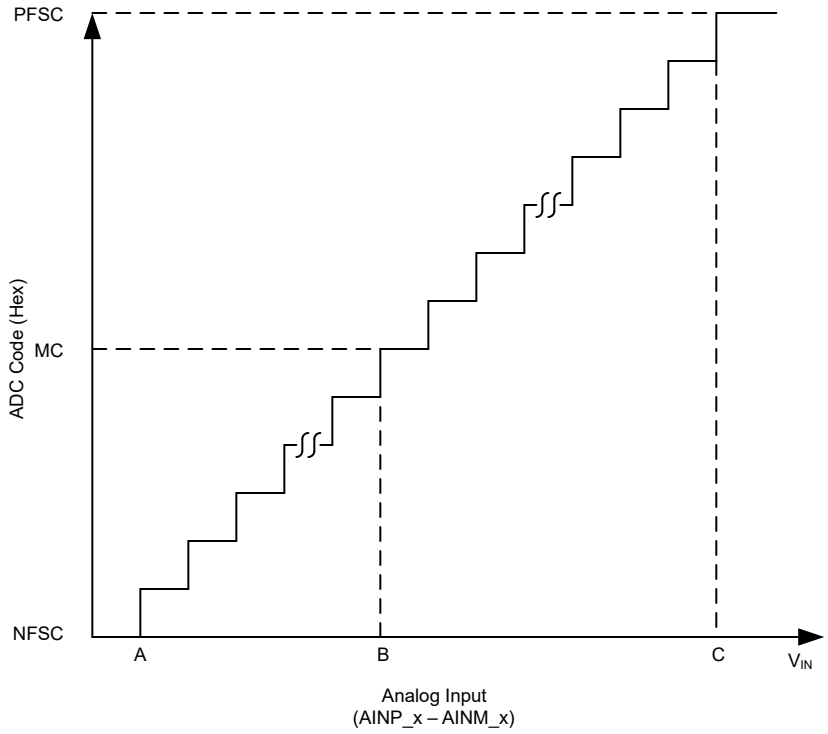


Figure 7-7. Transfer Characteristics

Table 7-4. Transfer Characteristics

STEP	INPUT VOLTAGE (AINP_x − AINM_x)	CODE	DESCRIPTION	16-BIT OUTPUT CODE (Two's Complement)	16-BIT OUTPUT CODE (Straight Binary)
A	≤ $-(V_{REFIO}$ + 1LSB)	NFSC	Negative full-scale code	0x8000	0x0000
B	0V + 1LSB	MC	Mid-code	0x0000	0x8000
C	≥ (V_{REFIO} – 1LSB)	PFSC	Positive full-scale code	0x7FFF	0xFFFF

7.3.4 Data Interface

The ADS932x features an SPI-compatible serial interface with 1-lane, 2-lane, and 4-lane options for the data output. Table 7-5 shows the register settings to configure the number of output data lanes and the corresponding ADC conversion data output on each serial data output pin.

Table 7-5. Output Data Interface Configuration Settings

NUMBER OF OUTPUT DATA LANES	NUM_DATA_LANES REGISTER VALUE	SERIAL DATA OUTPUT PIN	ADC CONVERSION DATA OUTPUT
4 lanes	000b	D3	ADC A[15:8]
		D2	ADC A[7:0]
		D1	ADC B[15:8]
		D0	ADC B[7:0]
2 lanes	101b	D3	ADC A[15:0]
		D2	Hi-Z
		D1	ADC B[15:0]
		D0	Hi-Z
1 lane	110b	D3	ADC A[15:0], 0x00, ADC B[15:0], 0x00
		D2	Hi-Z
		D1	Hi-Z
		D0	Hi-Z

7.3.5 Programmable Data Averaging Filter

The ADS932x features two built-in decimation filters that average the conversion results from the ADC:

- Simple average: The ADC output is the average of the conversion results in a fixed window size and the output data rate decreases with an increased window size.
- Moving average (1): The ADC output is the average of the conversion results in a moving window size. The output data rate stays constant with an increased window size.

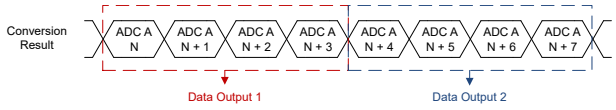


Figure 7-8. Simple Average Data Output

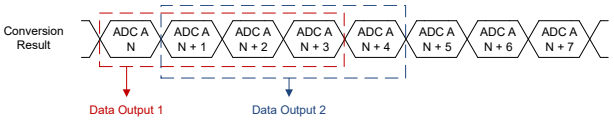


Figure 7-9. Moving Average Data Output

1. Moving average is not applicable for PADS9326VAER.

7.3.5.1 Simple Average

To enable simple data averaging, write 1b to SAVG_EN in address 0x0D and select the window size by writing to SAVG_MODE in address 0x0D.

Table 7-6 specifies the improvement in SNR with simple data averaging and the corresponding impact on ADC output rate. Figure 7-10 illustrates the ADC output timing for a simple average of four samples. When averaging is enabled, the output data frame width increases by four bits, as described in the *Data Frame Width* section.

Table 7-6. Simple Average - ADC Output Data Rate and SNR vs Data Averaging

OVERSAMPLING RATIO	SNR - ADS9327 (16-BIT)	MAXIMUM OUTPUT DATA RATE
No averaging	93.5dB	5MSPS
2	96.7dB	2.5MSPS
4	99dB	1.25MSPS
8	101.1dB	625kSPS
16	102.6dB	312.5kSPS

Table 7-6. Simple Average - ADC Output Data Rate and SNR vs Data Averaging (continued)

OVERSAMPLING RATIO	SNR - ADS9327 (16-BIT)	MAXIMUM OUTPUT DATA RATE
32	103.9dB	156.25kSPS
64	105.2dB	78.125kSPS
128	105.9dB	39.0625kSPS

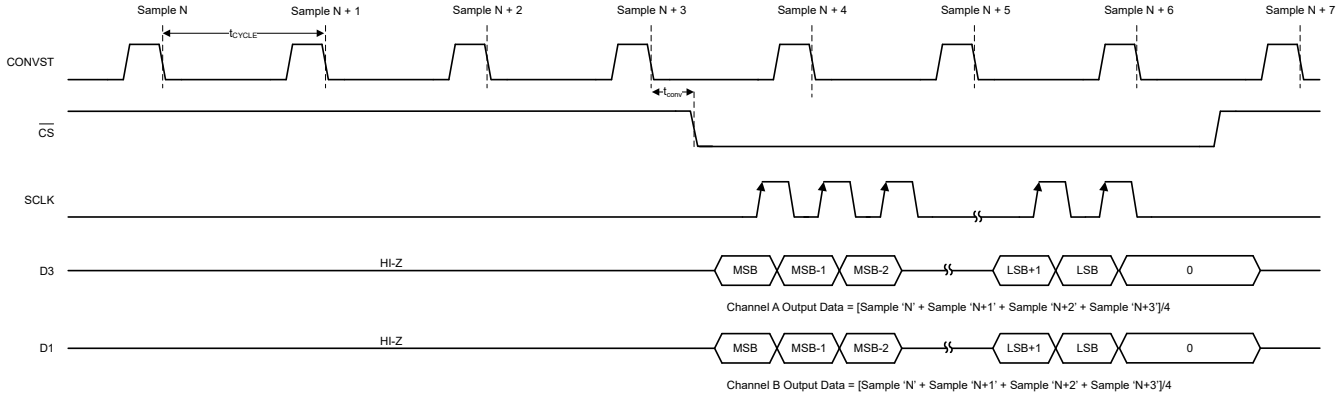


Figure 7-10. ADC Output Example for Simple Average of 4 Samples in 2-Lane Data Interface Mode

7.3.5.1.1 Simple Average with Noncontinuous CONVST

To enable averaging with a non-continuous CONVST, follow the sequence in Table 7-7.

Table 7-7. Simple Average Initialization Sequence for Non-continuous CONVST

Step	Description
1	Unlock the device register map.
2	Enable simple average by writing 1b to SAVG_EN and selecting the window size in SAVG_MODE.
3	Write 1b to AVG_SYNC.
4	Provide 1 pulse of CONVST.
5	Write 0b to AVG_SYNC.
6	Provide 2 additional pulses of CONVST. This step is required after toggling AVG_SYNC.

Figure 7-11 illustrates the timing to enable simple averaging for an average of 2 samples with a noncontinuous CONVST.

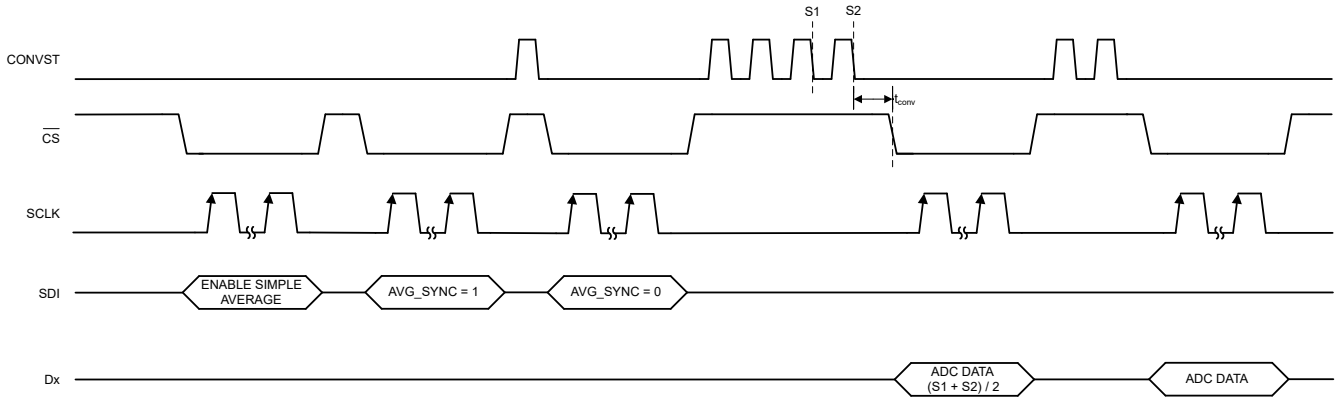


Figure 7-11. Simple Average Enable Sequence Timing with Noncontinuous CONVST for Average of 2 Samples

7.3.5.2 Moving Average

To enable moving data averaging, select the averaging window size by writing to MAVG_MODE in address 0x0D. in register bank 1. The moving average window size is user-selectable between 2, 4, and 8 conversions.

Table 7-8 specifies the improvement in SNR with moving data averaging. Figure 7-12 illustrates the ADC output timing for a moving average of four samples.

Table 7-8. Moving Average - ADC Output Data Rate and SNR vs Data Averaging

OVERSAMPLING RATIO	SNR - ADS9327 (16-BIT)	MAXIMUM OUTPUT DATA RATE
No averaging	93.5dB	5MSPS
2	96.6dB	5MSPS
4	98.9dB	5MSPS
8	100.9dB	5MSPS

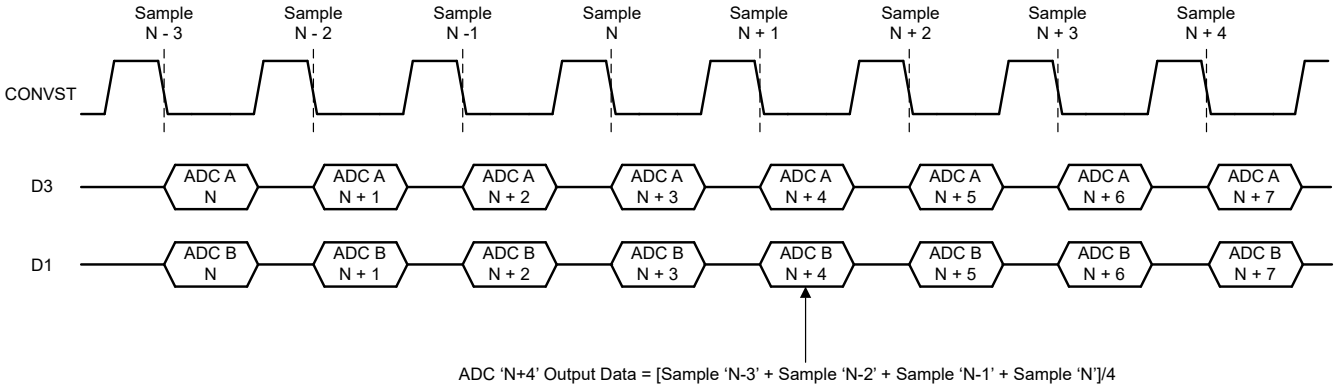


Figure 7-12. ADC Output Example for a Moving Average of 4 Samples

7.3.6 CRC on Output Data Interface

The cyclic redundancy check (CRC) is an error checking code that detects communication errors to the host. CRC is the division remainder of the data payload bytes by a fixed polynomial. The CRC mode is optional and is enabled by the CRC_EN bit in address 0x0D in register bank 1. The CRC in the ADS932x is only implemented on the output data interface and is not used for register read or write operations. When CRC is enabled, the CRC data byte is appended to the ADC conversion result, see the *Data Frame Width* section.

The CRC data byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the argument by a CRC polynomial. The CRC polynomial is based on the CRC-8-CCITT: $X^8 + X^2 + X^1 + 1$. The CRC calculation is preset with 0b11111111.

7.3.7 ADC Output Data Randomizer

The ADS932x features a data output randomizer. When enabled, the ADC conversion result is bit-wise exclusive-ORed (XOR) with the four pseudo-random binary sequence (PRBS) bits appended to the ADC data output. See the *Data Frame Width* section. The XOR PRBS bits have equal probability of being either 1 or 0. As a result of the XOR operation, the data from the ADS932x is randomized. The ground bounce created by the transmission of this randomized result over the data interface is uncorrelated with the analog input voltage. This uncorrelated transmission helps minimize interference between data transmission and analog performance of the ADC when the PCB layout does not minimize ground bounce. To enable the output data randomizer, write 01111b to XOR_EN in address 0x0D in register bank 1. Figure 7-13 shows the data output when the data output randomizer is enabled.

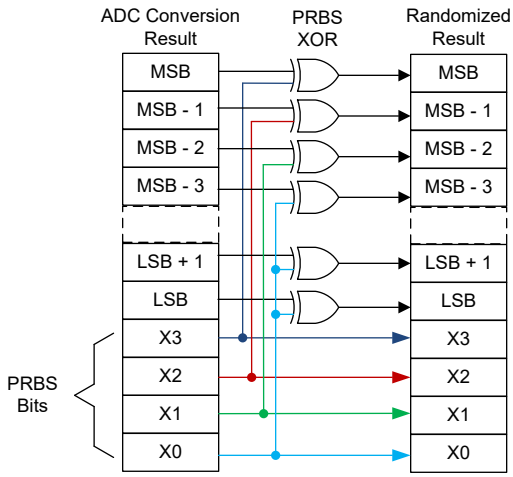


Figure 7-13. XOR Operation With 4-Bit PRBS

7.3.8 Data Frame Width

The ADS932x supports 16-bit, 20-bit, and 24-bit data frame width options. The default output data frame width is 16 bits. As shown in Table 7-9, the output data frame width increases to 20 or 24 bits depending on the use of averaging, XOR, and CRC.

Table 7-9. Output Data Frames

CRC_EN	SAVG_EN	XOR_EN	OUTPUT WIDTH (Bits)	OUTPUT DATA FRAME
CRC module disabled	No averaging	XOR disabled	16	{Conversion result [15:0]}
		XOR enabled	20	{Conversion result [15:0], PRBS[3:0]}
	Averaging enabled	XOR disabled	20	{Conversion result [17:0], 0b00}
		XOR enabled	24	{Conversion result [17:0], PRBS[3:0], 0b00}
CRC module enabled	No averaging	XOR disabled	24	{Conversion result [15:0], CRC[7:0]}
		XOR enabled	N/A	Not supported
	Averaging enabled	XOR disabled	N/A	Not supported
		XOR enabled	N/A	Not supported

7.3.9 Daisy-Chain Mode

The ADS932x operates either as a single converter or in a system with multiple converters. To take advantage of the simple, high-speed, SPI serial interface, cascade converters in a daisy-chain configuration when multiple converters are used. No register configuration is required to enable daisy-chain mode. Figure 7-14 shows a typical connection of three converters in daisy-chain mode.

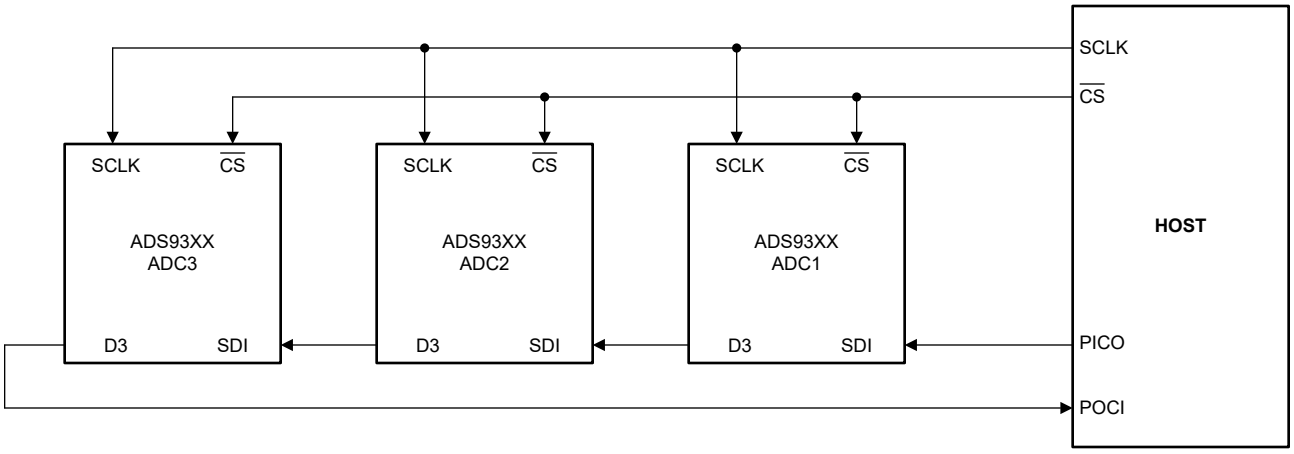


Figure 7-14. Daisy-Chain Connections

When the ADS932x is connected in daisy-chain mode, make sure the device operates in 1-lane interface mode by writing 110b to NUM_DATA_LANES. See the *Data Interface* section. The serial input data passes through the device with a 48 SCLK delay as long as $\overline{CS}$ is active. Figure 7-15 illustrates a detailed timing diagram of this mode when the conversion in each converter is performed simultaneously.

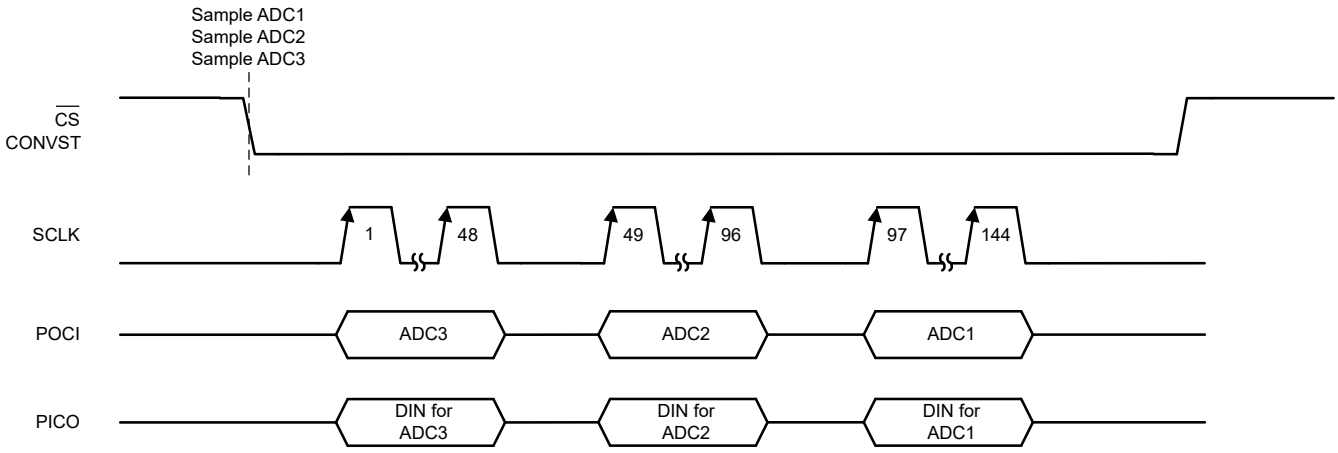


Figure 7-15. Simplified Daisy-Chain Timing

7.3.9.1 Daisy-Clock Mode

When operating in a daisy-chain configuration, as shown in Figure 7-16, the ADS932x features an option to feed-through SCLK on D0. To enable daisy-clock mode, write 1b to DAISY_CLK in address 0x09.

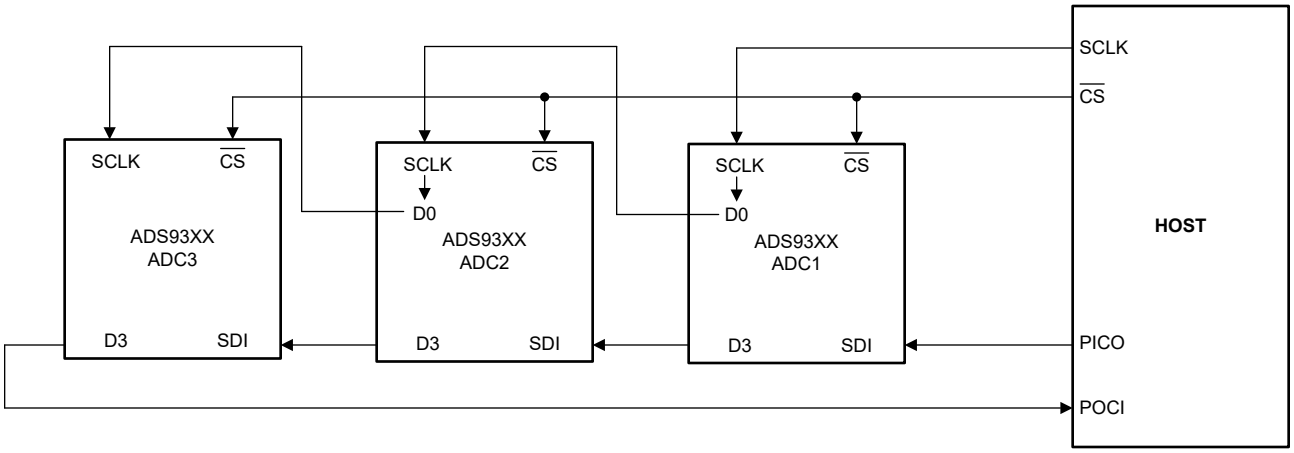


Figure 7-16. Daisy-Chain Connections With Daisy-Clock Mode Enabled

7.4 Device Functional Modes

7.4.1 Reset

Reset the ADS932x by writing 1b to the RESET field in address 0x01. The device registers are initialized to the default values after reset.

7.4.2 Normal Operation

In normal operating mode, the ADS932x is powered up and digitizes sample N on the falling edge of CONVST. Data corresponding to sample N − 1 is launched on the digital interface on the falling edge of $\overline{CS}$ as illustrated in Figure 6-2.

7.4.3 Low-Latency Mode

In low-latency mode, the conversion for sample N starts on the falling edge of CONVST. Data corresponding to sample N are launched on the digital interface on the falling edge of $\overline{CS}$. As illustrated in Figure 6-3, the host provides a minimum time of t_{CONV} between the falling edges of CONVST and $\overline{CS}$. To enter low-latency mode, write 1b to LATENCY_MODE in address 0x09.

7.4.4 $\overline{CS}$-CONVST Short Mode

In $\overline{CS}$-CONVST short mode, tie $\overline{CS}$ and CONVST together externally. As illustrated in Figure 6-4, the ADS932x digitizes sample N on the falling edge of CONVST. Data corresponding to sample N − 1 are launched on the digital interface on the falling edge of $\overline{CS}$. $\overline{CS}$-CONVST short mode is supported by default (1) and creates a 5ns internal delay between the falling edge of CONVST and $\overline{CS}$. The internal delay between CONVST and $\overline{CS}$ is disabled by writing 1b to CSZ_CONVST_DELAY_DIS in address 0x13.

1. $\overline{CS}$-CONVST short mode is not supported by default in PADS9326VAER.

7.4.5 Register Read Mode

In register read mode, the device launches the requested device register data on D3. To enter register read mode, set DATA_SEL = 1b as described in the *Register Read* section.

7.4.6 Initialization Sequence

As shown in Table 7-10 and Table 7-11, initialize ADS9326 and ADS9327 respectively with a sequence of register writes after device power-up or reset. The device registers are initialized with the default value after the initialization sequence is complete.

Table 7-10. ADS9326 Initialization Sequence

STEP NUMBER	REGISTER			DESCRIPTION
	BANK	ADDRESS	VALUE[15:0]	
1	0	0xFE	0xB38F	Register map unlock sequence frame 1
2		0xFE	0xABCD	Register map unlock sequence frame 2
3	0	0x01	0x0002	Software reset
4	Wait 1ms			
5	0	0x01	0x0000	Clear software reset
6	0	0xFE	0xB38F	Register map unlock sequence frame 1
7	0	0xFE	0xABCD	Register map unlock sequence frame 2
8	0	0x02	0x0002	Select register bank 1
9	1	0x0C	0x1200	Select internal reference and INIT_0(0xC[12]) = 1
10	Wait 25ms			
11	1	0x0C	0x0200	INIT_0(0xC[12]) = 0

Table 7-10. ADS9326 Initialization Sequence (continued)

STEP NUMBER	REGISTER			DESCRIPTION
	BANK	ADDRESS	VALUE[15:0]	
12	0	0x03	0x000B	Unlock register bank 2
13	0	0x02	0x0008	Select register bank 2
14	2	0x22	0x0080	INIT_2 = 1
15	0	0x02	0x0002	Select register bank 1
16	0	0xFE	0x1234	Register map lock sequence

Table 7-11. ADS9327 Initialization Sequence

STEP NUMBER	REGISTER			DESCRIPTION
	BANK	ADDRESS	VALUE[15:0]	
1	0	0xFE	0xB38F	Register map unlock sequence frame 1
2	0	0xFE	0xABCD	Register map unlock sequence frame 2
3	0	0x01	0x0002	Software reset
4	Wait 1ms			
5	0	0x01	0x0000	Clear software reset
6	0	0xFE	0xB38F	Register map unlock sequence frame 1
7	0	0xFE	0xABCD	Register map unlock sequence frame 2
8	0	0x02	0x0002	Select register bank 1
9	1	0x0C	0x0200	Select internal reference.
10	0	0x03	0x000B	Unlock register bank 2.
11	0	0x02	0x0008	Select register bank 2.
12	2	0x0F	0x4000	INIT_1 = 1
13	0	0x02	0x0002	Select register bank 1
14	0	0xFE	0x1234	Register map lock sequence

7.5 Programming

7.5.1 SPI Frame Length for Register Operations

As described in Table 7-12, use a 24-bit or 48-bit SPI for register read or write operations, depending on the number of output data lanes used. If the SPI frame length is longer or shorter than required, this disparity results in unintentional writes to the user registers.

Table 7-12. SPI Frame Length Requirements

NUMBER OF OUTPUT DATA LANES	NUMBER OF SCLKS REQUIRED
4	24
2	24
1	24 or 48

7.5.2 Register Map Lock

The ADS932x implements a register map lock feature that prevents an accidental or unintended write to the device registers. By default, the device register map is locked. Unlock the register map by following the sequence shown in Table 7-13 before writing or reading a register.

Table 7-13. ADS932x Register Map Unlock Sequence

STEP NUMBER	REGISTER		
	BANK	ADDRESS	VALUE[15:0]
1	0	0xFE	0xB38F
2	0	0xFE	0xABCD

After writing or reading registers, lock the register map to prevent unintended register writes. Writing any value other than the register map unlock sequence to address 0xFE locks the register map. Table 7-14 shows an example sequence to lock the device register map.

Table 7-14. ADS932x Example Register Map Lock Sequence

STEP NUMBER	REGISTER		
	BANK	ADDRESS	VALUE[15:0]
1	0	0xFE	0x1234

7.5.3 Register Write

Register write access is enabled by following the register map unlock sequence described in the *Register Map Lock* section. The 16-bit registers are grouped in two register banks and are addressable with an 8-bit register address. Register bank 1 is selected for read or write operation by writing 0x02 to REG_BANK_SEL in address 0x02. Registers in bank 0 are always accessible, irrespective of the REG_BANK_SEL bits. The register addresses in bank 0 are unique and are not used in register bank 1. The 24-bit data on SDI consist of an 8-bit address and 16-bit data. The data on SDI are latched on the rising edge of SCLK. The device decodes the write command on the $\overline{CS}$ rising edge and updates the specified register with 16-bit data specified in the register write operation. Figure 7-17 shows a 24-bit SPI frame for a register write and Table 7-15 describes the steps required to write a register.

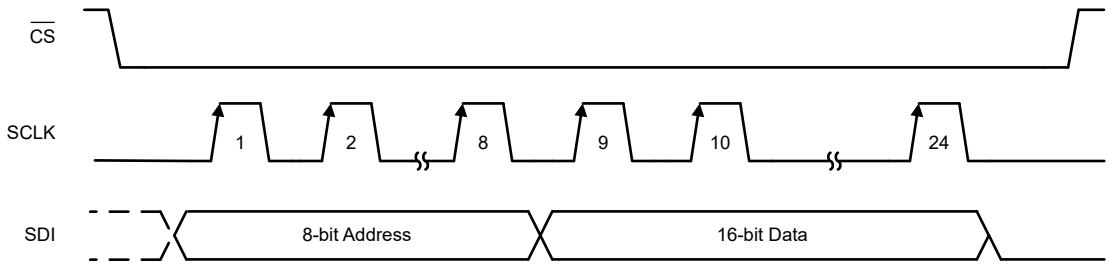


Figure 7-17. Register Write Frame

Table 7-15. Register Write Sequence

FRAME NUMBER	REGISTER		DESCRIPTION
	ADDRESS	VALUE[15:0]	
1	0xFE	0xB38F	Unlocks the register map.
2	0xFE	0xABCD	
3	0x02	0x02	Selects register bank 1. This step is only required for register bank 1.
4	REG_ADDR	DATA	Writes user data to the desired address. Repeat this step for the required number of register writes.
5	0xFE	0x1234	Locks the register map after register writes are completed.

7.5.4 Register Read

Register access is enabled by following the register map unlock sequence described in the *Register Map Lock* section. To read registers in bank 1, write 0x02 to register address 0x02. As shown in Figure 7-18, 24-bit or 48-bit SPI frames are required to read registers. Table 7-16 describes the sequence required to read a register. After the register map is unlocked and the register bank is selected, write the register address to be read to REG_READ_ADDR. Set DATA_SEL = 1 in address 0x01 to launch the register data on D3 in the next frame. On the rising edge of $\overline{CS}$, the read command is decoded and the requested register data are available for reading during the next frame. During the next frame, the first 16 bits on D3 correspond to the requested register read. Use SDI to initiate another operation or set SDI to 0. To begin launching ADC conversion results on the digital interface in the following frame, set DATA_SEL = 0b. After register operations are completed, lock the register map as described in the *Register Map Lock* section.

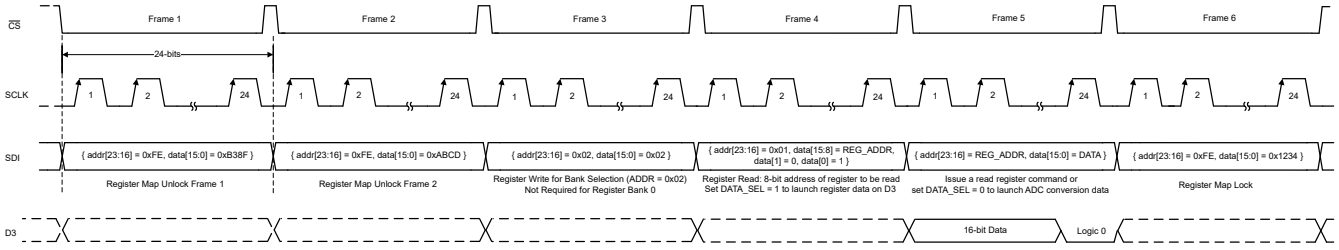


Figure 7-18. Register Read

Table 7-16. Register Read Sequence

FRAME NUMBER	REGISTER		DESCRIPTION
	ADDRESS	VALUE[15:0]	
1	0xFE	0xB38F	Unlocks the register map.
2	0xFE	0xABCD	
3	0x02	0x02	Selects register bank 1. This step is only required for register bank 1.
4	0x01	REG_READ_ADDR[15:8] = REG_ADDR, RESET[1] = 0, DATA_SEL[0] = 1	REG_READ_ADDR selects the address to be read and DATA_SEL launches the selected register data on D3 in the following frame.
5	REG_ADDR	DATA	The 16-bit data requested in the previous frame is available on D3. In this frame, issue another read register command or write DATA_SEL = 0 in address 0x01. This setting begins launching ADC conversion data on the data interface in the next frame. Repeat this step for the required number of register reads.
6	0xFE	0x1234	Locks the register map after register operations are completed.

8 Register Map: ADS9327

8.1 Register Bank 0

Table 8-1 lists the memory-mapped registers for the Register Bank 0 registers. All register offset addresses not listed in Table 8-1 must be considered as reserved locations and the register contents must not be modified.

Table 8-1. Register Map Bank 0

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	Register 01h	REG_READ_ADDR[7:0]							
		RESERVED						RESET	DATA_SEL
0x02	Register 02h	RESERVED							
		RESERVED				REG_BANK_SEL[3:0]			
0x03	Register 03h	RESERVED							
		RESERVED				BANK_2_UNLOCK[3:0]			
0xFE	Register FEh	REG_LOCK[15:0]							
		REG_LOCK[15:0]							

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. Register Bank 0 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 Register 01h (Address = 0x01) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-1. Register 01h

15	14	13	12	11	10	9	8
REG_READ_ADDR[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED						RESET	DATA_SEL
R/W-000000b						R/W-0b	R/W-0b

Table 8-3. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
15:8	REG_READ_ADDR[7:0]	R/W	00000000b	8-bit address of the register to be read.
7:2	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
1	RESET	R/W	0b	ADC reset control. 0b = Normal device operation. 1b = Reset ADC and all registers
0	DATA_SEL	R/W	0b	Select data to be launched on serial interface of the ADC. 0b = ADC conversion result is output. 1b = Register data is output on D3.

8.1.2 Register 02h (Address = 0x02) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-2. Register 02h

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				REG_BANK_SEL[3:0]			
R/W-000000000000b				R/W-0000b			

Table 8-4. Register 02h Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3:0	REG_BANK_SEL[3:0]	R/W	0000b	Register bank selection for read and write operations. 0000b = Select register bank 0. 0010b = Select register bank 1. 1000b = Select register bank 2.

8.1.3 Register 03h (Address = 0x03) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-3. Register 03h

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				BANK_2_UNLOCK[3:0]			
R/W-000000000000b				R/W-0000b			

Table 8-5. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3:0	BANK_2_UNLOCK[3:0]	R/W	0000b	Key to unlock register bank 2. 1011b = Unlock register bank 2.

8.1.4 Register FEh (Address = 0xFE) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-4. Register FEh

15	14	13	12	11	10	9	8
REG_LOCK[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
REG_LOCK[15:0]							
R/W-0000000000000000b							

Table 8-6. Register FEh Field Descriptions

Bit	Field	Type	Reset	Description
15:0	REG_LOCK[15:0]	R/W	0000000000000000b	Key to unlock and lock the register map. To unlock the register map, write 0xB38F followed by 0xABCD. To lock the register map, write 0x1234.

8.2 Register Bank 1

Table 8-7 lists the memory-mapped registers for the Register Bank 1 registers. All register offset addresses not listed in Table 8-7 should be considered as reserved locations and the register contents should not be modified.

Table 8-7. Register Map Bank 1

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	Register 08h	RESERVED							
		RESERVED				PDN_CH[1:0]		RESERVED	PDN_CTL
0x09	Register 09h	RESERVED					LATENCY_MODE	RESERVED	
		RESERVED	NUM_DATA_LANES[2:0]			RESERVED			DAISY_CLK
0x0A	Register 0Ah	RESERVED							
		RESERVED				DIG_DELAY_EN	DRIVE_STRENGTH[2:0]		
0x0B	Register 0Bh	RESERVED				DIG_DELAY_D3[2:0]			DIG_DELAY_D2[2:0]
		DIG_DELAY_D2[2:0]		DIG_DELAY_D1[2:0]			DIG_DELAY_D0[2:0]		
0x0C	Register 0Ch	RESERVED						PD_REF[1:0]	
		RESERVED	CLK_PWR[2:0]			RESERVED			
0x0D	Register 0Dh	XOR_EN[4:0]					CRC_EN	RESERVED	DATA_FORMAT
		SAVG_MODE[3:0]				MAVG_MODE[1:0]		AVG_SYNC	SAVG_EN
0x0F	Register 0Fh	RESERVED	TEST_PATT_2_LSB[3:0]				TEST_PATT_1_LSB[3:0]		
		TEST_PATT_1_LSB[3:0]	TEST_RAMP_RST	RESERVED		TEST_PATT_MODE[1:0]		TEST_PATT_EN_CHB	TEST_PATT_EN_CHA
0x10	Register 10h	TEST_PATT_1_MSB[15:0]							
		TEST_PATT_1_MSB[15:0]							
0x11	Register 11h	TEST_PATT_2_MSB[15:0]							
		TEST_PATT_2_MSB[15:0]							
0x13	Register 13h	RESERVED							
		CSZ_CONVST_DELAY_DIS	RESERVED						
0x14	Register 14h	RESERVED							
		RESERVED					DIS_INT_BUFFER	INT_REF_MODE[1:0]	
0x39	Register 39h	RESERVED	DIS_VCMOUT	RESERVED					
		RESERVED							

Complex bit access types are encoded to fit into small table cells. Table 8-8 shows the codes that are used for access types in this section.

Table 8-8. Register Bank 1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 Register 08h (Address = 0x08) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-5. Register 08h

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				PDN_CH[1:0]		RESERVED	PDN_CTL
R/W-000000000000b				R/W-00b		R/W-0b	R/W-0b

Table 8-9. Register 08h Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3:2	PDN_CH[1:0]	R/W	00b	Power-down control for the analog input channels. 00b = Normal device operation. 01b = Channel A powered down. 10b = Channel B powered down. 11b = Both channels powered down.
1	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
0	PDN_CTL	R/W	0b	Full device power-down control 0b = Normal device operation. 1b = Full device power-down control.

8.2.2 Register 09h (Address = 0x09) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-6. Register 09h

15	14	13	12	11	10	9	8
RESERVED					LATENCY_MODE	RESERVED	
R/W-00000b					R/W-0b	R/W-000b	
7	6	5	4	3	2	1	0
RESERVED	NUM_DATA_LANES[2:0]			RESERVED			DAISY_CLK
R/W-000b	R/W-000b			R/W-000b			R/W-0b

Table 8-10. Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.
10	LATENCY_MODE	R/W	0b	Control to select latency mode. 0b = Data corresponding to sample N - 1 is launched on $\overline{CS}$ falling edge during sample N frame. 1b = Low latency mode is active. Data corresponding to sample N is launched on $\overline{CS}$ falling edge during sample N frame. CS high until t_{CONV} (max).
9:7	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
6:4	NUM_DATA_LANES[2:0]	R/W	000b	Control to select the number of lanes used for the serial data interface. 000b = ADC A data output on D[3:2] and ADC B data output on D[1:0]. 101b = ADC A data output on D3 and ADC B data output on D1. D2 and D0 are HI-Z. 110b = ADC A and ADC B data output on D3. D[2:0] are HI-Z.
3:1	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
0	DAISY_CLK	R/W	0b	Control to feed-through SCLK (Pin 17) on D0 (Pin 16) when multiple devices are daisy-chained. 0b = D0 outputs data as per the data interface configuration. 1b = D0 feeds-through SCLK.

8.2.3 Register 0Ah (Address = 0x0A) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-7. Register 0Ah

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				DIG_DELAY_EN	DRIVE_STRENGTH[2:0]		
R/W-000000000000b				R/W-0b	R/W-000b		

Table 8-11. Register 0Ah Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3	DIG_DELAY_EN	R/W	0b	Control for digital delay on the output buffer path. 0b = Normal device operation. 1b = Digital delay on the output buffer path is enabled. The magnitude is controlled by DIG_DELAY_Dx fields in address 0Bh.
2:0	DRIVE_STRENGTH[2:0]	R/W	000b	Control to configure the drive strength of the digital output buffer. 000b = Normal device operation. 101b = 0.5x drive strength. 110b = 2x drive strength. 111b = 1.5x drive strength.

8.2.4 Register 0Bh (Address = 0x0B) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-8. Register 0Bh

15	14	13	12	11	10	9	8
RESERVED				DIG_DELAY_D3[2:0]			DIG_DELAY_D2[2:0]
R/W-0000b				R/W-000b			R/W-000b
7	6	5	4	3	2	1	0
DIG_DELAY_D2[2:0]			DIG_DELAY_D1[2:0]			DIG_DELAY_D0[2:0]	
R/W-000b			R/W-000b			R/W-000b	

Table 8-12. Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.
11:9	DIG_DELAY_D3[2:0]	R/W	000b	Programmable digital delay on D3. 000b = 0ns delay. 001b = 1ns delay. 010b = 2ns delay. 011b = 3ns delay. 100b = 4ns delay. 101b = 5ns delay.
8:6	DIG_DELAY_D2[2:0]	R/W	000b	Programmable digital delay on D2. 000b = 0ns delay. 001b = 1ns delay. 010b = 2ns delay. 011b = 3ns delay. 100b = 4ns delay. 101b = 5ns delay.
5:3	DIG_DELAY_D1[2:0]	R/W	000b	Programmable digital delay on D1. 000b = 0ns delay. 001b = 1ns delay. 010b = 2ns delay. 011b = 3ns delay. 100b = 4ns delay. 101b = 5ns delay.
2:0	DIG_DELAY_D0[2:0]	R/W	000b	Programmable digital delay on D0. 000b = 0ns delay. 001b = 1ns delay. 010b = 2ns delay. 011b = 3ns delay. 100b = 4ns delay. 101b = 5ns delay.

8.2.5 Register 0Ch (Address = 0x0C) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-9. Register 0Ch

15	14	13	12	11	10	9	8
RESERVED						PD_REF[1:0]	
R/W-000000b						R/W-00b	
7	6	5	4	3	2	1	0
RESERVED	CLK_PWR[2:0]			RESERVED			
R/W-0b	R/W-000b			R/W-0000b			

Table 8-13. Register 0Ch Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:8	PD_REF[1:0]	R/W	00b	ADC reference voltage source selection. 10b = Internal reference is active. 11b = Internal reference is inactive. Force an external reference via REFIO (pin 9).
7	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
6:4	CLK_PWR[2:0]	R/W	000b	Control to select the power supply domain for the input clock. 000b = IOVDD domain. 101b = VDD_1V8 domain.
3:0	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.

8.2.6 Register 0Dh (Address = 0x0D) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-10. Register 0Dh

15	14	13	12	11	10	9	8
XOR_EN[4:0]					CRC_EN	RESERVED	DATA_FORMAT
R/W-00000b					R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
SAVG_MODE[3:0]				MAVG_MODE[1:0]		AVG_SYNC	SAVG_EN
R/W-0000b				R/W-00b		R/W-0b	R/W-0b

Table 8-14. Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
15:11	XOR_EN[4:0]	R/W	00000b	Control to enable XOR operation on the ADC conversion result. 00000b = XOR operation is inactive. 01111b = Bit-wise XOR operation on the ADC conversion result is active.
10	CRC_EN	R/W	0b	Control to enable CRC on the data interface. 0b = CRC module is inactive. 1b = CRC module is active.
9	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
8	DATA_FORMAT	R/W	0b	Control to select the data format for the ADC conversion result. 0b = Two's complement format. 1b = Straight binary format.
7:4	SAVG_MODE[3:0]	R/W	0000b	Control for the number of samples to be averaged in simple averaging mode. 0000b = 2 samples averaged. 0001b = 4 samples averaged. 0010b = 8 samples averaged. 0011b = 16 samples averaged. 0100b = 32 samples averaged. 0101b = 64 samples averaged. 0110b = 128 samples averaged.
3:2	MAVG_MODE[1:0]	R/W	00b	Control for the number of samples to be averaged in moving average mode. 00b = Moving average is inactive. 01b = 2 moving samples averaged. 10b = 4 moving samples averaged. 11b = 8 moving samples averaged.
1	AVG_SYNC	R/W	0b	Synchronization control for the internal averaging filter. Write 1b to trigger when averaging starts from the subsequent cycle.
0	SAVG_EN	R/W	0b	Control to enable simple averaging. Select the number of samples to be averaged in SAVG_MODE. 0b = Simple averaging is inactive. 1b = Simple averaging is active.

8.2.7 Register 0Fh (Address = 0x0F) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-11. Register 0Fh

15	14	13	12	11	10	9	8
RESERVED	TEST_PATT_2_LSB[3:0]					TEST_PATT_1_LSB[3:0]	
R/W-0b	R/W-0000b					R/W-0000b	
7	6	5	4	3	2	1	0
TEST_PATT_1_LSB[3:0]	TEST_RAMP_RST	RESERVED		TEST_PATT_MODE[1:0]		TEST_PATT_EN_CHB	TEST_PATT_EN_CHA
R/W-0000b	R/W-0b	R/W-00b		R/W-00b		R/W-0b	R/W-0b

Table 8-15. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
14:11	TEST_PATT_2_LSB[3:0]	R/W	0000b	LSB 4-bit test pattern corresponding to ADC B.
10:7	TEST_PATT_1_LSB[3:0]	R/W	0000b	LSB 4-bit test pattern corresponding to ADC A.
6	TEST_RAMP_RST	R/W	0b	Control to reset the ramp pattern to start from 0. Toggle this register bit to reset the ramp pattern when TEST_PATT_MODE is set to ramp pattern.
5:4	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
3:2	TEST_PATT_MODE[1:0]	R/W	00b	Type of test pattern at the data interface. 00b = ADC outputs constant pattern defined in TEST_PATT_1_MSB in address 0x10 and TEST_PATT_1_LSB in address 0x0F for ADC A. Test pattern for ADC B is defined in TEST_PATT_2_MSB in address 0x11 and TEST_PATT_2_LSB in address 0x0F. 01b = Ramp pattern. 10b = Alternate pattern between AAAA and 5555 toggled at each readout.
1	TEST_PATT_EN_CHB	R/W	0b	Control to enable digital test pattern for ADC B. 0b = ADC conversion result is launched on the data interface. 1b = Digital test pattern is launched on the data interface.
0	TEST_PATT_EN_CHA	R/W	0b	Control to enable digital test pattern for ADC A. 0b = ADC conversion result is launched on the data interface. 1b = Digital test pattern is launched on the data interface.

8.2.8 Register 10h (Address = 0x10) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-12. Register 10h

15	14	13	12	11	10	9	8
TEST_PATT_1_MSB[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TEST_PATT_1_MSB[15:0]							
R/W-0000000000000000b							

Table 8-16. Register 10h Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TEST_PATT_1_MSB[15:0]	R/W	0000000000000000b	MSB 16-bit test pattern corresponding to ADC A.

8.2.9 Register 11h (Address = 0x11) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-13. Register 11h

15	14	13	12	11	10	9	8
TEST_PATT_2_MSB[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TEST_PATT_2_MSB[15:0]							
R/W-0000000000000000b							

Table 8-17. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TEST_PATT_2_MSB[15:0]	R/W	0000000000000000b	MSB 16-bit test pattern corresponding to ADC B.

8.2.10 Register 13h (Address = 0x13) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-14. Register 13h

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000b							
7	6	5	4	3	2	1	0
CSZ_CONVST_DELAY_DIS	RESERVED						
R/W-0b	R/W-0000000b						

Table 8-18. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R/W	00000000b	Reserved. Do not change from the default reset value.
7	CSZ_CONVST_DELAY_DIS	R/W	0b	Control to disable internal 5ns delay between CONVST and $\overline{CS}$ falling edges. 0b = Normal device operation. 1b = Disable internal 5ns delay between CONVST and $\overline{CS}$. t_{d_CSCK} reduces to 12ns and t_{ht_CVCS} increases to 10ns.
6:0	RESERVED	R/W	0000000b	Reserved. Do not change from the default reset value.

8.2.11 Register 14h (Address = 0x14) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-15. Register 14h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0000000000000b							
7	6	5	4	3	2	1	0
RESERVED					DIS_INT_BUFFER	INT_REF_MODE[1:0]	
R/W-0000000000000b					R/W-0b	R/W-00b	

Table 8-19. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	R/W	0000000000000b	Reserved. Do not change from the default reset value.
2	DIS_INT_BUFFER	R/W	0b	Control to disable internal input buffer and reduce AVDD current. 0b = Internal Buffer is active. 1b = Internal Buffer is inactive. AVDD current reduces up to 300uA at 5MSPS.
1:0	INT_REF_MODE[1:0]	R/W	00b	Control to select internal reference voltage when AVDD is 5V. 00b = 4.096V internal reference. 01b = 2.5V internal reference. 11b = 3.3V internal reference.

8.2.12 Register 39h (Address = 0x39) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-16. Register 39h

15	14	13	12	11	10	9	8
RESERVED	DIS_VCMOUT	RESERVED					
R/W-0b	R/W-0b	R/W-00000000000000b					
7	6	5	4	3	2	1	0
RESERVED							
R/W-00000000000000b							

Table 8-20. Register 39h Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
14	DIS_VCMOUT	R/W	0b	Control to disable VCMOUT. 0b = VCMOUT is active. 1b = VCMOUT is inactive.
13:0	RESERVED	R/W	00000000000000b	Reserved. Do not change from the default reset value.

8.3 Register Bank 2

Table 8-21 lists the memory-mapped registers for the register bank 2 registers. Consider all register offset addresses not listed in Table 8-21 as reserved locations and do not modify the register contents.

Table 8-21. Register Map Bank 2

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	Register 09h	RESERVED							
		RESERVED			PD_REFBUF	RESERVED			

Complex bit access types are encoded to fit into small table cells. Table 8-22 shows the codes that are used for access types in this section.

Table 8-22. Register Bank 2 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.1 Register 09h (Address = 0x09) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-17. Register 09h

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000000b							
7	6	5	4	3	2	1	0
RESERVED			PD_REFBUF	RESERVED			
R/W-00000000000b			R/W-0b	R/W-0000b			

Table 8-23. Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED	R/W	00000000000b	Reserved. Do not change from the default reset value.
4	PD_REFBUF	R/W	0b	Control to power down the internal reference buffer. 0b = Internal reference buffer is active. 1b = Internal reference buffer is inactive. Use an external reference buffer and connect the external reference to the REFIO and REF_CAP pins.
3:0	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.

9 Register Map: ADS9326

9.1 Register Bank 0

Table 9-1 lists the memory-mapped registers for the Register Bank 0 registers. All register offset addresses not listed in Table 9-1 must be considered as reserved locations and the register contents must not be modified.

Table 9-1. Register Map Bank 0

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	Register 01h	REG_READ_ADDR[7:0]							
		RESERVED						RESET	DATA_SEL
0x02	Register 02h	RESERVED							
		RESERVED				REG_BANK_SEL[3:0]			
0x03	Register 03h	RESERVED							
		RESERVED				BANK_2_UNLOCK[3:0]			
0xFE	Register FEh	REG_LOCK[15:0]							
		REG_LOCK[15:0]							

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. Register Bank 0 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.1.1 Register 01h (Address = 0x01) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-1. Register 01h

15	14	13	12	11	10	9	8
REG_READ_ADDR[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED						RESET	DATA_SEL
R/W-000000b						R/W-0b	R/W-0b

Table 9-3. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
15:8	REG_READ_ADDR[7:0]	R/W	00000000b	8-bit address of the register to be read.
7:2	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
1	RESET	R/W	0b	ADC reset control. 0b = Normal device operation. 1b = Reset ADC and all registers
0	DATA_SEL	R/W	0b	Select data to be launched on serial interface of the ADC. 0b = ADC conversion result is output. 1b = Register data is output on D3.

9.1.2 Register 02h (Address = 0x02) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-2. Register 02h

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				REG_BANK_SEL[3:0]			
R/W-000000000000b				R/W-0000b			

Table 9-4. Register 02h Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3:0	REG_BANK_SEL[3:0]	R/W	0000b	Register bank selection for read and write operations. 0000b = Select register bank 0. 0010b = Select register bank 1. 1000b = Select register bank 2.

9.1.3 Register 03h (Address = 0x03) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-3. Register 03h

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				BANK_2_UNLOCK[3:0]			
R/W-000000000000b				R/W-0000b			

Table 9-5. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3:0	BANK_2_UNLOCK[3:0]	R/W	0000b	Key to unlock register bank 2. 1011b = Unlock register bank 2.

9.1.4 Register FEh (Address = 0xFE) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-4. Register FEh

15	14	13	12	11	10	9	8
REG_LOCK[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
REG_LOCK[15:0]							
R/W-0000000000000000b							

Table 9-6. Register FEh Field Descriptions

Bit	Field	Type	Reset	Description
15:0	REG_LOCK[15:0]	R/W	0000000000000000b	Key to unlock and lock the register map. To unlock the register map, write 0xB38F followed by 0xABCD. To lock the register map, write 0x1234.

9.2 Register Bank 1

Table 9-7 lists the memory-mapped registers for the Register Bank 1 registers. All register offset addresses not listed in Table 9-7 must be considered as reserved locations and the register contents must not be modified.

Table 9-7. Register Map Bank 1

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	Register 08h	RESERVED							
		RESERVED				PDN_CH[1:0]		RESERVED	PDN_CTL
0x09	Register 09h	RESERVED					LATENCY_MODE	RESERVED	
		RESERVED	NUM_DATA_LANES[2:0]			RESERVED			DAISY_CLK
0x0A	Register 0Ah	RESERVED							
		RESERVED				DIG_DELAY_EN	DRIVE_STRENGTH[2:0]		
0x0B	Register 0Bh	RESERVED				DIG_DELAY_D3[2:0]			DIG_DELAY_D2[2:0]
		DIG_DELAY_D2[2:0]		DIG_DELAY_D1[2:0]			DIG_DELAY_D0[2:0]		
0x0C	Register 0Ch	RESERVED						PD_REF[1:0]	
		RESERVED	CLK_PWR[2:0]			RESERVED			
0x0D	Register 0Dh	XOR_EN[4:0]					CRC_EN	RESERVED	DATA_FORMAT
		SAVG_MODE[3:0]				RESERVED		AVG_SYNC	SAVG_EN
0x0F	Register 0Fh	RESERVED							
		RESERVED		TEST_PATT_INCR[1:0]		TEST_PATT_MODE[1:0]		RESERVED	TEST_PATT_EN
0x10	Register 10h	TEST_PATT_1[15:0]							
		TEST_PATT_1[15:0]							
0x11	Register 11h	TEST_PATT_2[15:0]							
		TEST_PATT_2[15:0]							
0x13	Register 13h	RESERVED						CSZ_CONVST_SHORT_EN[2:0]	
		CSZ_CONVST_SHORT_EN[2:0]	RESERVED						

Complex bit access types are encoded to fit into small table cells. Table 9-8 shows the codes that are used for access types in this section.

Table 9-8. Register Bank 1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.2.1 Register 08h (Address = 0x08) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-5. Register 08h

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				PDN_CH[1:0]		RESERVED	PDN_CTL
R/W-000000000000b				R/W-00b		R/W-0b	R/W-0b

Table 9-9. Register 08h Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3:2	PDN_CH[1:0]	R/W	00b	Power-down control for the analog input channels. 00b = Normal device operation. 01b = Channel A powered down. 10b = Channel B powered down. 11b = Both channels powered down.
1	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
0	PDN_CTL	R/W	0b	Full device power-down control 0b = Normal device operation. 1b = Full device power-down control.

9.2.2 Register 09h (Address = 0x09) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-6. Register 09h

15	14	13	12	11	10	9	8
RESERVED					LATENCY_MODE	RESERVED	
R/W-00000b					R/W-0b	R/W-000b	
7	6	5	4	3	2	1	0
RESERVED	NUM_DATA_LANES[2:0]			RESERVED			DAISY_CLK
R/W-000b	R/W-000b			R/W-000b			R/W-0b

Table 9-10. Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.
10	LATENCY_MODE	R/W	0b	Control to select latency mode. 0b = Data corresponding to sample N - 1 is launched on $\overline{CS}$ falling edge during sample N frame. 1b = Low latency mode is active. Data corresponding to sample N is launched on $\overline{CS}$ falling edge during sample N frame. CS high until t_{CONV} (max).
9:7	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
6:4	NUM_DATA_LANES[2:0]	R/W	000b	Control to select the number of lanes used for the serial data interface. 000b = ADC A data output on D[3:2] and ADC B data output on D[1:0]. 101b = ADC A data output on D3 and ADC B data output on D1. D2 and D0 are HI-Z. 110b = ADC A and ADC B data output on D3. D[2:0] are HI-Z.
3:1	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
0	DAISY_CLK	R/W	0b	Control to feed-through SCLK (Pin 17) on D0 (Pin 16) when multiple devices are daisy-chained. 0b = D0 outputs data as per the data interface configuration. 1b = D0 feeds-through SCLK.

9.2.3 Register 0Ah (Address = 0x0A) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-7. Register 0Ah

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				DIG_DELAY_EN	DRIVE_STRENGTH[2:0]		
R/W-000000000000b				R/W-0b	R/W-000b		

Table 9-11. Register 0Ah Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3	DIG_DELAY_EN	R/W	0b	Control for digital delay on the output buffer path. 0b = Normal device operation. 1b = Digital delay on the output buffer path is enabled. The magnitude is controlled by DIG_DELAY_Dx fields in address 0Bh.
2:0	DRIVE_STRENGTH[2:0]	R/W	000b	Control to configure the drive strength of the digital output buffer. 000b = Normal device operation. 101b = 0.5x drive strength. 110b = 2x drive strength. 111b = 1.5x drive strength.

9.2.4 Register 0Bh (Address = 0x0B) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-8. Register 0Bh

15	14	13	12	11	10	9	8
RESERVED				DIG_DELAY_D3[2:0]			DIG_DELAY_D2[2:0]
R/W-0000b				R/W-000b			R/W-000b
7	6	5	4	3	2	1	0
DIG_DELAY_D2[2:0]			DIG_DELAY_D1[2:0]			DIG_DELAY_D0[2:0]	
R/W-000b			R/W-000b			R/W-000b	

Table 9-12. Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.
11:9	DIG_DELAY_D3[2:0]	R/W	000b	Programmable digital delay on D3. 000b = 0ns delay. 001b = 1ns delay. 010b = 2ns delay. 011b = 3ns delay. 100b = 4ns delay. 101b = 5ns delay.
8:6	DIG_DELAY_D2[2:0]	R/W	000b	Programmable digital delay on D2. 000b = 0ns delay. 001b = 1ns delay. 010b = 2ns delay. 011b = 3ns delay. 100b = 4ns delay. 101b = 5ns delay.
5:3	DIG_DELAY_D1[2:0]	R/W	000b	Programmable digital delay on D1. 000b = 0ns delay. 001b = 1ns delay. 010b = 2ns delay. 011b = 3ns delay. 100b = 4ns delay. 101b = 5ns delay.
2:0	DIG_DELAY_D0[2:0]	R/W	000b	Programmable digital delay on D0. 000b = 0ns delay. 001b = 1ns delay. 010b = 2ns delay. 011b = 3ns delay. 100b = 4ns delay. 101b = 5ns delay.

9.2.5 Register 0Ch (Address = 0x0C) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-9. Register 0Ch

15	14	13	12	11	10	9	8
RESERVED						PD_REF[1:0]	
R/W-000000b						R/W-00b	
7	6	5	4	3	2	1	0
RESERVED	CLK_PWR[2:0]			RESERVED			
R/W-0b	R/W-000b			R/W-0000b			

Table 9-13. Register 0Ch Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:8	PD_REF[1:0]	R/W	00b	ADC reference voltage source selection. 10b = Internal reference is active. 11b = Internal reference is inactive. Force an external reference via REFIO (pin 9).
7	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
6:4	CLK_PWR[2:0]	R/W	000b	Control to select the power supply domain for the input clock. 000b = IOVDD domain. 101b = VDD_1V8 domain.
3:0	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.

9.2.6 Register 0Dh (Address = 0x0D) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-10. Register 0Dh

15	14	13	12	11	10	9	8
XOR_EN[4:0]					CRC_EN	RESERVED	DATA_FORMAT
R/W-00000b					R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
SAVG_MODE[3:0]				RESERVED		AVG_SYNC	SAVG_EN
R/W-0000b				R/W-00b		R/W-0b	R/W-0b

Table 9-14. Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
15:11	XOR_EN[4:0]	R/W	00000b	Control to enable XOR operation on the ADC conversion result. 00000b = XOR operation is inactive. 01111b = Bit-wise XOR operation on the ADC conversion result is active.
10	CRC_EN	R/W	0b	Control to enable CRC on the data interface. 0b = CRC module is inactive. 1b = CRC module is active.
9	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
8	DATA_FORMAT	R/W	0b	Control to select the data format for the ADC conversion result. 0b = Two's complement format. 1b = Straight binary format.
7:4	SAVG_MODE[3:0]	R/W	0000b	Control for the number of samples to be averaged in simple averaging mode. 0000b = 2 samples averaged. 0001b = 4 samples averaged. 0010b = 8 samples averaged. 0011b = 16 samples averaged. 0100b = 32 samples averaged. 0101b = 64 samples averaged. 0110b = 128 samples averaged.
3:2	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
1	AVG_SYNC	R/W	0b	Synchronization control for the internal averaging filter. Write 1b to trigger when averaging must start from the subsequent cycle.
0	SAVG_EN	R/W	0b	Control to enable simple averaging. Select the number of samples to be averaged in SAVG_MODE. 0b = Simple averaging is inactive. 1b = Simple averaging is active.

9.2.7 Register 0Fh (Address = 0x0F) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-11. Register 0Fh

15	14	13	12	11	10	9	8
RESERVED							
R/W-0000000000b							
7	6	5	4	3	2	1	0
RESERVED		TEST_PATT_INCR[1:0]		TEST_PATT_MODE[1:0]		RESERVED	TEST_PATT_EN
R/W-0000000000b		R/W-00b		R/W-00b		R/W-0b	R/W-0b

Table 9-15. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R/W	0000000000b	Reserved. Do not change from the default reset value.
5:4	TEST_PATT_INCR[1:0]	R/W	00b	Increment value for the ramp pattern output. 00b = 1024 01b = 2048 10b = 3072 11b = 4096
3:2	TEST_PATT_MODE[1:0]	R/W	00b	Type of test pattern at the data interface. 00b = ADC outputs constant pattern defined in TEST_PATT_1 in address 0x10 and TEST_PATT_2 in address 0x11 for ADC A and ADC B respectively. 01b = Ramp pattern. 10b = Alternate pattern between AAAA and 5555 toggled at each readout.
1	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
0	TEST_PATT_EN	R/W	0b	Control to enable digital test pattern for data. 0b = ADC conversion result is launched on the data interface. 1b = Digital test pattern is launched on the data interface.

9.2.8 Register 10h (Address = 0x10) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-12. Register 10h

15	14	13	12	11	10	9	8
TEST_PATT_1[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TEST_PATT_1[15:0]							
R/W-0000000000000000b							

Table 9-16. Register 10h Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TEST_PATT_1[15:0]	R/W	0000000000000000b	16-bit test pattern corresponding to ADC A.

9.2.9 Register 11h (Address = 0x11) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-13. Register 11h

15	14	13	12	11	10	9	8
TEST_PATT_2[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TEST_PATT_2[15:0]							
R/W-0000000000000000b							

Table 9-17. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TEST_PATT_2[15:0]	R/W	0000000000000000b	16-bit test pattern corresponding to ADC B.

9.2.10 Register 13h (Address = 0x13) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-14. Register 13h

15	14	13	12	11	10	9	8
RESERVED						CSZ_CONVST_SHORT_EN[2:0]	
R/W-000000b						R/W-000b	
7	6	5	4	3	2	1	0
CSZ_CONVST_SHORT_EN[2:0]	RESERVED						
R/W-000b	R/W-0000000b						

Table 9-18. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:7	CSZ_CONVST_SHORT_EN[2:0]	R/W	000b	Control to enable $\overline{CS}$-CONVST short mode. 000b = Normal device operation. 101b = $\overline{CS}$-CONVST short mode is active.
6:0	RESERVED	R/W	0000000b	Reserved. Do not change from the default reset value.

9.3 Register Bank 2

Table 9-19 lists the memory-mapped registers for the register bank 2 registers. Consider all register offset addresses not listed in Table 9-19 as reserved locations and do not modify the register contents.

Table 9-19. Register Map Bank 2

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	Register 09h	RESERVED							
		RESERVED			PD_REFBUF	RESERVED			

Complex bit access types are encoded to fit into small table cells. Table 9-20 shows the codes that are used for access types in this section.

Table 9-20. Register Bank 2 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.3.1 Register 09h (Address = 0x09) [Reset = 0x0000]

Return to the Summary Table.

Figure 9-15. Register 09h

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000000b							
7	6	5	4	3	2	1	0
RESERVED			PD_REFBUF	RESERVED			
R/W-00000000000b			R/W-0b	R/W-0000b			

Table 9-21. Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED	R/W	00000000000b	Reserved. Do not change from the default reset value.
4	PD_REFBUF	R/W	0b	Control to power down the internal reference buffer. 0b = Internal reference buffer is active. 1b = Internal reference buffer is inactive. Use an external reference buffer and connect the external reference to the REFIO and REF_CAP pins.
3:0	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The ADS932x with integrated averaging filters enables a low-latency, precision measurement of DC and AC signals. The following section gives an example circuit and recommendations for using the ADS932x to measure the analog $1V_{pp}$ output of sine-cosine encoders.

10.2 Typical Application

10.2.1 Analog $1V_{PP}$ Sine-Cosine Encoder Interface

The application circuit in Figure 10-1 shows a 2-channel circuit to measure the output of an analog $1V_{pp}$ sine-cosine encoder. Use the THS4552 as the fully differential amplifier that drives the ADS932x.

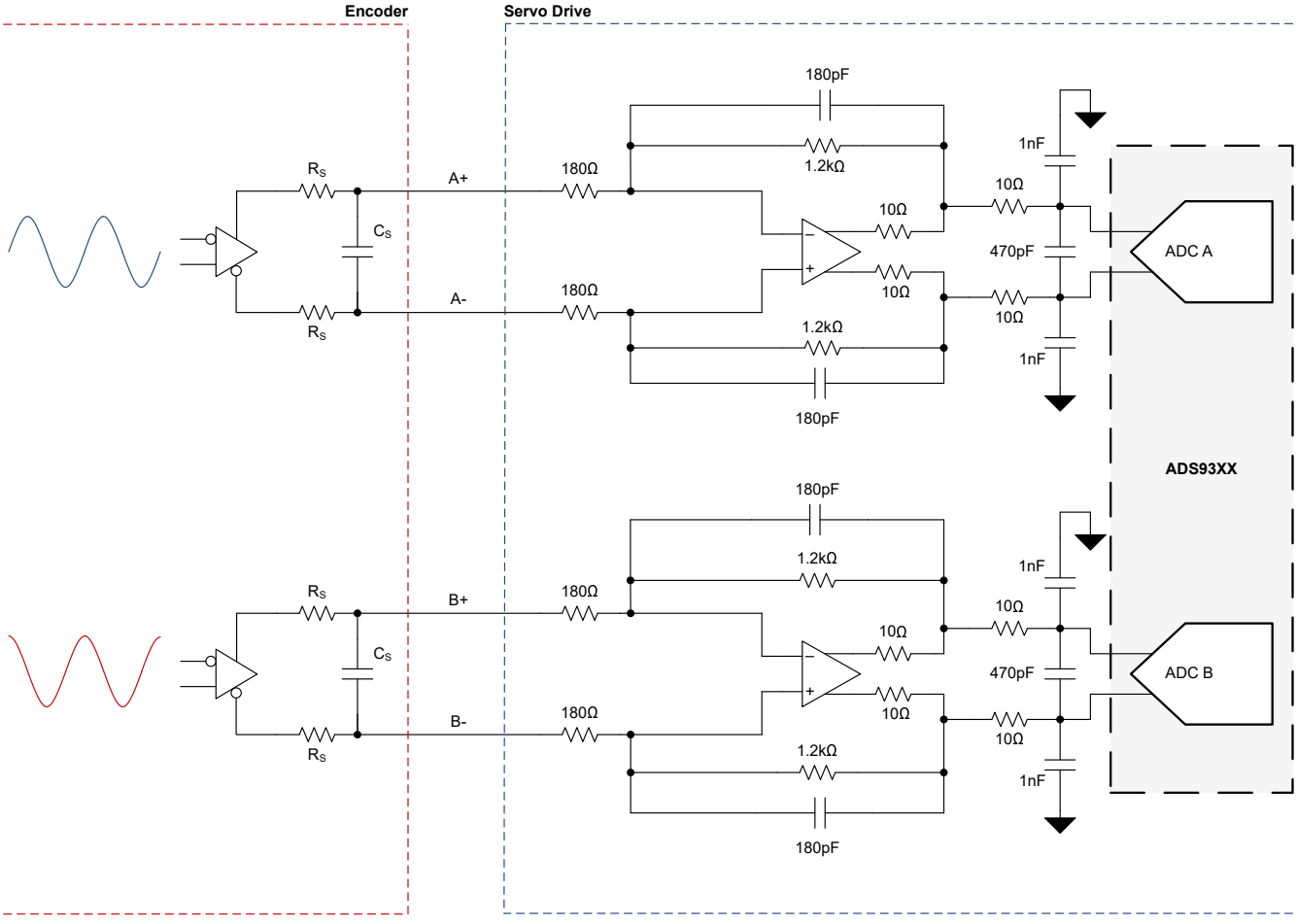


Figure 10-1. Sine-Cosine Encoder Interface Circuit With 500kHz Input Signal Bandwidth

10.2.2 Design Requirements

Table 10-1 lists the parameters for a $1V_{PP}$ sine-cosine encoder interface.

Table 10-1. Design Parameters

PARAMETER	VALUE
ADC resolution	16 bits
SNR	> 90dB
−3dB signal bandwidth	> 500kHz

10.2.3 Detailed Design Procedure

A typical encoder with an analog $1V_{pp}$ output has a maximum signal frequency of 500kHz. The −3dB cutoff frequency of the fully differential amplifier (FDA) circuit is designed for greater than 500kHz. Thus, supporting signals up to the maximum signal frequency of the encoder output. Choose the FDA such that the FDA settles the transient switching load from the sampling capacitor of the ADC within the ADC acquisition time (t_{ACQ}).

The output of a sine-cosine encoder has a typical amplitude of $1V_{pp}$ with a maximum amplitude of $1.2V_{pp}$. The full-scale range of the ADS932x is $\pm V_{REF}$, where the typical value of V_{REF} is 4.096V. To use the input range of the ADC, the gain of the FDA circuit is set to 6.8V/V.

To improve the SNR of the signal chain, the ADS932x offers integrated averaging filters as described in the *Programmable Data Averaging Filter* section. The results are shown in Table 10-2, which includes the typical SNR of the circuit with different averaging window sizes.

Table 10-2. THS4552 and ADS932x Data Summary

AVERAGING WINDOW SIZE (Simple Average)	OUTPUT DATA RATE (MSPS)	SNR (dB)	ENOB (Bits)
0	5	93.5	15.23
2	2.5	96.7	15.77
4	1.25	99	16.15
8	0.625	101.1	16.5
16	0.3125	102.6	16.75
32	0.15625	103.9	16.96
64	0.078125	105.2	17.18
128	0.0390625	105.9	17.29

10.3 Power Supply Recommendations

The ADS932x has three separate power supplies: AVDD, VDD_1V8, and IOVDD. There is no requirement for a specific power-up sequence. The data and configuration digital interfaces are powered by IOVDD. Figure 10-2 shows the decoupling capacitor connections for the respective power supplies. Make sure each power-supply pin has separate decoupling capacitors.

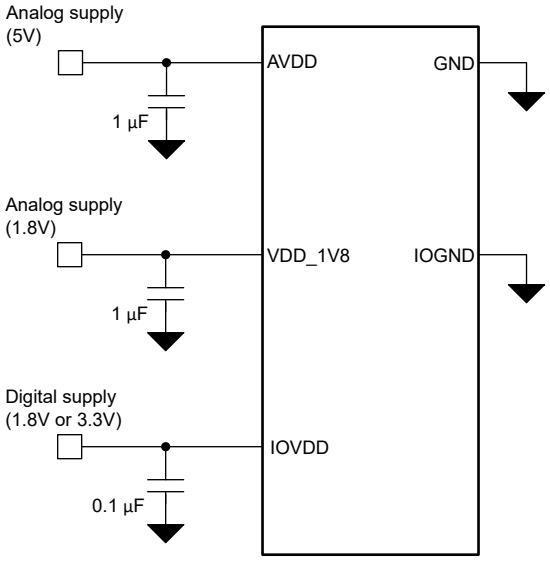


Figure 10-2. Power-Supply Decoupling

10.4 Layout

10.4.1 Layout Guidelines

Figure 10-3 illustrates a board layout example for the ADS932x. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources. Use 1µF ceramic bypass capacitors in close proximity to the analog (AVDD and VDD_1V8), and digital (IOVDD) power-supply pins. Avoid placing vias between the power-supply pins and bypass capacitors. Place the reference decoupling capacitor close to the device REF_CAP and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND and REFM pins to a ground plane using short, low-impedance paths.

10.4.2 Layout Example

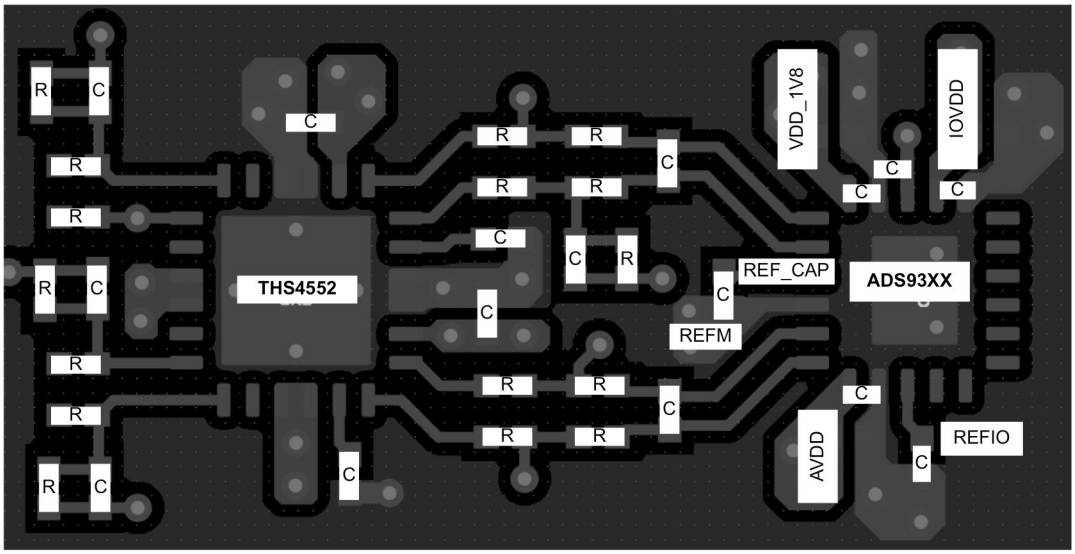


Figure 10-3. Example Layout

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *REF70 2ppm/°C Maximum Drift, 0.23 ppmp-p 1/f Noise, Precision Voltage Reference* data sheet
- Texas Instruments, *THS4552 Dual-Channel, Low-Noise, Precision, 150MHz, Fully Differential Amplifier* data sheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

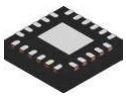
Changes from Revision * (April 2025) to Revision A (September 2025)	Page
• Changed the device status from Advanced to Production Data	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Mechanical Data

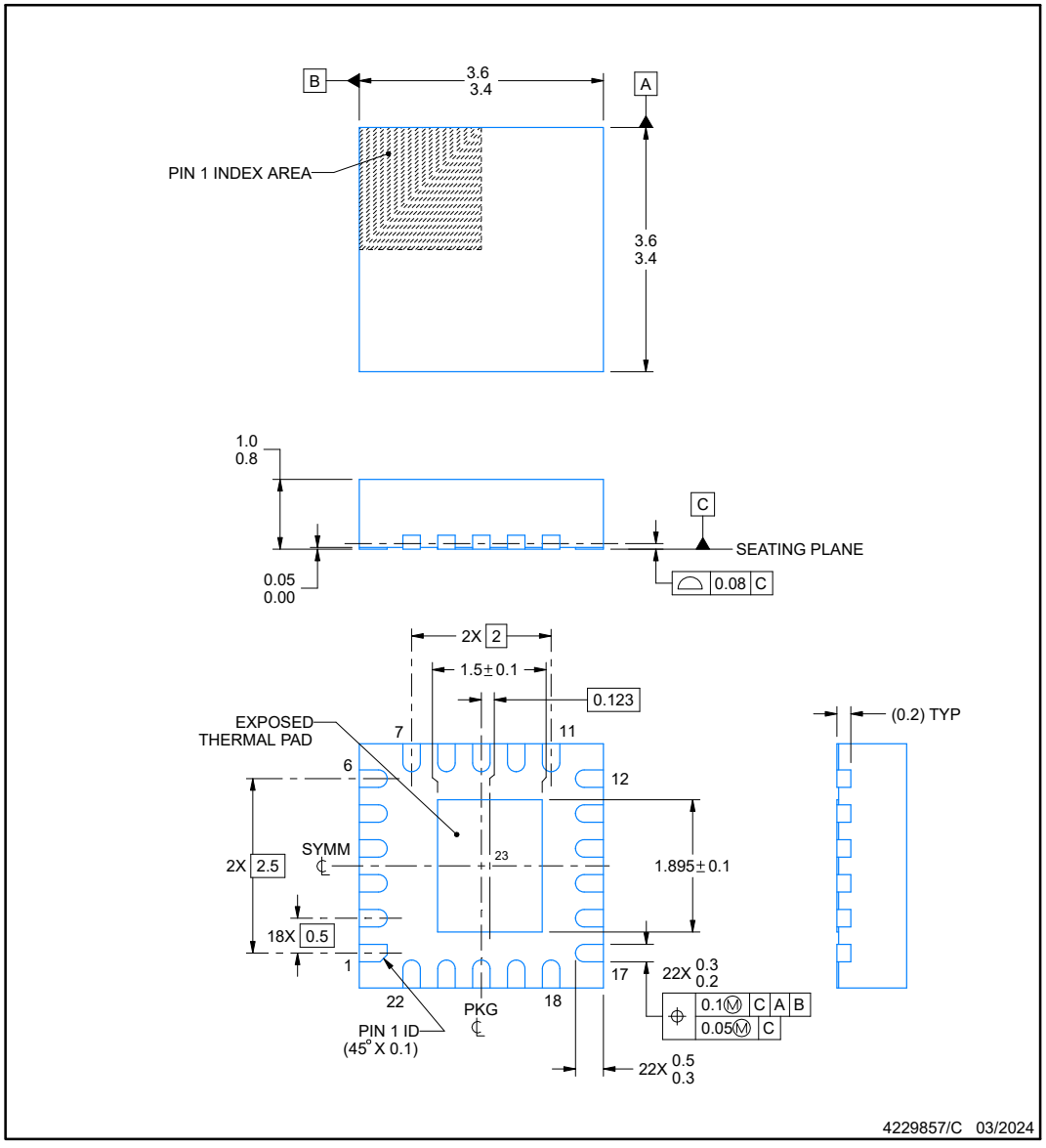
VAE0022A



PACKAGE OUTLINE

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



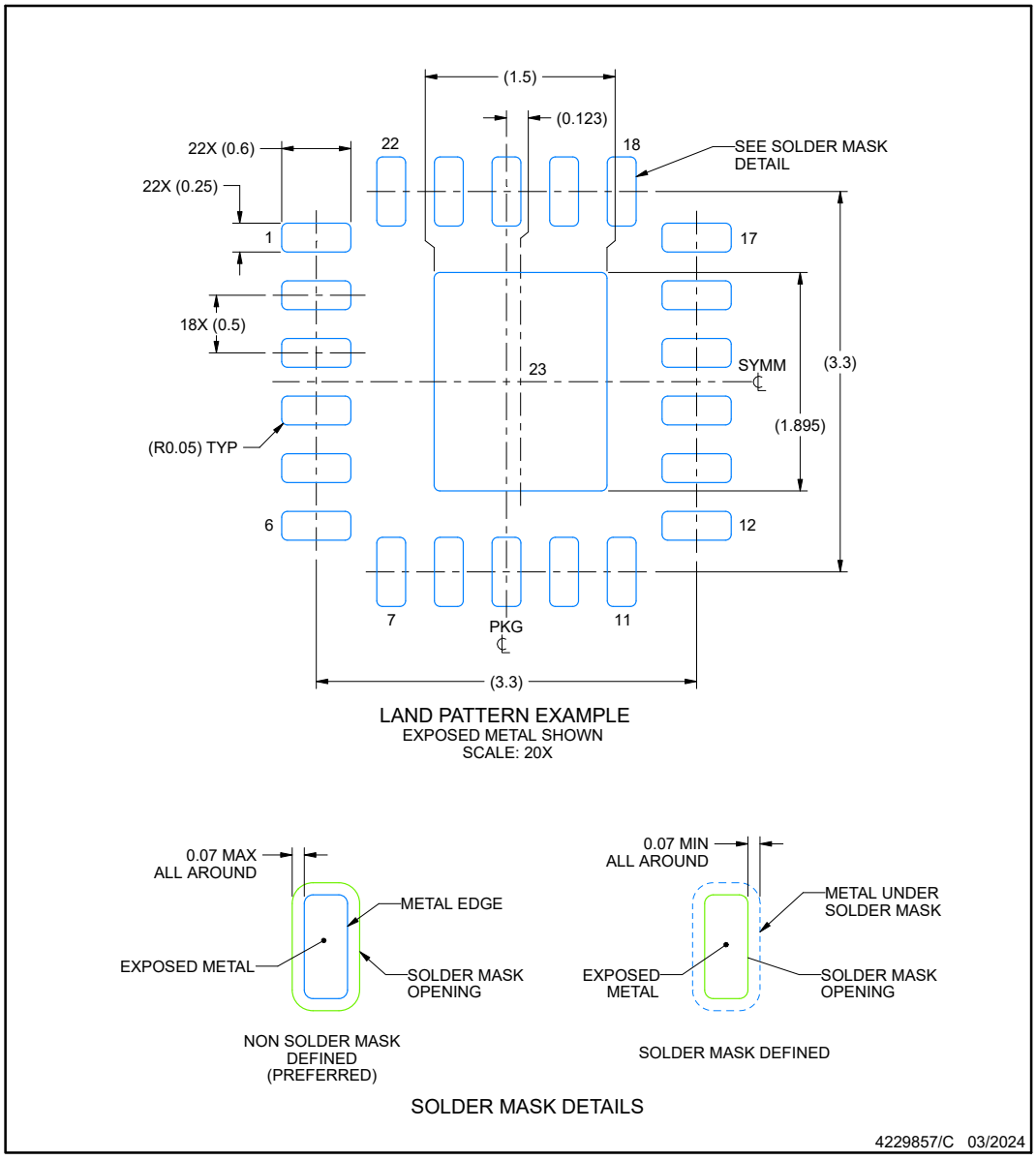
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

VAE0022A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



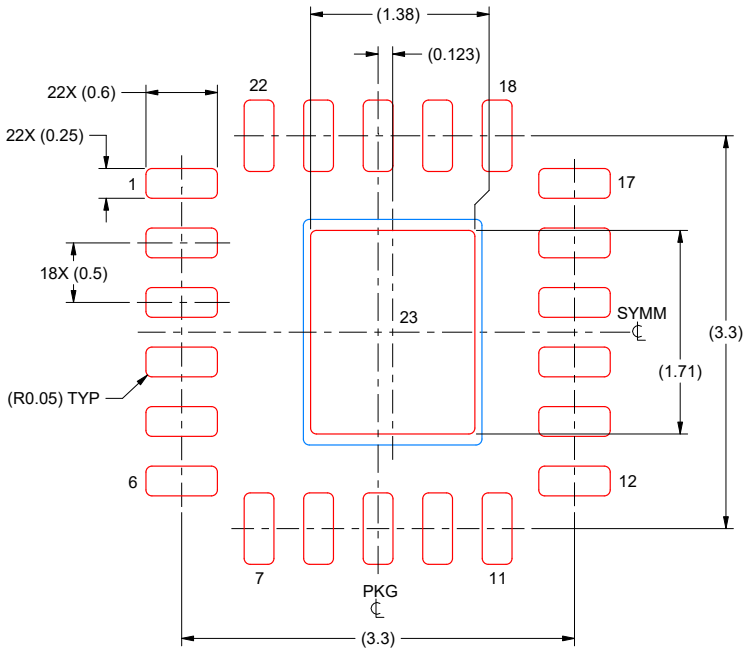
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VAE0022A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 23:
83% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229857/C 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PADS9326VAER	Active	Preproduction	VQFN-HR (VAE) | 22	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PADS9327VAER	Active	Preproduction	VQFN-HR (VAE) | 22	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

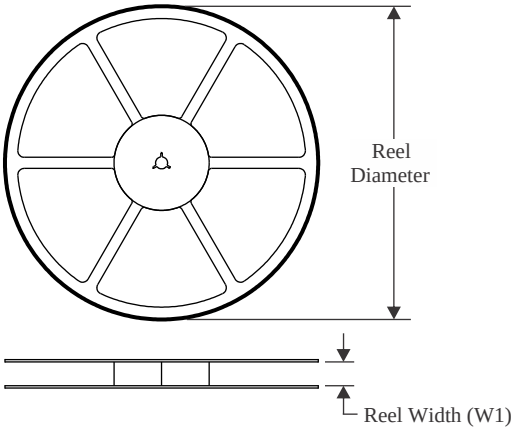
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

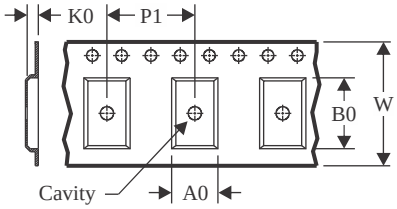
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

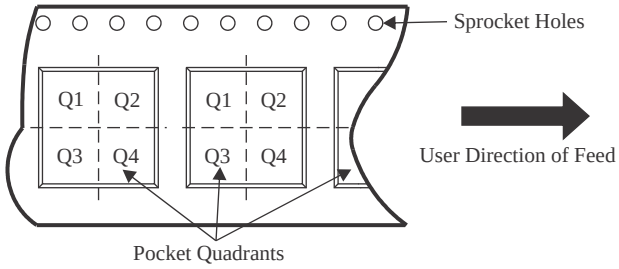


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

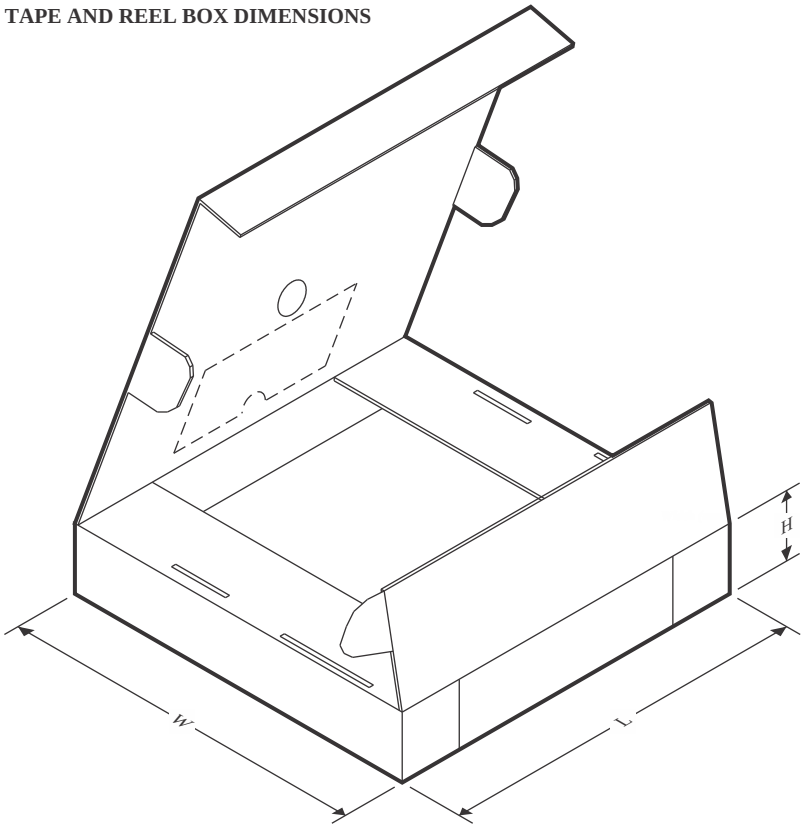
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS9327VAER	VQFN-HR	VAE	22	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS9327VAER	VQFN-HR	VAE	22	3000	367.0	367.0	35.0

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