

12-BIT, 3-MSPS, MICROPOWER, MINIATURE SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 3-MHz Sample Rate Serial Device
- 12-Bit Resolution
- Zero Latency
- 48-MHz Serial Interface
- Supply Range: 2.7 V to 5.5 V
- Low Power Dissipation:
 - 6.45 mW at 3-V V_{DD} , 2 MSPS
 - 13.5 mW at 5-V V_{DD} , 3 MSPS
- ± 0.6 LSB INL, ± 0.5 LSB DNL
- 72 dB SINAD, –84 dB THD
- Unipolar Input Range: 0 V to V_{DD}
- Power-Down Current: 1 μ A
- Wide Input Bandwidth: 30 MHz at 3 dB
- 6-Pin SOT23 Package

APPLICATIONS

- Base Band Converters in Radio Communication
- Motor Current/Bus Voltage Sensors in Digital Drives
- Optical Networking (DWDM, MEMS Based Switching)
- Optical Sensors
- Battery Powered Systems
- Medical Instrumentations
- High-Speed Data Acquisition Systems
- High-Speed Closed-Loop Systems

DESCRIPTION

The ADS7883 is a 12-bit, 3-MSPS analog-to-digital converter (ADC). The device includes a capacitor based SAR A/D converter with inherent sample and hold. The serial interface in the device is controlled by the $\overline{CS}$ and SCLK signals for glueless connections with microprocessors and DSPs. The input signal is sampled with the falling edge of $\overline{CS}$, and SCLK is used for conversion and serial data output.

The device operates from a wide supply range from 2.7 V to 5.5 V. The low power consumption of the device makes it suitable for battery-powered applications. The device also includes a power saving power-down feature for when the device is operated at lower conversion speeds.

The high level of the digital input to the device is not limited to device V_{DD} . Therefore the digital input can go as high as 5.5 V when the device supply is 2.7 V. This feature is useful when digital signals are received from another circuit with different supply levels. This also reduces restrictions on power-up sequencing.

The ADS7883 is available in a 6-pin SOT23 package and is specified for operation from –40°C to 125°C.

MicroPower Miniature SAR Converter Family

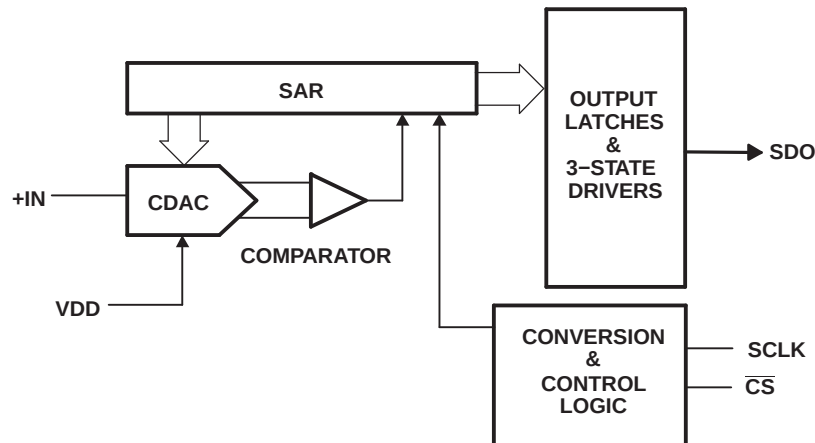
BIT	< 300 KSPS	300 KSPS – 1.25 MSPS	3 MSPS	
12-Bit	ADS7866 (1.2 V_{DD} to 3.6 V_{DD})	ADS7886 (2.35 V_{DD} to 5.25 V_{DD})	ADS7883	3 MSPS for 4.5 V_{DD} to 5.5 V_{DD} 2 MSPS for 2.7 V_{DD} to 4.5 V_{DD}
10-Bit	ADS7867 (1.2 V_{DD} to 3.6 V_{DD})	ADS7887 (2.35 V_{DD} to 5.25 V_{DD})	ADS7884 (2.7 V_{DD} to 5.5 V_{DD})	
8-Bit	ADS7868 (1.2 V_{DD} to 3.6 V_{DD})	ADS7888 (2.35 V_{DD} to 5.25 V_{DD})	ADS7885 (2.7 V_{DD} to 5.5 V_{DD})	



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



PACKAGE/ORDERING INFORMATION⁽¹⁾

DEVICE	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS7883SB	±1	±1	12	6-Pin SOT23	DBV	–40°C to 125°C	7883	ADS7883SDBVBT	Small Tape and Reel 250
							7883	ADS7883SDBBVR	Large Tape and Reel 3000
ADS7883S	±2	±2	11				7883	ADS7883SDBVBT	Small Tape and Reel 250
							7883	ADS7883SDBBVR	Large Tape and Reel 3000

(1) For most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

			UNIT
+IN to AGND			–0.3 V to +V _{DD} +0.3 V
+V _{DD} to AGND			–0.3 V to 7.0 V
Digital input voltage to GND			–0.3 V to (7.0 V)
Digital output to GND			–0.3 V to (+V _{DD} + 0.3 V)
Operating temperature range			–40°C to 125°C
Storage temperature range			–65°C to 150°C
Junction temperature (T _J Max)			150°C
Power dissipation, SOT23 package			(T _J Max–T _A)/θ _{JA}
Thermal impedance, θ _{JA}	SOT23		295.2°C/W
Lead temperature, soldering	Vapor phase (60 sec)		215°C
	Infrared (15 sec)		220°C

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }125^\circ\text{C}$, $f_{\text{sample}} = 2\text{ MSPS for }V_{DD} = 2.7\text{ V to }4.5\text{ V}$, $f_{\text{sample}} = 3\text{ MSPS for }V_{DD} = 4.5\text{ V to }5.5\text{ V}$

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUT								
Full-scale input voltage span ⁽¹⁾					0		V _{DD}	V
Absolute input voltage range			+IN		−0.2		V _{DD} +0.2	V
C _I	Input capacitance ⁽²⁾				27			pF
I _{Ilkg}	Input leakage current		T _A = 125°C		40			nA
SYSTEM PERFORMANCE								
Resolution					12			Bits
No missing codes		ADS7883SB			12			Bits
		ADS7883S			11			
INL	Integral nonlinearity	ADS7883SB			−1	±0.6	1	LSB ⁽³⁾
		ADS7883S			−2	±0.75	2	
DNL	Differential nonlinearity	ADS7883SB			−1	±0.5	1	LSB
		ADS7883S			−2	±0.75	2	
E _O	Offset error ⁽⁴⁾⁽⁵⁾⁽⁶⁾				−3	±0.2	3	LSB
E _G	Gain error ⁽⁵⁾				−3.5	±0.3	3.5	LSB
SAMPLING DYNAMICS								
Conversion time			32-MHz SCLK, V _{DD} = 3 V		398	422	ns	
			48-MHz SCLK, V _{DD} = 5 V		265	281		
Acquisition time			32-MHz SCLK, V _{DD} = 3 V		78		ns	
			48-MHz SCLK, V _{DD} = 5 V		52			
Maximum throughput rate			32-MHz SCLK, V _{DD} = 2.7 V to 4.5 V		2			MHz
			48-MHz SCLK, V _{DD} = 4.5 V to 5.5 V		3			
Aperture delay					10			ns
DYNAMIC CHARACTERISTICS								
THD	Total harmonic distortion ⁽⁷⁾		f _I = 100 kHz		−84			dB
SINAD	Signal-to-noise and distortion		f _I = 100 kHz, ADS7883SB		69	72	dB	
			f _I = 100 kHz, ADS7883S		68	70		
SFDR	Spurious free dynamic range		f _I = 100 kHz		86			dB
Full power bandwidth			At −3 dB		30			MHz
DIGITAL INPUT/OUTPUT								
Logic family — CMOS								
V _{IH}	High-level input voltage		V _{DD} = 2.7 V to 3.6 V		1.5		5.5	V
			V _{DD} = 3.6 V to 5.5 V		2.2		5.5	
V _{IL}	Low-level input voltage		V _{DD} = 2.7 V to 3.6 V				0.4	V
			V _{DD} = 3.6 V to 5.5 V				0.8	
V _{OH}	High-level output voltage		At I _{source} = 200 μA		V _{DD} −0.2			V
V _{OL}	Low-level output voltage		At I _{sink} = 200 μA		0.4			
POWER SUPPLY REQUIREMENTS								
+V _{DD}	Supply voltage				2.7	3.3	5.5	V

(1) Ideal input span; does not include gain or offset error

(2) Refer to [Figure 24](#) for details on sampling circuit

(3) LSB means least significant bit

(4) Measured relative to an ideal full-scale input

(5) Offset error and gain error ensured by characterization

(6) First transition of 000H to 001H at $(V_{\text{ref}}/2^{10})$

(7) Calculated on the first nine harmonics of the input frequency

ELECTRICAL SPECIFICATIONS (continued)

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $T_A = -40^{\circ}\text{C to }125^{\circ}\text{C}$, $f_{\text{sample}} = 2\text{ MSPS}$ for $V_{DD} = 2.7\text{ V to }4.5\text{ V}$, $f_{\text{sample}} = 3\text{ MSPS}$ for $V_{DD} = 4.5\text{ V to }5.5\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current (normal mode)	At $V_{DD} = 3\text{ V}$, 2-MSPS throughput		2.15	3	mA
	At $V_{DD} = 3\text{ V}$, Static state		1.8		
	At $V_{DD} = 5\text{ V}$, 3-MSPS throughput		2.7	4	
	At $V_{DD} = 5\text{ V}$, Static state		2		
Power-down state supply current	SCLK off			1	μA
	SCLK on (48 MHz)		90	250	
Power dissipation	$V_{DD} = 5\text{ V}$, 3 MSPS		13.5	20	mW
	$V_{DD} = 3\text{ V}$, 2 MSPS		6.45		
Power dissipation in static state	$V_{DD} = 5\text{ V}$		10	12.5	mW
	$V_{DD} = 3\text{ V}$		5.4		
Power-down time				0.1	μs
Power-up time				0.8	μs
TEMPERATURE RANGE					
Specified performance			-40	125	$^{\circ}\text{C}$

TIMING REQUIREMENTS (see Figure 21)

All specifications typical at $T_A = -40^{\circ}\text{C to }125^{\circ}\text{C}$, $V_{DD} = 2.7\text{ V to }5.5\text{ V}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
t_{conv} Conversion time	$V_{DD} = 3\text{ V}$			$13.5 \times t_{\text{SCLK}}$	ns
	$V_{DD} = 5\text{ V}$			$13.5 \times t_{\text{SCLK}}$	
t_{acq} Aquisition time	$V_{DD} = 3\text{ V}$	78			ns
	$V_{DD} = 5\text{ V}$	52			
t_q Minimum quiet time needed from bus 3-state to start of next conversion	$V_{DD} = 3\text{ V}$	10			ns
	$V_{DD} = 5\text{ V}$	10			
t_{d1} Delay time, $\overline{\text{CS}}$ low to first data (0) out	$V_{DD} = 3\text{ V}$		9	15	ns
	$V_{DD} = 5\text{ V}$		8	11	
t_{su1} Setup time, $\overline{\text{CS}}$ low to SCLK low	$V_{DD} = 3\text{ V}$	7			ns
	$V_{DD} = 5\text{ V}$	5			
t_{d2} Delay time, SCLK falling to SDO	$V_{DD} = 3\text{ V}$		11	20	ns
	$V_{DD} = 5\text{ V}$		9	12	
t_{h1} Hold time, SCLK falling to data valid ⁽²⁾	$V_{DD} < 3\text{ V}$	5.5			ns
	$V_{DD} > 5\text{ V}$	4			
t_{d3} Delay time, 16th SCLK falling edge to SDO 3-state	$V_{DD} = 3\text{ V}$		9	15	ns
	$V_{DD} = 5\text{ V}$		8	11	
t_{w1} Pulse duration, $\overline{\text{CS}}$	$V_{DD} = 3\text{ V}$	10			ns
	$V_{DD} = 5\text{ V}$	10			
t_{d4} Delay time, $\overline{\text{CS}}$ high to SDO 3-state,	$V_{DD} = 3\text{ V}$		9	15	ns
	$V_{DD} = 5\text{ V}$		8	11	
t_{wH} Pulse duration, SCLK high	$V_{DD} = 3\text{ V}$	$0.45 \times t_{\text{SCLK}}$			ns
	$V_{DD} = 5\text{ V}$	$0.45 \times t_{\text{SCLK}}$			
t_{wL} Pulse duration, SCLK low	$V_{DD} = 3\text{ V}$	$0.45 \times t_{\text{SCLK}}$			ns
	$V_{DD} = 5\text{ V}$	$0.45 \times t_{\text{SCLK}}$			

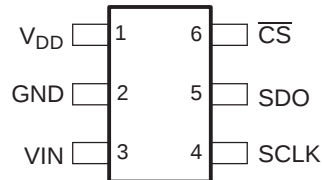
(1) 3-V Specifications apply from 2.7 V to 3.6 V, and 5-V specifications apply from 4.5 V to 5.5 V.

(2) With 10-pf load.

TIMING REQUIREMENTS (see Figure 21) (continued)

All specifications typical at $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{DD} = 2.7\text{ V}$ to 5.5 V , unless otherwise specified.

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
Frequency, SCLK		$V_{DD} = 2.7\text{ V to }4.5\text{ V}$			32	MHz
		$V_{DD} = 4.5\text{ V to }5.5\text{ V}$			48	
t_{d5}	Delay time, second falling edge of clock and $\overline{\text{CS}}$ to enter in powerdown (use min spec not to accidentally enter in powerdown) see Figure 22	$V_{DD} = 3\text{ V}$	–2		4	ns
		$V_{DD} = 5\text{ V}$	–2		3	
t_{d6}	Delay time, $\overline{\text{CS}}$ and 10th falling edge of clock to enter in powerdown (use max spec not to accidentally enter in powerdown) see Figure 22	$V_{DD} = 3\text{ V}$	–2		4	ns
		$V_{DD} = 5\text{ V}$	–2		3	

DEVICE INFORMATION
**SOT23 PACKAGE
(TOP VIEW)**

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1	–	Power supply input, also acts like a reference voltage to ADC.
GND	2	–	Ground for power supply, all analog and digital signals are referred with respect to this pin.
VIN	3	I	Analog signal input
SCLK	4	I	Serial clock
SDO	5	O	Serial data out
$\overline{\text{CS}}$	6	I	Chip select signal, active low

TYPICAL CHARACTERISTICS

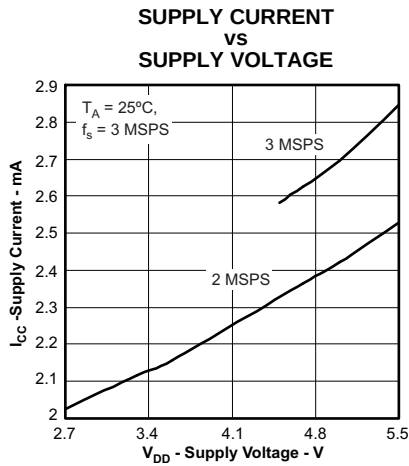


Figure 1.

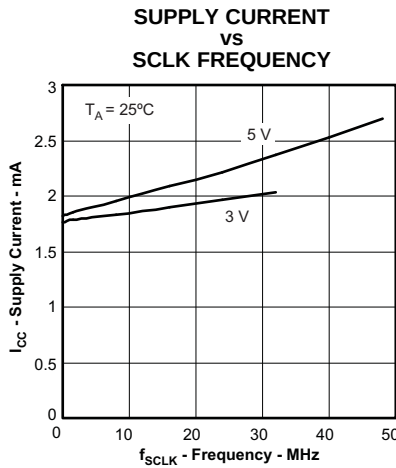


Figure 2.

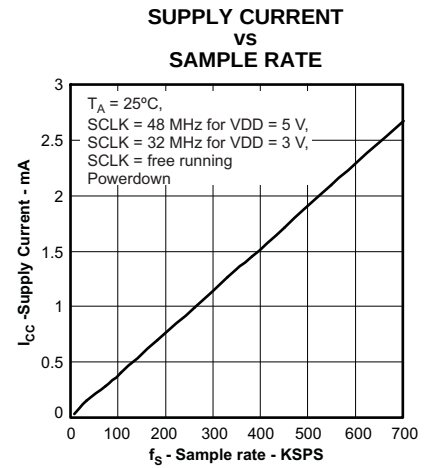


Figure 3.

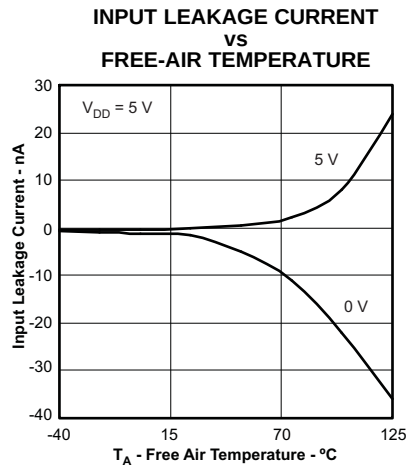


Figure 4.

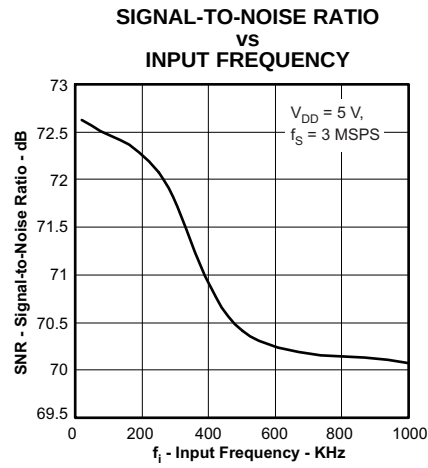


Figure 5.

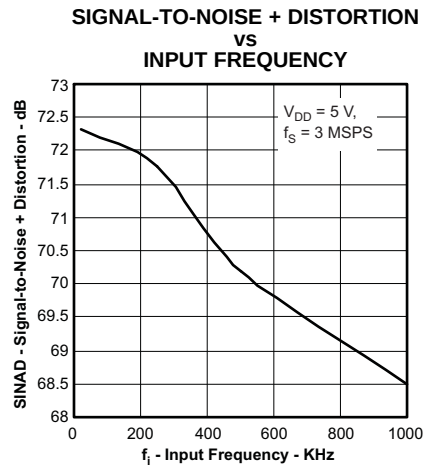


Figure 6.

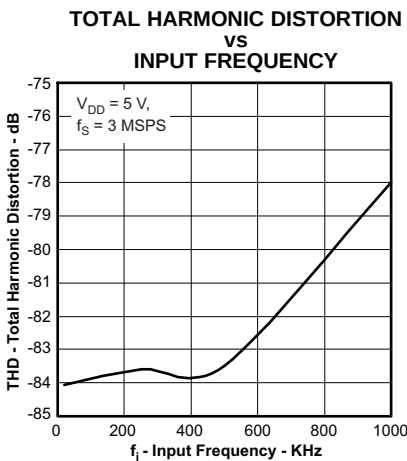


Figure 7.

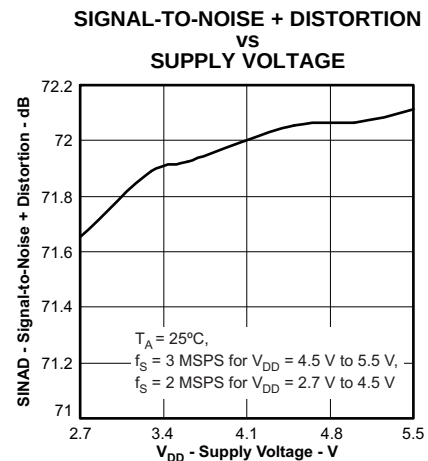


Figure 8.

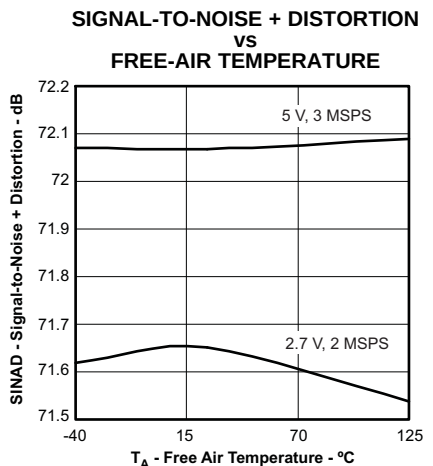


Figure 9.

TYPICAL CHARACTERISTICS (continued)

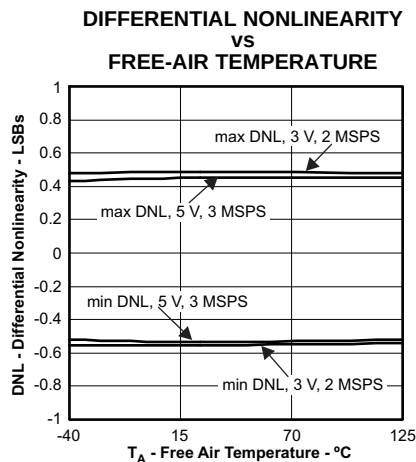


Figure 10.

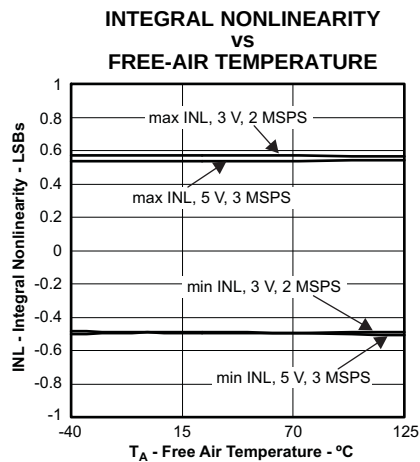


Figure 11.

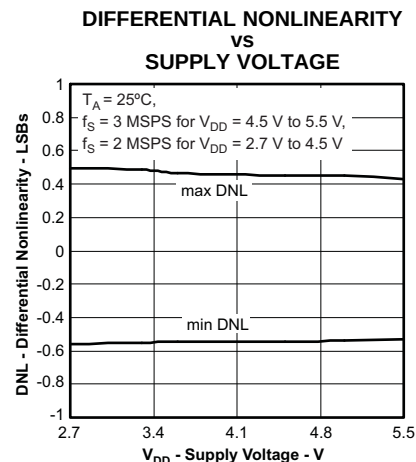


Figure 12.

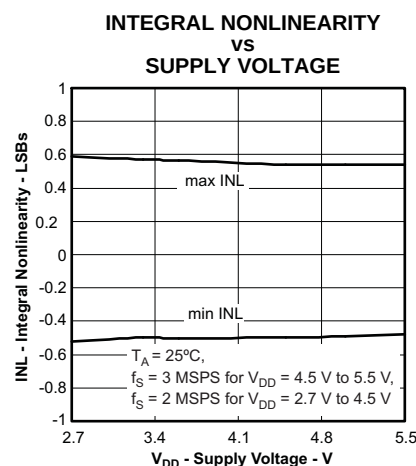


Figure 13.

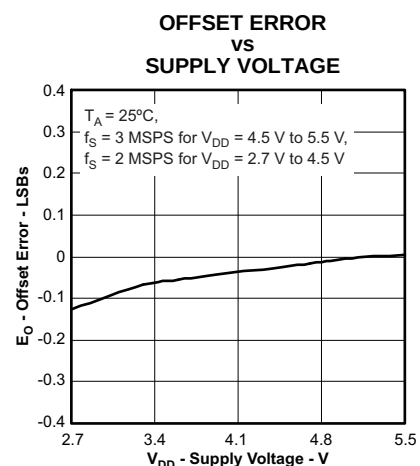


Figure 14.

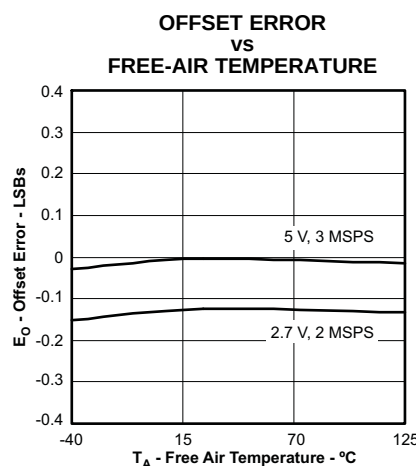


Figure 15.

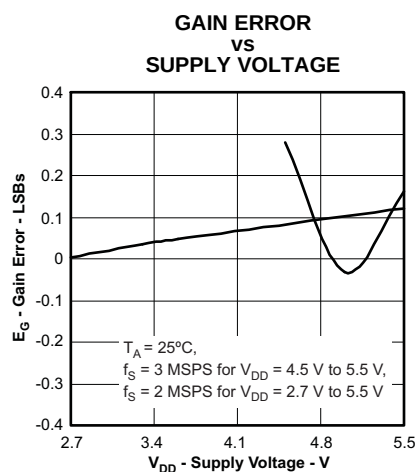


Figure 16.

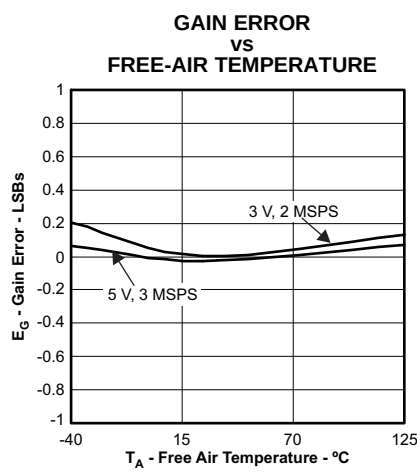


Figure 17.

TYPICAL CHARACTERISTICS (continued)

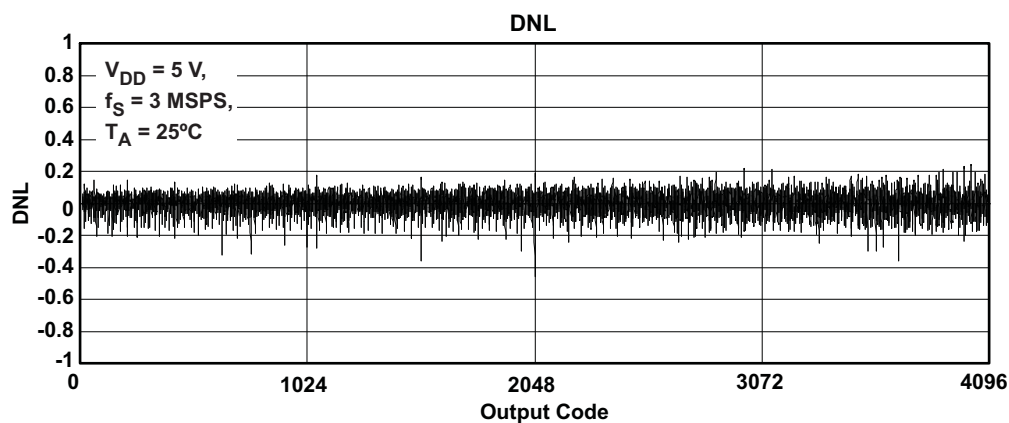


Figure 18.

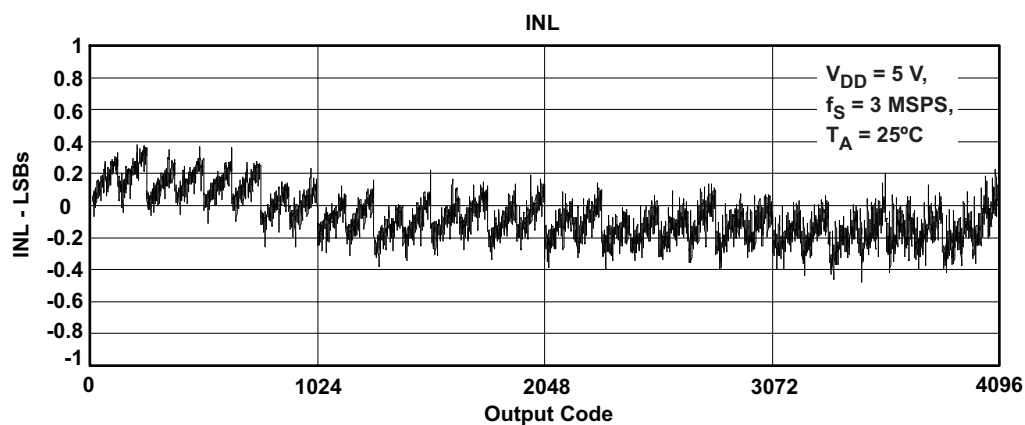


Figure 19.

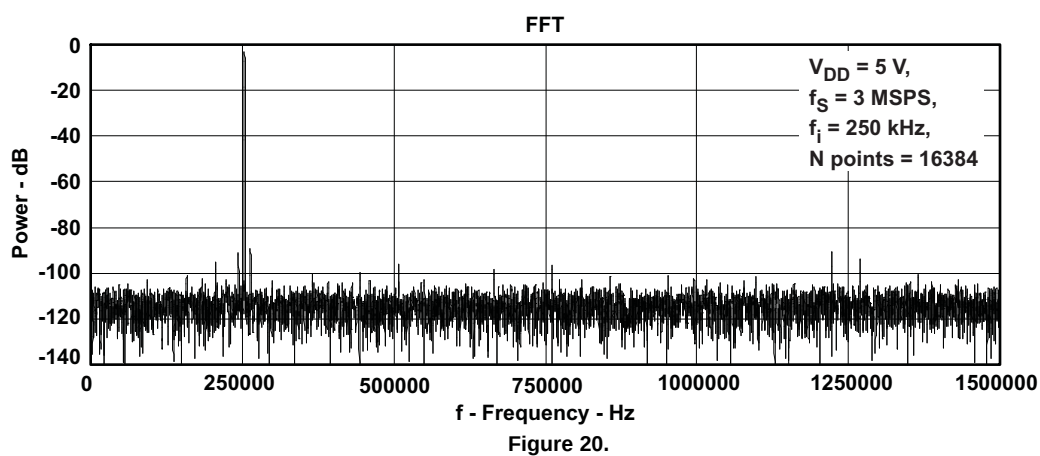


Figure 20.

NORMAL OPERATION

The cycle begins with the falling edge of $\overline{\text{CS}}$. This point is indicated as **a** in Figure 21. With the falling edge of $\overline{\text{CS}}$, the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains two leading zeros, followed by 12-bit data in MSB first format and padded by two lagging zeros.

The falling edge of $\overline{\text{CS}}$ clocks out the first zero, and a second zero is clocked out on the first falling edge of the clock. Data is in MSB first format with the MSB being clocked out on the 2nd falling edge. Data is padded with two lagging zeros as shown in Figure 21. The conversion ends on the first rising edge of SCLK after the 13th falling edge. At this point the device enters the acquisition phase. This point is indicated by **b** in Figure 21.

Figure 21 shows the device data is read in a sixteen clock frame. However, $\overline{\text{CS}}$ can be asserted (pulled high) any time after point **b**. SDO goes to 3-state with the $\overline{\text{CS}}$ high level. The next conversion should not be started (by pulling $\overline{\text{CS}}$ low) until the end of the quiet sampling time (t_q) after SDO goes to 3-state or until the minimum acquisition time (t_{acq}) has elapsed. To continue normal operation, it is necessary that $\overline{\text{CS}}$ is not pulled high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to the Power-Down Mode section for more details.) $\overline{\text{CS}}$ going high any time during the conversion aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V_{DD} . This means the digital input can go as high as 5.5 V when the device supply is 2.7 V. This feature is useful when digital signals are received from another circuit with different supply levels. Also, this relaxes the restriction on power-up sequencing. However, the digital output levels (V_{OH} and V_{OL}) are governed by V_{DD} as listed in the Electrical Specifications table.

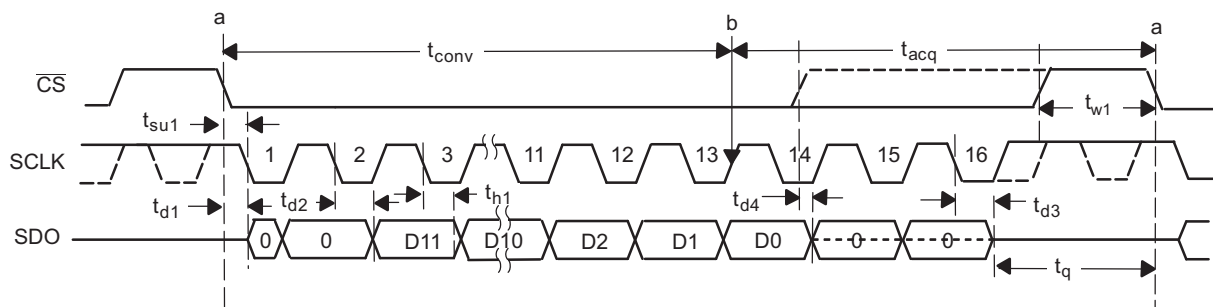


Figure 21. Interface Timing Diagram

POWER-DOWN MODE

The device enters power-down mode if $\overline{\text{CS}}$ goes high anytime after the 2nd SCLK falling edge to before the 10th SCLK falling edge. An ongoing conversion stops and SDO goes to 3-state under this power-down condition as shown in Figure 22.

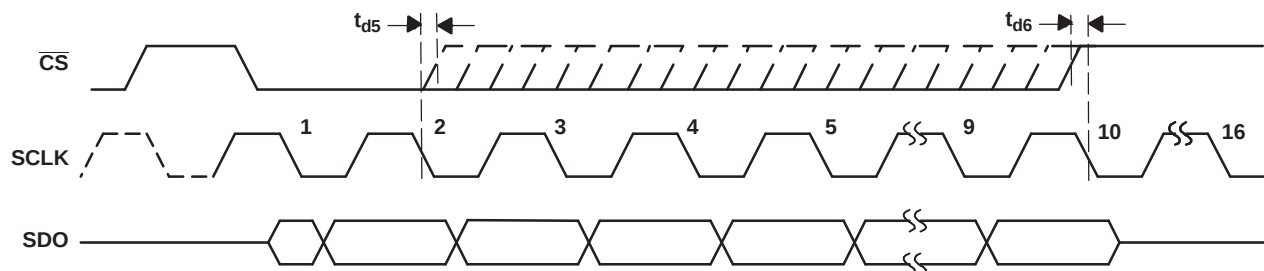


Figure 22. Entering Power-Down Mode

A dummy cycle with $\overline{\text{CS}}$ low for more than 10 SCLK falling edges brings the device out of power-down mode. For the device to reach the fully powered up condition requires $0.8\ \mu\text{s}$. $\overline{\text{CS}}$ can be pulled high any time after the 10th falling edge as shown in Figure 23. Note that the power-up time of $0.8\ \mu\text{s}$ is more than a single conversion cycle at 3-MSPS speed. This means the device requires three dummy conversion frames at 3-MSPS speed or one elongated dummy conversion frame. The data during the dummy conversion frames is invalid.

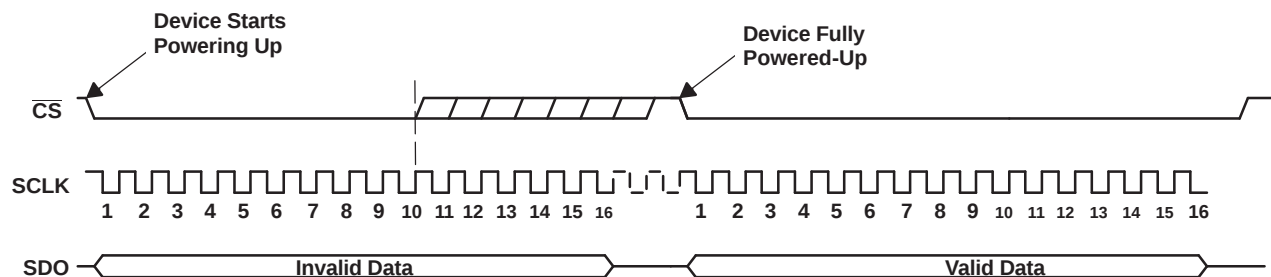


Figure 23. Exiting Power-Down Mode

APPLICATION INFORMATION

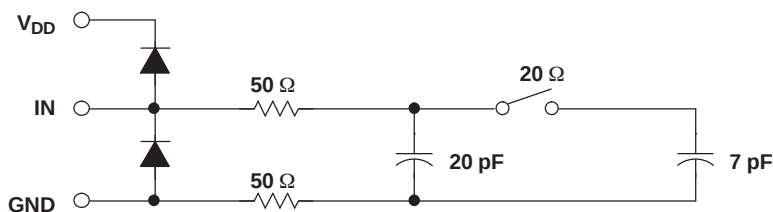


Figure 24. Typical Equivalent Sampling Circuit

Driving the VIN and VDD Pins

The VIN input to the ADS7883 should be driven with a low impedance source. In most cases additional buffers are not required. In cases where the source impedance exceeds 200 Ω, using a buffer would help achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the ADS7883 A/D converter is derived from the supply voltage internally. The device offers limited low-pass filtering functionality on-chip. The supply to these converters should be driven with a low impedance source and should be decoupled to the ground. A 1-μF storage capacitor and a 10-nF decoupling capacitor should be placed close to the device. Wide, low impedance traces should be used to connect the capacitor to the pins of the device. The ADS7883 draws very little current from the supply lines. The supply line can be driven by either:

- Directly from the system supply.
- A reference output from a low drift and low drop out reference voltage generator like the REF5030 or REF5050. The ADS7883 can operate with a wide range of supply voltages. The actual choice of the reference voltage generator depends upon the system. [Figure 26](#) shows one possible application circuit.
- A low-pass filtered version of the system supply followed by a buffer like the zero-drift OPA735 can also be used in cases where the system power supply is noisy. Care should be taken to ensure that the voltage at the VDD input does not exceed 7 V (especially during power up) to avoid damage to the converter. This can be done easily using single supply CMOS amplifiers like the OPA735. [Figure 27](#) shows one possible application circuit.

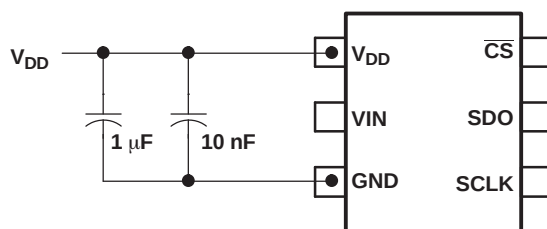


Figure 25. Supply/Reference Decoupling Capacitors

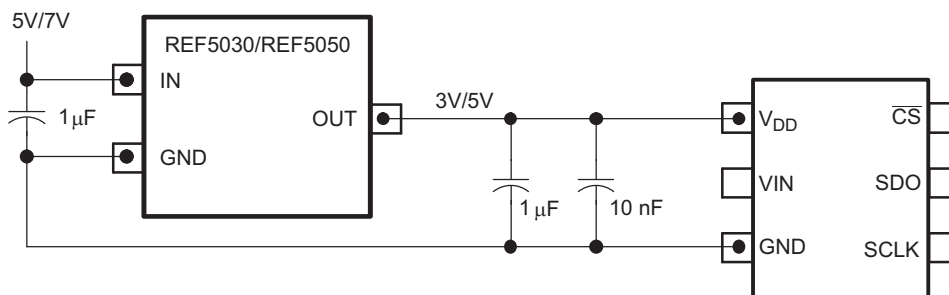


Figure 26. Using the REF5030/REF5050 Reference

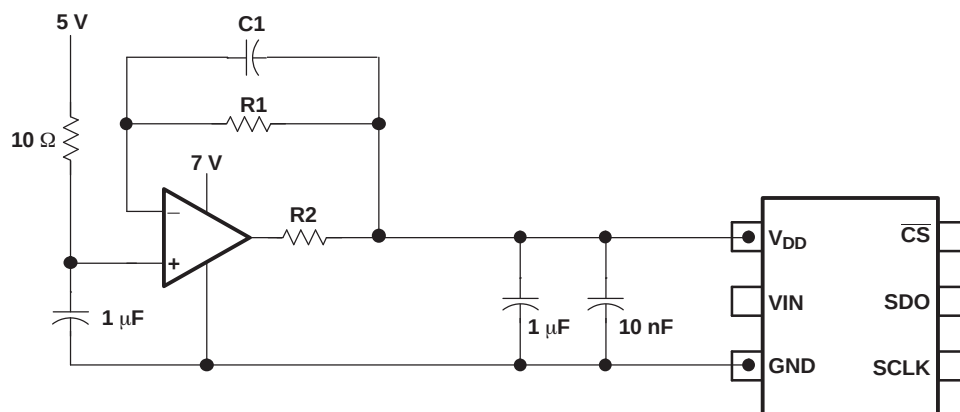


Figure 27. Buffering with the OPA735

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS7883SDBBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883
ADS7883SDBBVT	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883
ADS7883SDBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883
ADS7883SDBVT	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

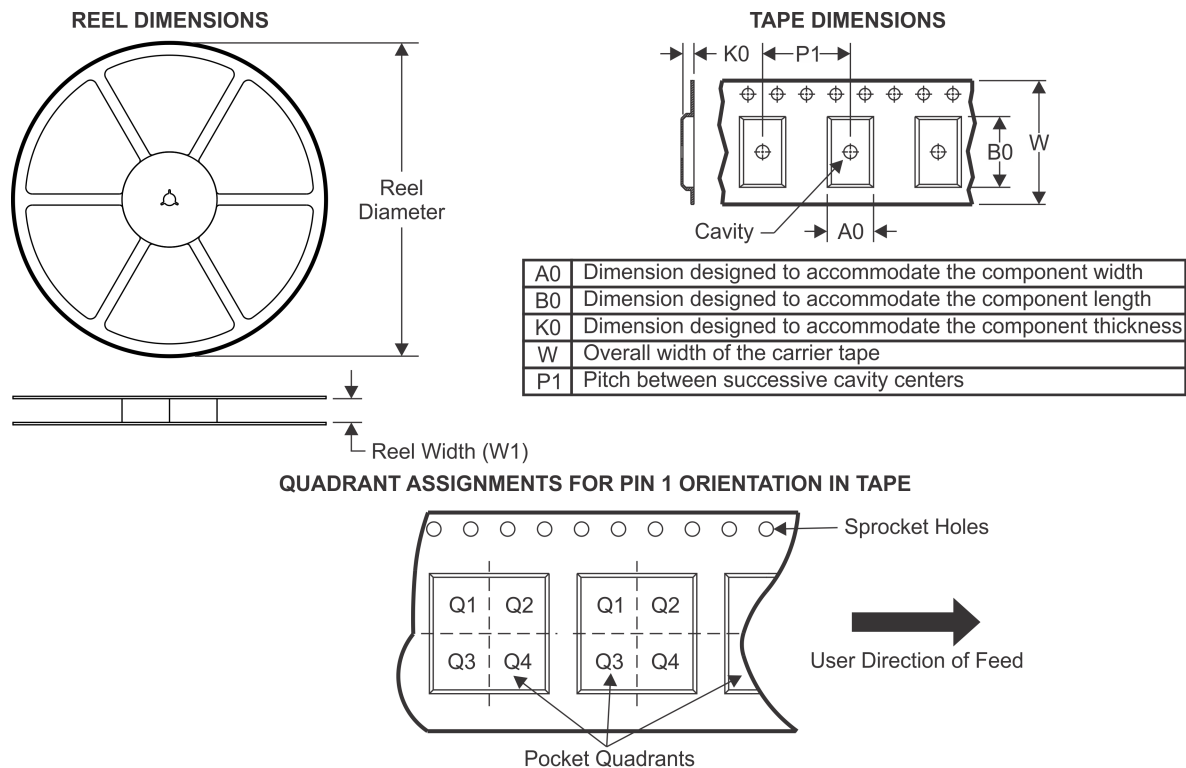
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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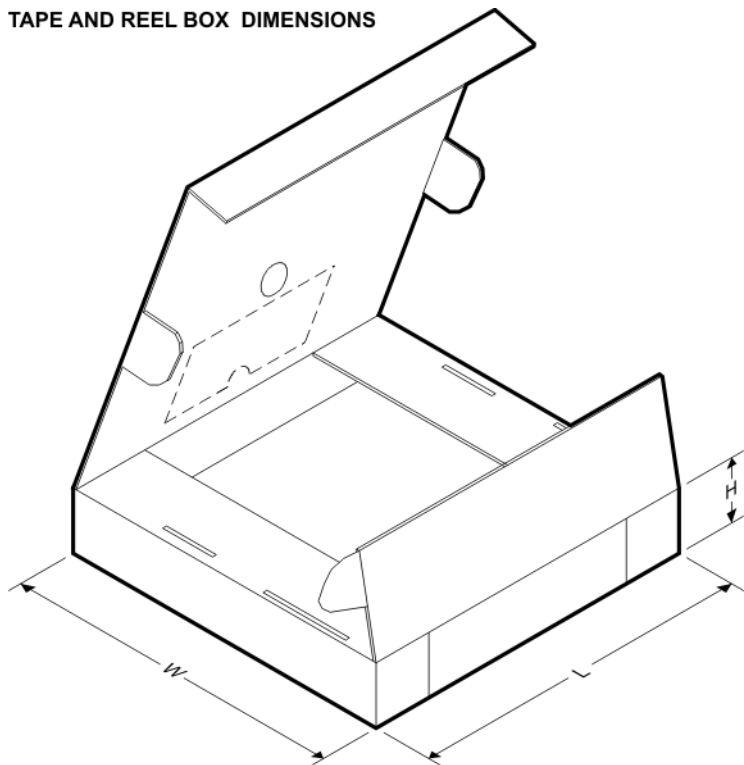
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7883SDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7883SDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7883SDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7883SDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7883SDBVVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
ADS7883SDBVVT	SOT-23	DBV	6	250	213.0	191.0	35.0
ADS7883SDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
ADS7883SDBVT	SOT-23	DBV	6	250	213.0	191.0	35.0



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



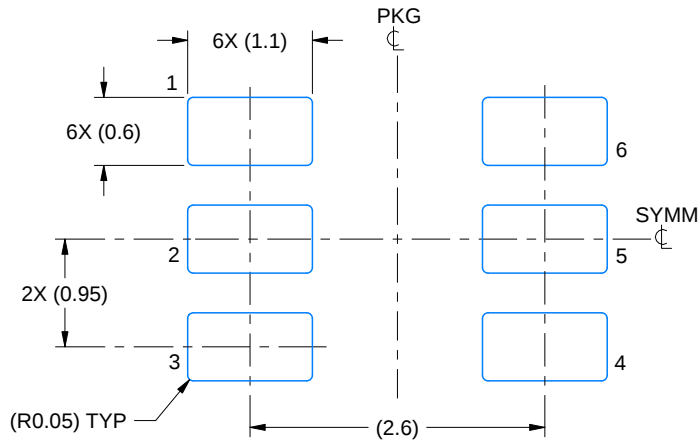
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

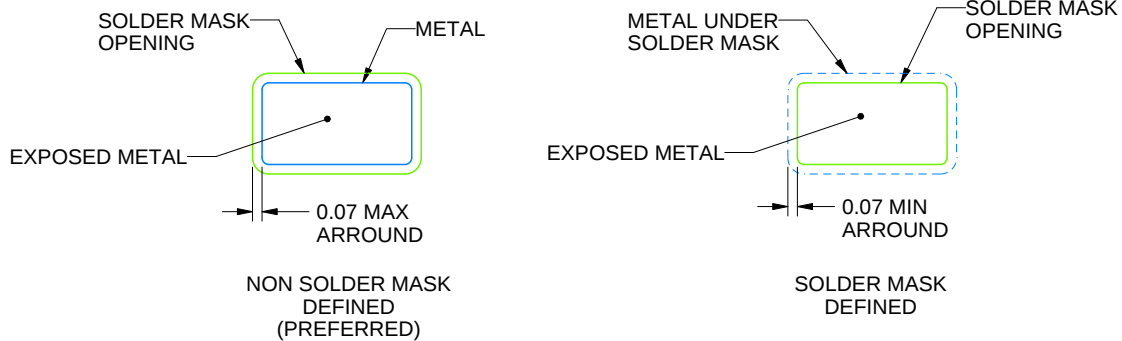
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

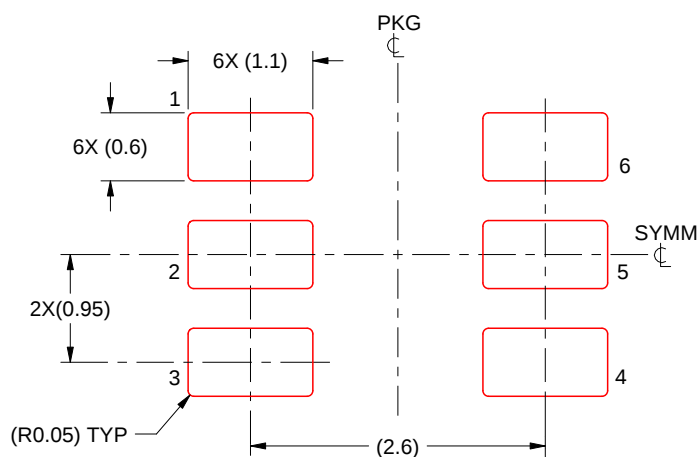
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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