



Quad-Channel, 250-MSPS Receiver and Feedback ADC

Check for Samples: ADS58H43

FEATURES

- **Quad Channel**
- **Three Different Operating Modes:**
 - 11-Bit: 250 MSPS
 - 11-Bit SNRBoost^{3G+}: 250 MSPS
 - 14-Bit: 250 MSPS (Burst Mode)
- Maximum Sampling Data Rate: 250 MSPS
- **Power Dissipation:**
 - 11-Bit Mode: 365 mW per Channel
- SNRBoost^{3G+} Bandwidth: 2x 45 MHz or 90 MHz
- Spectral Performance at 170 MHz IF (typ):
 - SNR: 70.5 dBFS in 90-MHz Band with SNRBoost3G+
 - SFDR: 85 dBc
- **DDR LVDS Digital Output Interface**
- 144-Pad BGA (10-mm × 10-mm)

APPLICATIONS

- **Multi-Carrier GSM Cellular Infrastructure Base Stations**
- Multi-Carrier Multi-Mode Cellular Infrastructure **Base Stations**
- **Active Antenna Arrays for Wireless** Infrastructures
- **Communications Test Equipment**

DESCRIPTION

The ADS58H43 is a high-linearity, quad-channel, 14bit, 250-MSPS analog-to-digital converter (ADC). The four ADC channels are separated into two blocks with two ADCs each. Each block can be individually configured into three different operating modes. One operating mode includes the implementation of the SNRBoost^{3G+} signal processing technology to provide high signal-to-noise ratio (SNR) in a band up to 90 MHz wide with only 11-bit resolution. Designed for low power consumption and high spurious-free dynamic range (SFDR), the ADC has low-noise performance and outstanding SFDR over a large input frequency range.



TRUMENTS

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE- LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN ⁽²⁾	LEAD AND BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
AD0501142	BGA-144	7CD	40°C to 105°C	GREEN (RoHS,	C. NiDdA	ADCEGLIAGI	ADS58H43IZCR	Tray
ADS58H43	BGA-144	ZCR	-40°C to +85°C	no SB or BR)	CuNiPdAu	ADS58H43I	ADS58H43IZCRR	Tape and Reel

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
- (2) These packages conform to Lead (Pb)-free and green manufacturing specifications. Additional details including specific material content can be accessed at www.ti.com/leadfree.
 - GREEN: TI defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight.
 - N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree.
 - Pb-FREE: TI defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
	AVDD33	-0.3 to +3.6	V
Supply voltage range	AVDD	−0.3 to +2.1	V
	DRVDD	-0.3 to +2.1	V
	AVSS and DRVSS	-0.3 to +0.3	V
Voltago hotwoon	AVDD and DRVDD	-2.4 to +2.4	V
Voltage between	AVDD33 and DRVDD	-2.4 to +3.9	V
	AVDD33 and AVDD	-2.4 to +3.9	V
	XINP, XINM	-0.3 to minimum (1.9, AVDD + 0.3)	V
Voltage applied to input pins	CLKP, CLKM ⁽²⁾	-0.3 to minimum (1.9, AVDD + 0.3)	V
	RESET, SCLK, SDATA, SEN, SNRB, TRIG_EN, PDN	-0.3 to +3.9	V
	Operating free-air, T _A	-40 to +85	°C
Temperature	Operating junction, T _J	+150	°C
	Storage, T _{stg}	-65 to +150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	2	kV

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP and CLKM is less than | 0.3 V |). This recommendation prevents the ESD protection diodes at the clock input pins from turning on.

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THERMAL INFORMATION

		ADS58H43	
	THERMAL METRIC ⁽¹⁾	ZCR (BGA)	UNITS
		144 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	35.9	
θ_{JCtop}	Junction-to-case (top) thermal resistance	5.1	
θ_{JB}	Junction-to-board thermal resistance	12.6	°C/W
ΨЈТ	Junction-to-top characterization parameter	0.1	C/VV
ΨЈВ	Junction-to-board characterization parameter	12.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD33			3.15	3.3	3.45	V
AVDD	Supply voltage		1.8	1.9	2.0	V
DRVDD			1.7	1.8	2.0	V
ANALOG II	NPUTS					
	Differential input voltage range			2		V_{PP}
	Input common-mode voltage		V _{CI}	_M ± 0.025		V
	Analog input common-mode current	(per input pin of each channel)		1.5		μA/MSPS
	VCM current capability			5		mA
	Mariana and a signal formation	2-V _{PP} input amplitude ⁽¹⁾		400		MHz
	Maximum analog input frequency	1.4-V _{PP} input amplitude		500		MHz
CLOCK IN	PUTS					
	Input clock sample rate		184 ⁽²⁾		250	MSPS
		Sine wave, ac-coupled	0.2	1.5		V_{PP}
	Input clock amplitude differential	LVPECL, ac-coupled		1.6		V_{PP}
	$(V_{CLKP} - V_{CLKM})$	LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		1.8		V_{PP}
	Input clock duty cycle		40%	50%	60%	
DIGITAL O	UTPUTS					
C _{LOAD}	Maximum external load capacitance (default strength)	from each output pin to DRVSS		3.3		pF
R _{LOAD}	Differential load resistance between	the LVDS output pairs (LVDS mode)		100		Ω
TEMPERAT	TURE RANGE					
T _A	Operating free-air temperature		-40		+85	°C
_	Operating innation towns are true	Recommended			+105	°C
T_J	Operating junction temperature	Maximum rated ⁽³⁾			+125	°C

See the *Theory of Operation* section.

The minimum functional clock speed can be 10 MSPS after writing the following special modes: address 4Ah, value 01h; address 62h, value 01h; address 92h, value 01h; and address 7Ah, value 01h. See the SPEČIAL MODE[17:14] bits in Table 4 of the Serial Interface

⁽³⁾ Prolonged use at this junction temperature may increase the device failure-in-time (FIT) rate.





Table 1. High-Performance Modes Summary (1)(2)

			f _S = 245.	76 MSPS		f _S = 184.32 MSPS		
ADDRESS (Hex)	DATA (Hex)	R _S = 50 ZONE = 2	R _S = 100 ZONE = 2	R _S = 50 ZONE = 3	R _S = 100 ZONE = 3	R _S = 50 ZONE = 2	R _S = 100 ZONE = 2	
D4	80				√			
D5	80				√			
D6	80	√	√	√	√	√		
D7	0C	√	√	√		√	√	
DB	30				√			
F0	38					√	√	
F1	20	√		√		√		
F5	42				√			

R_S refers to the source impedance. Zone refers to the Nyquist zone in which the signal band lies. Zone = 2 corresponds to the signal band that lies between f_S / 2 and f_S . Zone = 3 corresponds to the signal band that lies between f_S and 3 × f_S / 2. Best performance can be achieved by writing these modes depending upon source impedance, band of operation, and sampling speed.

ELECTRICAL CHARACTERISTICS

Typical values are at $T_A = +25$ °C, full temperature range is $T_{MIN} = -40$ °C to $T_{MAX} = +85$ °C, ADC clock frequency = 250 MHz, 50% clock duty cycle, AVDD33V = 3.3 V, AVDD = 1.9 V, DRVDD = 1.8 V, and -1-dBFS differential input, unless otherwise noted.

	PARAME	TER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RESOLUT	TION		•				
	Default resolution				11		Bits
ANALOG	INPUTS						
	Differential input full-sc	ale			2		V_{PP}
VCM	Common mode input v	oltage			1.15		V
R _{IN}	Input resistance, differe	ential	At 170-MHz input frequency		700		Ω
C _{IN}	Input capacitance, diffe	rential	At 170-MHz input frequency		3.3		pF
	Analog input bandwidth	n, 3 dB	With a $50-\Omega$ source driving the ADC analog inputs		500		MHz
DYNAMIC	ACCURACY						
Eo	Offset error		Specified across devices and channels	-15		15	mV
E _G	Gain error ⁽¹⁾	As a result of internal reference inaccuracy alone	Specified across devices and channels	– 5		5	%FS
		Of channel alone	Specified across channels within a device		±0.2		%FS
	Channel gain error tem	perature coefficient ⁽¹⁾			0.001		Δ%/°C
POWER S	SUPPLY ⁽²⁾					•	
I _{AVDD33}		3.3-V analog supply			51		mA
I _{AVDD}		1.9-V analog supply			350		mA
	Supply current		11-bit operation		340		mA
I_{DRVDD}		1.8-V digital supply	SNRBoost ^{3G+} enabled (90 MHz)		400		mA
			14-bit burst mode		355		mA
			11-bit operation		1.45	1.6	W
P_{TOTAL}		Total	SNRBoost ^{3G+} enabled		1.55	1.8	W
	Power dissipation		14-bit burst mode		1.47		W
P _{DISS(standb}	oy)	Standby			400		mW
P _{DISS(global)}		Global power-down			6	52	mW

There are two sources of gain error: internal reference inaccuracy and channel gain error.

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A 185-MHz, full-scale, sine-wave input signal is applied to all four channels.



ELECTRICAL CHARACTERISTICS (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC clock frequency = 250 MHz, 50% clock duty cycle, AVDD33V = 3.3 V, AVDD = 1.9 V, DRVDD = 1.8 V, and -1-dBFS differential input, unless otherwise noted.

	PARAMET	ER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC	AC CHARACTERISTICS(3)	(4)					
			f _{IN} = 140 MHz, A _{IN} = -1 dBFS		71		dBFS
		11-bit SNRBoost ^{3G+} , 90-MHz BW	f _{IN} = 170 MHz, A _{IN} = -1 dBFS	67	70.5		dBFS
SNR	Signal-to-noise ratio	30-IVII IZ DVV	f _{IN} = 220 MHz, A _{IN} = -1 dBFS		70		dBFS
		11-bit SNRBoost ^{3G+} ,	$f_{IN} = 307 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		71.7		dBFS
		60-MHz BW	$f_{IN} = 350 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		71.5		dBFS
			$f_{IN} = 140 \text{ MHz}, A_{IN} = -1 \text{ dBFS}$		70.6		dBFS
		11-bit SNRBoost ^{3G+} , 90-MHz BW	$f_{IN} = 170 \text{ MHz}, A_{IN} = -1 \text{ dBFS}$	66	70.1		dBFS
SINAD	Signal-to-noise and distortion ratio	SO WITE DVV	$f_{IN} = 220 \text{ MHz}, A_{IN} = -1 \text{ dBFS}$		69.5		dBFS
	alotoritori ratio	11-bit SNRBoost ^{3G+} ,	$f_{IN} = 307 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		69.7		dBFS
		60-MHz BW	$f_{IN} = 350 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		69.2		dBFS
			f _{IN} = 140 MHz, A _{IN} = -1 dBFS		85		dBc
			f _{IN} = 170 MHz, A _{IN} = -1 dBFS	76	85		dBc
SFDR	Spurious-free dynamic ra	ange	f _{IN} = 220 MHz, A _{IN} = -1 dBFS		82		dBc
			$f_{IN} = 307 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		78		dBc
			$f_{IN} = 350 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		77		dBc
			f _{IN} = 140 MHz, A _{IN} = -1 dBFS		82		dBc
			f _{IN} = 170 MHz, A _{IN} = -1 dBFS	73	82		dBc
THD	Total harmonic distortion	١	f _{IN} = 220 MHz, A _{IN} = -1 dBFS		80		dBc
			$f_{IN} = 307 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		77		dBc
			$f_{IN} = 350 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		76		dBc
			f _{IN} = 140 MHz, A _{IN} = -1 dBFS		86		dBc
			f _{IN} = 170 MHz, A _{IN} = -1 dBFS	76	85		dBc
HD2	Second-order harmonic	distortion (5)	$f_{IN} = 220 \text{ MHz}, A_{IN} = -1 \text{ dBFS}$		82		dBc
			$f_{IN} = 307 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		78		dBc
			$f_{IN} = 350 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		77		dBc
			f _{IN} = 140 MHz, A _{IN} = -1 dBFS		85		dBc
			f _{IN} = 170 MHz, A _{IN} = -1 dBFS	76	85		dBc
HD3	Third-order harmonic dis	tortion	$f_{IN} = 220 \text{ MHz}, A_{IN} = -1 \text{ dBFS}$		85		dBc
			$f_{IN} = 307 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		85		dBc
			$f_{IN} = 350 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		83		dBc
			f _{IN} = 140 MHz, A _{IN} = -1 dBFS		95		dBc
			$f_{IN} = 170 \text{ MHz}, A_{IN} = -1 \text{ dBFS}$	87	95		dBc
	Worst spur (non HD2, HD3)		$f_{IN} = 220 \text{ MHz}, A_{IN} = -1 \text{ dBFS}$		95		dBc
	(110111102, 1103)		$f_{IN} = 307 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		95		dBc
			$f_{IN} = 350 \text{ MHz}, A_{IN} = -3 \text{ dBFS}$		95		dBc
DNL	Differential nonlinearity			-0.95	±0.5	1.6	LSBs
INL	Integral nonlinearity				±1.5	±5.25	LSBs
	Input overload recovery		Recovery to within 1% (of final value) for 6-dB output overload with sine-wave input		1		Clock cycle
	Crosstalk		With a full-scale, 220-MHz signal on aggressor channel and no signal on victim channel		90		dB
PSRR	AC power-supply rejection	on ratio	For 50-mV _{PP} signal on AVDD supply		< 30		dB

⁽³⁾ Phase and amplitude imbalances onboard must be minimized to obtain good performance.

⁽⁴⁾ Dynamic ac characteristics are taken with respect to the 14-bit burst mode, unless otherwise noted.

⁵⁾ The minimum value across temperature is ensured by bench characterization.

DIGITAL CHARACTERISTICS

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. AVDD33 = 3.3 V, AVDD = 1.9 V, and DRVDD = 1.8 V, unless otherwise noted.

	PARAM	METER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITA	L INPUTS ⁽¹⁾ (RESET,	SCLK, SDATA, SEN, PDN	, SNRB, TRIG_EN)				
V _{IH}	High-level input vo	ltage	All digital inputs support 1.8-V logic levels. SPI supports 3.3-V logic levels.	1.25			V
V _{IL}	Low-level input vol	ltage	All digital inputs support 1.8-V logic levels. SPI supports 3.3-V logic levels.			0.45	V
High-level input		RESET, SCLK, PDN, SNRB, TRIG_EN pins	V _{HIGH} = 1.8 V		10		μΑ
	current	SEN ⁽²⁾ pin	V _{HIGH} = 1.8 V		0		μΑ
Low-level input		RESET, SCLK, PDN, SNRB, TRIG_EN pins	V _{LOW} = 0 V		0		μΑ
	current	SEN pin	V _{LOW} = 0 V		10		μΑ
DIGITA	L OUTPUTS (SDOUT	, HIRES, TRIG_RDY)					
V _{OH}	High-level output v	voltage		DRVDD - 0.1	DRVDD		V
V _{OL}	Low-level output v	oltage			0	0.1	V
	L OUTPUTS, LVDS II 3:0]P, DAB[13:0]M, D		LKOUTABP, CLKOUTABM, CLKOUTCDP,	CLKOUTCDM)			
V _{ODH}	Output differential	High ⁽³⁾	Standard-swing LVDS	270	350	465	mV
V _{ODL}	voltage	Low	Standard-swing LVDS	-465	-350	-270	mV
V _{OCM}	Output common-m	ode voltage			1.05		V

RESET, SDATA, SCLK, TRIG_EN, and SNRB have an internal 150-k Ω pull-down resistor.

SEN has an internal 150-k Ω pull-up resistor to DRVDD. With an external 100- Ω termination. (2)

TIMING REQUIREMENTS(1)

Typical values are at +25°C, AVDD33 = 3.3 V, AVDD = 1.9 V, DRVDD = 1.8 V, sine-wave input clock, C_{LOAD} = 3.3 pF⁽²⁾, and $R_{LOAD} = 100 \ \Omega^{(3)}$, unless otherwise noted.

Minimum and maximum values are across the full temperature range of $T_{MIN} = -40$ °C to $T_{MAX} = +85$ °C.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _A	Aperture delay		0.7	1.2	1.6	ns
	Aperture delay matching	Between any two channels of the same device		±70		ps
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±150		ps
tJ	Aperture jitter			140		fs rms
	Make up time	Time to valid data after coming out of global power down		100		μs
	Wake up time	Time to valid data after coming out of channel power down	10			μs
		Default latency in 11-bit mode		10		Output clock cycles
		Digital gain enabled		13		Output clock cycles
		Digital gain and offset correction enabled 14				Output clock cycles
ADC I	ADC latency ⁽⁴⁾⁽⁵⁾	SNRBoost ^{3G+} (90-MHz BW) enabled alone		13		Output clock cycles
		SNRBoost ^{3G+} (90-MHz BW), digital gain, and offset correction enabled		17		Output clock cycles
		SNRBoost ^{3G+} (45-MHz BW) enabled alone		15		Output clock cycles
		SNRBoost ^{3G+} (45-MHz BW), digital gain, and offset correction enabled	19			Output clock cycles
OUTPUT	TIMING ⁽⁶⁾					
t _{SU}	Data setup time ⁽⁷⁾⁽⁸⁾⁽⁹⁾	Data valid to CLKOUTxxP zero-crossing	0.6	0.85		ns
t _H	Data hold time ⁽⁷⁾⁽⁸⁾⁽⁹⁾	CLKOUTxxP zero-crossing to data becoming invalid	0.6	0.84		ns
	LVDS bit clock duty cycle	Differential clock duty cycle (CLKOUTxxP – CLKOUTxxM)		50%		
t _{PDI}	Clock propagation delay ⁽⁵⁾	Input clock falling edge cross-over to output clock falling edge cross-over, 184 MSPS ≤ sampling frequency ≤ 250 MSPS	$0.25 \times t_S + t_{delay}$		ns	
t _{delay}	Delay time	Input clock falling edge cross-over to output clock falling edge cross-over, 184 MSPS ≤ sampling frequency ≤ 250 MSPS	6.9	8.65	10.5	ns
t _{RISE} , t _{FALL}	Data rise and fall time	Rise time measured from –100 mV to +100 mV	0.1			ns
t _{CLKRISE} , t _{CLKFALL}	Output clock rise and fall time	Rise time measured from -100 mV to +100 mV	0.1			ns

- Timing parameters are ensured by design and characterization and are not tested in production.
- C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
- R_{LOAD} is the differential load resistance between the LVDS output pair.

 ADC latency is given for channels B and D. For channels A and C, latency reduces by half of the output clock cycles.
- Overall latency = ADC latency + t_{PDI}.

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- Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
- Data valid refers to a logic high of +100 mV and a logic low of -100 mV.
- Note that these numbers are taken with delayed output clocks by writing the following registers: address A9h, value 02h; and address ACh, value 60h. Refer to the Serial Interface Registers section. By default after reset, minimum setup time and minimum hold times are 520 ps each.
- The setup and hold times of a channel are measured with respect to the same channel output clock.

Table 2. LVDS Timings Across Lower Sampling Frequencies

SAMPLING FREQUENCY	SET	UP TIME (ns)		HOLD TIME (ns)		
(MSPS)	MIN	TYP	MAX	MIN	TYP	MAX
210	0.89	1.03		0.82	1.01	
185	1.06	1.21		0.95	1.15	

Product Folder Links: ADS58H43



PARAMETRIC MEASUREMENT INFORMATION

LVDS OUTPUT TIMING

Figure 1 shows a timing diagram of the LVDS output voltage levels. Figure 2 shows the latency described in the Timing Requirements table.

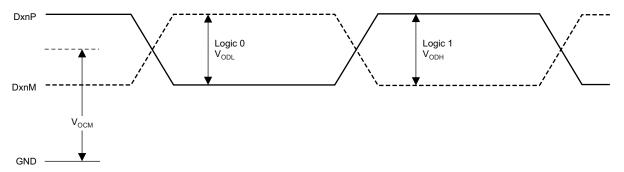


Figure 1. LVDS Output Voltage Levels

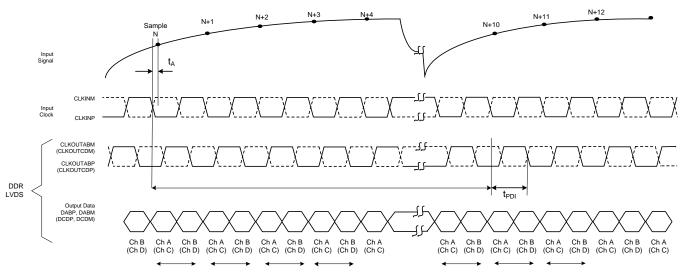


Figure 2. Latency Timing

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PARAMETRIC MEASUREMENT INFORMATION (continued)

All 14 data bits of one channel (11 data bits in default SNRBoost^{3G+} mode) are included in the digital output interface at the same time, as shown in Figure 3. Channel A and C data are output on the rising edge of the output clock while channels B and D are output on the falling edge of the output clock.

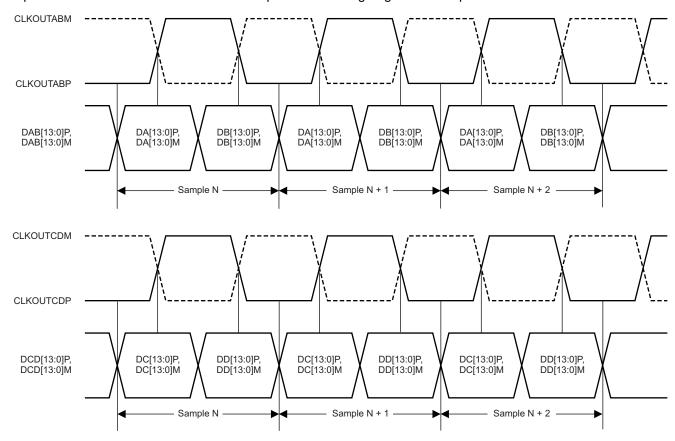


Figure 3. LVDS Output Interface Timing



PIN CONFIGURATION

ZCR PACKAGE BGA-144 (TOP VIEW)

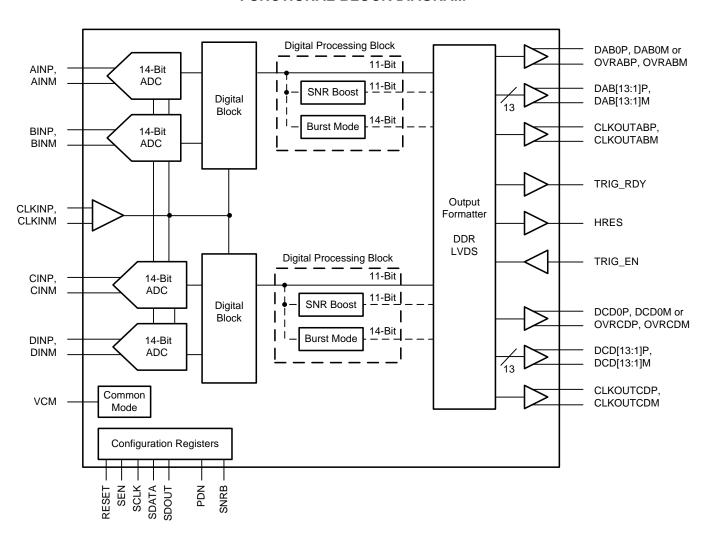
	1	2	3	4	5	6	7	8	9	10	11	12
Α	AVDD	AVDD	CINM	CINP	AVDD	VCM	VCM	AVDD	BINM	BINP	AVDD	AVDD
В	DINP	AVSS	AVDD	AVDD	AVSS	AVDD33	AVDD33	AVSS	AVDD	AVDD	AVSS	AINM
С	DINM	AVSS	AVSS	AVSS	AVSS	CLKINM	CLKINP	AVSS	AVSS	AVSS	AVSS	AINP
D	AVDD	AVDD	VCM	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	VCM	AVDD	AVDD
E	AVDD33	AVDD33	SNRB	DRVSS	DRVSS	DRVSS	DRVSS	DRVSS	DRVSS	PDN	AVDD33	AVDD33
F	DCD13M	DCD13P	DRVDD	DRVSS	DRVSS	DRVSS	DRVSS	DRVSS	DRVSS	DRVDD	DAB13P	DAB13M
G	DCD12M	DCD12P	TRIG_EN	TRIG_RDY	HIRES	RESET	SCLK	SDATA	SEN	SDOUT	DAB12P	DAB12M
н	DCD11M	DCD11P	DCD6P	DCD6M	DRVDD	DRVDD	DRVDD	DRVDD	DAB6M	DAB6P	DAB11P	DAB11M
J	DCD10M	DCD10P	DCD5P	DCD5M	DCD2P	DRVDD	DRVDD	DAB2M	DAB5M	DAB5P	DAB10P	DAB10M
к	DCD9M	DCD9P	DCD4P	DCD4M	DCD2M	DRVDD	DRVDD	DAB2P	DAB4M	DAB4P	DAB9P	DAB9M
L	DCD8M	DCD8P	DCD3P	DCD3M	DCD1P	DCD1M	DAB1M	DAB1P	DAB3M	DAB3P	DAB8P	DAB8M
М	DCD7M	DCD7P	CLKOUT CDP	CLKOUT CDM	DCD0P/ OVRCDP	DCD0M/ OVRCDM	DAB0M/ OVRABM	DAB0P/ OVRABP	CLKOUT ABM	CLKOUT ABP	DAB7P	DAB7M

PIN FUNCTIONS

	PIN				
NAME	NUMBER	1/0	DESCRIPTION		
AINM	B12	I	Negative differential analog input for channel A		
AINP	C12	I	Positive differential analog input for channel A		
AVDD33	B6, B7, E1, E2, E11, E12	1	Analog 3.3-V power supply		
AVDD	A1, A2, A5, A8, A11, A12, B3, B4, B9, B10, D1, D2, D11, D12	I	Analog 1.9-V power supply		
AVSS	B2, B5, B8, B11, C2-C5, C8-C11, D4-D9	I	Analog ground		
BINM	A9	I	Negative differential analog input for channel B		
BINP	A10	ı	Positive differential analog input for channel B		
CINM	A3	I	Negative differential analog input for channel C		
CINP	A4	1	Positive differential analog input for channel C		
CLKINM	C6	I	Negative differential clock input		
CLKINP	C7	1	Positive differential clock input		
CLKOUTABM	M9	0	Negative differential LVDS clock output for channel A and B		
CLKOUTABP	M10	0	Positive differential LVDS clock output for channel A and B		
CLKOUTCDM	M4	0	Negative differential LVDS clock output for channels C and D		
CLKOUTCDP	M3	0	Positive differential LVDS clock output for channels C and D		
DAB[13:1]P, DAB0P/OVRABP, DAB[13:1]M, DAB0M/OVRABM	F11, F12, G11, G12, H9-H12, J8-J12, K8-K12, L7-L12, M7, M8, M11, M12	0	DDR LVDS outputs for channels A and B. In 11-bit mode, DAB13 is the MSB, DAB3 is the LSB, and DAB0 is the over-range (OVR) bit. In 14-bit burst mode, DAB13 is the MSB and DAB0 is the LSB. LSB can be programmed as OVR bit in this mode.		
DCD[13:1]P, DCD0P/OVRCDP, DCD[13:1]M, DCD0M/OVRCDM	F1, F2, G1, G2, H1-H4, J1-J5, K1-K5, L1-L6, M1, M2, M5, M6	0	DDR LVDS outputs for channels C and D. In 11-bit mode, DCD13 is the MSB, DCD3 is the LSB, and DCD0 is the OVR bit. In 14-bit burst mode, DCD13 is the MSB and DCD0 is the LSB. LSB can be programmed as OVR bit in this mode.		
DINM	C1	1	Negative differential analog input for channel D		
DINP	B1	1	Positive differential analog input for channel D		
DRVDD	F3, F10, H5-H8, J6, J7, K6, K7	I	Digital 1.8-V power supply		
DRVSS	E4-E9, F4-F9	I	Digital ground		
HIRES	G5	0	Indication in burst mode if output data is high or low resolution		
PDN	E10	I	Power-down control; active high. Logic high is power down.		
RESET	G6	1	Hardware reset; active high		
SCLK	G7	I	Serial interface clock input		
SDATA	G8	1	Serial interface data input		
SDOUT	G10	0	Serial interface data output		
SEN	G9	1	Serial interface enable		
SNRB	E3	1	SNRB enable; active high		
TRIG_EN	G3	1	I Trigger burst mode; active high		
TRIG_RDY	G4	0	Indication if ADC is ready for another high-resolution burst mode		
VCM	A6, A7, D3, D10	0	Common-mode voltage for analog inputs. All VCM pins are internally connected together.		



FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

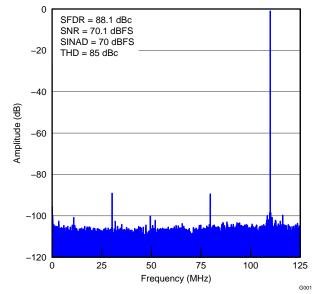


Figure 4. FFT IN 14-BIT MODE INPUT FREQUENCY (140 MHz)

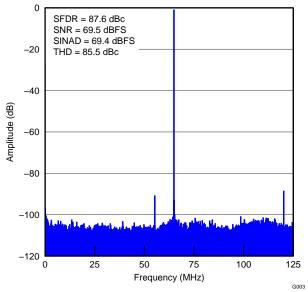


Figure 6. FFT IN 14-BIT MODE INPUT FREQUENCY (185 MHz)

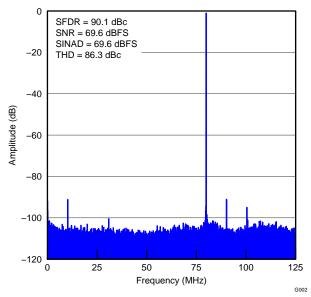


Figure 5. FFT IN 14-BIT MODE INPUT FREQUENCY (170 MHz)

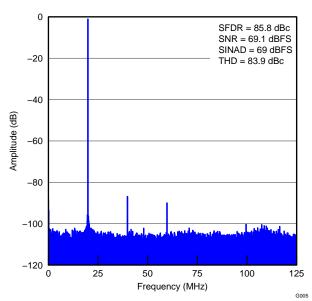


Figure 7. FFT IN 14-BIT MODE INPUT FREQUENCY (190 MHz)

TYPICAL CHARACTERISTICS (continued)

At $+25^{\circ}$ C, AVDD = 1.9 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, rated sampling frequency, 0-dB gain, 14-bit burst mode, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

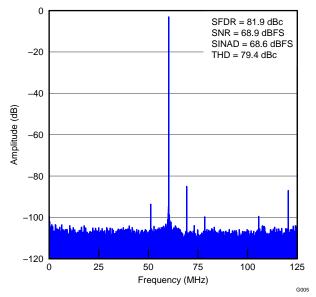


Figure 8. FFT IN 14-BIT MODE INPUT FREQUENCY (230 MHz)

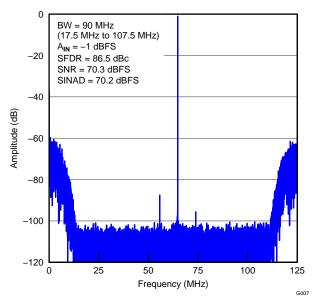
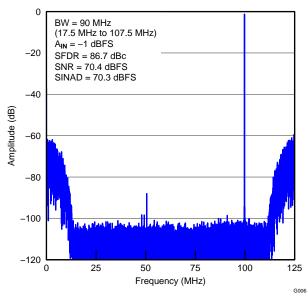


Figure 10. FFT IN 11-BIT MODE WITH SNRBoost^{3G+} INPUT FREQUENCY (185 MHz, 90-MHz Bandwidth)



NSTRUMENTS

Figure 9. FFT IN 11-BIT MODE WITH SNRBoost^{3G+} INPUT FREQUENCY (150 MHz, 90-MHz Bandwidth)

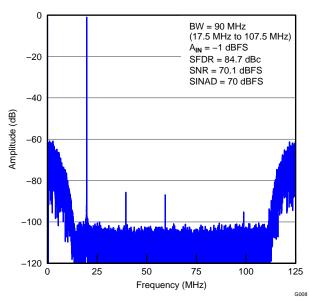


Figure 11. FFT IN 11-BIT MODE WITH SNRBoost^{3G+} INPUT FREQUENCY (230 MHz, 90-MHz Bandwidth)

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TYPICAL CHARACTERISTICS (continued)

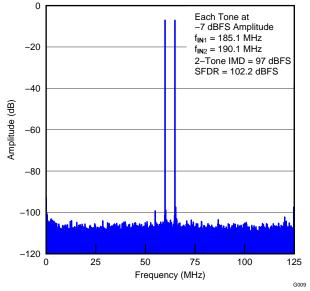


Figure 12. FFT FOR -7-dBFS, TWO-TONE INPUT SIGNAL IN 14-BIT MODE

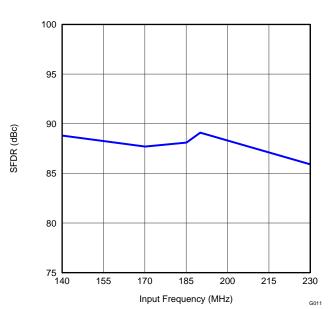


Figure 14. SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY

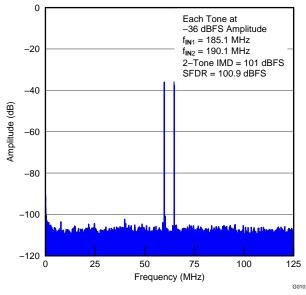


Figure 13. FFT FOR -36-dBFS, TWO-TONE INPUT SIGNAL IN 14-BIT MODE

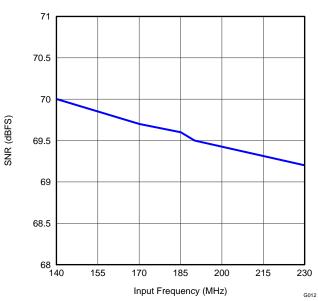


Figure 15. SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

TYPICAL CHARACTERISTICS (continued)

At $+25^{\circ}$ C, AVDD = 1.9 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, rated sampling frequency, 0-dB gain, 14-bit burst mode, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

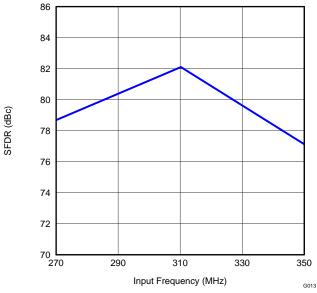


Figure 16. SPURIOUS-FREE DYNAMIC RANGE vs HIGH INPUT FREQUENCY (-3 dBFS)

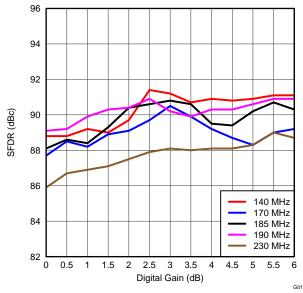
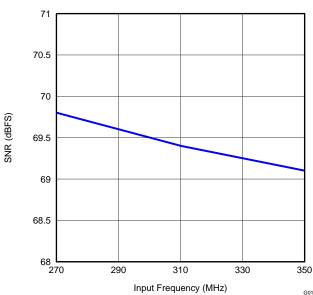


Figure 18. SPURIOUS-FREE DYNAMIC RANGE vs GAIN ACROSS INPUT FREQUENCY



STRUMENTS

Figure 17. SIGNAL-TO-NOISE RATIO vs HIGH INPUT FREQUENCY (-3 dBFS)

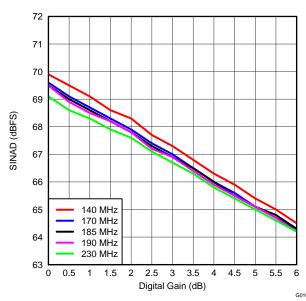
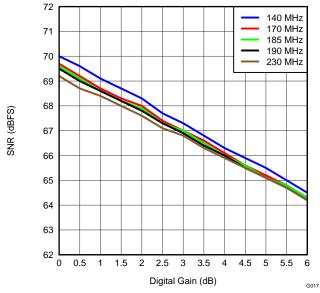


Figure 19. SIGNAL-TO-NOISE RATIO AND DISTORTION vs GAIN ACROSS INPUT FREQUENCY

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TYPICAL CHARACTERISTICS (continued)



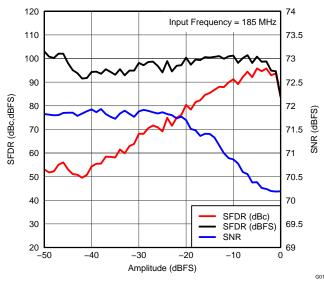
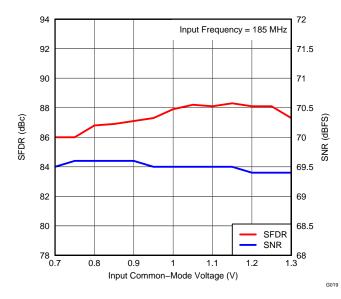


Figure 20. SIGNAL-TO-NOISE RATIO vs GAIN ACROSS INPUT FREQUENCY

Figure 21. PERFORMANCE vs INPUT AMPLITUDE



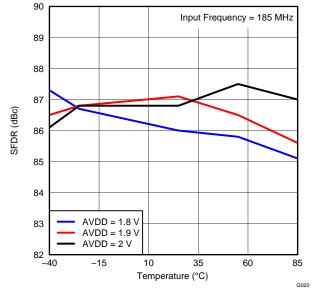


Figure 22. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

Figure 23. SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE (AVDD Supply)

ISTRUMENTS

TYPICAL CHARACTERISTICS (continued)

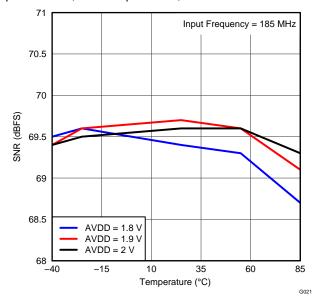


Figure 24. SIGNAL-TO-NOISE RATIO vs TEMPERATURE (AVDD Supply)

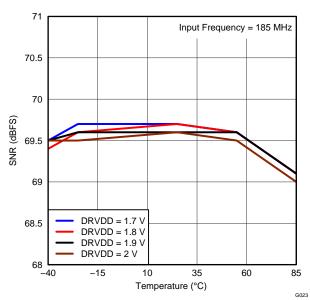


Figure 26. SIGNAL-TO-NOISE RATIO vs TEMPERATURE (DRVDD Supply)

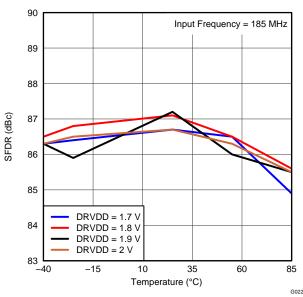


Figure 25. SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE (DRVDD Supply)

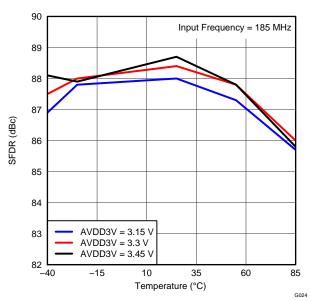


Figure 27. SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE (AVDD3V Supply)

TYPICAL CHARACTERISTICS (continued)

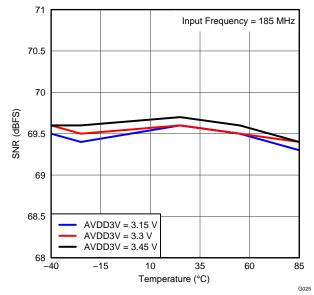


Figure 28. SIGNAL-TO-NOISE RATIO vs TEMPERATURE (AVDD3V Supply)

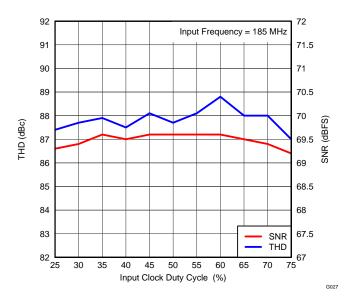


Figure 30. PERFORMANCE vs INPUT CLOCK DUTY CYCLE

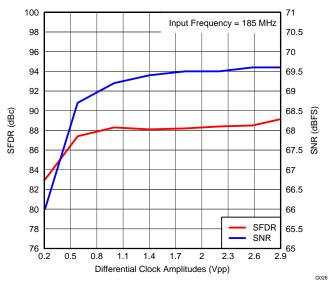


Figure 29. PERFORMANCE vs DIFFERENTIAL CLOCK AMPLITUDE

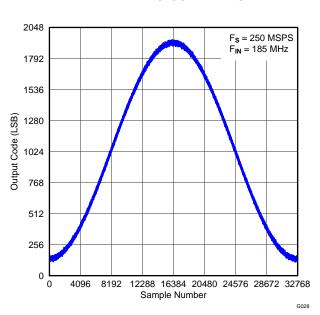


Figure 31. TIME DOMAIN DATA WITH SNRBoost^{3G+} ENABLED



TYPICAL CHARACTERISTICS (continued)

At $+25^{\circ}$ C, AVDD = 1.9 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, rated sampling frequency, 0-dB gain, 14-bit burst mode, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

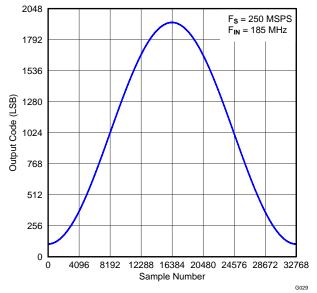


Figure 32. TIME DOMAIN DATA WITH SNRBoost^{3G+} DISABLED (Default is 11-Bit Mode)

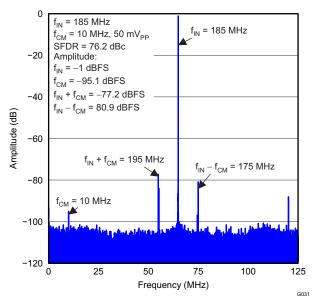


Figure 34. COMMON-MODE REJECTION RATIO SPECTRUM

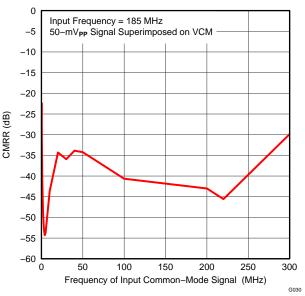


Figure 33. COMMON-MODE REJECTION RATIO vs FREQUENCY

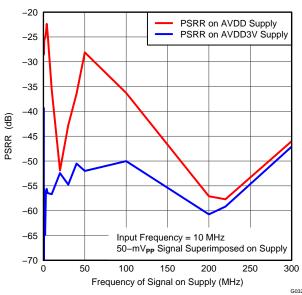


Figure 35. POWER-SUPPLY REJECTION RATIO vs FREQUENCY

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TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, rated sampling frequency, 0-dB gain, 14-bit burst mode, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

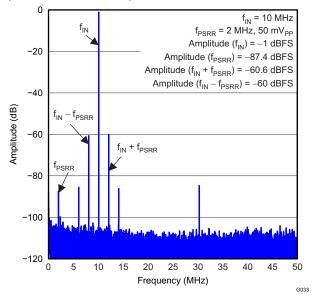


Figure 36. ZOOMED VIEW OF POWER-SUPPLY REJECTION RATIO SPECTRUM

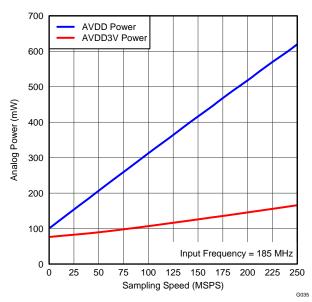


Figure 38. ANALOG POWER vs SAMPLING RATE

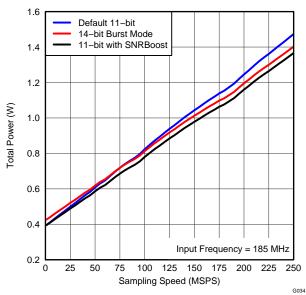


Figure 37. TOTAL POWER vs SAMPLING RATE

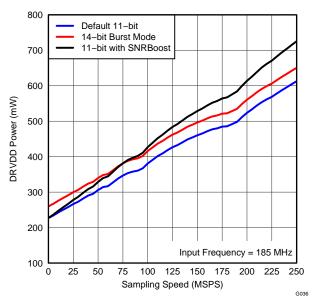


Figure 39. DRVDD POWER vs SAMPLING RATE IN **VARIOUS DIGITAL MODES**

Product Folder Links: ADS58H43



DEVICE CONFIGURATION

The ADS58H43 can be configured with a serial programming interface (SPI), as described in the Serial Interface section. In addition, the device has control pins that control power-down and SNRBoost^{3G+} operation.

SERIAL INTERFACE

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface input data), and SDOUT (serial interface read back data) pins. The serial shift of bits into the device is enabled when SEN is low. Serial data (SDATA) are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

- 1. Either through a hardware reset by applying a high pulse on the RESET pin (of widths greater than 10 ns), as shown in Figure 40; or
- 2. By applying a software reset. When using the serial interface, set the RESET bit (D1 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

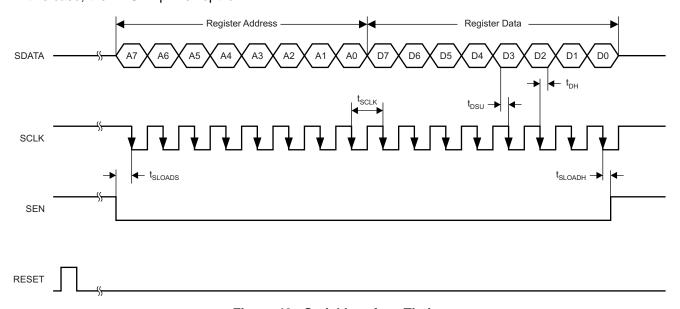


Figure 40. Serial Interface Timing

Table 3. Timing Characteristics for Figure 40

	PARAMETER	MIN	TYP	MAX	UNIT
f _{SCLK}	SCLK frequency (equal to 1 / t _{SCLK})	> dc		20	MHz
t _{SLOADS}	SEN to SCLK setup time	25			ns
t _{SLOADH}	SCLK to SEN hold time	25			ns
t _{DSU}	SDI setup time	25			ns
t _{DH}	SDI hold time	25			ns

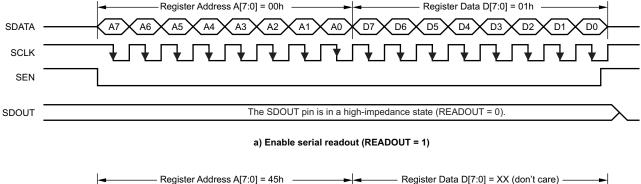
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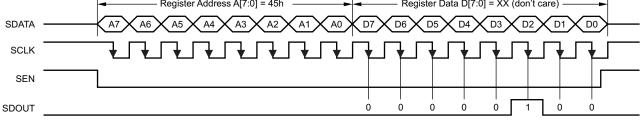
Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back, as shown in Figure 41. This read-back mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and ADC.

- 1. Set the READOUT register bit to '1'. This setting disables any further writes to the registers except register address 00h.
- 2. Initiate a serial interface cycle specifying the address of the register (A[7:0]) whose content must be read.
- 3. The device outputs the contents (D[7:0]) of the selected register on the SDOUT pin (pin G10).
- 4. The external controller can latch the contents at the SCLK falling edge.
- 5. To enable register writes, reset the READOUT register bit to '0'.

Note that the contents of register 00h cannot be read back because the register contains RESET and READOUT bits. When the READOUT bit is disabled, the SDOUT pin is in a high-impedance state. If serial readout is not used, the SDOUT pin must not be connected (must float).





The SDOUT pin functions as a serial readout (READOUT = 1).

b) Read contents of Register 45h. This register is initialized with 04h.

Figure 41. Serial Readout Timing Diagram

SDOUT comes out at the SCLK rising edge with an approximate delay (t_{SD DELAY}) of 8 ns, as shown in Figure 42.

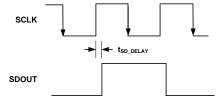


Figure 42. SDOUT Delay Timing





SERIAL INTERFACE REGISTERS

Table 4 summarizes the ADS58H43 registers.

Table 4. Register Map

REGISTER				REGIS	TER DATA			
ADDRESS A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	RESET	READOUT
01		<u> </u>		SWING			0	0
25		DIGITAL O	GAIN CH B		DIGITAL GAIN BYPASS CH B	1	TEST PATTERN CH	В
2B		DIGITAL O	GAIN CH A		DIGITAL GAIN BYPASS CH A	1	TEST PATTERN CH	Α
31		DIGITAL G	GAIN CH D		DIGITAL GAIN BYPASS CH D	1	EST PATTERN CH	D
37		DIGITAL G	SAIN CH C		DIGITAL GAIN BYPASS CH C	7	EST PATTERN CH	С
3D	0	0	SEL OFFSET CORR	0	0	0	0	0
3F	0	0				ATTERN[13:8]		
40			1	CUSTOM	PATTERN[7:0]			
41	0	0	0		HIGH RESOLUTION	ON SAMPLES, NH		AUTO BURST ENABLE
42	0	0	0	0	DIGITAL ENABLE	SNRB 45/95MHz	LOW RESOLUT	ION SAMPLES, NL
44	BMODE EN CH CD	BMODE EN CH AB	0	0	0	BMODE OVR ENABLE	0	DIS SNRB
45	0	0	0	0	SEL OVR	GLOBAL POWER DOWN	0	CONFIG PDN PIN
4A	0	0	0	0	0	0	0	SPECIAL MODE 14
62	0	0	0	0	0	0	0	SPECIAL MODE 15
7A	0	0	0	0	0	0	0	SPECIAL MODE 17
92	0	0	0	0	0	0	0	SPECIAL MODE 16
A9	0	0	0	0		CLOCKOUT DEL	AY PROG CH AB	-
AC	0		CLOCKOUT DEL	AY PROG CH CD		0	0	0
C3			Г	FAST OVR	THRESH PROG		Г	1
C4	EN FAST OVR THRESH	0	0	0	0	0	0	0
CF	0	0	0	0	SPECIAL MODE 0	0	0	0
D4	SPECIAL MODE 1	0	0	0	0	0	0	0
D5	SPECIAL MODE 2	0	0	0	0	0	0	0
D6	SPECIAL MODE 3	0	0	0	0	0	0	0
D7	0	0	0	0	SPECIAL MODE 5	SPECIAL MODE 4	0	0
DB	0	0	SPECIAL MODE 7	SPECIAL MODE 6	0	0	0	0
EA	SNRB PIN OVRD	0	0	0	0	0	0	0
F0	0	0	SPECIAL MODE 10	SPECIAL MODE 9	SPECIAL MODE 8	0	0	0
F1	0	0	SPECIAL MODE 11	0	0	ENA	BLE LVDS SWING	PROG
F5	0	SPECIAL MODE 13	0	0	0	0	SPECIAL MODE 12	0
FE	0	0	0	0	PDN CH D	PDN CH C	PDN CH A	PDN CH B

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DESCRIPTION OF SERIAL REGISTERS

Register Address 00h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	RESET	READOUT

Bits D[7:2] Always write '0'

Bit D1 RESET: Software reset applied

This bit resets all internal registers to the default values and self-clears to '0'.

Bit D0 READOUT: Serial readout

This bit sets the serial readout of the registers.

0 = Serial readout of registers disabled; the SDOUT pin is placed in a high-impedance

state.

1 = Serial readout enabled; the SDOUT pin functions as a serial data readout with

CMOS logic levels running from the DRVDD supply.

Register Address 01h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
		LVDS	SWING			0	0

Bits D[7:2] LVDS SWING: LVDS swing programmability

These bits program the LVDS swing only after the ENABLE LVDS SWING PROG bits

are set to '11'.

 $000000 = Default LVDS swing; \pm 350 mV with an external 100-Ω termination$

011011 = \pm 420-mV LVDS swing with an external 100- Ω termination 110010 = \pm 470-mV LVDS swing with an external 100- Ω termination 010100 = \pm 560-mV LVDS swing with an external 100- Ω termination 001111 = \pm 160-mV LVDS swing with an external 100- Ω termination

Bits D[1:0] Always write '0'



Register Address 25h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
	DIGITAL G	AIN CH B		DIGITAL GAIN BYPASS CH B	TES	ST PATTERN C	НВ

Bits D[7:4] DIGITAL GAIN CH B: Channel B digital gain programmability

These bits set the digital gain programmability from 0 dB to 6 dB in 0.5-dB steps for channel B. Set the DIGITAL ENABLE bit to '1' beforehand to enable this feature.

0000 = 0 - dB gain

0001 = 0.5 - dB gain

0010 = 1 - dB gain

0011 = 1.5 - dB gain

0100 = 2 - dB gain

0101 = 2.5 - dB gain

0110 = 3-dB gain

0111 = 3.5 - dB gain

1000 = 4 - dB gain

1001 = 4.5 - dB gain

1010 = 5 - dB gain

1011 = 5.5 - dB gain

1100 = 6 - dB gain

Bit D3 DIGITAL GAIN BYPASS CH B: Channel B digital gain bypass

0 = Normal operation

1 = Digital gain feature for channel B is bypassed

Bits D[2:0] TEST PATTERN CH B: Channel B test pattern programmability

These bits program the test pattern for channel B.

000 = Normal operation

001 = Outputs all 0s

010 = Outputs all 1s

011 = Outputs toggle pattern

In 11-bit mode, output data (D[10:0]) are an alternating sequence of 10101010101 and 01010101010.

In 14-bit burst mode, output data ([D:0]) are an alternating sequence of 0101010101011 and 101010101010.

100 = Outputs digital ramp

In 11-bit mode, output data increments by one 11-bit LSB every 8th clock cycle from code 0 to code 2047.

In 14-bit burst mode, output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383

101 = Outputs custom pattern

To program a pattern in 11-bit mode, use the CUSTOM PATTERN D[13:3] bits of registers 3Fh and 40h.

To program a pattern in 14-bit mode, use the CUSTOM PATTERN D[13:0] bits of registers 3Fh and 40h.

110 = Unused

111 = Unused

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Register Address 2Bh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
	DIGITAL O	_ GAIN CH A		DIGITAL GAIN BYPASS CH A	TES	I PALIERNI	H A

Bits D[7:4] DIGITAL GAIN CH A: Channel A digital gain programmability

These bits set the digital gain programmability from 0 dB to 6 dB in 0.5-dB steps for channel A. Set the DIGITAL ENABLE bit to '1' beforehand to enable this feature.

0000 = 0 - dB gain

0001 = 0.5 - dB gain

0010 = 1 - dB gain

0011 = 1.5 - dB gain

0100 = 2 - dB gain

0101 = 2.5 - dB gain

0110 = 3-dB gain

0111 = 3.5 - dB gain

1000 = 4 - dB gain

1001 = 4.5 - dB gain

1010 = 5 - dB gain

1011 = 5.5 - dB gain

1100 = 6 - dB gain

Bit D3 DIGITAL GAIN BYPASS CH A: Channel A digital gain bypass

0 = Normal operation

1 = Digital gain feature for channel A is bypassed

Bits D[2:0] TEST PATTERN CH A: Channel A test pattern programmability

These bits program the test pattern for channel A.

000 = Normal operation

001 = Outputs all 0s

010 = Outputs all 1s

011 = Outputs toggle pattern

In 11-bit mode, output data (D[10:0]) are an alternating sequence of 10101010101 and 01010101010.

In 14-bit burst mode, output data ([D:0]) are an alternating sequence of 0101010101011 and 101010101010.

100 = Outputs digital ramp

In 11-bit mode, output data increments by one 11-bit LSB every 8th clock cycle from code 0 to code 2047.

In 14-bit burst mode, output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383

101 = Outputs custom pattern

To program a pattern in 11-bit mode, use the CUSTOM PATTERN D[13:3] bits of registers 3Fh and 40h.

To program a pattern in 14-bit mode, use the CUSTOM PATTERN D[13:0] bits of registers 3Fh and 40h.

110 = Unused

111 = Unused



Register Address 31h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
	DIGITAL G	AIN CH D		DIGITAL GAIN BYPASS CH D	TES	T PATTERN C	H D

Bits D[7:4] DIGITAL GAIN CH D: Channel D digital gain programmability

These bits set the digital gain programmability from 0 dB to 6 dB in 0.5-dB steps for channel D. Set the DIGITAL ENABLE bit to '1' beforehand to enable this feature.

0000 = 0 - dB gain

0001 = 0.5 - dB gain

0010 = 1 - dB gain

0011 = 1.5 - dB gain

0100 = 2-dB gain

0101 = 2.5 - dB gain

0110 = 3-dB gain

0111 = 3.5 - dB gain

1000 = 4-dB gain

1001 = 4.5 - dB gain

1010 = 5 - dB gain

1011 = 5.5 - dB gain

1100 = 6 - dB gain

Bit D3 DIGITAL GAIN BYPASS CH D: Channel D digital gain bypass

0 = Normal operation

1 = Digital gain feature for channel A is bypassed

Bits D[2:0] TEST PATTERN CH D: Channel D test pattern programmability

These bits program the test pattern for channel D.

000 = Normal operation

001 = Outputs all 0s

010 = Outputs all 1s

011 = Outputs toggle pattern

In 11-bit mode, output data (D[10:0]) are an alternating sequence of 10101010101 and 01010101010.

In 14-bit burst mode, output data ([D:0]) are an alternating sequence of 0101010101011 and 101010101010.

100 = Outputs digital ramp

In 11-bit mode, output data increments by one 11-bit LSB every 8th clock cycle from code 0 to code 2047.

In 14-bit burst mode, output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383

101 = Outputs custom pattern

To program a pattern in 11-bit mode, use the CUSTOM PATTERN D[13:3] bits of registers 3Fh and 40h.

To program a pattern in 14-bit mode, use the CUSTOM PATTERN D[13:0] bits of registers 3Fh and 40h.

110 = Unused

111 = Unused

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Register Address 37h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
	DIGITAL G	SAIN CH C		DIGITAL GAIN BYPASS CH C	TES	T PATTERN C	H C

Bits D[7:4] DIGITAL GAIN CH C: Channel C digital gain programmability

These bits set the digital gain programmability from 0 dB to 6 dB in 0.5-dB steps for channel C. Set the DIGITAL ENABLE bit to '1' beforehand to enable this feature.

0000 = 0 - dB gain

0001 = 0.5 - dB gain

0010 = 1 - dB gain

0011 = 1.5 - dB gain

0100 = 2 - dB gain

0101 = 2.5 - dB gain

0110 = 3-dB gain

0111 = 3.5 - dB gain

1000 = 4-dB gain

1001 = 4.5 - dB gain

1010 = 5 - dB gain

1011 = 5.5 - dB gain

1100 = 6 - dB gain

Bit D3 DIGITAL GAIN BYPASS CH C: Channel C digital gain bypass

0 = Normal operation

1 = Digital gain feature for channel A is bypassed

Bits D[2:0] TEST PATTERN CH C: Channel C test pattern programmability

These bits program the test pattern for channel C.

000 = Normal operation

001 = Outputs all 0s

010 = Outputs all 1s

011 = Outputs toggle pattern

In 11-bit mode, output data (D[10:0]) are an alternating sequence of 10101010101 and 01010101010.

In 14-bit burst mode, output data ([D:0]) are an alternating sequence of 0101010101011 and 101010101010.

100 = Outputs digital ramp

In 11-bit mode, output data increments by one 11-bit LSB every 8th clock cycle from code 0 to code 2047.

In 14-bit burst mode, output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383

101 = Outputs custom pattern

To program a pattern in 11-bit mode, use the CUSTOM PATTERN D[13:3] bits of registers 3Fh and 40h.

To program a pattern in 14-bit mode, use the CUSTOM PATTERN D[13:0] bits of registers 3Fh and 40h.

110 = Unused

111 = Unused



Register Address 3Dh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	SEL OFFSET CORR	0	0	0	0	0

Bits D[7:6] Always write '0'

Bit D5 SEL OFFSET CORR: Offset correction setting

This bit enables the offset correction feature for all four channels after the DIGITAL ENABLE bit is set to '1,' correcting mid-code to 1023. In addition, write the SPECIAL MODE 0 bit (register CFh, value 08h) for proper operation of the offset correction feature. Note that the offset correction feature should only be used in the default 11-bit mode.

0 = Offset correction disabled1 = Offset correction enabled

Bits D[4:0] Always write '0'

Register Address 3Fh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	CUSTOM PATTERN D13	CUSTOM PATTERN D12	CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8

Bits D[7:6] Always write '0'

Bits D[5:0] CUSTOM PATTERN D[13:8]

Set the custom pattern using these bits for all four channels.

Register Address 40h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0	
CUSTOM								
PATTERN D7	PATTERN D6	PATTERN D5	PATTERN D4	PATTERN D3	PATTERN D2	PATTERN D1	PATTERN D0	

Bits D[7:0] CUSTOM PATTERN D[7:0]

Set the custom pattern using these bits for all four channels.

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Register Address 41h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	HI		ON SAMPLES. I	NH	AUTO BURST ENABLE

Bits D[7:5] Always write '0'

Bits D[4:1] HIGH RESOLUTION SAMPLES, NH

These bits control the number of high-resolution samples in 14-bit burst mode with

Equation 1:

 $2^{10 + NH}$ (1)

0000: NH = 0

0001: NH = 1

0010: NH = 2

0011: NH = 3

0100: NH = 4

0101: NH = 5

0110: NH = 6 0111: NH = 7

4000 111 - 1

1000: NH = 8

1001: NH = 9

1010: NH = 10

1011: NH = 11

1100: NH = 12

1101: NH = 13 1110: NH = 14

1111: NH = 15

Bit D0 AUTO BURST ENABLE

0 = 14-bit burst mode disabled

1 = 14-bit burst mode auto-enabled



Register Address 42h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	DIGITAL ENABLE	SNRB 45/90MHz	LOW RESOLUTI	ON SAMPLES, NL

Bits D[7:4] Always write '0'
Bit D3 DIGITAL ENABLE

1 = Digital gain and offset correction features disabled1 = Digital gain and offset correction features enabled

Bit D2 SNRB 45/90MHz: SNRBoost^{3G+} enable

0 = SNRBoost^{3G+} enabled with 90-MHz bandwidth (default after reset)

1 = SNRBoost^{3G+} enabled with 45-MHz bandwidth

Bits D[1:0] LOW RESOLUTION SAMPLES, NL

These bits control the number of low-resolution samples in 14-bit burst mode with

Equation 2:

 $2^{13 + NH + NL}$ (2)

00: NL = 0 01: NL = 1 10: NL = 2 11: NL = 3

Register Address 44h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
BMODE EN CH CD	BMODE EN CH AB	0	0	0	BMODE OVR ENABLE	0	DIS SNRB

Bit D7 BMODE EN CH CD

0 = 14-bit burst mode disabled for channels C and D 1 = 14-bit burst mode enabled for channels C and D

Bit D6 BMODE EN CH AB

0 = 14-bit burst mode disabled for channels A and B 1 = 14-bit burst mode enabled for channels A and B

Bits D[5:3] Always write '0'

Bit D2 BMODE OVR ENABLE

This bit can only be used in 14-bit burst mode. 0 = 14-bit data comes out without an OVR

1 = The ADC data out bit (Dxx[0]) becomes OVRxx. See the Overrange Indication

(OVRxx) section for details.

Bit D1 Always write '0'

Bit D0 DIS SNRB: Disable SNRBoost

This bit only functions when SNRB PIN OVRD is set.

0 = Default

 $1 = SNRBoost^{3G+}$ is disabled for all four channels.

Product Folder Links: ADS58H43



Register Address 45h (Default = 00h)

D.	7 D6	D5	D4	D3	D2	D1	D0
0	0	0	0	SEL OVR	GLOBAL POWER DOWN	0	CONFIG PDN PIN

Bits D[7:4] Always write '0'

Bit D3 SEL OVR: OVR selection

0 = Fast OVR selected

1 = Normal OVR selected. See the *Overrange Indication (OVRxx)* section for details.

Bit D2 GLOBAL POWER DOWN

0 = Normal operation

1 = Global power down. All ADC channels, internal references, and output buffers are

powered down. Wakeup time from this mode is slow (100 µs).

Bit D1 Always write '0'
Bit D0 CONFIG PDN PIN

Use this bit to configure PDN pin.

0 = The PDN pin functions as a standby pin. All channels are put in standby. Wake-up

time from standby mode is fast (10 µs).

1 = The PDN pin functions as a global power-down pin. All ADC channels, internal references, and output buffers are powered down. Wake-up time from global power mode is slow (100 μ s).

Register Address 4Ah (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	SPECIAL MODE 14

Bits D[7:1] Always write '0'
Bit D0 SPECIAL MODE 14

Set the SPECIAL MODE[17:14] bits high to reduce the minimum functional clock speed to 10 MSPS. Usage of these bits should be limited to functional checks only because performance degrades when these bits are set high.

Register Address 62h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	SPECIAL MODE 15

Bits D[7:1] Always write '0'
Bit D0 SPECIAL MODE 15

Set the SPECIAL MODE[17:14] bits high to reduce the minimum functional clock speed to 10 MSPS. Usage of these bits should be limited to functional checks only because performance degrades when these bits are set high.



Register Address 7Ah (Default = 00h)

			•	•		•	
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	SPECIAL MODE 17

Bits D[7:1] Always write '0'
Bit D0 SPECIAL MODE 17

Set the SPECIAL MODE[17:14] bits high to reduce the minimum functional clock speed to 10 MSPS. Usage of these bits should be limited to functional checks only because performance degrades when these bits are set high.

Register Address 92h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	SPECIAL MODE 16

Bits D[7:1] Always write '0'
Bit D0 SPECIAL MODE 16

Set the SPECIAL MODE[17:14] bits high to reduce the minimum functional clock speed to 10 MSPS. Usage of these bits should be limited to functional checks only because performance degrades when these bits are set high.

Register Address A9h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0		CLOCKOUT DLL	AY PROG CH AB	

Bits D[7:4] Always write '0'

Bits D[6:3] CLOCKOUT DELAY PROG CH AB

These bits program the clock out delay for channels A and B, see Table 5.

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Register Address ACh (Default = 00h)

		_		•	•		
D7	D6	D5	D4	D3	D2	D1	D0
0		CLOCKOUT DEL	AY PROG CH CD)	0	0	0

Bit D7 Always write '0'

Bits D[7:4] CLOCKOUT DELAY PROG CH CD

These bits program the clock out delay for channels C and D, as shown in Table 5.

Bits D[2:0] Always write '0'

Table 5. Clock Out Delay Programmability for All Channels

CLOCKOUT DELAY PROG CHxx	DELAY (ps)
0000	0
0001	-30
0010	70
0011	30
0100	-150
0101	-180
0110	–70
0111	-110
1000	270
1001	230
1010	340
1011	300
1100	140
1101	110
1110	200
1111	170

Register Address C3h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
			FAST OVR TH	HRESH PROG			

Bits D[7:0] FAST OVR THRESH PROG

The ADS58H43 has a fast OVR mode that indicates an overload condition at the ADC input. The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESH PROG bits.

FAST OVR is triggered seven output clock cycles after the overload condition occurs. To enable the FAST OVR programmability, enable the EN FAST OVR THRESH register bit. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESH PROG bits] / 255).

After reset, when EN FAST OVR THRESH PROG is set, the default value of the FAST OVR THRESH PROG bits is 230 (decimal).



D7	D6	D5	D4	D3	D2	D1	D0	
EN FAST OVR THRESH	0	0	0	0	0	0	0	

Bit D7 EN FAST OVR THRESH

This bit enables the ADS58H43 to be programmed to select the fast OVR threshold.

Bits D[6:0] Always write '0'

Register Address CFh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	SPECIAL MODE 0	0	0	0

Bits D[7:4] Always write '0'
Bit D3 SPECIAL MODE 0

This bit must be set to '1' when the SEL OFFSET CORR bit is selected.

Bits D[2:0] Always write '0'

Register Address D4h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
SPECIAL MODE 1	0	0	0	0	0	0	0

Bit D7 SPECIAL MODE 1

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bits D[6:0] Always write '0'

Register Address D5h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
SPECIAL MODE 2	0	0	0	0	0	0	0

Bit D7 SPECIAL MODE 2

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bits D[6:0] Always write '0'

Register Address D6h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
SPECIAL MODE 3	0	0	0	0	0	0	0

Bit D7 SPECIAL MODE 3

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bits D[6:0] Always write '0'



Register Address D7h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	SPECIAL MODE 5	SPECIAL MODE 4	0	0

Bits D[7:4] Always write '0'
Bit D3 SPECIAL MODE 5

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bit D2 SPECIAL MODE 4

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bits D[1:0] Always write '0'

Register Address DBh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	SPECIAL MODE 7	SPECIAL MODE 6	0	0	0	0]

Bits D[7:6] Always write '0'
Bit D5 SPECIAL MODE 7

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bit D4 SPECIAL MODE 6

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bits D[3:0] Always write '0'

Register Address EAh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
SNRB PIN OVRD	0	0	0	0	0	0	0

Bit D7 SNRB PIN OVRD

 $0 = SNRBoost^{3G+}$ is controlled by the SNRB pin.

1 = SNRBoost^{3G+} is controlled by the DIS SNRB register bit.

Bits D[6:0] Always write '0'



D7	D6	D5	D4	D3	D2	D1	D0
0	0	SPECIAL MODE 10	SPECIAL MODE 9	SPECIAL MODE 8	0	0	0

Bits D[7:6] Always write '0'
Bit D5 SPECIAL MODE 10

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bit D4 SPECIAL MODE 9

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bit D3 SPECIAL MODE 8

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bits D[2:0] Always write '0'

Register Address F1h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	SPECIAL MODE 11	0	0	ENABL	E LVDS SWING	B PROG

Bits D[7:6] Always write '0'
Bit D7 SPECIAL MODE 11

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bits D[4:3] Always write '0'

Bits D[2:0] ENABLE LVDS SWING PROG

This bit enables the LVDS swing control with the LVDS SWING bits.

00 = LVDS swing control disabled

01 = Do not use10 = Do not use

11 = LVDS swing control enabled



Register Address F5h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	SPECIAL MODE 13	0	0	0	0	SPECIAL MODE 12	0

Bit D7 Always write '0'
Bit D6 SPECIAL MODE 13

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bits D[5:2] Always write '0'
Bit D1 SPECIAL MODE 12

Refer to Table 1 for optimal performance in a given frequency band and source

impedance.

Bit D0 Always write '0'

Register Address FEh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PDN CH D	PDN CH C	PDN CH A	PDN CH B

Bits D[7:4] Always write '0'

Bit D3 PDN CH D: Power-down channel D

Channel D is powered down.

Bit D2 PDN CH C: Power-down channel C

Channel C is powered down.

Bit D1 PDN CH B: Power-down channel A

Channel B is powered down.

Bit D0 PDN CH A: Power-down channel B

Channel A is powered down.



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS58H43 is a quad-channel, 11-bit, analog-to-digital converter (ADC) with sampling rates up to 250 MSPS. At every falling edge of the input clock, the analog input signal for each channel is sampled simultaneously. The sampled signal in each channel is converted by a pipeline of low-resolution stages. In each stage, the sampled-and-held signal is converted by a high-speed, low-resolution, flash sub-ADC. The difference (residue) between the stage input and its quantized equivalent is gained and propagates to the next stage. At every clock, each subsequent stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and digitally processed to create the final code, after a data latency of 10 clock cycles. The digital output is available in a double data rate (DDR) low-voltage differential signaling (LVDS) interface and is coded in binary twos complement format.

ANALOG INPUT

The analog input consists of a switched-capacitor-based differential sample-and-hold architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates.

The INP and INM pins must be externally biased around a common-mode voltage of 1.15 V, available on the VCM pin. For a full-scale differential input, each input pin (INP, INM) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing.

The input sampling circuit has a high 3-dB bandwidth that extends up to 500 MHz when a $50-\Omega$ source drives the ADC analog inputs.

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This configuration improves the common-mode noise immunity and even-order harmonic rejection. A 5- Ω to 15- Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics.

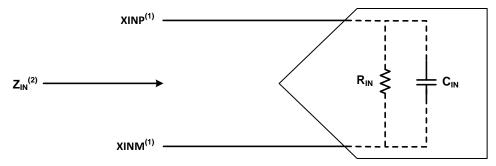
Spurious-free dynamic range (SFDR) performance can be limited because of several reasons (such as the effect of sampling glitches, sampling circuit nonlinearity, and quantizer nonlinearity that follows the sampling circuit). Depending on the input frequency, sampling rate, and input amplitude, one of these metrics plays a dominant part in limiting performance. At very high input frequencies, SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity typically limits performance.

Glitches are caused by opening and closing the sampling switches. The driving circuit should present a low source impedance to absorb these glitches, otherwise these glitches may limit performance. A low impedance path between the analog input pins and VCM is required from the common-mode switching currents perspective as well. This impedance can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

The ADS58H43 includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The R-C component values are also optimized to support high input bandwidth (up to 500 MHz). However, using an R-LC-R filter (refer to Figure 46, Figure 47, Figure 48, Figure 49, and Figure 50) improves glitch filtering, thus further resulting in better performance.

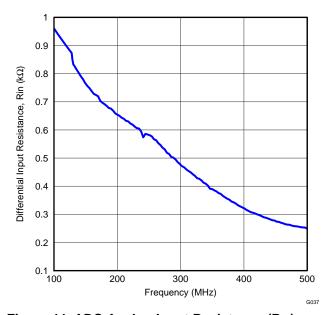
40

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched source impedance. In doing so, the ADC input impedance must be considered. Figure 43, Figure 44, and Figure 45 show the impedance ($Z_{IN} = R_{IN} \mid\mid C_{IN}$) at the ADC input pins.



- (1) X = A, B, C, or D.
- (2) $Z_{IN} = R_{IN} || (1 / j\omega C_{IN}).$

Figure 43. ADC Equivalent Input Impedance



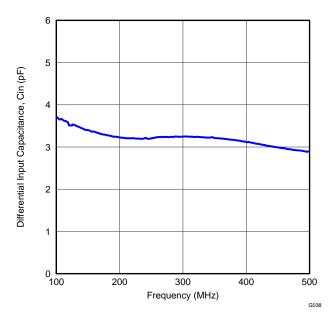


Figure 44. ADC Analog Input Resistance (R_{IN}) vs Frequency

Figure 45. ADC Analog Input Capacitance ($C_{\rm IN}$) vs Frequency



Driving Circuit

Two example driving circuits with a $50-\Omega$ source impedance are shown in Figure 46 and Figure 47. The driving circuit in Figure 46 is optimized for input frequencies in the second Nyquist zone (centered at 185 MHz), whereas the circuit in Figure 47 is optimized for input frequencies in third Nyquist zone (centered at 310 MHz).

Note that both drive circuits are terminated by 50 Ω near the ADC side. This termination is accomplished with a 25- Ω resistor from each input to the 1.15-V common-mode (VCM) from the device. This architecture allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals.

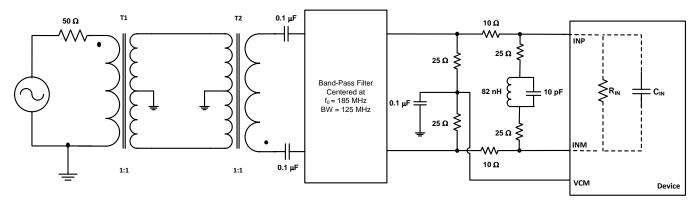


Figure 46. Driving Circuit for a 50- Ω Source Impedance and Input Frequencies in the Second Nyquist Zone

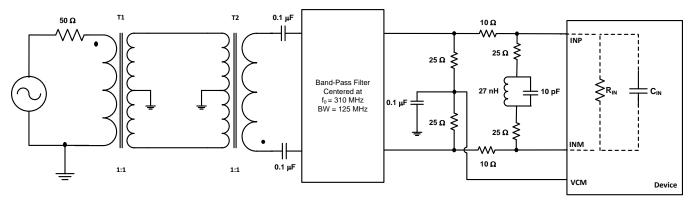


Figure 47. Driving Circuit for a 50- Ω Source Impedance and Input Frequencies in the Third Nyquist Zone

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Appropriate high-performance modes must be written to ensure best performance in a given Nyquist zone and source impedance. Table 6 summarizes all available high-performance modes.

Table 6. High-Performance	Modes	Summary ⁽¹⁾⁽²⁾
---------------------------	-------	---------------------------

			f _S = 245.	f _S = 184.32 MSPS			
ADDRESS (Hex)	DATA (Hex)	R _S = 50 ZONE = 2	R _S = 100 ZONE = 2	R _S = 50 ZONE = 3	R _S = 100 ZONE = 3	R _S = 50 ZONE = 2	R _S = 100 ZONE = 2
D4	80				√		
D5	80				√		
D6	80	\checkmark	√	√	√	√	
D7	0C	\checkmark	√	√		√	√
DB	30				√		
F0	38					√	√
F1	20	√		√		√	
F5	42				√		

- (1) R_S refers to the source impedance. Zone refers to the Nyquist zone in which the signal band lies. Zone = 2 corresponds to the signal band that lies between f_S / 2 and f_S . Zone = 3 corresponds to the signal band that lies between f_S and 3 x f_S / 2.
- (2) Best performance can be achieved by writing these modes depending upon source impedance, band of operation, and sampling speed.

Two example driving circuits with $100-\Omega$ differential termination are shown in Figure 48 and Figure 49. In these example circuits, the 1:2 transformer (T1) is used to transform the $50-\Omega$ source impedance into a differential 100 Ω at the input of the band-pass filter. In Figure 48, the parallel combination of two $68-\Omega$ resistors and one 120-nH inductor and two $100-\Omega$ resistors is used $(100-\Omega)$ is the effective impedance in pass-band) for better performance. The required high-performance modes for these applications are given in Table 6.

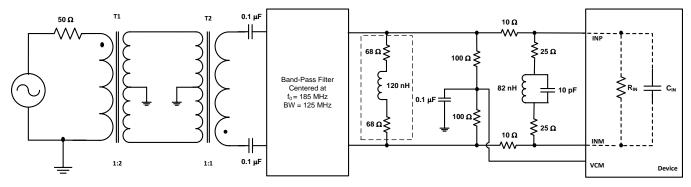


Figure 48. Driving Circuit for a 100-Ω Source Impedance and Input Frequencies in the Second Nyquist Zone

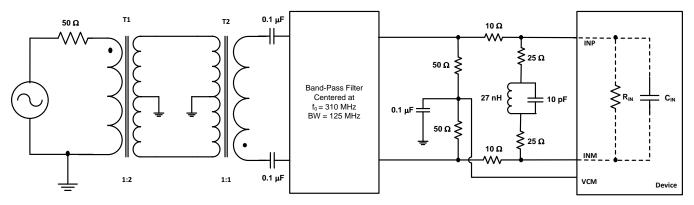


Figure 49. Driving Circuit for a 100-Ω Source Impedance and Input Frequencies in the Third Nyquist Zone

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Input Common Mode

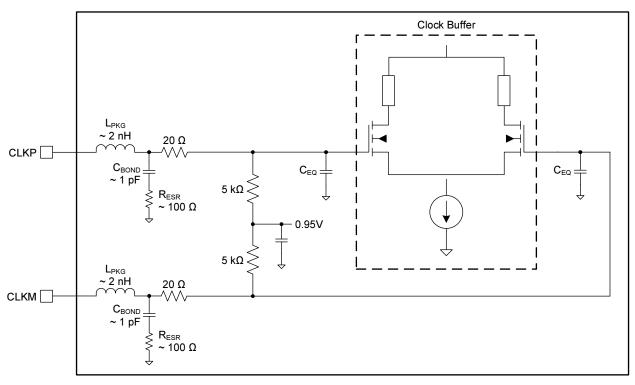
To ensure a low-noise, common-mode reference, the VCM pin should be filtered with a 0.1-μF low-inductance capacitor connected to ground. The VCM pin is designed to directly bias the ADC inputs (refer to Figure 46 to Figure 49).

Each ADC input pin sinks a common-mode current of approximately 1.5 μ A per MSPS of clock frequency. When a differential amplifier is used to drive the ADC (with dc-coupling), ensure that the output common-mode of the amplifier is within the acceptable input common-mode range of the ADC inputs (VCM \pm 25 mV).

Clock Input

The ADS58H43 clock inputs can be driven differentially with a sine, LVPECL, or LVDS source with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95 V using internal 5-k Ω resistors, as shown in Figure 50. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL, LVDS, and LVCMOS clock sources (see Figure 51, Figure 52, and Figure 53).

For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. TI recommends keeping the differential voltage between clock inputs less than 1.8 V_{PP} to obtain best performance. A clock source with very low jitter is recommended for high input frequency sampling. Bandpass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

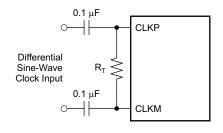


C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 50. Internal Clock Buffer

(1) R_T is the termination resistor (optional).

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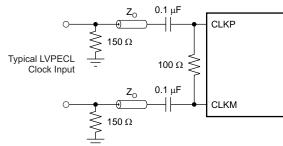


Figure 51. Differential Sine-Wave Clock Driving Circuit

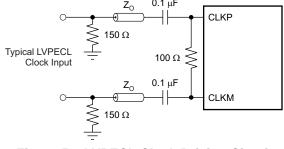


Figure 52. LVPECL Clock Driving Circuit

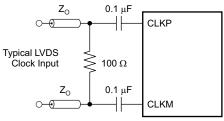




Figure 53. LVDS Clock Driving Circuit

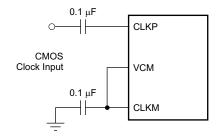


Figure 54. Typical LVCMOS Clock Driving Circuit

OVERVIEW OF OPERATING MODES

There are three available operating modes: 11-bit, 250-MSPS mode; 11-bit SNRBoost^{3G+}, 250-MSPS mode; and 14-bit, 250-MSPS mode (burst mode). Table 7 shows a summary of the operating modes.

Table 7. Operating Mode Summary

		RESULTING MODE OF OPERATION				
PIN SETTING	REGISTER SETTING	CHANNELS A AND B	CHANNELS C AND D			
Default (after power up)	_	11 bit, 250 MSPS	11 bit, 250 MSPS			
	_	SNRBoost ^{3G+} , 90 MHz	SNRBoost ^{3G+} , 90 MHz			
Set SNRB pin high	Set SNRB 45/95MHz bit (register 42h, value 4h)	SNRBoost ^{3G+} , 45 MHz	SNRBoost ^{3G+} , 45 MHz			
Set SNRB pin high	Set BMODE EN CH AB bit (register 44h, value 40h)	Burst mode: Low resolution = 11 bits at 250 MSPS High resolution = 14 bits at 250 MSPS	SNRBoost ^{3G+} , 90 MHz			
Set SNRB pin high	Set BMODE EN CH CD bit (register 44h, value 80h)	SNRBoost ^{3G+} , 90 MHz	Burst mode: Low resolution = 11 bits at 250 MSPS High resolution = 14 bits at 250 MSPS			
Set SNRB pin low (default)	Set both BMODE EN CH AB and BMODE EN CH CD bits (register 44h, value C0h)	Burst mode: Low resolution = 11 bits at 250 MSPS High resolution = 14 bits at 250 MSPS	Burst mode: Low resolution = 11 bits at 250 MSPS High resolution = 14 bits at 250 MSPS			

11-Bit, 250-MSPS Mode: Output of the 11 MSBs on the digital DDR LVDS interface.

11-Bit SNRBoost^{3G+}, 250-MSPS Mode: 11-bit output using SNRBoost^{3G+} signal processing.

- 90-MHz wide (centered on f_S / 4)
- 45-MHz wide (centered on f_S / 8 and 3 f_S / 8)

14-Bit, 250-MSPS (Burst) Mode: In burst mode, the 14-bit, 250-MSPS digital output data stream alternates between high resolution (14-bit) and low resolution (11-bit). The high-resolution sample can be transmitted using the burst trigger input (TRIG EN). The HIRES output flag indicates high-resolution data. The amount of highresolution samples is programmable.

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There are two different options available in burst mode: auto-trigger and manual-trigger.

- Auto-Trigger Mode: After transmission of the final low-resolution sample, the ADS58H43 immediately begins sending the high-resolution samples. However, auto-trigger mode requires an initial trigger at the TRIG_EN pin to start the high-resolution process. Thereafter, all subsequent triggers are automated.
- Manual-Trigger Mode: After transmission of the final low-resolution sample, the ADS58H43 is ready for the
 manual trigger of a high-resolution data burst indicated by the TRIG_RDY flag. The high-resolution samples
 are triggered every time by the rising edge of the pulse on the TRIG_EN pin.

The default mode of operation is 11-bit resolution. A set of two channels (channels A and B and channels C and D) can be in either SNRBoost^{3G+} mode or in burst mode, separately.

SNRBoost^{3G+} can be enabled by the SNRB pin or by the SPI bit (SNRB PIN OVRD). However, burst mode can only be enabled by using an SPI register bit. In burst mode, the automatic trigger can be enabled by setting the SPI register bit AUTO BURST ENABLE (register 41h, bit 0) and the manual trigger can be enabled through the TRIG_EN pin. Table 7 summarizes the process for enabling SNRBoost^{3G+} from pin settings and enabling burst mode from the SPI registers on different channels.

Burst Mode

After enabling burst mode, the device is limited to 11-bit (low-resolution) samples until a trigger is asserted through the TRIG_EN pin. A TRIG_EN rising edge causes the device to output a set of 14-bit (high-resolution) samples, followed by another set of 11-bit (low-resolution) samples.

In auto-trigger mode (set using the SPI register), this cycle repeats as long as the device is in burst mode. In manual-trigger mode, this cycle is followed by a delay until the next rising edge on the TRIG_EN pin occurs. During this cycle (high-resolution samples followed by low-resolution samples), any edge on TRIG_EN is ignored.

The HIRES output flag is set high when the device outputs high-resolution, 14-bit data; otherwise, HIRES is '0'. The TRIG_RDY output flag is set high while the device waits for a rising edge on the TRIG_EN pin; otherwise, this flag is cleared.

The ratio of high-resolution, 14-bit samples to low-resolution, 11-bit samples is programmable between 1:8 and 1:64. The number of high-resolution, 14-bit samples is also programmable.

The number of 14-bit, high-resolution samples is shown in Equation 3: 2^{10 + NH}

where:

$$0 \le \mathsf{NH} \le 15 \tag{3}$$

The number of 11-bit, low-resolution samples is shown in Equation 4: $2^{13 + NH + NL}$

where:

$$0 \le \mathsf{NL} \le 3 \tag{4}$$

Both NH and NL parameters can be programmed through the SPI at any time, but are internally updated at the end of the high-resolution data transmission.

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Manual-Trigger Mode

Figure 55 shows a timing diagram for this mode.

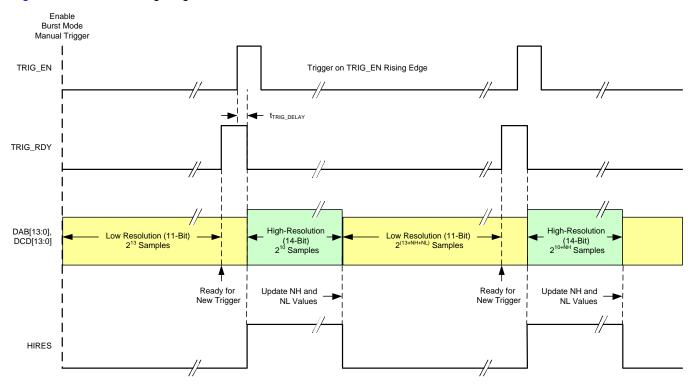


Figure 55. Timing For Manual-Trigger Mode

Auto-Trigger Mode

In this mode, the output data cycles automatically between 11-bit and 14-bit resolution, as shown in Figure 56. After the first rising edge of the pulse on TRIG_EN that turns the 14-bit burst mode on, the device continues to provide high-resolution samples interlaced with low-resolution samples and any subsequent edge on TRIG_EN is ignored. The TRIG_RDY output flag is invalid in this mode.

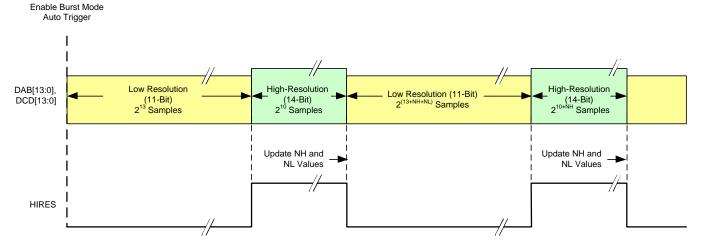


Figure 56. Timing for Auto-Trigger Mode

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Overrange Indication (OVRxx)

The ADS58H43 outputs overrange information on the Dxx0P and Dxx0M pins (where xx = channels A and B or channels C and D) of the digital output interface. When transmitting high-resolution (14-bit) output data in burst mode, Dxx0P and Dxx0M transmit the output data LSB instead. An OVR timing diagram is shown in Figure 57.

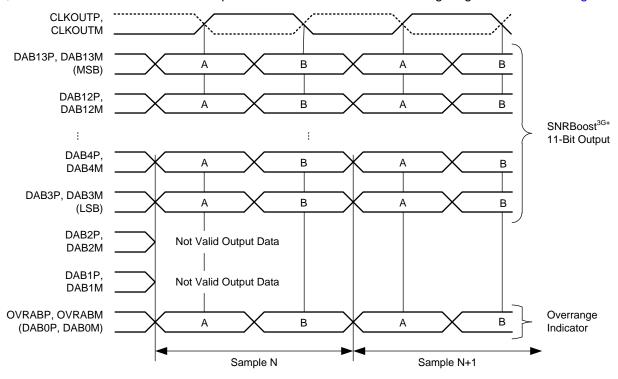


Figure 57. Overrange Indicator (OVR) Timing

Normal overrange indication (OVR) shows the event of the ADS58H43 digital output being saturated when the input signal exceeds the ADC full-scale range. Normal OVR has the same latency as digital output data. However, an overrange event can be indicated earlier (than normal latency) by using the fast OVR mode. The fast OVR mode (enabled by default) is triggered seven clock cycles after the overrange condition that occurred at the ADC input. The fast OVR thresholds are programmable with the FAST OVR THRESH PROG bits (refer to Table 4, register address C3h). At any time, either normal or fast OVR mode can be programmed on the Dxx0P and Dxx0M pins. A block diagram indicating required register writes to enable OVR is shown in Figure 58.

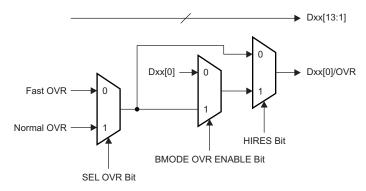


Figure 58. OVR Block Diagram

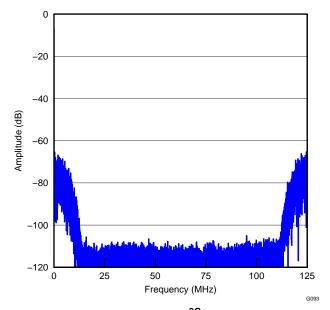
48

SNRBoost^{3G+} Implementation

There are two possible filter configurations in SNRBoost $^{3G+}$ mode. The SNRBoost $^{3G+}$ bandwidth can be set to 90 MHz (Figure 59) or 45 MHz (Figure 60). In the 45-MHz mode, there are two 45-MHz filter bands available simultaneously. One band is centered on f_S / 8 (low side) and the other band is centered on 3 f_S / 8 (high side). The filter configurations are detailed in Table 8.

Table 8. SNRBoost^{3G+} Filter Configurations

	CORNER FR	EQUENCIES	
BANDWIDTH (MHz)	START	STOP	CENTER FREQUENCY
90	0.06 × f _S	0.44 × f _S	f _S / 4
45 (low side)	0.03 × f _S	0.216 × f _S	f _S / 8
45 (high side)	0.286 × f _S	0.466 × f _S	3 × f _S / 8



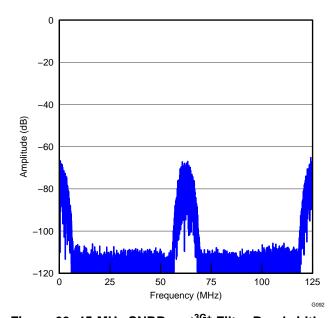


Figure 59. 90-MHz SNRBoost^{3G+} Filter Bandwidth Centered on f_S / 4

Figure 60. 45-MHz SNRBoost $^{3G+}$ Filter Bandwidth Centered on f $_{\rm S}$ / 8 and 3 f $_{\rm S}$ / 8

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Product Folder Links: ADS58H43



GAIN FOR SFDR AND SNR TRADE-OFF

The ADS58H43 includes gain settings that can be used to obtain improved SFDR performance. The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps) using the DIGITAL GAIN CH X register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 9.

Table 9. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V _{PP})
0	Default after reset	2
1	Fine, programmable	1.78
2	Fine, programmable	1.59
3	Fine, programmable	1.42
4	Fine, programmable	1.26
5	Fine, programmable	1.12
6	Fine, programmable	1

SFDR improvement is achieved at the expense of SNR; for each gain setting, SNR degrades by approximately 0.5 dB to 1 dB. SNR degradation is diminished at high input frequencies. As a result, the fine gain is very useful at high input frequencies because SFDR improvement is significant with marginal degradation in SNR. Therefore, fine gain can be used to trade-off between SFDR and SNR.

After a reset, the gain function is disabled. To use fine gain:

- First, program the DIGITAL ENABLE bits to enable digital functions.
- This setting enables the gain for all four channels and places the device in a 0-dB gain mode.
- For other gain settings, program the DIGITAL GAIN CH X register bits.

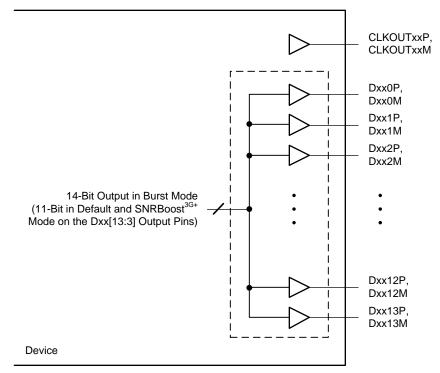
DIGITAL OUTPUT INFORMATION

The ADS58H43 provides 11-bit (or 14-bit in burst mode) digital data for each channel and two output clocks in LVDS mode. Output pins are shared by a pair of channels that are accompanied by one dedicated output clock.

DDR LVDS Outputs

In the LVDS interface mode, the data bits and clock are output using LVDS levels. The data bits of two channels are multiplexed and output on each LVDS differential pair of pins; see Figure 61 and Figure 62.

Submit S



NOTE: xx = channels A and B or C and D.

Figure 61. DDR LVDS Interface

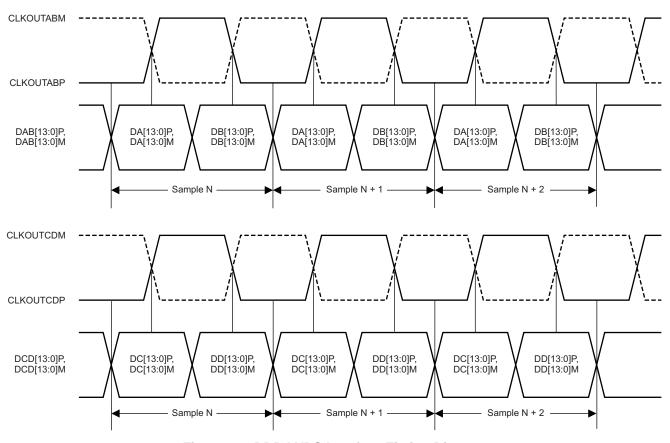


Figure 62. DDR LVDS Interface Timing Diagram



LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in Figure 63. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100- Ω termination.

The V_{DIFF} voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100- Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits (refer to Table 4, register address 01h). The buffer output impedance behaves similar to a source-side series termination. By absorbing reflections from the receiver end, the source-side termination helps to improve signal integrity.

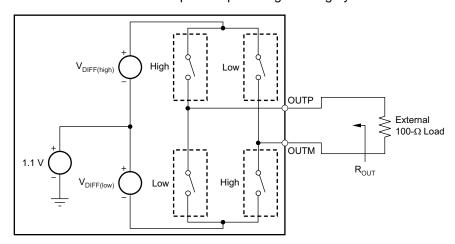


Figure 63. LVDS Buffer Equivalent Circuit

Output Data Format

The ADS58H43 transmits data in binary twos complement format. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 3FFh. For a negative input overdrive, the output code is 400h.

BOARD DESIGN CONSIDERATIONS

For evaluation module (EVM) board information, refer to the ADS58H40 EVM User's Guide (SLAU455).

Grounding

A single ground plane is sufficient to provide good performance, as long as the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS58H40 EVM User's Guide* (SLAU455) for details on layout and grounding.

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DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) - The sample-to-sample variation in aperture delay.

Clock Pulse Width and Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate - The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC actual input full-scale range from the ideal value. Gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN} .

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5 / 100) \times f_{S ideal}$ to $(1 + 0.5 / 100) \times f_{S ideal}$

Offset Error – Offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX} . The coefficient is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} - T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N) , excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N}$$
 (5)

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D}$$
 (6)

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
ADS58H43IZCR	Active	Production	NFBGA (ZCR) 144	184 JEDEC	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS58H43I
				TRAY (10+1)					
ADS58H43IZCR.A	Active	Production	NFBGA (ZCR) 144	184 JEDEC	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS58H43I
			` ''	TRAY (10+1)					
ADS58H43IZCRR	Active	Production	NFBGA (ZCR) 144	1000 LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS58H43I
ADS58H43IZCRR.A	Active	Production	NFBGA (ZCR) 144	1000 LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS58H43I

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS58H43IZCRR	NFBGA	ZCR	144	1000	330.0	24.4	10.25	10.25	2.25	16.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
AE	S58H43IZCRR	NFBGA	ZCR	144	1000	350.0	350.0	43.0	



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TRAY

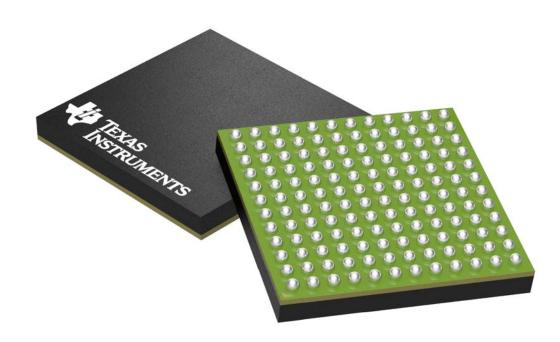


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

	Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	Κ0 (μm)	P1 (mm)	CL (mm)	CW (mm)
j	ADS58H43IZCR	ZCR	NFBGA	144	184	8 x 23	150	315	135.9	7620	13.4	10.1	19.65
-	ADS58H43IZCR.A	ZCR	NFBGA	144	184	8 x 23	150	315	135.9	7620	13.4	10.1	19.65

10 x 10 mm, 0.8 mm pitch

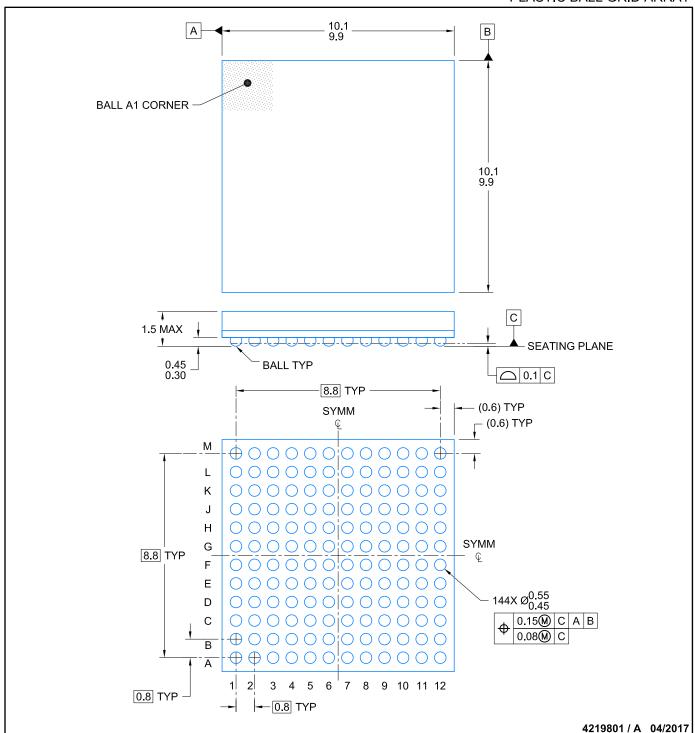


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC BALL GRID ARRAY

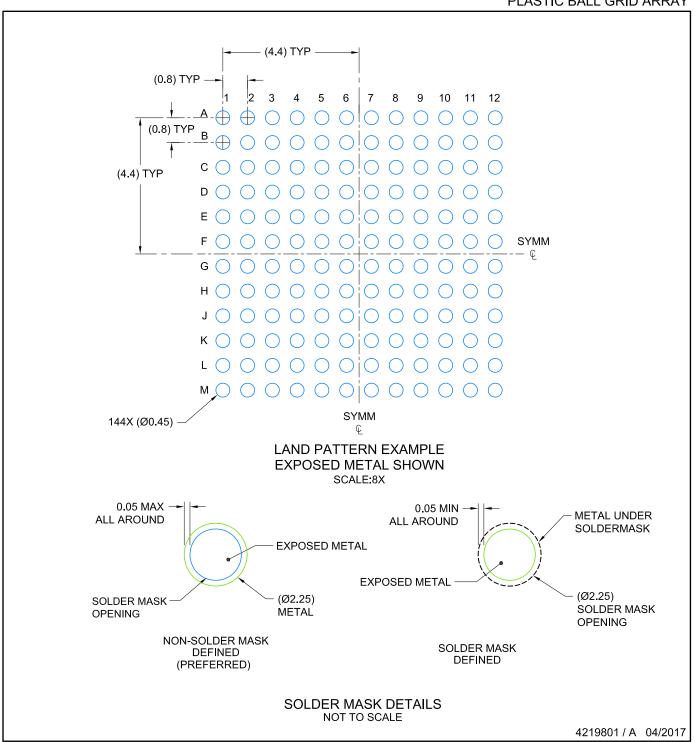


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.

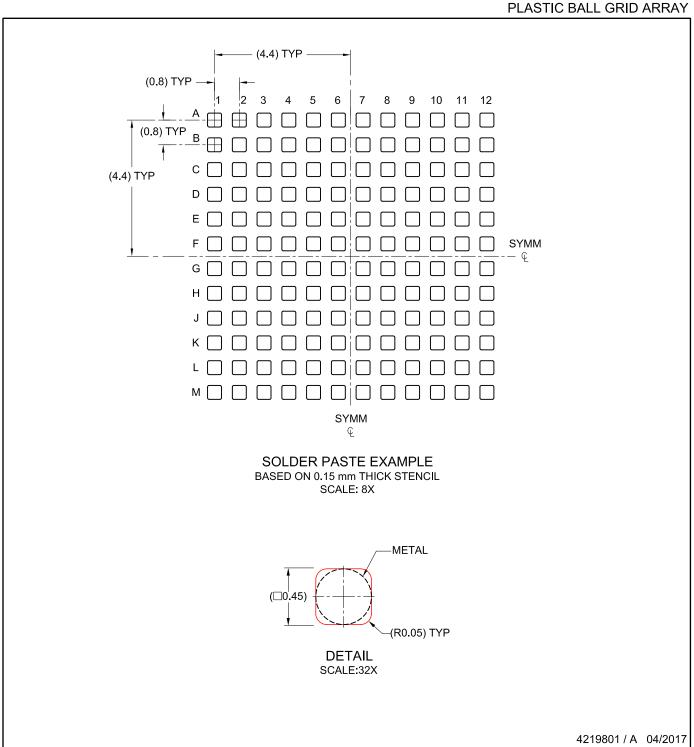


PLASTIC BALL GRID ARRAY



NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SPRAA99 (www.ti.com/lit/spraa9).



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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